COLUTA: Custom 8-Channel 15-bit 40-MSPS ADC for the ATLAS Liquid Argon Calorimeter Readout

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***Abstract*—The stringent radiation-tolerance, quantization requirements, and the need for seamless integration of the on-detector readout electronics chain require the design of a *full-custom* analog-to-digital converter (ADC) for the 182,468 channels in the ATLAS Liquid Argon (LAr) calorimeter at the Large Hadron Collider (LHC) at CERN, as part of the High-Luminosity LHC (HL-LHC) upgrade. Each of the 8 channels in the prototype 65 nm CMOS ADC with 15-bit resolution and >68 dB signal-to-noise-and-distortion ratio (SNDR), or equivalently >11 effective number of bits (ENOB), consists of a Multiplying-DAC (MDAC) and a successive-approximation (SAR) ADC. A digital data processing unit (DDPU) calibrates and serially transmits the quantized data. Initial lab characterization of 18 chips shows a minimum SNDR of 69.5 dB at full-scale at about 5 MHz and a maximum power consumption of 1.17 W; differential non-linearity (DNL) measurements show no missing codes. Additional validation of the ADC is ongoing before approximately 70k chips can be mass-produced for the upgrade.**

***Index Terms*—radiation-hard by design (RHBD), front-end board 2 (FEB2), digitizer, quantizer, application-specific integrated circuit (ASIC)**

I. Introduction

THE development of new readout electronics for the ATLAS LAr calorimeter is necessary to meet the physics goals in the demanding HL-LHC conditions, with up to 200 proton-proton (pp) collisions per bunch crossing at the bunch crossing rate of 40 MHz. The HL-LHC LAr calorimeter electronics upgrade [1] includes development of a full-custom ADC, dubbed 'COLUTA', to digitize each calorimeter channel after pre-amplification and pulse shaping. The ADC, designed in 65 nm CMOS, must quantize at a rate of 40 MSPS, achieve a minimum of 68 dB SNDR or 11 ENOB, and have at minimum a 14-bit resolution.

A key challenge in developing the LAr on-detector electronics is that they must be radiation-tolerant up to a total ionizing dose (TID) of 1.3 kGy, a total non-ionizing energy loss (NIEL) equivalent to 4.3×10^{13} neutrons/cm^2, and a total number of hadrons capable of producing single-event-effects (SEE) of 1.1×10^{13} h/cm^2. These requirements limit the potential use of commercial-off-the-shelf (COTS) components and therefore custom ASICs that can directly interface with each other must be used. Custom ASICs have been used in past upgrades, such as an ADC with similar specifications but with a lower resolution requirement [2] for the trigger path. Fig. 1 depicts the required custom ASICs for the HL-LHC ATLAS LAr readout: a preamplifier/shaper ASIC (ALFE) developed in 130 nm CMOS, the 65 nm ADC discussed in this paper, and a 10 Gbps serializer/transceiver (lpGBT) ASIC [3] used to multiplex, optically transmit ADC data off-detector for digital processing, and to provide clock and control functions.

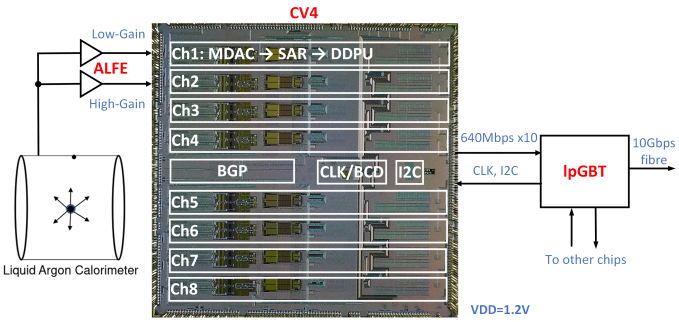

Fig. 1: *COLUTA ADC version 4 in the context of the LAr readout system and a photograph of the 5.5mm x 5.8mm 8-channel 65 nm CMOS ADC die. Connections to only two ADC channels are depicted.*

The COLUTA ADC is currently in its fourth design stage (CV4), serving as the full-functionality final prototype. This paper first presents how the analog performance, radiation hardness, and seamless integration requirements are met by design. Next, preliminary measurements are shown which demonstrate that the CV4 satisfies the performance requirements. CV4 radiation and integration tests are currently planned, though previous measurements with the preceding CV3 demonstrate satisfactory results. Once the full validation of CV4 is completed, the mass production of about 70k chips will be launched for use in the LAr HL-LHC upgrade.

II. Design Overview

Fig. 1 shows the CV4 in the context of the LAr on-detector readout system. The analog signal from each calorimeter channel goes into the ALFE, the shaped outputs of which are then differentially sampled and digitized by the CV4. The ALFE maps one LAr detector channel to two CV4 channels, one with "low-gain" and the other with "high-gain". The digitized data is then multiplexed and transmitted at 10 Gbps from the lpGBT. There are eight identical-by-design digitizer channels within the CV4, in addition to shared blocks such as reference/bias generation (BGP), I^{2}C digital slow-control, and timing distribution (CLK/BCD). Each channel contains an MDAC, SAR, and a DDPU for applying calibrated bit-weights and presenting the data in a way that is compatible with the lpGBT. Radiation-hardened-by-design techniques are applied where all digital logic is triply-redundant using the TMRG

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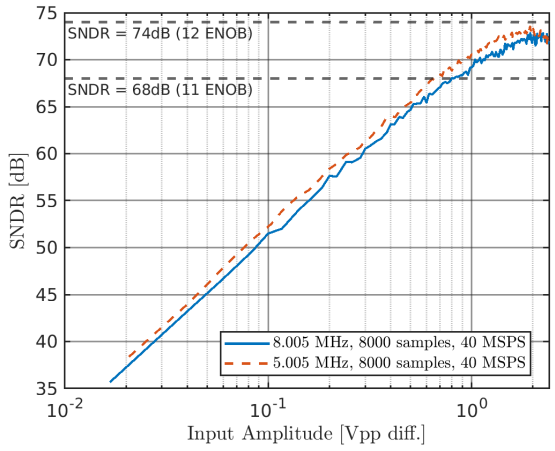

Fig. 2: *SNDR versus input amplitude.*

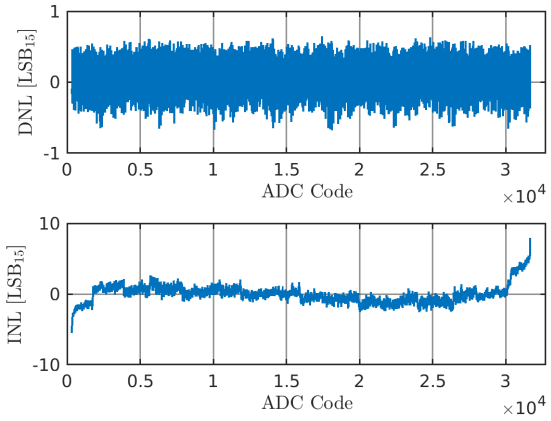

Fig. 3: *Measured INL and DNL using a sinusoid.*

tool [4] to decrease the probability of radiation-induced bit-flips. Interfacing the three ASICs (ALFE, CV4, lpGBT) does not require additional components in the signal path that could otherwise present a vulnerability to radiation induced effects.

The analog performance is achieved by redundancy [5], sufficient sizing of the input sampling capacitor, and integration of individual reference buffers for the MDAC and SAR in each channel. The MDAC produces 3-bits of quantization and has a gain of 4 V/V which provides 1-bit of redundancy between the MDAC and the downstream SAR. The SAR consists of two capacitive-DAC (cap-DAC) stages and an inter-stage residue amplifier and outputs a 13-bit code after considering redundancy. The 3-bit MDAC code, minus 1-bit of MDAC+SAR redundancy, and the 13-bit SAR code satisfy the >14-bit resolution requirement. Furthermore, the built-in redundancy makes the analog signal path tolerant to errors such as comparator offset; it is also necessary for the foreground calibration process. The MDAC sampling capacitor of 4 pF differential has a kT/C noise of 32 μVrms which is a fraction of the V_{LSB} (15-bits over 2 Vpp diff.) of 61 μV diff. This ensures that the input-referred noise does not significantly degrade the overall 15-bit resolution. Lastly, the 8 separate SAR and 8 separate MDAC reference buffers minimize channel-to-channel interference and ensure sufficient settling of the quantization voltage reference.

Metric	Units	Specification	Measurement
Input full-scale	[Vpp diff.]	2	
Sampling rate	[MSPS]	40	
Resolution	[bits]	14	15
SNDR min/max	[dB]	68.0	69.5/73.0
SFDR min/max	[dB]	—	80.3/87.9
Power cons. min/max	[W]	minimize	1.11/1.17
Input referred noise	[μV rms]	—	70.2
DNL min/max	[LSB_{15}]	-1.00/+1.00	-0.67/+0.65
INL min/max	[LSB_{15}]	—	-5.51/+7.98

TABLE I: *CV4 performance summary. SNDR, SFDR, and power consumption were measured across 18 packaged chips with a 5.005 MHz full-scale sinusoid input.*

III. Measurements

Table I summarizes the static and dynamic performance and Fig. 2 presents a SNDR versus amplitude for an input sinusoid applied to the MDAC input using a 50Ω passive unbalanced-to-balanced transformer input network. All measurements are done after an initial calibration procedure that is scalable across the entire readout infrastructure because the procedure is the same for every chip. The resulting calibration weights fluctuated by a few LSB's at most over a continuous duration of 68 hours at approximately the same ambient conditions as for the final installation. The frequencies 5.005 MHz and 8.005 MHz were chosen because the spectral content of the LAr pulse shape lies predominantly within this range; both exceed the 68dB SNDR requirement at full input range. Testing of the 18 packaged chips yielded consistent performance. Fig. 3 shows no missing codes over the entire input range. The measured integral non-linearity (INL) exceeds $\pm$1 LSB and the maximum SNDR for a sinusoidal input is distortion limited to <12 ENOB. This is sufficient for the targeted application while the extra resolution aids in the reconstruction of the LAr pulse shape. Validation of the ALFE chip driving the MDAC is ongoing.

IV. Conclusions

We have presented the design, integration, and performance of a custom 8-channel ADC intended to address challenges in upgrading the ATLAS LAr readout electronics for the HL-LHC environment. The upgraded readout electronics are intended to not only survive the higher radiation levels but also provide finer quantization than previous generations. Past design phases of the COLUTA ADC demonstrated satisfactory radiation and integration results; the same is expected for CV4. Once the analog performance, radiation, integration with the ALFE and lpGBT, and BGA package studies are concluded, the CV4 chip will be ready for mass production of ∼70k devices for use in the LAr HL-LHC upgrade.

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