PRIMA The PRobe far-Infrared Mission for Astrophysics

Spaceflight KID Readout Electronics Development for PRIMA

Sumit Dahal (NASA Goddard Space Flight Center)

21 June 2024
Paper 13102-56

Other PRIMA Talks and Posters at SPIE

Mission Science and Instrument Overview (in Space Telescope and Instrumentation 2024 Optical Infrared and Millimeter-wave

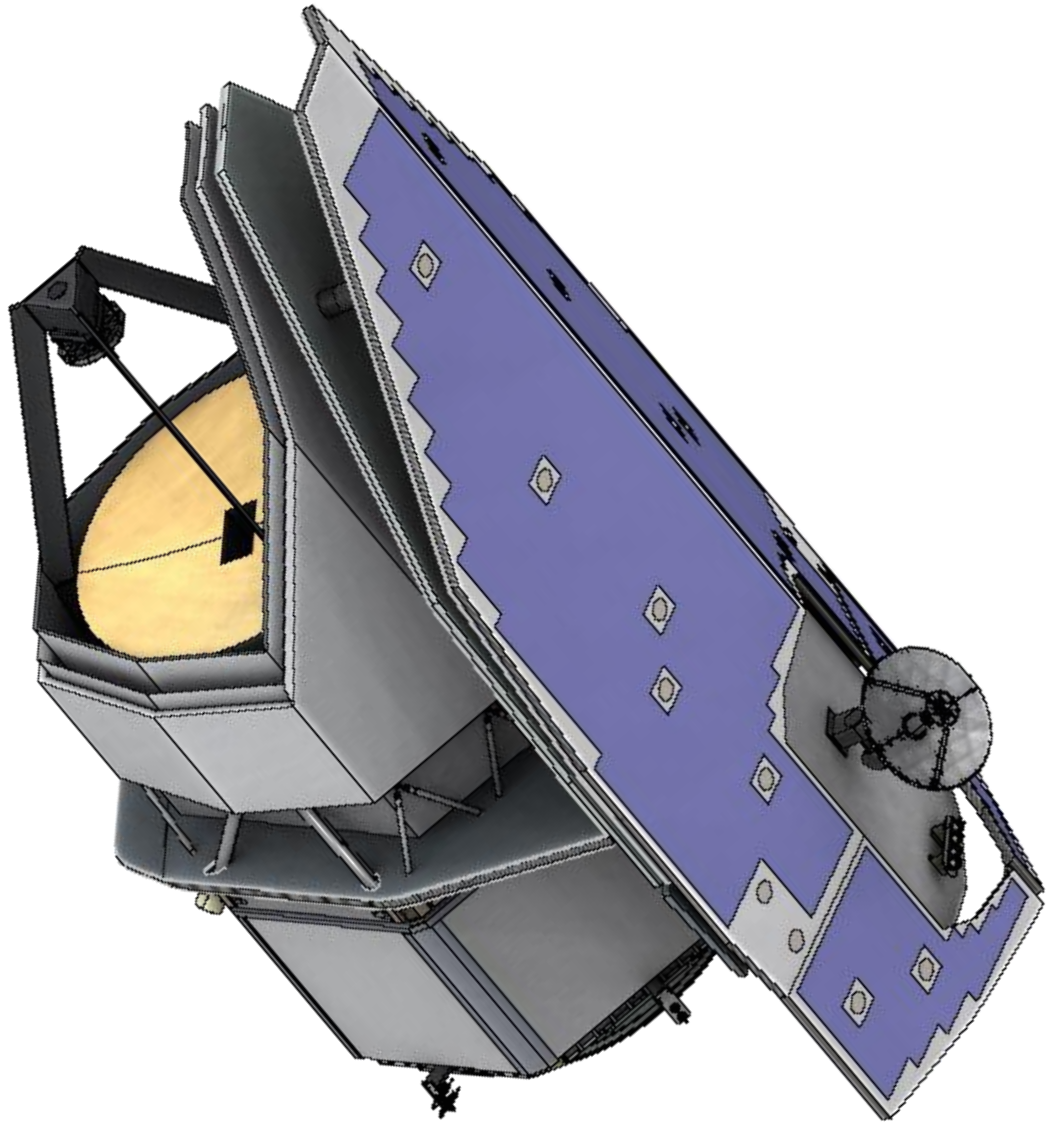
Jason Glenn	PRIMA Overview	Sunday, June 16, 17:00-17:20	G303/304 North -3F
Laure Ciesla	PRIMAger	Sunday, June 16, 17:20-17:40	G303/304 North -3F
Matt Bradford	FIRESS	Sunday, June 16, 17:40-18:00	G303/304 North -3F
Denis Burgarella	(poster) PRIMAGer science	Monday, June 17 17:30-19:00	G5, North -1F

PRIMA Technology (in Millimeter, Submillimeter, and Far-Infrared Detectors and Instrumentation for Astronomy XII)

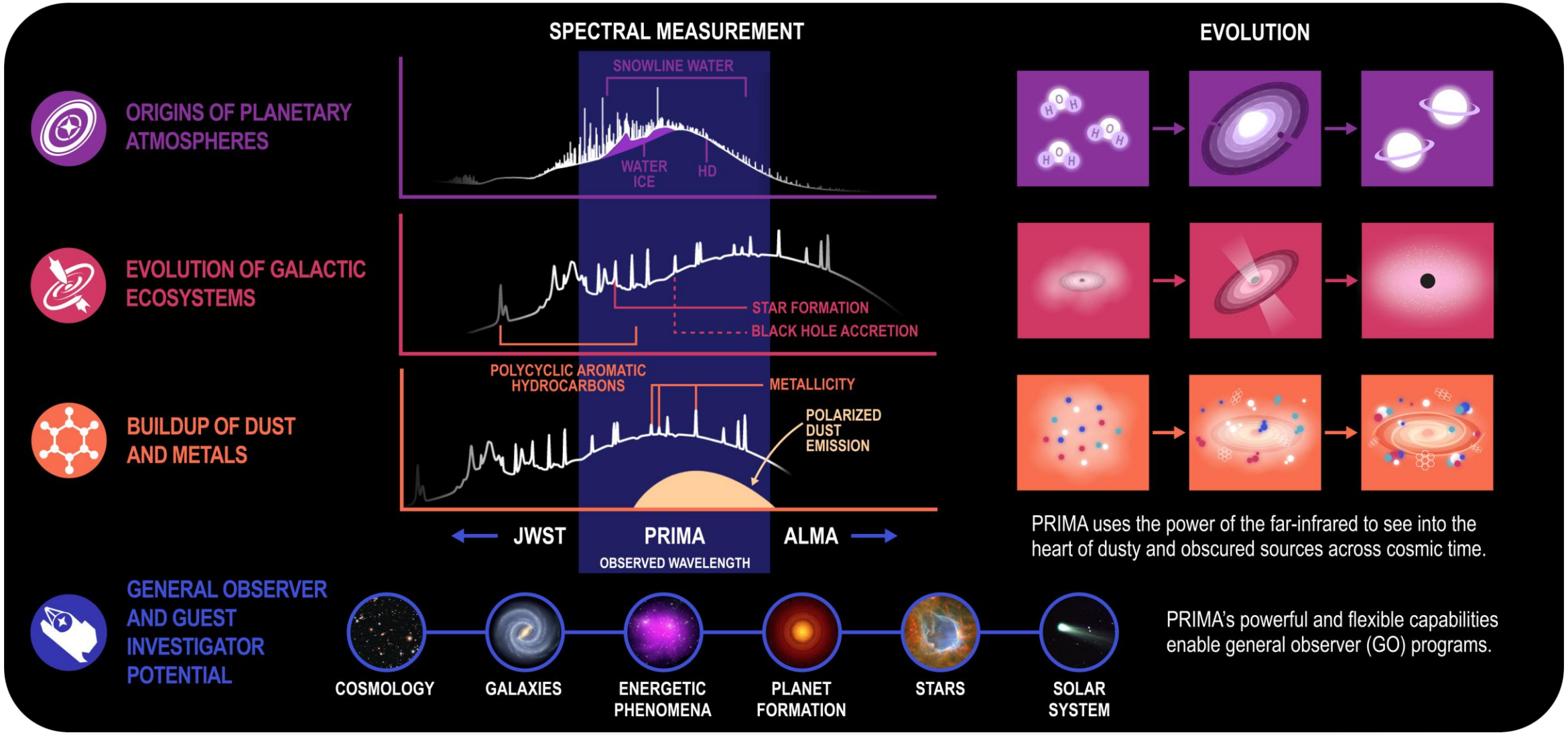
Nick Cothard	Microlens array development	Wednesday, June 19, 15:50-16:10	G318/319, North -3F
Shahab Dabironezare	PRIMAger absorber coupled architecture	Thursday, June 20, 15:50-16:10	G318/319, North -3F
Logan Foote	PRIMA / FIRESS detectors & 25-micron array	Wednesday, June 19, 15:00-15:20,	G318/319, North -3F
Willem Jellema	Linear variable filters for PRIMAger	Friday, June 21, 15:50-16:10	G318/319, North -3F
Chris Albert	(poster) Single-photon work and pixel identification	Wednesday, June 19, 17:30-19:00	G5, North -- 1F
Mike DiPirro	(poster) PRIMA sub-Kelvin cooler.	Monday, June 17, 17:30-19:00	G5, North -1F
Elijah Kane	(poster) 200 micron brassboard yield and NEP	Tuesday, June 18, 17:30-19:00	G5, North – 1F

What is PRIMA?

Telescope	1.8-m, all aluminum, 4.5 Kelvin
PRIMAger Imager & polarimeter	R = 10 hyperspectral imaging, 25-80 μm R= 4 imaging & polarimetry, 91-261 μm
FIRESS Spectrometer	R > 85 spectroscopy, 24-235 μm High-Res mode, R = 4,400 x ($\lambda/112\mu$m)
Detectors	100 mK KID arrays (~11k total)
Data	IPAC
Orbit	Earth-Sun L2
Launch	2032
Observations	75% GO, 25% PI (→ GI)



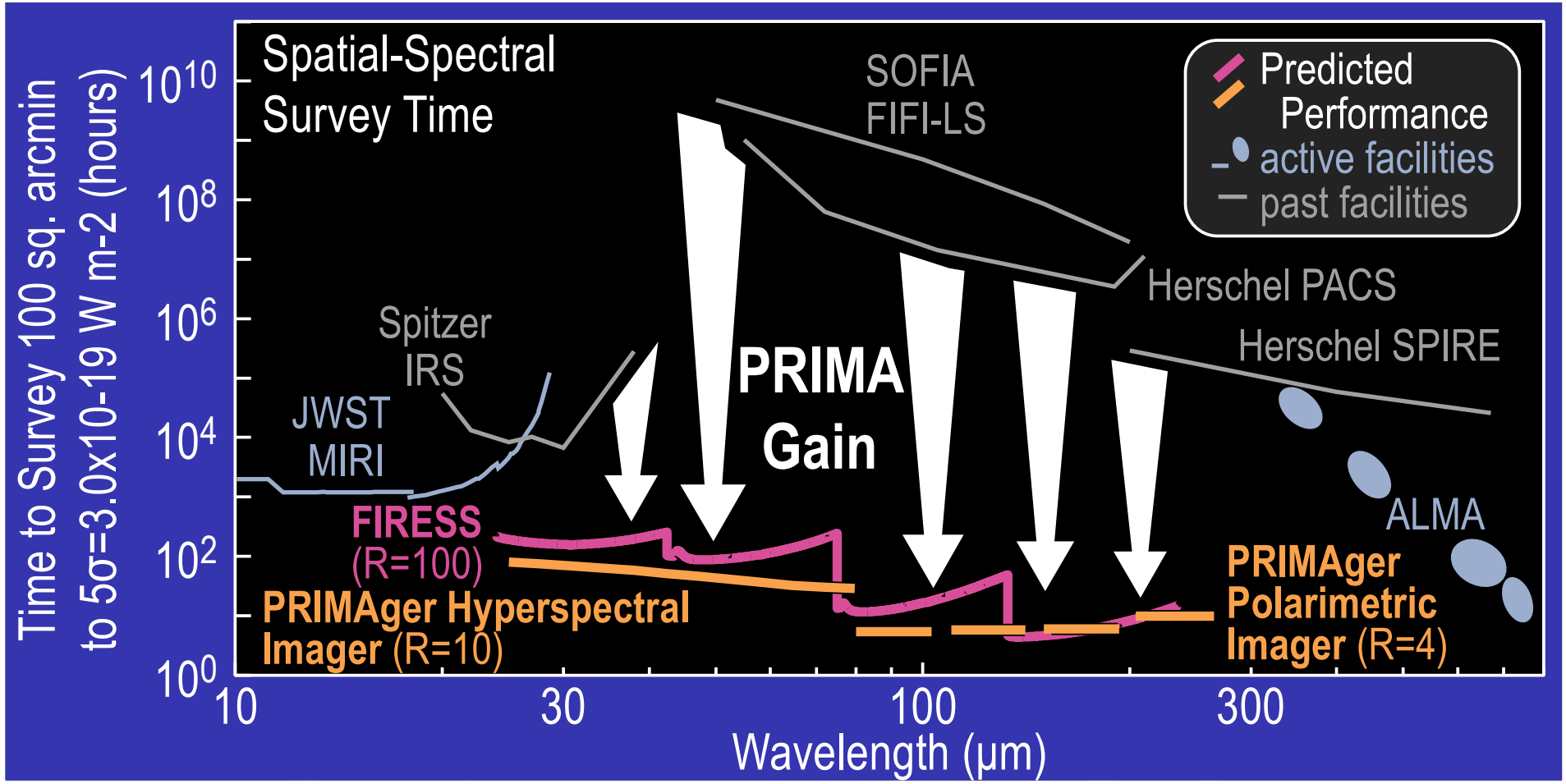
PRIMA PI Science Addresses Decadal Survey Priorities



PI Science is 25% of time, with 75% devoted to General Observer (GO) program

Large Gains and New Capabilities from Sensitive KID Arrays

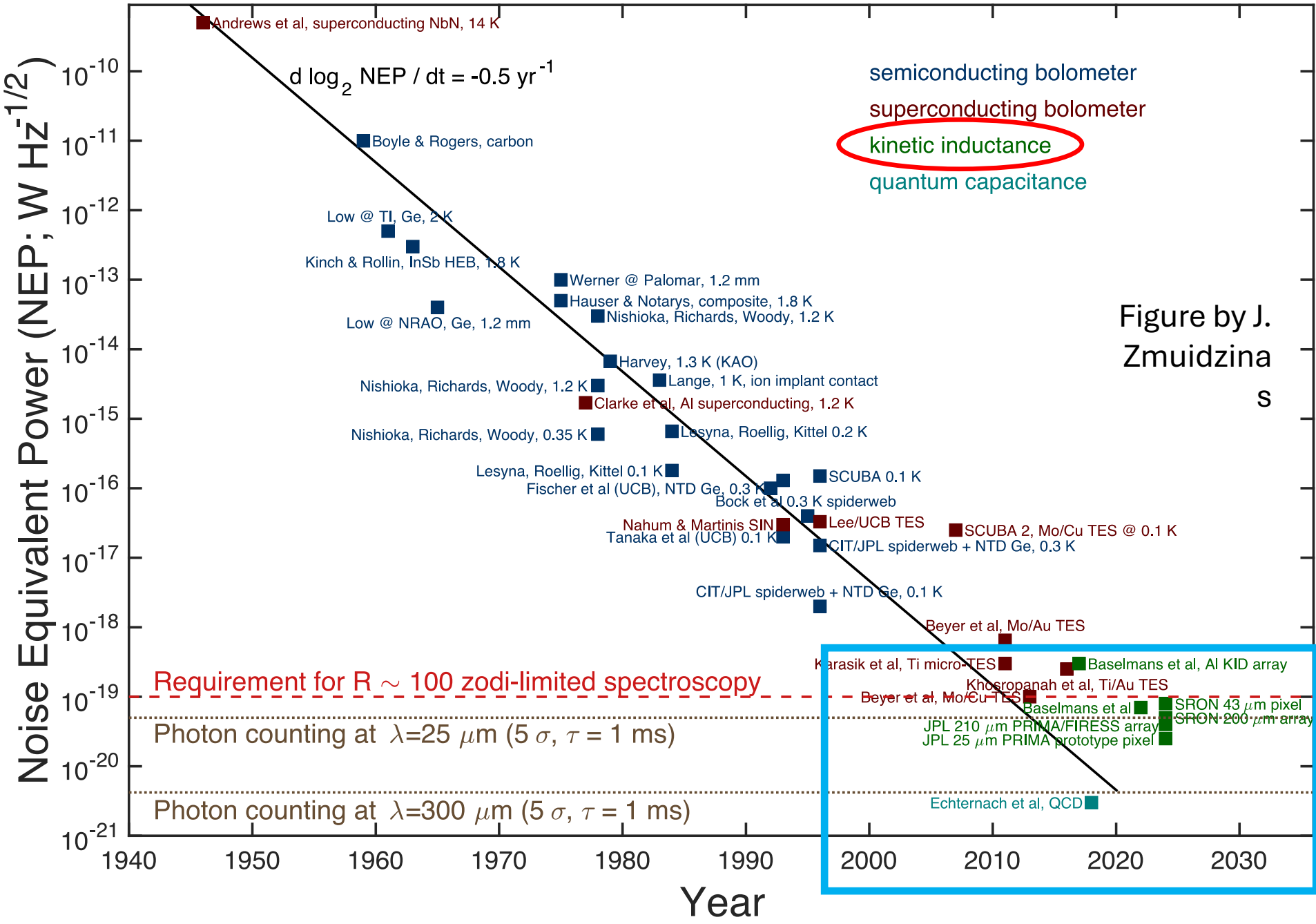
- Extended-source and "blind" spectral mapping
- Extensive polarimetric mapping
- Deep all-sky far-IR survey



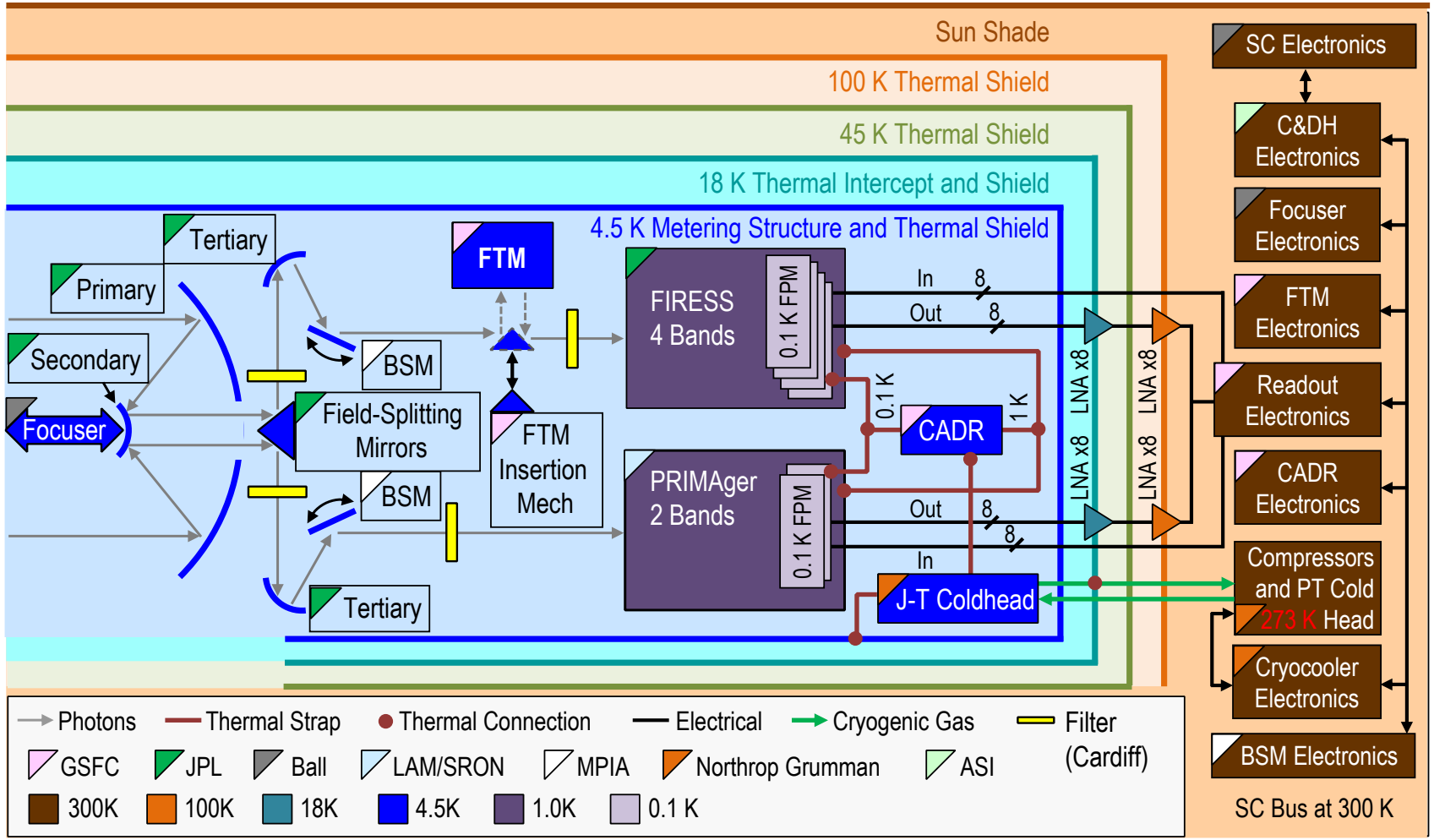
Stepping Back: Far-IR Detector Technological Readiness

Sensitivities of far-IR detectors have doubled approx. every two years for 75 years!

Probe region of interest



Payload Block Diagram



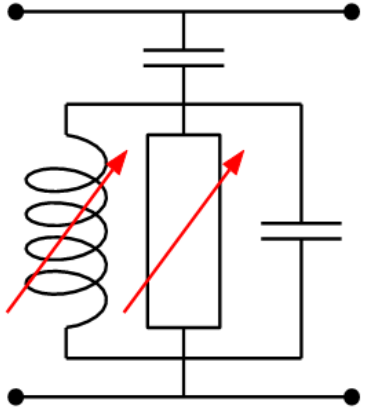
PRIMA provides required sensitivities by utilizing a 4.5K, 1.8-m cryogenic primary mirror, 1K instrument optics, and 0.1K ultra-sensitive KID detector arrays. Multiple organizations provide expertise to enable PRIMA's science.

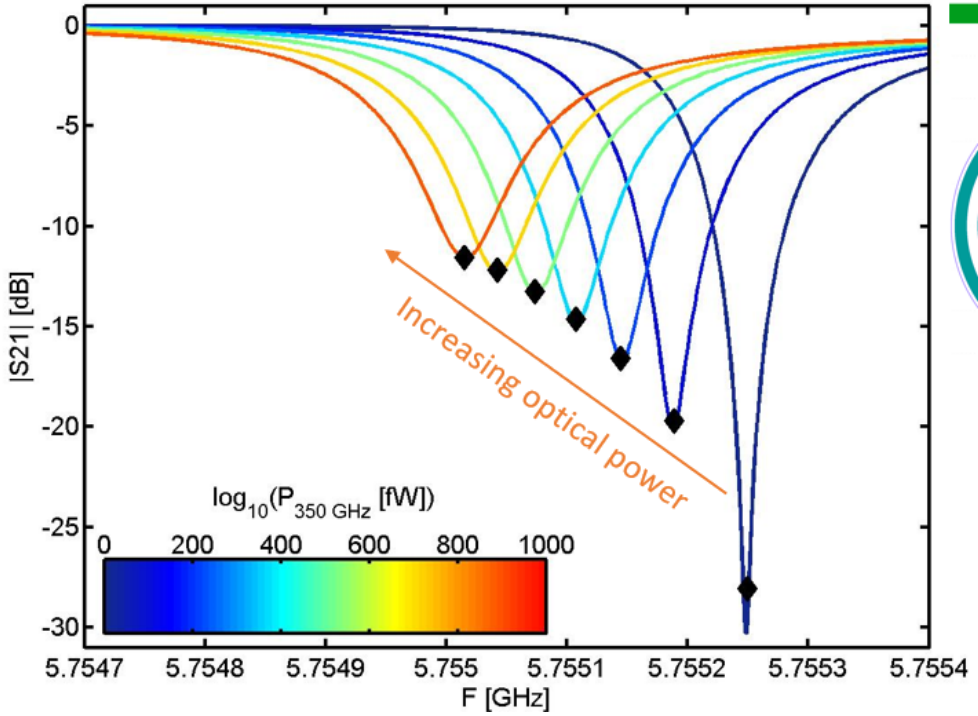
Kinetic Inductance Detectors – Operational Principle
enables massive multiplexing

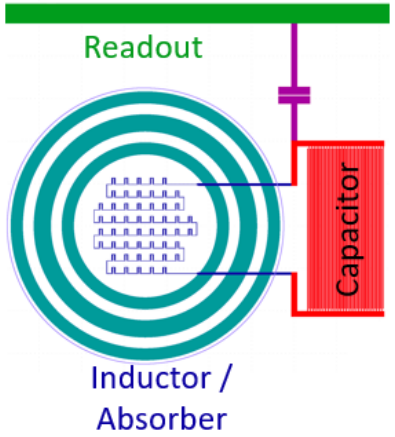
Superconducting resonator

Q ~ 10^4 – 10^6

Fres ~ 0.1 – 10 GHz







PRIMA uses kinetic inductance detectors (KIDs) coupled to silicon lenslets.

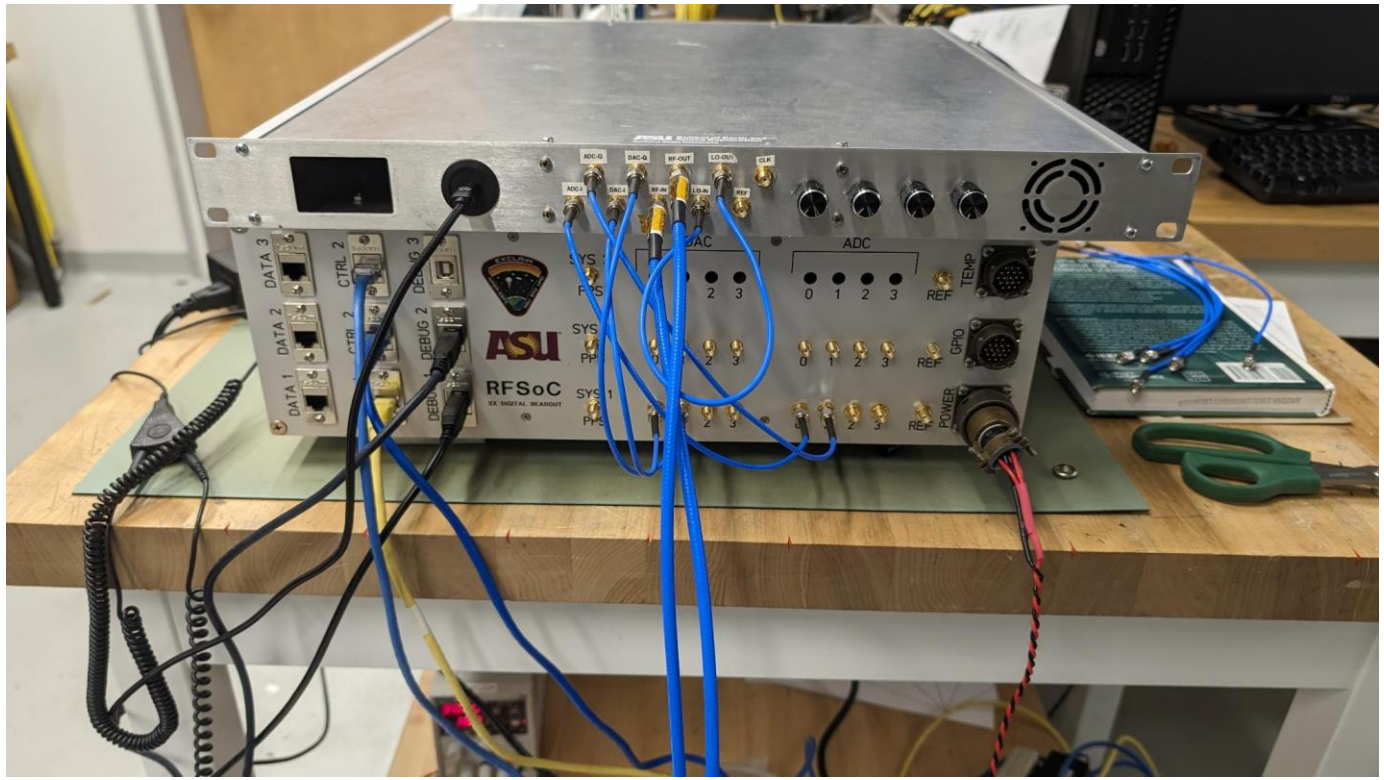
KIDs are microwave resonators where incoming optical power shifts the resonance frequency and quality factor.

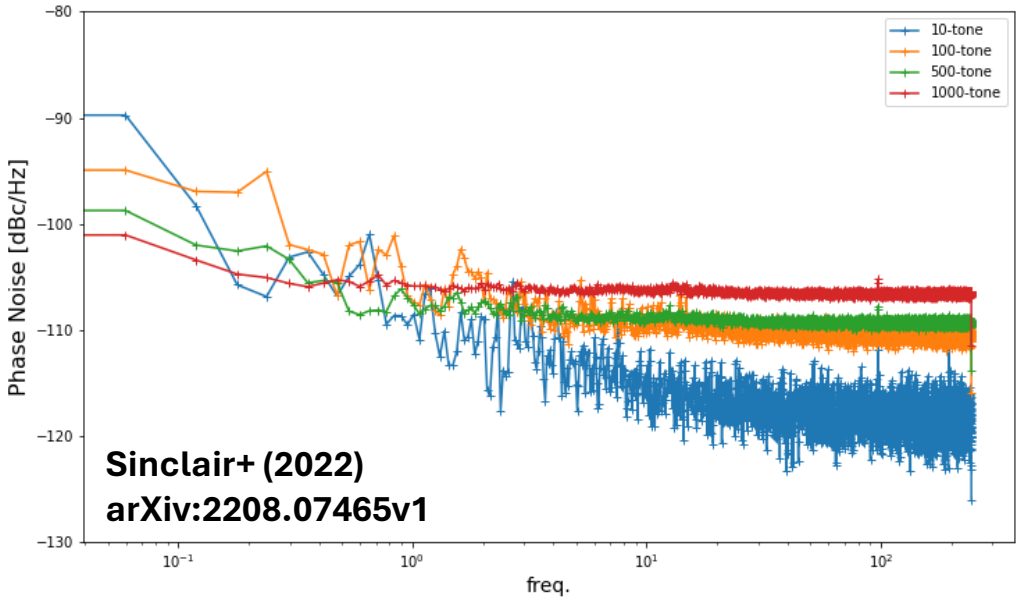
An array of 1000+ of KIDs can be read out on a single coaxial cable.

GSFC readout electronics requirements:

1. Synthesize and output a comb of tones, one for each detector in an array
2. Receive and measure amplitude and phase of returning tones
3. Remove cosmic ray hits in high-speed (10 kHz) data and down-sample to 200-400 Hz to stay within mission downlink budget (~200 GB/day)
4. Switch digital readout chains between FIRESS (0.4-2.4 GHz) and PRIMAger high-frequency (2.5-5.0 GHz) bands.
5. Implement in radiation-tolerant parts appropriate for spaceflight

RFSoC Current State of the Art



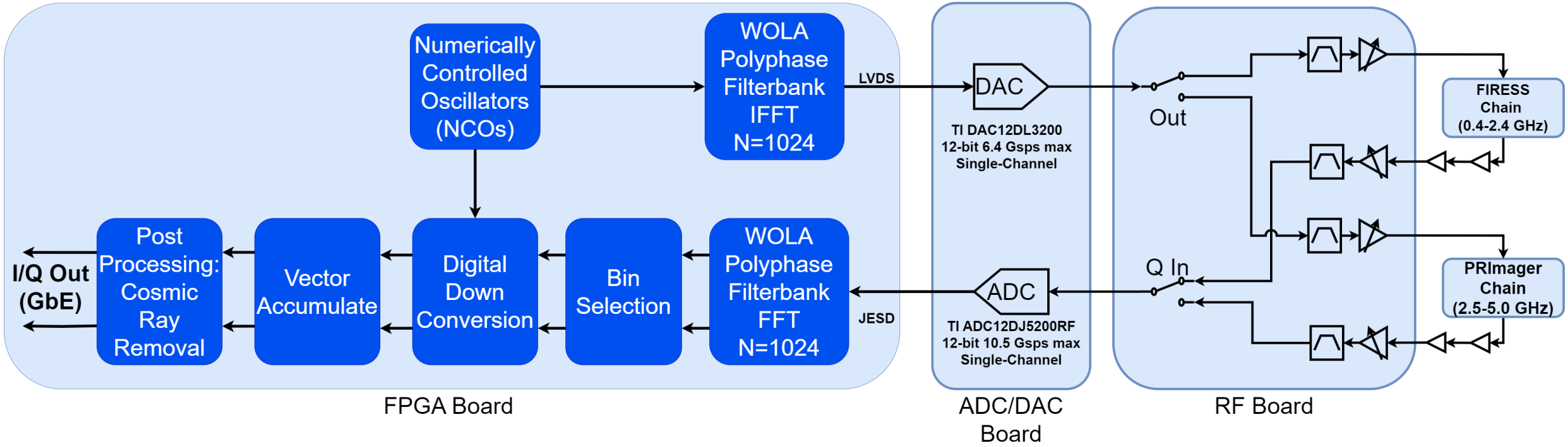


Current readout systems for ground and balloon-borne telescopes are performing well, but do not meet spaceflight requirements:

- Xilinx radio-frequency system-on-a-chip (RFSoC) for EXCLAIM pictured above is not radiation tolerant.

PRIMA needs to implement readout in existing radiation-tolerant chips (Xilinx Kintex KU060 FPGA, TI ADC/DAC)

Readout Electronics Signal Flow



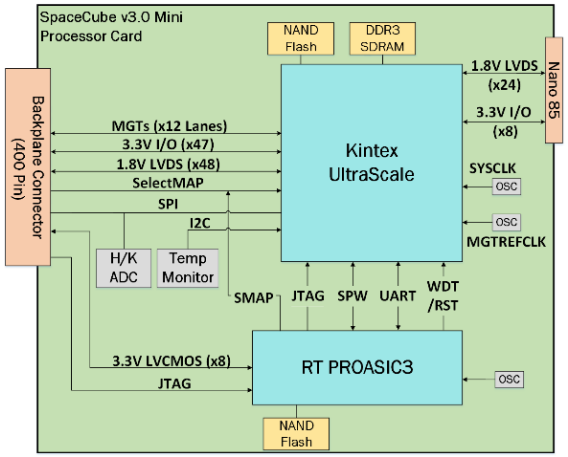
- Detector readout electronics provide switching between the FIRESS and PRIMAger instruments
- With a 5 Gsps readout rate and appropriate filtering, we read out:
  - FIRESS (0.4-2.4 GHz) in the first Nyquist zone and
  - PRIMAger (2.5-5.0 GHz) in the second Nyquist zone of the ADC and DAC
- A high-heritage SpaceCube Mini v3.0 card houses a Xilinx Kintex Ultrascale KU060 FPGA and interfaces over high-speed communications lanes with an ADC/DAC board
- Real-time, on-FPGA processing provides cosmic-ray glitch removal

PRIMA Readout Electronics Implementation: High-Heritage SpaceCube Cards

SpaceCube Mini v3.0 FPGA Card

High-Level Specifications:
- 1x 2GB DDR3 SDRAM (x72 wide)
- 2x 16GB NAND Flash
- Radiation-Hardened Monitor
- External Interfaces
  - 12x Multi-Gigabit Transceivers
  - 48x LVDS pairs or 96x 1.8V single-ended I/O
  - 48x 3.3V GPIO
  - SelectMAP Interface
  - (Front Panel) 24x LVDS pairs or 48x 1.8V single-ended I/O
  - (Front Panel) 8x 3.3V GPIO
- Debug Interfaces
  - 2x RS-422 UART (external transceivers)
  - JTAG

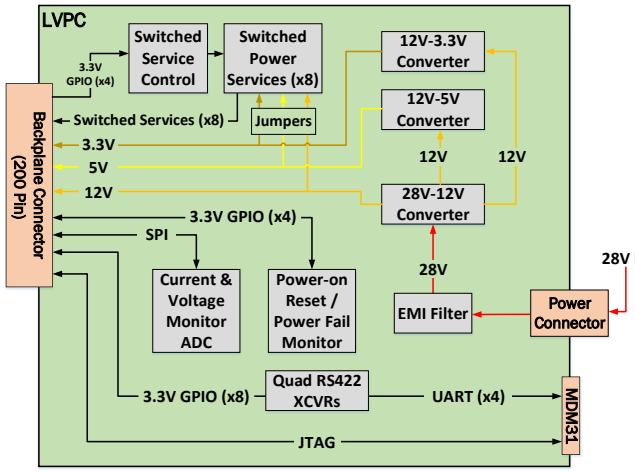
Primary Side



Secondary Side

SpaceCube Mini LVPC Power Card

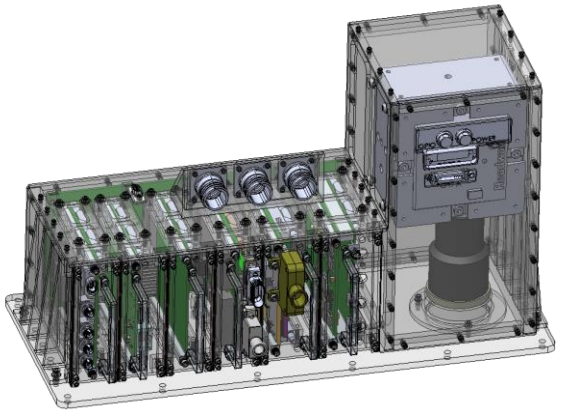
High-Level Specifications
- 40W Output 18-40V/3.33A Input
- 15W Output in development
- 2x 8-ch 12-bit ADC monitoring
- 12V, 5V, 3.3V voltage telemetry
- 12V, 5V, 3.3V current telemetry
- Two thermistor telemetry
- SPI Interface
- 4x RS-422 UARTs
- 8x Switched Services
- 4x 3.3V/5V @ 6A
- 4x 5V/12V @ 3A
- Power-on-Reset



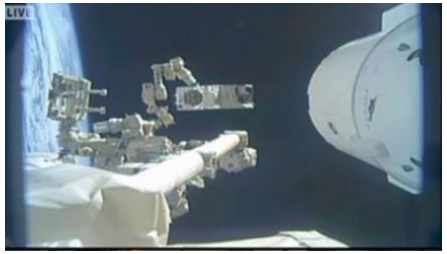
STP-H9-SCENIC Heritage

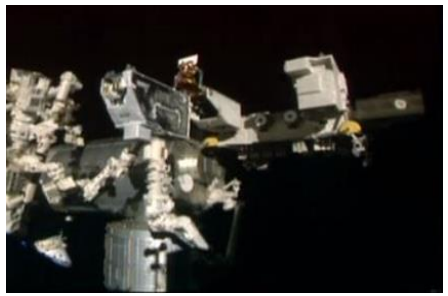
SCENIC: SpaceCube Edge Node Intelligent Collaboration

- ISS-based testbed to evaluate and validate AI/machine learning technology on FPGA and custom AI microchip platforms in space
  - Collaborations with AFRL and the Aerospace Corp.
  - Successfully launched on March 14, 2023 and now deployed to ISS
  - Flight debut and TRL advancement for multiple SpaceCube cards
- Goals
  - Demonstrate cutting-edge AI applications on multiple space-based platforms for next-generation on-board intelligence, and monitor device availability due to radiation effects (i.e., Intel Myriad X, Google Coral TPU, AMD-Xilinx DPU)







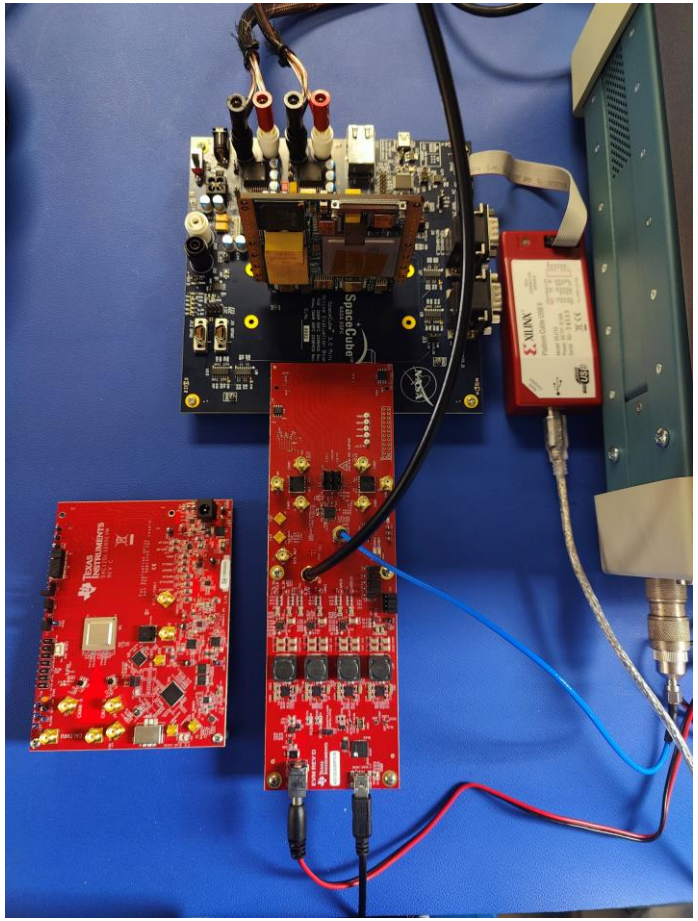


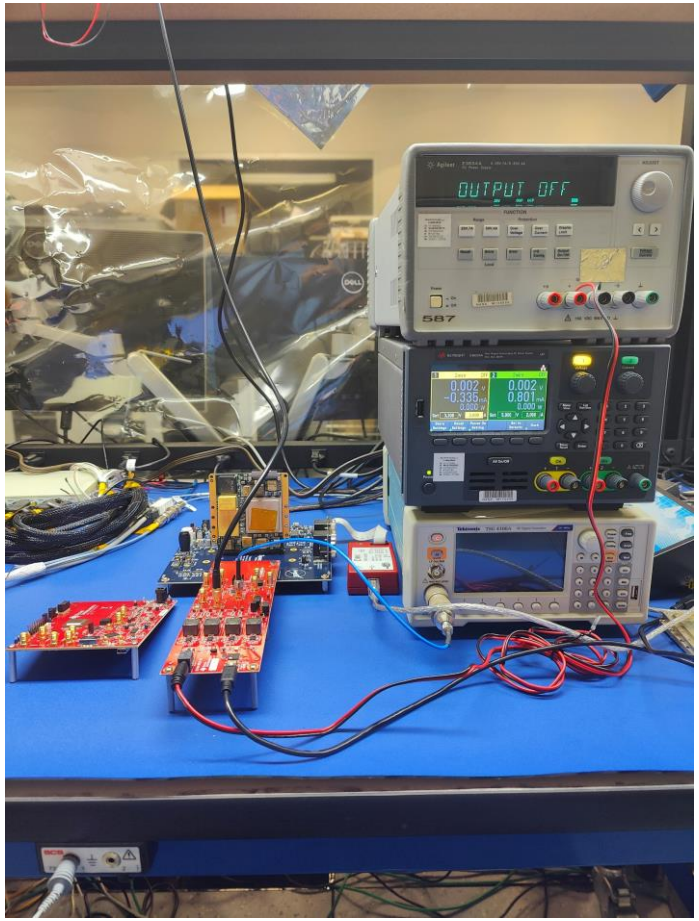




SpaceCube Mini Testbed

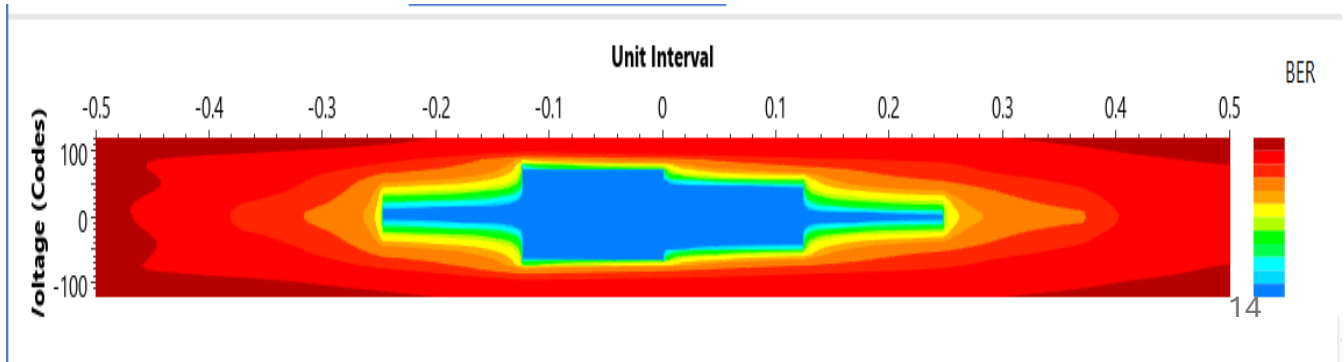
- SpaceCube v3.0 Mini Processor Card with Active Evaluation Kit (XCKU060)
- TI ADC12DJ5200RFEVM ADC Evaluation Board (Right, red)
- TI DAC12DL3200EVM DAC Evaluation Board (Left, red)
- Tektronix 4106a RF Synthesizer





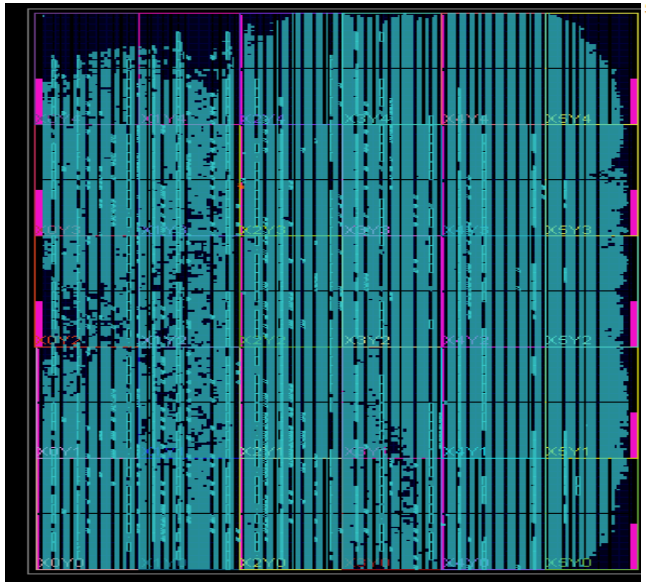
PRIMA ADC/DAC Progress

- Current Progress
  - Setup testbed for the ADC/DAC
  - Evaluated the TI ADC board on both the KCU105 development board and the SpaceCube v3.0 Mini processor card
  - Captured eye diagrams for the ADC running at 6 lanes, 4.8 GSps, 9.9 Gbps with a bit error rate (BER) < 10^{-12} upper limit – no errors seen during test. **Meets mission requirements for data rate.**
  - Measured preliminary power numbers for the SpaceCube Mini and Active Eval Kit when interfacing with the ADC evaluation board.
- Challenges
  - Some trouble establishing basic communication with the ADC due to inverted polarity on the evaluation board's transceiver lanes
  - Distorted clock from a cheap RF synthesizer was preventing the multi-gigabit transceiver (MGT) phase-locked loops (PLLs) from locking initially
- Future Work
  - Adjust ADC pre-emphasis settings to improve eye diagram
  - ADC data capture
  - Evaluate DAC board



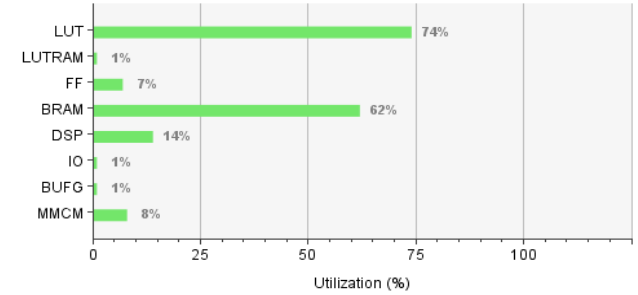
Firmware Resource Utilization

- Firmware design in simulation has been completed for 2 and 3 GHz readout bandwidths capable of meeting PRIMA requirements.
- Evaluating whether two readout chains can fit within a single Kintex KU060 FPGA.
- Initial utilization estimates (at right) show 2, 2GHz signal chains fit onto the KU060 fabric but at unacceptably high resource utilization.
- On-going investigation of resource savings from moving data stored in LUTs/BRAM to SpaceCube Mini DDR3 memory off-chip, as well as firmware refinements.
- 15 W per readout chain is current best estimate of FPGA power consumption
- Including power usage from ADC/DAC, power card, backplane loss, communications, and RF electronics brings pessimistic power usage per chain to 35 W.



Summary

Resource	Utilization	Available	Utilization %
LUT	246533	331680	74.33
LUTRAM	1378	146880	0.94
FF	44120	663360	6.65
BRAM	669	1080	61.94
DSP	400	2760	14.49
IO	3	624	0.48
BUFG	7	624	1.12
MMCM	1	12	8.33

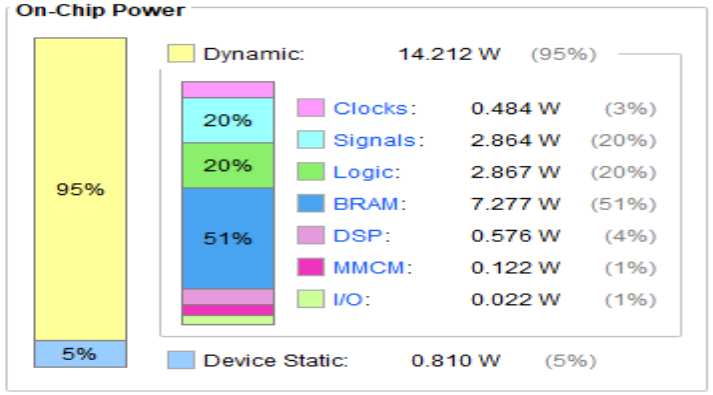


Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**15.023 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**42.2°C**
Thermal Margin:	57.8°C (48.5 W)
Effective ϑJA:	1.1°C/W
Power supplied to off-chip devices:	-0.004 W
Confidence level:	Medium

Launch Power Constraint Advisor to find and fix invalid switching activity



ADC + DAC Modeling

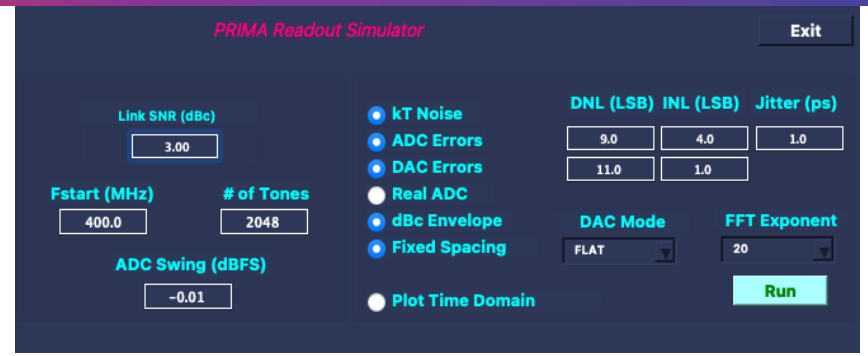
Detailed modeling of both the ADC and the digital-to-analog converter (DAC) show performance sufficient to meet PRIMA mission requirements.

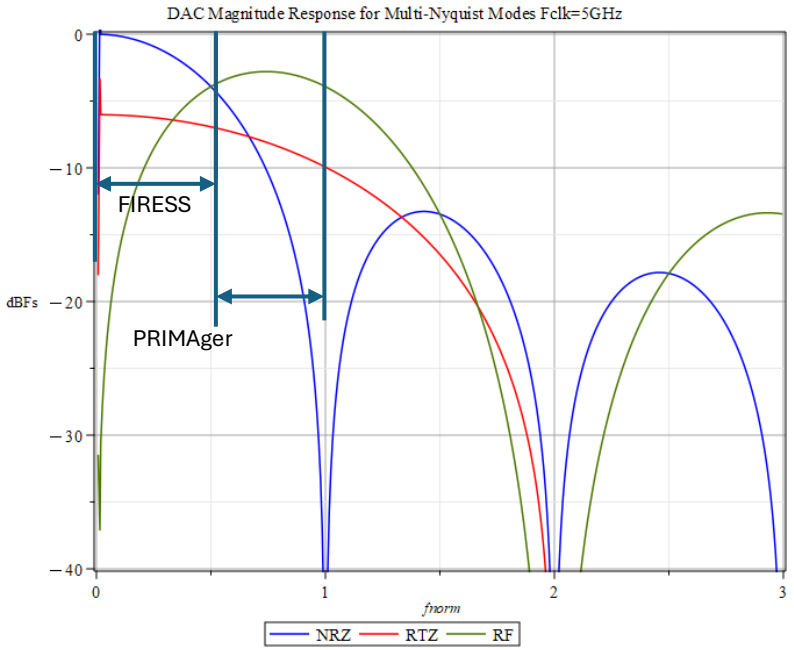
Simulations include realistic:

- ADC and DAC Differential non-linearity (DNL)
- ADC and DAC Integral non-linearity (INL)

2048 tones spaced evenly over FIRESS 0.4-2.4 GHz

Band with 5 Gsps sampling rate gives -90 dBc/Hz spectral density.





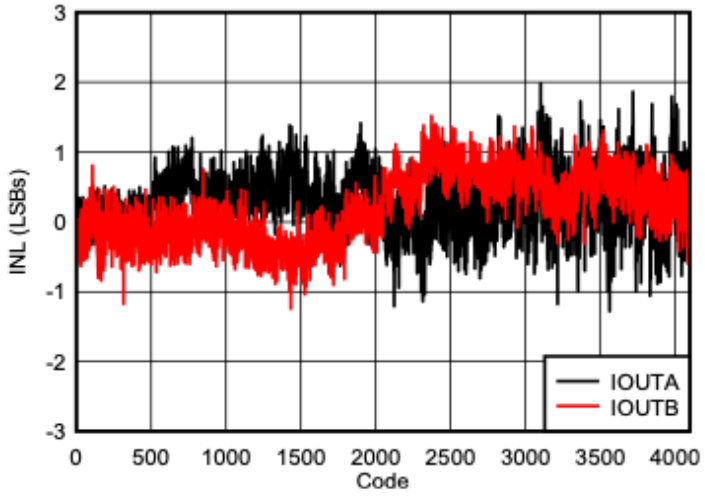
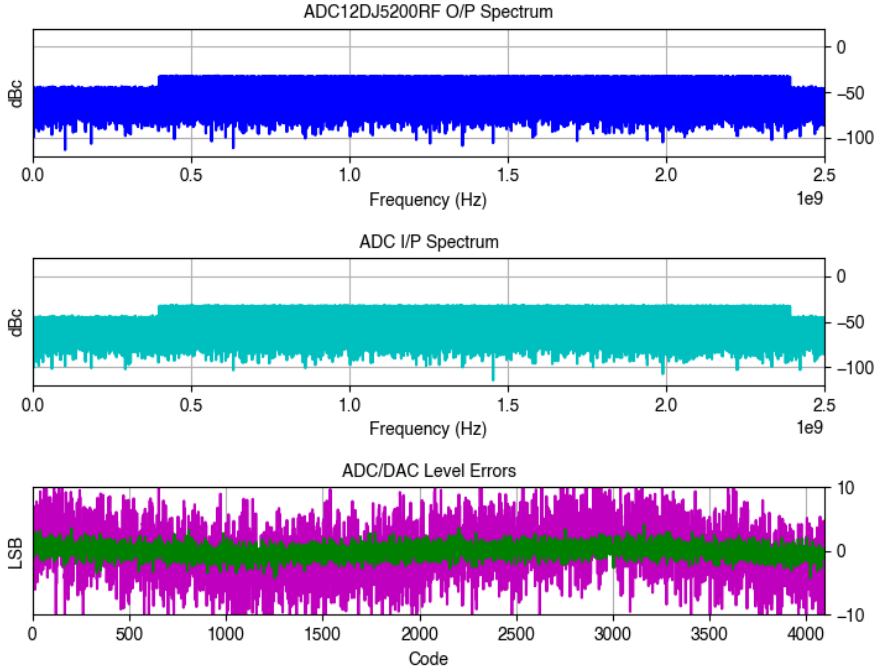


Figure 6-2. Output Current INL vs Code



	SINAD	SFDR	NSD	NBIN	Max	Min	En	Qn	Gain	Att	CF
ADCout	-3.6	41.9	-90.4	-53.6	4093	3	-	3.92	-	-	-
ADCin	-3.6	41.9	-90.4	-53.6	0.8	0.0	0.072	-	81.1	-15.5	13.2
Units	dBc	dBc	dBc/Hz	dBc	Q-V	Q-V	V	V	dB	dB	dB

Cosmic Ray Removal

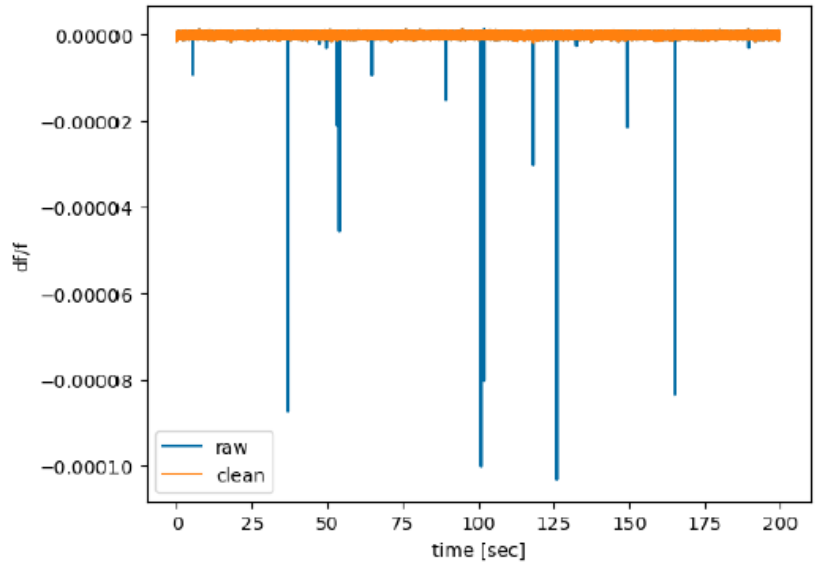
To stay within achievable daily downlink bandwidths (~200 GB/day), cosmic ray glitch removal will be carried out on high-rate (10 kHz) data in real time on board the FPGA before down-sampling to 200-400 Hz (depending on observing mode).

Should be more than sufficient to isolate cosmic ray glitches with acceptable observing efficiency (estimate > 90%), given measured detector time constants (< 3 ms affected data per cosmic ray hit)

Initial prototyping of algorithms uses high-level synthesis (HLS) to quickly turn C/python code into FPGA firmware for estimates of the resource utilization.

A simple peak-finding cosmic ray removal algorithm was found to use < 3% of SpaceCube Mini FPGA resources.

Refinement of the algorithms is on-going, including investigation of more sophisticated matched-filter methods.



Provided graph visualization of input raw data (blue) and output clean data (orange) after ray removal

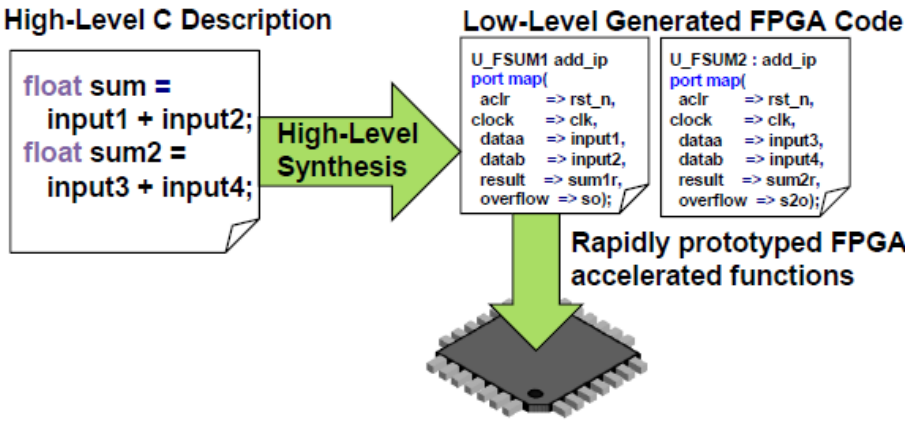


Illustration of HLS Design Process

KID Readout Electronics for PRIMA: Conclusions

- PRIMA is a far-IR mission proposed as a NASA Astrophysics Probe Explorer that addresses key Decadal Survey priorities with two instruments:
  - FIRESS: R > 85 spectroscopy (24-235 μm) + High-Res mode R = 4,400 x (λ/112μm)
  - PRIMAger: R = 10 hyperspectral imaging 25-80 μm + R= 4 imaging & polarimetry 91-261 μm
- PRIMA sensitivity is enabled by large arrays of kinetic inductance detectors (KIDs).
- Frequency multiplexing electronics read out 1000+ KIDs per coaxial cable.
- Spaceflight readout electronics are being developed by Goddard Space Flight Center (GSFC) for PRIMA using Xilinx Kintex KU060 FPGA and high-speed TI ADC/DAC chips.
- PRIMA readout electronics are implemented using high-heritage SpaceCube parts:
  - Build-to-print SpaceCube Mini v3.0 FPGA board, LVPC power card
  - New digitizer card development to incorporate high-speed TI ADC/DAC chips
  - Modeling of FPGA, ADC, and DAC show that they will meet or exceed PRIMA mission requirements for power consumption, noise, and dynamic range.
- The limited downlink bandwidths available for a space mission require on-board processing to flag and remove cosmic ray hits and downsample in real time.