Solid State Drive Radiation Assurance With Active Testing

Edward P. Wilcox[1], Adia Wood[1], Gregory Allen[2], Martin Carts[1], Megan Casey[1]
[1]NASA Goddard Space Flight Center
[2]Jet Propulsion Laboratory

National Aeronautics and Space Administration

Testing Description

Automotive and industrial grade SSDs (listed in Table I) were tested for TID and SEE response at the assembly level to investigate radiation tolerance trends and explore radiation hardness assurance best practices in commercial memory devices [1]. SSDs were installed in passive NVMe extenders to place only the drive in the beam line. A digital I/O module connected to the test computer (Fig. 1) provided inhibit signals to block both facility beam delivery and power while attempting recovery from any device failure conditions (e.g., failed write, failed read, or unresponsive device).

Table I. Description of devices under test

	Micron MTFDHBK256TDP-1AT12AIYY	Swissbit SFPC320GM1AG4TO-I-8C-51P-STD	Exascend EXPI4M960GB-DL	Western Digital SDBPTPZ-085G-XI
Operating Temperature	M.2: -40°C to +95°C BGA: -40°C to +105°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C
LDC	3BA22 and 3PA22	0423	Unavailable	19JUN2023
Memory Type	256 GB TLC or 85 GB SLC Intel-marked (Micron B17A) 64 Layer 3D NAND	320 GB pSLC Kioxia/Toshiba 64 Layer 3D NAND	960 GB TLC	85 GB SLC 96 Layer 3D NAND
DRAM	No	Micron DDR3 1GB	No	No
Controller	Silicon Motion SM2263A PCIe 3.0	Phison PS5008-E8-10 PCIe 3.0	Marvell 88SS1321 PCIe 4.0	WD - Possibly PCIe 3.0 20-82-10048-A1 Polaris MP16
Footprint	M.2 2230	M.2 2280	M.2 2280	M.2 2230

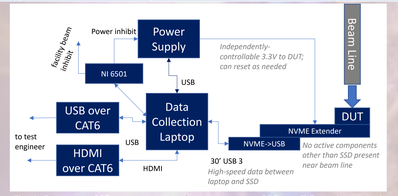

Fig. 1. Full-board SSD test apparatus for autonomous SEE and TID testing at a distance.

A fully autonomous test is illustrated in Fig. 2. As observed by supply current, 8 separate events occur, all of which are recovered with a power cycle. In each case, the device completes entire read and write cycles between events. The lower curve denotes NSRL-delivered beam spills, with a typical fluence of 500/cm^2.

The SEE and TID test flows are depicted in Fig. 3 and 4. In each case, test data was 1,024 to 4,096 random locations written with 1,024 kB of pseudorandom data. Data was uniquely marked to indicate any addressing errors. On each operational loop, the random locations were changed.

Fig. 2. Supply current (top) of critical events during heavy-ion testing, with beam spill fluence (bottom).

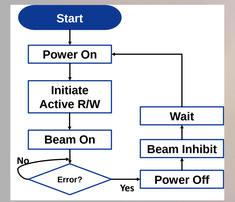

Fig. 3. SEE dynamic read/write test flow

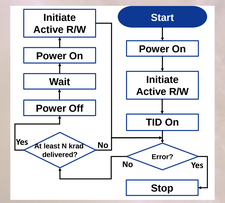

Fig. 4. TID dynamic read/write test flow, including power cycling added after initial results

Proton Results

Micron TLC automotive grade SSDs and Western Digital SLC industrial grade SSDs were irradiated dynamically at the Massachusetts General Hospital's Francis H. Burr Proton Therapy Center in January, 2024. Both devices suffered unrecoverable failures during both read and write operations. Mean fluence between failure (including both recoverable and unrecoverable events together) are in Fig. 5.

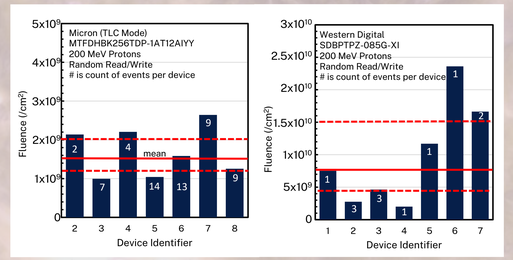

Fig. 5. Mean fluence between failures for Micron (left) and Western Digital (right) with 200 MeV proton testing. Each device is a separate bar, with total failures per device listed. Mean and 95% confidence ranges are shown.

While the MFBF appear quite different between the two, the fluence to *unrecoverable* failure are similar – about 2.22x10^{10}/cm^2 for the Micron and 1.43x10^{10}/cm^2 for the WD. The WD device requires intervention less often than the Micron device, but neither is immune to proton-induced functional failure. Irradiations in an *unbiased* configuration (4.28x10^{10}/cm^2 for each device) did not cause any observable failures even though both device's NAND flash arrays are susceptible to bit cell upsets in this condition.

Heavy Ion Results

In June 2024, the Micron, Western Digital, Swissbit, and Exascend drives were all tested with high-energy heavy ions at the NASA Space Radiation Lab (NSRL). All were susceptible to unrecoverable errors. A small improvement was observed in the Micron device when provisioned into 100% SLC storage (Fig. 8). Here, mean fluence between failure includes both recoverable (with power cycle) and unrecoverable events.

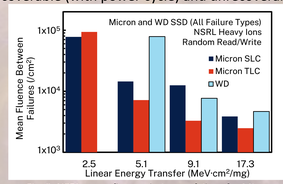

Fig. 8. NSRL mean fluence between failure for Micron and WD SSDs, with the Micron drives provisioned into TLC or SLC for comparison. In both cases, the entire drive is fully exposed to the beam. Untested configurations are blank

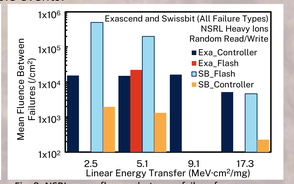

Fig. 9. NSRL mean fluence between failure for Exascend and Swissbit drives, with irradiations focused on either the NAND flash or the controller (and DRAM, for the Swissbit). Untested configurations are blank.

The TLC Exascend flash was significantly more vulnerable (Fig. 9) than the SLC Swissbit flash, while the Swissbit controller was the most sensitive region tested – which notably is the only device with onboard DRAM. However, these were primarily recoverable events. Unrecoverable errors occurred on all devices, including when irradiating only the NAND flash for both the TLC Exascend drive and the SLC Swissbit drive (i.e., not merely user data corruption).

Table II. Unrecoverable Errors with Heavy Ions

Part	Target	Unique Parts Tested	Threshold LET for Unrecoverable	Fluence at Highest Passing LET
Micron (SLC)	Entire Device	6	9.1 < x < 17.3	1x10^5/cm^2
Micron (TLC)	Entire Device	7	2.5 < x < 5.1	9.4x10^4/cm^2
Swissbit	Flash	3	5.1 < x < 9.1	2x10^5/cm^2
Swissbit	Controller/DRAM	2	x > 17.3	6.59x10^3/cm^2
Exascend	Flash	2	x < 5.1	N/A
Exascend	Controller/DRAM	3	2.5 < x < 5.1	4.61x10^4/cm^2
WD	Entire Device	2	5.1 < x < 9.1	8.65x10^5/cm^2

TID Results

Total ionizing dose testing with gamma irradiation at the NASA GSFC Radiation Effects Facility (REF) provided intriguing results. The same test setup from SEE testing enabled full board-level irradiations with in-situ dynamic reading and writing. The original intent was to ensure that all internal components were exercised (e.g., high-voltage charge pump transistors [2,4] known to be a weak link of modern NAND). Random read/write testing of a Swissbit industrial-grade SLC SSD (Fig. 6, top) suggested a TID tolerance of approximately 55 krad(Si) for a sample size of 1. The next irradiation of another Swissbit sample was halted at 30 krad(Si) to perform a thorough characterization. However, the device could not be powered-on after removing it from the in-situ test setup.

The TID test was modified (sequence in Fig. 4) to periodically test for bootability. The next Swissbit device failed in-situ bootability after only 16 krad(Si) (Fig. 6, bot).

The Exascend PI4 TLC industrial SSD failed (Fig. 7) at 23 krad(Si) when dynamically read/written in-situ, but at only 7 krad(Si) when power cycling was included (and 17 krad(Si) for a "cold spare" test).

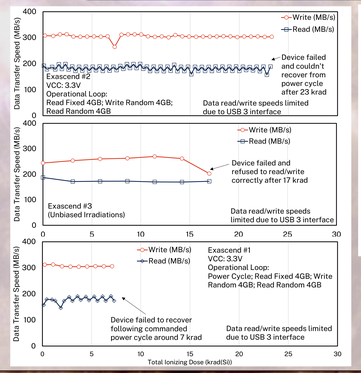

Fig. 7 (left). TID tolerance as measured by read/write speeds for the Exascend PI4 SSD with continuous read/write (top), cold spare (middle), and read/write with periodic power cycling (bottom).

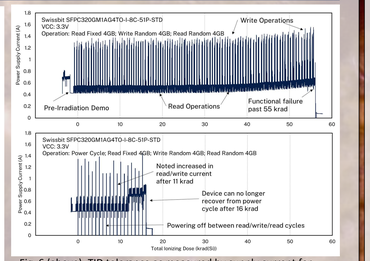

Fig. 6 (above). TID tolerance as measured by supply current for the Swissbit SSD with continuous read/write (top) and read/write with periodic power cycling (bottom).

Hardness Assurance Implications

That dynamic testing of a complex system may expose new error signatures is not a novel concept [4], nor is the presence of functional failures in solid-state drives [5]. However, the hardness assurance implications herein address the momentum towards flying off-the-shelf [1] systems with little formal radiation engineering practices, and whose original designers had no intention to include radiation tolerance whatsoever. These systems may be tested for TID tolerance in a manner intended to reflect flight usage [6] and/or tested for destructive SEE with the plan to power cycle [7] as needed operationally. Indeed, such objectives may be mutually exclusive – the devices tested in this work perform best in a dose environment when *never* turned off, and best in an SEE environment when left off *as much as possible*.

NAND flash memories are well-known to be susceptible to charge-pump failures [2,3] at lower total ionizing dose levels than mainstream CMOS microcircuits. Similarly, commercial CMOS devices commonly fail due to single-event latchup [8] under heavy-ion irradiation. It is not unreasonable to hypothesize that an arbitrary solid-state drive might be dose-limited by NAND erasures and be SEE-limited by unidentified CMOS microcircuit controllers. The devices tested herein are neither. The SSDs are dose-limited by power-on processes and are SEE-limited by errors in controller, DRAM, and memory circuitry that are neither traditional destructive SEE (e.g., SEL) nor easily-correctable soft errors (these drives feature extensive error-correction [9] that should be sufficient for the errors induced by low fluences of heavy-ions or 200 MeV protons observed in previous testing [10]).

It is prudent that the usage of any complex system be predicated upon some estimation of radiation response, and while a trend toward test-as-you-fly on a black-box system may be the only practical solution for many applications (e.g., cost and schedule), underlying vulnerabilities in these systems require a particularly careful approach [11] that may not resemble that of piece-part tests (e.g., those in [8]).

The off-the-shelf SSDs tested in this work provide automotive- and industrial-grade temperature ranges and reasonable assurance of manufacturing quality [1]. They likely have acceptable TID performance for the lowest of dose environments (or when heavily shielded), and the remedy for TID testing practices is clear – ensure that test-like-you-fly really means a full test case, not merely testing the most common usage. However, their SEE performance remains troubling from a testing standpoint and requires further exploration.

Complex devices procured off-the-shelf offer little customizability, less error reporting, and potentially no architectural details. Yet, they cannot be reliably screened with a destructive SEE test when all parts tested in this study failed unrecoverably for reasons likely related to the architecture (e.g., SSD mapping tables and other configuration information stored in the non-volatile array) rather than a familiar single-event latchup signature.

Acknowledgements and Further References

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CMOS: Complementary Metal Oxide Semiconductor
COTS: Commercial Off The Shelf
DRAM: Dynamic Random Access Memory
DUT: Device Under Test
LDC: Lot Date Code
LET: Linear Energy Transfer
NVMe: Non-Volatile Memory express
SEE: Single-Event Effect
SEFI: Single-Event Functional Interrupt
SEL: Single-Event Latchup
SEU: Single-Event Upset
SLC: Single-Level Cell
SSD: Solid State Drive
TID: Total Ionizing Dose
TLC: Triple-Level Cell