



2024 HELIOPHYSICS TECHNOLOGY SYMPOSIUM

Designing and Testing for Radiation Tolerance

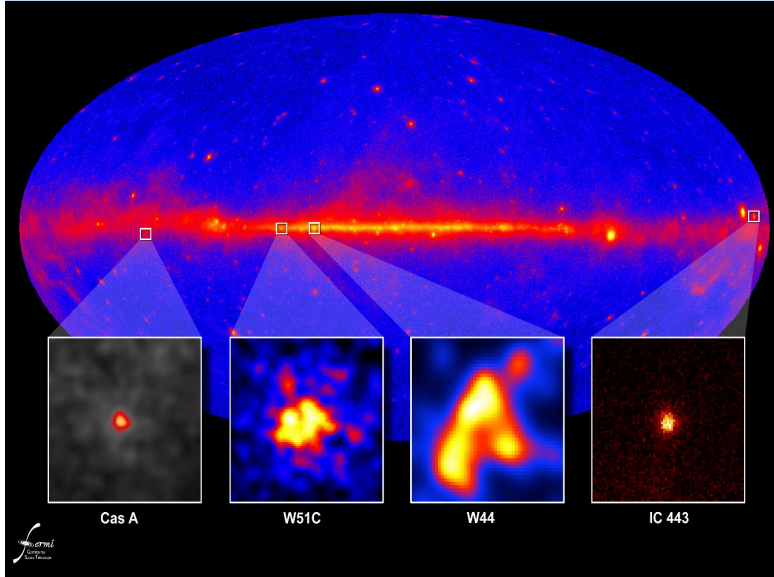
Michael J. Campola, michael.j.campola@nasa.gov

Radiation Effects and Analysis Group Leader

NASA Goddard Space Flight Center (GSFC)

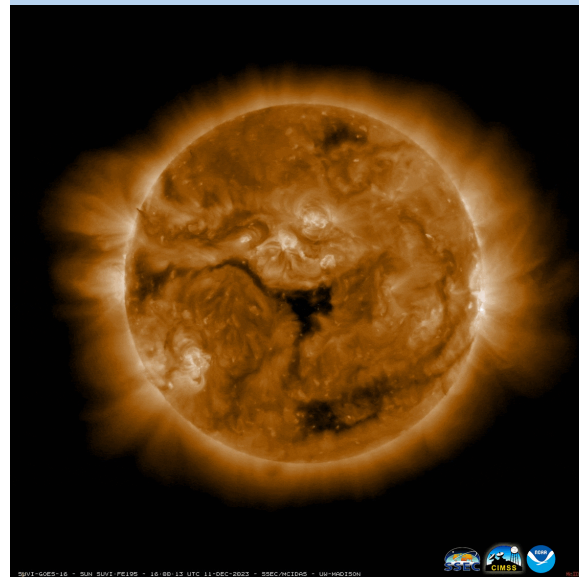
Natural space radiation environment

Galactic Cosmic Rays



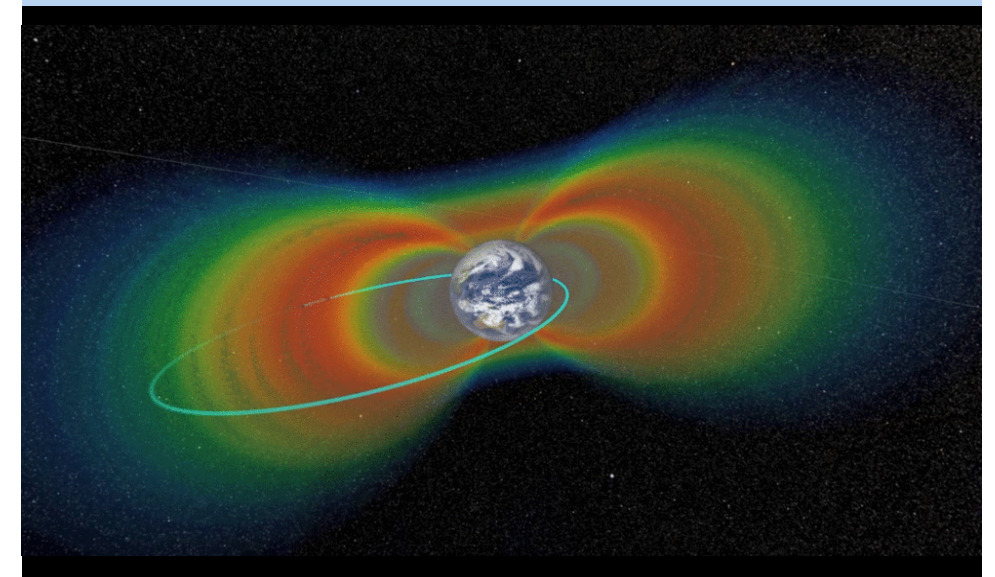
Energetic supernovae remnants
(~GeV, $Z=1-92$)
Originate outside of our solar system

Solar Activity



Solar Wind
~11-year Solar Cycle
CMEs (proton rich)
Flares (heavy ion rich)

Trapped Particles in Planetary Magnetic Fields



Fluctuate with Solar Activity and Events
Not a perfect dipole
Protons and Electrons trapped at different
L-shell values and energies

These sources are **dynamic**.

Images from left to right – NASA FERMI X-ray telescope, Solar Dynamics Observatory, Janet Barth (radhome.gsfc.nasa.gov)

Ionizing Radiation Effects

Total Ionizing
Dose (TID)

Total
Non-Ionizing
Dose (TNID)

Single-Event Effects (SEE)

Non-Destructive

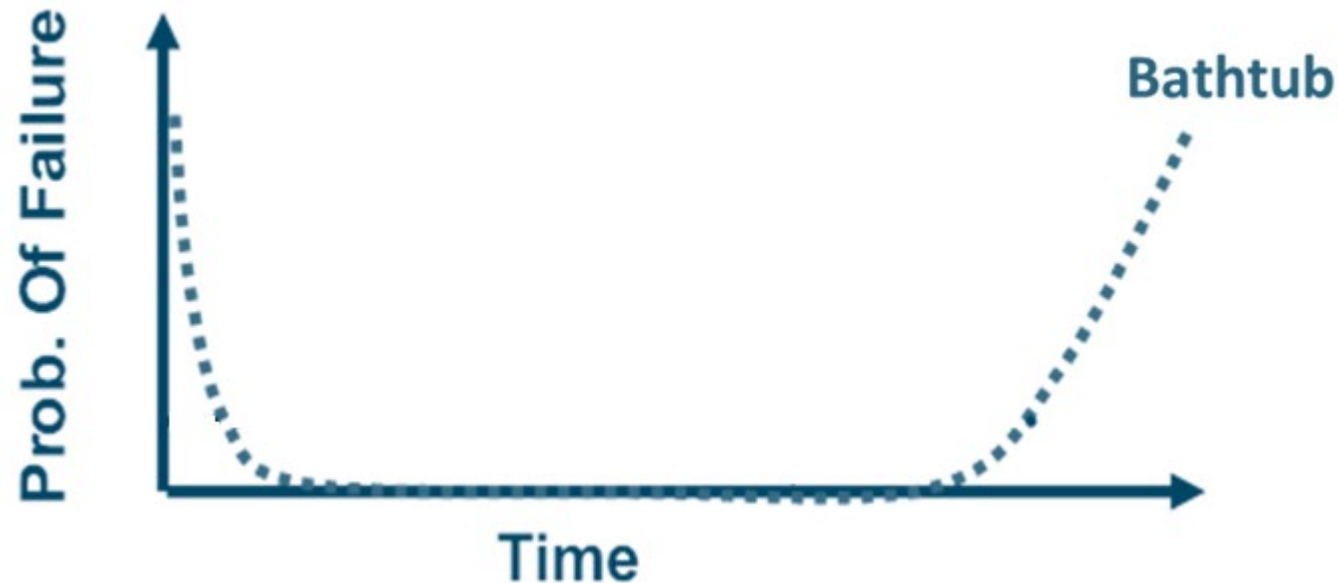
Destructive

Primarily high-energy protons and heavy ions

Damage is a two-fold problem

Dose shows up as you'd expect: wear-out mechanism (cumulative) – many damage sites or trapped charges accrue over time

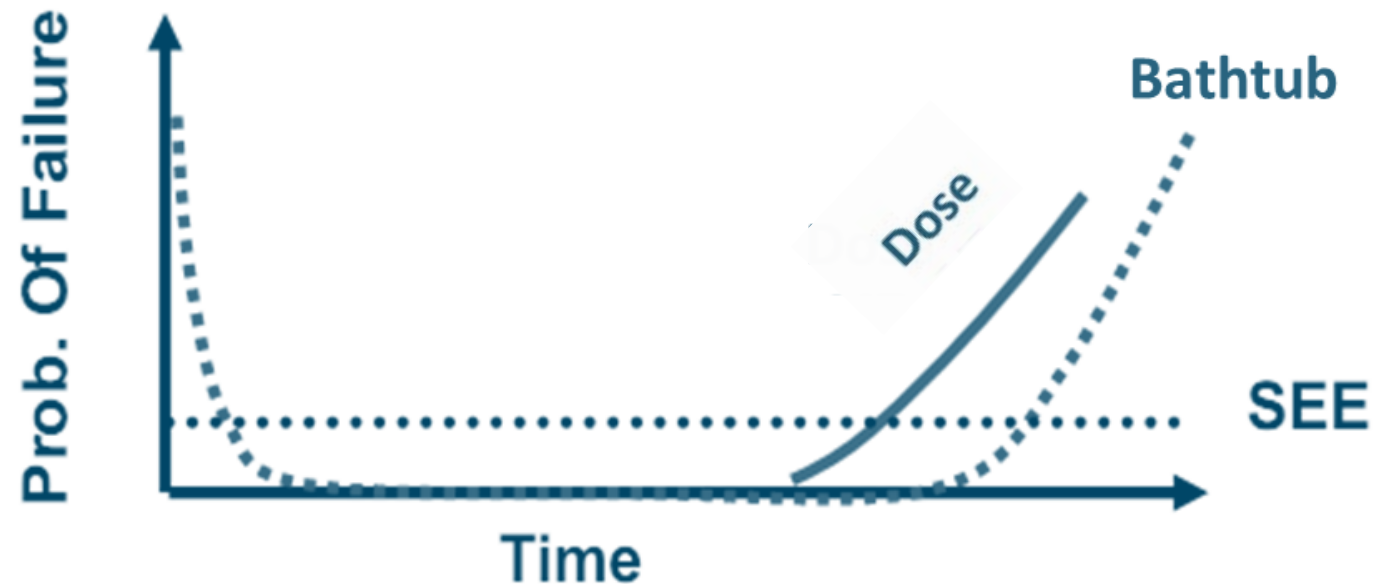
Single events show up as random failures-in-time (instantaneous) – one particle with sufficient energy deposition in the right location



Damage is a two-fold problem

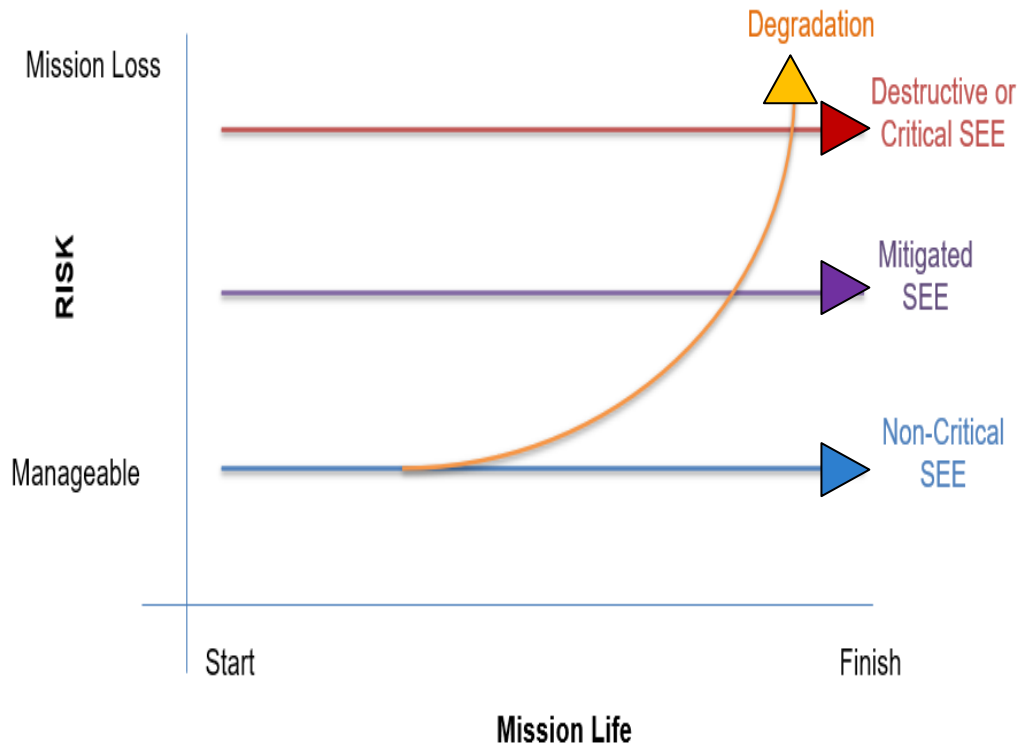
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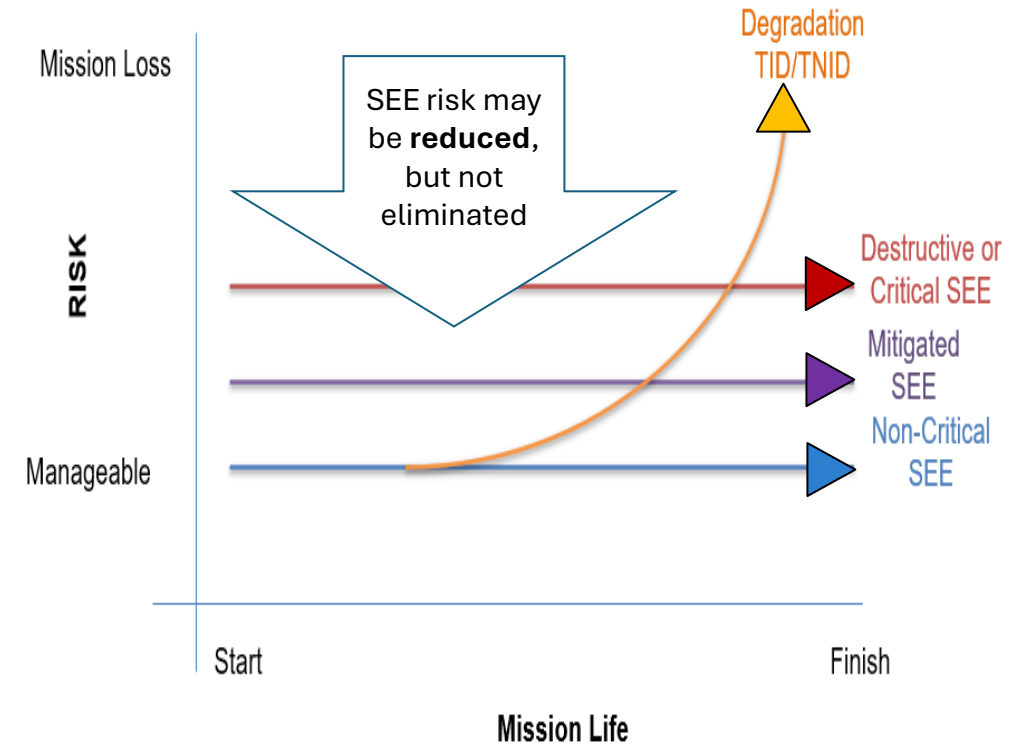
Redundancy in electronics

Single Points of Failure



vs

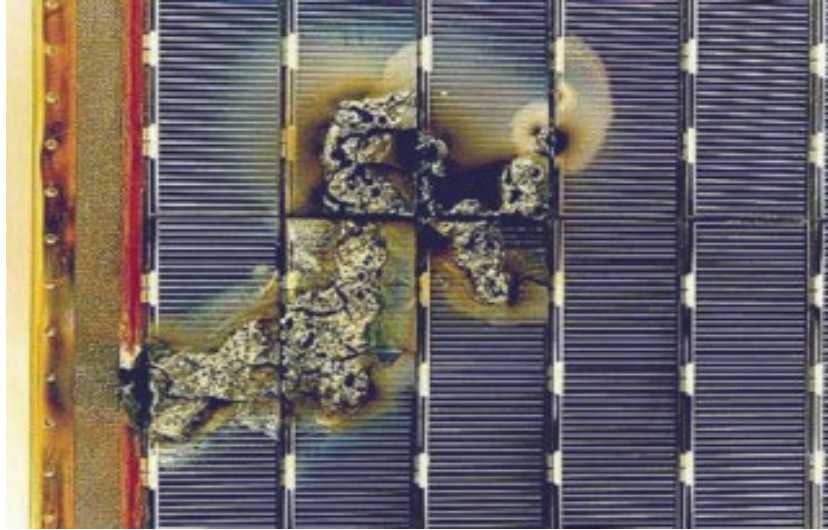
Redundancy



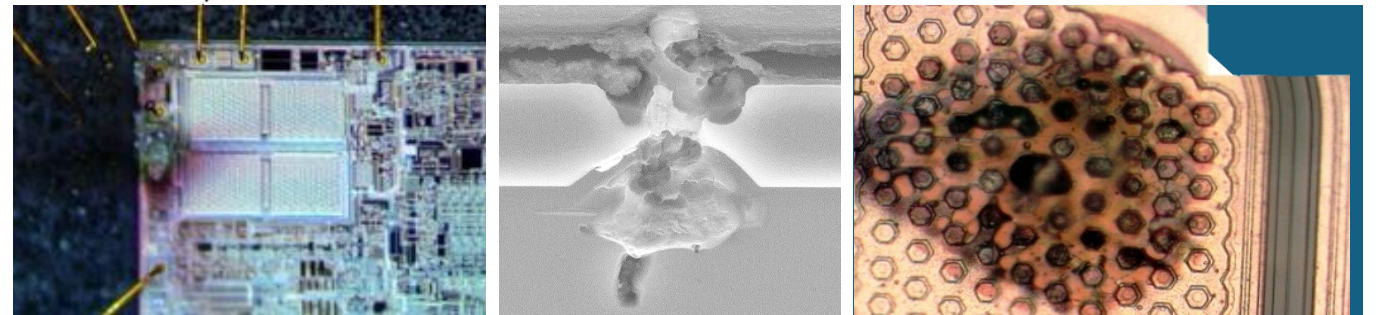
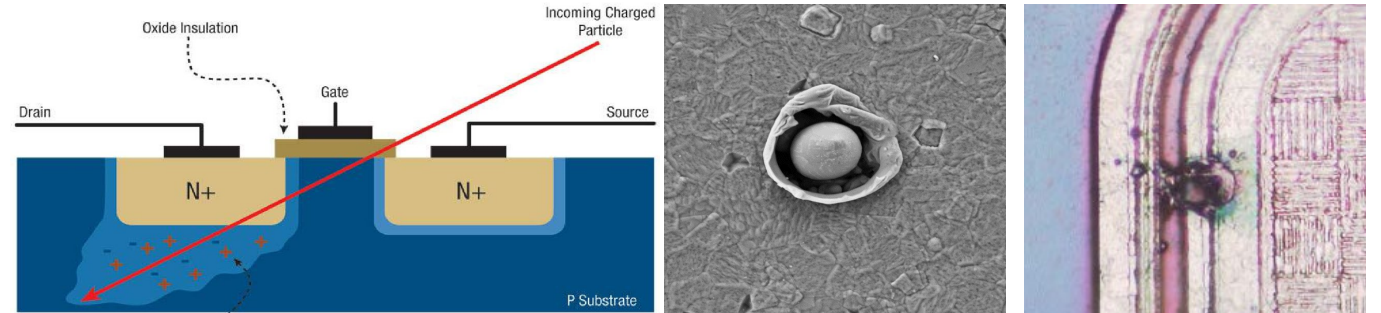
Redundancy does **not** remove SEE risk; it reduces impact. Common failures like TID still exist.

Electronics don't like that

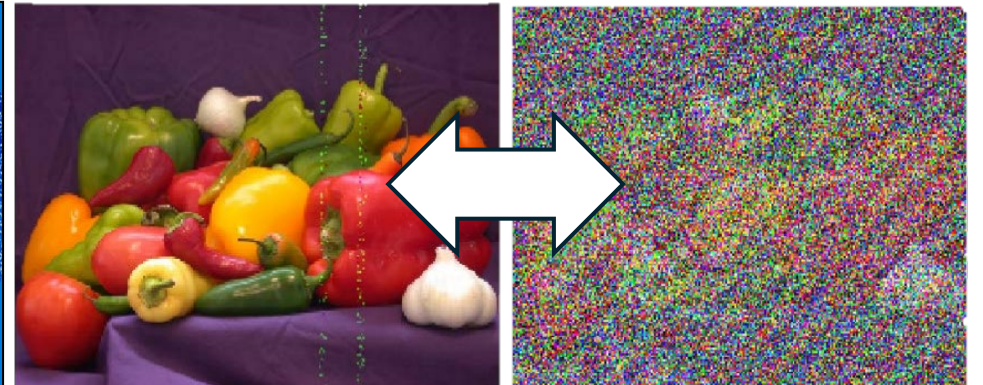
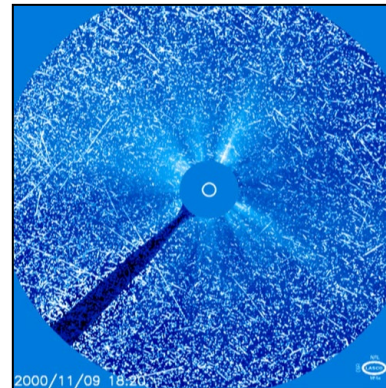
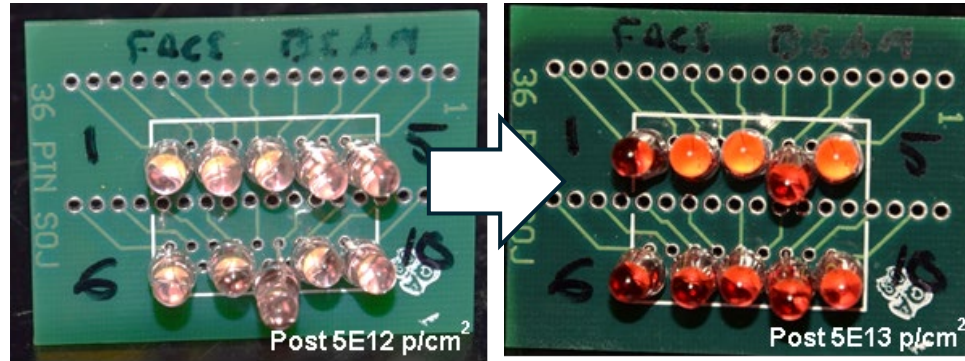
Charging leads to arcing



SEE leads to failures/functional disruptions



Dose leads to degradation/functional failure



Summary of risks to electronic parts

TID	TNID/DDD
• Increased leakage current, power consumption • Threshold voltage shifts • Stuck bits in memory cells • Changes in timing • Decreased functionality	• Decreased efficiency in optical devices • Increased dark current in CCDs • Degradation of CCD charge transfer efficiency • Degradation of solar cells, optocouplers, linear bipolar devices
SEE	Charging:
• Voltage/current spikes (SET) • Bit-flips (SEU) • Instantaneous high current states (SEL) • Program crashes (SEFI) • Catastrophic device failure in power devices (SEB, SEGR)	• Electrostatic discharge • Arcing • Enhanced surface contamination • Local dielectric breakdown

(After K. Ryder)

How do we assure something that is complex?

Technology Feasibility (show-stoppers)

Partnerships

Preliminary
testing

Roadmaps &
demand

Manufacturer
testing

Process
performance

Independent
verification

Radiation effects community driven:
NASA Electronic Parts and Packaging (NEPP)

Architectural Demonstration

Characterization

Reliability at
extrema

Availability
constraints

Corner cases

Worst case
conditions

Physics of
failure

Design community driven,
intentional test design

System Assurance

Concept of
operations

Requirements
verification

Likelihood in
environment

Criticality and
impacts

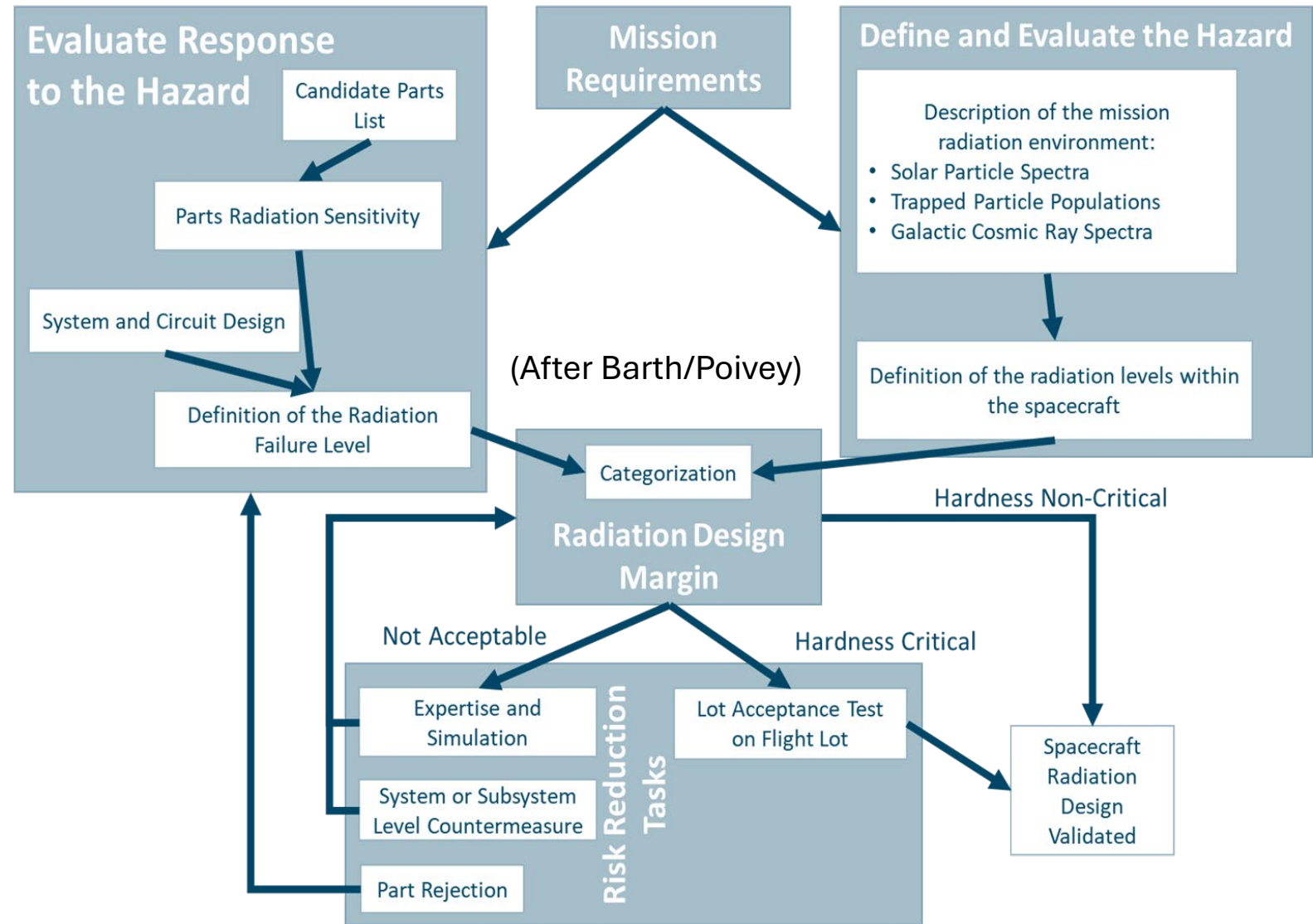
Risk
quantification

Maintainability
& validation

Environment and
end-user/project/program driven

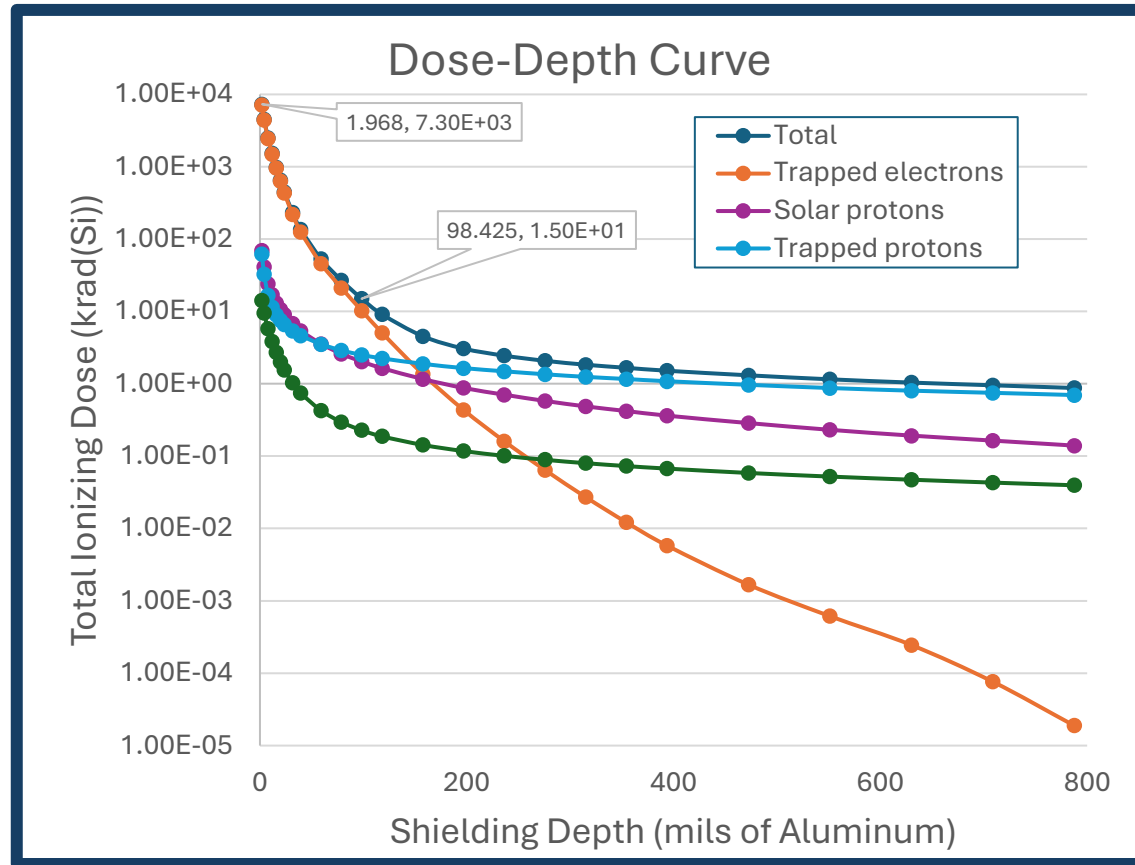
Designing for tolerance - RHA flow

- Hardness Assurance is the practice of designing for radiation effects
- What it takes to overcome the radiation challenges
- Competing failure modes



Shielding helps – to an extent

Cumulative Dose

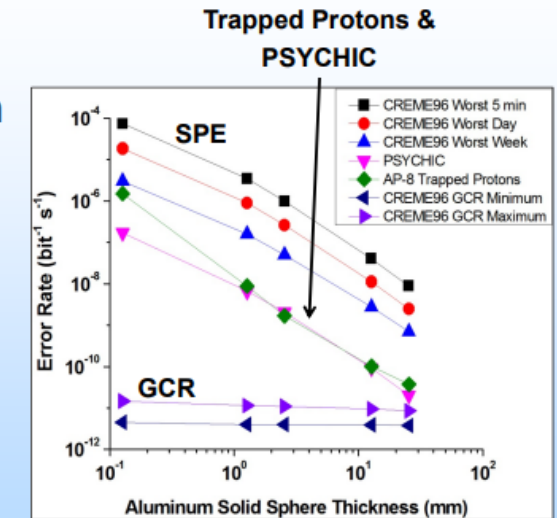


Single Events

45 nm SOI SRAM Soft Error Rates



- Shielding has significant impact on both solar event radiation (SPE and PSYCHIC) and trapped protons, but not GCR



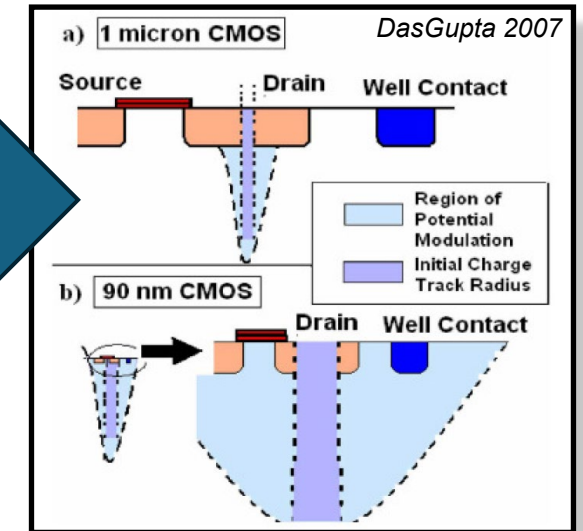
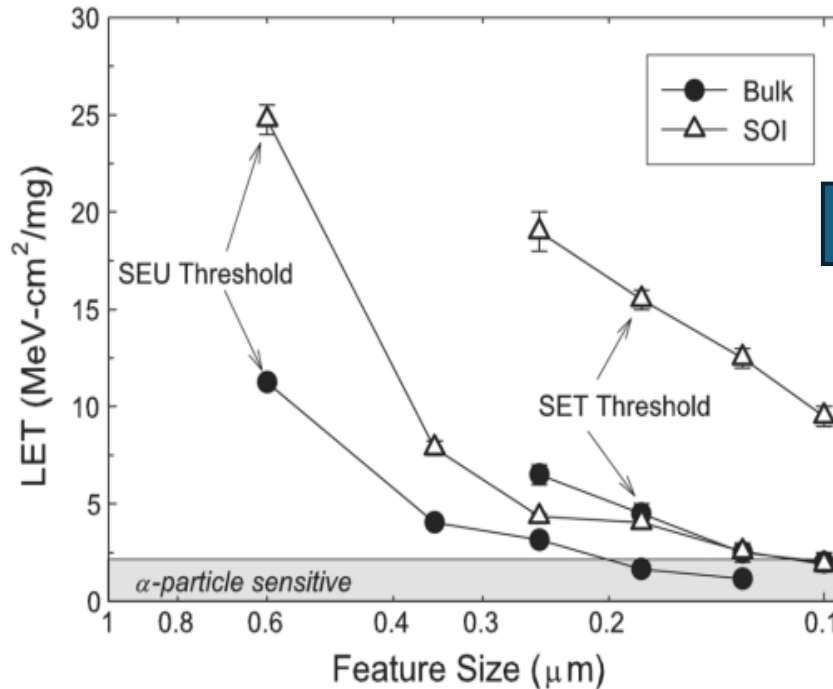
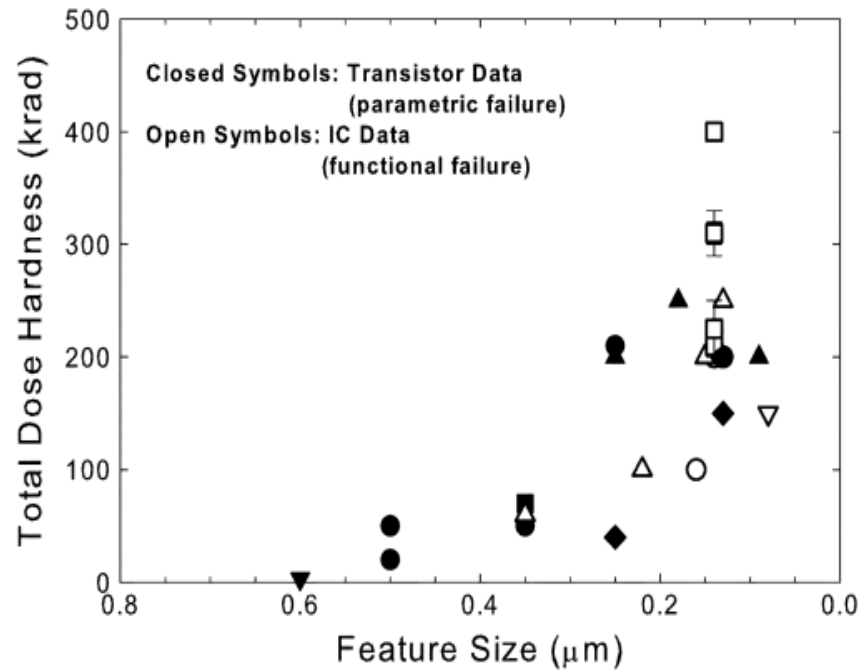
Trapped proton environment dominates error rate under ambient conditions

Presented by J. A. Pelish at the 2010 Nuclear and Space Radiation Effects Conference (NSREC), Denver, CO USA 19-23 July 2010 and published on <http://radhome.gsfc.nasa.gov/> and <http://www.nepp.gov/>.

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Commercial scaling of semiconductor devices

For CMOS in general, the scaling of feature size is increasing resilience with respect to dose and **increasing the susceptibility** to single event effects.



P. E. Dodd, M. R. Shaneyfelt, J. R. Schwank and J. A. Felix, "Current and Future Challenges in Radiation Effects on CMOS Electronics," in IEEE Transactions on Nuclear Science, vol. 57, no. 4, pp. 1747-1763, Aug. 2010, doi: 10.1109/TNS.2010.2042613.

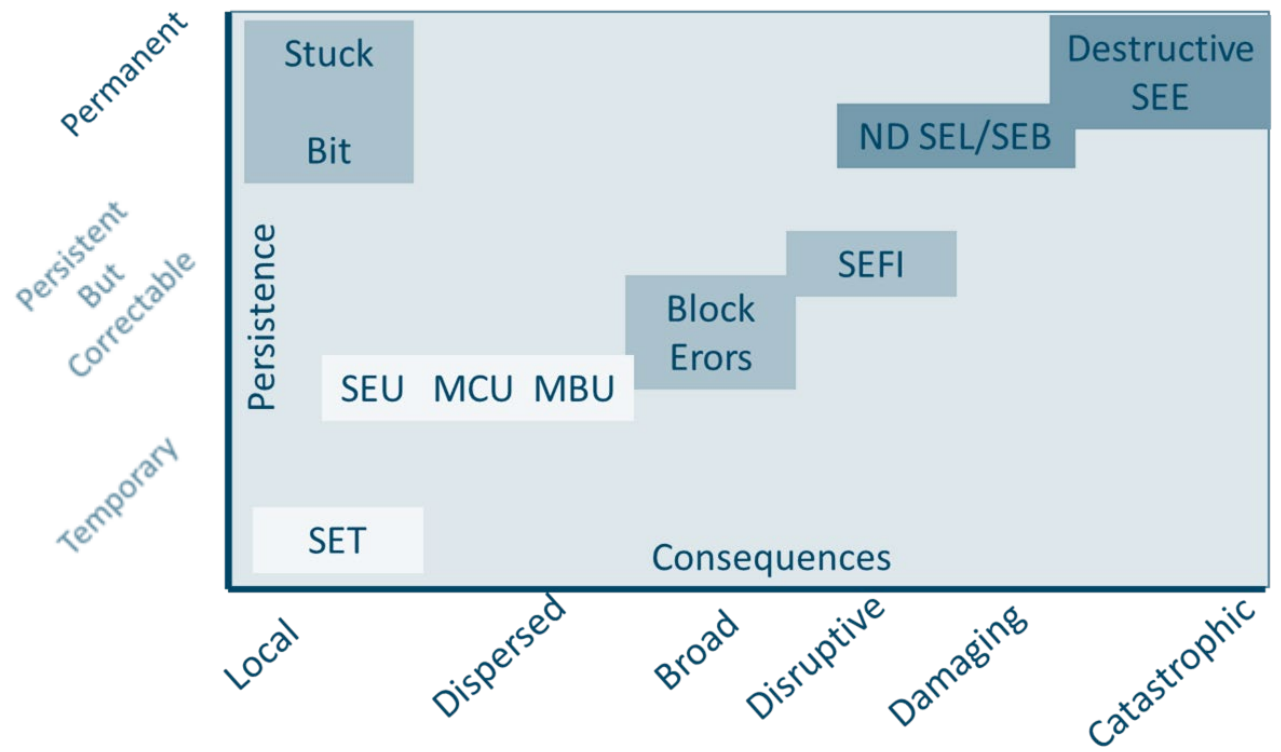
Types of Single Event Effects (SEE)

Destructive

- SEL - Latchup
- SEB - Burnout
- SEGR – Gate Rupture
- SEDR – Dielectric Rupture
- *SEU – Upsets can become stuck bits*

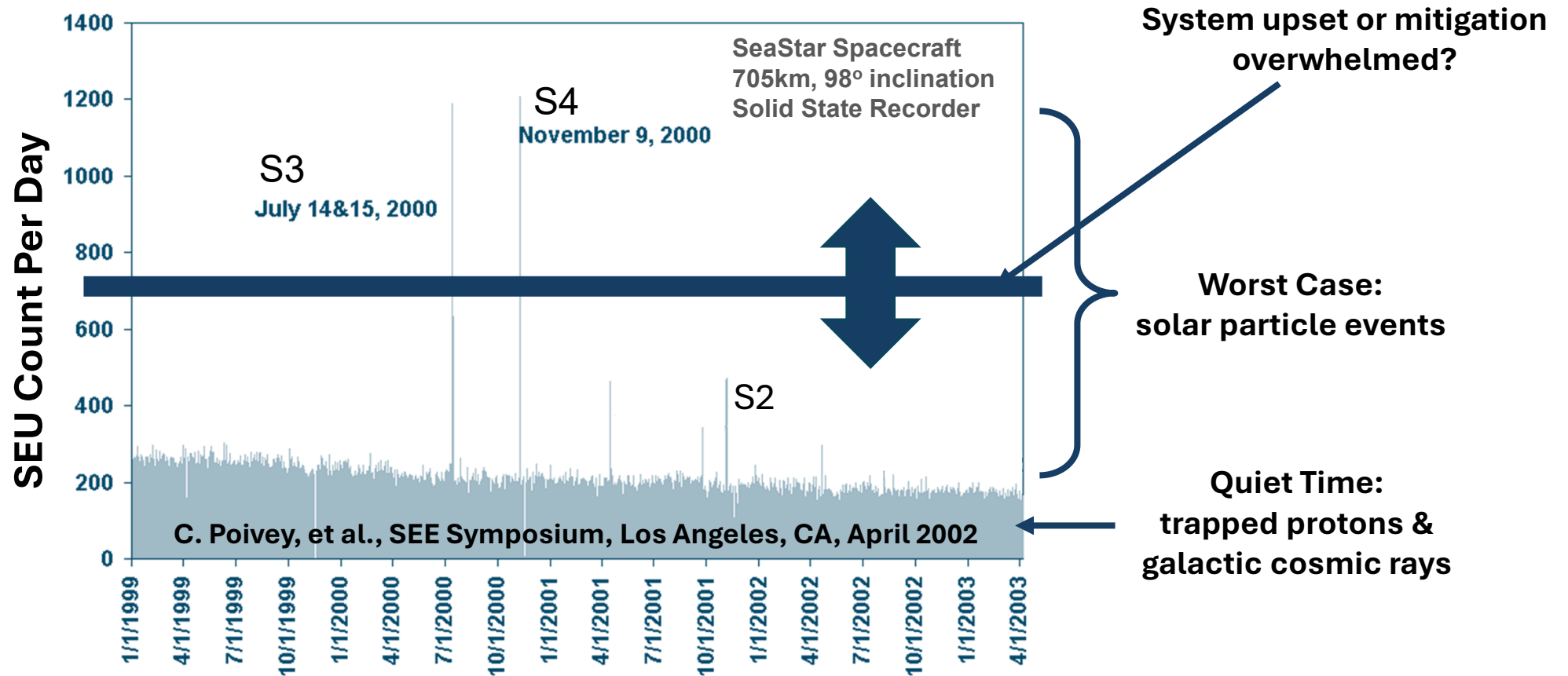
Non-destructive

- SET – Transients, can be analog and digital
- SEU – Upsets, can happen in multiple bits or multiple cells – MBU/MCU
- SEFI – Functional Interrupts, for complex devices, typical category for response that needs refresh/reset/power-cycle to return to operation
- Non-destructive does not mean non-disruptive



(After Ladbury)

How do you plan to mitigate?



Without information on the flight design, we don't know if we are in or out of bounds, this isn't just a parts selection question.

Deciding if you need to mitigate at all

Error-Functional

- High number of SEE signature allowable
- Design may inherently be indifferent to SEE signature with mitigation in place or robust design practices
- Nuisance or manageable function impacts (e.g. filtered transients, error detection and correction on memories) beyond part responses
- No action needed

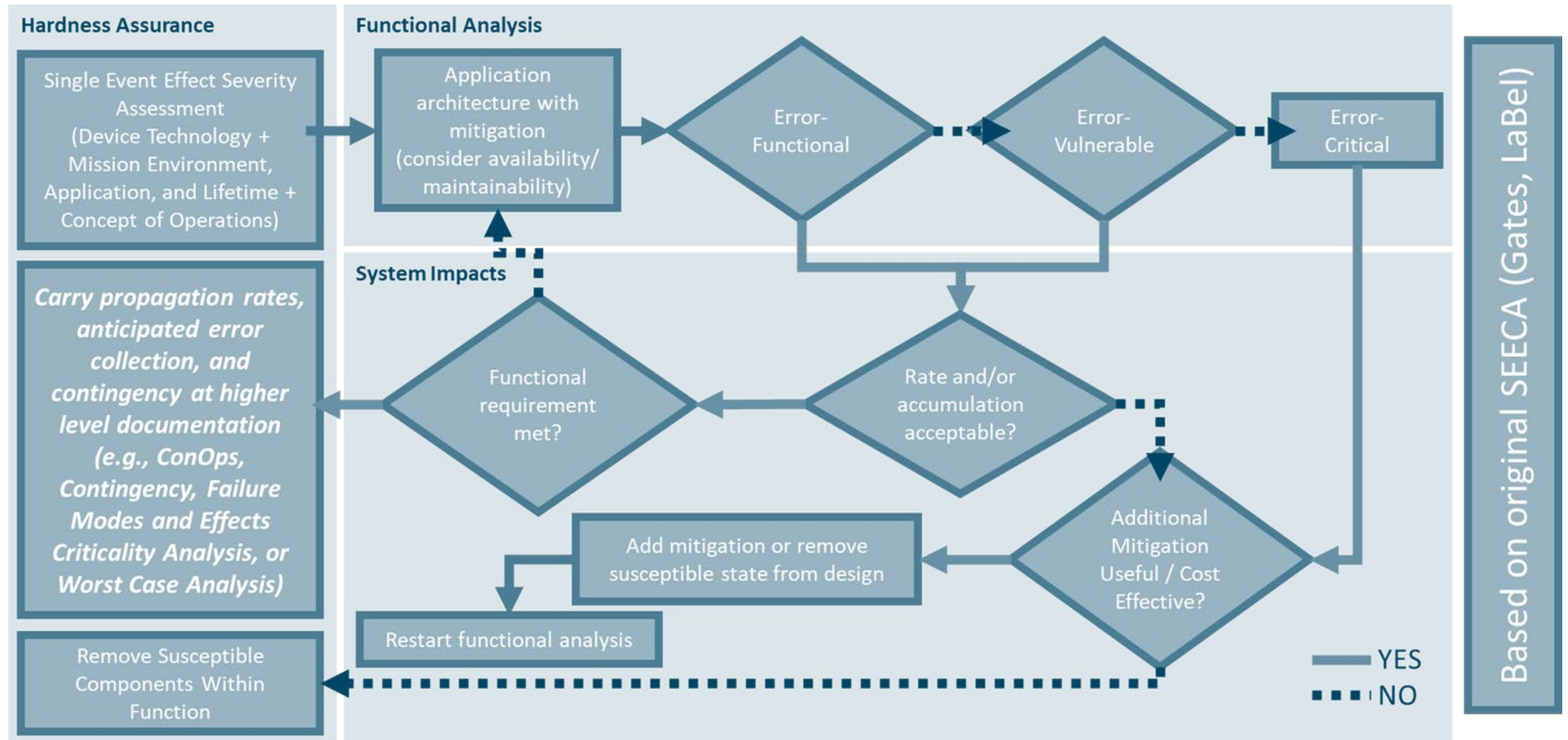
Error-Vulnerable

- Low number of SEE signature tolerable
- Design may require function for small window of availability or spend very little time in the susceptible state
- Mitigation needed in order to be reclassified as error-functional (e.g. SEFI of Flash, Multi-bit upsets)
- Ground or autonomous operations must be anticipated

Error-Critical

- SEE signature not allowable
- Disruption of function identified as single point of failure or design cannot continue to perform after SEE
- Mitigation needed in order to be reclassified as error-vulnerable (e.g. destructive SEL, many error accumulation, boot image corrupted due to error accumulation, SEFI that requires ground intervention or box level reset waiting on ground)
- Anomaly review needed or loss of mission

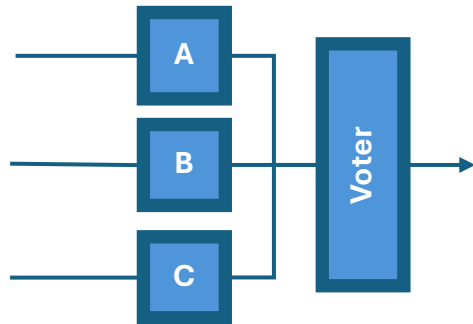
Mitigating with system architecture



Some Typical Mitigations

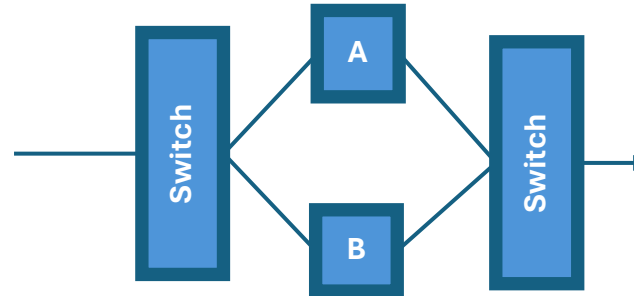
Triple Mode Redundancy

- Using redundancy and voting to mask SEE
- Frequently used in FPGA fabric of combinatorial logic
- Local, Block, Global all have trades associated with SEE response



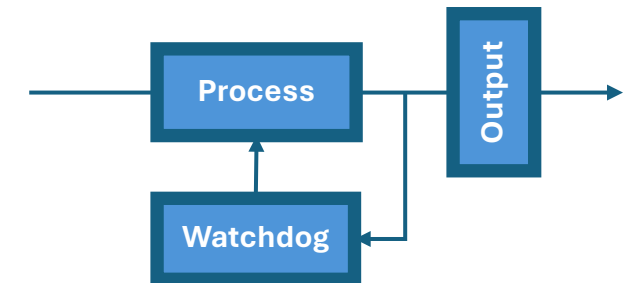
Cold Sparing

- Backup systems that are unpowered and can replace a faulty system (side A/B)
- Will still accrue dose and sometimes errors while in off state

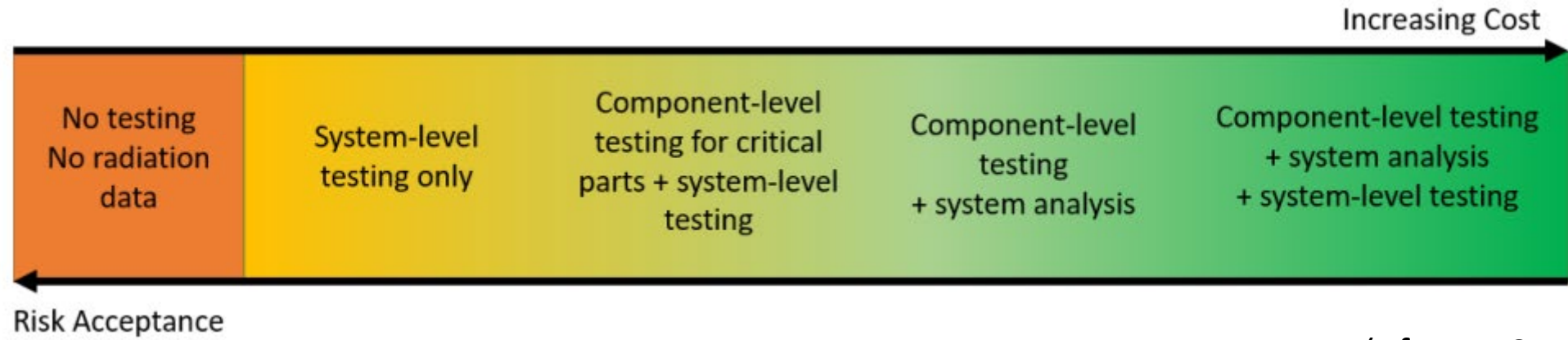


Watchdog Timers

- Feedback loop with expectation of current or power draw
- If operation is not performing check



Radiation Testing



(After A. Coronetti)

For TID we use energetic photons, typically gamma rays

They can be imparted uniformly and have good charge yield

For TNID we use energetic protons or neutrons avoiding coulombic interactions

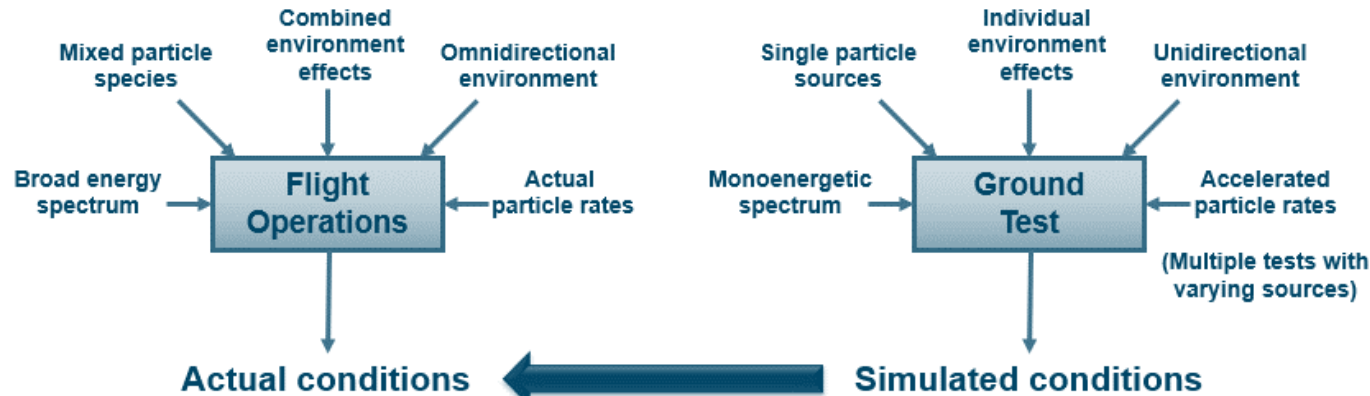
Can use mono-energetic fluences to represent full damage predicted in environment if the material follows Non-ionizing Energy Loss (NIEL) principles

For SEE we use heavy ions, protons (mostly secondaries), secondaries of neutrons, and sometimes pulsed laser

We try to know the amount of charge creation, so that we can estimate rates on-orbit

Test costs grow with complexity

How accurate is the ground SEE test in predicting space performance?



Graphic prepared by K. A. LaBel, NASA GSFC, 2008.

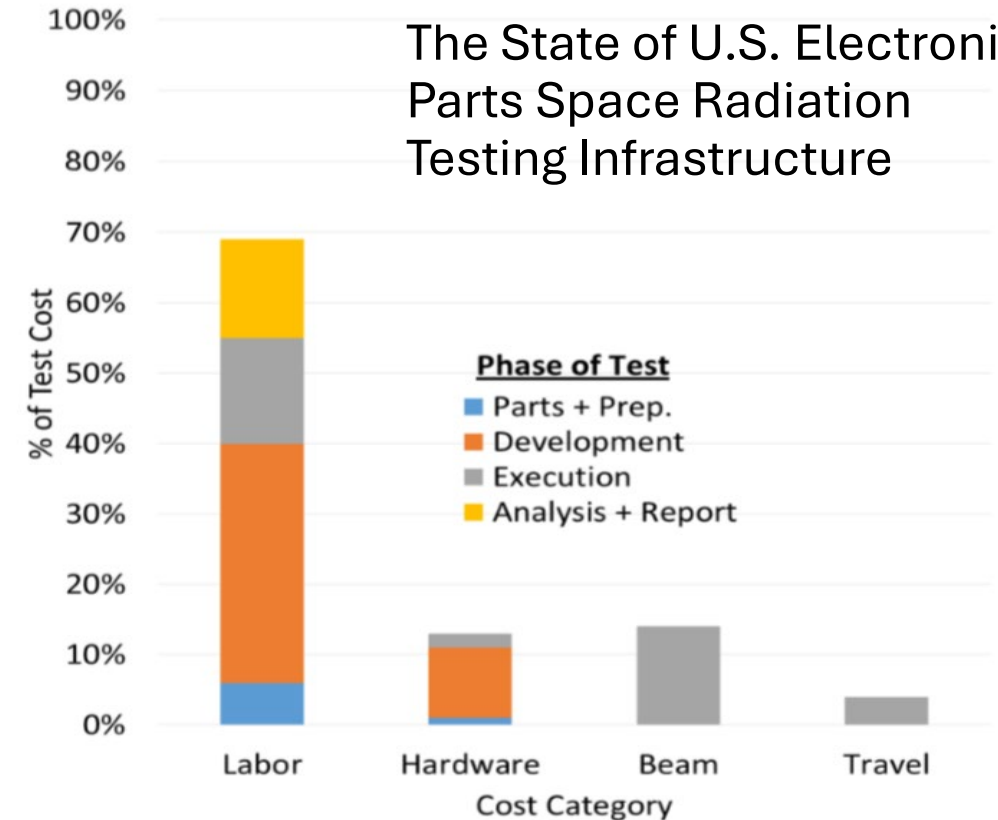
TABLE 3.2.1 Approximate Single-Event Effects Test Cost for Various Part Complexities and Packages (in thousands of dollars)

Part Complexity/Package Difficulty	Easy	Moderate	Difficult
Simple (Op. Amp, Comparator, etc.)	25–35	35–45	>50
Moderately Simple (ADC, DAC, SRAM, etc.)	40–75	50–85	>100
Difficult (Flash, DRAM, Simple Processor, etc.)	85–150	100–200	>250
Very Difficult (FPGA, Complex Processor, other highly complex and highly integrated components)	>500	>550	>600

NOTE: ADC, analog-to-digital converter; DAC, digital-to-analog converter; DRAM, dynamic random-access memory; FPGA, field-programmable gate array; SRAM, static random-access memory.

Pulled from the NAS Study:
Testing at the Speed of Light

The State of U.S. Electronic Parts Space Radiation Testing Infrastructure



To Clarify

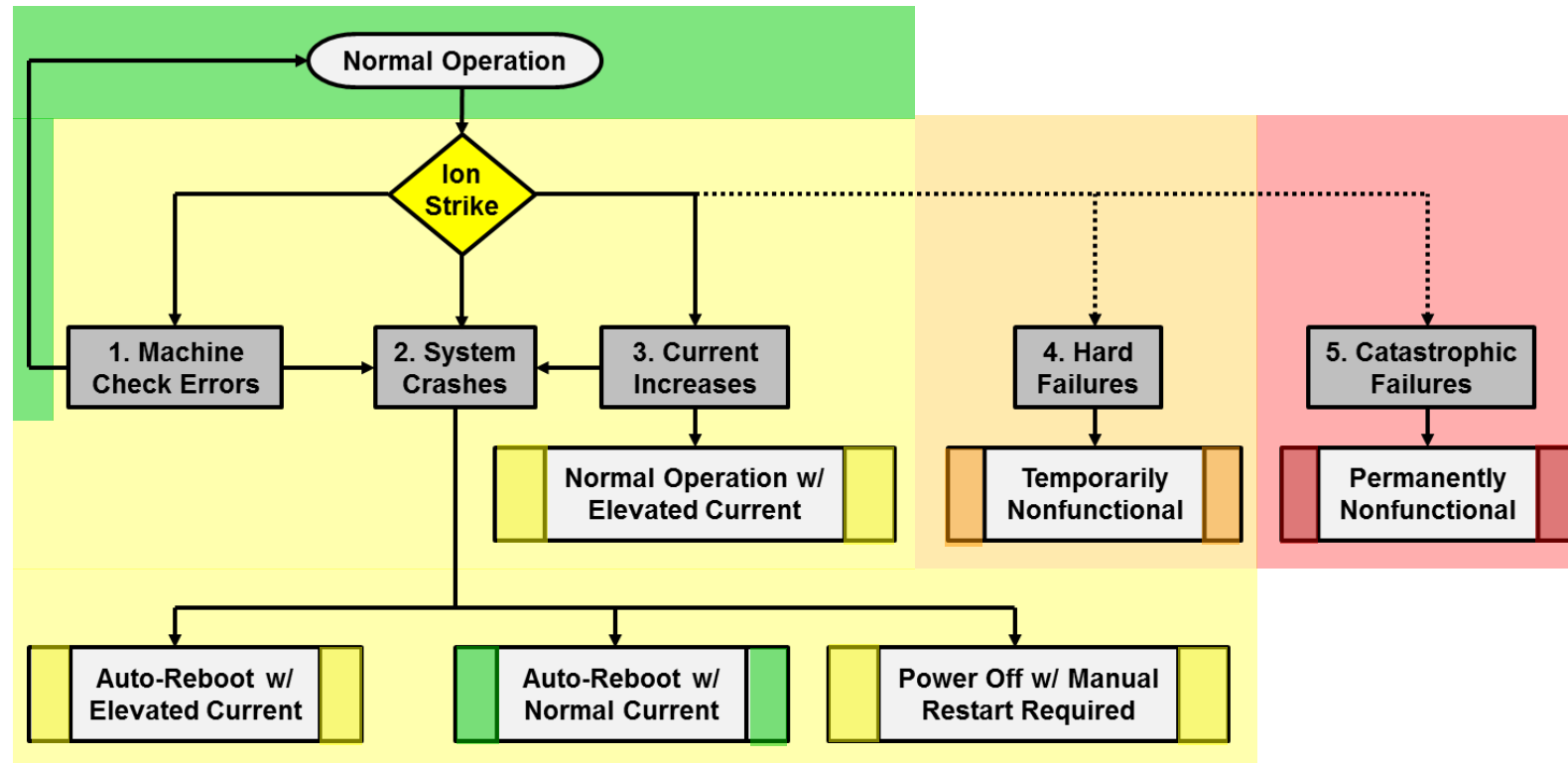
We do radiation tests to

- Ensure mission lifetime needs are met
- Characterize Error Signatures,
- Anticipate Event Rates, and,
- To maximize efficiency (time lost) for Event Recovery.

The point is to return to a known state in a deterministic manner after the event to allow functions to continue.

Test Flow & Fault Tree

These qualitative bins are how we attempt to classify error signatures recorded during testing. A disturbance is not the same as an upset. There are recoverable errors, much like there are unrecoverable ones.

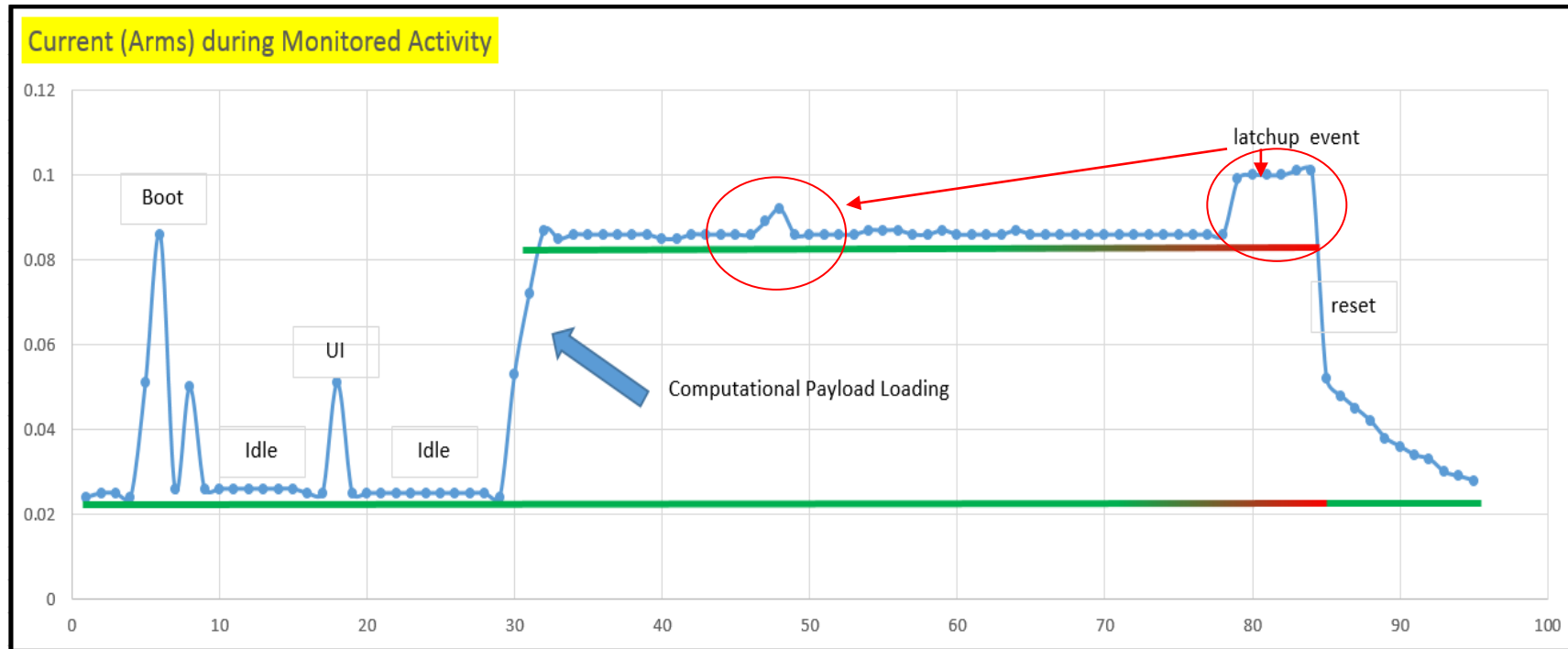


Adapted from Edward Wyrwas' presentation from the 12th Space Computing Conference in Pasadena, CA. July 30 – August 1, 2019. STI DAA number 20190028690

Identifying Patterns to Create Mitigation Solutions

If we can identify an electrical behavior which indicates particle collisions are happening, then we can abort a computational routine to save the science payload or isolate the component in question.

For the NVIDIA TX2, we can simply monitor current consumption against a threshold. When that threshold is exceeded, we disregard the current computation, reset the system to prevent bad data, and avoid a system crash.



Intentional test results can increase fidelity

Bounding allows for engineering trades to be explored

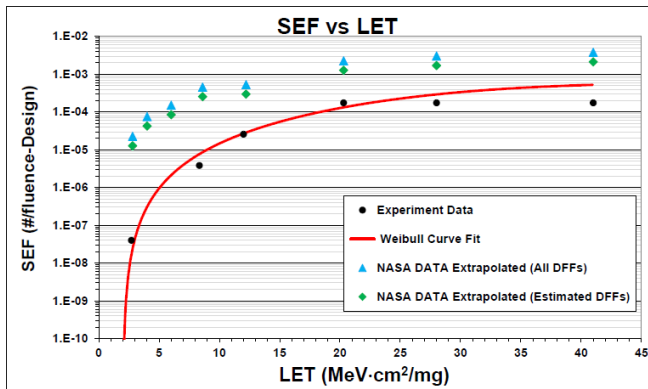
Complex devices need targeted application-based test campaigns

Test-As-You-Fly versus Extrapolation Data

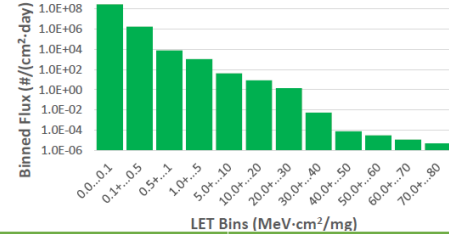
Test-as-you-fly data were able to prove (statistically) mission requirements will be met.

SEF: single event failure

LET: Linear energy transfer



Worst Week 350 mils



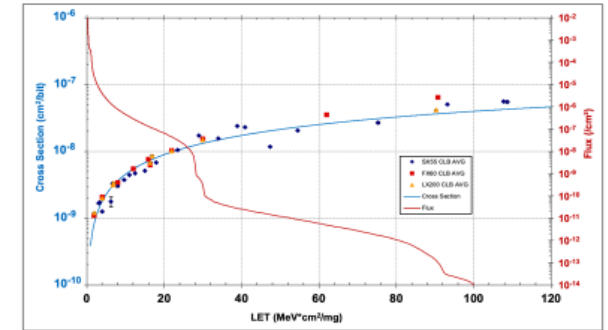
LET Range	Fluence/Day
0.1 ...0.5	1.8×10^6
0.5 ...1.0	7.6×10^3
1.0 ...5.0	1.0×10^3
5.0 ...10.0	4.2×10^1
10.0 ...20.0	8.4×10^0

To be presented by Melanie Berg at the Microelectronics Reliability & Qualification Working Meeting (MRQW), El Segundo, CA February 8, 2023

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Predicting on-orbit rates

- There will be different rates for different environmental conditions
- There are more than one ways to get a rate estimation
- All are similar in that you must consider the environment and part sensitivity
- Calculation is forgiving



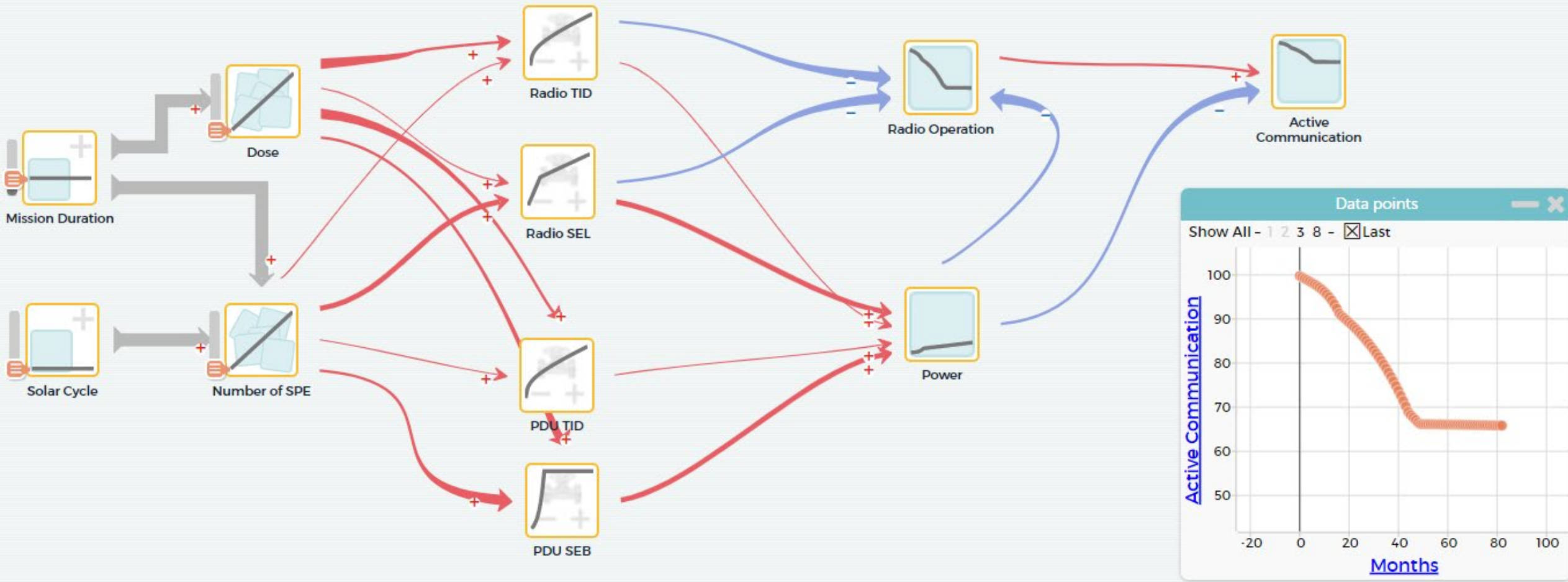
$$\text{Rate} = \int \underbrace{\frac{d\text{flux}(LET, \theta)}{dLET}}_{\text{environment}} \cdot \underbrace{\sigma(LET, \theta)}_{\text{device response}} d\theta dLET$$

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System Functional Impacts

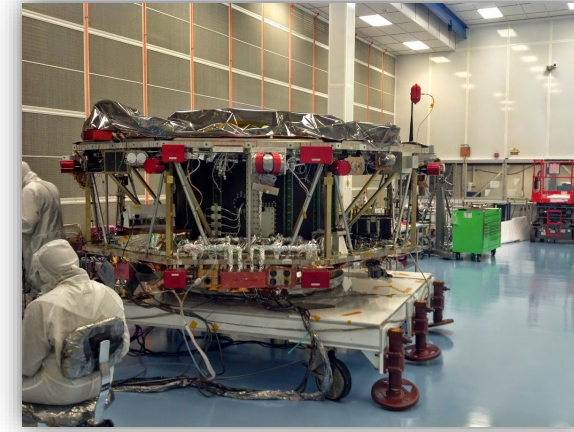
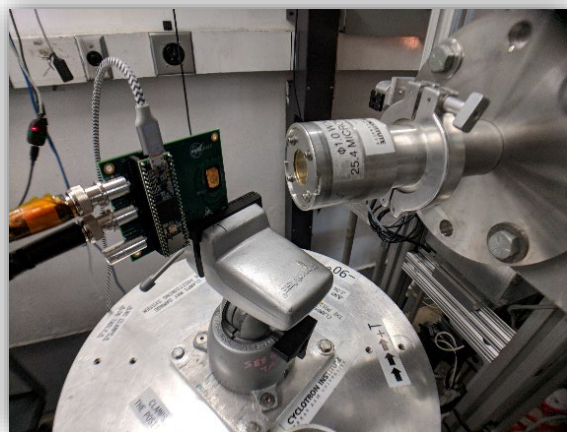
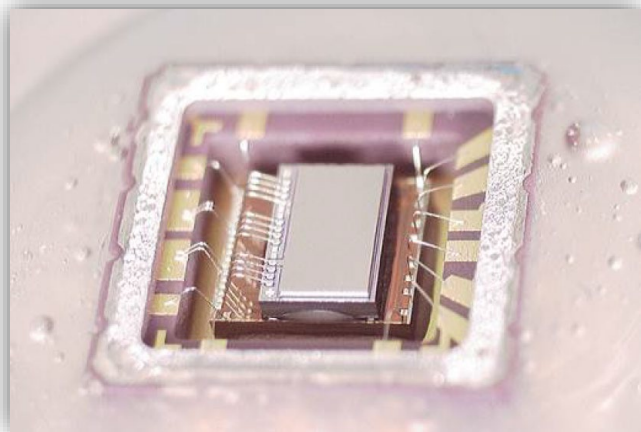


Takeaways

- Use the parts that get you the science you want
 - Gather relevant information on the process and pathfinding tests from research publications
 - Avoid pitfalls by not just using the newest thing because it's new
- Only add mitigation where you need it
 - Use shielding wisely
 - Adding complexity can create more problems
- Radiation testing plays a crucial role
 - Pre-existing data
 - Data representation is caveat emptor
 - Application specific driven characterization will give you the best information for engineering trades
- Model your environment
 - Low level efforts for impactful design trades and awareness
 - Radiation sources and intensity vary greatly

When you need to be careful

- Seek Expert Opinions
 - Electronics on booms or external to the spacecraft
 - Cryogenic detectors/ASIC/FPAs
 - Long duration GEO or Jovian missions
 - Science data is worst case environments (flares/CMEs)
- Using heritage
 - Manufacturing changes of the die change the radiation response
 - Short LEO missions are not indicative of all environments



Thank you

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Reference Material

Part Summary for TID

Technology Category	Sub Category	Effects
MOS	NMOS PMOS CMOS CMOS/SOS/SOI	Threshold voltage shift Decreased in drive current Decrease in switching speed Increased leakage current
BJT		H_{fe} degradation
JFET		Enhanced source drain leakage current
Analog microelectronics		Change in offset voltage and offset current Change in bias current Gain degradation
Digital microelectronics		Enhanced leakage Logic failure
CCDs		Increased dark current Effects on MOS transistor elements
CIS		Same as CCD and change in pixel amplifier gain
Quartz resonant crystal		Frequency shifts

TOTAL IONIZING AND NON-IONIZING DOSE RADIATION HARDNESS ASSURANCE
(cern.ch)

Part Summary for TNID

Technology category	Sub-category	Effects
General bipolar	BJT	hFE degradation in BJTs, particularly for low-current conditions (PNP devices more sensitive to DD than NPN)
	Diodes	Increased leakage current increased forward voltage drop
Electro-optic sensors	CCDs	CTE degradation, Increased dark current, Increased hot spots, Increased bright columns Random telegraph signals
	CIS	Increased dark current, Increased hot spots, Random telegraph signals Reduced responsivity
	Photo diodes	Reduced photocurrents Increased dark currents
	Photo transistors	hFE degradation?? Reduced responsivity?? Increased dark currents??
Light-emitting diodes	LEDs (general)	Reduced light power output
	Laser diodes	Reduced light power output Increased threshold current
Opto-couplers		Reduced current transfer ratio
Solar cells	Silicon GaAs, InP etc	Reduced short-circuit current Reduced open-circuit voltage Reduced maximum power

[TOTAL IONIZING AND NON-IONIZING DOSE RADIATION HARDNESS ASSURANCE
\(cern.ch\)](https://cern.ch)

Part Summary for SEE

Type of SEE	Effect	Type of devices sensitive
Single Event Transient (SET)*	Impulse response of a certain amplitude and duration	all
Single Event Upset (SEU)	Corruption of the information stored in a memory element	Memories, latches in logic devices
Multiple Cell Upset (MCU)	Several memory elements corrupted by a single ion or proton strike	Memories, latches in logic devices
Single Event functional Interrupt (SEFI)	Corruption of a data path leading to loss of normal operation	Complex devices with built-in state machine/control sections
Stuck bit / Intermittent Stuck bits (ISB)	Permanent or semi-permanent corruption of the information stored in a memory element	DRAM, SDRAM, DDR, DDR2, DDR3, DDR4
Single Event Latchup (SEL)	High current condition	CMOS, BiCMOS devices
Single Event Burnout (SEB)	Destructive burnout due to high current conditions	N channel power MOSFET, diodes
Single Event Gate/Dielectric Rupture (SEGR/SEDR)	Rupture of a (gate) dielectric due to high electrical field conditions	Power MOSFETs, Non volatile memories, linear devices,....

* Fundamental to all non-destructive SEEs

[TOTAL IONIZING AND NON-IONIZING DOSE RADIATION HARDNESS ASSURANCE \(cern.ch\)](https://cern.ch)