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System for Long-Duration Electrical Testing of SiC IC Generation 12 Chips at 500 °C

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Summary

The system described in this report is an improved testing rig designed to enhance measurement flexibility, provide a compact oven footprint, and reduce costs for parallel oven-testing silicon carbide (SiC) integrated circuit devices at 500 °C for long durations (greater than 100 h). The testing rig design was characterized in terms of the ovens' internal and external temperatures, system noise, and the leakage properties of their substrate/inner boards, where the devices under test (DUTs) reside. The test rig employs a National Instruments (NI) Peripheral Component Interconnect eXtensions for Instrumentation (PXI) measurement system, room-temperature pin-switching/customizing boards, and high-temperature compact ovens.

Nomenclature

AI	analog input
AO	analog output
ASIC	application-specific integrated circuit
CC	closed circuit
COTS	commercial off-the-shelf
DC	direct current
DUT	device under test
FFT	fast Fourier transform
GND	ground
IC	integrated circuit
JFET-R	junction field-effect transistor and resistor
MUX	multiplexer
NI	National Instruments
OC	open circuit
PID	proportional-integral-derivative
PXI	Peripheral Component Interconnect eXtensions for Instrumentation
SiC	silicon carbide
SMU	source-measure unit
VDD	positive supply voltage
VSS	negative supply voltage

1.0 Introduction

At the NASA Glenn Research Center, a team has been advancing an area of extreme-temperature silicon carbide (SiC) junction field-effect transistor and resistor (JFET-R) integrated circuits (ICs)

(Refs. 1 and 2). To characterize these devices, an improved testing rig capable of making long-term electrical measurements of multiple chips in parallel at 500 °C was required. This improved testing rig addresses three recognized drawbacks of the team's previous testing rig approaches: (1) oven size, (2) the cost of temperature tracing, and (3) customizable electrical measurement connections specific to a wide variety of IC designs.

Because the SiC ICs are no more than 5 by 5 mm in size, an oversized industrial oven was not needed for high-temperature testing. Using too large of an oven not only wastes energy but creates heat gradients, with fluctuations of ±25 °C from the steady-state setpoint temperature (Ref. 3). Smaller ovens allow testing larger numbers of chips in parallel in far less laboratory space and at a considerably lower energy cost.

The redesigned testing rig also had to cost-efficiently bring conductive signal traces from the hot zone to the room-temperature measurement instrument. In previous large-oven testing setups, long, 10-mil-diameter gold wires were used to make connections to the ovens at a cost of approximately $1,000 per oven. To save costs, these wires were generally reused from test to test, as long as they had not been exposed to temperatures >500 °C. However, a more robust and cost-efficient test platform was sought to eliminate these gold wires, as well as save researchers/technicians time and energy.

The NASA Glenn prototype JFET-R IC Generation 12 chipset includes more than 30 different application-specific integrated circuit (ASIC) chip designs that require electrical testing (Ref. 4). The majority of these chips comprise multiple smaller ICs. Given that each IC/chip type to be tested is unique, the testing rig requires customized routing of signals between chips and measurement instrumentation. The variety of circuits being tested meant this new testing rig had to be able to handle signal routing through automated software-driven relay switching rather than by making hard-wired connections. By sequentially switching between ICs and ovens through software control commands, the various ICs housed in different ovens can readily be measured independently over the course of testing.

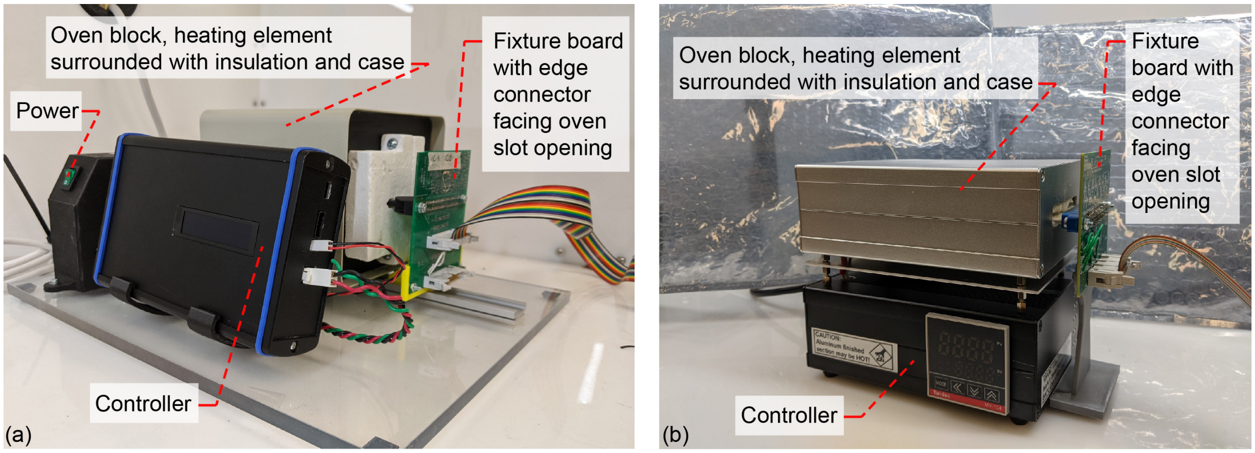

Figure 1.—Before and after comparison of small oven testing rigs with ceramic board inserted and connected to vertical fixture board. (a) Oven setup described in (Ref. 5) with 30.48- by 30.48-cm footprint. (b) Generation 12 small oven with 10.77- by 15.24-cm footprint.

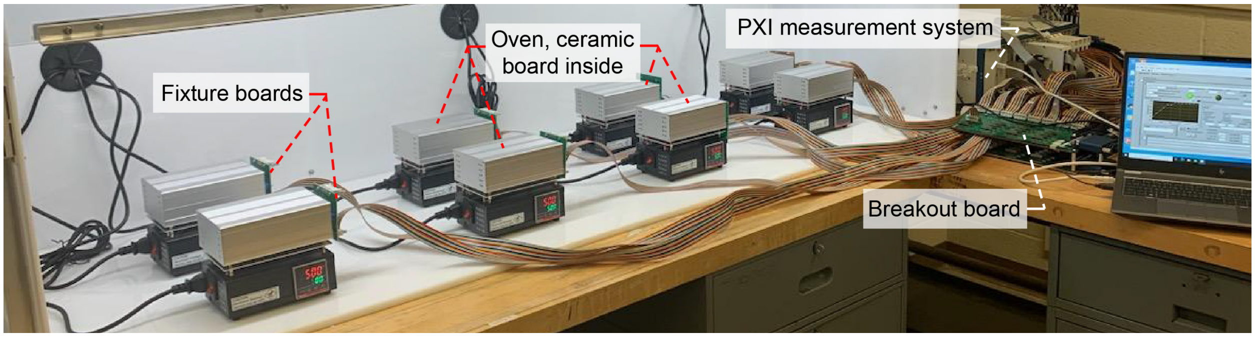

Figure 2.—Major components of Generation 12 oven testing setup.

This new oven setup, depicted in Figure 1(b) and Figure 2, is part of a larger testing rig design. Figure 2 shows several key components: a compact measurement system based on the Peripheral Component Interconnect eXtensions for Instrumentation (PXI) platform, breakout boards for organizing ribbon cables that connect to each small oven, fixture boards mounted immediately next to each oven, ceramic substrate boards extending into a slot opening of each oven, and eight small ovens. The chassis-based PXI measurement system (described in detail in Section 4.0) is configured with two forms of software-controlled reed-relay multiplexer (MUX) switching module cards. These cards are designed to switch signals between the fixture board and the matrix module cards; a LabVIEW®-based (National Instruments (NI)) software application controls connecting specific IC input/output signals to specific instruments mounted in the PXI chassis.

The breakout boards connect each oven's ASIC-specific fixture board to the PXI MUX cards; they can be reconfigured depending on the ASICs being tested and the allowed topology of the MUX module cards. These breakout boards connect to each individual fixture board via the ribbon cables running to each oven; two 20-pin connectors per fixture board include dedicated positive supply voltage (VDD), negative supply voltage (VSS), and ground (GND) pins and enable up to 32 signals to be sourced or measured by the PXI measurement system instrumentation. The fixture boards contain jumpers and/or 20 mΩ resistors that facilitate rapid pretest configuration of the fixture boards to the desired IC testing connections. The ceramic substrate boards bridge signals between the ceramic-packaged chip residing in the hot zone; the fixture boards with female edge connectors are located just outside each oven's slot opening. The ceramic boards,[1] made of aluminum oxide (Al_2O_3), are screen printed with DuPont® 5771 conductive gold tracing. DuPont® 5771 was chosen from the prospects studied in Reference 6 because its properties allow it to bond with alumina and alumina nitride element makeups. The layout of conductive traces on these ceramic boards can be changed to accommodate specific ceramic chip package designs. For example, three substrate board designs have been created to handle the three different ceramic chip package designs (with 16, 24, and 44 pads, respectively, as detailed in Ref. 7) that will be used to package almost all of the Generation 12 ASIC chip designs.

This report details the latest advancements to the multiple small oven parallel testing approach beyond its initial implementation, which was shown in Figure 1(a) and described in Reference 5. This second version builds upon the lessons learned from the first version, including: (1) the use of the NI PXI system, which provides modularity, compactness, and programming of electrical test instruments and signal-routing switch relay matrices and (2) the use of ceramic substrate boards, one end of which holds the chip and is inserted into the oven while the other end extends from the oven and provides electrical

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[1] Thick Film Technologies (https://www.thickfilmtech.com/) provides these substrate boards to the team.

edge connections. These ceramic boards dissipate heat well enough to use room-temperature edge connectors and circuit boards to assist in bias/measurement signal routing.

Several more lessons learned during the development of the first version of the testing rig led to improvements that were incorporated into the second version's design:

1. The first version's (Ref. 5) oven heater block involved molding ceramic casings, which took extra fabrication time. Given that the team does not often test the SiC ICs at temperatures higher than 500 °C, the ceramic-encased heaters were replaced by commercial off-the-shelf (COTS) modular heaters, eliminating the need to add ceramic encasing.
2. The oven controller electronics for the first version (Ref. 5) were built by hand, which demanded a less than optimal number of construction and debugging labor hours. The oven control electronics have been updated to use COTS parts with plug-and-play characteristics that save time and energy.
3. Using a NI SwitchBlock module in the first version of the rig limited the switching to just 16 signals per oven/chip. This limited the number of signal pins available for future ICs and was incompatible with testing more complex Generation 12 SiC chips, some of which require 32 signals.
4. Room-temperature fixture boards that routed the signals from each high-temperature oven to the measurement system were unique to each chip design, requiring population of many fixture boards of different designs. Given that the signal connections were soldered, each unique fixture board was incompatible with testing different IC designs subsequently.

The Generation 12 testing rig was designed to be flexible enough to accommodate upcoming generations of SiC ICs with minimal modifications. These modifications might include the following:

1. The ability to increase from 32 to 64 testing signals to accommodate future, more complex SiC ASICs.
2. Fixture boards that allow any substrate board trace to be connected to power, ground, or signal with simple jumpers. The signals would provide at least two redundant connection paths to the PXI chassis.
3. A physically thicker breakout board to handle the heavy connectors and push and pull of the oven connectors to prevent breaking the internal board traces.
4. Daisy-chaining an additional PXI chassis and related module cards to the first chassis to allow incorporating additional ovens into the testing rig to handle testing more ICs.

The remainder of this report describes the construction and characterization of key aspects of the second version of the small oven rig: Section 2.0 describes these new Mark I ovens, as well as internal and external thermal measurements. Section 3.0 discusses the ceramic substrate board performance and presents examples of some circuit-specific fixture boards. Section 4.0 provides details of the switching and measurement system, along with the noise floor measurements. Section 5.0 summarizes the work and possible further testing rig advancements, areas of growth, and an overview of all the calculations from the previous sections.

2.0 Mark I Compact Test Oven

A new set of compact ovens (designated Mark I) were designed, drawing upon experiences gained from the work described in Reference 5. The footprint of each Mark I oven was less than 106.68 by 152.4 mm, with a 27.94- by 12.7-mm oven opening to accommodate the largest Generation 12 ceramic chip package height of 3 mm (Ref. 7). A design and assembly instruction guide for the Mark I oven is available through NASA's NTRS website (Ref. 8). These ovens were built to maintain the internal temperature at a specific setpoint using a commercially available proportional-integral-derivative (PID) controller. For initial testing, the Mark I oven's setpoint is 500 °C,[2] which is consistent with specific NASA needs, including the robotic exploration of Venus's surface. Eight Mark I ovens were initially built for this testing rig, even though the testing rig architecture can be expanded.

A few key characteristics were tested as part of qualifying the new ovens for long-duration 500 °C testing of chips, including the internal temperature dispersion (Section 2.1) and external thermal measurements (Section 2.2). The internal oven temperature gradient tests were necessary to make certain (1) the center of the IC follows the setpoint within a tolerance of ±5 °C, and (2) the temperature difference from the center of the IC to the edge of the package remains less than 35 °C to prevent ceramic cracking.[3] The external thermal measurements were performed for (1) safety knowledge, (2) confirmation that close-proximity conventional-temperature electronic components remain within their safe temperature specifications, and (3) verification that edge connectors can safely attach to the end of the ceramic substrate board that remains outside of the oven during testing.

2.1 Internal Oven Characterization

Tests were conducted to characterize the internal oven temperate versus position and time profiles. Three calibrated type-K thermocouples were positioned approximately 88.9 mm inside the oven opening (Figure 3), roughly where the SiC ASIC would normally reside while the oven was heated up using its internal PID controller's cylindrical heaters and type-K thermocouple. The substrate board thermocouples are each separated by 5 mm between A and B and between A and C, on a Generation 11 substrate board without a chip or package mounted on it. The center on a Generation 11 substrate is comparable to the Generation 12 substrate locations because the ceramic board is the same width, length, and thickness. The temperature of the Mark I oven was controlled using the PID control parameter values found in (Ref. 8) up to 300 °C. At this point, it was allowed to stabilize at this setpoint for at least 15 min before ramping up another 100 °C. These ramping and stabilization steps were repeated at 400 °C and again at 500 °C.

Oven ramp rates per setpoint and PID value constraints are also evident from the data in Figure 4. From room temperature to 300 °C, a ramp rate of 18 °C per min was attainable. This differs from the ramp rate from 400 to 500 °C, which was only 5.74 °C per min. This higher temperature makes for a slower ramp rate because it requires more frequent use of the heaters. In addition, when the oven's setpoint is relatively close to its present temperature, the PID controller will not provide continuous power to the heaters; instead, it will pulse power in smaller increments to avoid overshooting the setpoint temperature. When the setpoint of an oven at room temperature is set to 500 °C (data not shown), its ramp rate is faster than either the room temperature to 300 °C or the 400 to 500 °C ramp rates because the PID controller will not limit the heater output until the temperature approaches 500 °C. The Mark I oven requires about 15 min to reach 500 °C when starting from room temperature.

Figure 5 shows the Mark I oven's cool-down without the use of any active cooling mechanism, only ambient air. The fastest cool-down from 500 °C to room temperature that the Mark I can accomplish is 3.6 °C per min linearly. As expected, the closer the Mark I oven's internals approached room temperature, the slower the cool-down rate was.

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[2] The setpoint should not exceed 600 °C unless a different metal is used; aluminum melting point is 660 °C.

[3] IC cracking has been observed on a probe station at a temperature gradient greater than 35 °C across the IC.

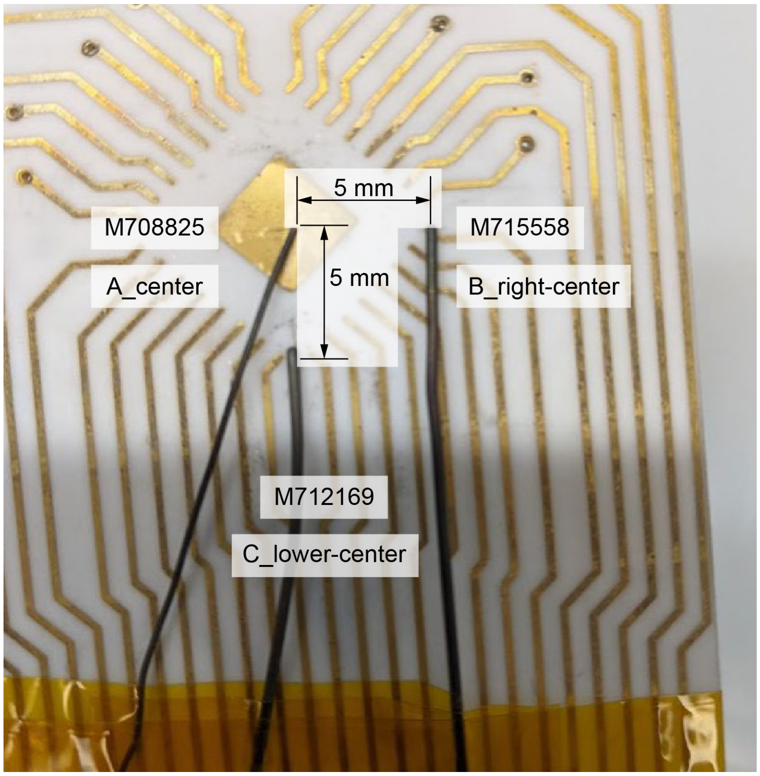


Figure 3.—Thermocouple locations on Generation 11 ceramic substrate (without chip package).

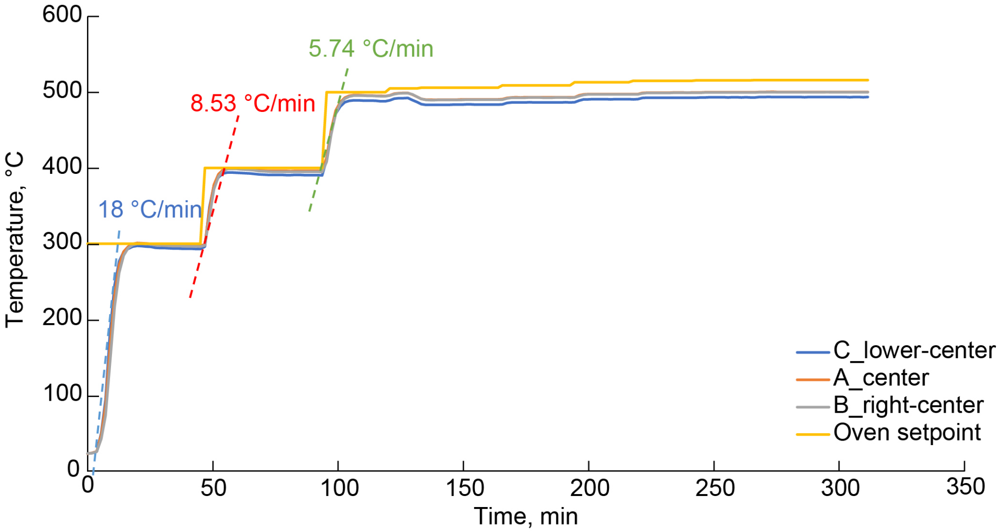


Figure 4.—Mark I oven temperature versus time profiles during heat-up.

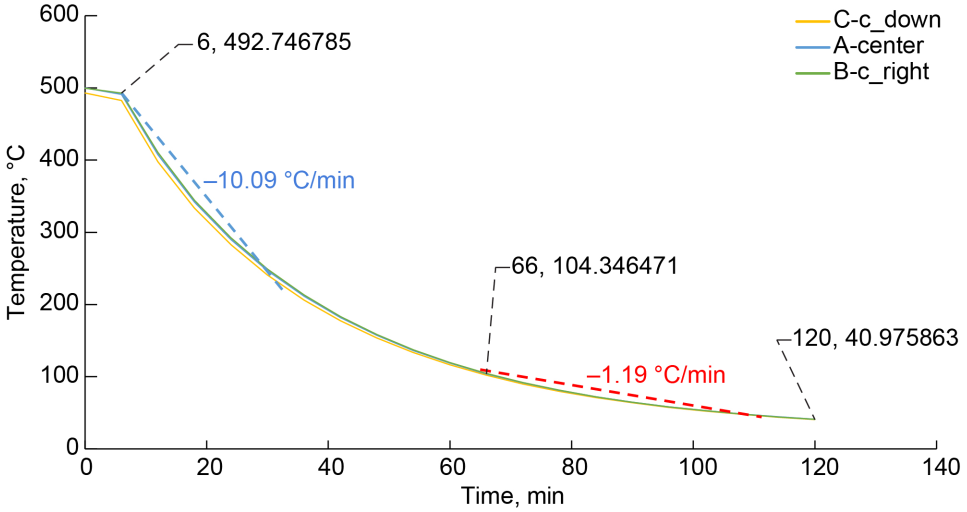


Figure 5.—Mark I oven temperature versus time profiles during cool-down.

2.2 External Temperature Measurements

Surface temperature measurements were taken at various locations outside three Mark I ovens (Figure 6) using a Fluke® Model 561 infrared thermometer after the ovens soaked at a 500 °C setpoint for 2 h. Oven 1 (Figure 7(a)) had two pieces of opening insulation inside the oven opening. Oven 3 (Figure 7(b)) contained one piece of opening insulation inside the oven opening. Oven 5 (Figure 7(c)) contained one piece of opening insulation inside and one outside the case's oven opening.

Interestingly, the outside surfaces of the oven heater block experienced significant temperature variations between the ovens. It was speculated that this might have been due to variations in the insulation stuffing or the infrared thermometer reflected inconsistently due to the shiny surface or the ridges of the silver aluminum case. Figure 6 shows that at the 500 °C setpoint, the outer box surfaces are hotter than 52 °C, so touching them for prolonged times is not recommended. To bring the exterior surface temperatures lower than 52 °C, a different insulation or doubling up internal box insulation would be required.

In Figure 6, it is interesting to note some of the similarities between the ovens. First, the drilled-hole vent case regions experienced cooler temperatures due to the airflow. Second, the central case regions maintained a steady temperature around 100 °C in all ovens.

As expected, the greatest variation seen in Figure 6 is at the edge where the opening of the oven is due to the differences in the insulation at the oven opening. To get a more complete picture of the oven opening, temperature measurements were taken on the fixture board as well (Figure 7). The room-temperature components used are rated up to 125 °C (Ref. 9). Only the Oven 1 insulation solution, two layers of insulation within the case at the oven opening, kept the components within their temperature specifications. It is worth noting that Oven 5, which contained an extra piece of insulation outside of the oven, seems to have redirected the heat upward, producing the 112.8 °C result seen in Figure 6(c).

To ensure that the Oven 1 insulation configuration could prevent fixture board failure over the long term, a 24-h test was conducted with all three ovens configured with two pieces of insulation inside the opening (i.e., the original opening insulation configuration of Oven 1). All three ovens passed the test; subsequently, all eight Mark I ovens were outfitted with a secondary insulation piece at the oven opening, allowing sufficient air to move between the fixture board and the hot oven. Unlike the other opening insulation configurations tested, this Oven 1 configuration kept the fixture board at acceptable temperatures. As expected, the further from the substrate board connector, the cooler the temperatures. Near the top and bottom of the fixture board, the temperatures cooled off to maximum measured temperatures of 79.4 and 39.4 °C, respectively.

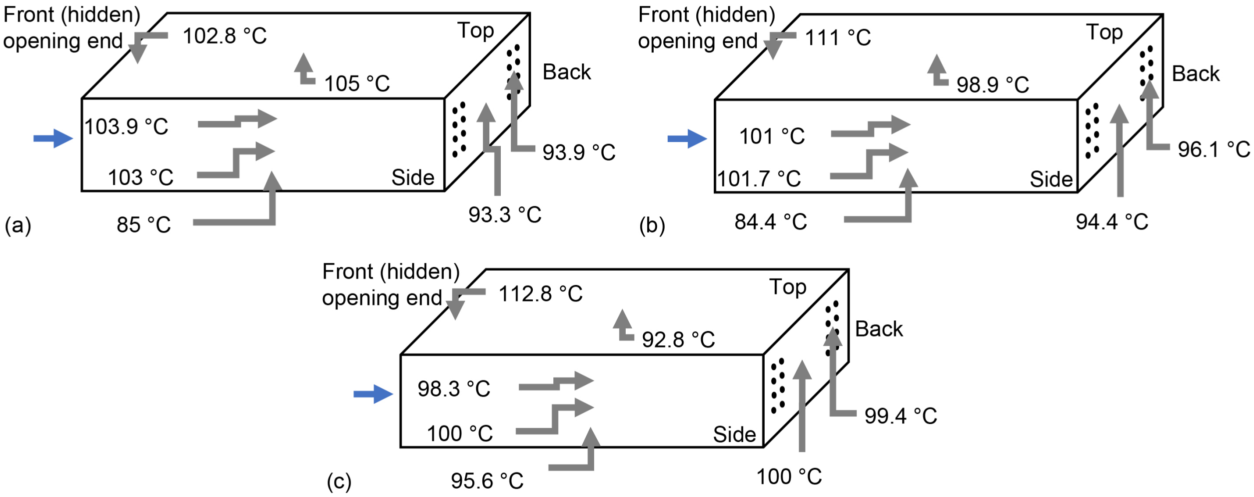


Figure 6.—Outer case temperatures measured on back and side of three Mark I ovens. (a) Oven 1 with two inside layers of insulation at oven opening. (b) Oven 3 with one inside layer of insulation at oven opening. (c) Oven 5 with one inside layer and one outside layer of insulation at oven opening.

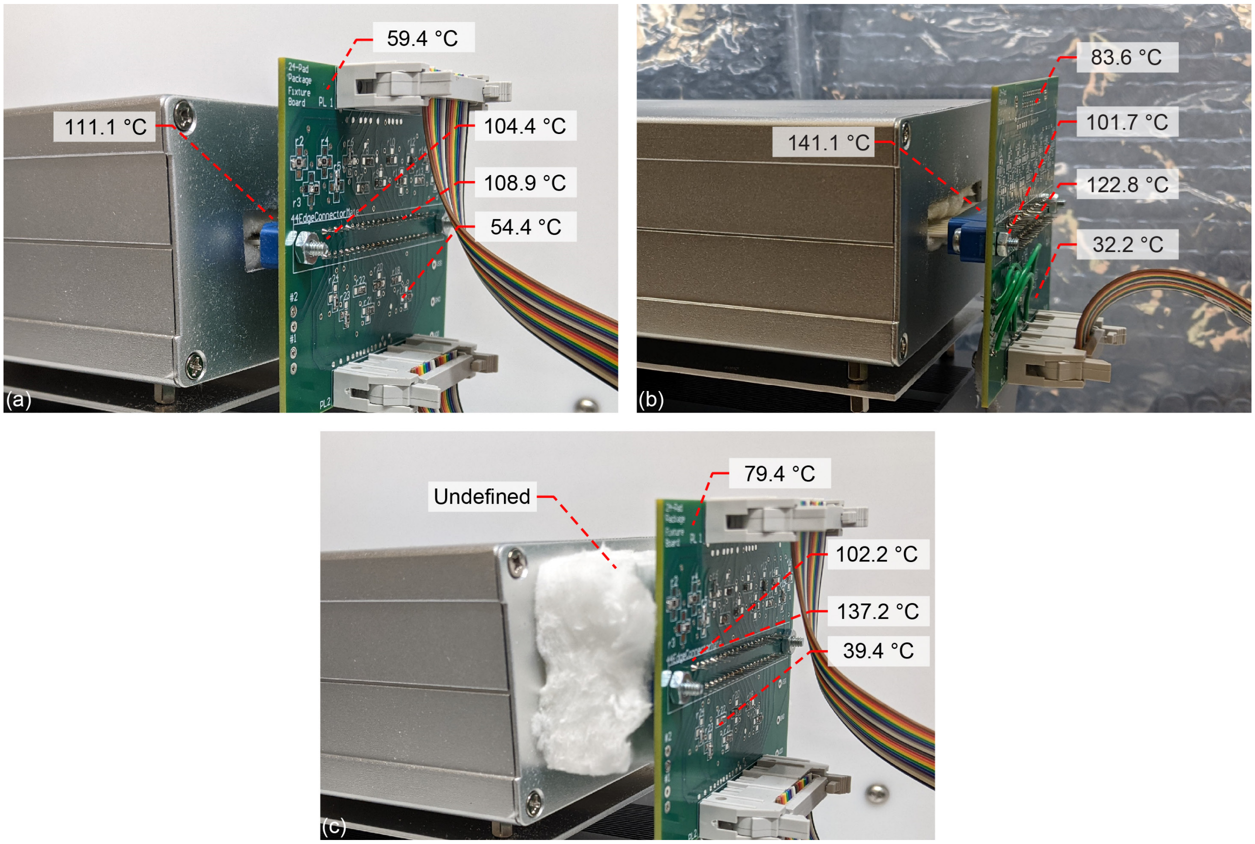


Figure 7.—Mark I ceramic board and fixture board temperatures. (a) Oven 1 with two inside layers of insulation at oven opening. (b) Oven 3 with one inside layer of insulation at oven opening. (c) Oven 5 with one inside layer and one outside layer of insulation at oven opening.

As anticipated, the black control electronics box located beneath the oven remained cool no matter which insulation configuration was used. Temperatures on both the middle of a side and a back panel of the electronics box were measured and experienced a maximum temperature of 31.7 °C with variation of less than 3 °C.

3.0 Test System Circuit Boards

The change from gold wires that connected to the IC pins inside the oven to ceramic substrate boards connected to fixture boards has proven to be a cost-efficient solution. The ceramic substrate boards, made of Al_2O_3, are attached to the SiC IC package (Ref. 10). The chip end of these boards is designed to slide into the oven's hot zone while the cool end connects to a room-temperature fixture board outside of the oven.

3.1 Substrate Boards

Testing as reported in (Ref. 5) revealed that the ceramic substrate boards have specific nuances that must be accounted for during oven tests. For example, it was found that with thinner substrate boards at high temperatures, electrical signals can leak or create crosstalk between nearby traces. The leakages happen as a result of impurities in or on the surface of the ceramic materials; however, those same impurities can be imperative for conductive trace construction or package bonding. To gain further insight into these relevant interrelated aspects of oven testing, board leakage diagnostic tests were undertaken.

3.1.1 Diagnostic Leakage Testing

Six diagnostic test structures in addition to the IC package were designed into three substrate boards of different thicknesses (25, 40, and 60 mil). Test results from the six diagnostic test structures on each board were compared. Three of the test structures were closed-circuit (CC) loops of conductive traces and three test structures were open circuits (OCs) of unconnected conductive traces. The resistances of these test structures were measured as a function of temperature and time using the direct current (DC) source-measure instruments in the PXI system. Specifically, the test structures listed in Table I were located as shown in Figure 8.

TABLE I.—DIAGNOSTIC LEAKAGE TEST STRUCTURES

T1(OC) Insulation of board outside of hot zone (open circuit (OC)).	Contains side-by-side traces of a constant minimum width of 0.686 mm and a constant minimum spacing of 2 mm. These traces run parallel to each other from the edge connector and end before the hot zone entrance.
T2(CC) Conductivity of traces outside of hot zone (closed circuit (CC)).	Contains side-by-side traces of a constant minimum width of 0.686 mm and a constant minimum spacing of 2 mm. These traces run parallel to each other from the edge connector and are shorted together just outside the hot zone entrance.
T3(OC) Insulation of board including hot zone (OC).	Contains side-by-side traces of a constant minimum width of 0.686 mm and a constant minimum spacing of 2 mm. These traces run parallel to each other, extending all the way through the hot zone.
T4(CC) Conductivity of traces including hot zone (CC).	Contains side-by-side traces of a constant minimum width of 0.686 mm and a constant minimum spacing of 2 mm. These traces run parallel next to each from the edge connector and are shorted together in the middle of the hot zone.
T5(OC) Insulation through board thickness (OC).	This test structure is similar to the T1 and T3 but ends in the middle of the hot zone and the traces are placed on opposite sides (top and bottom) of the substrate board rather than next to each other on the same side.
T7(CC) Through-via in hot-zone conductivity (CC).	Contains a pattern of series-connected chain of two through-vias in the hot zone.

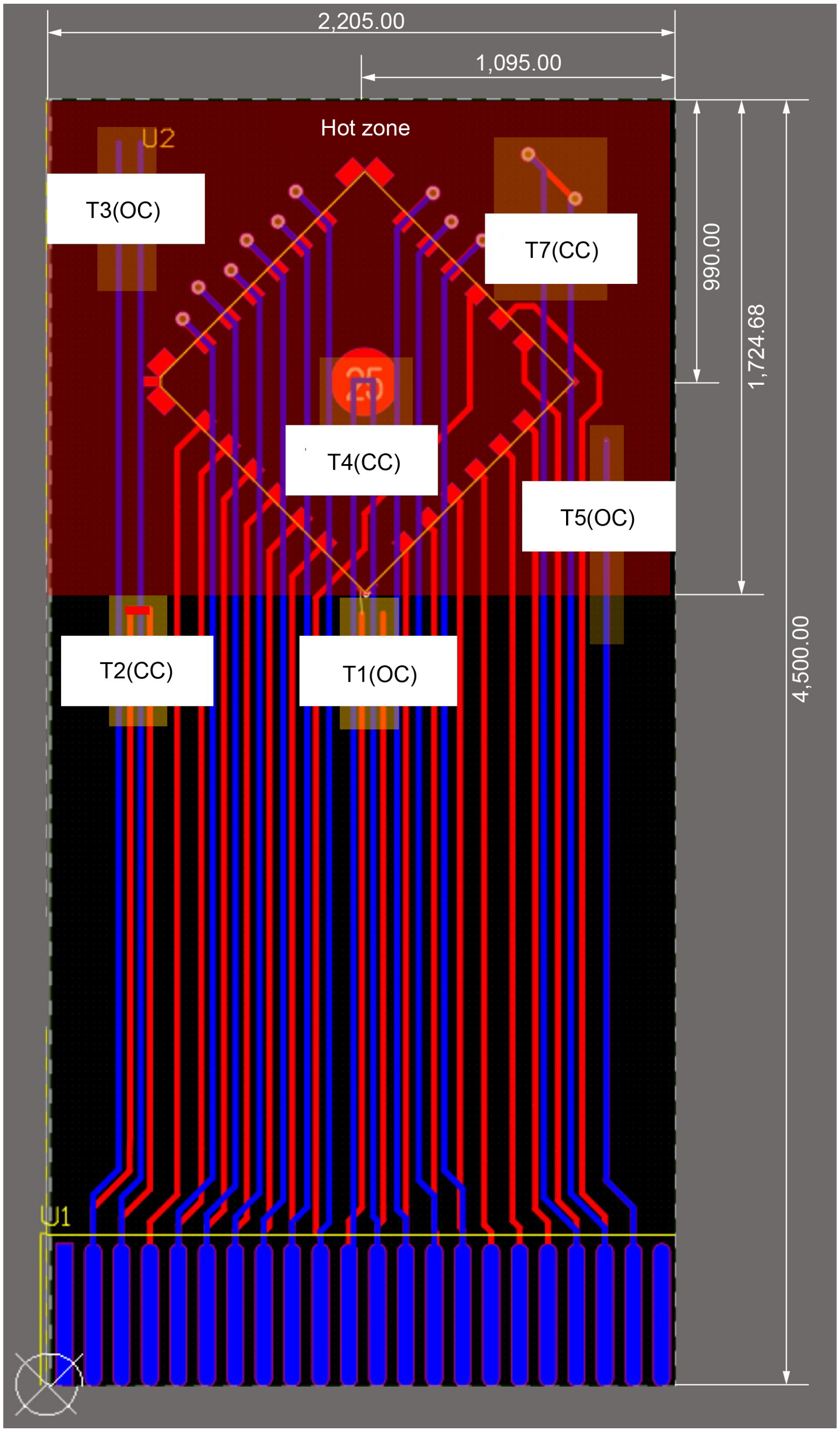


Figure 8.—Locations of diagnostic test structures on substrate board. OC is open-circuit insulation test; CC is closed-circuit conductance test.

Figure 9 shows the 500 °C steady-state results of these diagnostic ceramic substrate board tests. Specifically, Figure 9(a) shows defined groupings of the board thicknesses for the open-circuit tests, regardless of their diagnostic test location within the Mark I oven. In addition, the 25-mil-thick ceramic substrate boards provide less insulation by a factor of 10 than the 40- and 60-mil-thick ceramic substrate boards. The closed-circuit results in Figure 9(b) show 209 Ω of resistance or less and that the 40-mil-thick ceramic substrate board provides the least resistance for each diagnostic test grouping, but the overall spread is less than 1 percent.

The oven testing results summarized in Figure 9 prove that the main difference between the ceramic substrate board thicknesses is primarily in the board leakages and not in the additive conductive trace resistance. Therefore, deciding which ceramic substrate board thickness will work for Generation 12 IC testing depends on the acceptable leakage current threshold of the IC in testing. The addition of >200 Ω of substrate board trace series resistance must also be accounted for in testing the ICs. Previous IC versions measured the on-chip bond pad resistances of roughly 50 to 100 Ω at 500 °C.

Going forward, the 40-mil boards will be used for SiC IC testing. The leakage was 45 percent higher than the 60-mil board but remains acceptable for the ICs being tested for Generation 12. Importantly, the 40-mil-thick board offers the easiest insertion into the room-temperature fixture board edge connector.

Figure 10 details the measured data of the ramp-up to 500 °C (Figure 10(a)) and ramp-down to room temperature (Figure 10(b)). It is interesting to note how the temperature affects the current. For example, in Figure 10(a), note how when the temperature rises to 500 °C, the current readings for each board thickness and diagnostic trace test diverge from each other based on their ceramic board thicknesses. This has been speculatively attributed to the hot air allowing impurities within the ceramic board and traces on the ceramic board to connect with the electrical signals of nearby traces. After a prolonged time at 500 °C, the ceramic boards burn off some impurities, which level out the current at lower currents. This possibly explains why different 25 °C current values are measured before and after heating the boards to 500 °C.

3.2 Fixture Boards

The fixture board designs have also evolved for the Mark I ovens. The testing rig described in Reference 5 was the first time that fixture boards were incorporated, but they required unique customized board designs for each IC package type or specific IC chip. The testing rig now uses a universal fixture board design that enables connection to all Generation 12 ASICs via the configuration of jumpers on the board. The removable shorting connectors make it quick and easy to change the fixture board because no soldering is required.

Figure 11 shows the back-side view of the roughly 152.4- by 119.38-mm (6- by 4.7-in) universal fixture board to be employed for Generation 12 oven testing. The middle has the pins from the front-side edge connector where the ceramic substrate board electrically connects just outside the oven to the fixture board. This fixture board employs two-position shunt connectors for connecting each trace to its proper power or signal pin, depending on the specific IC trace requirements.

Two stages are required to configure each fixture board. First, each trace of the edge connector going to the ceramic substrate board is directed to a specific power pin or a signal going to the PXI measurement system (for signal routing via reed relays and measuring or sourcing). Three types of power options are available for each edge connector trace, namely VDD, VSS, and GND. To make certain VDD, VSS, and GND are correct on the corresponding pins, test points are provided on the upper-left portion of the board to facilitate checking supply voltages. The voltages are provided to the fixture board by the PXI system via a DC power supply module card (PXIe-4112) and the power switching relay module card (PXIe-2737), on the last four pins of each PXI ribbon cable connector. Second, each signal pin is connected to a specific pin of these connectors. Each PXI ribbon cable connector can provide 16 lines to the PXI measurement system, which allows for 32 total potential signals to or from a chip. However, the substrate board can bring up to 44 potential connections (power or signal) to the fixture board. Each Generation 12 SiC chip type can be configured on this fixture board without the need to cut traces, jump externally by other wires, or miss an IC trace.

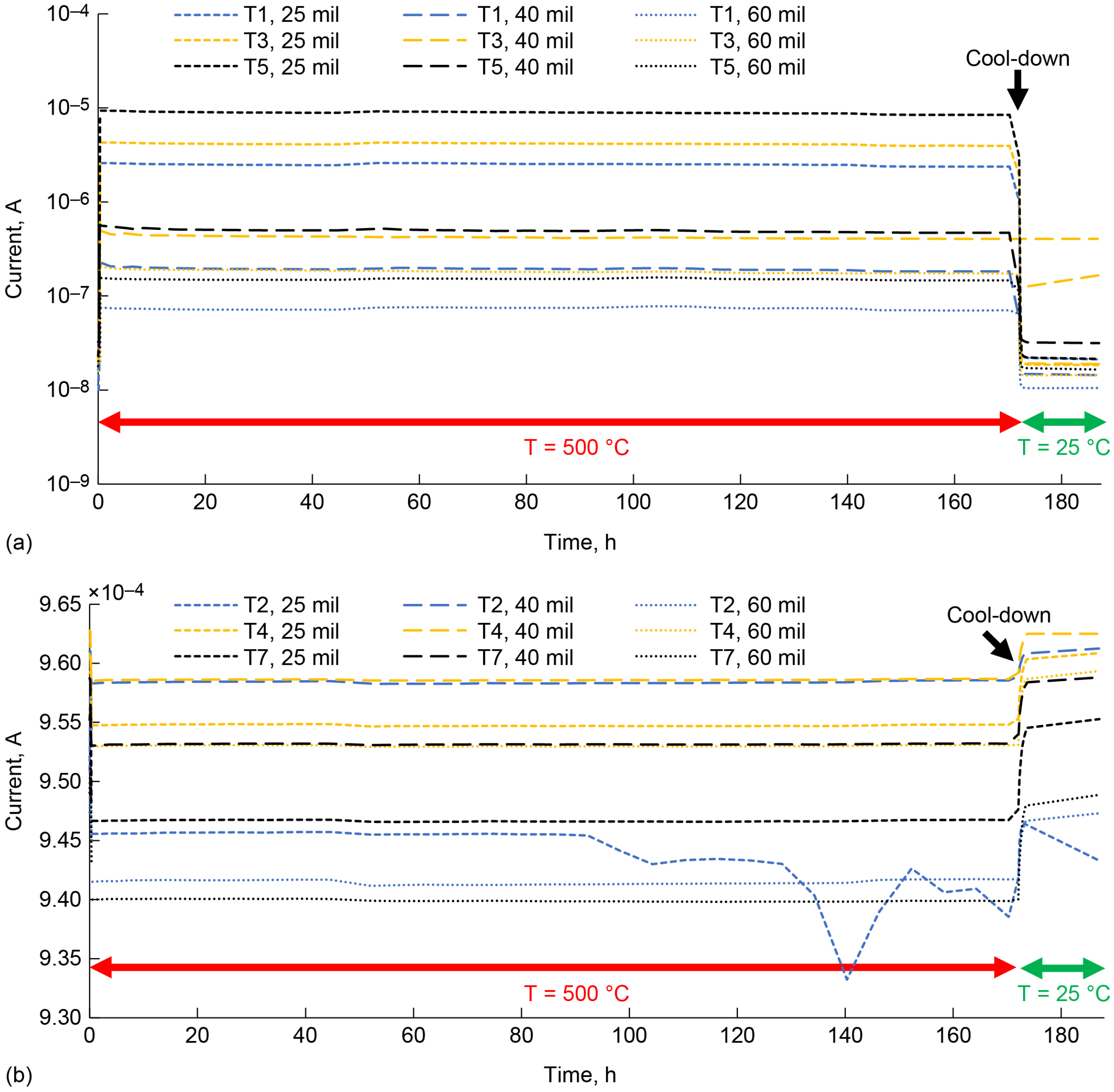


Figure 9.—Comparison of different ceramic substrate board thicknesses with onboard diagnostic tests split by open- and closed-circuit results. Thinnest ceramic board (25 mil thick) had least effective high-temperature insulation. (a) Open-circuit current measured at 50 V as function of ceramic board thickness and test location (T1, T3, or T5 listed in Table I) and time. Oven was heated from 25 to 500 °C starting at time = 0 h. (b) Closed-circuit trace current measured at 0.2 V as function of ceramic board thickness and test location (T2, T4, or T6 listed in Table I) and time. Oven was cooled from 500 to 25 °C at time = 172 h.

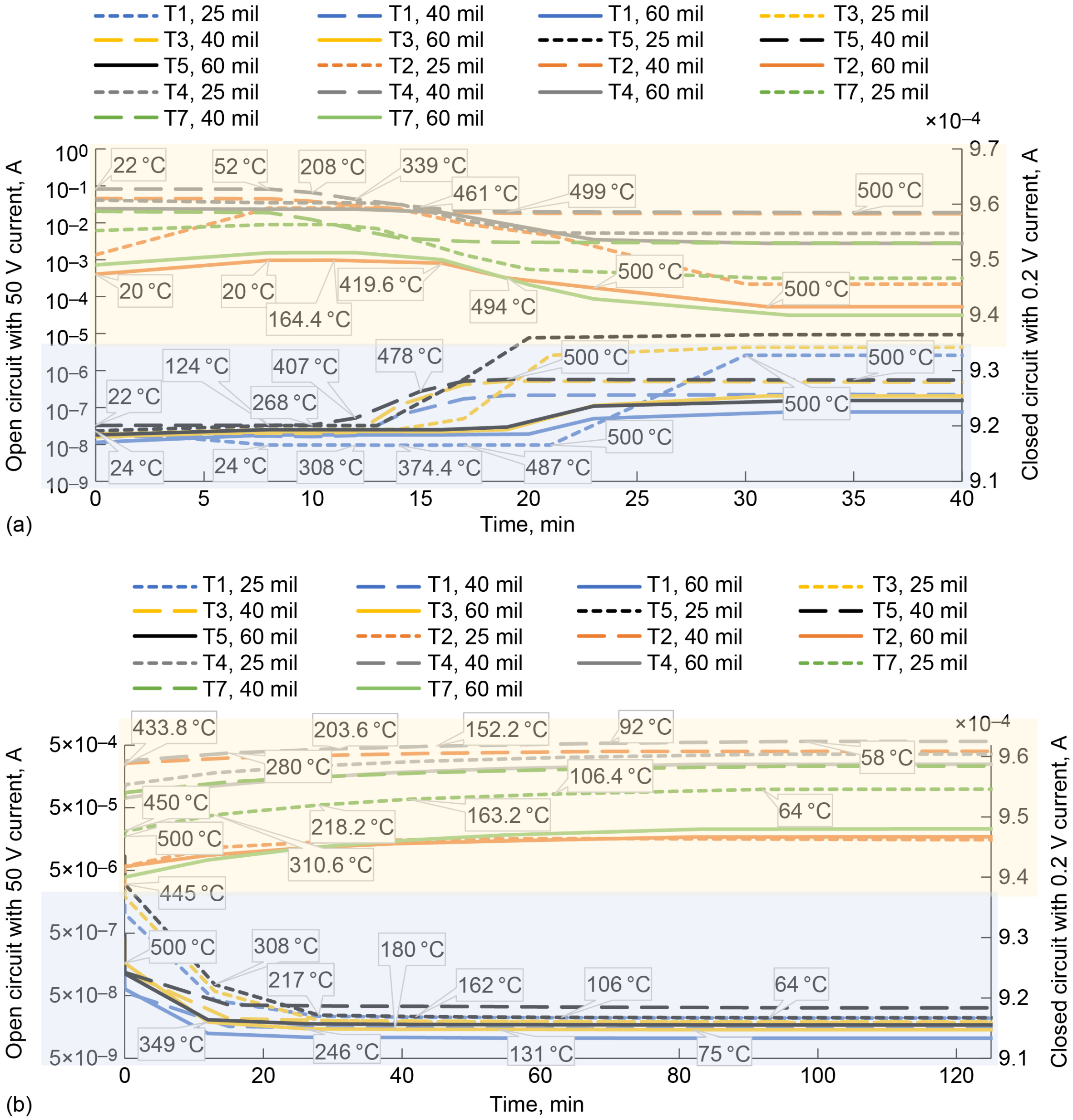


Figure 10.—Thermal ramp-up and cool-down comparing measured data for different ceramic substrate board thicknesses. (a) Diagnostic circuit results compared ramp-up to 500 °C. (b) Diagnostic circuit results compared ramp-down from 500 °C.

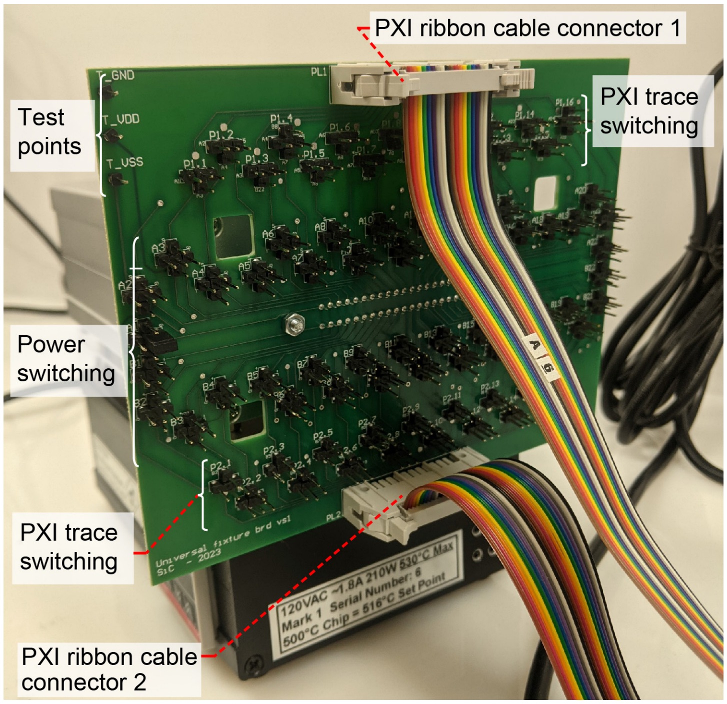


Figure 11.—Generation 12 universal fixture board with installed jumpers.

4.0 Switching and Measurement System

Each fixture board provides 32 measuring and sourcing signal connections for the IC(s) under test that connect to the two breakout boards via two ribbon cables to the fixture boards' two PXI ribbon cable connectors. The breakout boards electrically route signals and power to reed relay matrix cards (PXI-2530) in the PXI chassis. One of the PXI module relay matrix cards is designated for power (i.e., GND, VDD, and VSS) and resides in Slot 18, as depicted in Figure 12, which illustrates the PXI system chassis configuration. This relay matrix card can route power to multiple ICs and ovens simultaneously via 8 of the 32 total PXI ribbon cable connections per oven. The 32 chip-function signals are routed through four PXI-2530 MUX module cards installed in Slots 2 to 5 of the PXI chassis. The MUX cards are organized by oven and PXI ribbon cable trace based upon a one-wire octal 16×1 MUX configuration. Once relays in the MUX cards are closed, the test signals are further routed through a pair of PXI-2532 switching matrix module cards, with each card configured as dual-bank 8×32 matrices. The columns connect to various source and measuring devices, including source-measure units (SMUs), a power supply, an oscilloscope, and analog inputs (AIs) and outputs (AOs). Figure 12 shows only one of these matrices symbolically. The PXI device controls the matrix, MUX, and measurement instrument cards via a software application created in the LabVIEW® graphical programming environment to enable automating the testing rig's operation. LabVIEW® scripts configure the connections to test the desired ICs and save the measurement result data files as often as the researcher desires. The connections are not hard wired directly to the source and measuring devices, so researchers are able to connect to the computer remotely with the PXI hard-wired connection to configure and run the tests from anywhere.

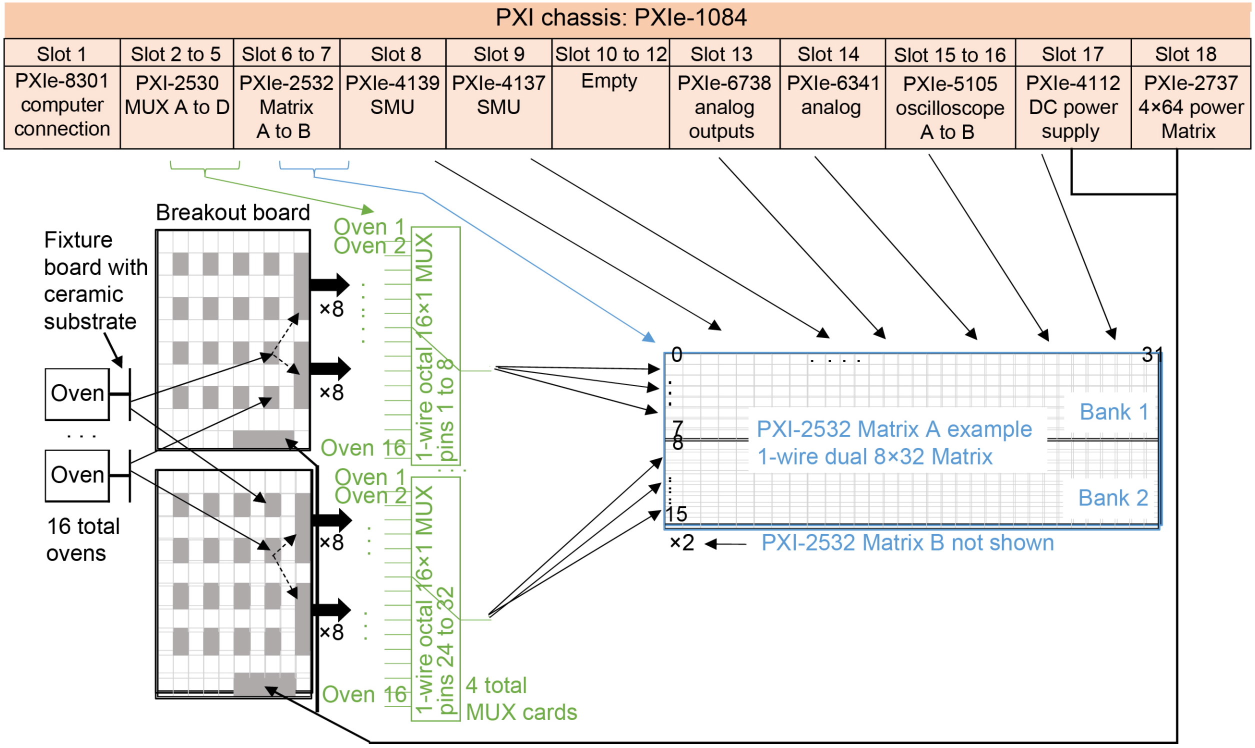
4.1 System Noise Test

Even though the measurement system was not optimized for low-noise measurements, ascertaining the level of noise the chip measurement signals will experience is relevant, nevertheless. Therefore, noise-measurement tests were conducted with the PXI oscilloscope module card and its oscilloscope probe on the 1× setting. These tests were conducted on each segment of the system (i.e., oscilloscope to matrix module to another piece of the system, such as an analog source pin, a MUX connection, etc.) going to Mark I Oven 0 (Figure 13), which contained a Generation 12 60-mil-thick, 24-pad package ceramic substrate board. Also, ceramic substrate board diagnostic trace TC(OC) shown in Figure 8 was specifically tested because it is an isolated, antenna-like trace that goes through the hot zone. These noise-test measurements were performed with the SMU module card providing a 50 V DC bias. Figure 13 presents a series of fast Fourier transform (FFT) oscilloscope results shown with increasing noise, as well as the measurement system to the oven. The FFT shows within what frequency how much system noise there is. In the future, shielding the cables could reduce the level of noise the device under test (DUT) experiences.

Two FFT measurements were taken at the oscilloscope module card with all PXI system cards installed and powered. The first measurement was simply the result of the 1× probe exposed to air; the second test was performed with a wire connecting the probe to the matrix module card at the point connects to all other source and measurement devices in the PXI chassis. The probe-only test shows the noise of the oscilloscope only. The second test shows the noise levels when the oscilloscope is connected to the relay matrix for measurements.

After collecting noise results from the probe connected and unconnected with the rest of the system, tests were conducted at other system components, including the following (Figure 13):

- System noise at Matrix B, MUX D, breakout board, SMU, and to substrate board
- PXI noise for AO terminal block to Matrix B, probe, and AI terminal block
- Noise to oven directly when the oven is turned on
- Noise to oven directly when the oven is turned off



PXI chassis: PXIe-1084										
Slot 1	Slot 2 to 5	Slot 6 to 7	Slot 8	Slot 9	Slot 10 to 12	Slot 13	Slot 14	Slot 15 to 16	Slot 17	Slot 18
PXIe-8301 computer connection	PXI-2530 MUX A to D	PXIe-2532 Matrix A to B	PXIe-4139 SMU	PXIe-4137 SMU	Empty	PXIe-6738 analog outputs	PXIe-6341 analog	PXIe-5105 oscilloscope A to B	PXIe-4112 DC power supply	PXIe-2737 4×64 power Matrix

Figure 12.—Detailed PXI chassis connections.

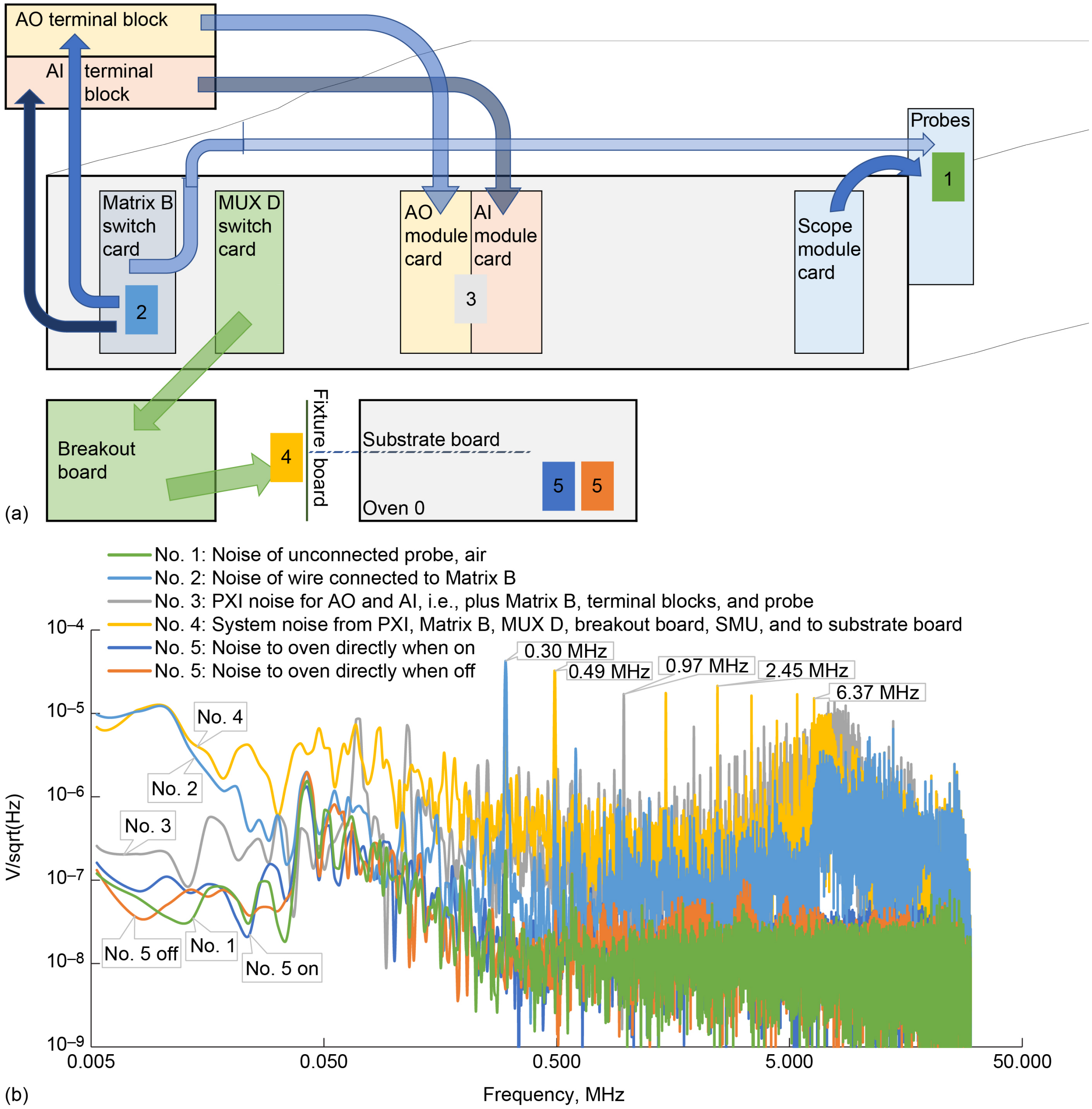


Figure 13.—Noise floor overview of noise recorded at various areas of measurement system.

The total system with the oven turned on experiences a peak noise frequency between 0.5 and 10 MHz. Figure 14 shows a closeup of these crucial frequencies. Here, the system has a mean of 1.61×10^{-6} magnitude.

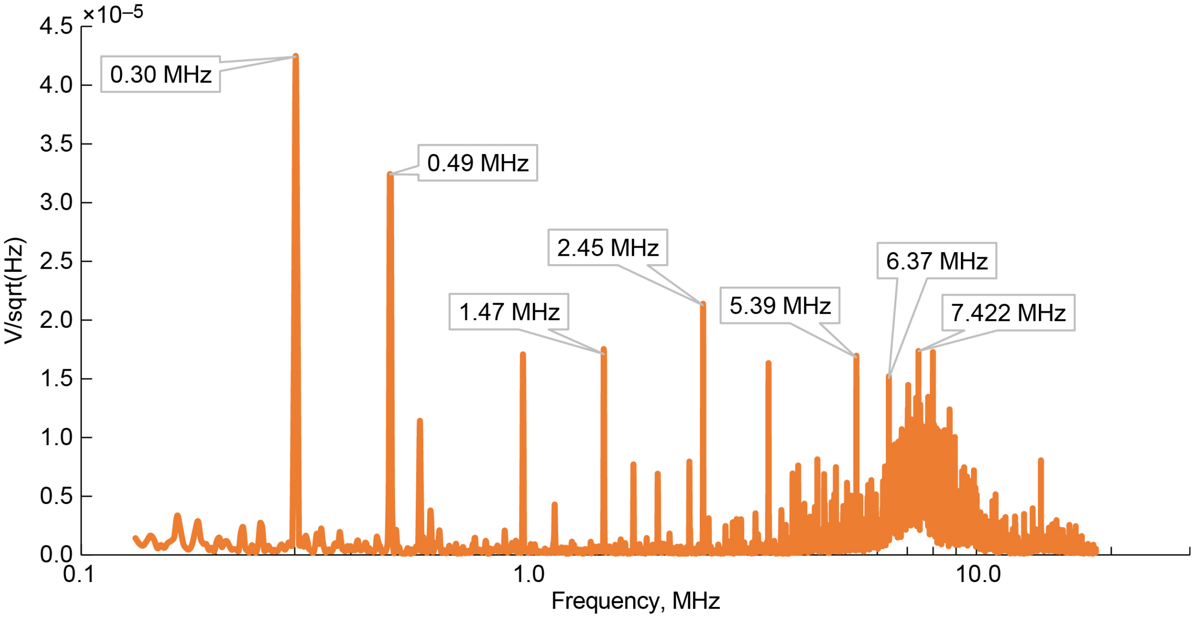


Figure 14.—Total system noise floor closeup.

5.0 Conclusion

The Generation 12 testing rig described in this report creates a robust, reliable, and reconfigurable environment for parallel testing of the electrical performance and durability of a variety of silicon carbide (SiC) integrated circuits (ICs). The testing rig presently contains 8 ovens but can be expanded to 16 ovens. Each oven can hold one or two ICs depending on the ceramic substrate board and package configuration used, but no fixture board can presently handle more than 32 test signals simultaneously with the current setup. The current power connections with the power supply matrix can accommodate up to 64 test signals.

Three minor improvements are being considered for the test ovens. First, the ovens can be enhanced with a more capable proportional-integral-derivative (PID) controller that allows for more complicated temperature versus time setpoint profiles. This would enable the ovens to better mimic more realistic aerospace mission thermal profiles than the single/simple setpoints of the Mark I oven controller. Second, active cooling would enable testing under rapid cool-down and accelerate thermal cycling testing. Finally, achieving temperatures higher than 600 °C will demand the use of nickel, bronze, copper, or a similar metal to replace the Mark I plate and heater block, which are made of an 80/20 aluminum alloy.

The results of system qualification testing have already been described. The internal oven temperature measurements prove that the IC is within 5 °C of the 500 °C oven setpoint while external thermal measurements prove that the substrate board protruding outside the oven opening can be safely mated to a signal-routing fixture board with a conventional edge connector, saving money. In addition, the external thermal measurements show that the temperature of the oven's outer case is only around one-fifth that of the inside-the-oven temperature. The ceramic substrate boards proved to be a cost-efficient solution for facilitating electrical signal connections to the device under test (DUT) inside the oven's hot zone. Ceramic substrate board ≥40 mil thick demonstrated acceptable leakages at 500 °C. The fixture boards near the opening of each oven provide connection to the ceramic substrate board with enough customization using simple jumpers. Finally, the switching and measurement system (i.e., the breakout boards and National Instruments (NI) Peripheral Component Interconnect eXtensions for Instrumentation

(PXI) chassis) provides necessary source-measurement-power connections to characterize the electrical performance of a variety of SiC ICs inside the ovens.

Additional work to enhance the testing rig further is planned, but no major modifications should be necessary to proceed with next-generation IC testing. Going forward, the testing rig will contain small-footprint, high-temperature ovens, substrate boards, fixture boards, breakout boards, and PXI devices. Currently, work has begun toward building Mark II ovens equipped with more capable PID controllers and active cooling.

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