NASA High Performance Spaceflight Computing (HPSC) Overview

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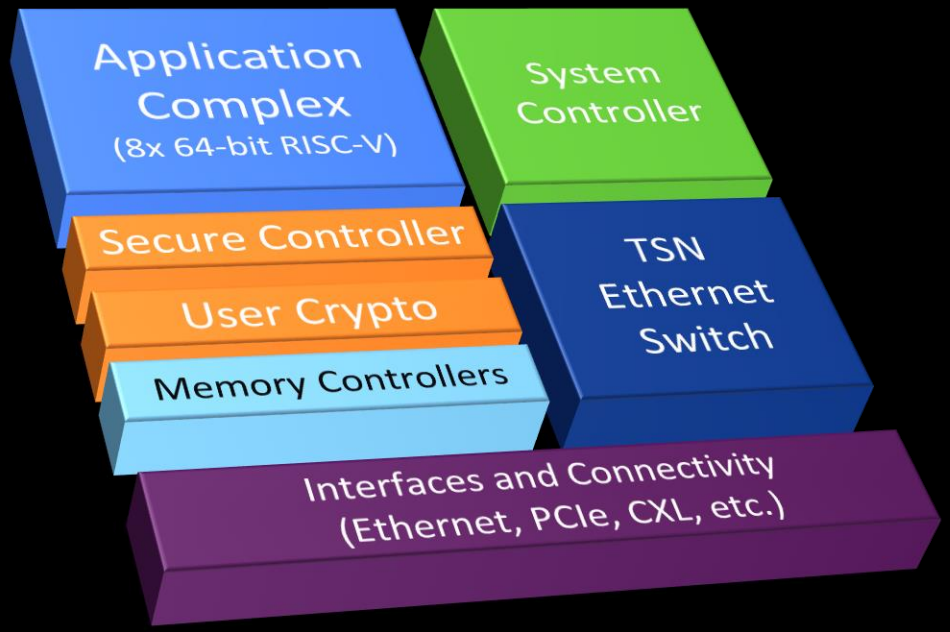
What is HPSC?



- **100X the computational capacity of current space flight processors**
- **Multicore architecture provides unprecedented flexibility between computational performance, power management, & fault tolerance**

- **NASA Program:** (Partnership jointly funded by STMD and Microchip): HPSC advances the capabilities of space-based computing for upcoming missions. Infusion targets across human, robotic, and science missions

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- **Requirements:** Jointly developed by NASA, JPL, and Microchip

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- **Fault-tolerant 10-core Heterogenous RISC-V Architecture:** Extremely high performance per watt. Radiation hard by design

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- **Initial Delivery**: SoC, Evaluation Board, Software Stacks, Models, Education & Training, Application Support

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- **Industry Eco-System**: Industry-funded, HPSC-compatible roadmap benefits NASA, JPL, mil-aerospace, & terrestrial applications for decades to come

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- **Capability Advances:** Cost, Schedule, Risk reduction: Mission and science autonomy, intelligent vehicles, flagship science, crew assist. Software-based flexibility

NASA Science: HPSC Use Cases

Rovers & Helis

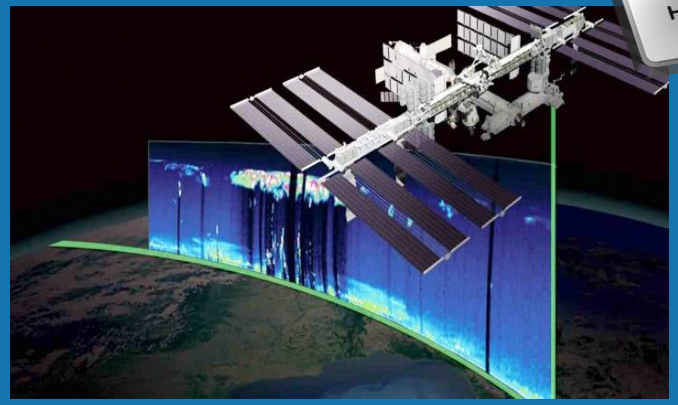
- Vision Processing
- Motion/Motor Control
- Nav Planning
- Science Instruments
- Communication
- Power Management
- Thermal Management
- Fault Detection/recovery

Landers

- Hard real-time compute
- High-rate sensors w/zero data loss
- High level of fault protection/fail over

High Bandwidth Instruments

- Real-time sensor data
- Non-mission critical
- High bandwidth sensors
- Large calibration sets in non-vol memory



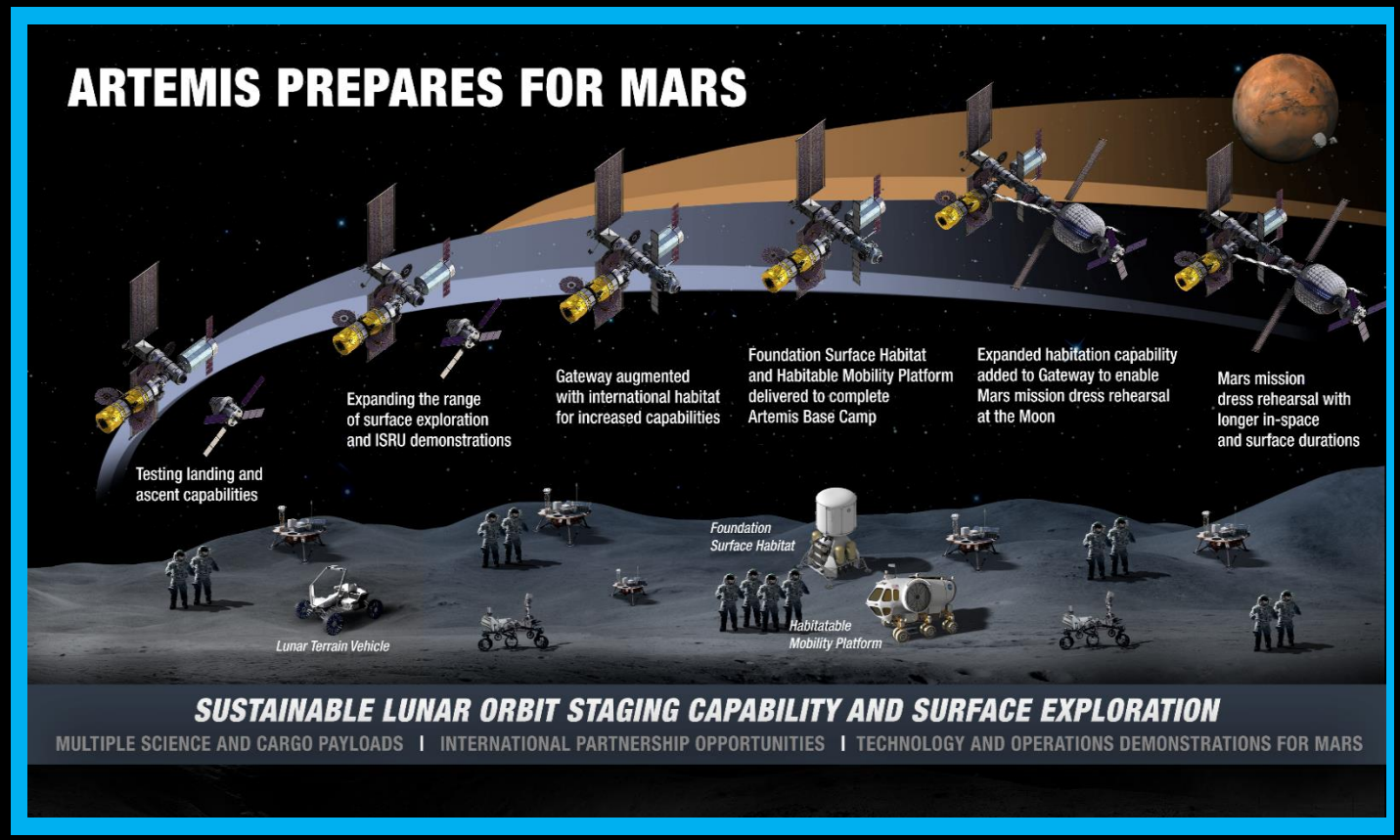
Smallsats

- Hard & soft real-time
- Guidance & Control
- Autonomy & crosslink communication
- Sensor data processing
- Autonomous science

NASA Crew Exploration: HPSC Use Cases

- Robotics working independently and collaboratively with crew
- Robotics enabling lunar surface infrastructure
- Autonomous landing systems
- Increased autonomy extends missions beyond LEO
- Support for Earth independent operations

Gateway - Full Configuration in Orbit



HPSC Feature Highlights

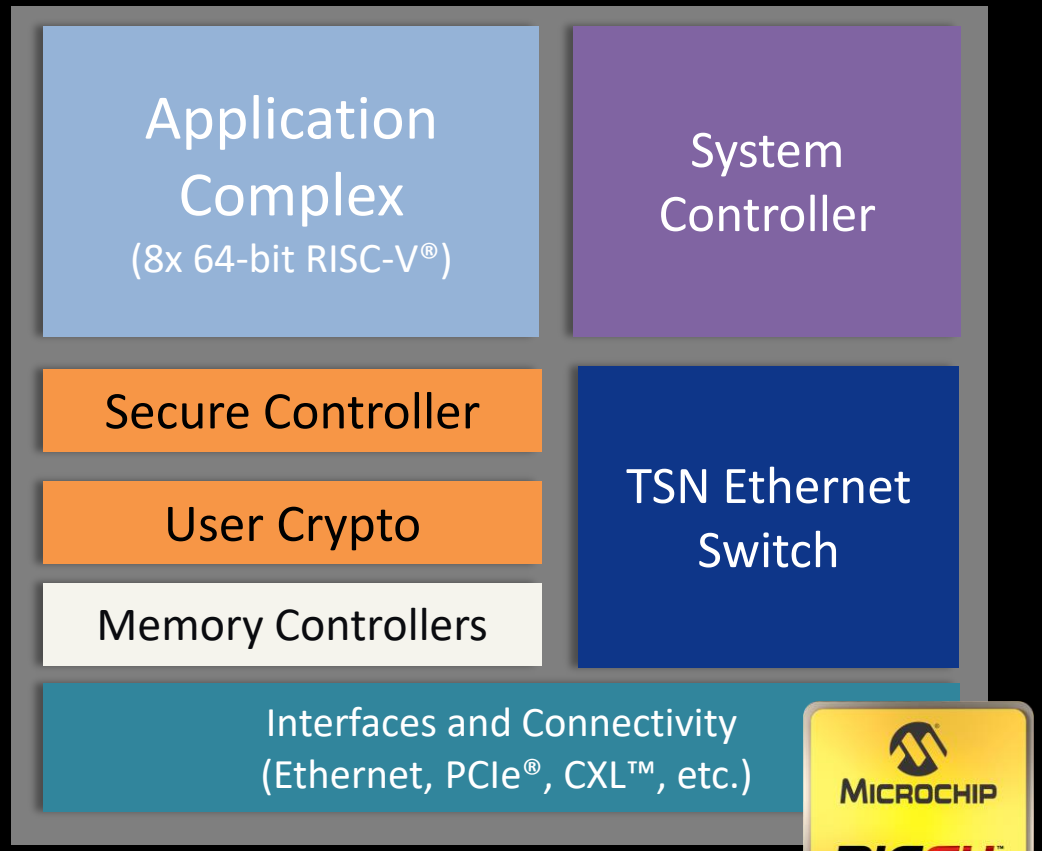
Radiation-Hardened and Radiation-Tolerant Versions Enable a Spectrum of Mission Profiles

Compute

Groundbreaking **64-bit RISC-V © Vector** processing with virtualization targeting Edge AI (SiFive X288/X280)

Security

Defense Grade Security Enclave supporting **Post-Quantum** Cryptographic algorithms



Fault Tolerance

Unprecedented **Fault-Tolerance** capabilities for Mission Critical Applications (DCLS, Split-Mode, WorldGuard)

Massive Connectivity

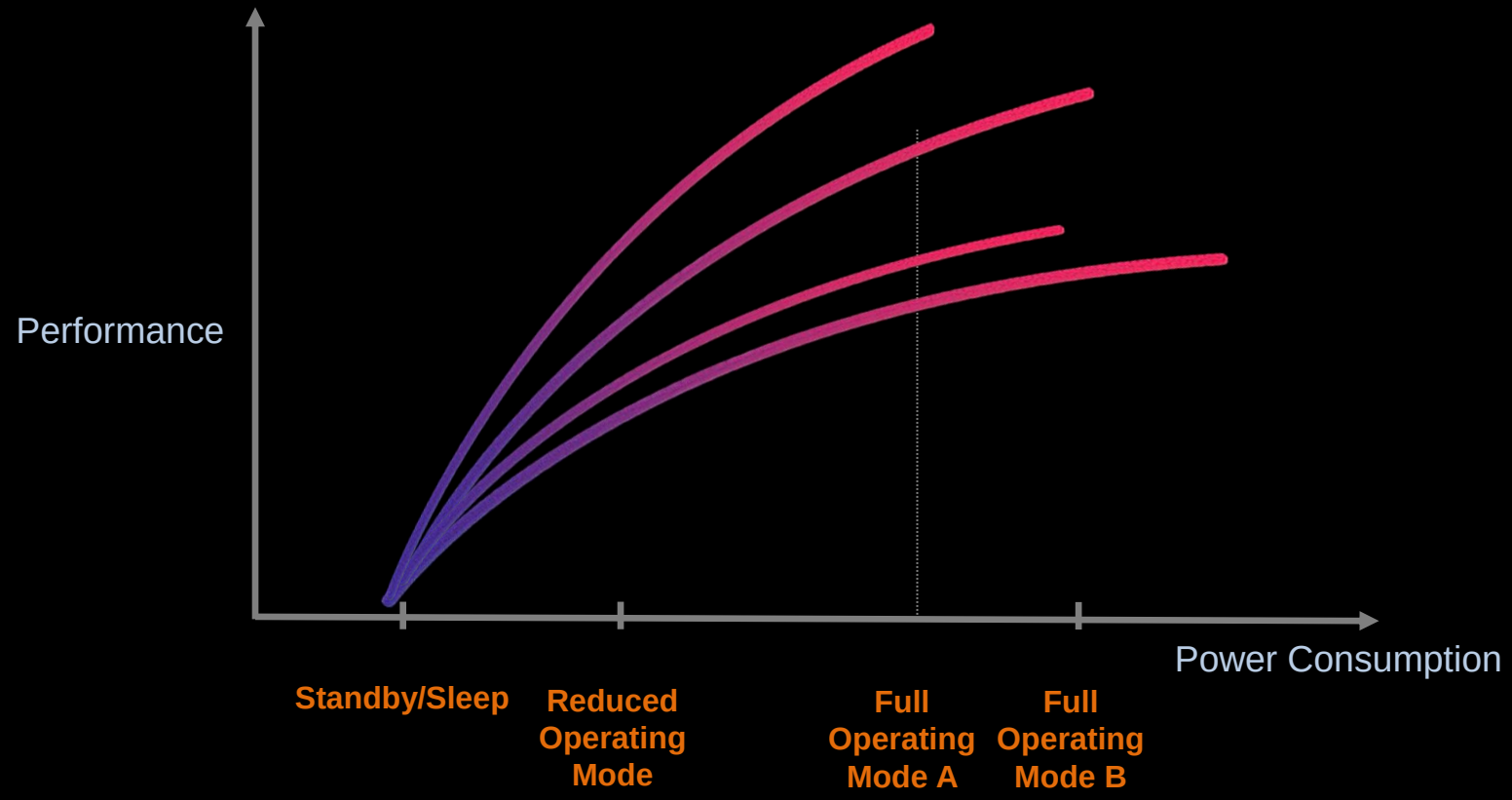
Integrated **240G TSN Ethernet** Switch, **10GbE**, **PCIe**/CXL and **RDMA** for Networking & Deterministic Connectivity, **SpaceWire** Router

HPSC Compute Performance Stack Up

	HPSC	RAD-750	RAD-510	GR740	RAD-5545
Operating Frequency	1 GHz (POR)	200 MHz	462 MHz	250 MHz	466 MHz
CPU Core Microarchitectural Date	Present day	*Circa mid 1990's*	*Circa 2010*	Circa 2010	Circa 2010
Number of processor cores	10 (eight SiFive x280 and two SiFive s21)	1 (PowerPC 750)	1 (RAD5500)	4 (LEON4)	4 (RAD5500)
SpaceBench (speed-up v. GR740)	1,343x (@1GHz)	*N/A (less than GR740)*	*N/A (less than GR740)*	1.0 (baseline)	1.6
DMIPs	28,130 (@1GHz)*	400 (@200MHz)	1,386 (@462MHz)	1,700 (@250MHz)	5,592 (@466MHz)
Vector Processing Performance	256 GFLOPs*	*No hardware vector engine*	*No integrated vector engine*	*No hardware vector engine*	*No hardware vector engine*
AI/ML – BFLOAT16 Matrix Multiplication	1,024 GFLOPs*	*No hardware AI/ML support*	*No hardware AI/ML support*	*No hardware AI/ML support*	*No hardware AI/ML support*
AI/ML – INT8 Matrix Multiplication	2 TOPs*	*No hardware AI/ML support*	*No hardware AI/ML support*	*No hardware AI/ML support*	*No hardware AI/ML support*

HPSC Scalability - Small to Large

Power, Performance, Fault Tolerance and other Functions: Scalable via Software Control

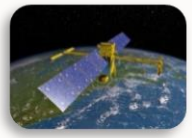


HPSC Performance & Power are Dynamically Tunable based on Mission Needs

Supporting Open Source & Commercial Software

Extensive Development Tools, Libraries and Operating Systems for PIC64-HPSC Series

Applications

Satellites 

Spacecraft 

Rovers/Landers 

Aviation 

Defense 

Industrial 

Middleware

System Libraries: OpenSBI, OpenAMP, OpenMP, OpenSSL (Cryptography and SSL/TLS Toolkit)

Performance Libraries: FFTW, POCL, OpBL

AI Frameworks: PyTorch, TensorFlow, TensorFlow Lite

Operating Systems

Linux
Operating System, BSP and Drivers

Real-Time Operating System(s): RTEMS, WNDRVR, SYSGO EMBEDDING INNOVATIONS, Green Hills SOFTWARE

Hypervisors: Xen Project, KVM

Design Resources

Simulation Models 

Velocity Switch S/W 

Drivers 

System Controller 

Configuration Tool 

Crypto Tool 

Tools

Compilers: LLVM COMPILER INFRASTRUCTURE, OpenXLA, IREE, GCC

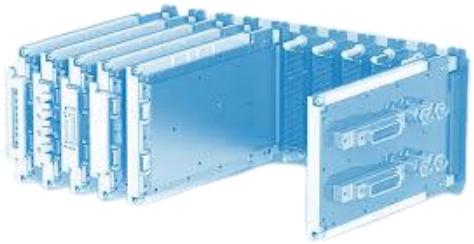
Development Tools: MPLAB EXT, LAUTERBACH DEVELOPMENT TOOLS, ENTRUST SECURING A WORLD IN MOTION

HPSC Ecosystem - Hardware

Interoperable, Industry Standard Hardware to Reduce Mission Risk, Lower Costs, and Improve Development Efficiency

Open/Interoperable

SPACEVPX™



DOD already successfully uses this procurement model terrestrially. Currently working to establish it for space.

Build vs. Buy

NASA

U.S. Department of Defense

esa

NASA can buy SpaceVPX SBCs and build custom boards when necessary.

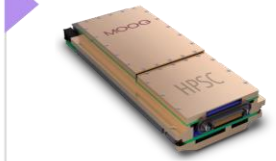
Single Board Computer and Module Partners

Partners

MOOG

ibeos

IDEAS Engineering & Technology



HPSC Partners developing flight-capable Single Board Computers in various form factors (SpaceVPX 3U/6U, VNX+).

"Buy what we can … build what we must"

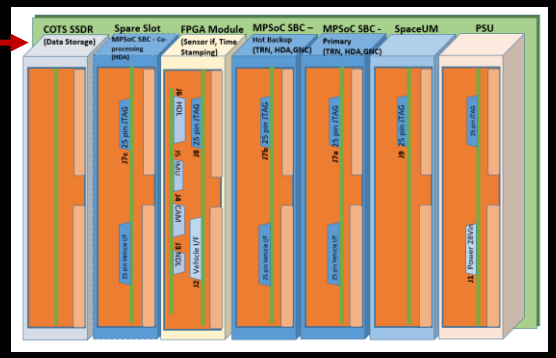
SpaceVPX Overview

SpaceVPX is an architecture standard that defines modules, backplanes, and chassis for spaceflight avionics boxes (the SpaceVPX standard is managed by VMEbus International Trade Association (VITA) as VITA-78)

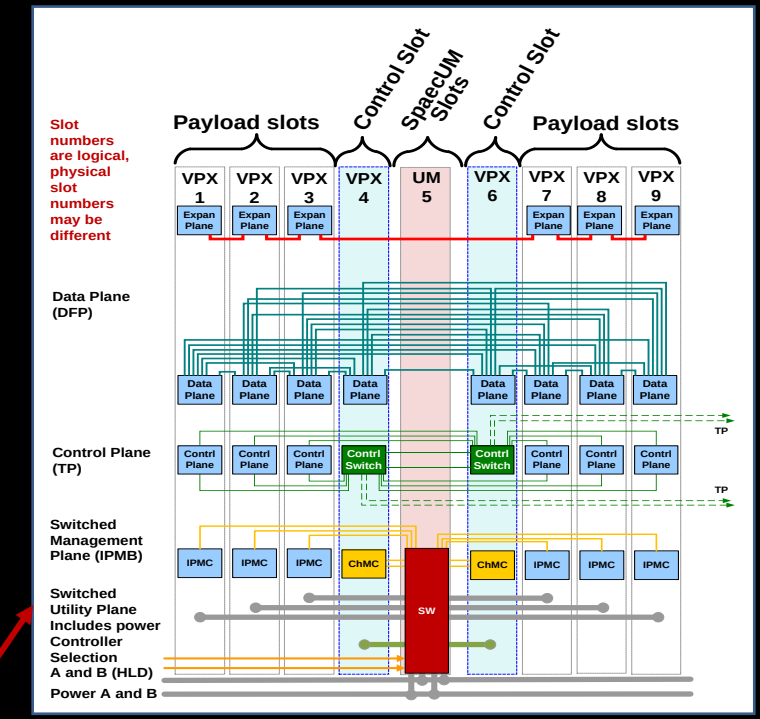
SpaceVPX adapts a Modular Open System Approach (MOSA), derived from VPX and OpenVPX (VITA-65), for space

SpaceVPX defines several general module types and how they can be interconnected, using the concept of "profiles"

- Slot Profile – A physical mapping of ports onto a slot's backplane connectors
- Module Profile - Extends a slot profile by mapping protocols to a module's ports and defines physical dimensions
- Backplane Profile - Defines number and types of modules supported and their interconnection topology



Profile Name	Data Plane 4 FP	Expansion Plane P2/J2	Control Plane 2 TP	User Defined
	DP01 to DP04		CPtp01 to CPtp02	P3/J3, P5/J5
MOD6-PAY-4F1Q2T-12.2.1-1-cc	sRIO 2.2 at 3.125 Gbaud per Section 5.2	sRIO 2.1 at 3.125 Gbaud per Section 5.2	SpaceWire per Section 5.2.1	User Defined DIFF pins



[VITA-78]

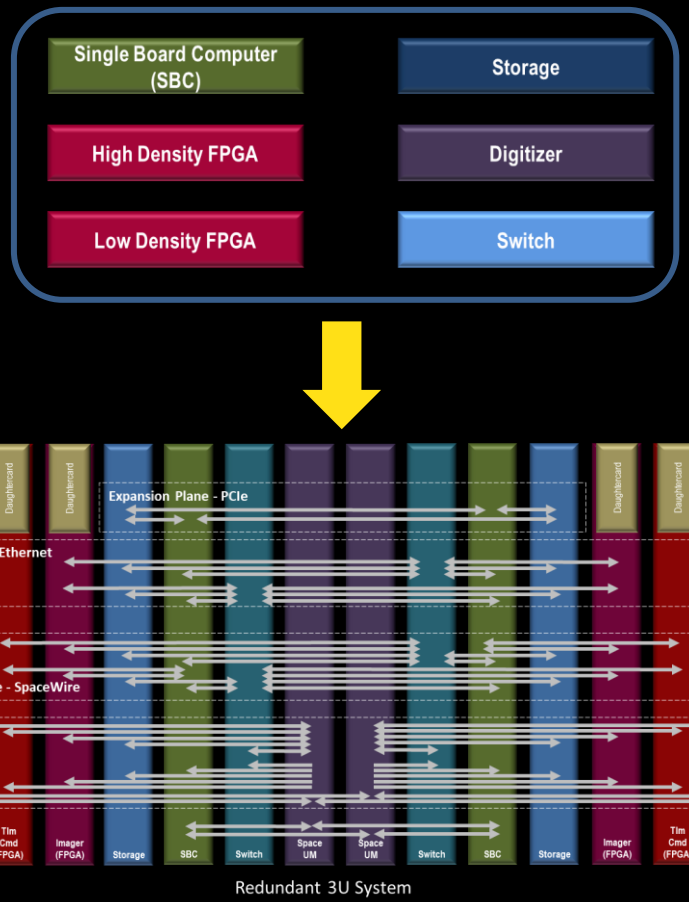
Problem statement – There is so much flexibility within SpaceVPX that it's possible to implement two different modules that are fully compliant with the standard yet cannot interoperate

Benefits of Interoperable SpaceVPX

- NASA is collaborating with industry and other agencies on the development of an interoperable variant of SpaceVPX (currently specified in the VITA-78 standard) within the Sensor Open System Architecture (SOSA™) standards organization

- Once completed, an interoperable SpaceVPX standard can guide SpaceVPX development within NASA and industry to ensure interoperable avionics for future NASA missions
  - SpaceVPX provides a scalable architecture with the high-bandwidth inter-module communication and inherent fault tolerance to meet the increased onboard computing demands of future missions
  - System integrators can configure systems consisting of SpaceVPX modules from multiple vendors
  - SpaceVPX module vendors can leverage broader markets for their products, which can reduce per unit cost
  - Interoperability provides a key step toward interchangeability that would be needed for common sparing for future crewed missions

- Interoperable SpaceVPX can form the backbone of the HPSC (High Performance Spaceflight Computing) avionics ecosystem



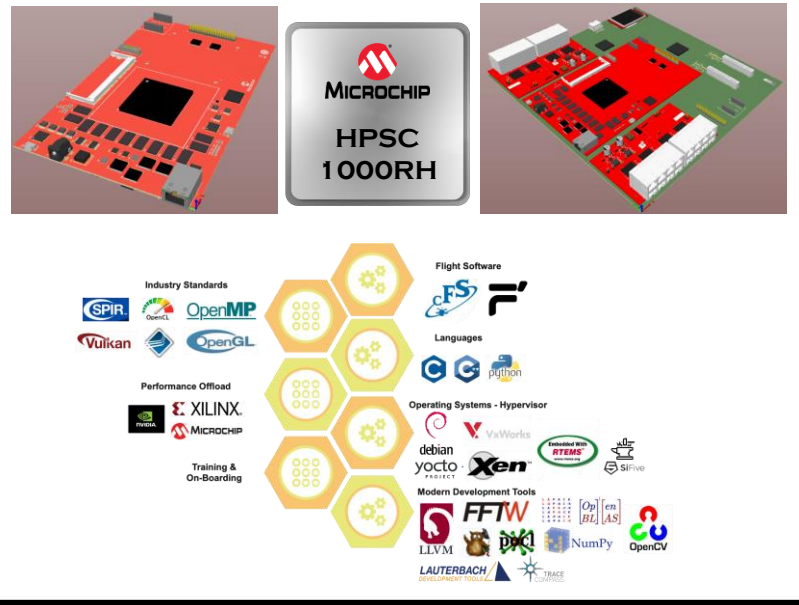
Redundant 3U System

HPSC Roadmap

HPSC Program

(Program of record – Fully Funded)
Completes CY2025

- Space qualified chips
- Evaluation/Development Boards (out of form factor)
- OS, drivers, libraries
- Microchip: Training, documentation, support
- Microchip: Goto Market

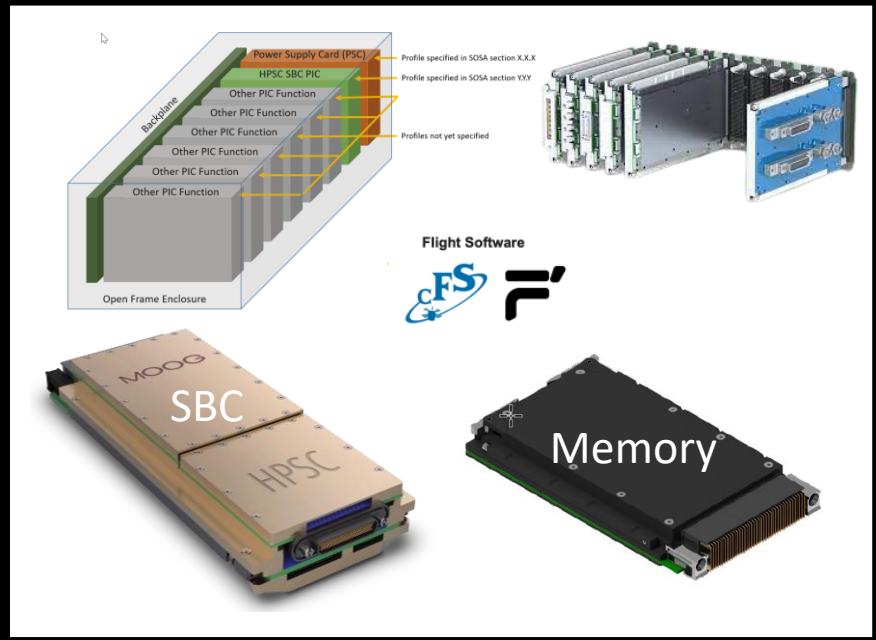


HPSC Test Kit

(In Process w/NASA – Needs Funding)

CY2025-2026

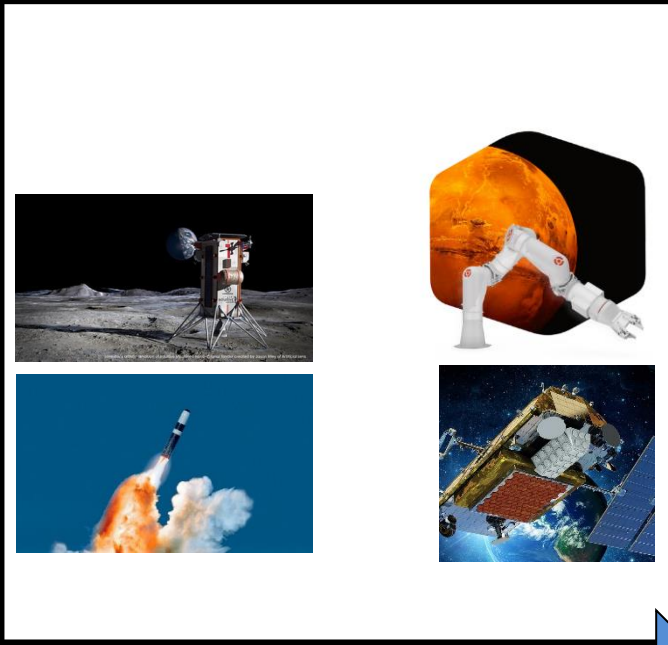
- SpaceVPX S3C form factor
- SBC, PSC, SSD, other PICS
- Flight Software Frameworks
- Board Support Package
- Components have Path to Flight Certification
- GSE
- First push signal to industry. In-form factor “real” systems



HPSC/SpaceVPX Mission Infusion, Tech Demo

POTENTIALS:

- Mass Spec
- Lunar Comm Relay
- SPLICE
- Aerocapture
- Orion upgrade
- Gateway
- Others



HPSC is On-Track to Deliver

- **HPSC Delivery is on track**
  - **Samples available early 2025**
- **Partners Engaging:** Investing in Eco-System. SBCs, Memory Modules, Software, Systems
- Significant "**HPSC Early Adopters**" are committing to HPSC
- NASA is investing $80M in HPSC
- Microchip is making strategic investments in HPSC

In Summary

- HPSC provides significant advancement in onboard flight computing for our future missions
- Beyond NASA, HPSC can also provide a compelling fault-tolerant computing solution for Mil-Aerospace, Government, and Commercial Industry
- HPSC is coming soon, with evaluation boards expected in early 2025
- Work with industry in underway to develop an interoperable avionics standard, and HPSC products have already been announced that will comply with this standard
- We look forward to working with stakeholders to develop an HPSC ecosystem and identify demonstration and infusion opportunities

Acronym List

AI	Artificial Intelligence	NSF	National Science Foundation
API	Application Programming Interface	NumPy	Numerical Python
CCSDS	The Consultative Committee for Space Data Systems	OGA	Other Government Agency
cFE/cFS	Core Flight Executive/Core Flight Software	Open BLAS	Open Basic Linear Algebra Subprograms
cPCI	Compact Peripheral Component Interconnect	OpenCL	Open Computing Language
COTS	Commercial Off the Shelf	OpenCV	Open-Source Computer Vision
C&DH	Command and Data Handling	OpenGL	Open Graphics Library
CXL	Compute Express Link	OpenMP	Open Multiprocessing
CY	Calendar Year	OS	Operating System
ECC	Error Correction Code	PCIe	Peripheral Component Interconnect Express
EDL	Entry Descent and Landing	POL	Point of Load
FET	Field Effect Transistor	QOS	Quality of Service
FPGA	Field Programmable Gate Array	RISC	Reduced Instruction Set Computer
GPU	Graphics Processing Unit	RTEMS	Real-Time Executive for Multiprocessor Systems
IEEE	Institute of Electrical and Electronics Engineers	RTOS	Real Time Operating System
HW	Hardware	SAE	Society of Automotive Engineers
ILPM	Industry Leading Parts Manufacturer	SBC	Single Board Computer
JPL	Jet Propulsion Laboratory	SEE	Single Event Effect
LEO	Low Earth Orbit	SOC	System-On-a-Chip
LLVM	Low Level Virtual Machine	SOSA	Sensor Open Systems Architecture
MEAL	Mission, mission Environment, Application, and Lifetime	STMD	Space Technology Mission Directorate
ML	Machine Learning	SW	Software
MOSA	Modular Open Systems Architecture	SWaP-C	Size Weight and Power, and Cost
MUSTANG	Modular Unified Space Technology Avionics for Next Generation missions	TBD	To Be Determined
NASA	National Aeronautics and Space Administration	TSN	Time-Sensitive Networking
NESC	NASA Engineering & Safety Center	VITA	VMEbus (Versa Module Eurocard Bus) International Trade Association
NRO	National Reconnaissance Office		