National Aeronautics and Space Administration

NASA Electronic Parts and Packaging (NEPP) Program
2024 EEE Parts Training Workshop

Discrete Semiconductor Manufacturing Process Basics

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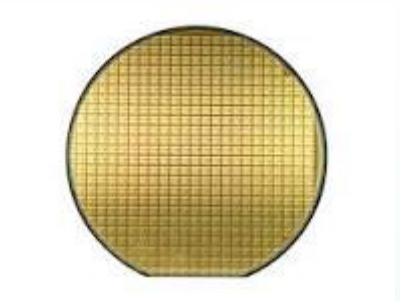
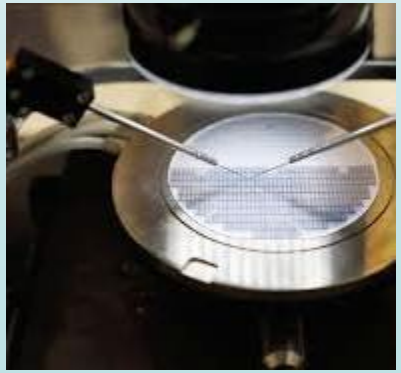
Wafer Fabrication Process



- Wafer starting material with epitaxial layer on 3, 4, 6, or 8-inch wafers depending on manufacturer.
- Diffusion furnaces – oxide layer growth
- Photolithography, and junction development in diodes, transistors, and MOSFETs
- Metal layers and backside grind
  - Top metal - evaporation or sputter process, sintering process
  - Bond pads
  - Backgrind process for wafer thinning
  - Back side metal – evaporation or sputter process
  - Metal sintering
- Wafer probe
- Wafer saw



Discrete Semiconductor Assembly Process

- Die, headers, packages, wire etc., and kitted for traceability.
- Visual inspection and equipment setup prior to assembly start.
- Die attach – eutectic or solder die attach may be manual, semiautomated, or automated.
  - SPC to monitor die attach process.
- Wire bond – manual, semiautomated, or automated process and varies by manufacturer.
  - SPC to monitor wire bond trends.
- Precap visual inspection prior to package seal for JANTXV and JANS (space) product.
- Package seal – in a controlled atmosphere - glass sleeves for glass diodes, welding for round TO packages, seam sealing for some TO packages such as TO-25X, vacuum sealing for surface mount such as UA and UB.

Discrete Semiconductor Assembly Process

- Screening
  - Environmental testing – temperature cycling, constant acceleration, and PIND.
  - Electrical testing – initial electrical test, surge, thermal impedance, high temperature reverse bias (HTRB), and burn-in.
  - Electricals after HTRB and burn-in with PDA.
  - Seal test – performed on all quality levels JANTX, JANTXV, and JANS.
  - Radiography for JANS space level only.
  - Visual inspection for JANS space level only.
  - Device marking process can be ink or laser marked and marking step varies.

Discrete Semiconductor Assembly Process

Qualification conformance inspection (QCI) testing

- Manufacturer initial device qualification and device requalification consists of Group A inspection electrical testing, Group B environmental and electrical testing, Group C is electrical and environmental testing, Group D radiation testing, and Group E electrical and environmental testing.
- Group A conformance inspection consists of external visual, DC electricals, electricals at minimum and maximum operating temperatures, and switching tests.
- Group B Conformance inspection consists of environmental, life tests, and electricals.

Discrete Semiconductor Assembly Process

Qualification conformance inspection (QCI) testing

- Group C testing is performed on an annual basis after initial qualification and consists of physical dimensions, mechanical and environmental testing and 1,000 hour life test.
- Group D testing is performed at device radiation characterization at initial device qualification and for radiation wafer lot qualification testing including static electrical tests.
- Group E testing is performed at device qualification and requalification as required and consists of electrical and environmental testing.

Acronyms

DC	Direct Current
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSFC	Marshall Space Flight Center
NASA	National Aeronautics and Space Administration
NEPAG	NASA Electronic Parts Assurance Group
NEPP	NASA Electronics Parts and Packaging
PDA	Percent Defective Allowable
PIND	Particle Impact Noise Detection
SPC	Statistical Process Control
TO	Transistor Outline
TM	Test MethodUA not an acronym
UB	not an acronym

NEPAG

THANK YOU !

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