National Aeronautics and Space Administration

Progress Towards SiC ASICs for Extreme Temperature and Radiation Environments

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https://go.nasa.gov/sic

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Outline

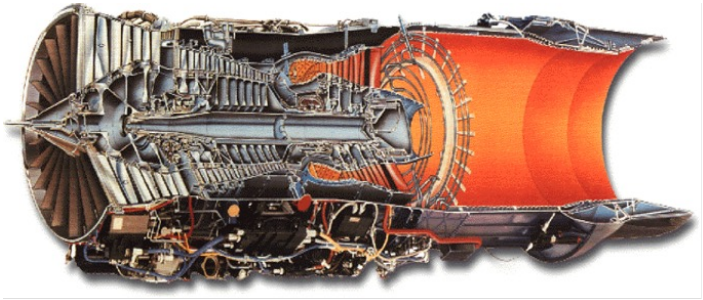
- 500 °C Durable SiC JFET IC Technology

- High Radiation Environment Potential

- Path to ASIC Manufacturing & Infusion

High-T Electronics Benefits to NASA Missions

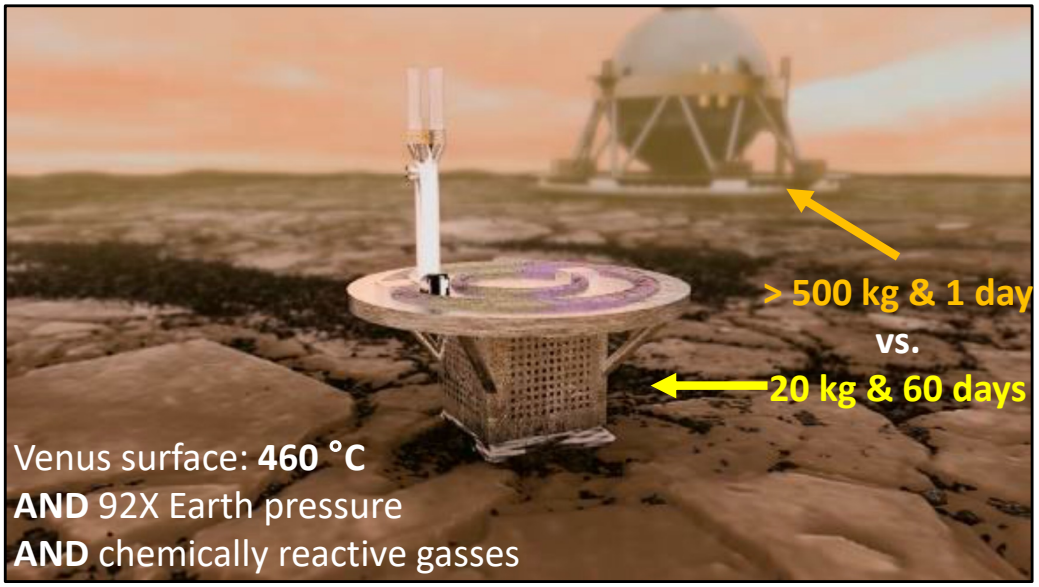
Intelligent Propulsion Systems



T > 450 °C sensors with electronics in key engine areas for realizing advanced concepts in distributed control and compressor/combustion instability detection and avoidance for improving engine performance
- Thrust to weight ratio
- Fuel efficiency & emissions

Power devices for aerospace electric propulsion and actuation

Venus Exploration Landers[1]



Long duration landers require electronics that endure the Venus surface environment

[1] T. Kremic and G. W. Hunter, Bulletin of the American Astronomical Society, vol. 53, (2021)

High Temperature Semiconductor Device Development

Prototype T > 450 °C operation has been reported for decades.

- Multiple research groups (industrial, academic, and governmental)
- Multiple semiconductor materials (SiC, III-N, silicon-on-insulator)
- Multiple transistor approaches (JFET, MESFET, MOSFET/CMOS, and Bipolar)

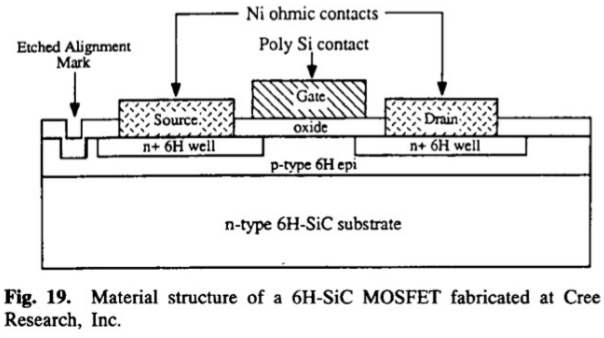
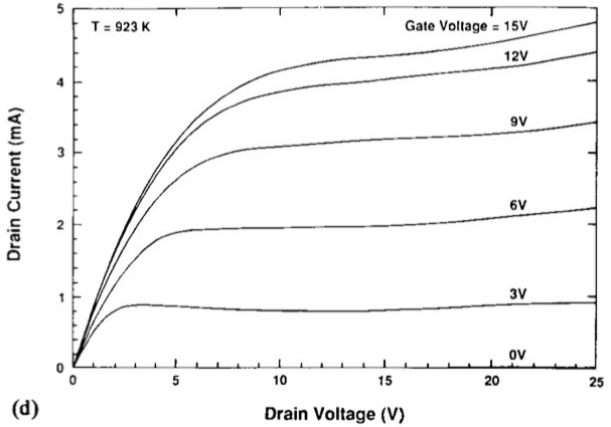


Fig. 19. Material structure of a 6H-SiC MOSFET fabricated at Cree Research, Inc.



Davis et al., Proc. IEEE, vol. 79, no. 5 pp. 677-701 (1991).

Missing from majority of reports: Long term operational stability at T > 450 °C

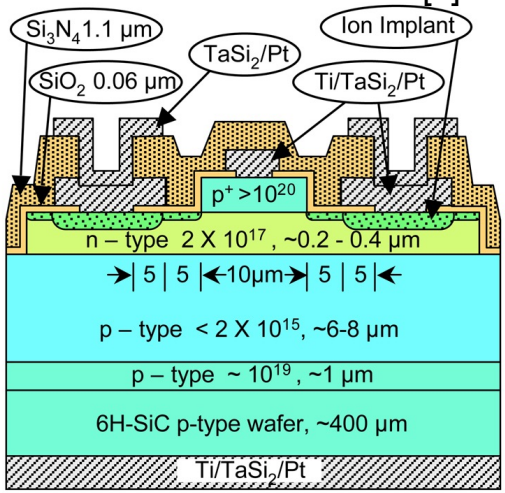
- In most cases, only brief (~ 1 hour) heated probe-station testing

Demonstrations insufficient for serious consideration by systems designers

Durable Transistor Device Approach

Epitaxial SiC n-JFETs developed as the most straightforward foundational transistor for achieving maximum durability in extreme environments

2007 NASA 6H-SiC JFET [1]



SiC is the most stable/inert semiconductor crystal
- Low impurity diffusion, low reactivity

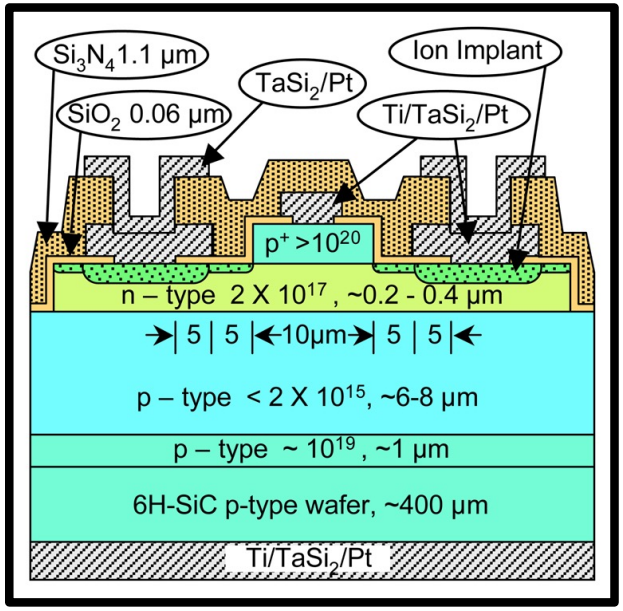
Inherent JFET High-T Stability Advantages
- Majority carrier device
- Low-leakage epilayer PN homojunctions
- Minimal sensitivity to p-type (gate) contact
- N-type ohmic contacts/implants

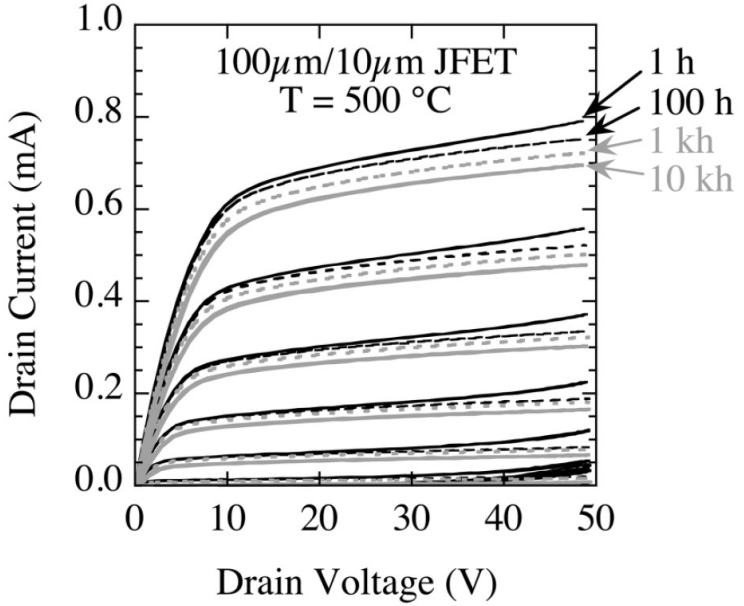
Other transistor types are more challenging to render stable/durable at T > 450 °C.
- Bipolar transistors: n-type AND p-type contact AND minority carrier sensitivity
- MOSFETs/CMOS: MOS junction sensitivity (charge injection, damage, interface states)
- MESFETs: Rectifying metal-semiconductor junction leakage & sensitivity at high-T
- III-N HFETs: Heterojunction sensitivity, more diffusion, more reactive than SiC at high-T

[1] Neudeck et al., IEEE Electron Device Lett. vol. 25, no. 5, pp 456-459 (2008).

NASA Glenn Low-Power 6H-SiC JFETs

Discrete packaged JFETs operate with excellent stability for 10,000 hours at 500 °C

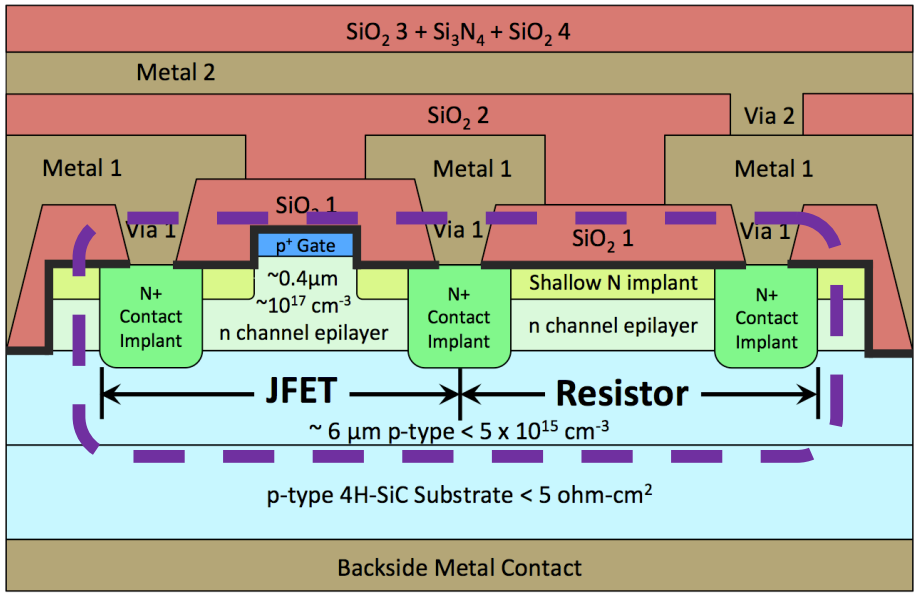




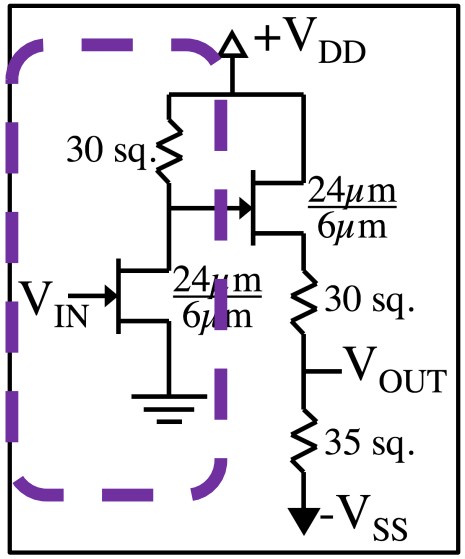
< 10% changes during 10000 hours of electrical operation in air at 500 °C!

D. Spry et al, Mat. Sci. Forum vol. 600-603, p. 1079 (2008)
Ohmic Contacts from R. Okojie et al, J. Appl. Phys, vol. 91, p. 6553, (2002)

Circuit Approach[1,2]



NOT Logic Gate Schematic



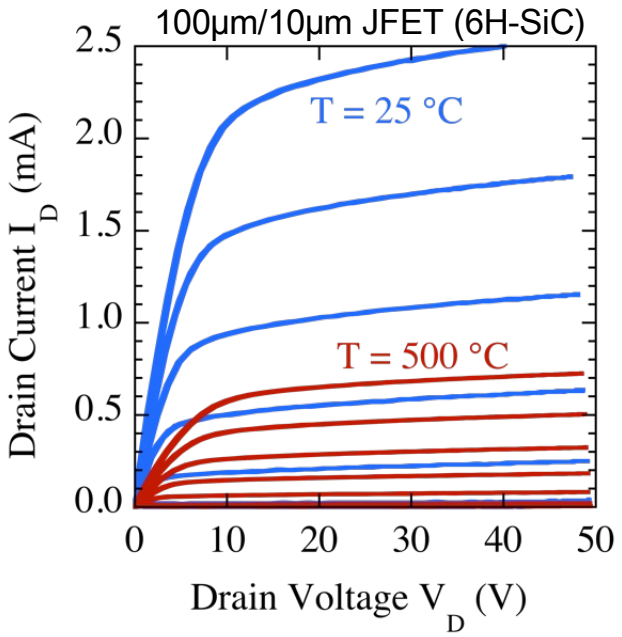
- **Resistors made with same epi as JFET → well-matched T dependence**
- Layout ratio based circuit design (not absolute component values)
- Negative threshold voltage V_T → negative signal voltages (roughly -1V to -10V logic)
- Typical V_{DD} = +25 V, V_{SS} = -25V Chip backside is biased at V_{SS}

[1]M. J. Krasowski, US Patent 7,688,117 (2010).
[2]P. G. Neudeck, et al., Proc. IMAPS High Temperature Electronics Conf., 2016, pp. 263-271.

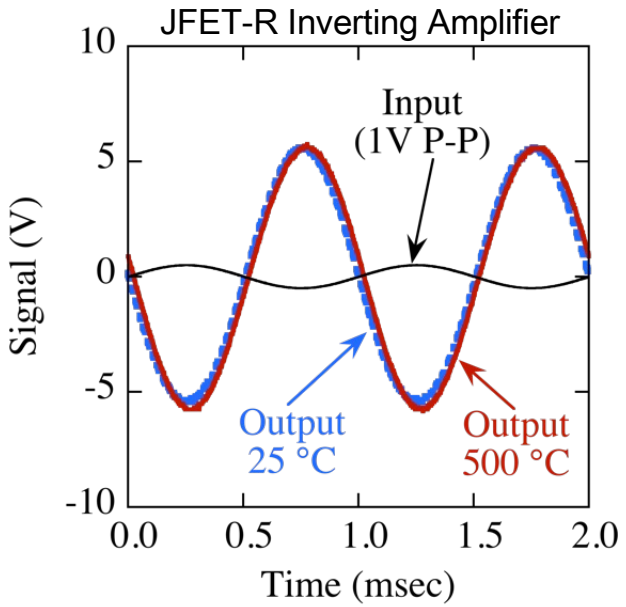
Temperature Performance

(Slide Presented at 2011 Electrochemical Society Meeting)

Transistor Characteristics



Circuit Characteristics

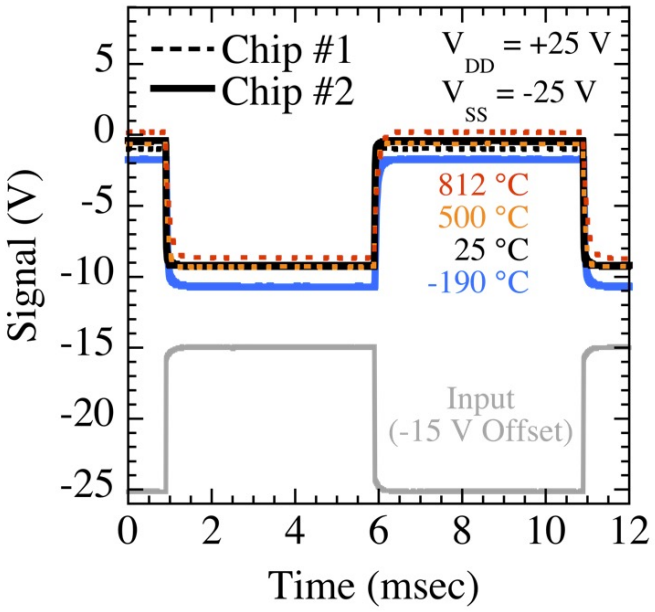


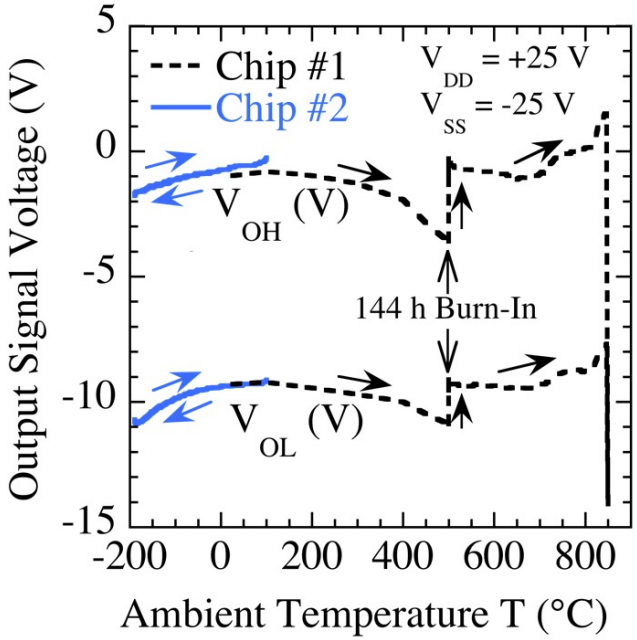
Despite large (> 3X) change in JFET characteristics…

…nearly temperature-independent circuit operation can be achieved!

-190 °C to +812 °C Functionality[1]

(Prototype IC Generation 10.1 NOT Gate)

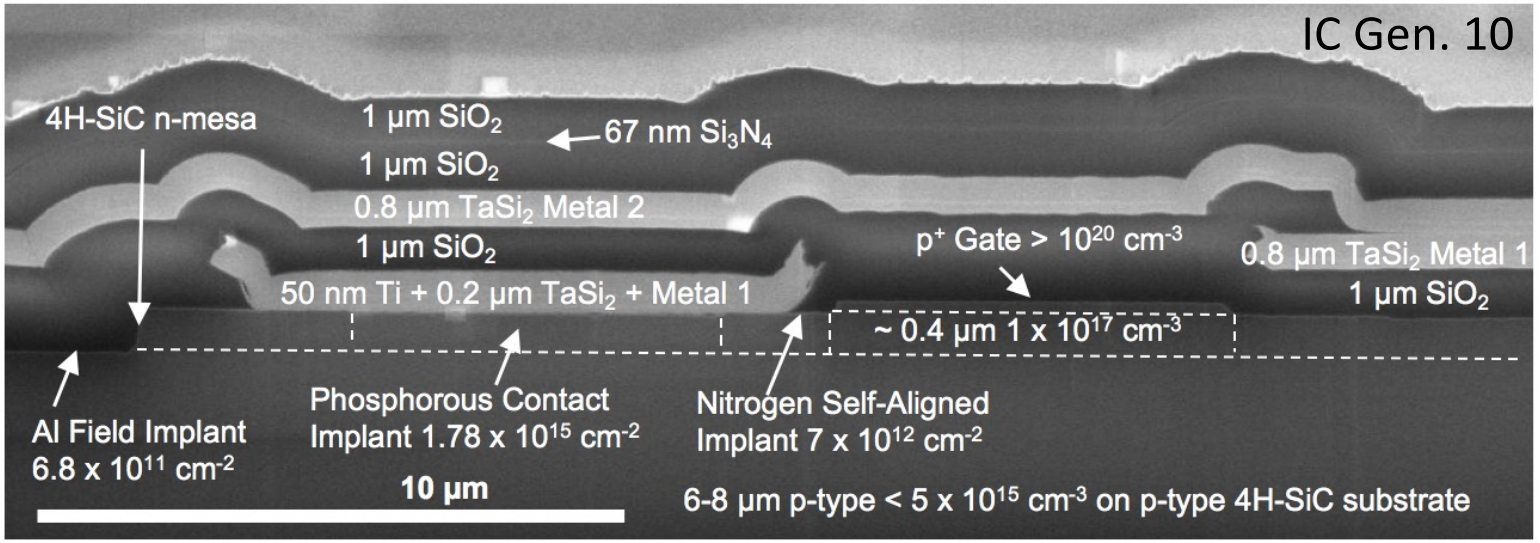




- **> 1000 °C temperature span without changing signal/supply input voltages.**
- Straightforward functional yield screening at 25 °C (on-wafer probe test).
- "Cold Start" capability crucial to many applications.

[1]Neudeck, Spry, Krasowski, Prokop, Chen, Materials Science Forum, vol. 963, pp. 813-817 (2019).

500 °C Stable Two Levels Interconnect[1]

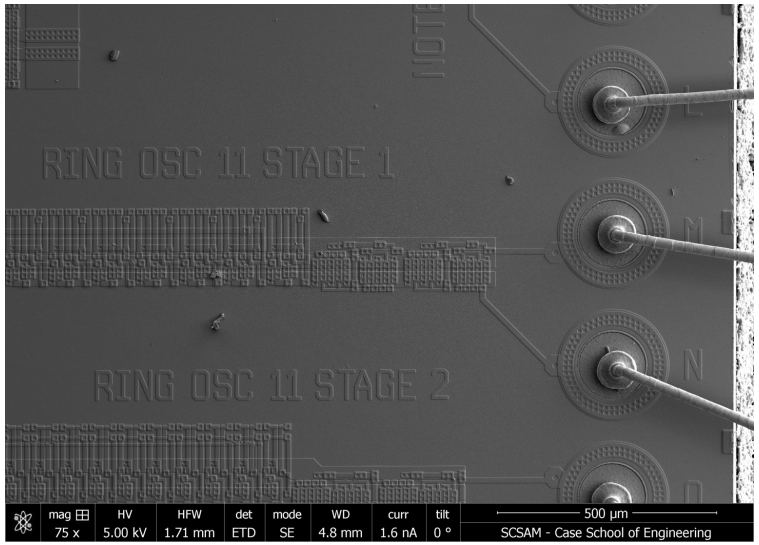


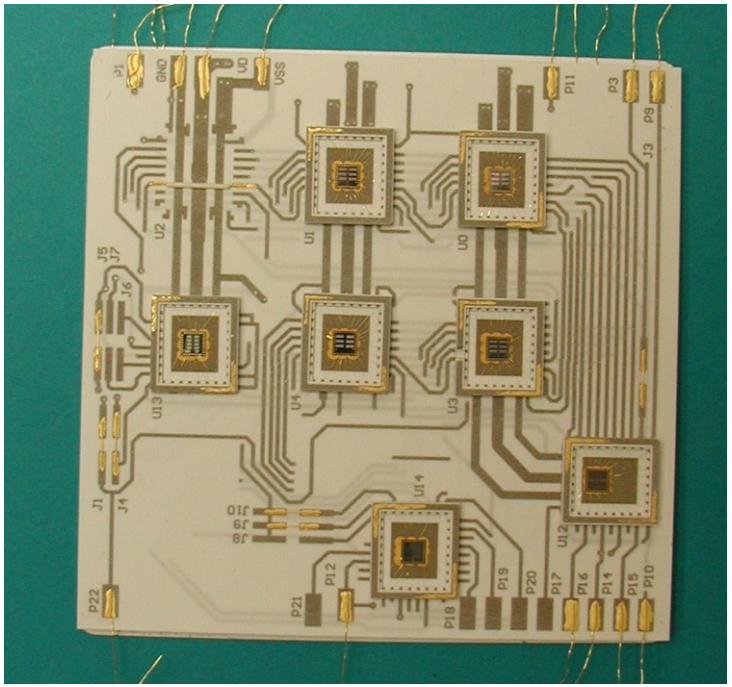
IC processing and materials compatible with SiC power device tools & manufacturing

- Close-proximity sputtering of $TaSi_2$ (21mm target to substrate spacing)
- LPCVD tetraethyl orthosilicate (TEOS) and Si_3N_4 layers deposited at 720 °C
- Interconnect completely buried beneath dielectric

[1]P. G. Neudeck, et al., 2018 IMAPS High Temperature Electronics Conf. pp. 71-78

500 °C Stable Bond Pads and Multi-Chip Packaging[1,2]

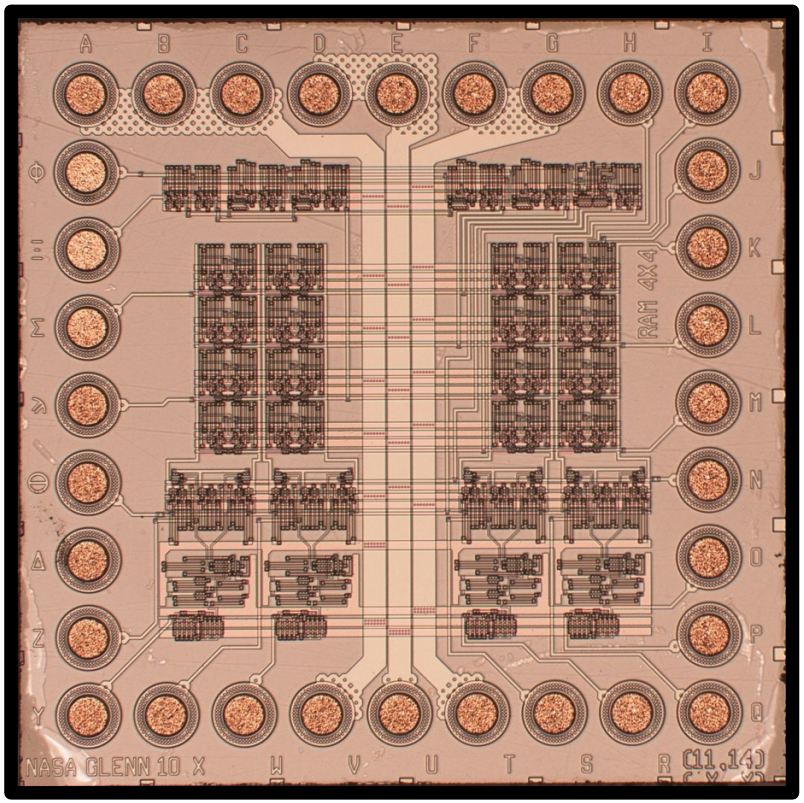




- "IrIS" bond pad metal stack anchored directly to SiC[1]
- Pt thick-film traces, Au/Pt pads, Au die attach (600 °C), and Au ball bonding[2].

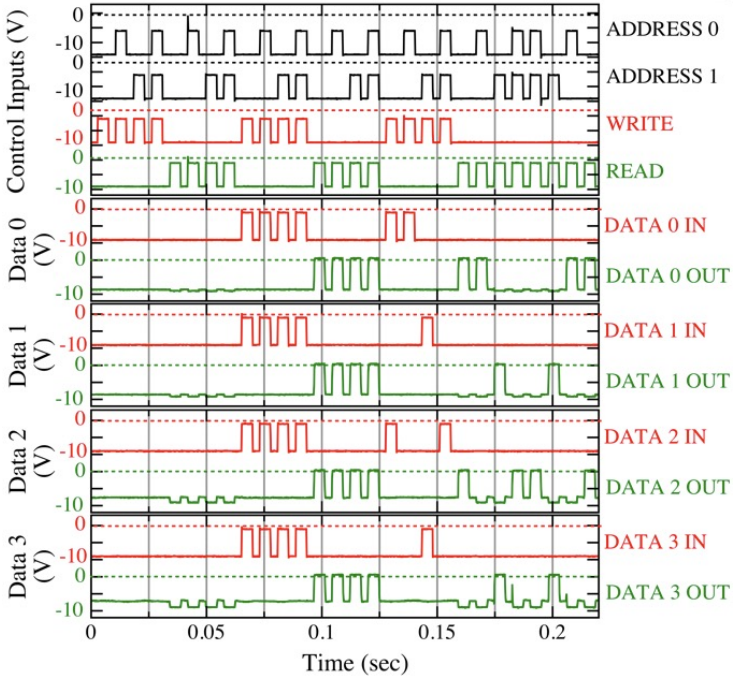
[1]D. Spry & D. Lukco, J. Electronic Materials 41 p. 915 (2012)
[2]L. Chen, et al., Proc. 2016 IMAPS High Temperature Electronics Conf. pp. 66-72

500 °C Durable NASA Glenn Gen. 10 SiC JFET-R RAM Chip[1]



RAM #2 Chip
T = 500 °C, **t = 421 days**

Write	Read	Write	Read	Write	Read	Reverse Address Order Read	Bitline Column
0000	0000	1111	1111	1100	1100	0011	Data 0
0000	0000	1111	1111	0010	0010	0100	Data 1
0000	0000	1111	1111	1001	1001	1001	Data 2
0000	0000	1111	1111	0010	0010	0100	Data 3

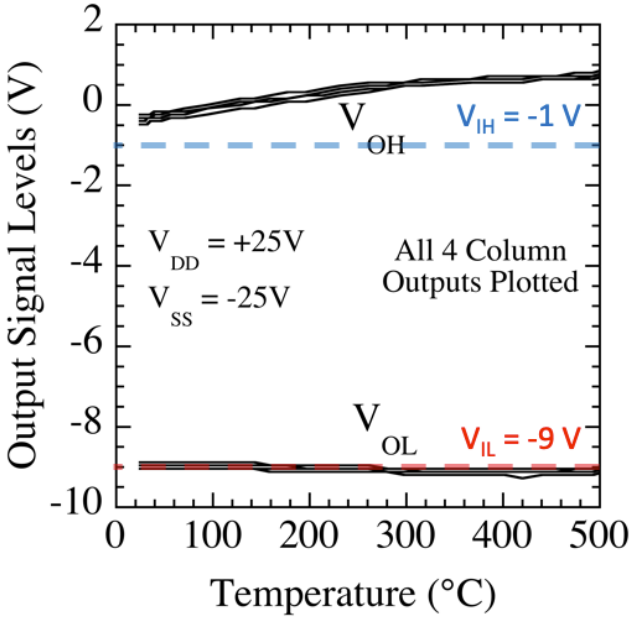


[1]P. G. Neudeck, et al., 2018 IMAPS High Temperature Electronics Conf. pp. 71-78

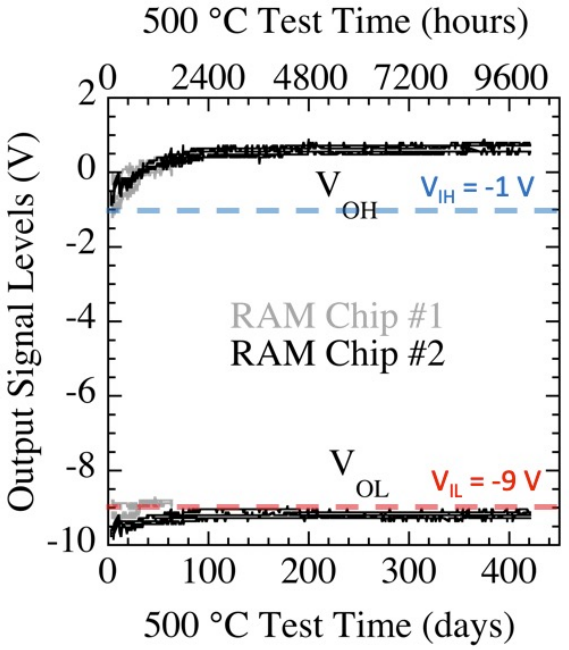
NASA Glenn Gen. 10 RAM Chip Output Levels

(2018 IMAPS High Temperature Electronics Conference)

vs. Temperature



vs. Time @ 500 °C

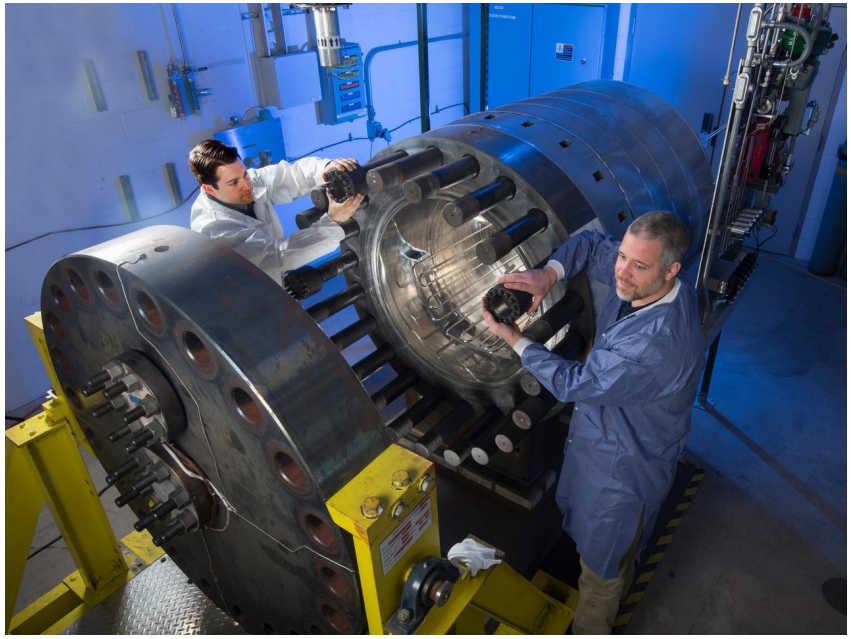


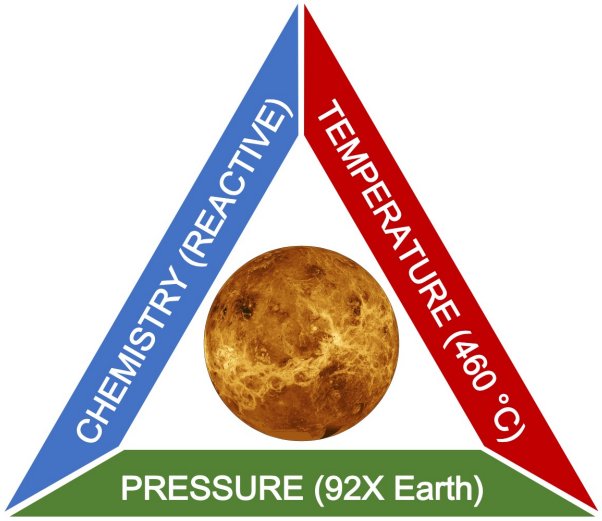
- ✓ Operation over broad application temperature range
- ✓ Prolonged (year+) operation at T > 450 °C for applications

NASA Glenn Extreme Environment Rig (GEER)

https://geer.grc.nasa.gov

800-liter test chamber for high-fidelity simulation of Venus surface environment





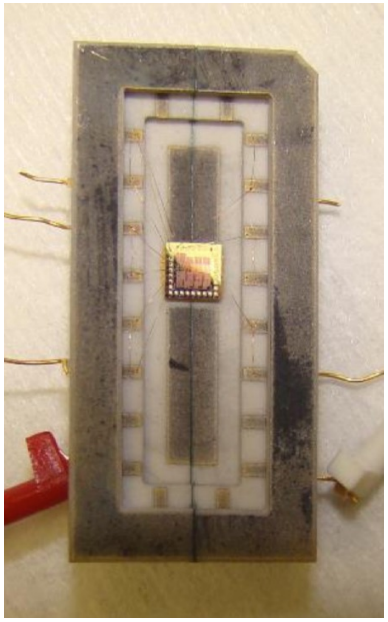
- **First 10 chemical constituents of Venus atmosphere.**
- 460 °C (860 °F), 1350 psia (~ 92 Earth atmospheres).
- Long duration (months) test runs.

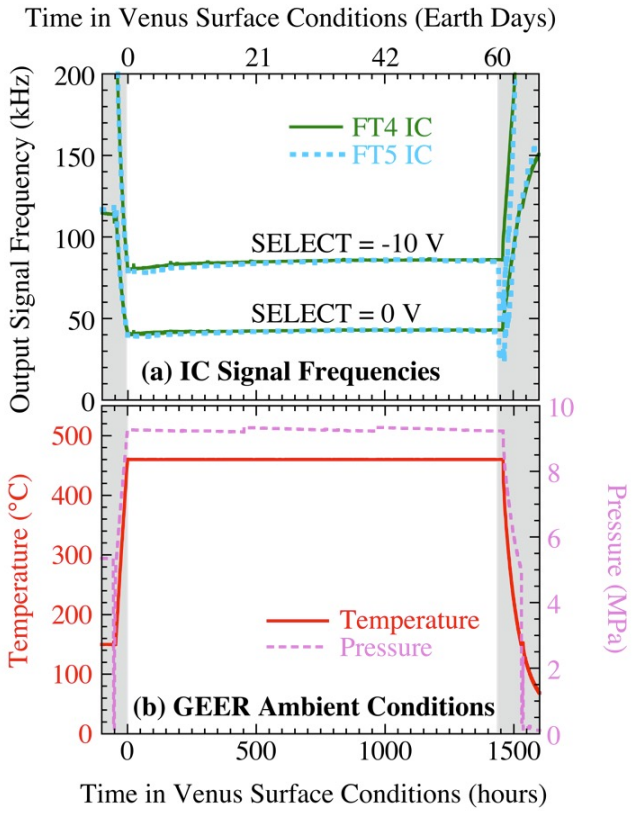
60-Day Venus Environment IC Test (in GEER)[1,2]

Two Generation 10 ÷2/÷4 Clock ICs (175 JFETs/chip) successfully operated in GEER Venus surface conditions for 60 days duration (lidless package).

Before GEER

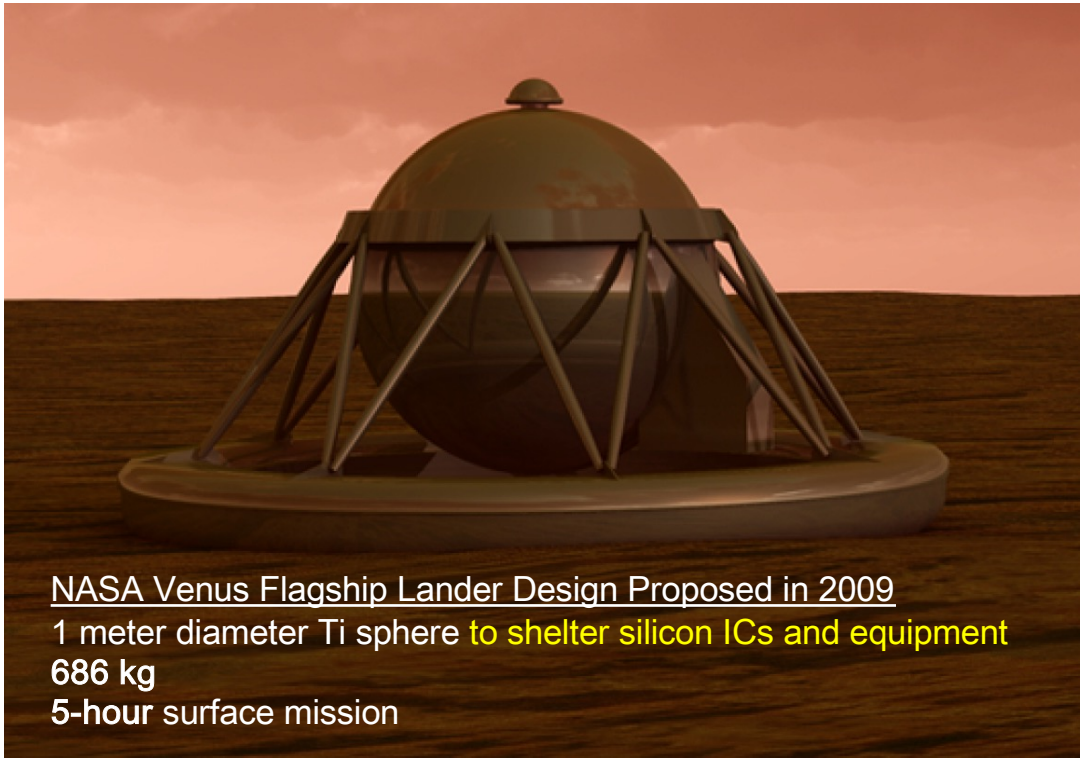
After 60 days GEER





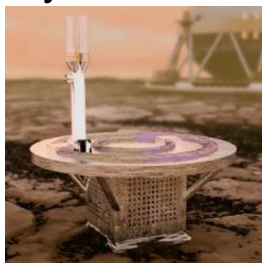
[1]Neudeck et al., IEEE J. Electron Devices Soc., vol. 7, p. 100 (2018).
[2]Chen et al., Proc. 2018 Int. High Temperature Electronics Conf.

Impact of Extreme Environment SiC Electronics



NASA Venus Flagship Lander Design Proposed in 2009
1 meter diameter Ti sphere to shelter silicon ICs and equipment
686 kg
5-hour surface mission

New Venus Lander Concept
Unsheltered SiC ICs
< 20 kg (mostly battery)
60-day surface mission



Completely new mission approach with superior capability enabled by SiC ICs.

Outline

- 500 °C Durable SiC JFET IC Technology

- High Radiation Environment Potential

- Path to ASIC Manufacturing & Infusion

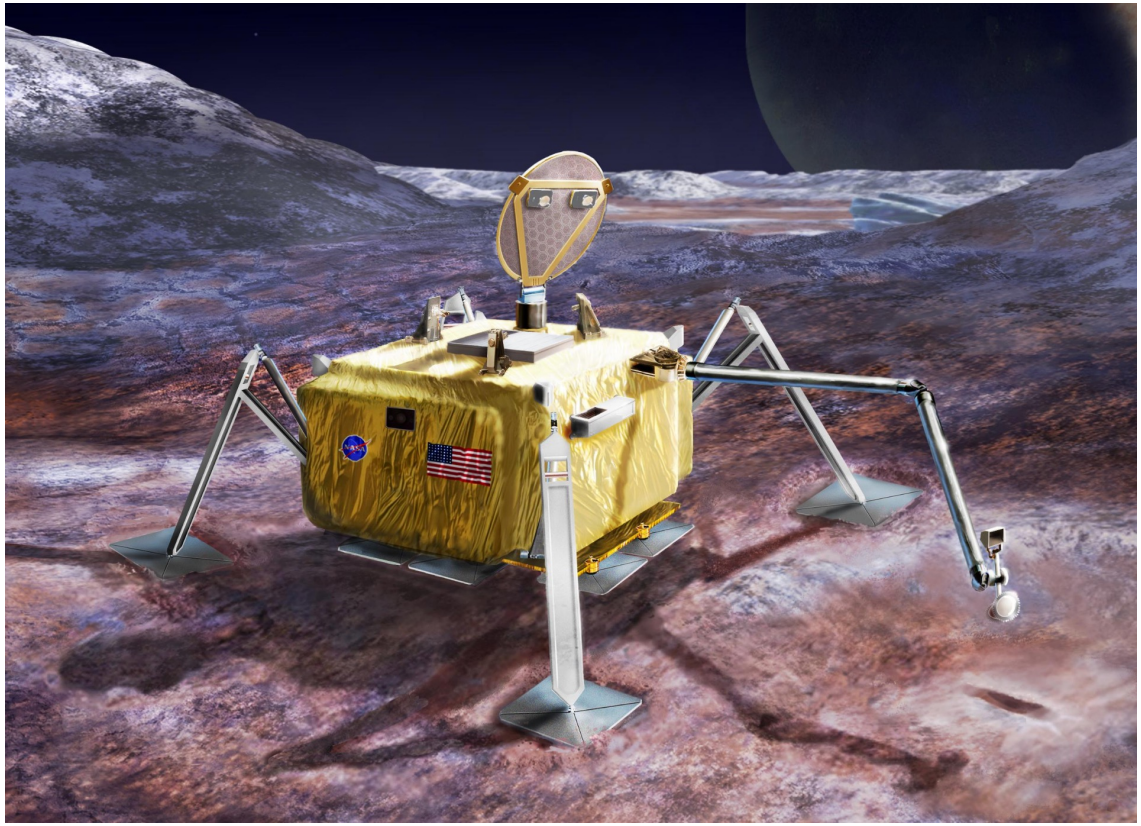
Juno Mission Electronics Vault

https://science.nasa.gov/mission/juno/

https://en.wikipedia.org/wiki/Juno_Radiation_Vault

- Jupiter system missions inherently operate in high-radiation environment.
- Spacecraft mission trajectory selected to minimize radiation belt exposure.
- Anticipated mission total ionizing dose near 20 Mrad.
- The electronics shielding radiation vault weighs about 180 kg, comprised of 1 cm thick titanium walls.
- Total spacecraft weight = 1593 kg (without propellants)

Europa Lander Mission Study Concept



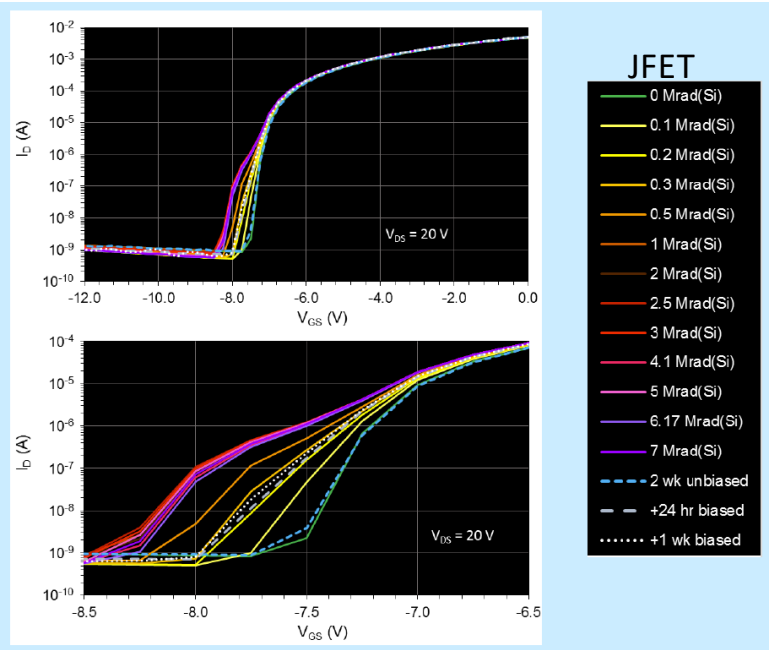
- Jupiter system missions inherently operate in high-radiation environment.
- Large, heavy, immobile lander.
- Present electronics shielding vault mass prohibitive to mobile rover mission.
- Substantial improvement in rad-hard electronics could remove sufficient electronics shielding mass to enable rover missions to travel and study multiple sites of greatest interest (e.g., active geysers!).

https://www.jpl.nasa.gov/images/pia21048-europa-lander-mission-concept-artists-rendering/

Radiation Testing of NASA Glenn JFET ICs[1]

Generation 10 JFETs, Oscillators, Flip-Flops, Op-Amps tested by NASA Goddard

Total Ionizing Dose
(Gamma to 7 MRad without failure)



Single Event Effects
(Heavy Ion Strike up to Gold)

Ring Oscillator

- No destructive effects at LET(Si) = 86 MeV-cm²/mg
- Only small glitches recorded

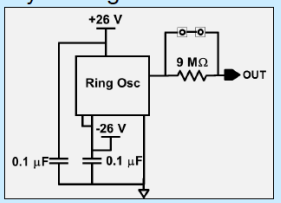


Fig.16. Ring oscillator test circuit.

Summary

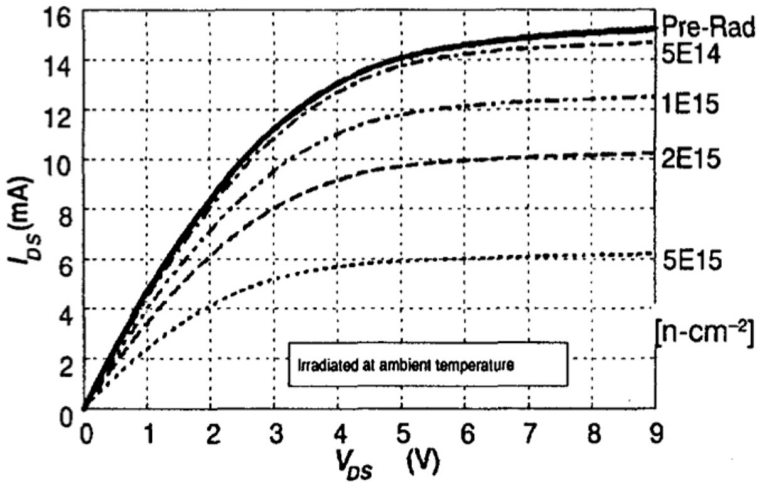
Prototype 4H-SiC JFET ICs developed & fabricated at NASA GRC for harsh Venus conditions demonstrate potential for Jovian-type environments as well:

- **> 7 Mrad(Si) TID tolerance**
- **No destructive SEE at LET(Si) = 86 MeV-cm²/mg**
- **SEUs occurred in the clock circuit**
  - **3.5 MeV-cm²/mg ≤ onset LET(Si) ≤ 9.6 MeV-cm²/mg**

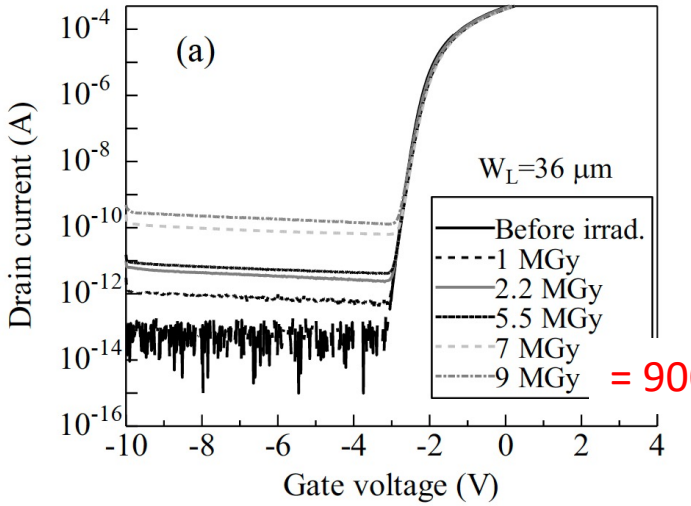
[1]Lauenstein et. al., 2019 IEEE Radiation Effects Data Workshop (REDW)

SiC JFET Radiation Testing Results in Literature

Neutrons[1]



Total Ionizing Dose (TID)[2]



= 900 Mrad!

Similar radiation hardness is feasible when SiC JFET-R ICs get tested to these radiation levels.

[1]McClean et al., IEEE Trans. Nucl. Sci. 41(6) 1884 (1994)

[2] Takeyama et al., Mat Sci Forum 1004 1109 (2020).

Outline

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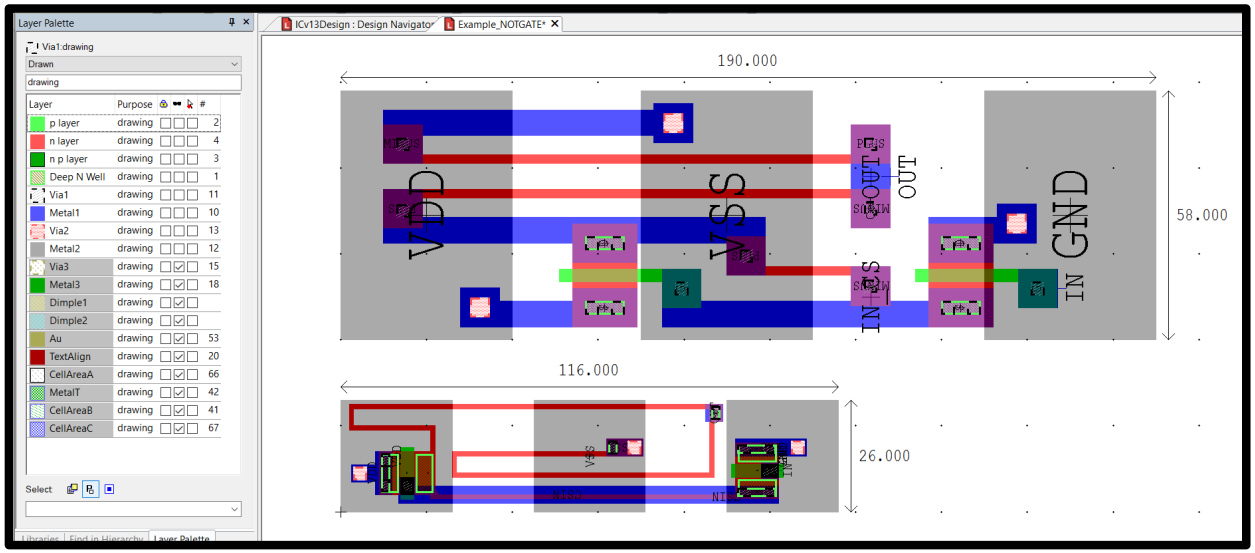
Online SiC JFET-R IC Design Guide

https://go.nasa.gov/jfetic



Gen. 12
NOT Gate Area
11021 µm^2

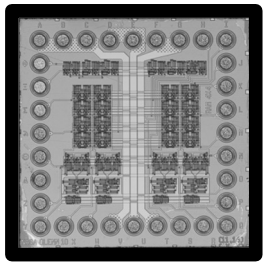
Gen. 13
NOT Gate Area
3016 µm^2

- SPICE models for circuit design and mask layout rules (Gen. 12 and Gen. 13)
- External partner IC designs are in Gen. 12 fabrication run (Space Act Agreements)
- Commercial SiC JFET-R IC design services available (https://www.ozarkic.com)
- Collaborative project to improve design kit and manufacturing access is pending

Prototype SiC JFET-R Random Access Memory (RAM) ICs

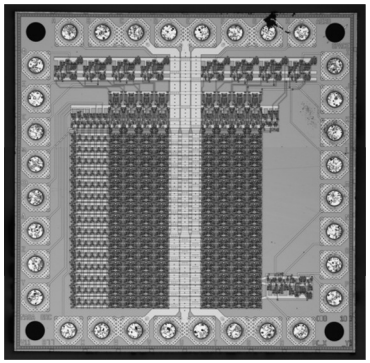
Benchmark of on-going IC upscaling needed to meet broader range of missions/applications

"IC Gen. 10"
16-bit RAM
~200 JFETs
3 mm x 3 mm
> 1 year @ 500 °C [1]



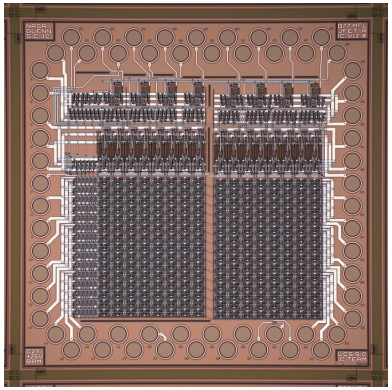
Fab: NASA Glenn

"IC Gen. 11"
120-bit RAM
~ 1000 JFETs
4.65 mm x 4.65 mm
Not 500 °C Durable [2]



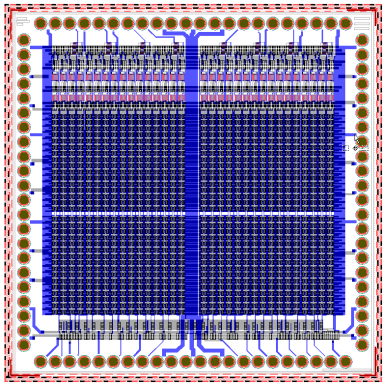
Fab: NASA Glenn

"IC Gen. 12"
248-bit RAM
~ 2000 JFETs
5 mm x 5 mm
In Fabrication



Fab: GE Aerospace and NASA Glenn

"IC Gen. 13"
1024-bit RAM
~ 8000 JFETs
5 mm x 5 mm
Finished Design



Fab: GE Aerospace and NASA Glenn

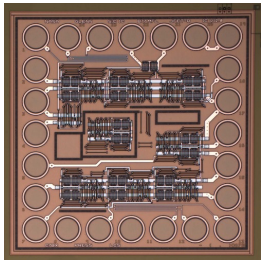
[1] P. Neudeck, D. Spry, Mat. Sci. Forum **1004** p. 1057 (2020).
[2] D. Spry, P. Neudeck, C. Chang, Mat. Sci. Forum **1004** p. 1148 (2020).

50 Application Specific Integrate Circuit (ASIC) chip designs are being fabricated in IC Gen. 12

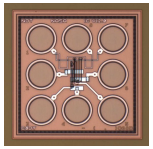
Including:

- Microprocessor dual-chip (assembly language)
- 8-bit analog to digital (serial output), digital to analog
- 2-kbit mask-programmed ROM, 248-bit RAM
- Venus lander control and analog-to-digital conversion
    - 4-channel 6-bit “Tech Demo”
    - 16-channel 8-bit “Exploration Mission”
    - Microseconds to hours clock/timer
- Venus imager array signal processing
- 12 customized analog sensor amps (op-amp based)
    - Wind, pressure, temperature, gas, & battery
- Power JFET chips for paralleling in power module
- External customer Space Act Agreement chips
    - Makel Engineering (NASA/MEI designed chip)
    - Ozark IC (Ozark IC designed chip)
    - Draper Labs (Draper designed half-chip)
- Miscellaneous logic (gates, flip flops, multiplexors, tri-states), analog (op-amp), and process test chips

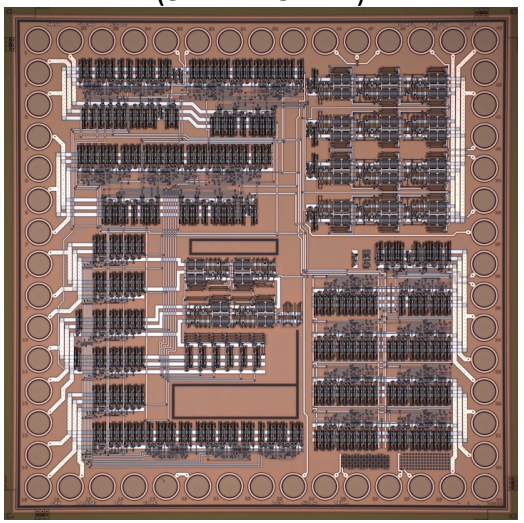
Pressure Sensor ASIC
(2.5 mm x 2.5 mm)



NOT Gate Chip
(1.3 mm x 1.3 mm)

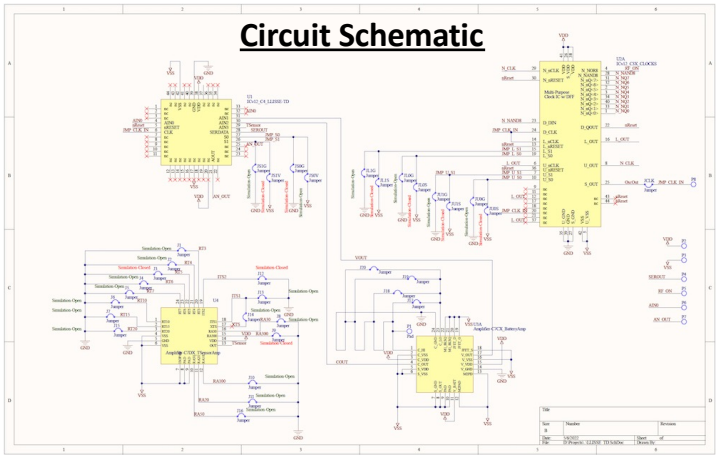


Venus Lander Control ASIC
(5 mm x 5 mm)

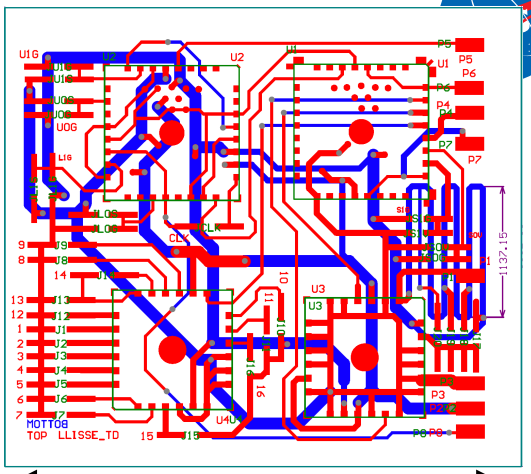


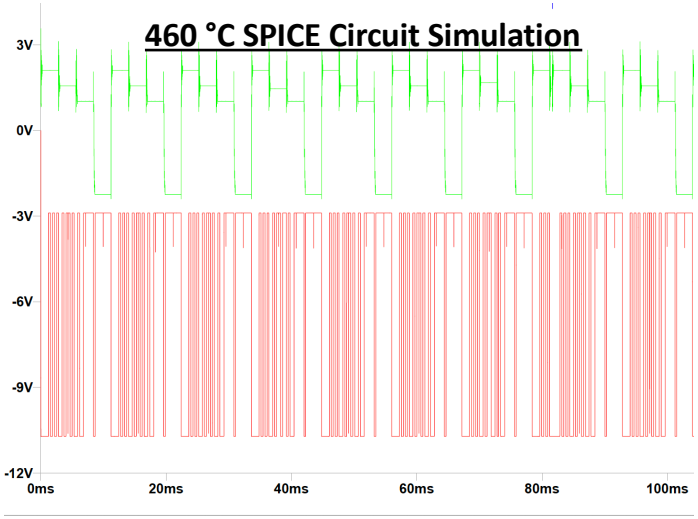
Venus Lander Tech Demo (TD) Control Demonstration Board

Accomplishes timing, control, and digitization for long-lived Venus lander demonstration mission



Circuit Board Layout
2-sided with through vias
4 chips
11.4 cm x 10.1 cm

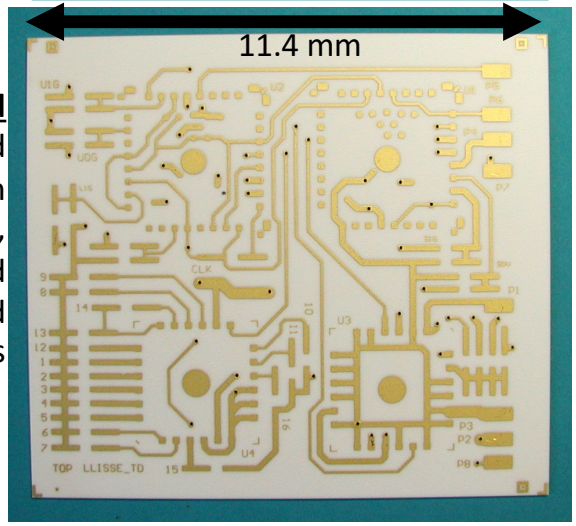




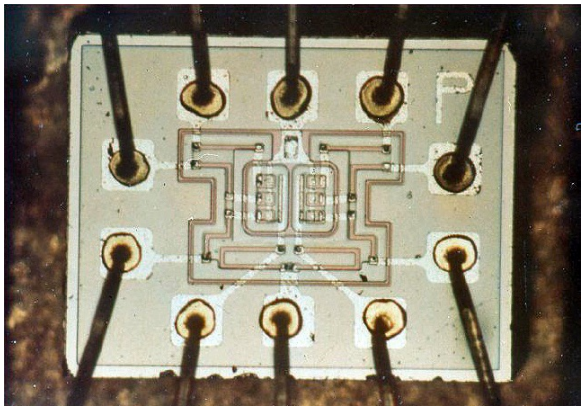
DAC output wave

Output data bitstream

Circuit Board
Manufactured by Thick Film Technology, Inc., to be populated with packaged IC Gen. 12 chips



“Simple” ICs Explored The Solar System



Apollo flew using 6 transistors per chip ICs.

Voyager spanned the solar system and Viking landed on Mars using few thousand transistors/chip ICs.

Durable SiC JFET-R ICs are already reaching a useful level of complexity.

Summary Perspective

For infusion into most applications, IC-based systems must be stable, durable, and reliable FOR MANY YEARS across the entire intended application environment range.

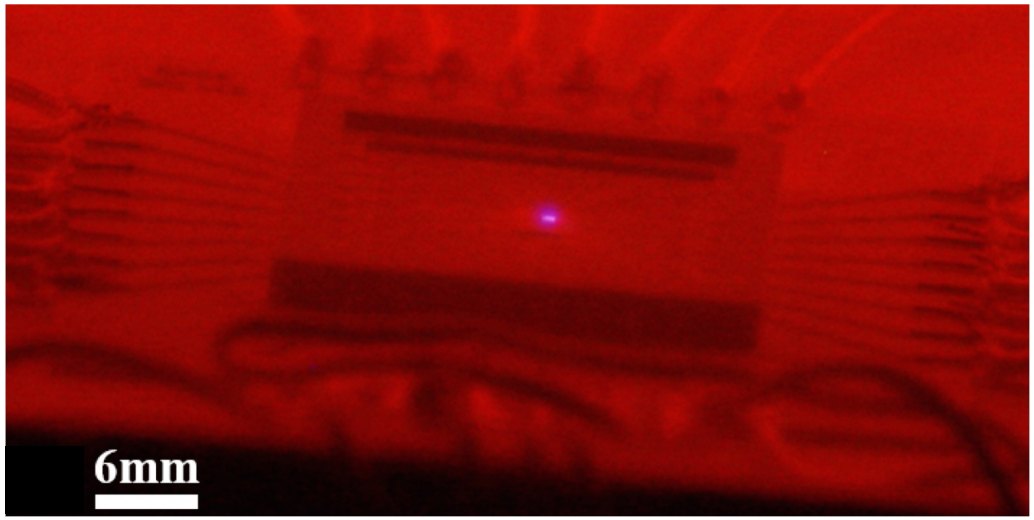
To date, NASA Glenn SiC JFET-R is the only semiconductor IC approach to have demonstrated 1+ year stable operation at 500 °C. Radiation tolerance appears good, but quantitative limits remain to be ascertained by future studies.

For more conventional temperatures, less-durable IC-based technologies are viable options (usually at lower cost and higher functionality).

With technology improvement, upscaling and access to IC foundry design and manufacturing, SiC JFET-R can enable important improvements to high-value systems (aerospace, automotive, energy production, etc.).

Conclusion

SiC JFET-R ICs now demonstrating application-viable prolonged functionality in previously inaccessible extreme environments.

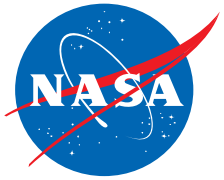


Potentially “Go Anywhere” ICs

- High temperature +500 °C
- Low temperature -190 °C
- High radiation (TBD)
- Venus surface +460 °C
- Analog and digital
- Ceramic multi-chip packaging

Migration underway towards foundry manufacture to enable widespread access to novel extreme environment IC capability

Image from D. Spry et al., https://ntrs.nasa.gov/citations/20170001674



NASA Glenn SiC Team Website: https://go.nasa.gov/sic
NASA Glenn SiC JFET IC Technology Guide: https://go.nasa.gov/jfetic
NASA Glenn Microsystems Fabrication Lab: https://www1.grc.nasa.gov/facilities/microfab/