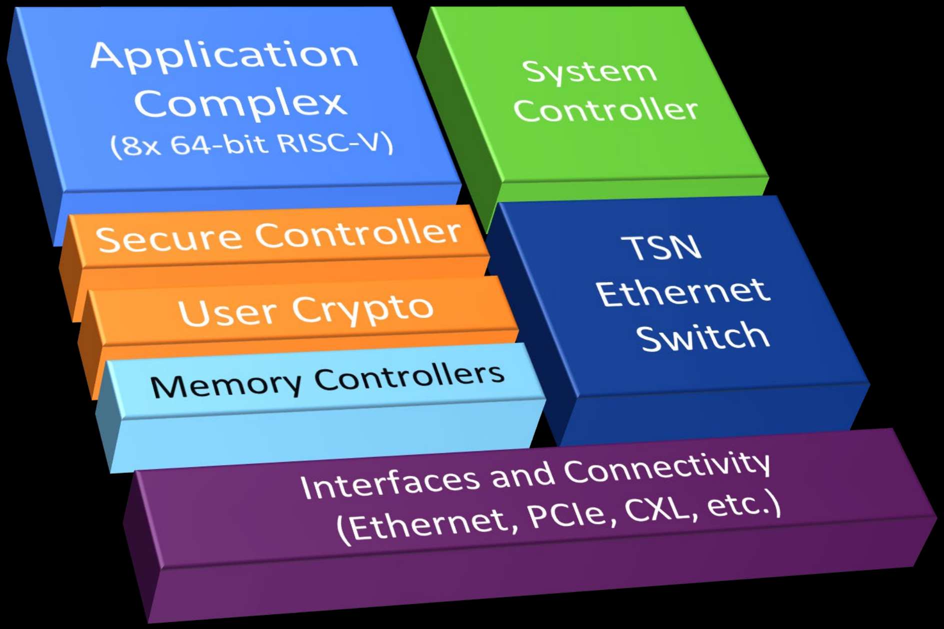
EXPLORE SPACE TECH
TECHNOLOGY DRIVES EXPLORATION

NASA High Performance Spaceflight Computing (HPSC) Overview

Wesley Powell – NASA STMD Principal Technologist for Advanced Avionics
Wesley.A.Powell@nasa.gov, 301-286-6069

To be presented at the Core Flight Executive / Core Flight Software (cFE/cFS) Symposium, Greenbelt, MD,
January 29, 2025

What is HPSC?



- **100X the computational capacity of current space flight processors**
- **Multicore architecture provides unprecedented flexibility between computational performance, power management, & fault tolerance**

- **NASA Program:** (Partnership jointly funded by STMD and Microchip): HPSC advances the capabilities of space-based computing for upcoming missions. Infusion targets across human, robotic, and science missions

---

- **Requirements:** Jointly developed by NASA, JPL, and Microchip

---

- **Fault-tolerant 10-core Heterogenous RISC-V Architecture:** Extremely high performance per watt. Radiation hard by design

---

- **Initial Delivery**: SoC, Evaluation Board, Software Stacks, Models, Education & Training, Application Support

---

- **Industry Eco-System**: Industry-funded, HPSC-compatible roadmap benefits NASA, JPL, mil-aerospace, & terrestrial applications for decades to come

---

- **Capability Advances:** Cost, Schedule, Risk reduction: Mission and science autonomy, intelligent vehicles, flagship science, crew assist. Software-based flexibility

Candidate Applications

Application	Description	Key Challenges
Science spacecraft avionics	• Spacecraft health/safety management • Station keeping • Subsystem/instrument control and data handling	• Varies by mission size, environment, and class
Crewed vehicles avionics	• Spacecraft health/safety management • Station keeping • Environmental Control and Life Support System (ECLSS) management • Crew interface • Subsystem control and data handling	• Fault tolerance, ranging from 2 FT and 1 FT to single string, based on application criticality • Mission life • Serviceability
Crewed habitat avionics	• Spacecraft health/safety management • Station keeping • ECLSS management • Crew interface • Subsystem control and data handling	• Fault tolerance, ranging from 2 FT and 1 FT to single string, based on application criticality • Mission life • Serviceability • High sensor count • Earth independent operations


PACE Spacecraft


Gateway


Lunar Habitat Concept

Candidate Applications

Application	Description	Key Challenges
Rover avionics	• Rover health/safety management • Situational awareness • Traverse path planning • Mobility control • Subsystem/instrument control and data handling • Crew interface (for crewed exploration rovers)	• Processing performance for autonomous driving • Fault tolerance • Power efficiency • Operational flexibility • Harsh environments
Planetary aerobot avionics	• Aerobot health/safety management • Situational awareness • Path planning • Flight control • Subsystem/instrument control and data handling	• SWaP efficiency • Processing performance for autonomous flight • Fault tolerance • Operational flexibility • Harsh environments
Space suit avionics	• Suit health/safety management • Crew health/safety management • Crew interface	• SWaP efficiency • Resource efficient graphics processing • Fault tolerance


Spirit Rover


Mars Ingenuity Helicopter

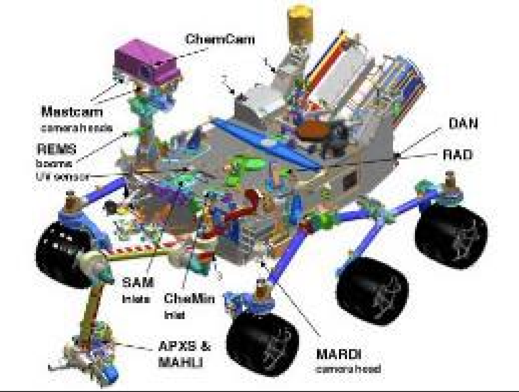

Space Suits

Candidate Applications

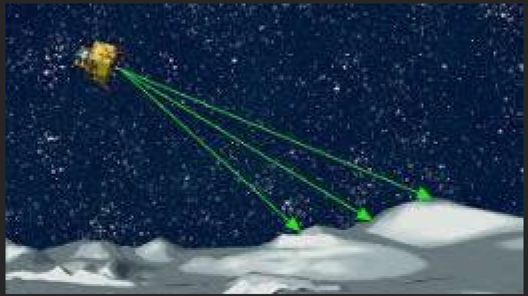
Application	Description	Key Challenges

Science Instrument Data Processing and Control	• Land imagers
	• Telescopes
	• Mass specs
	• Lidar
	• Radar
	• Cameras
	• Radiometers
	• Magnetometers
	• Biological and physical science experiments
		• Varies by instrument, but can include:
		  • Adaptive wavefront sensing and control
		  • Data reduction
		  • Low-latency alert generation
		  • SWaP sensitivity
		  • Harsh environments
		  • Autonomous operations

Landing systems	• Autonomous landing and hazard avoidance • Terrain relative navigation • Hazard detection and avoidance	• Fault tolerance (based on mission class), ranging from 2 FT to 1 FT • Operate through faults • Performance for terrain mapping and path planning
Communication relay	• In-space or surface relays for crewed and/or science missions using Delay Tolerant Networking (DTN) • Navigation and timing signals	• High bandwidth I/O • High bandwidth encryption/decryption • Onboard storage for buffering



Instruments on Curiosity Rover


ALHAT Concept


TDRSS Satellite

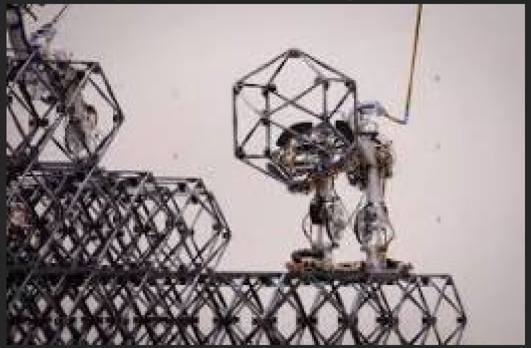
Candidate Applications

Application	Description	Key Challenges

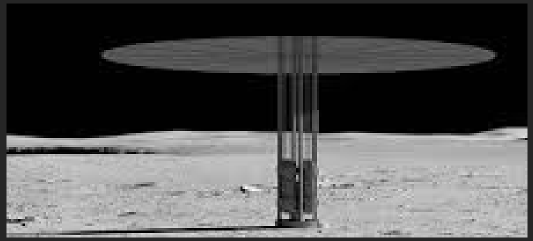
Robotics	• In-space and surface robotics, including:
	  • Rendezvous, Proximity Operations & Capture (RPOC)
	  • Servicing
	  • Assembly
	  • Construction
	  • Manufacturing
	  • Maintenance
		• Fault tolerance and safety for crew collaboration
		• Processing performance
		• Leveraging for industry standard interfaces
		• Leveraging for industry standard software tools (ROS support)
		• Mapping robotics applications to avionics requirements
		• Harsh environments

Surface systems and infrastructure for crewed presence	• Excavation and construction • In-Situ Resource Utilization (ISRU) • Surface power systems	• Processing performance to support robotics • Harsh environments
Space cloud computing	• Disaggregation of onboard processing applications to across multiple spacecraft or surface systems	• Communication overhead • Use cases identification and analysis needed

Integrated System for Autonomous and Adaptive Caretaking (ISAAC)

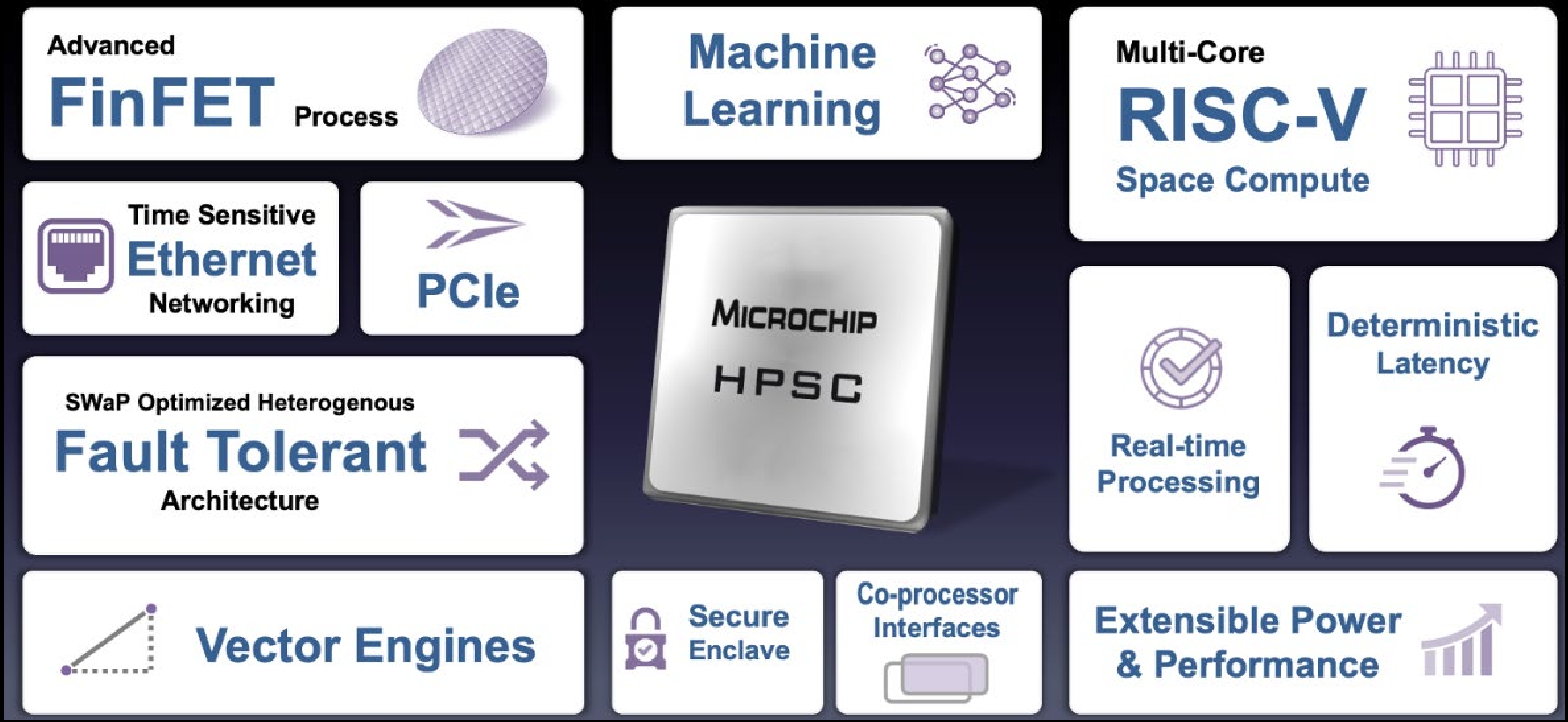


Automated Reconfigurable Mission Adaptive Digital Assembly Systems (ARMADAS)



Fission Surface Power

HPSC Architecture Highlights



HPSC Feature Highlights

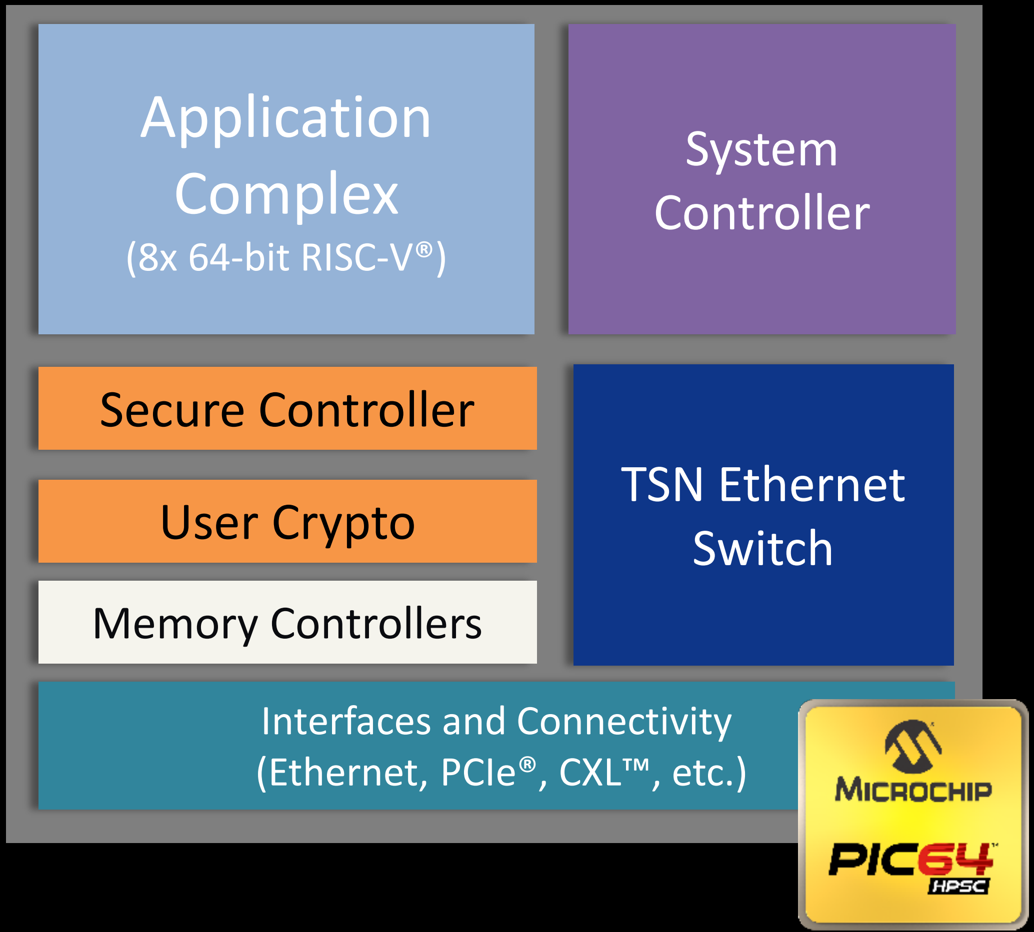
Radiation-Hardened and Radiation-Tolerant Versions Enable a Spectrum of Mission Profiles

Compute

Groundbreaking **64-bit RISC-V © Vector** processing with virtualization targeting Edge AI (SiFive X288/X280)

Security

Defense Grade Security Enclave supporting **Post-Quantum** Cryptographic algorithms



Fault Tolerance

Unprecedented **Fault-Tolerance** capabilities for Mission Critical Applications (DCLS, Split-Mode, WorldGuard)

Massive Connectivity

Integrated **240G TSN Ethernet** Switch, **10GbE**, **PCIe**/CXL and **RDMA** for Networking & Deterministic Connectivity

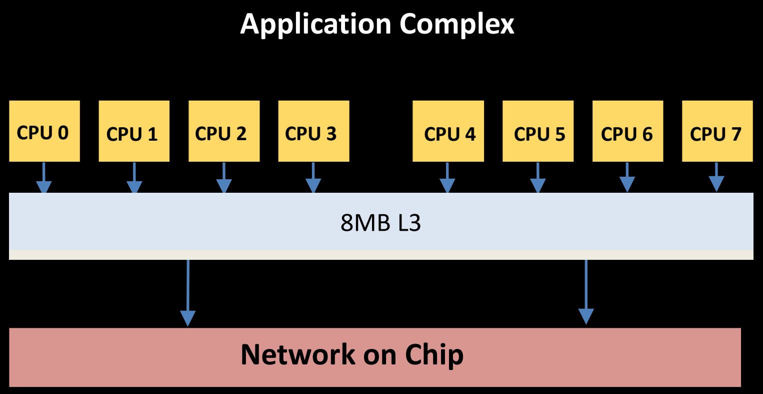
Mission Customization by Partitioning Modes

- The App Complex CPU cores can be configured for: Unified Mode, Split Mode or Cache-Isolated
  - Tradeoffs for performance, error detection, containment and availability
  - Combine with hypervisor to facilitate virtualization

High Performance ⟷ **Isolation and Fault Tolerance**

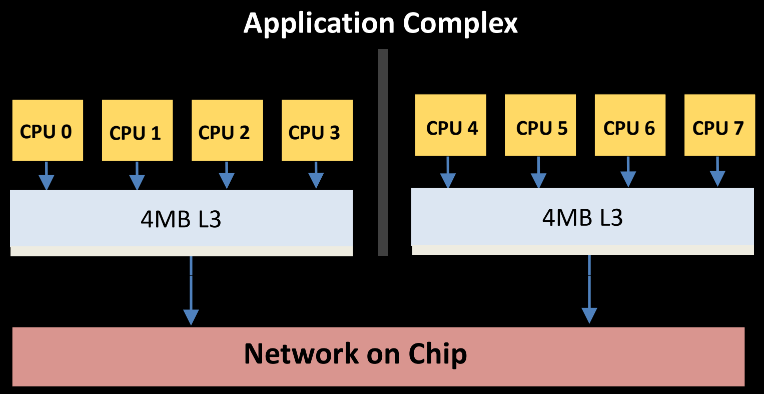
Unified Mode

Example:
- 8 core SMP Linux® or RTOS
- Highest overall performance



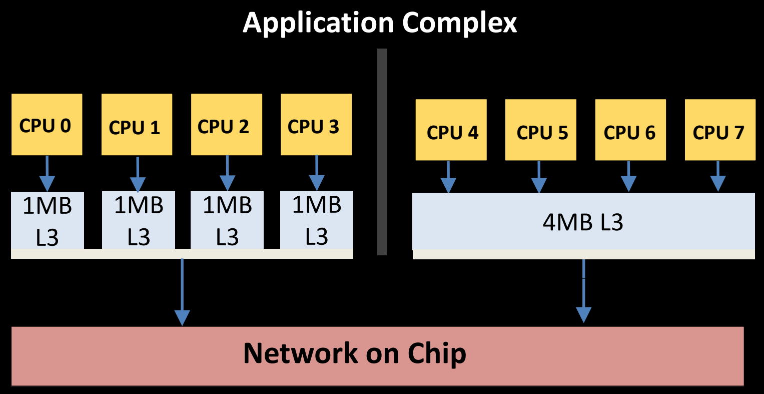
Split Mode

Example:
- 4 core SMP Linux + 4 core RTOS
- Strong isolation b/w 2 workloads with mixed criticality



Cache-Isolated + Split Modes

Example:
- 4 Core Linux + 4 isolated RTOS cores
- Further extend with DCLS for error containment & detection at core boundary



HPSC Compute Performance Stack Up

	HPSC	RAD-750	RAD-510	GR740	RAD-5545
Operating Frequency	1 GHz (POR)	200 MHz	462 MHz	250 MHz	466 MHz
CPU Core Microarchitectural Date	Present day	*Circa mid 1990's*	*Circa 2010*	Circa 2010	Circa 2010
Number of processor cores	10 (eight SiFive x280 and two SiFive s21)	1 (PowerPC 750)	1 (RAD5500)	4 (LEON4)	4 (RAD5500)
SpaceBench (speed-up v. GR740)	1,343x (@1GHz)	*N/A (less than GR740)*	*N/A (less than GR740)*	1.0 (baseline)	1.6
DMIPs	28,130 (@1GHz)*	400 (@200MHz)	1,386 (@462MHz)	1,700 (@250MHz)	5,592 (@466MHz)
Vector Processing Performance	256 GFLOPs*	*No hardware vector engine*	*No integrated vector engine*	*No hardware vector engine*	*No hardware vector engine*
AI/ML – BFLOAT16 Matrix Multiplication	1,024 GFLOPs*	*No hardware AI/ML support*	*No hardware AI/ML support*	*No hardware AI/ML support*	*No hardware AI/ML support*
AI/ML – INT8 Matrix Multiplication	2 TOPs*	*No hardware AI/ML support*	*No hardware AI/ML support*	*No hardware AI/ML support*	*No hardware AI/ML support*

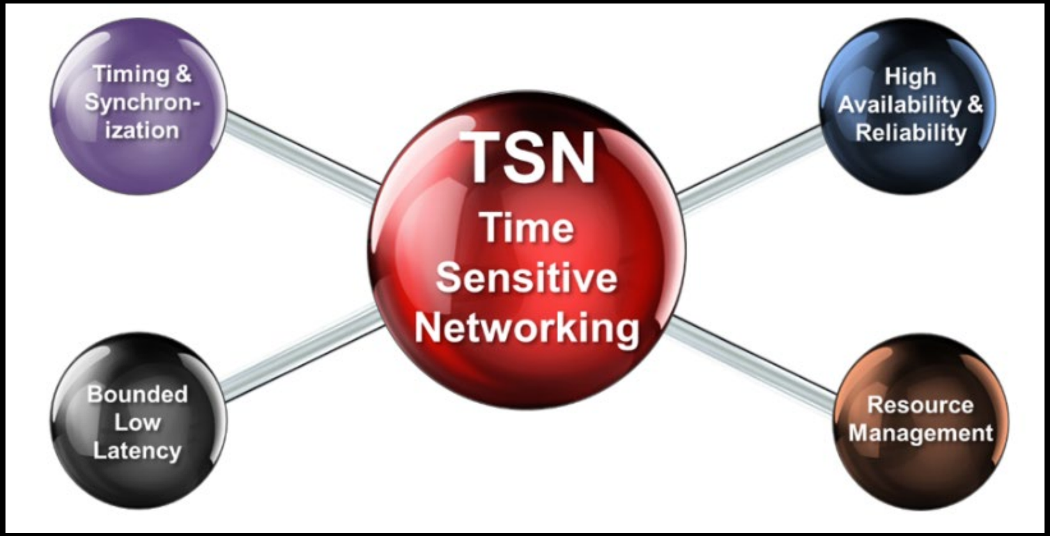
Time-Sensitive Networking (TSN)

TSN an IEEE 802 standard - enables us to transmit time-critical traffic over a standard ethernet physical medium, side by side with conventional ethernet traffic

Time-Sensitive Networking (TSN) Profiles (Selection and Use of TSN tools)

Audio Video Bridging	Fronthaul	Industrial Automation	Automotive In-Vehicle	Service Provider	Aerospace Onboard
[802.1BA/Revision]	[802.1CM/de]	[IEC/IEEE 60802]	[P802.1DG]	[P802.1DF]	[IEEE P802.1DP / SAE AS6675]

- **TSN Components (TSN toolset):**
  - **Time Synchronization**
  - **Bounded Low Latency**
  - **High Availability / Ultra reliability**
  - **Resource Management & API**



Path Selection, Reservation, and Fault Tolerance

Scheduling and Traffic Shaping

Resource Management

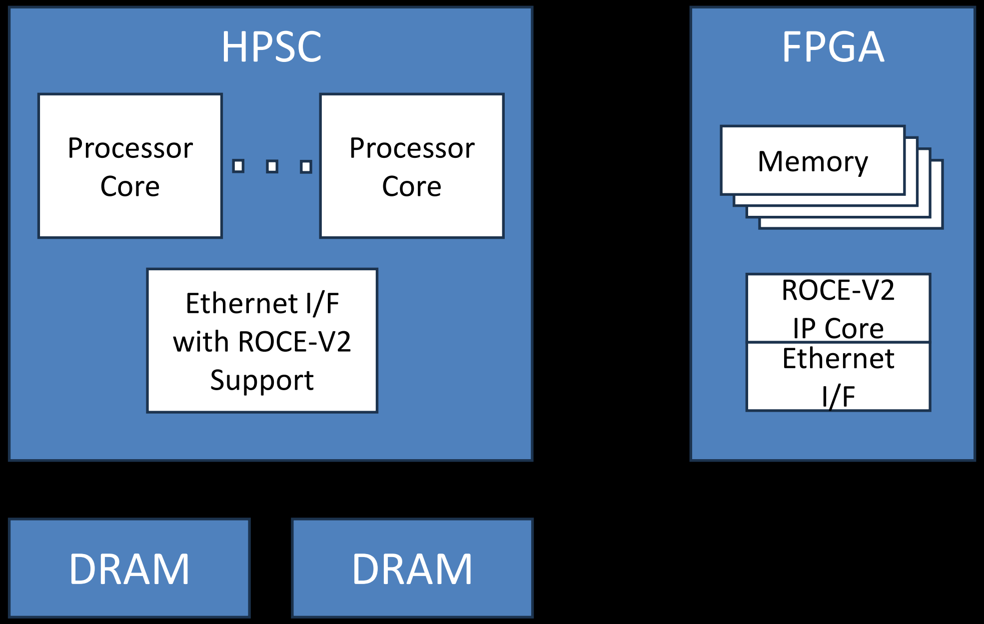
Timing & Synchronization

TSN 802.x spec Categories

RDMA Over Converged Ethernet (ROCE)

ROCE is a network protocol to allow remote direct memory access (RDMA) over ethernet

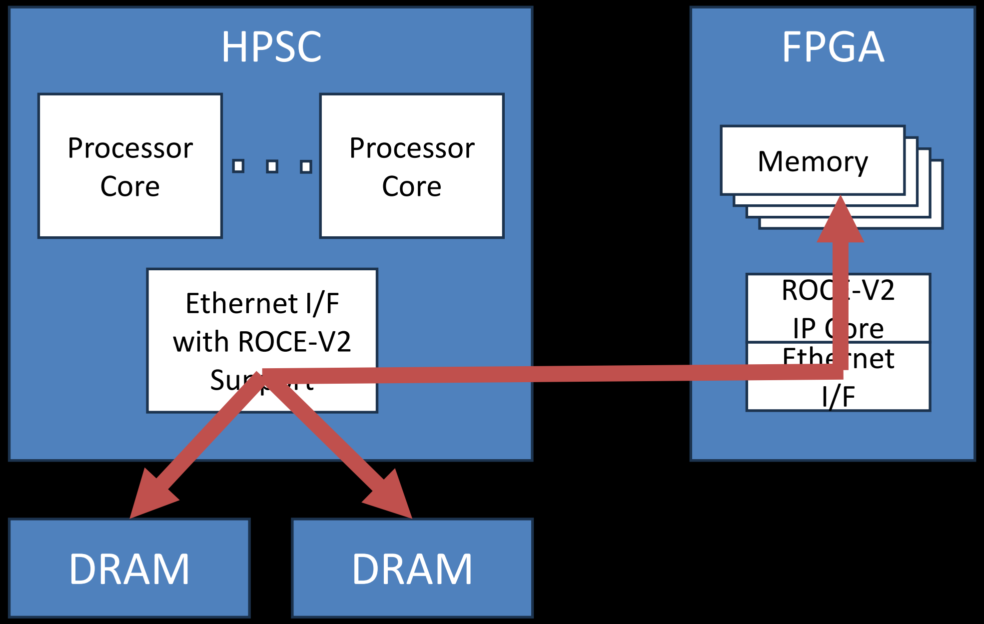
Within HPSC-based avionics, this can allow access to memory in FPGAs or other ROCE-enabled computing devices without intervention on HPSC processing cores.



RDMA Over Converged Ethernet (ROCE)

ROCE is a network protocol to allow remote direct memory access (RDMA) over ethernet

Within HPSC-based avionics, this can allow access to memory in FPGAs or other ROCE-enabled computing devices without intervention on HPSC processing cores.



Fault Tolerance - A Layered Approach

Application Software
- **Layer 6** – SW Application Layer Fault Tolerance (optional per use-case)

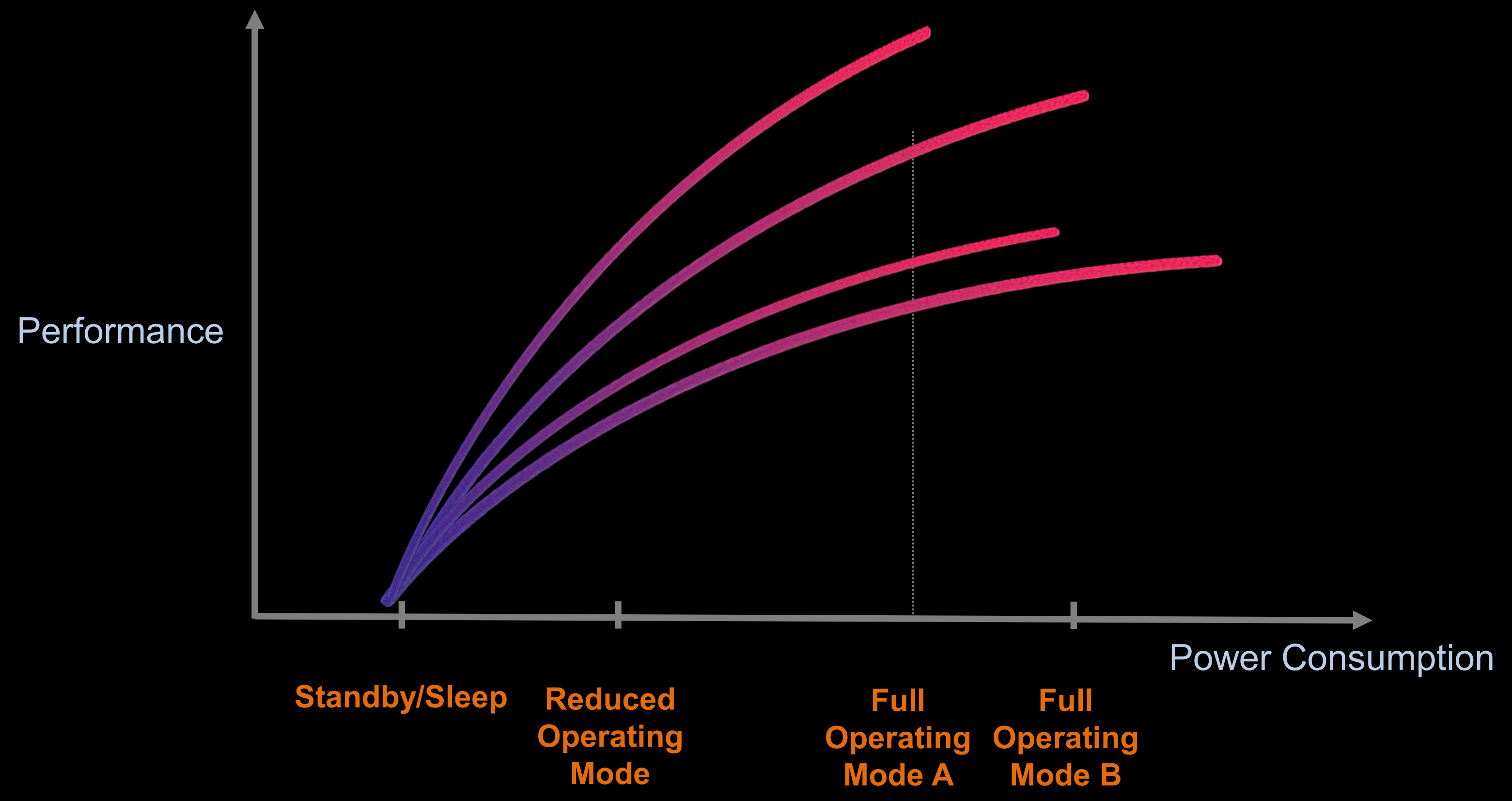
Middleware
- **Layer 5** – SW Managed FT, Health Monitoring of HW, SW mods to HW QoS

OS Software
- **Layer 4** – FT hooks for middleware to utilize

SoC Hardware
- **Layer 3** – HW-based Fault Tolerance
- **Layer 2** – HW Fault Detection Boundaries/Containment Regions
- **Layer 1** – At-site Error Detection/Correction (parity checking, ECC)
- **Layer 0** – Process Technology & SEE Hardened Cells

HPSC Scalability - Small to Large

Power, Performance, Fault Tolerance and other Functions: Scalable via Software Control

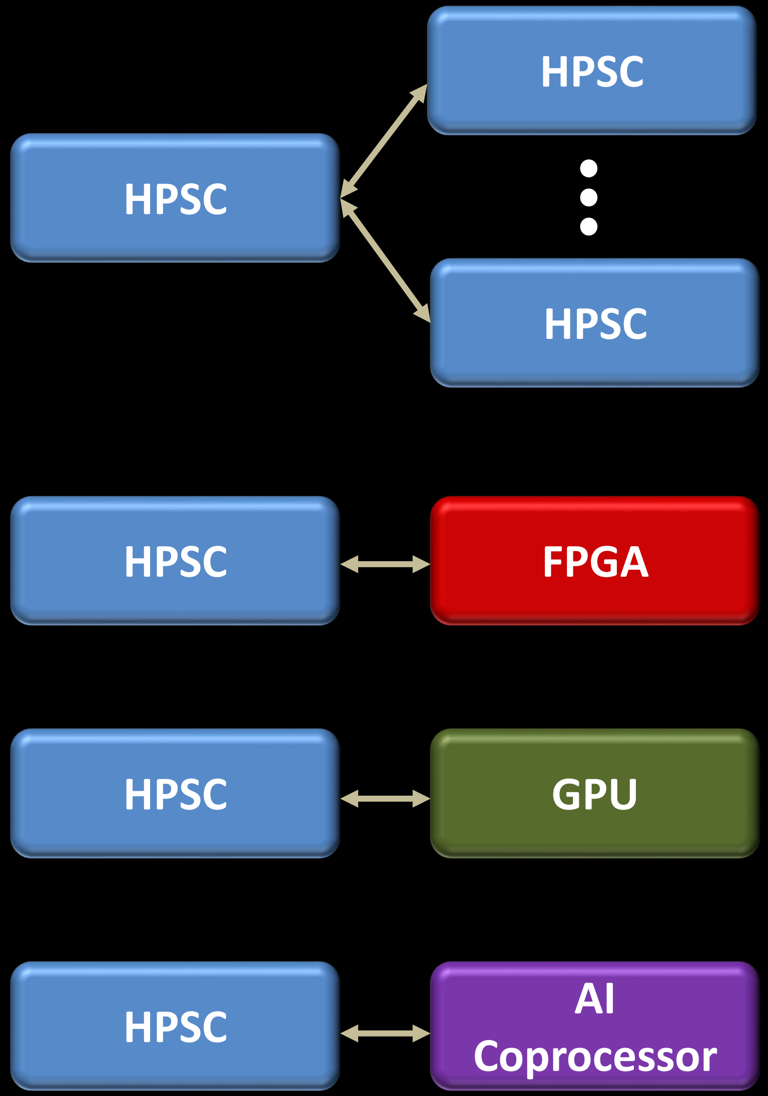


HPSC Performance & Power are Dynamically Tunable based on Mission Needs

HPSC Expandability and Extensibility

HPSC embraces mission customizable extensibility

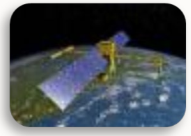
- Extend for
  - Performance
  - Increased performance/watt
  - Interface Bridging
  - Mission specific functionality
  - Fault Tolerance



Supporting Open Source & Commercial Software

Extensive Development Tools, Libraries and Operating Systems for PIC64-HPSC Series

Applications

Satellites


Spacecraft


Rovers/Landers


Aviation


Defense


Industrial


Middleware

System Libraries
OpenSBI
OpenAMP
OpenMP
OpenSSL Cryptography and SSL/TLS Toolkit

Performance Libraries
FFTW
POCL
OpenBLAS × OpenBLAS

AI Frameworks
PyTorch
TensorFlow
TensorFlow Lite

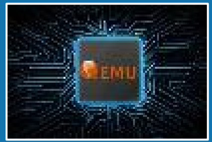
Operating Systems

Linux
Operating System, BSP and Drivers

Real-Time Operating System(s)
RTEMS
WNDRVR
SYSGO EMBEDDING INNOVATIONS
Green Hills SOFTWARE

Hypervisors
Xen Project
KVM

Design Resources

Simulation Models


Velocity Switch S/W


Drivers


System Controller


Configuration Tool


Crypto Tool


Tools

Compilers
LLVM COMPILER INFRASTRUCTURE
OpenXLA IREE
GCC

Development Tools
MPLAB EXT
LAUTERBACH DEVELOPMENT TOOLS
ENTRUST SECURING A WORLD IN MOTION

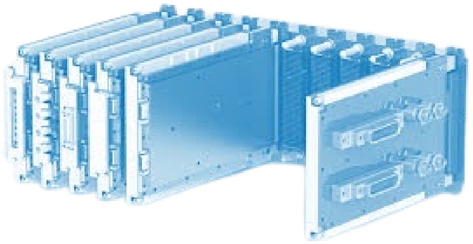
To be presented at the Core Flight Executive / Core Flight Software (cFE/cFS) Symposium, Greenbelt, MD, January 29, 2025

HPSC Ecosystem - Hardware

Interoperable, Industry Standard Hardware to Reduce Mission Risk, Lower Costs, and Improve Development Efficiency

Open/Interoperable

SPACEVPX™



DOD already successfully uses this procurement model terrestrially. Currently working to establish it for space.

Build vs. Buy

NASA

U.S. Department of Defense

esa

NASA can buy SpaceVPX SBCs and build custom boards when necessary.

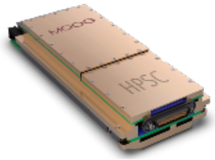
Single Board Computer and Module Partners

Partners

MOOG

ibeos

IDEAS



HPSC Partners developing flight-capable Single Board Computers in various form factors (SpaceVPX 3U/6U, VNX+).

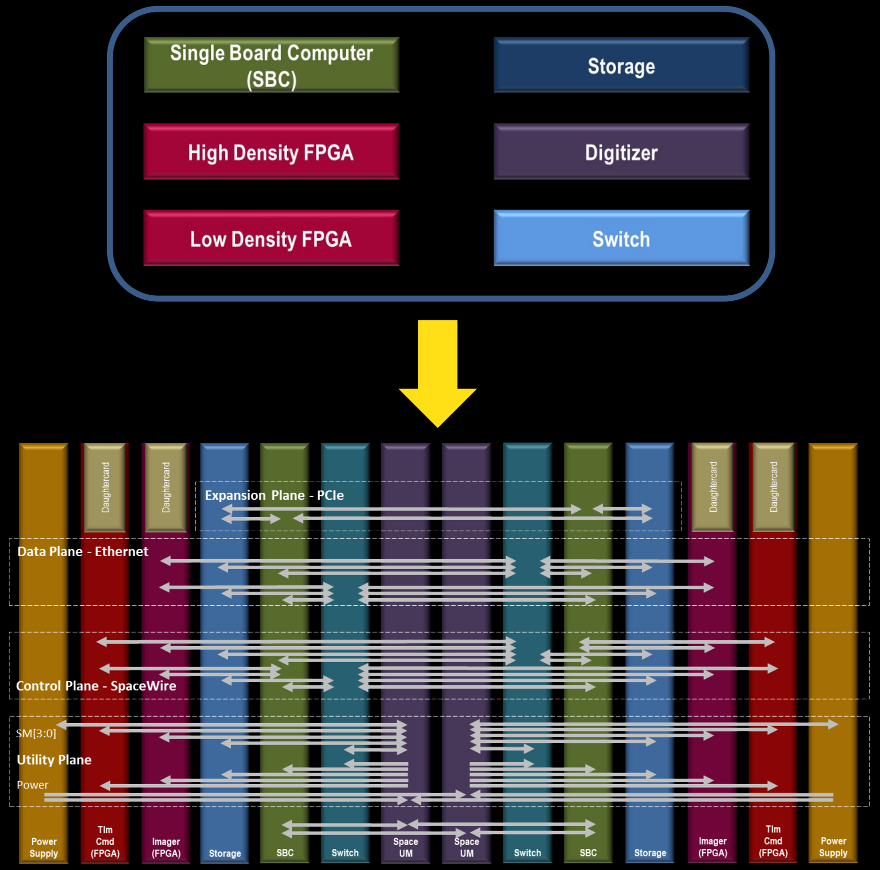
“Buy what we can … build what we must”

SOSA™ SpaceVPX Standardization

- NASA is collaborating with industry and other agencies on the development of an interoperable variant of SpaceVPX (currently specified in the VITA-78 standard) within the Sensor Open System Architecture (SOSA™) standards organization

- Once completed, an interoperable SOSA™ SpaceVPX standard can guide SpaceVPX development within NASA and industry to ensure interoperable avionics for future NASA missions
  - Provides a scalable architecture with the high-bandwidth inter-module communication and inherent fault tolerance to meet the increased onboard computing demands of future missions
  - System integrators can configure systems consisting of SpaceVPX modules from multiple vendors
  - SpaceVPX module vendors can leverage broader markets for their products, which can reduce per unit cost
  - Interoperability provides a key step toward interchangeability that would be needed for common sparing for future crewed missions

- Interoperable SpaceVPX will form the backbone of the HPSC (High Performance Spaceflight Computing) avionics ecosystem



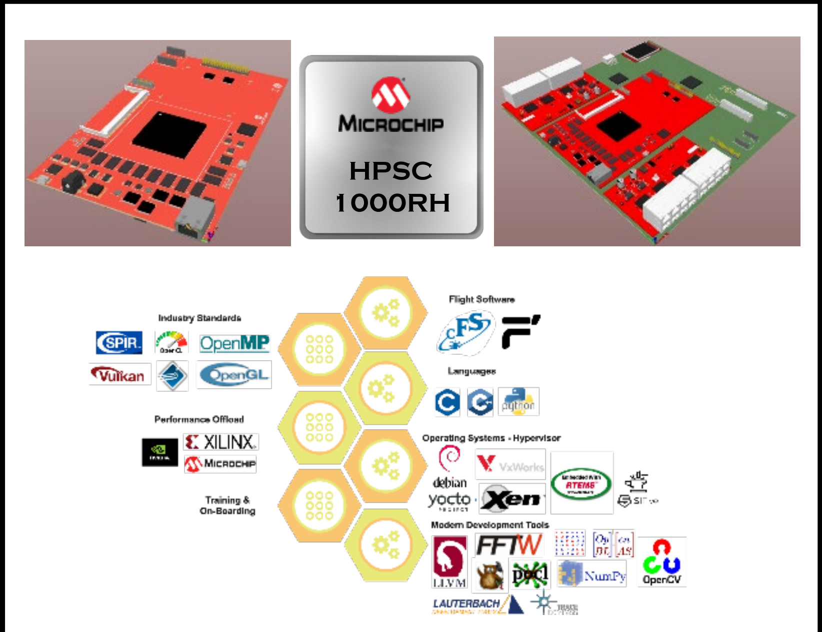
Redundant 3U System

HPSC Roadmap

HPSC Program

(Program of record – Fully Funded)
Completes CY2025

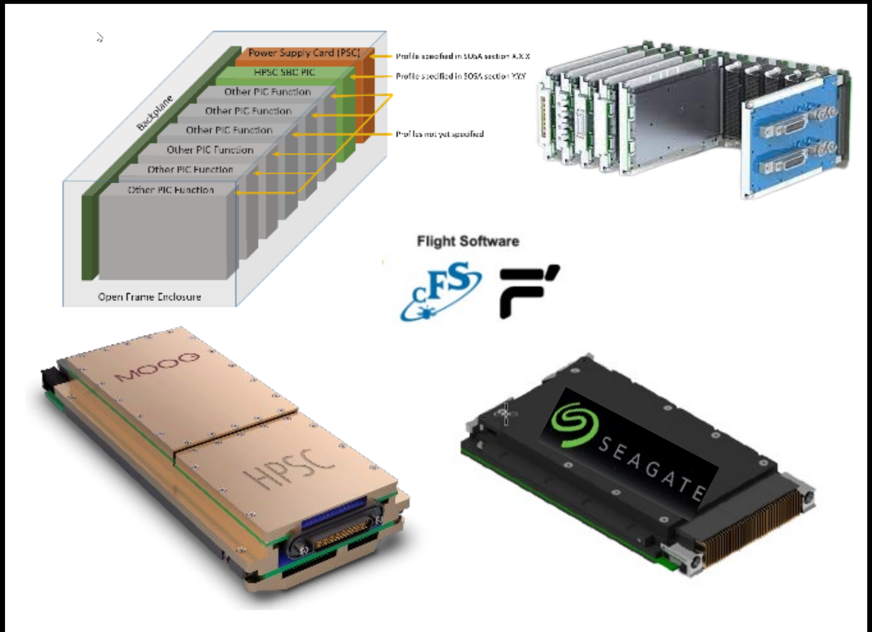
- Space qualified chips
- Evaluation/Development Boards (out of form factor)
- OS, drivers, libraries
- Microchip: Training, documentation, support
- Microchip: Goto Market



HPSC Test Kit

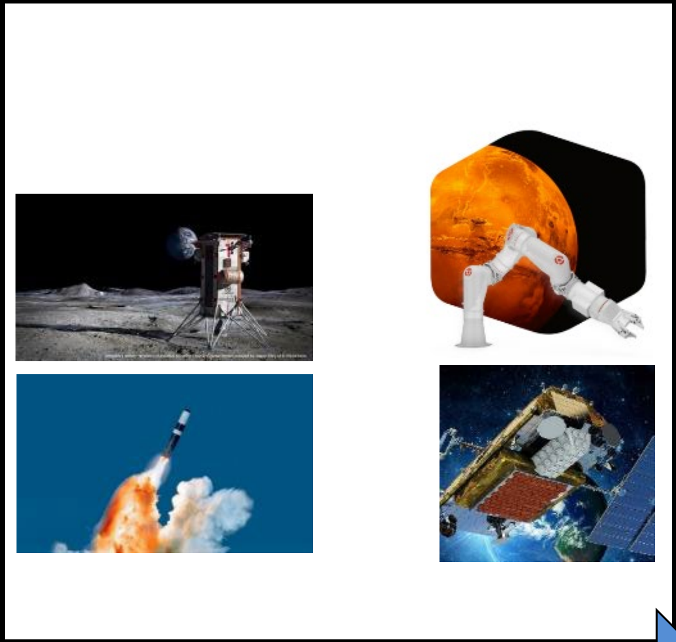
(In Process w/NASA – Needs Funding)
CY2025-2026

- SpaceVPX S3C form factor
- SBC, PSC, SSD, other PICS
- Flight Software Frameworks
- Board Support Package
- Components have Path to Flight Certification
- GSE
- First push signal to industry. In-form factor “real” systems



HPSC/SpaceVPX Mission Infusion, Tech Demo

POTENTIALS:
- Mass Spec
- Lunar Comm Relay
- SPLICE
- Aerocapture
- Orion upgrade
- Gateway
- Others



HPSC is On-Track to Deliver

- **Partners Engaging:** Investing in Eco-System. SBCs, Memory Modules, Software, Systems
- Significant "**HPSC Early Adopters**" are committing to HPSC
- NASA is investing $80M in HPSC
- Microchip is making strategic investments in HPSC

Some Software Considerations for HPSC

- HPSC is has unprecedented processing performance and flexibility
  - Flight software architectures such as cFE/cFS must be adapted to leverage these capabilities (i.e. how to deploy AI/ML applications?)
  - With flexibility comes complexity, which flight software architectures must manage (i.e. power domains, fault tolerance modes, etc.)
  - The partitioning that HPSC provides may simplify integration of software deliverables from different organizations, and could even allow unused resources to demonstrate new algorithms on orbit
- The SOSA SpaceVPX architecture has required functions that will require software
  - Chassis Manager software is needed to control SpaceVPX chassis
  - IPMC (Intelligent Platform Management Interface Controller) software is needed for local control of each SpaceVPX Plug-In-Card
  - Make vs. Buy
- How does cFE/cFS on HPSC interface and interact with other architectures
  - F’
  - SpaceROS

In Summary

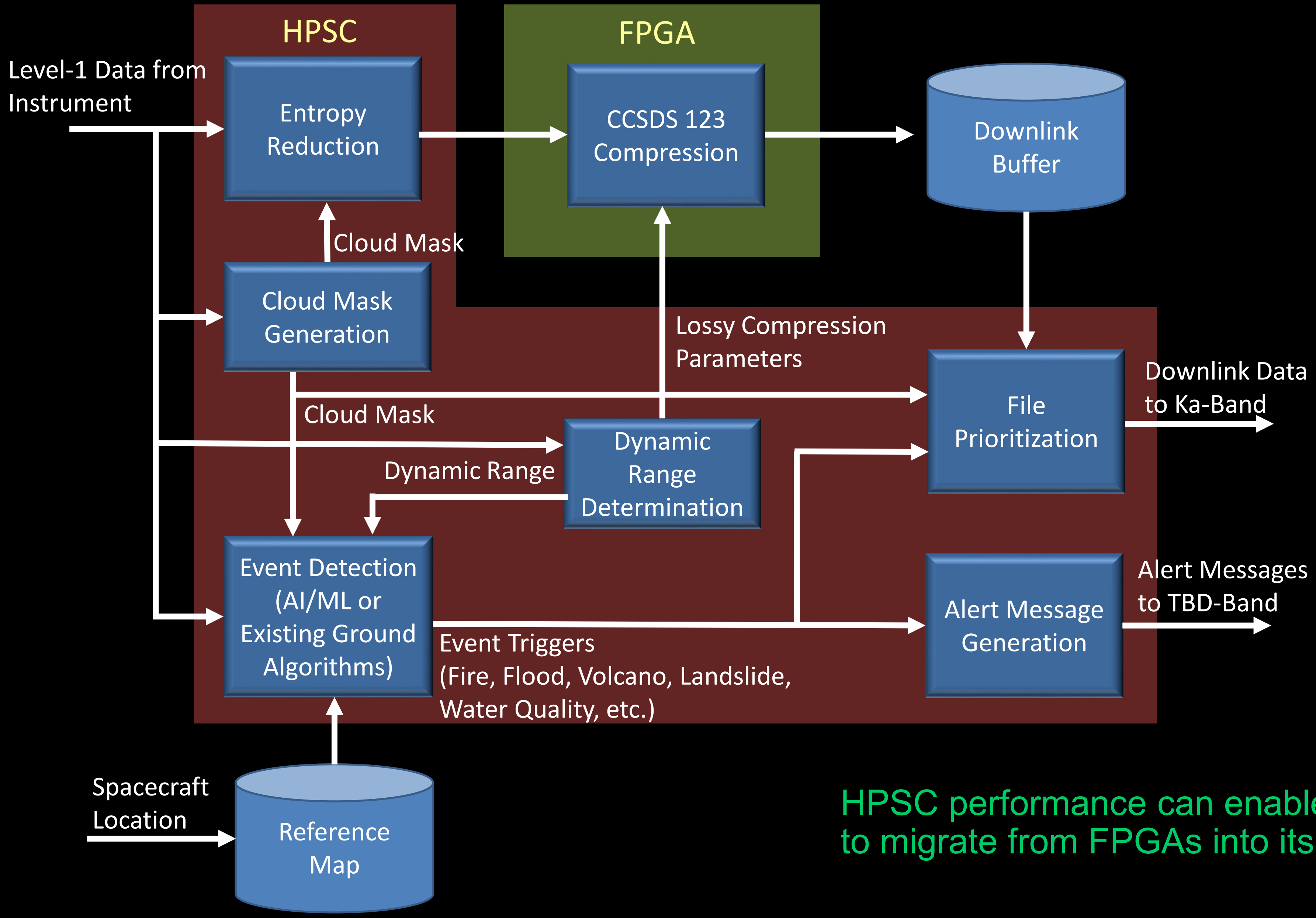
- HPSC provides significant advancement in onboard flight computing for our future missions
- Beyond NASA, HPSC can also provide a compelling fault-tolerant computing solution for Mil-Aerospace, Government, and Commercial Industry
- HPSC is coming soon, with evaluation boards expected in Q2 2025
- Work with industry in underway to develop an interoperable avionics standard, and HPSC products have already been announced that will comply with this standard
- We look forward to working with the flight software community as they adapt cFE/cFS to leverage the capabilities of HPSC

Acronym List

AI	Artificial Intelligence	GPU	Graphics Processing Unit	PIC	Plug-In Card
API	Application Programming Interface	IEEE	Institute of Electrical and Electronics Engineers	QoS	Quality of Service
ARMADAS	Automated Reconfigurable Mission Adaptive Digital Assembly Systems	HPSC	High Performance Spaceflight Computing	ROCE	Remote Direct Memory Access Over Converged Ethernet
ASIC	Application Specific Integrated Circuit	HW	Hardware	ROS	Robot Operating System
cFE/cFS	Core Flight Executive/Core Flight Software	I/O	Intput/Output	RPOC	Rendezvous, Proximity Operations & Capture
C&DH	Command and Data Handling	IP	Intellectual Property	RTOS	Real Time Operating System
CXL	Compute Express Link	IPMI	Intelligent Platform Management Interface	SBC	Single Board Computer
DDR	Double Data Rate	IPMC	IPMI Controller	SEE	Single Event Effect
DTN	Delay Tolerant Networking	ISAAC	Integrated System for Autonomous and Adaptive Caretaking	S3C	SOSA Space Subcommittee
ECC	Error Correction Code	ISRU	In Situ Resource Utilization	SOC	System-On-a-Chip
ELCSS	Environmental Control and Life Support System	JPL	Jet Propulsion Laboratory	SOSA	Sensor Open Systems Architecture
ESA	European Space Agency	ML	Machine Learning	SSD	Solid State Drive
FPGA	Field Programmable Gate Array	NASA	National Aeronautics and Space Administration	STMD	Space Technology Mission Directorate
FT	Fault Tolerance	OS	Operating System	SW	Software
Gbps	Gigabits Per Second	PCIe	Peripheral Component Interconnect Express	TSN	Time-Sensitive Networking

Back Up

Notional Earth Science Processing Flow



HPSC performance can enable processing to migrate from FPGAs into its processors

Notional Earth Sensing Software Architecture

- C&DH Application
- Instrument Management and Control Application
- Event Detection Management and Message Generation Application
- Cloud Mask Generation
- Dynamic Range Determination
- Entropy Reduction
- Event Detection Applications (varying by spacecraft location)
  - Fire
  - Flood
  - Volcano
  - Landslide
  - Water Quality
- Resources for new algorithm demonstration (i.e. a sandbox)