

Solid State Drive Radiation Assurance With Active Testing

Edward P. Wilcox, *Member, IEEE*, Adia M. Wood, Gregory R. Allen, *Member, IEEE*, Martin A. Carls, *Member, IEEE*, Megan C. Casey, *Member, IEEE*

Abstract—Single-event effects (SEE) and total ionizing dose (TID) data are presented for several automotive- and industrial-grade solid-state drives, and the effects of different active test configurations on hardness assurance are explored.

Index Terms—radiation, assurance, automotive, solid state drive, flash, memory, system, dose

I. INTRODUCTION

AUTOMOTIVE- and industrial-grade memories offer capacities greater than 1 Terabit in assembled PCIe (Peripheral Component Interconnect Express) solid-state drive (SSD) modules [1] as small as 22 mm x 30 mm, with a mass of only a few tens of grams. While not targeted at the aerospace market specifically, let alone a high-radiation space environment, characterization of such devices offers the opportunity for ultra low-cost, small form-factor, or cutting-edge applications with an appropriate risk tolerance [2] to evaluate a wider trade space in the data storage market compared to discrete flash memory piece parts [3].

However, many of these devices are challenging to fully characterize independently as they contain multiple interconnected components behind proprietary controllers and integrated voltage regulators. A radiation evaluation of currently-available memories has been conducted at the assembly level using high-energy heavy-ion beams at the NASA Space Radiation Laboratory (NSRL), 200 MeV protons at the Massachusetts General Hospital's Francis H. Burr Proton Therapy Center (MGH), and 1 MeV gamma rays at the NASA Goddard Space Flight Center's Radiation Effects Facility (GSFC REF).

The initial intent of this work was to survey the radiation response of alternate-grade parts for broad spaceflight use, but new insight into the importance of testing not just in an active condition [4], but through repeated and varied operational states has developed. Details of the development, methodology, and results are presented along with discussion and conclusions drawn from the present results.

This work was directed by the the NASA Electronic Parts and Packaging (NEPP) Program, testing was funded by the Defense Common Parts Testing – Radiation (DeCPTR) Program, and test development was funded in part by the Office of the Undersecretary of Defense's Trusted and Assured Microelectronics Radiation Hardened Microelectronics Technical Execution Area.

Edward P. Wilcox is with NASA Goddard Space Flight Center, Greenbelt, MD 20771 USA (e-mail: ted.wilcox@nasa.gov).

Adia M. Wood, Martin A. Carls, and Megan C. Casey are with NASA Goddard Space Flight Center, Greenbelt, MD 20771 USA (e-mail: adia.m.wood@nasa.gov; martin.a.carls@nasa.gov; megan.c.casey@nasa.gov;).

Gregory R. Allen is with the NASA Jet Propulsion Laboratory, Pasadena, CA 91109 USA.

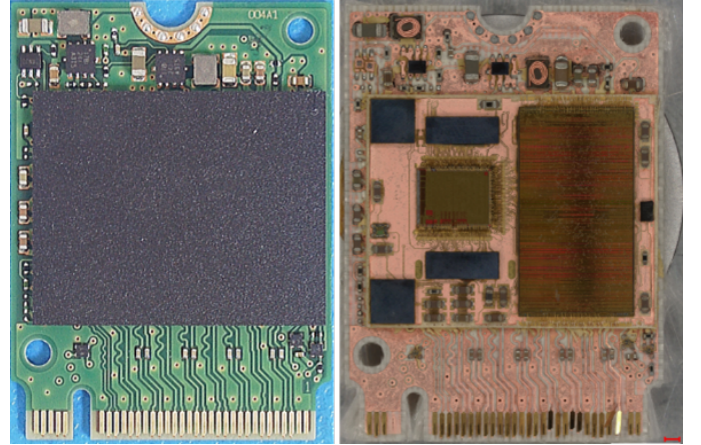


Fig. 1. Micron 256 GB SSD, as-received (left) and after complete decapsulation (right)

II. TESTING DESCRIPTIONS

A. Devices Under Test

The automotive- and industrial-grade SSDs listed in Table I were tested for total ionizing dose (TID) and single-event effects (SEE) response at the assembly level under a variety of operational modes. The NAND flash memories onboard were configured in single-level cell (SLC) or triple-level cell (TLC) by the manufacturer, and in the case of the Micron device, provisioned from TLC to SLC in certain devices before heavy-ion testing. One device contained dynamic random access memory (DRAM) while the other drives are DRAM-less architectures. All are commercially available and not otherwise hardened for a radiation environment, nor were the test samples prepared in any special way.

To gain further insight into the components, several cross-sectional analyses and tear-downs were completed on the Micron 256 GB SSD in the NASA GSFC Parts Analysis Lab. Die-level micrographs indicate markings of “Intel B17A 2016” on the four-die flash memory stack, “SM2263A” on the PCIe controller die, and “TLV733A1P8” on the low-dropout regulator (LDO) as shown in (Fig. 1). Several resistors and capacitors, one possible wafer chip scale package die (illegible markings) and unidentified blocks are also present. Cross-sectional measurements of the flash die stack and the PCIe controller were informative in linear energy transfer (LET) and range calculations necessary for the NSRL heavy ion testing. As a reminder, all devices in this study were irradiated as-received, without decapsulation.

TABLE I
DESCRIPTION OF DEVICES UNDER TEST

	Micron MTFDHBK256TDP -1AT12AIYY	WD SDBPTPZ-085G -XI
Operating Temp (°C)	M.2: -40 to +95 BGA: -40 to +105	-40 to +85
LDC	3BA22 and 3PA22	19JUN2023
Memory Type	256GB TLC, 85GB SLC Micron B17A 64 Layer 3D NAND	85GB SLC 96 Layer 3D NAND
DRAM	No	No
Controller	Silicon Motion SM2263A	WD Proprietary
Footprint	M.2 2230	M.2 2230
	Swissbit SFPC320GM1AG4TO -I-8C-51P-STD	Exascend EXPI4M960GB -DL
Operating Temp (°C)	-40 to +85	-40 to +85
LDC	0423	Unmarked
Memory Type	320 GB pSLC Kioxia 64 Layer 3D NAND	960 GB TLC 96 Layer 3D NAND
DRAM	Micron DDR3 1GB	No
Controller	Phison PS5008-E8-10 PCIe 3.0	Marvell 88SS1321 PCIe 4.0
Footprint	M.2 2280	M.2 2280

Facility configured for 16 MeV/amu tune, in vacuum.

B. Test Setup

The enabling technology for this study is an automated solid-state drive test setup (Fig. 2) designed to test PCIe SSDs [6] at distances up to 30' from a data processing computer, and theoretically unlimited distance to a test conductor via HDMI- and USB-over-CAT6 links. The devices under test were installed in passive PCIe extenders with standard M.2 SSD slots to move supporting components on PCIe-to-USB adapters (e.g., the NVMe-to-USB microcircuits) well clear of beam during proton, high-energy heavy-ion, and total dose testing. The data processing computer can then be at the far end of a USB-C cable, well clear of dose or particle fluence, at the expense of peak data rate. This setup allows active operation of the full device in any type of radiation, rather than relying on static bias configurations, particularly in a dose facility. Additionally, the gold fingers for 3.3 V power on the M.2 connector were removed prior to testing, and an external 3.3 V power supply was connected between the host PC's USB link and the device-under test to allow independent monitoring and control of the power supply.

Test automation from the PC (via National Instrument USB digital I/O module) controls a Keysight N6702C power supply and interfaces with external beam inhibit inputs (e.g., at MGH and NSRL) to accurately halt beam, recover functionality, and resume beam when ready. With this setup functioning, repetitive fluence-between-failure system-level tests of the SSDs are possible, providing meaningful levels of statistical data [5]. By correlating accurate power supply timestamped data with facility and data logs, results such as Fig. 3 were generated showing multiple radiation events. As observed by supply current, eight separate events occurred in Fig. 3, all of which recovered with a forced power cycle. In each case, the device completed entire read and write cycles between events.

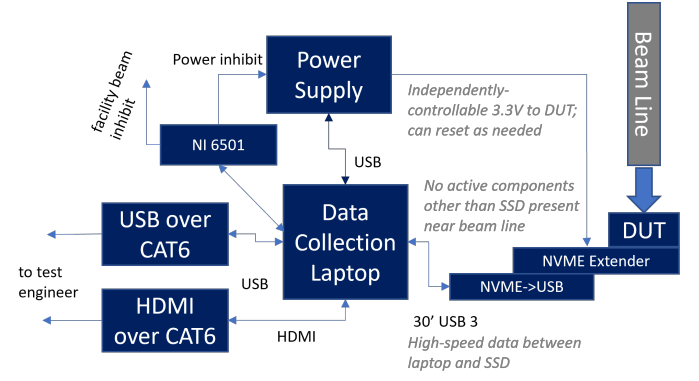


Fig. 2. TID/SEE test setup

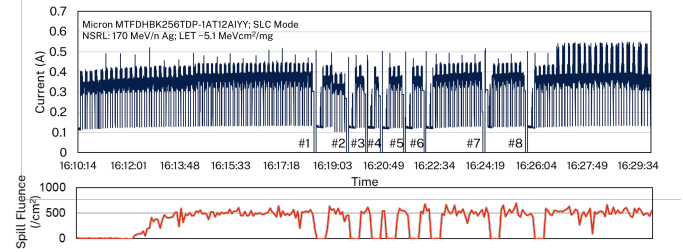


Fig. 3. Power supply current (top) and beam spill fluence (bottom) for an active read/write irradiation at NSRL.

The lower portion denotes NSRL-delivered beam spills, with a typical fluence of 500/cm².

The SEE and TID test flows are depicted in Fig. 4 and Fig. 5. In each case, test data was 1,024 (SEE) or 4,096 (TID) random locations each written with 1,024 kB of pseudorandom data. Data was uniquely marked to indicate any addressing errors that might occur due to upsets in control registers. On each operational loop, the random locations were changed to avoid over-testing any portion of the memory, ensure that readbacks were not merely reading back the data written several cycles previous, and to minimize the effects of system-level caching.

The SEE flow was unmodified during testing. The TID test flow, as discussed later, did not originally contain the left-hand portion with the power supply cycling. Fig. 5 represents the final version settled-upon during test execution.

C. Test Facilities

Testing was conducted with 200 MeV protons at the Massachusetts General Hospital's (MGH) Francis H. Burr Proton Therapy Center in January 2024, with gamma rays at the Goddard Space Flight Center's Radiation Effects Facility (GSFC REF) in April 2024, and with high-energy heavy ions at the Brookhaven National Laboratory's NASA Space Radiation Lab (NSRL) in June 2024.

Testing at all facilities shared the common test setup, including all cabling and hardware. At MGH and NSRL, the test setup actively inhibited beam delivery. At GSFC, the gamma irradiation was continuous due to practical facility constraints and the relatively low amount of dose received

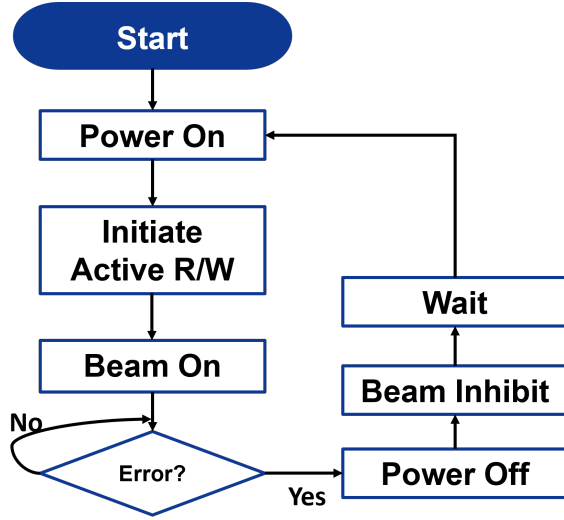


Fig. 4. SEE test flow

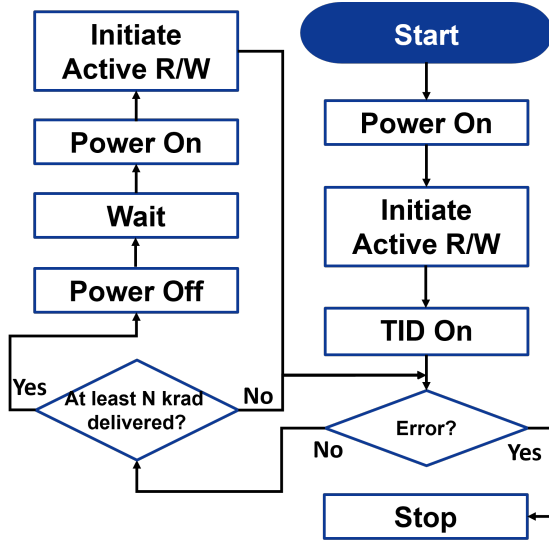


Fig. 5. TID test flow

during the few seconds of power cycling. Devices were fully encapsulated (i.e., not delidded) when tested. A single device (Fig. 1) was cross-sectioned to properly develop the material stackup to determine linear energy transfer (LET) and range when testing with heavy ions as NSRL. The selected ions at NSRL are listed in Table II for the PCIe controller in the Micron device, then in Table III for the four-die flash array.

TABLE II
BEAM LIST FOR HEAVY ION IRRADIATION OF MICRON SSD PCIe CONTROLLER

Ion Species	Energy (MeV/n)	LET (MeV·cm ² /mg)	Residual Range in Si (mm)
Fe	190	2.5	10.27
Ag	170	9.1	4.73
Ag	460	5.1	26.29
Bi	380	17.3	12.57

TABLE III
BEAM LIST FOR HEAVY ION IRRADIATION OF MICRON SSD NAND FLASH FOUR-DIE STACK

Ion Species	Energy (MeV/n)	LET (MeV·cm ² /mg)	Residual Range in Si (mm)
Fe	190	2.50-2.53	10.32
Ag	170	8.93-9.14	4.79
Ag	460	5.10-5.12	26.34
Bi	380	17.23-17.36	12.62

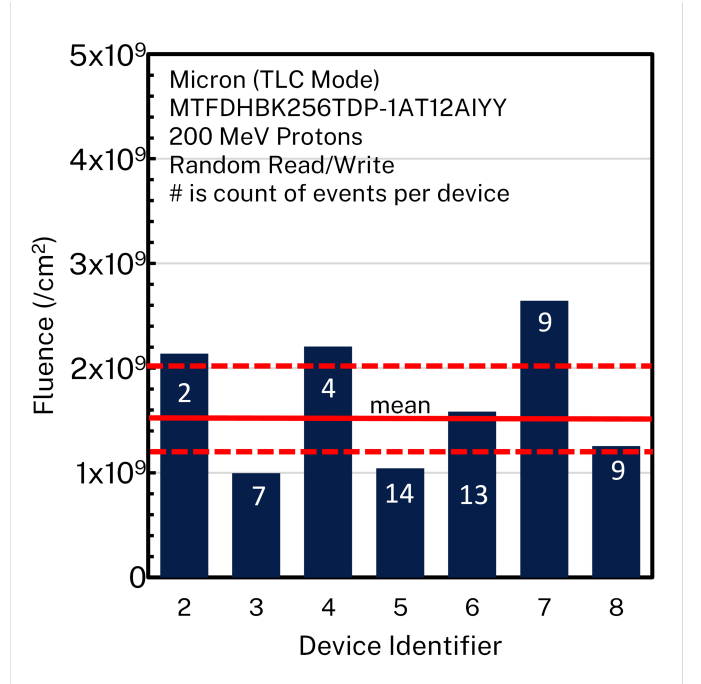


Fig. 6. Mean fluence between failure for the Micron automotive-grade SSDs with 200 MeV proton testing, including both recoverable and unrecoverable error modes. Mean and 95% confidence lines are shown.

III. TEST RESULTS

A. High-Energy Proton Results

The Micron SSD (in default TLC mode only) and Western Digital SSD (SLC) described in Table I were irradiated dynamically while under 200 MeV proton irradiation at MGH. Both device types suffered failure events that manifested as a timeout during a read or write event under active irradiation. When the device could be recovered with the automatic power cycle, the event was classified as a recoverable failure. When the device could not be restored with a power cycle, manual intervention was attempted. If all attempts failed, the event was classified as an unrecoverable failure. Both types of events occurred during both read and write operations (read and write block sizes were purposely large enough to ensure that the failed operation was readily traceable to a specific command). Mean fluence between failure (MFBF) data including both recoverable and unrecoverable events together are in Fig. 6 and Fig. 7.

While the MFBF appear quite different between the two, the fluences to unrecoverable failure are similar – about $2.22 \times 10^{10}/\text{cm}^2$ for the Micron and $1.43 \times 10^{10}/\text{cm}^2$ for the Western Digital. The Western Digital device required interven-

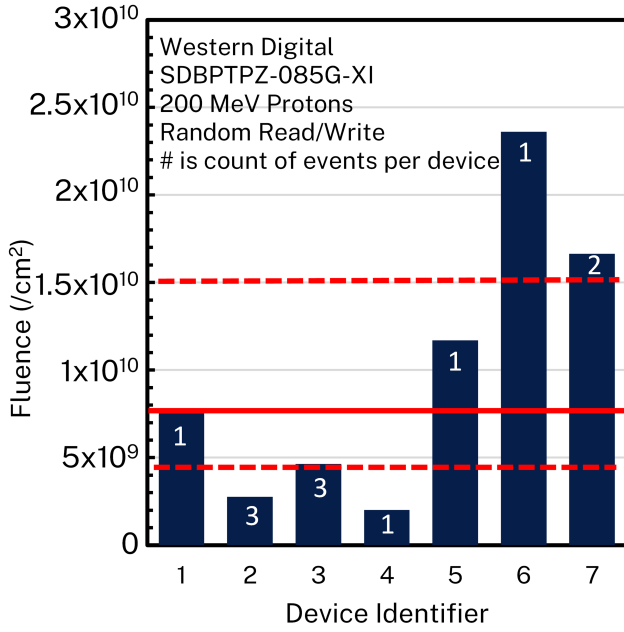


Fig. 7. Mean fluence between failure for the Western Digital industrial-grade SSDs with 200 MeV proton testing, including both recoverable and unrecoverable error modes. Mean and 95% confidence lines are shown.

tion less often than the Micron device, but neither is immune to proton-induced functional failure.

To further explore the mechanism, irradiations in an unbiased configuration ($4.28 \times 10^{10}/\text{cm}^2$ for each device) were performed, and did not cause any observable failures. Devices irradiated unbiased were fully functional upon power up after the irradiation, even though NAND flash arrays themselves are equally susceptible to bit cell upsets in this condition [14], [16].

B. Total Ionizing Dose Results

Total ionizing dose testing was then performed with gamma irradiation at the NASA GSFC Radiation Effects Facility. The same test setup proven during proton SEE testing enabled full board-level irradiations with in-situ dynamic reading and writing by keeping the active test circuitry safely away from significant dose rates. The intent as-planned was to ensure that all internal components were exercised and powered (e.g., high-voltage charge pump transistors [3], [7] known to be a weak link of modern NAND) and to monitor continuously for indications of failure. The first random read/write TID test of a Swissbit industrial-grade SLC SSD (Fig. 8, top) suggested a TID tolerance of approximately 55 krad(Si) for a sample size of 1. This was result is in-line with failure points of modern NAND flash [3], [7], [16], and suggested that the flash might be the weak link in the design.

The next irradiation of another Swissbit sample was halted at 30 krad(Si) to perform a thorough device characterization in a higher-speed test fixture as a further verification that the device was unaffected at this dose level, and no signs of

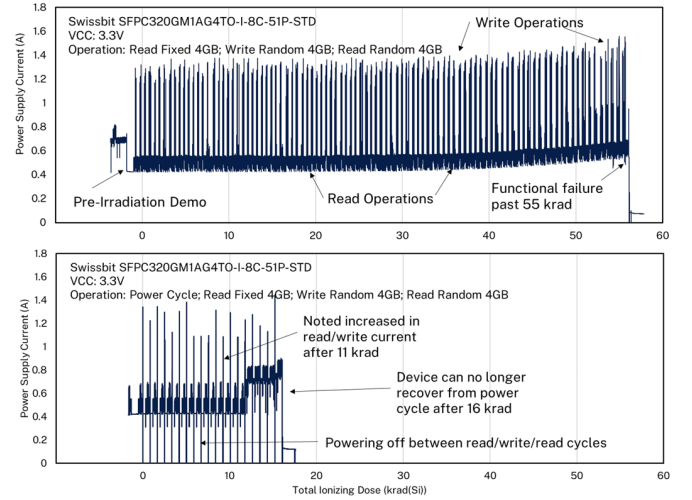


Fig. 8. TID tolerance as measured by supply current for the Swissbit SSD with continuous read/write (top) and the addition of power cycling (bot).

degradation had yet been observed. However, the device could not be powered-on after removing it from the in-situ test setup.

Recognizing a critical oversight in test design, the TID test was immediately modified (sequence in Fig. 5) to periodically test for bootability rather than only checking for bootability in the event of a failure recovery attempt. The next Swissbit device failed this in-situ bootability test after only 16 krad(Si) (Fig. 8, bot).

The Exascend PI4 TLC industrial SSD failed (Fig. 9) at 23 krad(Si) when dynamically read/written in-situ, and at only 7 krad(Si) when power cycling was included (and 17 krad(Si) for a “cold spare” test in which the irradiations were performed completely unbiased). As with the proton SEE testing previously, TID-induced bit cell upsets should be mostly bias-independent. That the cold spare test lasted longer than the in-situ power cycling test may indicate that bit cell upsets do not play a role in this failure mechanism.

Micron automotive-grade SSD test data are presented in Fig. 10 and Fig. 11. The Micron data shows a lesser issue with power-on failures than the previous two devices, with performance relatively unchanged to 20 krad(Si), albeit with much lower than expected write speeds starting immediately with irradiation. As of publication, this device has not yet been tested in the SLC configuration for TID for comparison.

The Western Digital device was limited to a single device tested in the no-power cycling mode. As in Fig. 12, this device failed operationally around 25 krad(Si), though an unexplained increase in write-mode current appeared after 10 krad(Si).

C. Heavy-Ion Results

In June 2024, the Micron, Western Digital, Swissbit, and Exascend drives were all tested with high-energy heavy ions at the NASA Space Radiation Lab (NSRL). The two physically-smaller devices (Micron and Western Digital M.2 2230 SSDs) were irradiated with the entire device in the beam at all times. The Micron device’s cross-sectional analysis was used to estimate LET and range, as previously listed in Table II for

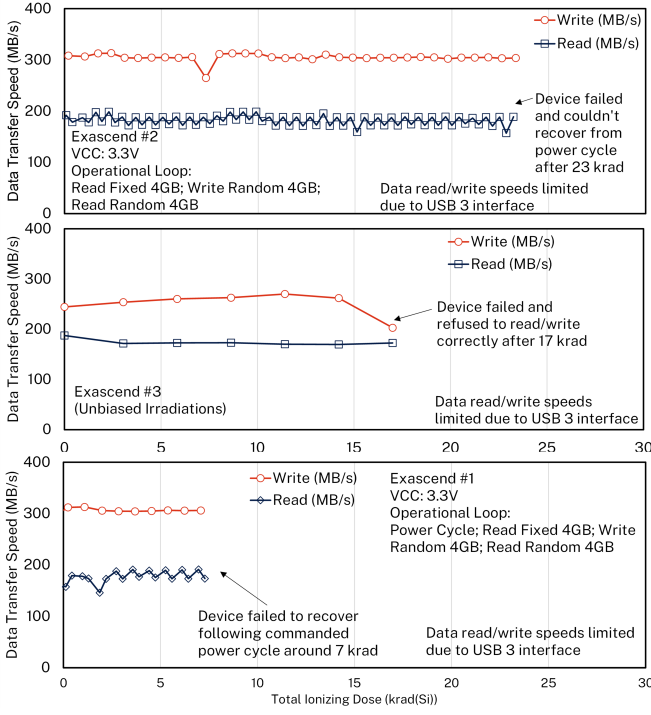


Fig. 9. TID tolerance as measured by read/write speed for the Exascend SSD with continuous read/write (top), cold spare (mid), and the addition of power cycling (bot).

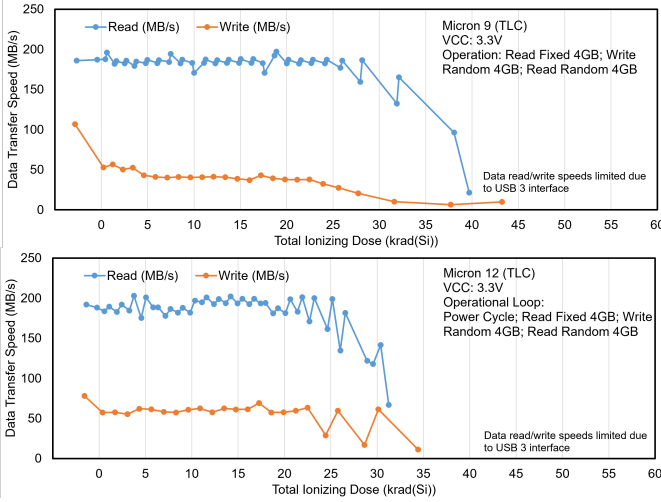


Fig. 10. TID tolerance as measured by read/write speed for the Micron SSD with in-situ power cycling (top) and continuous read/write (bot).

the wire-bonded PCIe controller and Table III for the multi-die flash memory stack. The two physically-larger devices (Swissbit and Exascend are M.2 2280 devices) were irradiated both in the full-board configuration and by shielding half the device. The partially-shielded tests attempted to differentiate the susceptibilities of the NAND flash devices themselves (for correlation with existing piece-part test data) and the susceptibilities of the controllers, DRAM (Swissbit only), and surrounding peripherals (e.g., power-management).

All four devices were susceptible to unrecoverable errors at LET of $17.3 \text{ MeV} \cdot \text{cm}^2/\text{mg}$ and below.

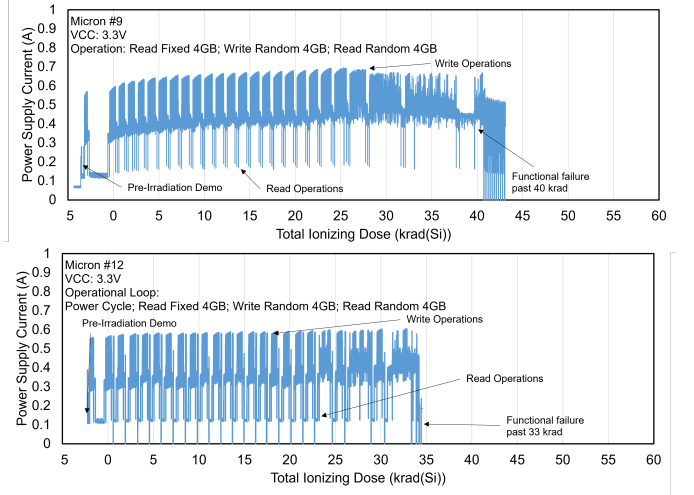


Fig. 11. TID tolerance as measured by power supply current for the Micron SSD with continuous read/write (top) and the addition of power cycling (bot).

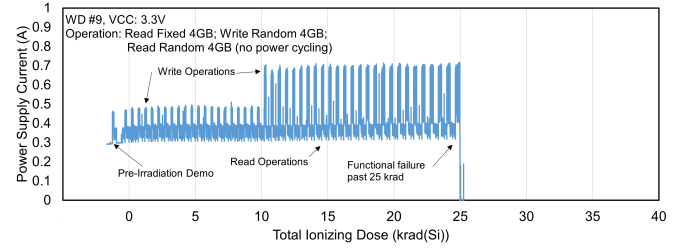


Fig. 12. TID tolerance as measured by read/write speed for the Western Digital SSD with continuous read/write testing only.

A small improvement was observed in the Micron device when its memory array was provisioned into 100% SLC storage (Fig. 13). The Western Digital device (natively SLC) performed better than the Micron device, with fluence-between-failure up to an order of magnitude higher at an LET of $5.1 \text{ MeV} \cdot \text{cm}^2/\text{mg}$.

For the two devices where the flash could be separately irradiated from the controllers, the Exascend's TLC flash was significantly more vulnerable (Fig. 14) than the Swissbit's SLC flash, while the Swissbit's controller was the most sensitive region tested – which notably is the only device with DRAM installed. However, these were primarily recoverable events. Unrecoverable errors occurred on all devices, including when irradiating only the NAND flash for both the TLC Exascend drive and the SLC Swissbit drive (i.e., not merely user data corruption observed).

IV. HARDNESS ASSURANCE DISCUSSION

That dynamic testing of a complex system may expose new error signatures is not a novel concept [8], nor is the presence of functional failures in solid-state drives [9]. However, the hardness assurance implications herein address the momentum towards flying off-the-shelf [2] systems, whose original designers had no intention to include radiation tolerance whatsoever, with either reduced radiation hardness assurance efforts or the misguided imposition of legacy piece-part hardness

TABLE IV
UNRECOVERABLE ERRORS WITH HEAVY IONS

Part	Target	Unique Parts Tested	Threshold LET for Unrecoverable	Fluence at Highest Passing LET
Micron (SLC)	Entire Device	6	$9.1 < x < 17.3$	$1 \times 10^5 / \text{cm}^2$
Micron (TLC)	Entire Device	7	$2.5 < x < 5.1$	$9.4 \times 10^4 / \text{cm}^2$
Swissbit	Flash	3	$5.1 < x < 9.1$	$2 \times 10^5 / \text{cm}^2$
Swissbit	Controller/DRAM	2	$x > 17.3$	$6.59 \times 10^3 / \text{cm}^2$
Exascend	Flash	2	$x < 5.1$	N/A
Exascend	Controller	3	$2.5 < x < 5.1$	$4.61 \times 10^4 / \text{cm}^2$
WD	Entire Device	2	$5.1 < x < 9.1$	$8.65 \times 10^5 / \text{cm}^2$

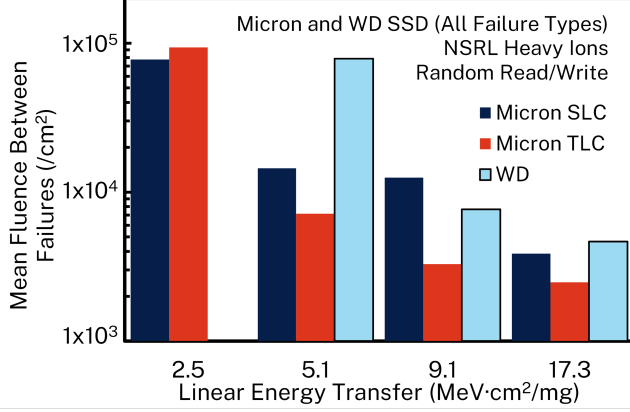


Fig. 13. NSRL mean fluence between failure for Micron and WD SSDs, with the Micron drives provisioned into TLC or SLC for comparison. In both cases, the entire drive is fully exposed to the beam. Untested configurations are blank.

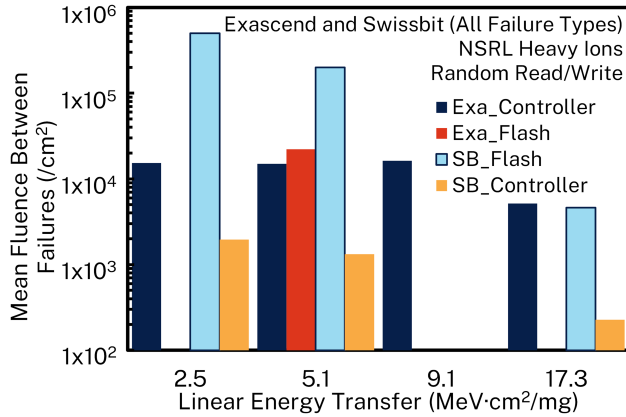


Fig. 14. NSRL mean fluence between failure for Exascend and Swissbit drives, with irradiations focused on either the NAND flash or the controller (and DRAM, for the Swissbit). Untested configurations are blank.

assurance practices. Applying legacy RHA practices without thought to system complexities could result in missing significant mission-ending threats that do not manifest as classic single-event effect phenomena. The clearest example of this would be the SEE failure modes, including fatal errors, readily apparent at very low fluences while actively reading or writing but not when passively irradiated with heavy ions either biased or unbiased.

Furthermore, an SSD tested for TID tolerance in a manner reflective of common flight usage [10], and tested for SEE

only to rule out catastrophic single-event latchup, might lead to a reasonable mitigation plan to power cycle [11] as needed operationally while maintaining a cold spare device. Indeed, such objectives may be mutually exclusive – the devices tested in this work perform best in a dose environment when never turned off, and best in an SEE environment when left off as much as possible.

SSDs contain a relatively small number of active components, but those components present a wide range of radiation failure mechanisms, increasing the challenges of performing accelerated testing in a worst-case condition. For example, NAND flash memories are well-known to be susceptible to charge-pump failures [3], [7] at lower total ionizing dose levels than mainstream highly-scaled CMOS microcircuits, while commercial CMOS devices commonly fail due to single-event latchup [12] under heavy-ion irradiation. It is not unreasonable, then, to hypothesize that an arbitrary solid-state drive might be dose-limited by NAND charge pumps and be SEE-limited by unidentifiable CMOS controllers. The devices tested herein are neither. The SSDs are dose-limited by power-on processes and are SEE-limited by errors in controller, DRAM, and memory circuitry that are neither traditional destructive SEE (e.g., SEL) nor easily-correctable soft errors (these drives feature extensive error-correction [13] that should be sufficient for the errors induced by low fluences of heavy-ions or 200 MeV protons observed in previous testing [14]). Testing passively for SEL would not identify that any of the devices in this study have unrecoverable failure modes at LET values relevant even in the proton-rich environments of low Earth orbit.

It is prudent that the usage of any complex system be predicated upon some knowledge of expected radiation response, and while a trend toward test-as-you-fly on a black-box system may be the only practical solution for many applications (e.g., cost and schedule realities), underlying vulnerabilities in these systems require a particularly careful approach [15] that may not resemble that of piece-part tests (e.g., those in [12]).

The off-the-shelf SSDs tested in this work provide automotive- and industrial-grade temperature ranges and reasonable assurance of manufacturing quality [2]. They may have acceptable TID performance for the lowest of dose environments (or when heavily shielded), and one remedy for the TID hardness assurance concerns is simply to ensure that test-like-you-fly really means a full test case, not merely testing the most common or most concerning application. However, their SEE performance remains troubling from

a testing standpoint, with conflicting worst-case conditions, system-level interruptions that limit total fluence even with an automated test, and piece parts that behave worse irradiated in a system than when tested as parts (e.g., unhandled errors in NAND flash bringing down the entire system when the same parts have no destructive SEE concerns).

Ultimately, complex devices procured off-the-shelf offer little customization, limited error reporting, and potentially no architectural details. Yet, they cannot be reliably screened with a straightforward destructive SEE test when all parts tested in this study failed unrecoverably for reasons likely related more to the architecture rather than a familiar single-event latchup signature.

V. ACKNOWLEDGMENTS

The authors wish to thank their colleagues at NASA GSFC's Radiation Effects and Analysis Group (REAG) for assistance with proton, heavy ion, and total dose testing and data analysis; Exascend for providing samples; and, the staff of the Massachusetts General Hospital's Francis H. Burr Proton Therapy Center (particularly Ethan Cascio) and the NASA Space Radiation Laboratory for their assistance with irradiations.

REFERENCES

- [1] Y. Li, "3D NAND Memory and Its Application in Solid-State Drives: Architecture, Reliability, Flash Management Techniques, and Current Trends," in *IEEE Solid-State Circuits Magazine*, vol. 12, no. 4, pp. 56-65, Fall 2020.
- [2] R. F. Hodson et al., "Recommendations on Use of Commercial-Off-The-Shelf (COTS) Electrical, Electronic, and Electromechanical (EEE) Parts for NASA Missions," December 2020; ntrs.nasa.gov/api/citations/20205011579/downloads/20205011579.pdf.
- [3] S. Gerardin et al., "Radiation Effects in Flash Memories," in *IEEE Transactions on Nuclear Science*, vol. 60, no. 3, pp. 1953-1969, June 2013.
- [4] Boychenko D. et al., "Total ionizing dose effects and radiation testing of complex multifunctional VLSI devices", *Facta Universitatis Series: Electronics and Energetics*, Vol. 28, No. 1, 2015, pp. 153-164.
- [5] N. Mielke et al., "Accelerated Testing of Radiation-Induced Soft Errors in Solid-State Drives," in *IEEE Transactions on Device and Materials Reliability*, vol. 15, no. 4, pp. 552-558, Dec. 2015.
- [6] Ganesh T.S. and B. Tallis, "The Western Digital WD Black 3D NAND SSD Review: EVO Meets Its Match" *Anandtech*. <https://www.anandtech.com/show/12543/the-western-digital-wd-black-3d-nand-ssd-review> (accessed Apr. 22, 2024).
- [7] F. Irom et al., "Evaluation of Mechanisms in TID Degradation and SEE Susceptibility of Single- and Multi-Level High Density NAND Flash Memories," in *IEEE Trans. Nuc. Sci.*, vol. 58, no. 5, pp. 2477-2482, Oct. 2011.
- [8] K. A. LaBel et al., "Radiation Test Challenges for Scaled Commercial Memories," in *IEEE Trans. Nuc. Sci.*, vol. 55, no. 4, pp. 2174-2180, Aug. 2008.
- [9] D. Chen et al., "Heavy Ion Irradiation Test Report for the Samsung 850 PRO Series Solid State Drive," October 2014; ntrs.nasa.gov/api/citations/20205003052/downloads/Chen-14-055_TAMU20141024_SamsungSSD.pdf.
- [10] M. Campola, "Taking SmallSats to The Next Level - Sensible Radiation Requirements and Qualification That Won't Break The Bank," 32nd Annual AIAA/USU Conference on Small Satellites, 2018.
- [11] K. A. LaBel and M. M. Gates, "Single-event-effect mitigation from a system perspective," in *IEEE Transactions on Nuclear Science*, vol. 43, no. 2, pp. 654-660, April 1996.
- [12] G. R. Allen et al., "2017 Compendium of Recent Test Results of Single Event Effects Conducted by the Jet Propulsion Laboratory's Radiation Effects Group," 2017 IEEE Radiation Effects Data Workshop (REDW), New Orleans, LA, USA, 2017, pp. 1-9.
- [13] Y. Cai, S. Ghose, E. F. Haratsch, Y. Luo and O. Mutlu, "Error Characterization, Mitigation, and Recovery in Flash-Memory-Based Solid-State Drives," in *Proceedings of the IEEE*, vol. 105, no. 9, pp. 1666-1704, Sept. 2017.
- [14] M. Bagatin et al., "Single Event Effects in 3-D NAND Flash Memory Cells With Replacement Gate Technology," in *IEEE Trans. Nuc. Sci.*, vol. 70, no. 4, pp. 308-313, April 2023.
- [15] A. de Bibikoff and P. Lamberbourg, "Method for System-Level Testing of COTS Electronic Board Under High-Energy Heavy Ions," in *IEEE Trans. Nuc. Sci.*, vol. 67, no. 10, pp. 2179-2187, Oct. 2020.
- [16] E. P. Wilcox and M. J. Campola, "A TID and SEE characterization of multi-terabit COTS 3D NAND flash," in *Proc. IEEE Radiat. Effects Data Workshop*, Jul. 2019, pp. 238-244.