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A System-Agnostic Process to Design DC Series Arc Fault Detectors

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***Abstract*—Researchers are developing and testing electrified aircraft propulsion (EAP) systems which promise to stimulate new markets and missions, reduce operating costs, and increase efficiency. High-voltage direct current (HVDC) power systems are especially attractive for EAP because high voltages are required to minimize cable mass for desired operating power levels, and DC architectures enable both simpler control schemes and easier integration of sources and loads. On the other hand, electric arcs are more destructive at high powers and more likely to form at high voltages and altitudes. Furthermore, DC arcs formed by an interruption in a single electrical wire (series arcs) can resemble other spurious events such as switching noise. It is crucial both to the aircraft and to passenger safety to detect and isolate this species of arc fault, but doing so poses a non-trivial problem: DC arcs do not have a zero-crossing to facilitate their quenching, and classical overcurrent protection methods fail to detect them. This paper outlines a method of designing series arc fault detection algorithms by collecting arc test data, building a model of the power system, and optimizing arc detector parameters and structures to maximize accuracy and minimize latency as tested against the model. Interpretable machine learning optimization techniques and detectors were employed because they have a more assured and simpler path to aerospace flight certification than black box algorithms. Arcs were generated on a 28 VDC testbench, a circuit model and redundant arc detectors were designed, and one candidate detector solution was implemented in a field-programmable gate array (FPGA) and tested against live arcs.**

Keywords—HVDC, DC series arc fault, electrified aircraft, digital signal processing, FPGA, reliability

I. Introduction

Electric arcs are a significant threat to the safety and public acceptance of aircraft with electrified propulsion systems [1]. DC series arcs pose a particular challenge because they can resemble switching noise or load steps [2]. Overcurrent protection methods cannot detect these species of arc, so the uninterrupted arc's incident energy poses a risk of catastrophic damage to adjacent equipment or even to the entire aircraft [3]. This paper outlines a process to design high-performance DC series arc fault detectors (i.e., detection logic). This process is tailored to the sensing location and power system to which it is applied and is based on groups of human-interpretable physics- or signal-based detection schemes. Maximum 10 ms detection latency was chosen as a performance requirement because it was an order of magnitude less than an estimate of arc duration (90 ms) which caused a 2012 crash of a U.S. Air Force F-22 Raptor [4]. Maximum accuracy was chosen as the other requirement.

Black box type machine learning (ML) algorithms (e.g., random forest classifiers) have been applied to detect DC series arc detection problems in the past [5]. However, it is expected that interpretable ML algorithms will have a more assured and simpler path to aerospace flight certification than black box algorithms because their transparency allows them to be more easily understood and analyzed rather than explained post hoc [6]. Black box detector design processes and black box detector algorithms do not readily permit understanding of potential problems or what could be done to remedy them [7]. Therefore, the interpretability of both detector solutions and detector optimizer were chosen as essential requirements early in this development effort. In addition to human interpretability, the idea of multiple arc detectors was adapted from [8], with the key distinction that each detector would be a signal processing-based or physics-based test providing unique information about the arc signature rather than a piece of a black box machine learning arc detector ensemble.

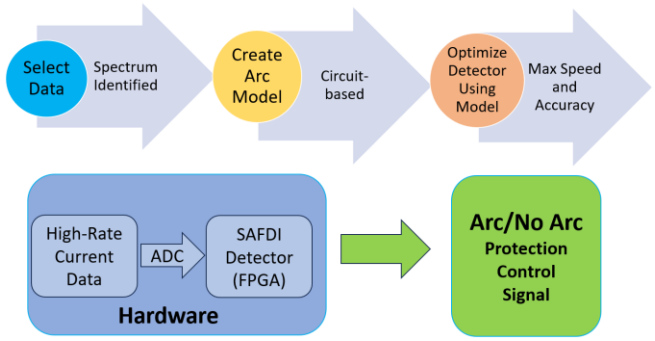

Fig. 1. SAFDI Workflow

Section II describes the System-Agnostic Arc Fault Detection Implementer (SAFDI) process (Fig. 1). Section III describes the 28 VDC SAFDI test bench configuration used to generate arcs and collect data for development and testing of SAFDI. Section IV describes the noisy dynamic model of the 28 VDC power system that was manually created from SAFDI test bench data and used for arc fault detector design. Arc fault detector design, test results, and hardware implementation are discussed in Section V. Finally, Section VI provides conclusions and future work.

II. SAFDI Workflow

The SAFDI workflow to design a human-interpretable DC series arc detector consists of three basic steps: generate arc data, model the arc data, and optimize arc detectors. These steps are broadly outlined here and discussed in III-V.

A. Step 1: Generating Arc Data

The SAFDI process begins with arc characterization data. If the SAFDI process is to be applied to hardware, arcs must be generated in the power system and arc characterization data must be collected. In this work, a 28 VDC test circuit adapted from [15] was built to accomplish Step 1 (see III for details). This circuit represents an avionics power bus and was chosen as a starting point to develop the technology.

B. Step 2: Creating Arc Model

Using the data generated in the previous step, a model must be constructed to match the data (see Section IV for details). In this work, circuit state equations were first developed to match the physical circuit. Then, series arc gap voltage as well as line current noise models were added to the model and tuned to match both arcing and non-arcing test conditions. Once the model's time-domain line current and line current power spectral density (PSD) sufficiently approximated laboratory data, the model could be used in the next step to detect an arc as quickly and accurately as possible.

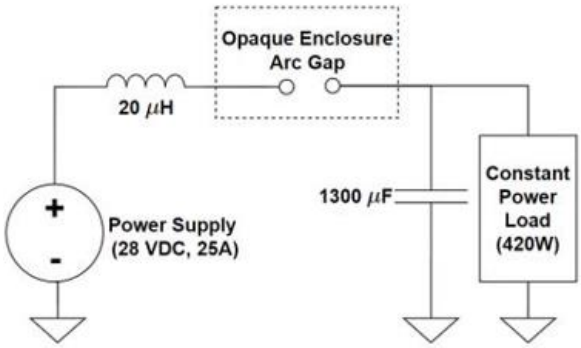

Fig. 2. DC Series Arc Test Circuit

C. Step 3: Optimizing Arc Detector

For the final step, the model must be used to develop optimized arc detection logic. In this work, several digital signal processing (DSP)-based techniques from the literature were implemented in software and optimized for performance as tested with the previously developed model. The detector design problem was cast as an optimization with two objectives: (1) minimize average latency and (2) maximize accuracy as measured over a suite of tests. An evolutionary algorithm optimization tool was used to optimize the detector thresholds for these objectives (see Section V.A).

III. SAFDI Arc Generator Test Bench

The test circuit in this work consisted of a 28 VDC power supply current-limited to 25 A, a 20 μH inductor, a 1300 μF load capacitance, and a DC electronic constant power load (420 W). A diagram of this circuit is given in Fig. 2. An arc generator, composed of two normally connected conductors that can be pulled apart via a linear actuator, was connected in series with the positive cable connecting the supply to the load. This arc generator is run inside of an opaque enclosure to protect test operators' eyesight, and a camera is used to record video of the arc. The arc generator was used to produce DC series arc faults in order to characterize the arc behavior of the test circuit. An inexpensive infrared camera displayed arc gap temperature data in real time and was used for general diagnostics. A phototransistor was set up to observe light from the arc in order to serve as a reference arc detection signal. Detector outputs were compared to this signal to obtain detector latency. The phototransistor signal was also was used to trigger the oscilloscope-based data collection. Fig. 3 shows the layout of the arc test bench.

Two aspects of the test circuit, the large load capacitance and the low DC voltage, made it challenging to sustain series arcs. A large load capacitance tends to quench DC series arcs by driving to 0 J the energy needed to shore up an arc after the line inductance energy has been transferred to the arc following initial electrode separation, as explained by [9] and [10]. Higher DC voltages and currents could overcome this energy limitation imposed by the load capacitance [10].

The arc generator produced arcs by separating its two electrodes to a user-prescribed arc gap length at a user-

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defined speed while the circuit was energized. A stepper motor, ball screw, and linear guide provided precise control over gap length (mm) and electrode separation speed (mm/s). Testing showed that the combination of one sharp graphite electrode and one flat copper electrode was the most repeatable setup for generating arcs. It also revealed that copper-copper electrode configurations did not repeatably produce arcs, likely because copper's high thermal conductivity did not allow the material to heat up sufficiently to produce sustained arcs. For these reasons, the flat copper, sharp graphite electrode setup was used in this work, despite the fact that in terms of materials, a copper-copper electrode

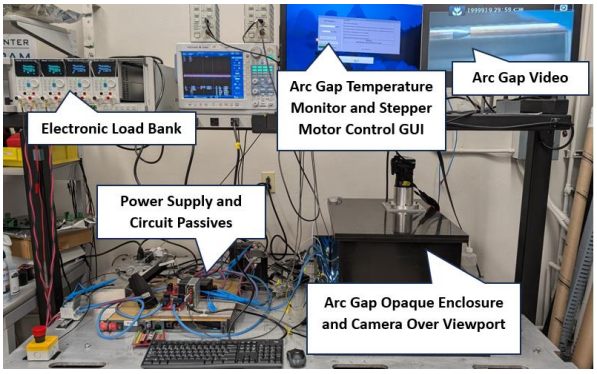

Fig. 3. Arc Fault Test Bench

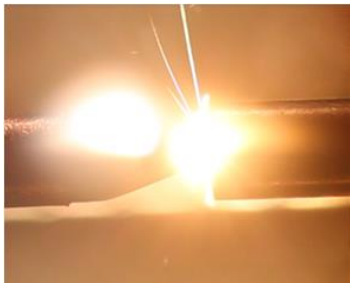

Fig. 4. Arc Drawn with C and Cu Electrodes

setup would be more representative of a flight power system that would experience an arc. Electrode separation speed and final arc gap length were held constant at 0.75mm/s and 0.75mm, respectively. These speed and separation values were selected because they were found by trial and error to generate arcs reliably. An arc drawn with C and Cu electrodes is shown in Fig. 4.

IV. Model Development

For Step 2, a manual model development process was chosen to inform future efforts to prototype the SAFDI process and help determine how best to automate future model development. State equations for capacitances and inductances (Equation (1) through (4) below) as well as an arc gap voltage equation were developed into an ordinary differential equation (ODE) model. Then, bandpass-filtered noise was added to the model after differential equations were solved to match both arcing and non-arcing data. The Modified Ayrton-Paukert equation as provided in [11] was used for the steady state arc gap voltage. Hand-tuned proportional-integral (PI) controllers were used to represent the dynamic behaviors of the current-limiting power supply and constant power load.

$$\dot{V_{cs}} = \frac{V_s - V_{cs}}{Rline} \tag{1}$$

$$\dot{I_{arc}} = \frac{V_{cs} - V_{gap} - V_c}{L} \tag{2}$$

$$\dot{V_c} = \frac{I_{arc} - \frac{V_C}{R_{load}}}{C} \tag{3}$$

$$V_{gap} = \frac{a + bG}{I_{bus}^{c+dG}} + aG^{\frac{b}{a}} \tag{4}$$

Model tuneable parameters included the following: source voltages, load powers, scenario types (arc fault or scenario intended to induce a false positive), and arc fault test detection thresholds. Non-arcing test conditions to test for false positives were the following: load power steps, source voltage disturbances, ripple voltages, and short circuits. Coefficients in the arc gap voltage equation were tuned to match observed arc gap voltages, and a noise model was adjusted for arcing and non-arcing conditions to generate the match testbed data and model outputs. A qualitative match was deemed sufficient to move forward with detector design and optimization.

V. Detector Implementation

A. Detector Design in Software

To accomplish a prototype of Step 3, three different detectors selected from the literature were implemented, tuned, and tested in software using the model from Section IV. All the detectors look for signatures in the sensed current data spectrum unique to electric arcs: (1) an autocorrelation-based method [12], (2) a detector composed of a bandpass filter and envelope detector, and (3) a method based on integrating the Fast Fourier Transform (FFT) of current through a capacitance in parallel with the load (shunt capacitance) [13]. Flowcharts describing these algorithms and their detection criteria are given in Fig. **6**. The autocorrelation and envelope detectors both require the arc spectrum to be isolated using a bandpass filter. Early testing identified a useful frequency band of interest for arc detection to be between 5 kHz and 20 kHz as shown in Fig. 5. Therefore, a bandpass filter with a passband between 5 and 20 kHz was used for these detectors.

The model was run both with arcs generated and with other spurious events designed to induce false positive detections (i.e., load steps, shorts, and bus voltage disturbances). High-bandwidth current data from these runs of the model were fed into each detector to determine their average latency and estimated accuracy. Edge case (parameters varied +/- 10% of nominal values) and Monte Carlo (parameters set to random values within +/- 10% of nominal values) simulations were run, and the OpenMDAO Simple Genetic Algorithm (GA) [14] was used to tune the

parameters of these detectors to maximize their performance (Fig. **7**).

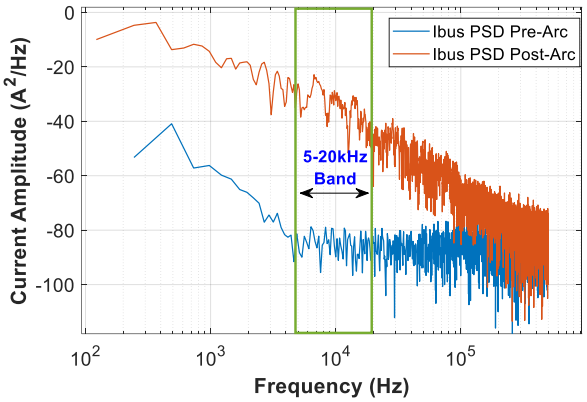

Fig. 5. Line Current PSD Pre- and Post-Arc

The objectives used for the GA were F1, a simultaneous measure of the detectors' immunity to false positives and to false negatives (as opposed to simple accuracy), and average detection latency [15]. Detector speed and accuracy (or F1 value) are competing objectives, so the optimization process for each type of detector produced a Pareto front in these two objective dimensions. The solution chosen from the Pareto front was the one with the maximum F1 score, and if multiple solutions with maximum F1 were found, then the one with minimum latency was chosen.

B. Validating Detectors with Hardware Data

Thirty-six total test cases were run on the test setup described in Section III. Of those, 20 were arc fault cases, 10 were power load steps (+/-10% of nominal load power (420W)), and 6 were source voltage steps (+/-10% nominal source voltage (28VDC)). No false positives were induced by the load and voltage steps. The autocorrelation detector failed to detect 3 out of 20 arcs, and the shunt capacitor detector failed to detect 1 out of 20. The envelope detector successfully detected all 20 arcs. In software, both the envelope and shunt capacitor detectors averaged latencies below 1 ms, while the autocorrelation detector averaged 8ms latency (Fig. 8 and Fig. 9).

C. Envelope Detector Implementation on Hardware

The envelope detector was implemented in an AMD Artix 7 XC7A35T-1CPG236C FPGA onboard a Digilent CMOD A7. The bandpass filter was designed as a 100-order FIR bandpass filter via the least-squares method for a passband of 5 kHz to 20 kHz. The lowpass filter inherent in the envelope detector was a single pole FIR filter with a pole at 1 kHz. The sample rate was 400 kHz. A live arc was detected within 2 ms, besting the 10 ms detection latency requirement put forward at the start of this work (Fig. **10**). The autocorrelation and shunt capacitor algorithms will later be implemented on the same FPGA to assess their real-time performance (see future plans in VI).

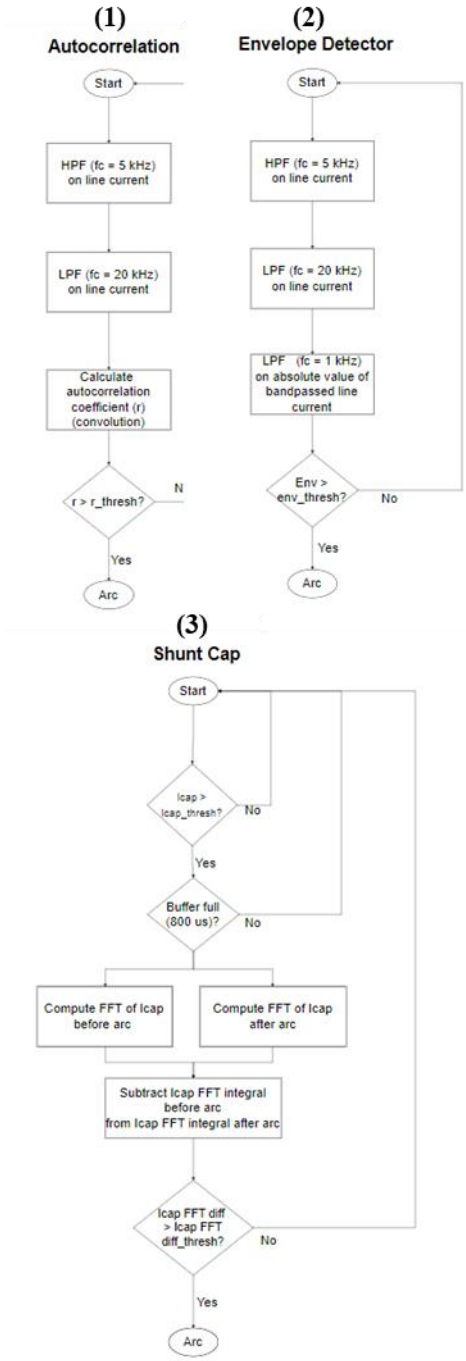

Fig. 6. Detector Algorithm Flowcharts

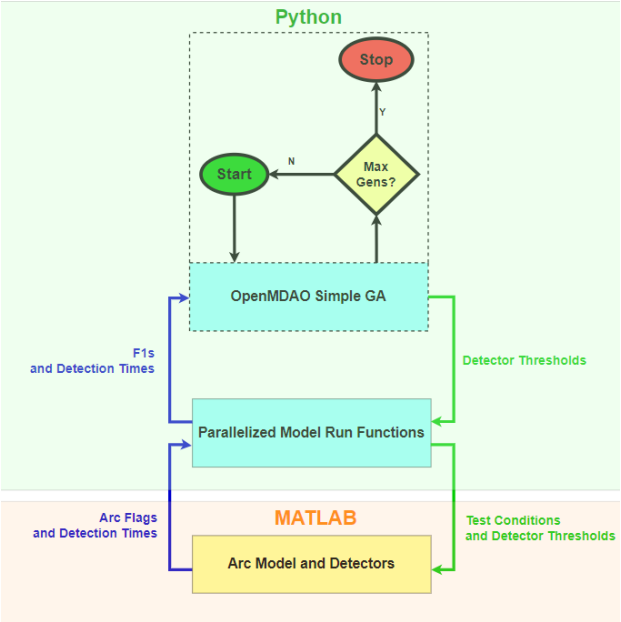

Fig. 7. OpenMDAO Simple GA and Arc Model

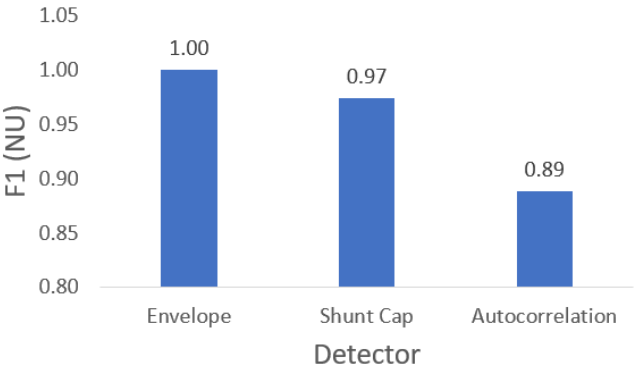

Fig. 8: Detector F1 Scores

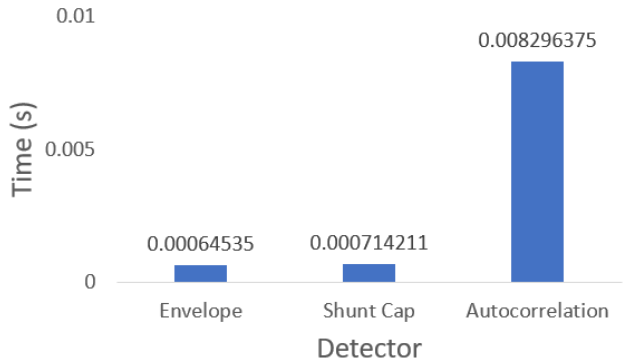

Fig. 9. Average Detector Latencies

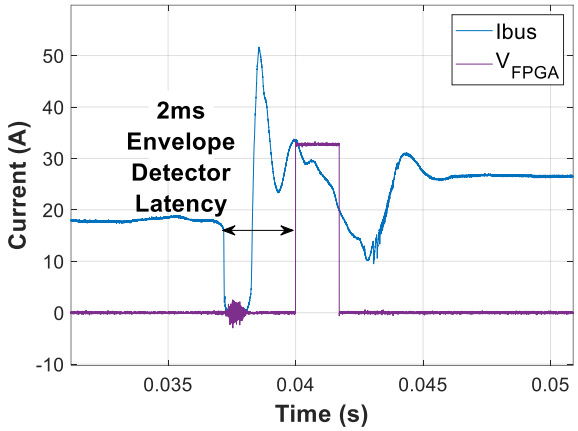

Fig. 10. Envelope Detector Latency in Hardware

VI. Conclusions and Future Work

This paper describes a process applicable to any DC power system for designing a DC series arc detector. An initial prototyping effort to implement this process was made, culminating in a demonstration of a detector design in FPGA hardware. Public acceptance of emerging electrified aircraft relies on accurate, low-latency detection of DC arc events. The SAFDI workflow was advised by the expectation that interpretable algorithms will have a more assured and simpler path to aerospace flight certification than black-box algorithms. DC arc data was generated, which was used to create the arc model and optimize three arc detectors. One of these algorithms, a line current envelope detector, was then successfully implemented on an FPGA. Successful arc detection was performed with the setup described in Section III. For this low-power system, the line current envelope detector's performance dominated the other two detectors, achieving a perfect F1 score and detection speed an order of magnitude or greater than the 5-10ms requirement.

Future work involves plans to design an amalgamation of multiple detection approaches (including those studied in this work) using an interpretable AI approach to achieve better performance than would achieved by any single detector. There are plans to implement the autocorrelation and shunt capacitor algorithms on an FPGA, test them in hardware, and combine them with the envelope detector into a single detector. Higher detection speeds are expected with the implementation of improved current sensors interfacing with the FPGA. Voltage sensing tests will also be explored, such as a measurement of the magnitude of a voltage difference between the source and load voltages as signaling the presence of an arc (due to the voltage drop across the series arc column). Other future work involves evolving from a manual implementation of the SAFDI process to a fully automated one. The SAFDI process will also need to be tested not only against a greater volume of arc test data, but also against different power system topologies and impedances: higher voltages and powers, different atmospheric pressures, different arc gaps and separations speeds, alternative electrode materials and shapes, and a variety of sources and loads, among other conditions, need to

be tested to show conclusively that the SAFDI process is in fact "system-agnostic." In addition, other human-interpretable machine learning techniques for optimizing detector thresholds and accurately modeling arc behavior will be explored, including Kolmogorov-Arnold Networks (KANs) [16] and symbolic regression techniques such as those available in the PySR module [17].

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