

High-Impedance and Low-Impedance Fault Protection Requirements and Verification Testing for Electric Aircraft Power Systems

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Abstract— Electric- and hybrid-electric vertical takeoff and landing (eVTOL) aircraft are essential to the success of many of the advanced air mobility (AAM) air transportation systems. High-voltage direct current (HVDC) architectures have received most of the aviation industry's focus in electrical power system (EPS) research, but requirements of HVDC power systems have not yet been defined for these aircraft. This paper will describe a method of high-impedance and low-impedance fault verification testing per requirements for developing HVDC power quality standard(s). Two novel fault injection test systems were developed. The first method uses parallel integrated bipolar junction transistors (IGBTs) to switch high-impedance faults onto a HVDC bus, and the second uses an integrated gate-commutated thyristor (IGCT) to switch low-impedance faults onto a DC bus. This paper demonstrates hardware design and fabrication, power quality testing procedure, and test results.

Keywords—HVDC, power quality, DC fault injection, electrified aircraft

I. INTRODUCTION

Investigations into high voltage direct current (HVDC) power quality (PQ) and power system integration issues are being performed to enable the benefits of electric aircraft propulsion [1]. The investigations are feeding results to international standards for HVDC PQ [2]. To ensure validation of new standards development, new test methods are required for HVDC systems. This need prompted the development and fabrication of the DC Fault Injection Unit, which consists of high impedance (soft) fault and short circuit (hard) fault injection options. This paper presents a new design for a one-stop-shop, rack-mount unit that can be used for fault testing of the HVDC propulsion system.

II. DC FAULT INJECTION UNIT OVERVIEW

A DC Fault Injection Unit (FIU) capable of injecting high-impedance faults, low-impedance faults, and large signal disturbances onto a HVDC bus was designed and built to test electrical power system (EPS) power quality in abnormal and faulted conditions (Fig. 1). The unit was designed to be modular and capable of being installed in numerous electric propulsion system topologies. This paper will discuss the high-impedance and low-impedance fault injection components.



Fig. 1. DC Fault Injection Unit

A. High-Impedance Faults

A high-impedance fault, otherwise known as a soft fault, is a type of fault that produces an overcurrent condition that is not normally removed by protective elements such as a fuse or breaker. Overcurrent conditions resulting from a high-impedance fault must be removed by the EPS within a specified timeframe to prevent system damage. The ability for the EPS to detect and remove this type of fault must be verified via test to ensure safe and proper operation of the power system. Impacted requirements related to fault clearing, fault coordination, overvoltage surge, and undervoltage surge must be verified by new test methods and techniques that are capable of repeatably injecting a soft fault condition onto the HVDC bus.

B. Low-Impedance Faults

Low-impedance (hard) faults are the most destructive type of faults that can occur on an EPS. These types of faults produce excessively high currents. Impacted requirements related to fault clearing, fault coordination, overvoltage surge, and undervoltage surge must be verified by new test methods and techniques that are capable of repeatably injecting a high-current or short circuit (“hard”) fault condition onto the HVDC bus.

III. FAULT INJECTION UNITS

A. High-Impedance Fault Injection Unit

The new method of soft fault emulation detailed in this document utilizes two high-power Silicon Carbide (SiC) Insulated Gate Bipolar Transistors (IGBTs) in parallel, outlined in Fig. 2, which can provide up to 1 kA of current emulating a soft fault through a set impedance.

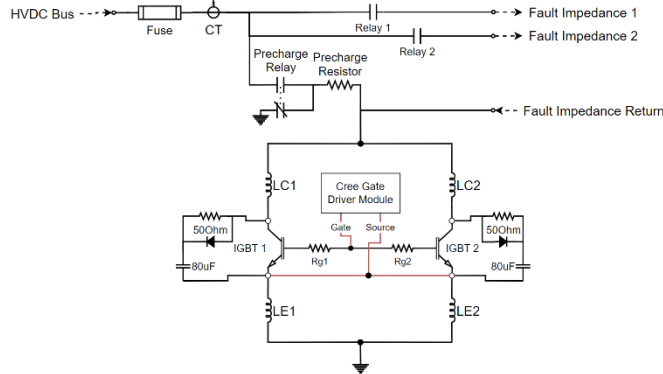


Fig. 2. High-Impedance Fault Injection Circuit

The advantages of this technique include high configurability, high adaptability, lower cost and smaller footprint than similar EPS equipment, and impedance selection for different fault conditions. The parallel configuration of two SiC IGBTs provides up to 1 kA of soft fault current emulation through a configurable impedance. The IGBTs are controlled by a central CREE XM3 gate driver to ensure simultaneous commutation. The branch connections to each switch are designed to ensure balanced current sharing during the

injection interval as shown in Fig. 3 IGBT1 and IGBT2 currents.

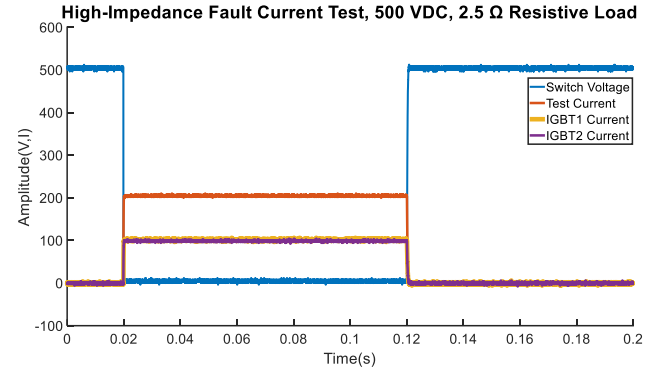


Fig. 3. Parallel IGBT Fault Current Test

This is accomplished by placing the IGBTs close together to minimize overall inductance (see Fig. 4), providing uniform connection between each branch to minimize the differences in branch inductance, and driving both IGBTs with a central gate driver unit. The unit contains two 1.5 kV, 1 kA contactors for selecting between two desired impedances for soft fault injection and a pre-charge circuit to prevent IGBT snubber shoot-through when engaging fault impedances [3].

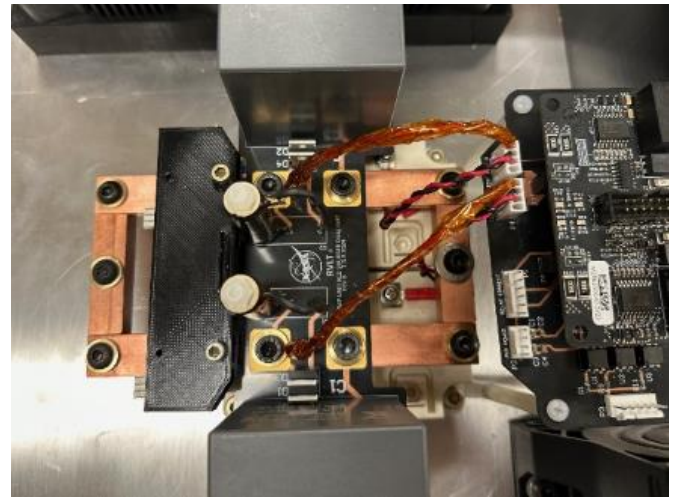


Fig. 4. IGBT Connection and Spacing

B. Low-Impedance Fault Injection Unit

The new method of short circuit emulation introduced in this paper uses an integrated gate-commutated thyristor (IGCT) to initiate and interrupt a hard fault (should protective devices fail to do so) (Fig. 5). Advantages of this technique include the following: a commercial-off-the-shelf (COTS) IGCT is highly reconfigurable, controllable, low-cost, low-volume, and able to execute a wide range of test durations. An asymmetric IGCT capable of withstanding 6 kA (derated to 4 kA) at 4.5 kV is used to initiate a hard fault on the DC bus (Fig. 6).

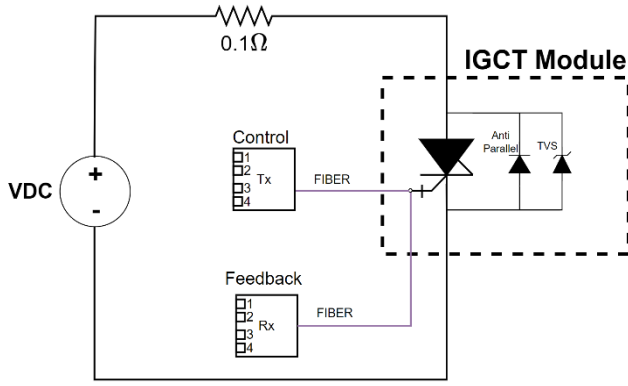


Fig. 5. Low-Impedance Fault Injection Test Circuit

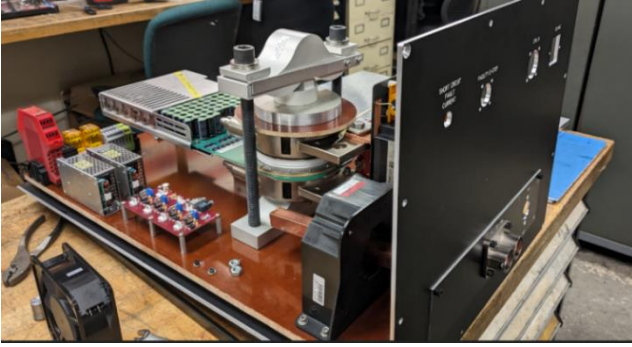


Fig. 6. Low-Impedance Fault Injection Test Enclosure

The gate unit's turn-off circuitry is illustrated in Fig. 7: a bank of MOSFETs closes to send enough charge carriers to the capacitor bank from the thyristor cathode (red line on the right-hand side) to reverse bias the gate-cathode junction, switching off the IGCT [4]. This capability is necessary because a thyristor latches in DC.

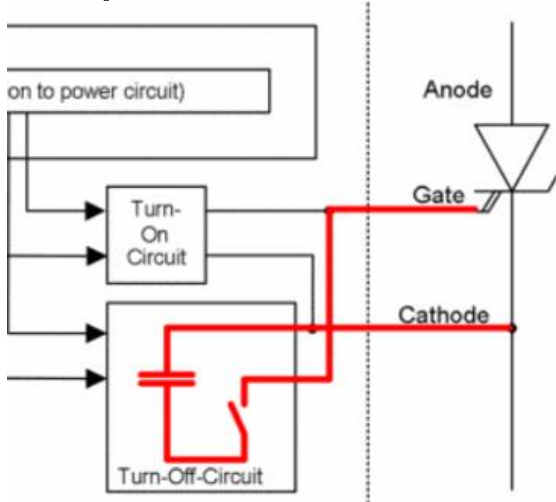


Fig. 7. IGCT Turn-off Mechanism

The IGCT was bench tested at various DC bus voltages up to 200 VDC. Fig. 8 shows testing conducted at 200 VDC

and 250 VDC with a 0.1 Ω , 250 W wire-wound chassis-mount resistor acting as a representative source impedance and 500 A current-limiting power supply for 2 ms. At higher bus voltages (and hence higher currents) with the same load, longer IGCT turn-off times were observed, but no turn-off time greater than 1ms was observed in this testing.

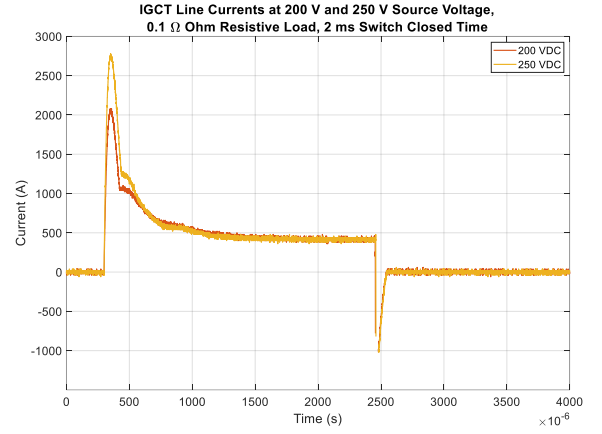


Fig. 8. Low-Impedance Fault Injection Test Data

Fig. 9 shows IGCT air-cooled and liquid-cooled permissible operating areas. These curves were obtained by operating the IGCT in an air-cooled mode with a continuous current at an 80 W heat dissipation rate until the temperature stabilized. The voltage drop across the IGCT when switched on was 3 V, the maximum allowable test current was 4 kA, the maximum allowable test duration was 400 ms, and the minimum time between tests was 60 s:

$$3 \text{ V} \cdot 4 \text{ kA} \cdot 0.4 \text{ s} / 60 \text{ s} = 80 \text{ W}. \quad (1)$$

Air-and-water-cooled operation permits substantially longer test pulse durations, as the dark blue area of Fig. 9 shows. A metal-oxide varistor clamps voltage at 2 kV at the 4 kA maximum test current.

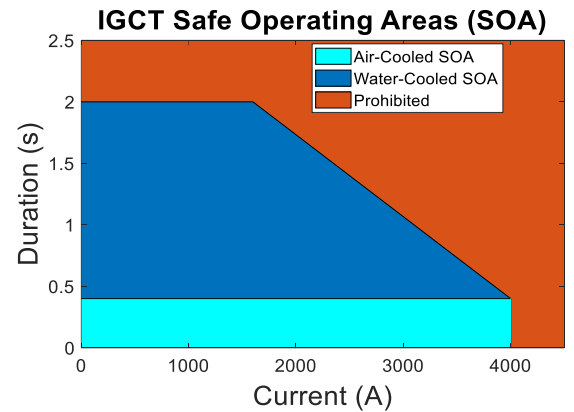


Fig. 9. Low-impedance Fault Injection IGCT Safe Operating Areas

C. Enclosure Control and Interface

A central control unit was created to interface with each test unit. The control unit contains a small single-board computer that hosts a graphical user interface (GUI) shown in Fig. 10 to configure and operate each test apparatus.

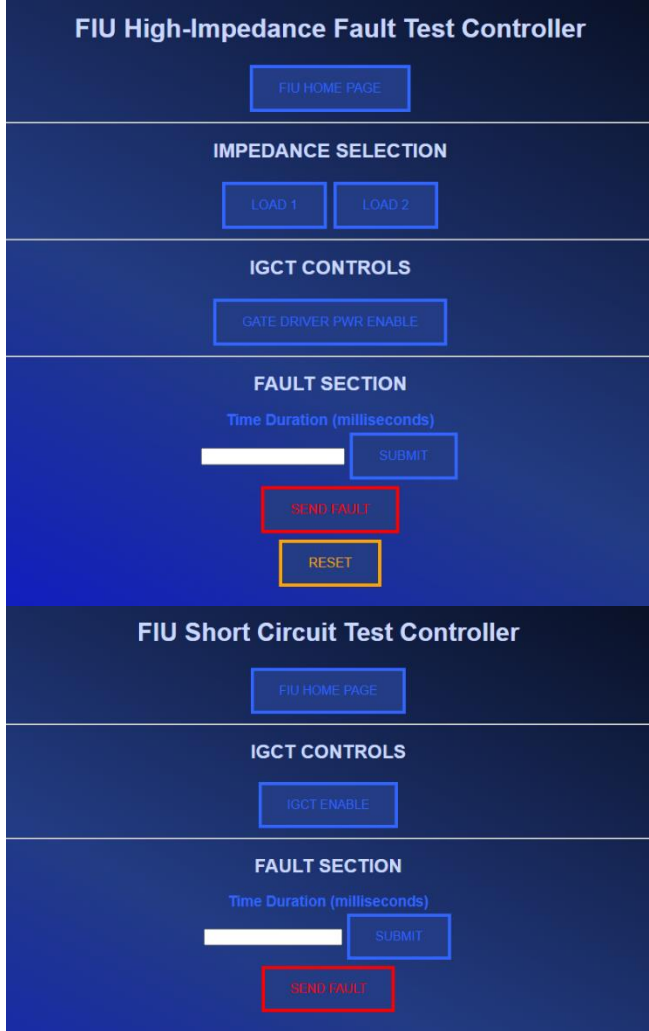


Fig. 10: High-Impedance and Low-Impedance FIU GUI

The single-board computer operates each test unit through an Internet of Things communication protocol called Message Queuing Telemetry Transport (MQTT). This lightweight publish/subscribe messaging protocol provides simple machine-to-machine telemetry to operate the semiconductor devices and relays in each test unit [5].

A python client monitors messages published from the GUI and enclosure feedback, outlined in Fig. 11, and determines general-purpose input/output control states to relays and gate drive units.

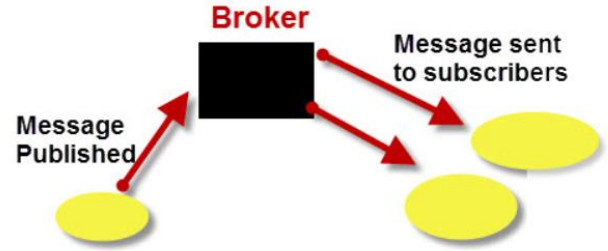


Fig. 11: MQTT – Publish Subscribe Model [6]

Cable connection points are located on the rear of each unit while power switches, temperature meter readouts, and colored machine state light-emitting diodes are located on the front of each unit.

IV. FAULT TESTING IN ELECTRIC AIRCRAFT POWER QUALITY TESTBED

A. Testbed Features and Capabilities

The National Aeronautics and Space Administration (NASA) Revolutionary Vertical Lift Technology (RVLT) project has constructed the Advanced Reconfigurable Electrified Aircraft Laboratory (AREAL). This laboratory is a 200 kW, 300 VDC-1 kVDC (peak) testbed able to be adapted to test multiple HVDC system configurations. Dynamic power supplies act as high-voltage sources in the testbed. Permanent magnet motors, as well as an electric motor emulator, act as loads. A COTS inverter/motor pair is located on a drivestand with one motor acting as the device under test while the other acts as a dynamometer load with the inverters operating in speed or torque control mode depending on test needs. An Inverter/Electric Motor Emulator (EME) pair exists in parallel with the real motor to minimize risk of testing abnormal faulted operating scenarios on actual hardware [7].

B. Testbed Multistring Configuration

The testbed's multistring configuration refers to parallel motor (or emulated motor) loads fed by two dynamic high-voltage sources. A Main Bus Switching Unit (MBSU) houses overcurrent and overload protection for cables and loads (motors or emulated motors) connected to the HVDC bus, as shown in Fig. 12 [7].

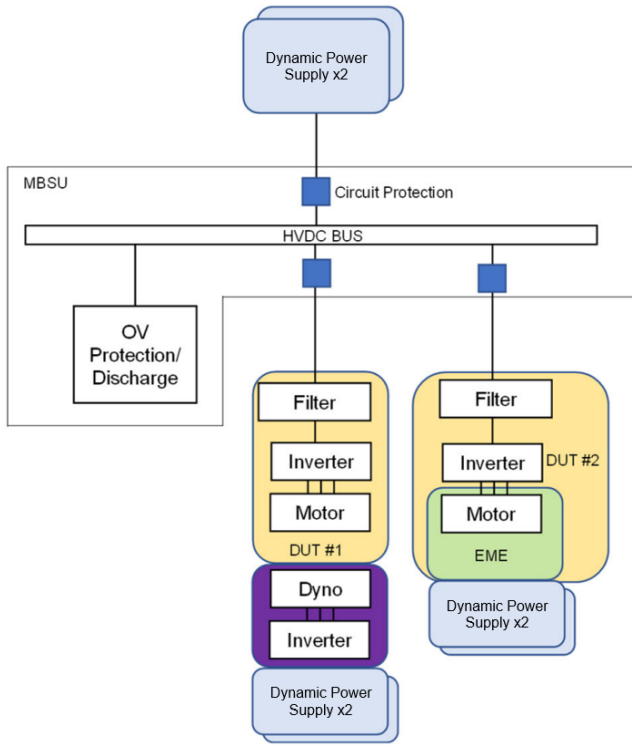


Fig. 12. AREAL System Configuration

C. Fault Testing in Power Quality Testbed

The high-impedance and low-impedance fault injection units will be connected to the DC bus in the multistring configuration via the MBSU as shown in Fig. 13. Abnormal fault current operating scenarios will be tested to validate the power system removes the excess current within a specified time frame. The fault will be cleared by the MBSU or circuit protection within the inverter, and EPS abnormal performance relative to the bus and drive stand inverter will be measured and characterized. Power quality testing pass/fail criteria will be used to determine whether the EPS and loads connected to the same electrical bus as the fault injection unit can withstand faulted operation [7].

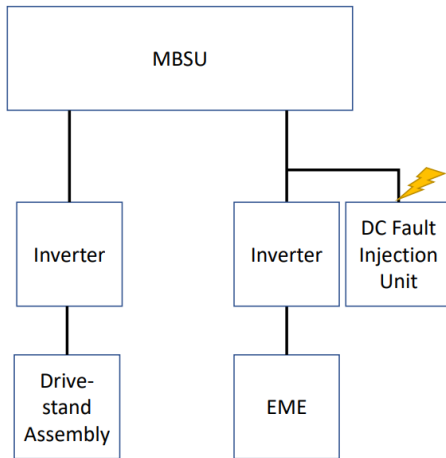


Fig. 13. AREAL Fault Injection Configuration

V. CONCLUSION AND FUTURE WORK

Two DC fault injection apparatuses were built and integrated into a larger DC Fault Injection Unit. Parallel IGBTs were used to generate high-impedance faults, and an IGCT was used to generate low-impedance faults. Each enclosure enables high voltage DC power quality testing in faulted conditions to satisfy power quality testing requirements. Once integrated into a high-power testbed, results obtained from each fault injection unit will enable characterization and testing of a high voltage DC EPS for power quality. These enclosures enable validation of the proposed PQ specifications and enable verification of the hardware's ability to meet those PQ specifications if adopted by the aerospace industry.

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