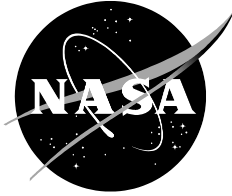
NASA/TM—20250005202



Single-Event Effects Test Report Micron MT25QU512ABB Serial NOR Flash Memory

Adia M. Wood

Edward P. Wilcox

December 2023

NASA STI Program Report Series

The NASA STI Program collects, organizes, provides for archiving, and disseminates NASA's STI. The NASA STI program provides access to the NTRS Registered and its public interface, the NASA Technical Reports Server, thus providing one of the largest collections of aeronautical and space science STI in the world. Results are published in both non-NASA channels and by NASA in the NASA STI Report Series, which includes the following report types:

- TECHNICAL PUBLICATION. Reports of completed research or a major significant phase of research that present the results of NASA Programs and include extensive data or theoretical analysis. Includes compilations of significant scientific and technical data and information deemed to be of continuing reference value. NASA counterpart of peer-reviewed formal professional papers but has less stringent limitations on manuscript length and extent of graphic presentations.

- TECHNICAL MEMORANDUM. Scientific and technical findings that are preliminary or of specialized interest, e.g., quick release reports, working papers, and bibliographies that contain minimal annotation. Does not contain extensive analysis.

- CONTRACTOR REPORT. Scientific and technical findings by NASA-sponsored contractors and grantees.

- CONFERENCE PUBLICATION. Collected papers from scientific and technical conferences, symposia, seminars, or other meetings sponsored or co-sponsored by NASA.

- SPECIAL PUBLICATION. Scientific, technical, or historical information from NASA programs, projects, and missions, often concerned with subjects having substantial public interest.

- TECHNICAL TRANSLATION. English-language translations of foreign scientific and technical material pertinent to NASA's mission.

Specialized services also include organizing and publishing research results, distributing specialized research announcements and feeds, providing information desk and personal search support, and enabling data exchange services.

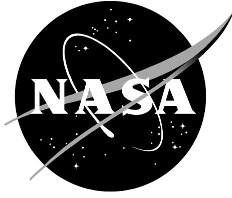
For more information about the NASA STI program, see the following:

- Access the NASA STI program home page at http://www.sti.nasa.gov

- Help desk contact information:

https://www.sti.nasa.gov/sti-contact-form/ and select the "General" help request type.

NASA/TM—20250005202



Single-Event Effects Test Report Micron MT25QU512ABB Serial NOR Flash Memory

Adia M. Wood
Goddard Space Flight Center, Greenbelt, MD

Edward P. Wilcox
Goddard Space Flight Center, Greenbelt, MD

Test Date: 12/2/2023
Report Date: 1/30/2024

National Aeronautics and
Space Administration

Goddard Space Flight Center
Greenbelt, MD 20771

December 2023

Acknowledgments

This work was sponsored by the NASA Electronic Parts and Packaging (NEPP) Program.

Trade names and trademarks are used in this report for identification only. Their usage does not constitute an official endorsement, either expressed or implied, by the National Aeronautics and Space Administration.

Level of Review: This material has been technically reviewed by technical management.

Available from

NASA STI Program
Mail Stop 148
NASA's Langley Research Center
Hampton, VA 23681-2199

National Technical Information Service
5285 Port Royal Road
Springfield, VA 22161
703-605-6000

This report is available in electronic form at
https:// nepp.nasa.gov/

1. Introduction and Purpose

This study was undertaken to explore the device response to a single-event effects (SEE) radiation environment. Specifically, the device was monitored for destructive single-event latchup (SEL) and fully characterized for non-destructive single-event upsets (SEU) and functional interrupts (SEFI). Discovery of minimum necessary recovery steps in the event of a functional interrupt was also a key objective.

2. Test Result Summary

The MT25QU512ABB has a single-event latchup (SEL) linear energy transfer (LET) threshold between 29.4 and 45.3 MeVcm^2/mg at 55°C. The threshold is less than 29.4 MeVcm^2/mg at 82°C.

The single event upset (SEU) LET threshold is less than 8.2 MeVcm^2/mg, and the measured cross-section is approximately 1.8x10^{-16}cm^2/bit at that LET.

3. Device Description

The MT25QU512ABB is a 512Mb serial NOR flash memory. Twenty devices were commercially procured with an automotive-grade part number, and ten underwent chemical-laser decapsulation. Five devices were tested at the Lawrence Berkeley National Laboratory (LBNL). The lot date code of the devices tested is 2YA15. The device is provided in a plastic 16-pin SOIC package.

Table I. Part description

Part Number	MT25QU512ABB
Full Procurement Part Number	MT25QU512ABB8ESF-0AAT
Manufacturer	Micron
Lot Date Code	2YA15
REAG ID #	23-025
Quantity Tested	5
Part Function	Serial NOR flash
Part Technology	CMOS
Package	SOP2-16

Photographs of the device prior to (Fig. 1) and after (Fig. 2) decapsulation are provided below.

Fig. 1. Device as procured

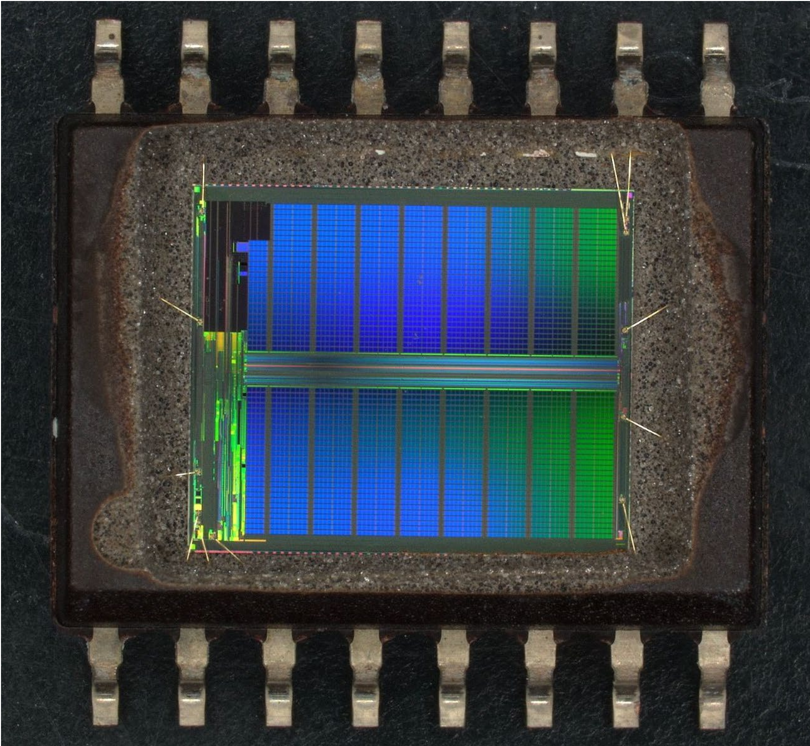


Fig. 2. Device after chemical-laser decapsulation exposing silicon die

4. Test Setup

Devices were evaluated with a commercial Zynq-7020 evaluation board (Pynq-Z2), with test execution in the dual core ARM-9 processor and a hardware SPI interface to the memory. Power was provided to a carrier board (Fig. 3 middle board, with BNC connected) that also translated I/O voltages during testing. The surface-mount DUTs were installed on daughtercards (Fig. 3 smallest board on far right).

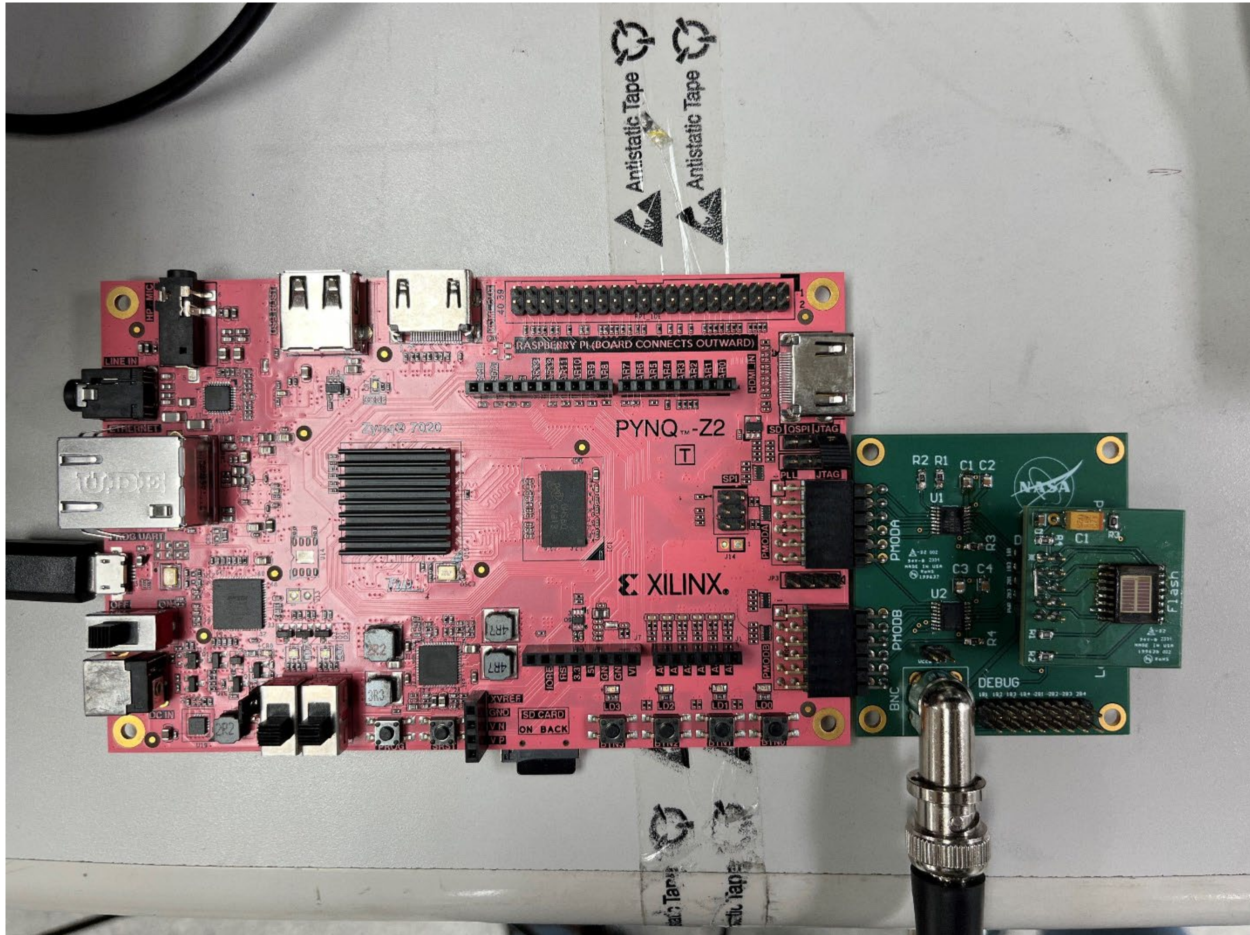


Fig. 3. Test setup with Zynq 7020 board (left, pink), carrier board (middle, with BNC), and device under test daughtercard (right)

Heating for the device under test was provided by resistive heating strips (not pictured) applied to the backside of the DUT card for use in a vacuum chamber. Temperature monitoring was conducted via thermistors (not pictured) thermally glued to the DUT casings.

5. Test Facility

Facility:	Lawrence Berkeley National Lab (LBNL) 88" Cyclotron
Type of Radiation:	Heavy ions
Facility Configuration:	10 MeV/amu tune (16 MeV/amu tune acceptable)
Flux:	Approximately $1x10^4 cm^{-2}s^{-1}$.
Fluence:	Testing shall be conducted to at least $1x10^6 cm^{-2}$ at each test condition for three devices. At least one device shall be tested to $1x10^7 cm^{-2}$ at the worst-case planned SEL test condition.
Beams / LET:	10 MeV/amu Au; surface LET 86 MeV·cm^2/mg 10 MeV/amu Kr; surface LET 31 MeV·cm^2/mg 10 MeV/amu Cu; surface LET 21 MeV·cm^2/mg 10 MeV/amu Ar; surface LET 9.7 MeV·cm^2/mg 10 MeV/amu Ne; surface LET 3.5 MeV·cm^2/mg 10 MeV/amu B; surface LET 0.89 MeV·cm^2/mg

6. Test Conditions

Temperature:	SEU/SEFI: Ambient temperature, vacuum SEL: 85°C, vacuum
In-Air or Vacuum:	In-air

7. Test Methods

7.1. Single-Event Latchup

Characterization of SEL LET threshold was an objective of this test. Determination of the highest possible passing LET (without SEL) was prioritized over a large sample size at each LET.

The device was powered at worst-case V_{CC} and elevated temperature, and it was monitored for excessive supply current while in a static configuration. If a sudden elevated current was observed, the test was concluded, and the power supply was reset. The part was characterized for functional performance and the test repeated until a total fluence of $1x10^7/cm^2$ (when possible).

7.2. Single-Event Upsets

The device memory was programmed with a known pattern, irradiated with power off, and then evaluated for single-event upsets. A checkerboard pattern, an all zeros pattern, and an all ones pattern were used to explore pattern dependence. The SEU LET threshold was identified as well as reasonably practical, along with the saturated cross-section (high LET) and at least two intermediate LET points to construct a reasonable Weibull fit.

7.3. Single-Event Functional Interrupts

A series of active tests were performed to identify susceptibilities to SEFIs while in standby (by means of verifying device communications without affecting memory) and while dynamically reading and programming the memory.

In each case, when a SEFI event was observed by the tester, the beam was blocked, and a RESET command was attempted to clear the error and repeat the operation. If the error failed to clear, the run was ended and the power to the device cycled. Automatic SEFI testing was not implemented for this test.

SEFI testing was performed with a flux determined on-site so as to not overwhelm the performance of the device. The memory must be capable of operating for several seconds without SEFI occurring, and the time necessary to recover operation from a SEFI should be small relative to the mean time to failure (MTTF). The balance between low flux for improved test resolution and high flux for maximum testing in the time available was a game-time decision that cannot be entirely pre-planned.

8. Test Procedure

8.1. Single-Event Upset Characterization

1. Power on test setup and device and verify nominal current draw
2. Prepare for irradiation
   2.1. Erase memory
   2.2. Program memory with specified pattern
   2.3. Readback memory and record all errors
3. Power off the DUT
4. Irradiate to target fluence
5. Power on the DUT and verify nominal current draw
6. Collect post-test data
   6.1. Readback memory and record all errors
   6.2. Optional: readback again and record all errors to verify stable operation
   6.3. Record error counts and run data in test log for real-time analysis
7. Repeat

8.2. Single-Event Latchup Testing

If testing with manual beam intervention:

1. Power on test setup and device and verify nominal current draw
2. Heat device to 85°C
3. Irradiate to target fluence while actively monitoring DUT current draw
    3.1. If current reaches pre-set limit (TBD), turn off power to DUT and close beam shutter
4. Cycle power to DUT
5. Verify post-irradiation functionality
    5.1. Erase memory
    5.2. Program memory with specified pattern
    5.3. Readback memory and record all errors

If testing with automated power supply cycling:

1. Power on test setup and device and verify nominal current draw
2. Heat device to 85°C
3. Arm power supply current limit to level TBD
4. Irradiate to target fluence while actively monitoring DUT current draw
    4.1. If current reaches pre-set limit (TBD), test setup will automatically cycle power to DUT and log the time and count of power cycling
    4.2. Continue until target fluence reached.
5. Cycle power to DUT
6. Verify post-irradiation functionality
    6.1. Erase memory
    6.2. Program memory with specified pattern
    6.3. Readback memory and record all errors

8.3. Single-Event Functional Interrupt Testing

1. Power on test setup and device and verify nominal current draw
2. Begin test routine (base functionality, read-only, or read-write) and verify operating nominally
3. Irradiate to target fluence while monitoring operations. The crossed-out steps are parts of the test plan that ultimately were not implemented.
    ~~3.1. If an operation fails, test setup will automatically attempt RESET and (if necessary) power cycle operations to resume functionality. Each shall be counted and recorded.~~
    ~~3.2. If automated testing is failing to correct, test engineer must manually intervene by stopping the run and ending the test program.~~
    3.3. When a SEFI is identified, test engineer shall block the beam to the device and investigate functionality. If the effect is no longer present, the run may continue with the event manually logged. If the effect requires a reset, the run shall be ended here.
4. Cycle power to DUT
5. Verify post-irradiation functionality if any anomalies were observed during test
    5.1. Erase memory
    5.2. Program memory with specified pattern
    5.3. Readback memory and record all errors

9. Test Results

9.1. Single-Event Upsets

SEUs were recorded with the device unpowered to isolate raw bit cell upsets from support circuitry effects. Results are summarized in the following table:

UNBIASED SEU *italic: no errors observed* bits 536870912

LET	test type	pattern	Total Fluence	Total Pre	Total Post
8.2	SEU_unbiased	0xAA	1.01E+07	0	*1*
29.4	SEU_unbiased	0xAA	1.10E+07	0	2
45.3	SEU_unbiased	0xAA	4.46E+07	0	17
56.0	SEU_unbiased	0xAA	1.00E+06	0	62
79.2	SEU_unbiased	0xAA	2.12E+06	0	418

9.2. Single-Event Latchup

Single-event latchup was observed to be temperature-dependent for this device. When irradiated at ambient temperature, SEL was observed at an LET of 45.3 MeVcm^2/mg after 3.41x10^7/cm^2 fluence. This fluence is high enough that many tests would consider the device latchup immune after passing 1x10^7/cm^2 without SEL.

When the device was warmed to 55°C, four runs to a combined 1.03x10^7/cm^2 each ended with recoverable SEL.

At a maximum testing temperature of 82°C, SEL was possibly observed at an LET of 29.4 MeVcm^2/mg during a run with a total fluence of 1.1x10^7/cm^2. At this LET, the supply current only increased to 20 mA. SEL was more clearly observed with LETs of 45.3 and 79.2, where the supply current reached levels of 108 mA to 136 mA. The SEL cross-sections measured are summarized in the table below:

SEL LET cross-sections (italics for 0 SEL observed)

LET:	29.4	45.3	56.0	79.2
<29°C		4.15E-08	*1.00E-06*	
~55°C		3.88E-07		
~82°C	*9.09E-08*	1.56E-06		1.01E-06

9.3. Single-Event Functional Interrupts

9.3.1. Zeroed-Out Pages

SEFIs were observed both when actively testing for SEFIs (e.g., during active read/write testing) and when performing unbiased SEU tests. While SEFIs are not generally associated with unbiased irradiations, the results are provided here and may warrant further study. In these results, individual pages (256 bytes) readout all-zeros despite being programmed with 0xAA prior to the run. The phenomenon was relatively rare (note for example only one occurrence with $1.1 \times 10^7/cm^2$ at an LET of 29.4 $MeVcm^2/mg$), but the consequences could be significant for some applications – the authors urge caution when applying these results without further study into the cause.

UNBIASED ZEROED_PAGES bits: 536870912

LET	test type	pattern	Total Fluence	Total Wiped Pages	CS
8.2	SEU_unbiased	0xAA	1.01E+07	*1*	9.90E-08
29.4	SEU_unbiased	0xAA	1.10E+07	1	9.09E-08
45.3	SEU_unbiased	0xAA	4.46E+07	4	8.97E-08
56.0	SEU_unbiased	0xAA	1.00E+06	12	1.20E-05
79.2	SEU_unbiased	0xAA	2.12E+06	51	2.40E-05

9.3.2. READID Communications Checks

Active SEFI tests were performed with the device rapidly performing “READID” commands to verify the functionality of the control and communications circuitry, separate from the memory array. With an LET of 8.2 $MeVcm^2/mg$, two SEFI events were observed out of three runs, and a collective fluence was $1.49 \times 10^7/cm^2$. The SEFI required a power cycle to regain functionality.

At an LET of 29.4 $MeVcm^2/mg$, a single run ended with a SEFI at $2.80 \times 10^5/cm^2$. A power cycle was required.

At an LET of 45.3 $MeVcm^2/mg$, three test runs to a cumulative $3.1 \times 10^6/cm^2$ each ended with SEFIs requiring power cycling.

9.3.3. Erase/Program/Read SEFI Testing

Active memory operations in the beam were evaluated with a loop that rapidly erased, programmed, and read a single page of 256 bytes of data. In all tests, the run ended with a SEFI. When irradiating with an LET of 2.6 $MeVcm^2/mg$, the fluence to SEFI was $6.95 \times 10^5/cm^2$ for a single run. The mechanism appeared to be an erase cycle that did not correctly execute.

With an LET of 8.2 $MeVcm^2/mg$, five runs totaling $1.31 \times 10^6/cm^2$ resulted in five SEFIs. Four of the five appeared to be erases that didn’t execute correctly. The fifth was a very slow erase followed by a failed program command (device was stuck in an erased state). The device was subsequently unusable for unknown reasons, but a significantly-elevated supply current was not observed and the test was performed at room temperature.

At an LET of 29.4 MeV·cm²/mg, six runs totaling $8.33 \times 10^5/cm^2$ resulted in six SEFIs. In three of these cases, the SEFI was a communications failure; twice it required power cycling, and once a toggle of the physical RESET pin was sufficient. In two other cases the supply current went to 155 mA before recovering; a power cycle was necessary to clear these events.

10. Equipment List

Table II. Equipment List

Manufacturer and P/N	Function	S/N or ECN	Calibration Status
Keysight E36312A	Power Supply	MY61005525	Not calibrated
Pynq-Z2	Digital Tester		