AC AND DC FAULT MANAGEMENT FOR MEGAWATT ELECTRIFIED AIRCRAFT ELECTRICAL POWERTRAINS

TASK 1: CIRCUIT BREAKER DESIGN, DEVELOPMENT, TESTING AND EVALUATION

FINAL REPORT

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ACRONYMS

	-A-
AC	Alternating Current
AM	Additive Manufacturing
	-C-
CA	Collins Aerospace
	-D-
DC	Direct Current
DUT	Device Under Test
	-E-
EAP	Electrified Aviation Propulsion
EWS	Electrical Wiring System
	-F-
FCL	Fault Current Limiter
FEA	Finite Element Analysis
	-H-
HAEP	High-Altitude Emulated Pressure
HFCT	High Frequency Current Transformer
	-I-
IEC	International Electrotechnical Commission
	-M-
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MW	Megawatt
	-N-
NASA	National Aeronautics and Space Administration
	-P-
PCA	Principal Component Analysis
PD	Partial Discharge
PDEV	Partial Discharge Extinction Voltage
PDIV	Partial Discharge Inception Voltage
PMT	Photomultiplier Tube
P&W	Pratt & Whitney
	-R-
RM	Rugged Monitoring
RTAPS	Research and Technology for Aerospace Propulsion Systems
RTRC	RTX Technology Research Center
RTX	Raytheon Technology Corporation

-S-

SAP	Standard Altitude Pressure
SiC	Silicon Carbide
SSCB	Solid State Circuit Breaker

-T-

TVS	Transient Voltage Suppression

1. EXECUTIVE SUMMARY

The NASA RTAPS program on AC and DC Fault Management for Megawatt (MW) Electrified Power Train is a multi-year joint project with Pratt & Whitney (P&W), Collins Aerospace (CA), and RTX Technology Research Center (RTRC). This research program focuses on high-voltage distribution issues that present a significant technological obstacle in the adoption of Electrified Aviation Propulsion (EAP) systems. One of the most significant issues to overcome for high-voltage electric distribution systems to meet the EAP vehicle weight and efficiency requirements are high-power density, low-loss circuit breakers to control power and clear faults. This issue is addressed by the first task of the NASA RTAPs program, wherein a 1.2 MVA direct current (DC) circuit breaker is developed to protect the EAP system battery and motor drive.

This report covers the development and testing of the 1.2 MVA circuit breaker that was developed by RTX NASA RTAPS program for application to electrified aircraft. The breaker is designed to achieve the following performance: 1.2 kV, 1 kA, 35 kft, <100 us response time, with > 99.5% efficiency at 100 kW/kg. Detailing the development and testing of the circuit breaker, this report is therefore segmented into the following:

- Down selection of the DC circuit breaker topology to achieve the lowest steady state losses in the smallest footprint.
- Critical enabling component designs: the additive manufactured cold plate, high-bandwidth current sensors, and transient voltage suppression circuit to achieve the aggressive target metrics of the program.
- Characterization of the solid-state circuit breaker and its components.
- Testing and validation of the solid-state circuit breaker under steady state loading and emulated high-altitude conditions to achieve target fault clearing time and to examine the long-term insulation challenges due to the potential of partial discharge effects.

This program was able to successfully meet or exceed all defined program metrics, as highlighted in the Summary Table. As a point of context, solid-state circuit breakers as they currently exist in the commercial marketplace offer a specific power density in the range of 10-20 kW/kg under an operational voltage of less than 300V. Thus, the outcome of this program task is a step towards electrified propulsion by providing a critical distribution element that is capable of 1.2 kV/1 kA operation, fast protection and a specific power density that is approximately 5x better than the state of the art.

Table 1-1. *Summary Table of Achieved Program Metrics vs. Original Goals*

Metric	Measured	Goal
Bus Voltage	1.2 kV	1.2 kV
Clearing Time	< 100 us	100 us
Altitude	35 kft	35 kft
Efficiency ($50°C$)	> 99.5%	99.5%
DC Current	1 kA	1 kA
Specific Power Density	$> 100\ kW/kg$	$100\ kW/kg$

2. INTRODUCTION

Under pressure from increasing regulations on emissions, the aviation industry is experiencing an inevitable turn towards further electrification. Beginning with the "more electric aircraft', wherein electric power was utilized for the non-propulsion systems onboard the aircraft, the next frontier of development is the partial or full electrification of the propulsion system. However, while the transition to more electric components required adoption of electrical wiring systems (EWS) that were more complicated and higher power compared to past aviation systems, as shown in Figure 1, electrified propulsion systems will require processing in the multi-MW level – potentially with an order of magnitude increase in power levels over current systems. Further, while modern EWS on aircraft have DC subsections in the 270V range, distribution power levels in the multi-MW range requires higher DC operating voltages in the kV range to meet the specific power density requirements required to be competitive with traditional gas-powered aviation systems [1].

However, in addition to requiring high specific power densities and low loss operation, electrified aviation systems are also required to operate at the highest level of reliability. One challenge to the EWS reliability is the dielectric insulation failure due to either accelerated aging from partial discharge, or mechanical stress. Under higher operating voltages, the aging in the insulation due to partial discharge can be accelerated – particularly in the case of high-altitude operation and within power conversion equipment [2]. Further, due to the higher power levels, the impact of the faults is dramatically more consequential in released energy, and there is less system impedance due to the use of DC voltages to stop the buildup of dangerous arc currents [3]. Thus, the NASA RTAPS program aims to make a step change towards the development of lightweight, high reliable and high voltage power distribution components for EAP systems. This effort is coordinated across three primary tasks: the development of a lightweight, high efficiency DC circuit breaker, lightweight and low-loss magnetic materials for filter components, and the understanding of the aging of insulators in high voltage EWS on board aviation systems. These three efforts are depicted in Figure 2-1, as part of a demonstration electrified single aisle aircraft.

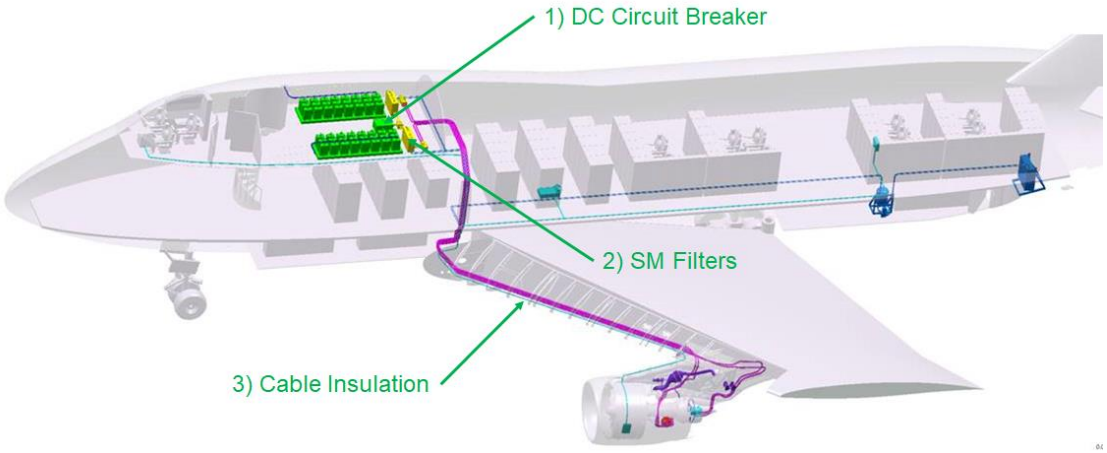


Figure 2-1. *Key Power Distribution Development Areas in an Electrified Aviation System*

This report focuses solely on the development of a solid-state circuit breaker, intended to operate within the system battery and the power conversion components, as per the RTX vision system in Figure 2-2. As part of this vision system, the intended DC operating voltage is 1.2 kV, with a steady state current of 1 kA and should be capable of completing the breaking operating in under 100 us to cope with the lower system impedance common to DC distribution systems. Further, a target of 100 kW/kg is envisioned for the solid-state circuit breaker (SSCB) with a single ended efficiency target of greater than 99.5% at an altitude of 35 kft. These key metrics are summarized in Table 2-1 and form the basis for the development of the NASA RTAPS SSCB development task.

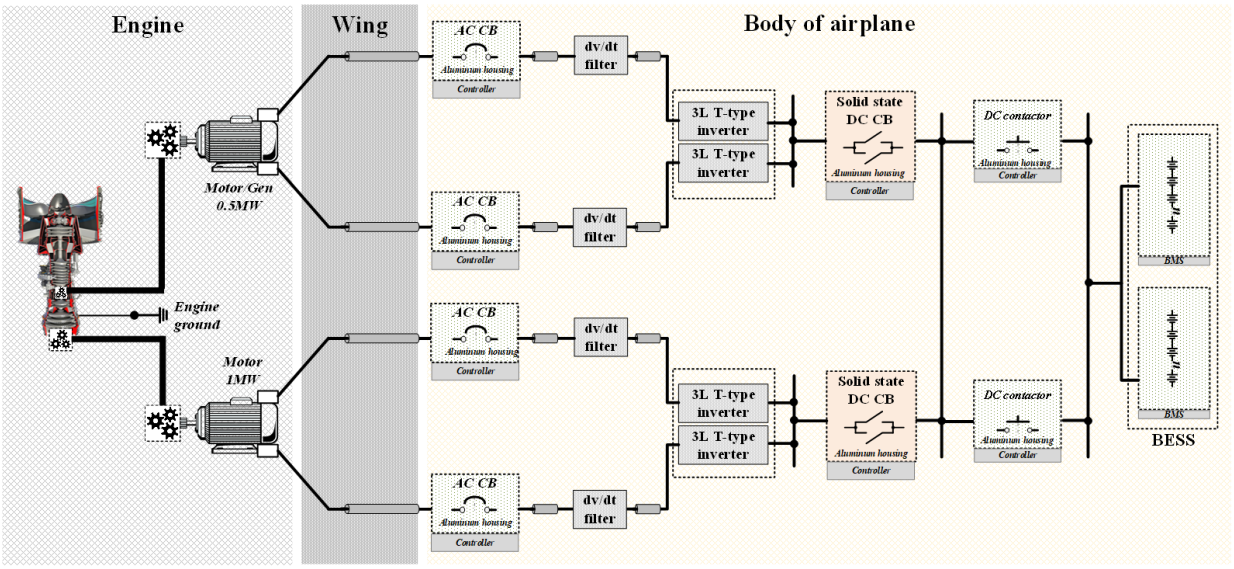


Figure 2-2. *DC Power Distribution Components and the Solid-State Circuit Breaker*

Table 2-1. *Key Program Metrics for the NASA RTAPS Solid-State Circuit Breaker*

	Metrics	Expected	Stretch	Gen-I
RFP Metrics	Specific Power (kw/kg)	100	200	>100
	Voltage (kV)	1-1.2kV	>2kV	1.2kV
	Current (A)	1,000	>1,000	1,000
	Response (µs)	100	10	<100
	Efficiency (%)	99.5	99.7	≥99.5
	Altitude (ft)	35,000	52,000	35,000
RTX Metrics	Fault Current Limiting Inductance (uH)			~10uH
	Voltage Clamping (kV)			< 2kV
	Losses (W)			<5,000

3. PROJECT OVERVIEW

The development of the NASA RTAPS SSCB occurred over a period of 6/2020 to 6/2023, with an additional quarter dedicated to the study of integrating DC arc detection into the developed hardware. Accordingly, the down selection of all components, development of the SSCB, characterization and testing of the design occurred across 12 quarters, across 4 design teams (Collins ECMS, Collins EPS, Collins HSG and RTRC) as per the development schedule in Figure 3-1. This section focuses on the operation of the SSCB, down selection of the circuit topology, as well as the development strategy for the three progressive builds to facilitate early learning, characterization of critical components and the eventual validation of the SSCB.

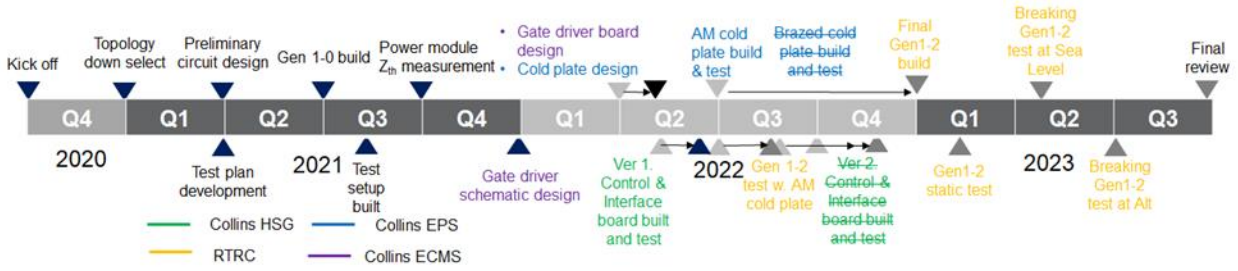


Figure 3-1. *Program Timeline and Team Coordination Across RTX*

3.1. Solid-State Circuit Breaker Elements and Operation

The SSCB is circuit breaker technology family wherein the primary line current conducting component and the component responsible breaking the line current during a fault are based on power semiconductors [4]. While hybrid configurations also exist, where the power semiconductors are only active during the fault interruption process [5], using the power semiconductors for all aspects of the circuit breaker operation has the best potential for the fastest fault interrupt time without compromising the specific power density [4].

The general topology of a solid state circuit breaker is depicted in Figure 3-2, highlighting four key components: the current limiting element (passives), which act to limit the rise time of the line current , the power semiconductors, which act as a low-loss element during normal operation and provides the mechanism for breaking the current during a fault, the energy absorption element, which avoids the formation of an arc over the breaking path, and the surge arrestor element, which clamps the voltage during the fault interruption phase to safely discharge the stored energy in the grid. Each of these elements within the solid-state circuit breaker form a technology tree, and have many variations reported in the state of the art [4], as shown in Figure 3-3.

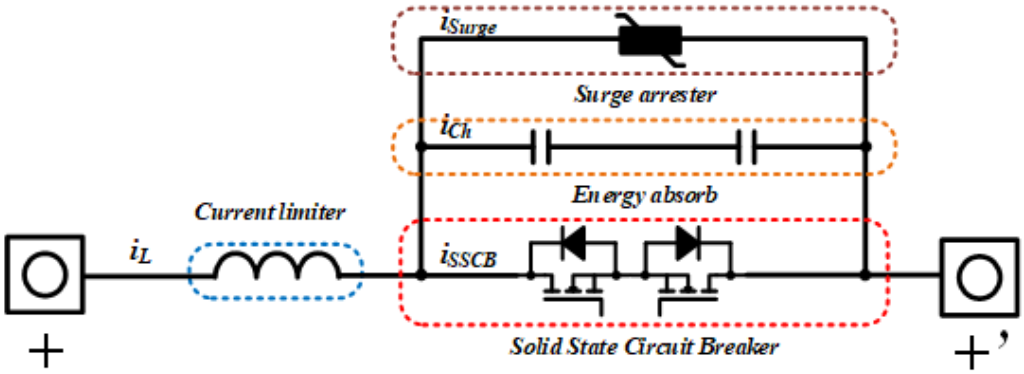


Figure 3-2. *Solid State Circuit Breaker Elements*

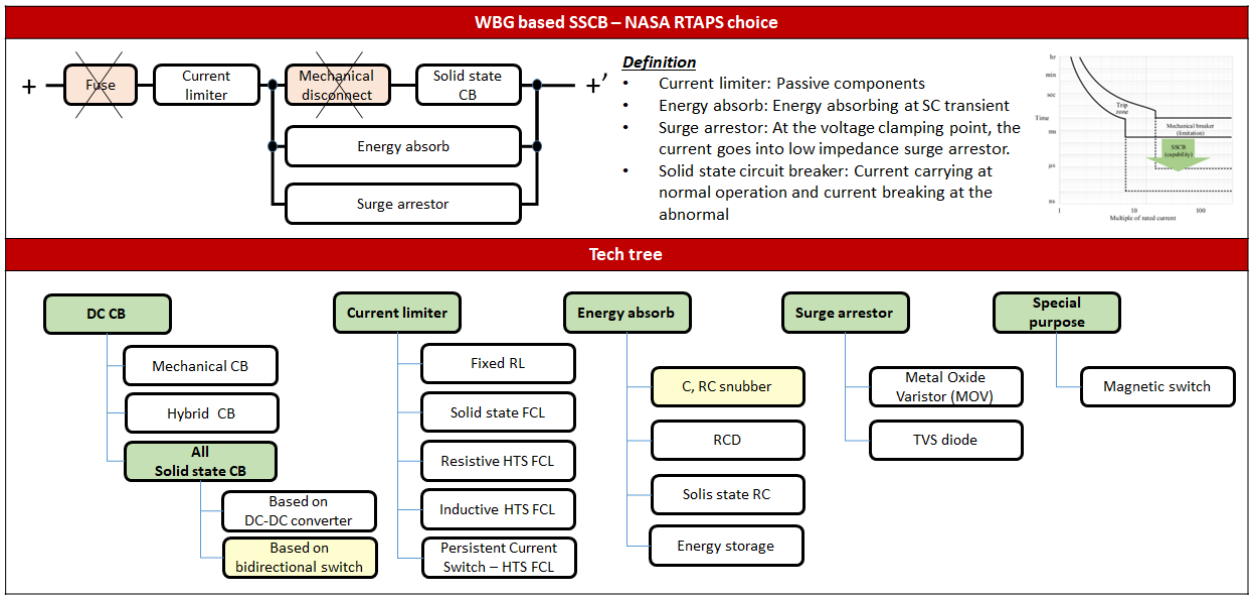


Figure 3-3. *Technology Tree of the Elements within the Solid-State Circuit Breaker*

The operation of the solid-state circuit breaker during a fault interruption event or a breaking event involves all elements to safely protect the immediate up and down stream components within the distribution system. In the normal operating condition, the power semiconductors are controlled to provide as minimal of a voltage drop as possible, typically with one semiconductor conducting in a single direction only. During a fault within the distribution system, time t_0 as per Figure 3-4, the current begins to increase – being limited by the current limiter and the system inductance. At some time, t_1, the increase in current is detected by the solid-state circuit breaker controller and the power semiconductors are switched off. Immediately, the previously conducting current in the power semiconductors begins to decrease and is taken up by the energy absorption element by time t_2. After this time, depending on the type of energy absorption element, the voltage and current continue to increase (forming a resonant mode in the case of a snubber circuit) until the voltage its peak, and the clamping circuit begins to take over the line current, as in time t_3. At some point the current is shunted into the clamping circuit, reverse biasing the system inductance causing the current to fall back to zero by time t_5. After this time, the solid-state circuit breaker has completed the fault current interruption event and can be safely reset.

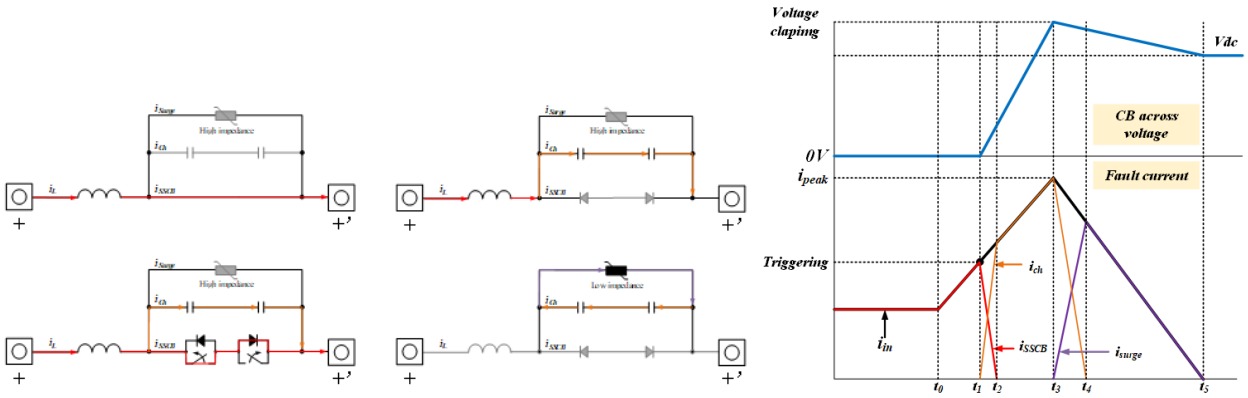


Figure 3-4. *Fault Current Interruption Sequence within a Generic Solid-State Circuit Breaker*

3.2. Topology Down-Selection

The initial efforts of the SSCB design involved studying and comparing a wide range of power electronic topologies. Many DC/DC converters based SSCB designs were originally considered owing to their ease of integration with many multi-voltage distribution grids [6] but were ultimately rejected due to their more complicated configuration compared to bidirectional power electronic topologies. In this case, the use of bidirectional power electronic topologies allows for a simple but high efficiency implementation with a good potential for a compact configuration [7]. It is the latter configuration that the RTX team focused on in more detail to optimize the RTAPS SSCB implementation.

In brief, five bidirectional configurations were evaluated in a qualitative manner to understand the key tradeoffs in terms of positive and negative attributes required to achieve the program metrics. A summary of this study is depicted in Figure 3-5, with the fourth type (type IV in Figure 3-5) selected as the configuration with the best attributes due to the inherent parallel path configuration obtained with standard half-bridge power modules.

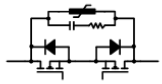
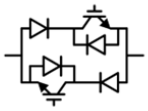
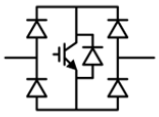
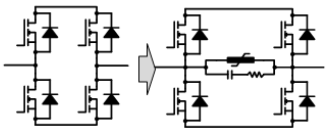
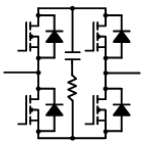
Type I	Type II	Type III	Type IV	Type V
				
Pros • Popular bidirectional SSCB • HW fault - deSAT fault Cons • Needs Energy absorbing and Voltage clamping circuit	Pros • Lower conduction losses with series diode Cons • Needs two more diodes • Needs Energy absorbing and Voltage clamping circuit	• H bridge Pros • Simple operation • Low voltage stress Cons • More conduction losses	H bridge Pros • Bidirectional SW in parallel - Higher current capability Cons • Needs Energy absorbing and Voltage clamping circuit • Unbalanced current • Complicated operation • Trip off timing	H bridge Pros • Double current path • Higher blocking voltage • Energy absorbing Cons • Complicated

Figure 3-5. *Bidirectional Switch Configurations Considered*

While the type IV configuration has the most appealing characteristics to meet the RTAPS program metrics, there also exists many possibilities to arrange the surge arrester and snubber circuitry within topology. As an example, the existence of common source and half-bridge power module configurations means that gate driver and protection circuitry must be different with the identical topology. In this case, both the peak overvoltage, and transient characteristics are the same but the available off-the-shelf availability for the common source approach might be limited despite requiring a lower number of gate drivers.

3.3. Development Strategy

As a strategy to reduce the developmental risk, the buildup of the SSCB is split into three stages: design 0, 1 and 2 or Gen 1-0, Gen 1-1, and Gen 1-2 in reference to the first-generation design from RTX of the SSCB (see performance metrics of Table 1 for reference). On a conceptual level, the Gen 1-0 design enables the development of all the controller software and hardware to start without finalizing the complete design. The next revision, Gen 1-1, uses the power modules intended for the final design, but allows for the characterization of all components and the optimization of the control software with the fabricated test benches. Finally, the last revision, Gen 1-2, has the complete packaged design with all components. This latter revision is the intended design to meet the program metrics listed in Table 2-1. A summary of the various stages of the development strategy is highlighted in Figure 3-6, along with the relevant tests to be completed.

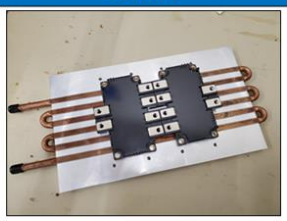
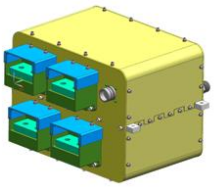
	Gen 1-0	Gen 1-1	Gen 1-2
Overview			
Test items	Test-bed • Risk assessment • Continuous current test set up • SIMENSE SSCB test or custom SSCB • CAP bank and discharge Operation • State machine • DI/DO and signal level	• Hi-pot test • Double-pulse • Thermal characterization • Rated load • Short circuit test • Operation and state machine • Optimized sequence & tradeoff study	• Rated load • Coldplate characterization • Short circuit test • Operation and state machine
SSCB	• Si IGBT 3.3kV, 400A @ full bridge • SiC MOSFET 1.2kV, 1600A @ full bridge	• SiC MOSFET 3.3kV, 1500A @ full bridge topology	• SiC MOSFET 3.3kV, 1500A @ full bridge topology
Normal operation	• Depending on the test circuit	• 1000A, 1.2kV continuous current	• 1000A, 1.2kV continuous current
SC test	• Depending on the test circuit	• 1.2kVdc Cap bank • <3kVpeak, <3kApeak (<100us)	• 1.2kV Vdc Cap bank • <3kVpeak, <3kApeak (<100us)

Figure 3-6. *Three Stages of Development for the RTAPS SSCB Design*

4. SOLID-STATE CIRCUIT BREAKER DESIGN

In this section, the individual component considerations are presented, and the methodology for down selecting each design is detailed. However, considering proprietary knowledge from RTX in aviation SSCB products, all aspects are not covered in this report, i.e., the software, controller board and gate driver designs, and only a focus on those components critical to meeting the performance metrics in Table 1 are covered in detail. Therefore, this section of the report focuses on the cold plate design, snubber and transient voltage suppression circuit, packaging of the Gen 1-2 system, as well as the approach to the current sensor design, the fault current limiter, and the power modules used in the SSCB.

4.1. Selected Power Modules

Simulations of the SSCB operation highlight that even for a DC-bus voltage of 1.2 kV, the transient overvoltage experienced by the composite power semiconductors is on the order of 2-2.5 kV. As a result, the 3.3 kV class of power semiconductors, and in particular, SiC (Silicon Carbide) power semiconductor offer the lowest on-state resistance per unit semiconductor area. After a review of several 3.3 kV SiC power module packages, the FMF750DC-66A was selected from Mitsubishi Electric as the leading candidate for the SSCB, with the package and layout shown in Figure 4-1.

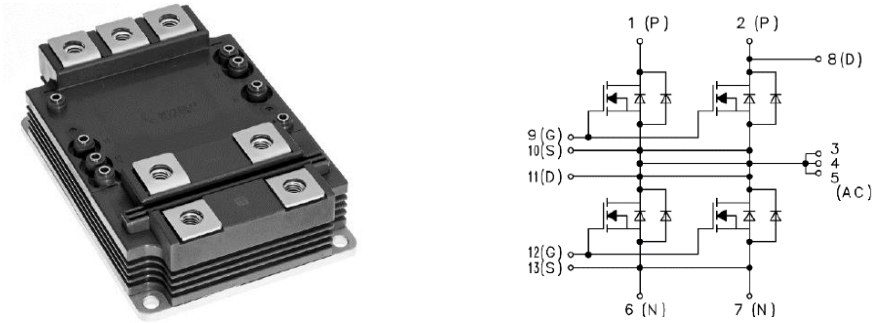


Figure 4-1. *FMF750DC-66A Power Module Package and Circuit Diagram*

Critically, the static on-state losses are associated with the average efficiency of the SSCB, as the load current passes through two series connected components in the selected topology. Note that in the typical bi-directional configuration, one switch is reversed in orientation, but owing to the 'third quadrant' operation of a MOSFET, wherein a negative current can be conducted through the channel of the device with a positive gate voltage, the effective voltage drop is effectively two devices in series. Consequently, as under the selected topology two half-bridge power modules enable two parallel current paths, four SiC MOSFETs are active during normal conduction of the SSCB. Using the on-state resistance as a function of temperature, the total losses are therefore calculated in Figure 4-2. Considering the additional lead resistance due to the package, a maximum junction temperature of $160°C$ is still within the loss target envelop required to meet the efficiency specification highlighted in Table 2-1.

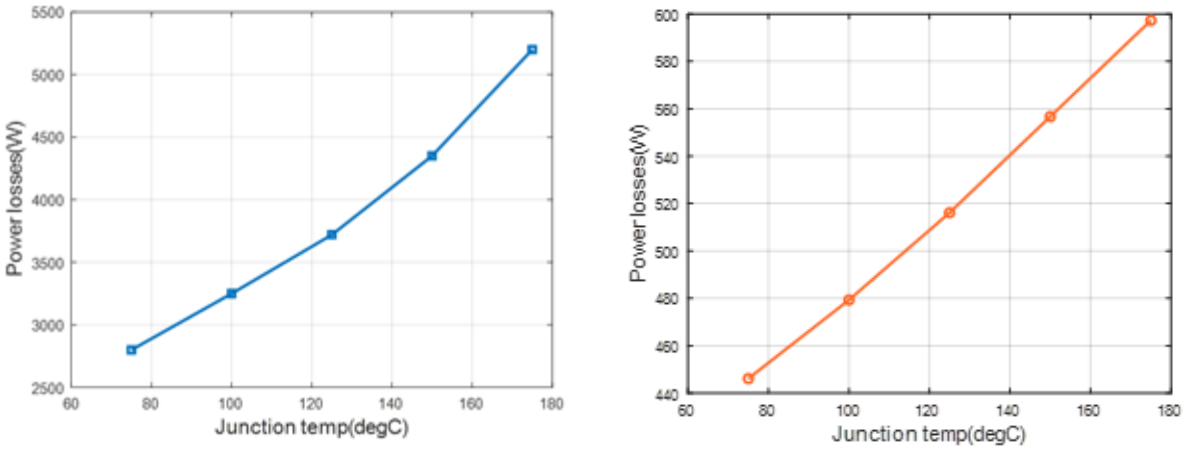


Figure 4-2. *Total Semiconductor Loss (Left) and Terminal Loss (Right) as a Function of Temperature*

Using a fixed temperature reference of $70°C$ to represent the cold plate surface on the underside of the 100um thick thermal interface material ($\lambda = 1W/mK$), the die temperature distribution is calculated using a thermal FEA simulation, as shown in Figure 12. The peak surface temperature under the peak loss condition from Figure 4-3 is less than $140°C$ – indicating that the peak junction temperature is likely even lower due to the average value that this quantity represents in the power semiconductor terminology. Thus, the selected topology and power module have a safe margin of at least $35°C$ duing the worst-case thermal loading, and an estimated efficiency to be above 99.5%, assuming a coolant temperature of $50°C$.

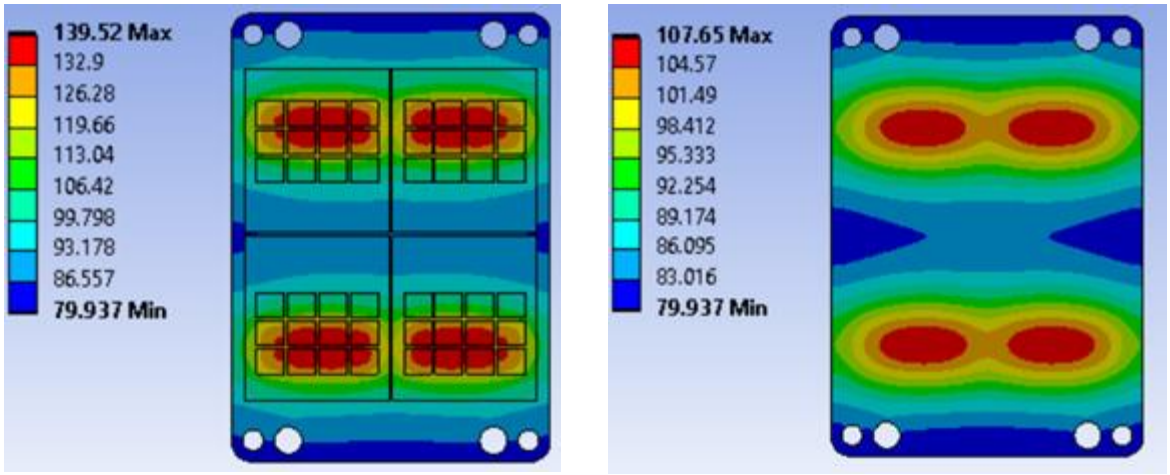


Figure 4-3. *Temperature Distribution Under Worst Case Loading: Die Side (Left), Baseplate (Right)*

4.2. Snubber Circuitry and Transient Overvoltage Suppression

As highlighted in Section 3.2, the energy absorption circuitry and overvoltage suppression elements provide a critical means of de-energizing the stored energy due in the grid inductance. As each component begins to operate during specific moments during the breaking or transient period of the SSCB operation, the layout and design of each component is critical. Further, while metal-oxide varistors are a popular choice for overvoltage suppression, a semiconductor based transient voltage suppression (TVS) diode is utilized instead due to the latter component's high repeatability without degradation.

A combination of a RC snubber (resistor/capacitor) and a TVS diode network form the basis of the clamping and energy absorption approach for the SSCB. While each component can also perform the role of de-energizing the source/load inductance within the network during a fault, the combination of the two leads to the lowest overvoltage, with an acceptable compromise on the fault clearing time, as highlighted in Table 4-1. An electrical schematic of the combined snubber and TVS circuit is shown in Figure 4-4.

Table 4-1. *Comparison of Snubber/TVS Combinations*

Circuit	Topology	Positives	Negatives
CON1	TVS	Lowest TVS energy, footprint, current rating, and fault clearing time	Largest V_{pk}, dV/dt
CON2	Subber	No TVS, lowest dV/dt	i_{pk} is 2x higher, lossy, slowest, and largest volume
CON3	TVS+Snubber	Lowest V_{pk}, medium fault clearing, i_{pk}	Most parts, somewhat bulky

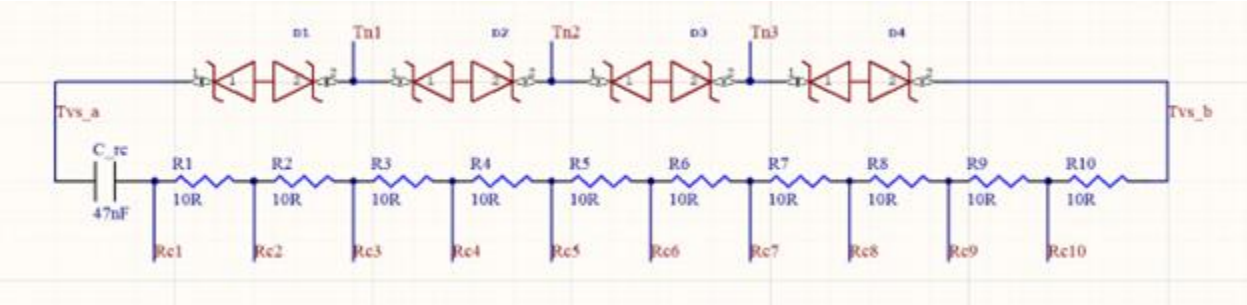


Figure 4-4. *Electrical schematic of the TVS and Snubber Circuits for the SSCB*

However, to minimize the peak overvoltage (which occurs when the SiC MOSFETs have turned off and the snubber circuitry have taken the fault current over), the parasitic inductance between all components must be minimized. Within the context of the project, multiple revisions of the TVS/Snubber board occurred, beginning with the layout in Figure 4-5, which was analyzed in ANSYS Q3D and determined to have a loop inductance of approximately 10.3 uH. Consequently, the distance between the TVS diodes was revised, reducing the stray inductance by a factor of 50% and resulting in the layout shown in Figure 4-6.

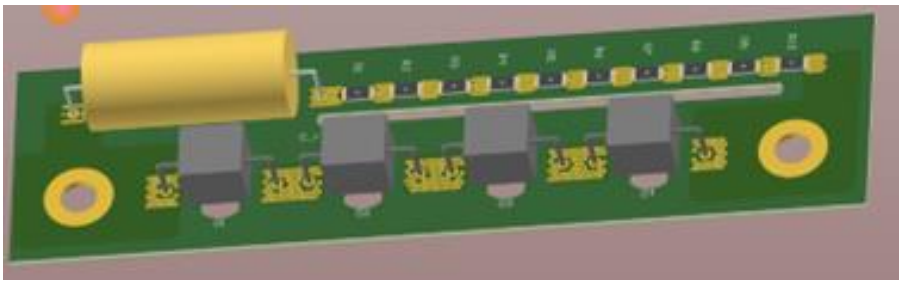


Figure 4-5. *Initial Design for the TVS/Snubber Board*

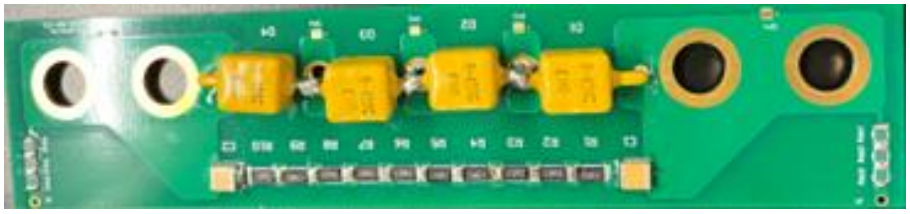


Figure 4-6. *Final Design of the TVS/Snubber Board*

4.3. Fault Current Limiter

One of the least power dense items within a SSCB is the fault current limiter (FCL), as these are typically passive elements designed to reduce the current rise time during a fault. Therefore, meeting the specific power density specification as per Table 2-1 requires careful consideration of the fault current limiter design in the context of the worst-case grid inductance.

In the initial analysis, a maximum response time of the SSCB was estimated as 10 us with a negligible system inductance, i.e., the fault current limiter would be required to provide all of inductance to limit the current rise time, resulting in a required inductance value of 10 uH. The project therefore focused on the design of a lightweight fault current limiter using an air-core design integrated into the SSCB package, as per Figure 4-7. However, given the weight of copper and required number of turns to achieve 10 uH is at least 11 kg, meeting the objective power density target for the SSCB would therefore require significant compromise to the other aspects of the circuit breaker design. Considering this conclusion, the team focused on optimizing the minimum protection time with the selected control system components and the additional minimum required inductance to achieve the target grid inductance of 10 uH.

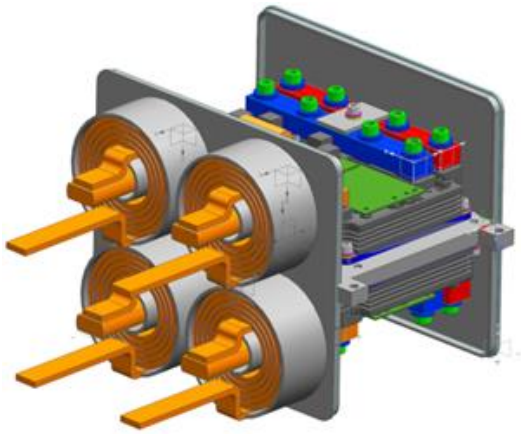


Figure 4-7. *Initial SSCB Concept with Integrated Fault Current Limiting Inductance*

Starting with the entire signal chain and breaking down each component from current sensor to the controller interface logic to the gate driver, the median delay from each component datasheet was used to calculate the total delay time, as per Table 4-2. In this case, it is calculated that the median delay time for the protection circuitry is roughly 3 us vs 10 us as originally estimated. Further, as the SSCB is not directly installed within the battery system or at the source/load itself, some cable distance is naturally present in the system. Using an approximation of the incremental inductance of 20 nH/cm, a rough estimation of 6 uH is obtained with 1.5m cable length on either side of the SSCB. Lastly, given the reverse-bias safe operating area of the selected SiC MOSFETs is safely over 3 kA the total required inductance for safe operation can be met with 6 uH – requiring no additional inductance. An illustration of this study is shown in Figure 4-8, where only the case requiring a peak current of less than 2.5 kA results in the requirement of an additional inductance in the SSCB. Thus, the SSCB can achieve safe fault current limiting values because of the low delay time circuitry selected and the natural cable inductance of the SSCB within the system.

Table 4-2. *Delay Time Calculation for the Protection Circuitry*

		Delay	Notes
Gate driver	Propagation	0.05 us	
MOSFET	Turn off delay time	1.3 us	Turn-off delay time + Turn-off fall time
Current sensor	SSA-1000	1.6 us (expected)	Reaction time (50% rise in input to output)
	RAZNC-305xUNF	1.5 us (expected)	Rise time + 1st order RC filter emulating BW
	Rogowski + Interface	0.2 us (expected)	Designed, need to be validated
Interface delay	Buffer logic	0.13 us	Logic: Comparator + Buffer
Maximum anticipated delay		**3.08 us**	Summation using max of the current sensors is selected

	Case 1	Case 2	Case 3
DC voltage	1200 V	1200 V	1200 V
Trip current	2000 A	2000 A	2000 A
Peak current	3000 A	2700 A	2400 A
Delay time	3.08 us	3.08 us	3.08 us
Needed	3.7 uH	5.3 uH	9.3 uH
External	-	-	3.3 uH

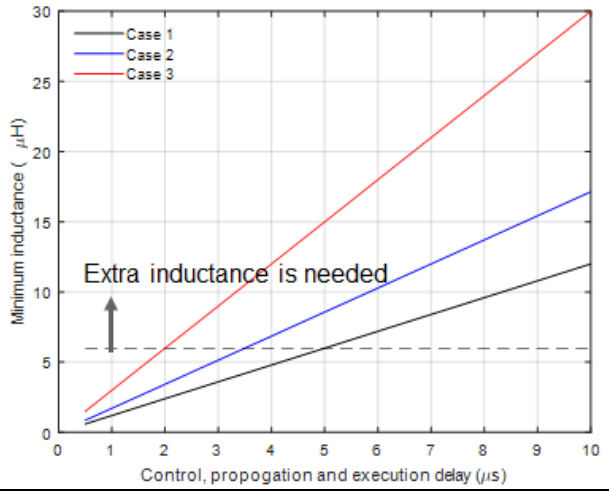


Figure 4-8. *Protection Delay and Required Inductance Due to SSCB Cables*

4.4. Current Sensors

The current sensors represent one of the most critical elements of the SSCB, as they are required to not only sense the DC current but provide fast response to any fault condition with a high degree of precision. In addition, the size and weight of the current sensing option must be minimal – thereby eliminating many traditional hall-effect based current sensors. To meet the weight, and performance requirements of the SSCB, three technologies were evaluated: Rogowski coil sensor, shunt resistor, and a proximity-based hall effect sensor, as shown in Figure 4-9.

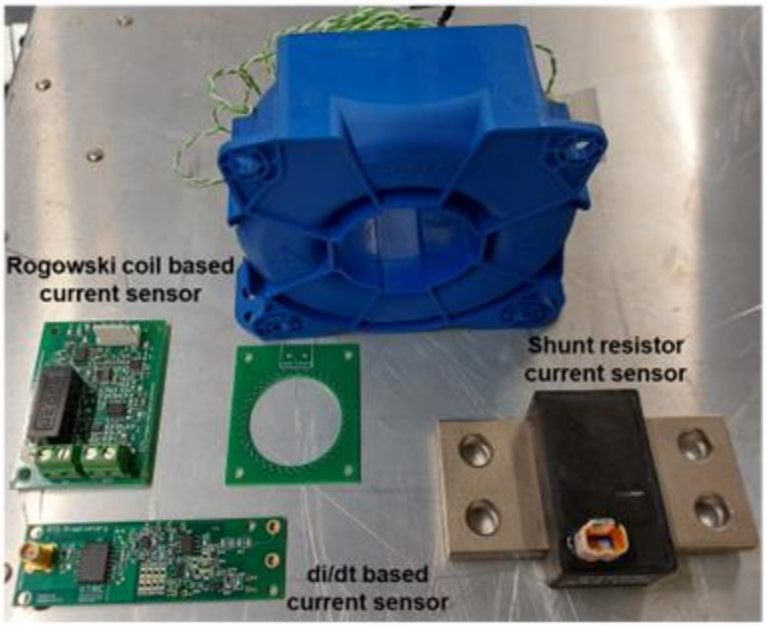
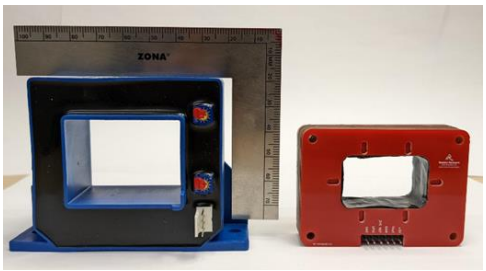


Figure 4-9. *Initial Current Sensors Considered*

Under the initial evaluation, the off-the-shelf Rogowski coil demonstrated the best performance during a fault event, but the size and lack of DC current detection removed it from consideration. The shunt based current sensor on the other hand had significant distortions during positive di/dt and negative di/dt periods due to the stray package inductance, as well as an initial delay compared to the other sensors considered. To capture the DC component of the SSCB current then, a compact coreless Hall effect sensor was fabricated by Raztec, with the result compared to a traditional hall effect current sensor in Figure 4-10. In this case, not only is the solution smaller by a factor of 5 compared to the LEM current sensor, but the upper frequency limit is improved by 8 times with a higher temperature rating.



Parameter	LEM HAT 1000-S	Raztec RAZNC-305xUNF
Primary current range [pk-A]	±2500	±3000
Typical supply voltage [V]	±15	5.0
Typical supply current [mA]	±20	100
Frequency bandwidth [kHz]	DC..25	210
Volume [L]	0.26	0.05
Mass [g]	300	72
Rise time	< 5 us (0 to 90%, di/dt = 50A/us)	1 us (0 to 1000AT)
Primary conductor window	30 mm x 40 mm	33 mm x 20 mm

Figure 4-10. *Current Sensor Comparison (LEM and Raztec)*

Unfortunately, the rise time of the fault current can exceed the custom packaged Hall effect current sensor. Thus, to capture the DC to 10 MHz current information, a Rogowski coil output and the Raztec current sensor are used in tandem to provide the current feedback to the SSCB. In this case, the Raztec current sensor provides the low frequency bandwidth, and a custom Rogowski coil provides the bandwidth

up to 10 MHz. To meet the packaging requirements from the SSCB, the Rogowski coil underwent multiple iterations ended with a rectangular design, as will be elaborated upon in later segments of this report. A sample of the combined current sensor output is shown in Figure 4-11 with the custom designed Rogowski coil and Raztec hall-effect sensor.

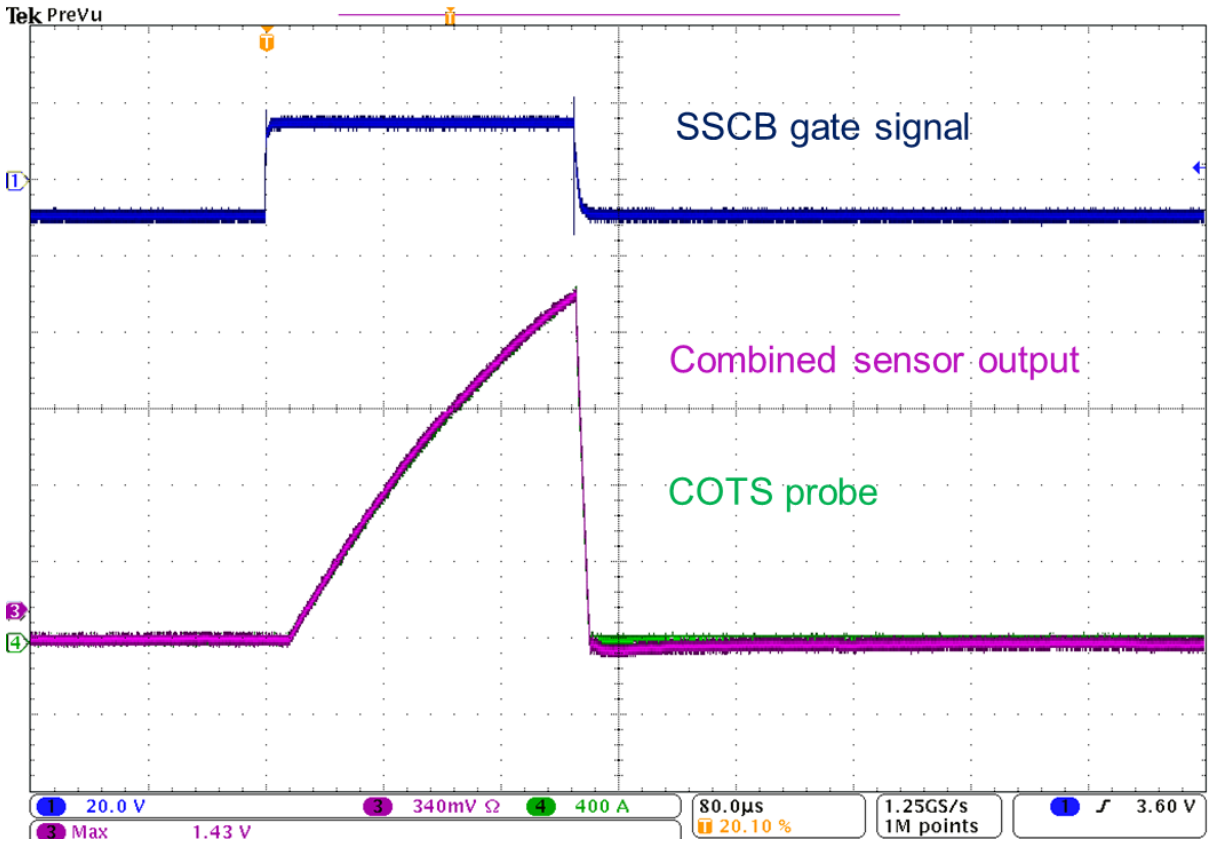


Figure 4-11. *Sample Current Waveform Under a Fault Current (Combined Raztec and Rogowski Coil Output)*

4.5. Additive Manufactured Cold Plate

The cold plate provides cooling to the 3.3 kV SiC MOSFET power modules and forms a key component in the structure integrity of the SSCB. Further, owing to the high specific power density target of the project, the internal current carrying busbars have the potential to produce significant internal heat, thereby requiring direct cooling to meet the internal temperature requirements of the components. While the RTRC team has extensive experience in the design of custom machined cold-plates, the significant thermal constraints on the SSCB due to the power modules and internal bus-bar bars necessitated the move towards additive manufacturing (AM) technology using a custom working material.

Based on the thermal loading of the power modules, the cold plate design was optimized and analyzed to understand the thermal performance. A pin design was developed based off the expected thermal gradient across the cold plate and the flow rate. Denser fins are located near the outlet port of the cold plate, allowing for an ideal thermal balance in the power modules based off the flow rating modelling, as illustrated in Figure 4-12.

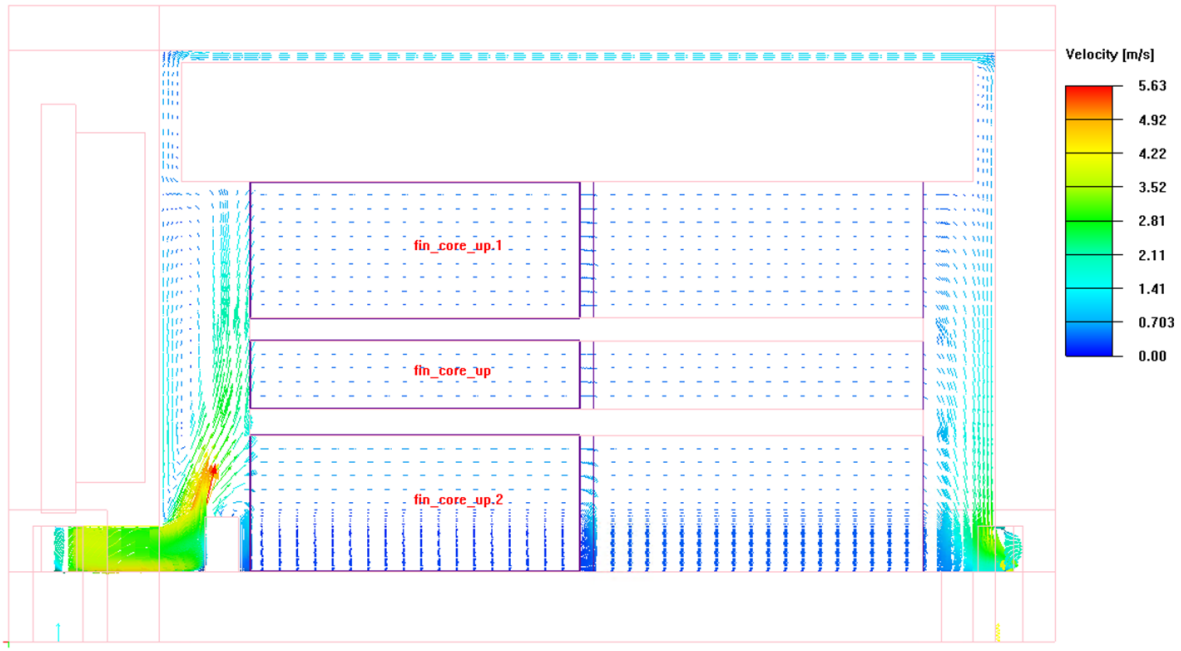


Figure 4-12. *Flow Rate Modelling to Ensure Thermal Balance for the AM Cold Plate*

4.6. Packaging Design

Integrating all the components together is the package, which also must manage interconnections between the power, cooling, and signal interfaces. The housing design approach is derived from a standard practice within Collins Aerospace for in-service power electronics. The SSCB cold plate serves as the central backbone to the assembly, with the power modules for the positive and negative lines on the top and bottom. The top and bottom covers are all formed from aluminum, with the electrical input/output on the front of the housing and the fluid connections on the rear, as per Figure 4-13. The cover gage is selected as a compromise between durability and weight, based on internal company experience. Finally, the controller card, as shown in Figure 4-13, provides a common point of access for both the positive and negative circuit breaker components, with the mounting considered to minimize the impact of vibrations.

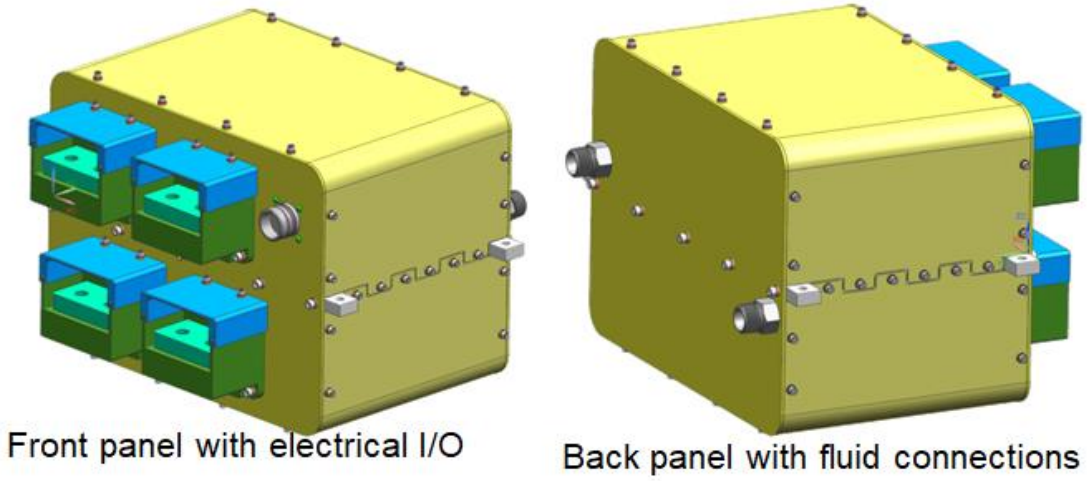


Figure 4-13. *Final Design of the SSCB Package*

The terminal blocks, shown in Figure 4-13, are made from dielectric material (a type of plastic), with a nut plate within each block to clamp the aircraft busbars onto the SSCB terminals. These terminal blocks are designed to provide the appropriate voltage spacing, clamping force and protection against inadvertent contact. The voltage clamping circuitry are mounted near the terminal blocks to minimize the total distance to the input busbars, thereby minimizing the parasitic loop inductance and the possible overvoltage during a fault breaking event. Within each terminal block region, the current sensors are also mounted to minimize the wire length within the SSCB and total weight associated with the feedback circuitry. Finally, the system package is depicted in Figure 22. Note that the initial weight of 13.3 kg was based on estimates, and post-build, the Gen 1-2 package weight is 11.5 kg due to housing/cold plate modifications – allowing the SSCB to meet the >100 kW/kg specification.

5. CHARACTERIZATION OF THE SSCB

With the major components of the SSCB detailed in Section 4, this Section describes the build-up of the fault current test bench, as well as the electrical characterization of the SSCB. Further, individual component testing, i.e., the pressure testing of the cold plate, as well as additional modelling for the design of the SSCB, is also described for the sake of completeness.

5.1. Thermomechanical Modelling

As a further step to de-risk the buildup of the SSCB package prior to fully loading the design, a detailed thermal model of the system was developed. Beginning with the cold plate and the associated fin design, Figure 5-1 highlights a balanced thermal profile of less than 1% difference across the two power modules. Consequently, under the static loading of the SSCB, the loss profile is also expected to be balanced, and the efficiency maximized (as the SiC MOSFETs have a resistive on-state characteristic) due to this balanced thermal loading within the SSCB.

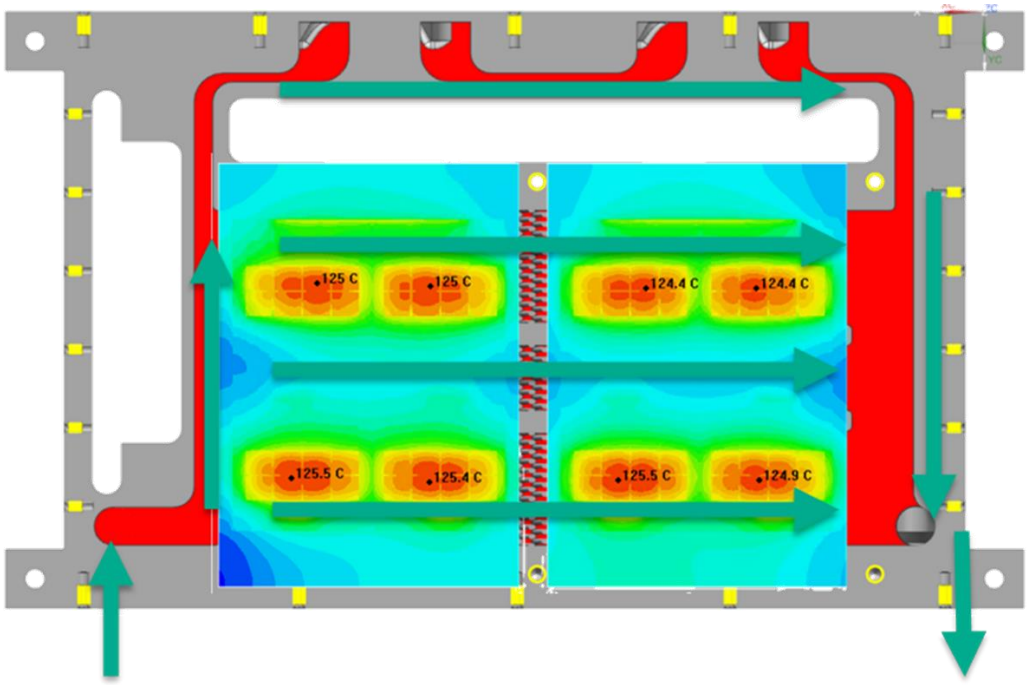
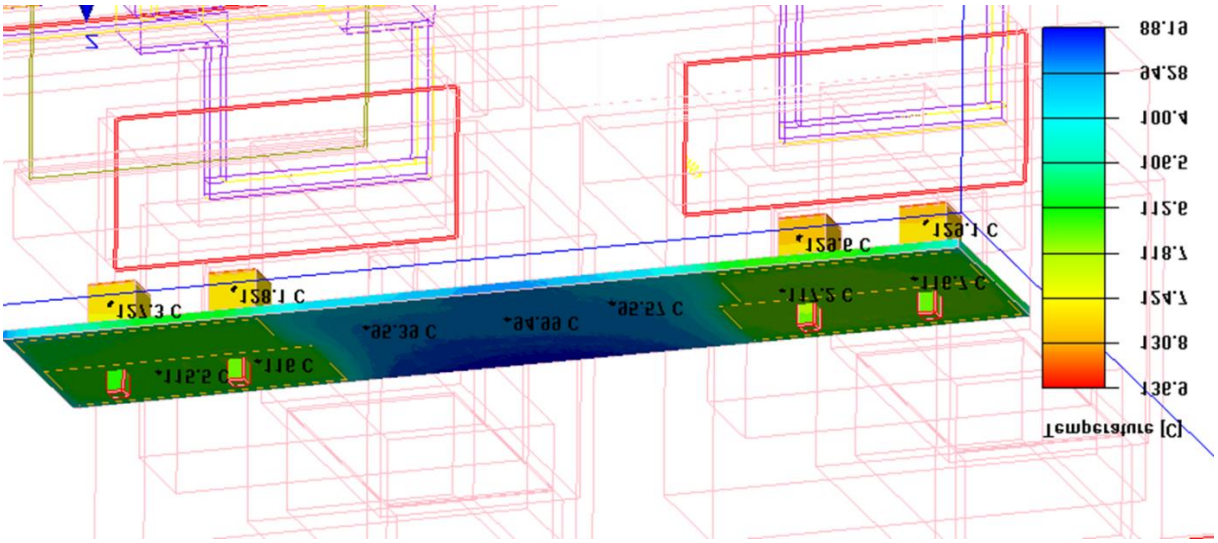
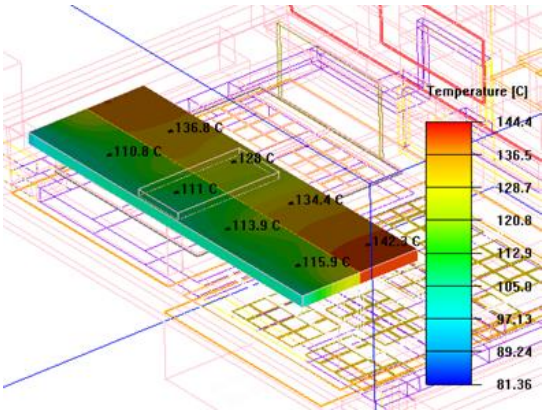


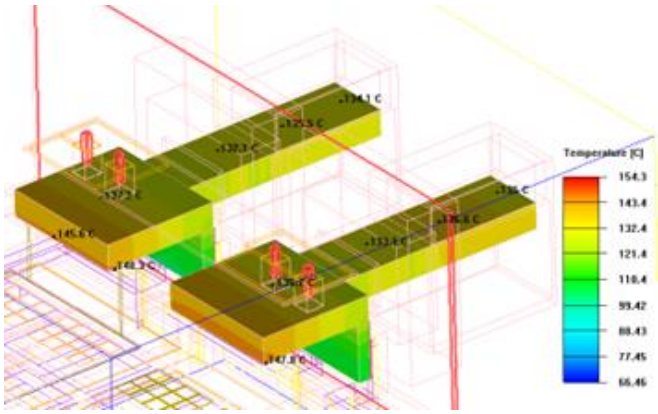
Figure 5-1. *Thermal Modelling of the Cold Plate Under a Fixed Load*

Outside of the cold plate, three additional components are modelled under simulated full loading and a coolant temperature of $70°C$ while placed within the SSCB: the TVS circuit, output bus bar and the internal power module busbar. The maximum temperature of $100°C$ experienced by the TVS board is located at the bolted joint, as per Figure 5-2, allowing for a margin of at least $25°C$ on the circuit board. As the input busbar not only contains the connection to the power module, but also a close thermal contact with the current sensors, the thermal modelling of the input busbar is critical for long-term reliability. Assuming no internal heat-exchange, i.e., a closed box, the maximum input bus-bar connection is calculated to be $154°C$, with the power module busbar at $144°C$, as per Figure 5-2.



TVS Board





Internal Bus-Bar Input Bus-bar

Figure 5-2. *Thermal Modelling of the Internal SSCB Components*

5.2. Dynamic Test Bench Build-Up

The SSCB acts as a pass-through element during normal operation and is required to interrupt the load current at rated conditions in under 100 us, as per Table 1. Accordingly, a test bench is required to be able to bias the SSCB at the rated voltage of 1.2 kV and supply up to 3 kA to emulate the fault interruption operation. Further, this test must be completed with little to no deviation of the input DC bus, as the battery emulated acts as an invariant DC source to the load.

An electrical schematic of the designed dynamic test bench is shown in Figure 5-3, with the electrolytic capacitor bank specified to maintain a voltage deviation of less than 1% over 100 us at an average of 1.5 kA. The input of the DC capacitor bank is controlled by a 1.6 kV, 400A DC power supply located in the RTRC ‘high power system testing’ laboratory. A contactor is added for safety to enable a redundancy of isolation for the high-power supply. A series IGBT (3.3 kV/1500A) from Infineon was used to provide a second order safety turn off ability and fault protection in case the SSCB was unable to turn off. A picture of the test bench without the safety cover is shown in Figure 5-4 with the Gen 1-1 prototype installed.

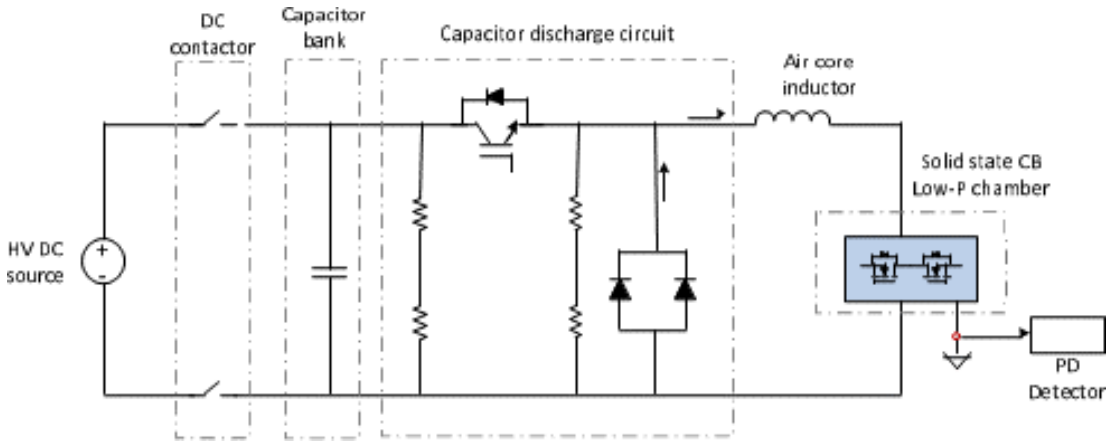


Figure 5-3. *1Electrical Schematic of the Dynamic Test Bench*

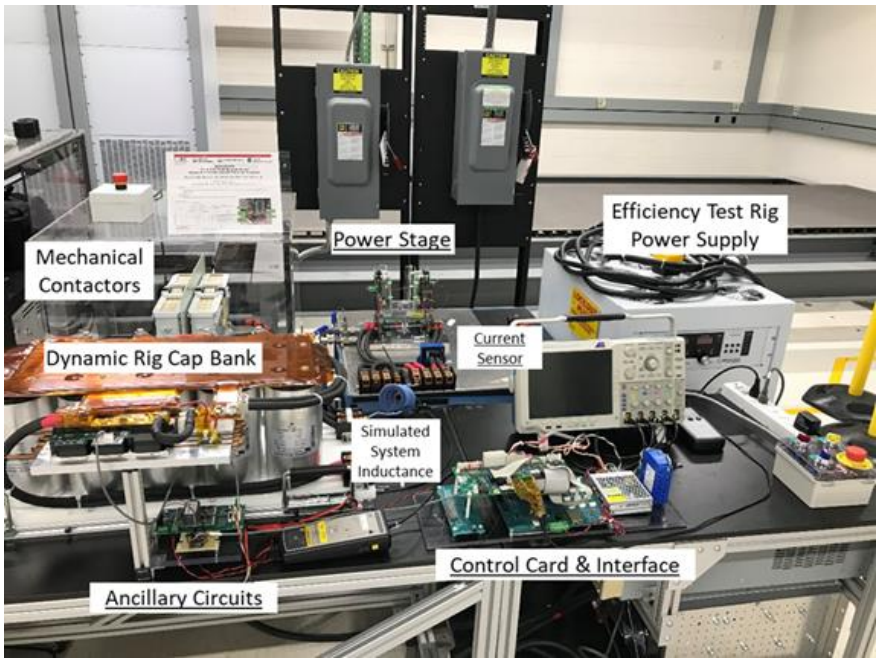


Figure 5-4. *Dynamic Test Bench to Emulate Fault Currents*

5.3. Final Build of the SSCB

The fabrication of the Gen 1-2 prototype of the SSCB occurred over the latter half of 2022. Of note, the cold plate with the applied dielectric coating but without mounted power modules, with the input busbar and integrated current sensors shown in Figure 5-5. Finally, it is important to note that the final weight of the packaged SSCB is 11.5 kg, as optimizations were made in the package material, cold plate, and boards to save 1.5 kg over the original estimated weight. This final weight was confirmed via scale in the lab. At first each part was weighed independatly and compared back to the original estimated mass, with the final mass being weighed after assembly.

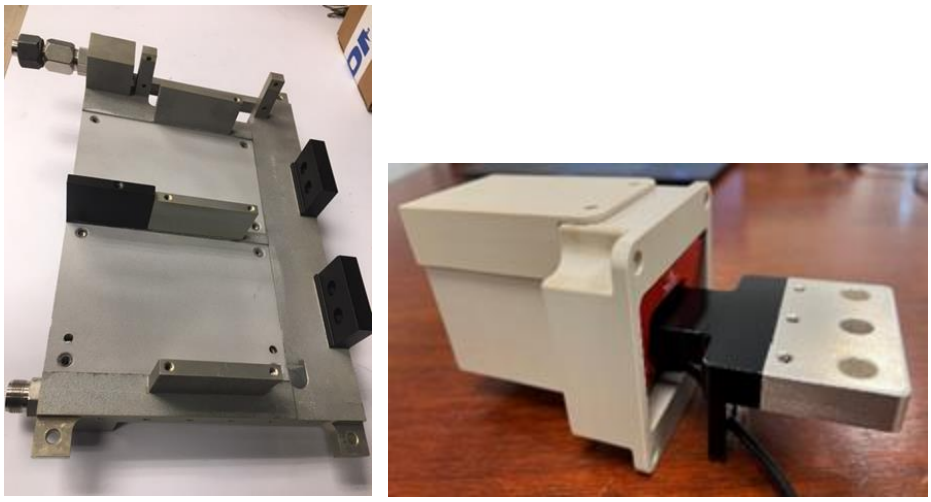


Figure 5-5. *Cold Plate without Power Modules (Left) and Input Busbar with Integrated Hall Effect Sensor (Right)*

5.4. Cold Plate Pressure Testing

Prior to the assembly of the SSCB, the fabricated cold plate was tested to verify the maximum pressure drop as a function of flow rate. In this test, the cold plate was first pressurized to 70 psig and left overnight to ensure the fabrication is leak free. The cold plate was then run in a cooling loop depicted in Figure 5-6, and the differential pressure was monitored as a function of the flow rate, as shown in Figure 5-7. Two coolant temperatures of $30°C$ and $50°C$ was used to observe the impact of abolute pressure on the pressure drop across the cold plate with variable flow rate, and the result is compared against a CFD model at $50°C$, as per Figure 5-8. The observed different between the number and experimental results are minor, indicating the cold plate behaves as the team predicted.

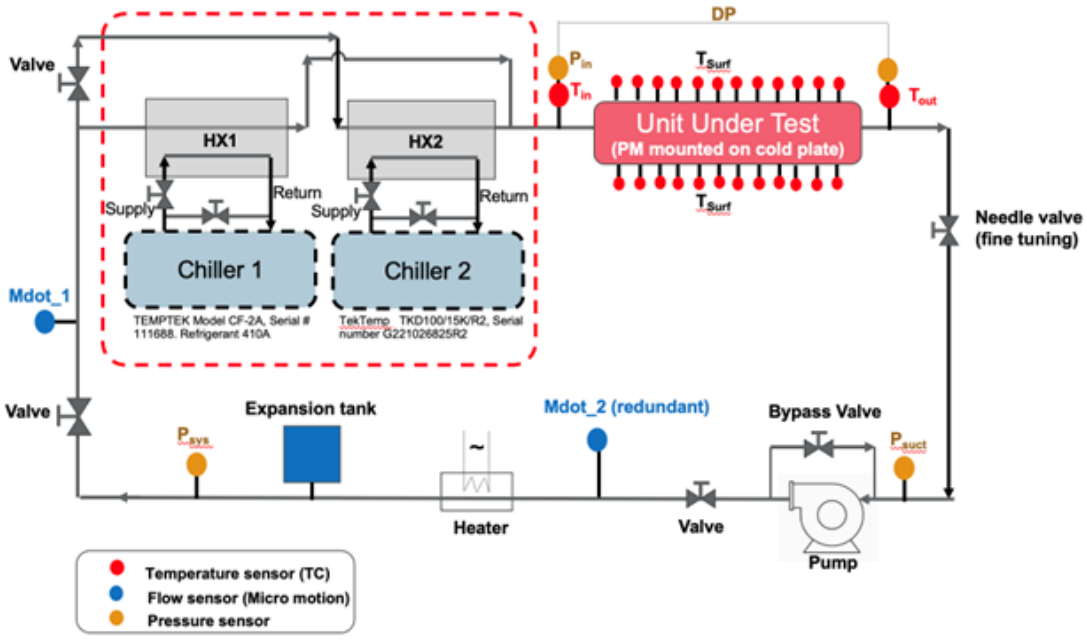


Figure 5-6. *Cold Plate Characterization Set-up*

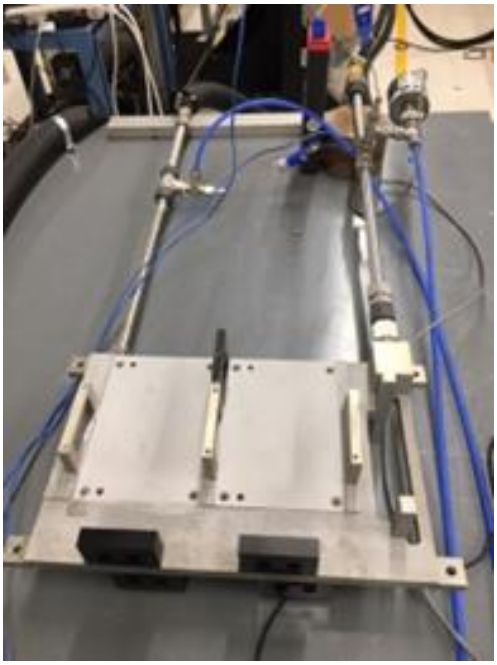


Figure 5-7. *Differential Pressure Monitoring of the Cold Plate*

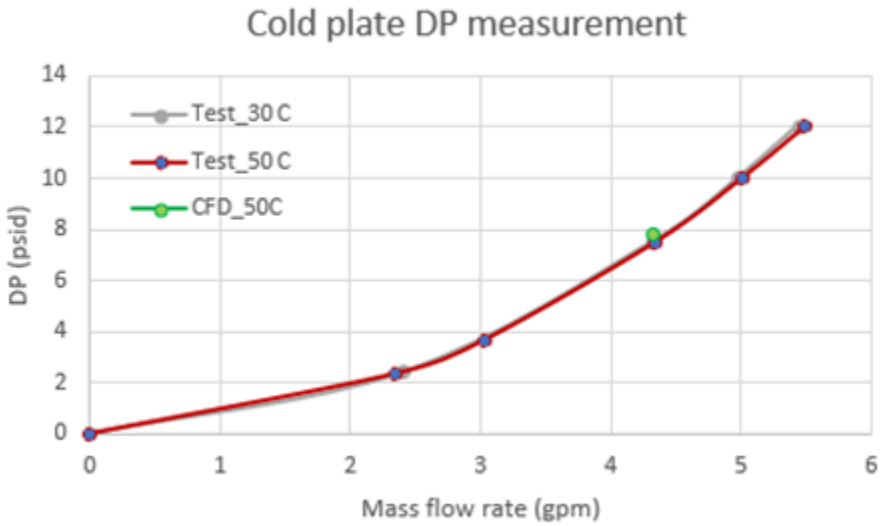


Figure 5-8. *Experimental vs. Predicted Pressure Drop vs. Flow Rate*

5.5. Electrical Characterization

Two qualities make up the electrical characterization tests for the SSCB: interconnection resistance and the isolation resistance (or dielectric breakdown).

5.5.1. Interconnection Resistance

Owing to the high magnitude of current that flows through the SSCB during steady state operation, the interconnection resistance is not only critical to achieve the rated efficiency, but also safe operation. Two specific interconnection resistances are measured to ensure low path resistance is ensured: the power

module terminal and the bus-bar terminal, as shown in Figure 5-9. To measure the ultra-low values of resistance, a microohm meter (DRL010HDX) is employed.

Measuring the two identified resistances requires a back substitution of two measurements. The first step is to calculate the contact resistance between the power modules and input bus-bar by measuring the total resistance from one side to the next ($2.655\ m\Omega$). This bus-bar is then removed, and then the power module connections at these points is measured ($2.638\ m\Omega$), allowing the contact resistance with the bolts to be measured ($5.5\ u\Omega$). Individual measurements were then made from the DC+ (P) or DC-(N) terminal to determine that each DC bus bar is $98 - 118\ u\Omega$.

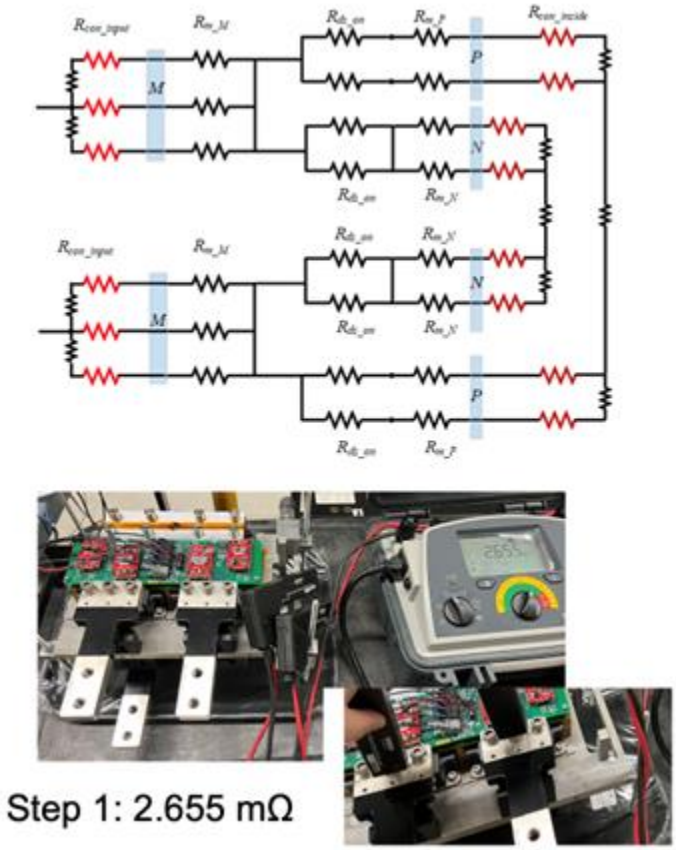


Figure 5-9. *Sample Measurement (First Step Shown) of the Contact Resistance within the SSCB*

5.5.2. Dielectric Testing

To ensure that there is no insulator failure due to creepage/clearance distances within the compact SSCB, a high-potential insulation was performed. In this test, both the DC+ and DC- terminals were measured relative to the cold plate, which was grounded as in the application. The insulation testing procedure involves slowly ramping the applied DC voltage from 1 kV to 5 kV, after which this voltage is held for approximately 1 minute. After this time, the leakage current is measured and compared against a critical value (1 mA), and the test is considered a pass if the leakage current is below this threshold value. Note that this testing level of 5 kV is defined by the International Electrotechnical Commission (IEC) and is 2x the peak voltage experienced during fault interruption by the breaker. Both connection configurations had negligible leakage current detected, giving the measurement shown in Figure 5-10.

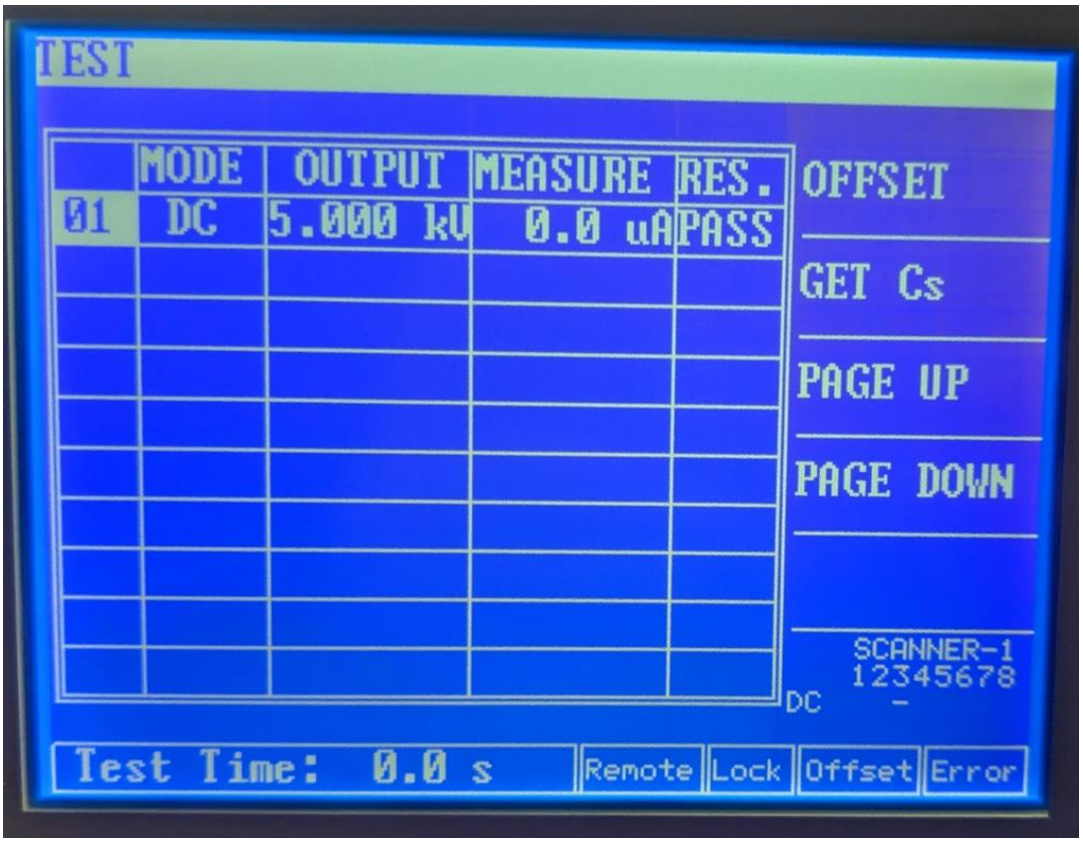


Figure 5-10. *Dielectric Testing (DC) Results*

5.6. Power Module Partial Discharge Testing

Partial discharge (PD) is the gradual insulation breakdown by small electrical discharges that occur over time under high electric fields. The Mitsubishi Electric power modules used in the SSCB are engineered to provide 6 kV of isolation, with an estimated partial discharge inception voltage of 2.6 kV rms at ground level. These power modules are specifically designed for utility or traction converter applications and are not designed to achieve rated conditions at 38 kft, as required in this project. Nevertheless, as no market ready solution exists in the 3.3 kV power module class for aviation applications, there exists some ambiguity as to how the selected power modules behave in terms of PD characteristics during operation. Specifically, there is an open question as to what the PDIV rating of the power modules is reduced to at 38 kft, and how the specific operating profile impacts the PDIV of the power module. To gain a better understanding of the power module PDIV characteristics, the team collaborated with the Ohio State University (OSU), which has the capability of testing the power modules under high altitude emulated conditions with complex profiles.

Beginning with the standard 60 Hz IEC tests, highlighted in Figure 5-11, two power modules were characterized at ambient temperature and pressure, i.e., standard altitude pressure (SAP), and compared against the PD characteristics obtained at the 10 kPa, equivalent to 50 kft (stretch condition from Table 2-1). This test was repeated for 5 times per power module, and the resultant PD inception and extinction voltages (PDIV and PDEV) are given in Figure 5-12. Consequently, based on the standard 60 Hz profile, the PDIV drops from 3.6 kV peak to 1.02 kV and 1.12 kV for the two power modules tested.

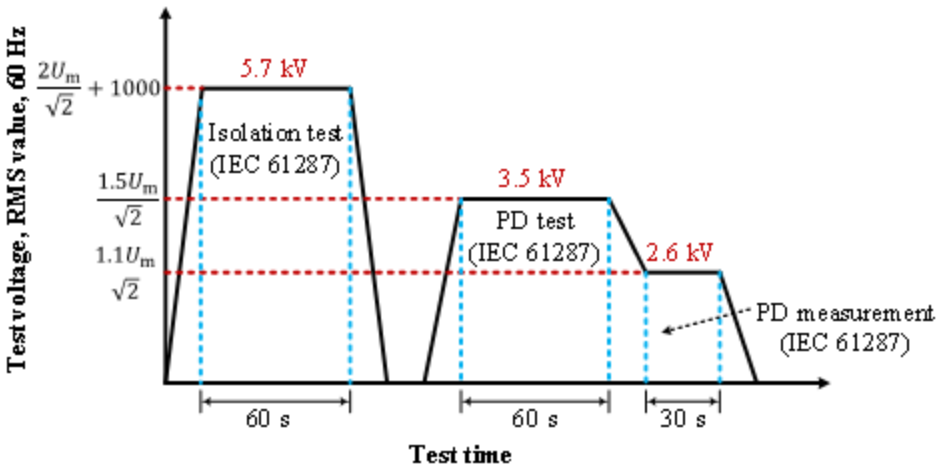


Figure 5-11. *Test Procedure per IEC 61287*

Sequence	1	2	3	4	5	Average
PDIV (kV)	1.15	1.02	0.99	0.97	0.97	1.02
PDEV (kV)	0.91	0.86	0.75	0.85	0.85	0.84

Sequence	1	2	3	4	5	Average
PDIV (kV)	1.51	1.01	0.98	1.09	1.13	1.14
PDEV (kV)	0.85	0.85	0.83	0.92	0.85	0.86

Figure 5-12. *PDIV/PDEV Measurements for Two Power Modules Under the IEC 61287 Testing Procedure at 50kft*

Moving to more application representative tests, a high dV/dt test bench was used where a 10 kV SiC power module applies a pulse voltage waveform to the device under test (DUT), as per Figure 5-13. In this case, traditional PD detection methods are not applicable as the discharge of the parasitic capacitance at the DUT node masks any PD. Therefore, a high frequency current transformer (HFCT) is used in conjunction with a UHF antenna (290 MHz to 3 GHz bandwidth) and photomultiplier tube (PMT) to detect high frequency discharges within the DUT. As a consequence of these additional detectors, the DUT is placed under an optical cloak, and within a Faraday cage, as shown in Figure 5-13. Further, the DUT is placed within a pressure chamber to emulate the high-altitude conditions, also illustrated in Figure 5-13. In the test sequence for the application representative tests, the applied voltage is gradually increased to 5 kV, with the pulses repeated 10 times to ensure that PD, if present, has a higher probability of being captured.

During the testing, the DUT is subjected to two different rise times, 70 ns and 215 ns, with a maximum pulse width of 100 us. In this test, the maximum dV/dt experienced by the DUT was more than 20 kV/us, like the turn off speed of the SSCB, but none of the PD detection equipment indicated the presence of PD. Only the HFCT detected the discharge of the parasitic capacitance during this test. An illustration of the pulse applied to the DUT, and HFCT measurement is shown in Figure 5-14, with the dV/dt pulse zoomed in for the right-hand side of Figure 5-14. Owing to the lack of PD detected, the pulse-width duration is increased by 10x to 1 ms under the assumption that the energization time is insufficient to establish PD within the power module. However, in this case too, no PD is detected, as shown in Figure 5-15. Thus, while the high-altitude validation of the SSCB is required as part of the validation, attempting to characterize the PD under emulated conditions within the breaker were unable to produce PD.

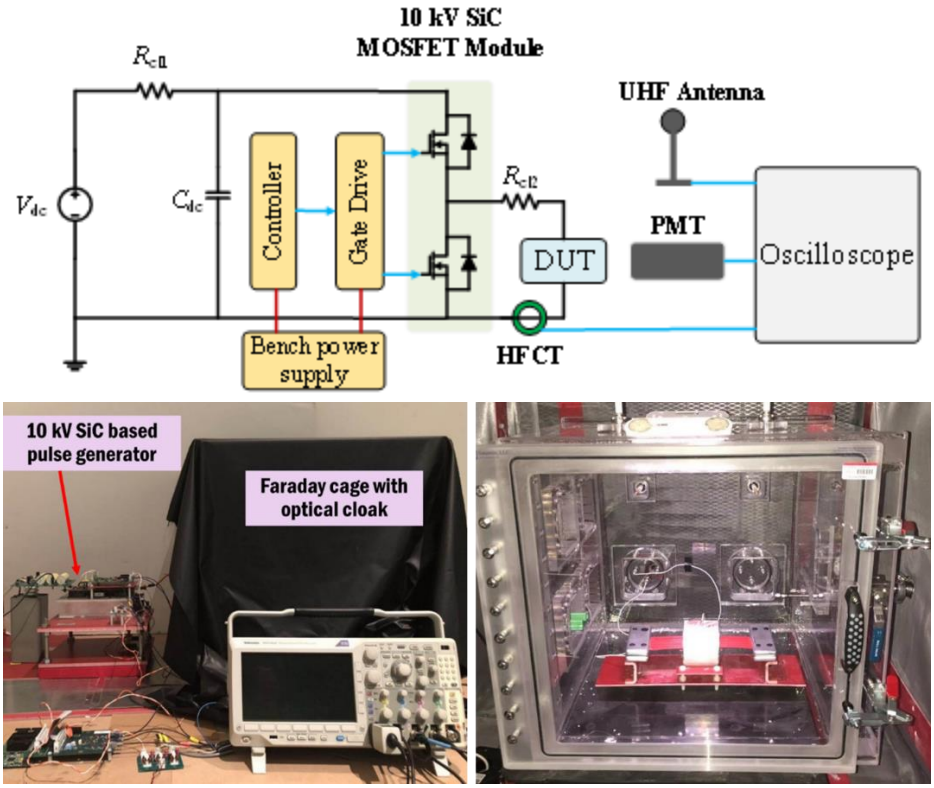


Figure 5-13. *10 kV Pulse Generator for DUT (Above), Faraday Cage/Cloak for DUT (Left), and High-Pressure Chamber (Right)*

Figure 5-14. *5 kV, 100 us pulse on DUT (left), and zoom on voltage edge (right)*

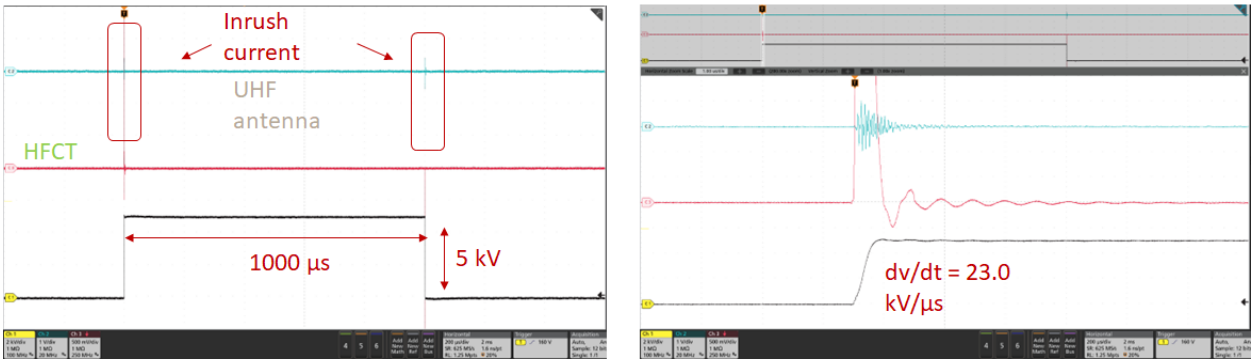


Figure 5-15. *5 kV, 1 ms pulse on DUT (Left) and zoom on voltage edge (Right)*

6. EXPERIMENTAL VALIDATION

With the design covered and the major component characterization detailed in the previous sections, this section highlights the validation testing of the SSCB to ensure compliance with the program specifications as per Table 2-1. Thus, to validate these specifications, this section covers two tests: static efficiency test with temperature validation, and the dynamic breaking test under ambient and emulated high-altitude conditions.

6.1. Static Loading Test

Fundamentally, circuit breakers are required to have as minimum loss as possible to ensure high efficiency across the entire distribution system. In this case, a single side of the SSCB is specified to reach a target of greater than 99.5%, or a total loss of less than 6 kW at rated conditions with an inlet coolant temperature of $50°C$. In the static loading, or steady-state thermal test, a continuous DC current is therefore applied to the SSCB and the resultant losses are measured to ensure that the specifications of Table 2-1 are met. The primary objective of this test is to evaluate the cold plate cooling performance and assess the power efficiency of the packaged Gen 1-2 SSCB. As in the case of the cold plate characterization test, the cooling test setup in Figure 6-1 is employed with a DC power supply set to constant current mode to regulate the loading current. A picture of the SSCB within the coolant loop is shown in Figure 39, with the most significant components labeled. Approximately 20 thermocouples were installed in the SSCB – ranging from the busbars, power module baseplates to various spots within the system package.

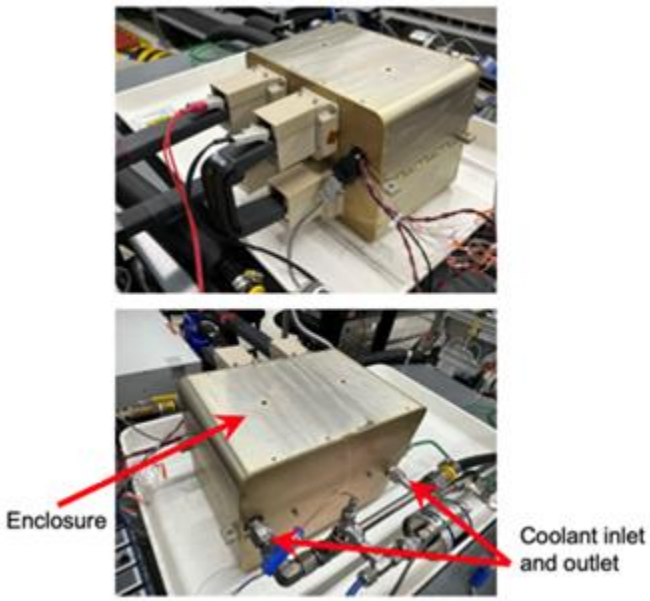


Figure 6-1. *Thermal Loading Test of the SSCB and Key Components*

The initial set of tests on the SSCB was performed with the covers off the package at a coolant temperature of $22°C$ and with a 1 kA DC current. As the internal interconnections temperatures are area of highest concern, these temperature readings are highlighted in Figure 6-2 (left) after a heating time of 10 minutes. In this case, the measured power losses are less than 6.3 kW with two SSCBs in series, i.e., less than 3.15 kW per SSCB side. A further set of tests measured the thermal loading of the SSCB with the covers on, thereby creating an abietic boundary within the package. In this case, the loading current of 1 kA was applied for 50 minutes, with the bus-bar thermal couples reaching a peak temperature of $92.5°C$,

as per Figure 6-2 (right). For the sake of comparison, the internal temperature with the covers and without is presented in Figure 6-3 for a $22°C$ inlet coolant temperature. The impact of closing the SSCB package increases the internal ambient temperature of the breaker from $30°C$ to apprixmately $57°C$. Finally, the efficiency can be calculated by measuring the differential voltage across the breaker at steady state conditions, and normalizing it to the nominal voltage, i.e., $\eta = 1 - \Delta v/V_{nom}$, as shown in Figure 6-4 (left) without the side covers and Figure 6-4 (right) with the side covers. Note that 'Eff_1' refers to the efficiency on either the top or bottom path of the SSCB, and 'Eff_2' refers to the series connection of the top and bottom SSCB path. As shown in Figure 6-4, the calculated efficiency under 1.2 kV operating voltage, and 22°C was >99.5% for a single breaker path, or approximately 99.5% when both breakers are connected in series – emulating protection on the positive and negative rails for a single load.

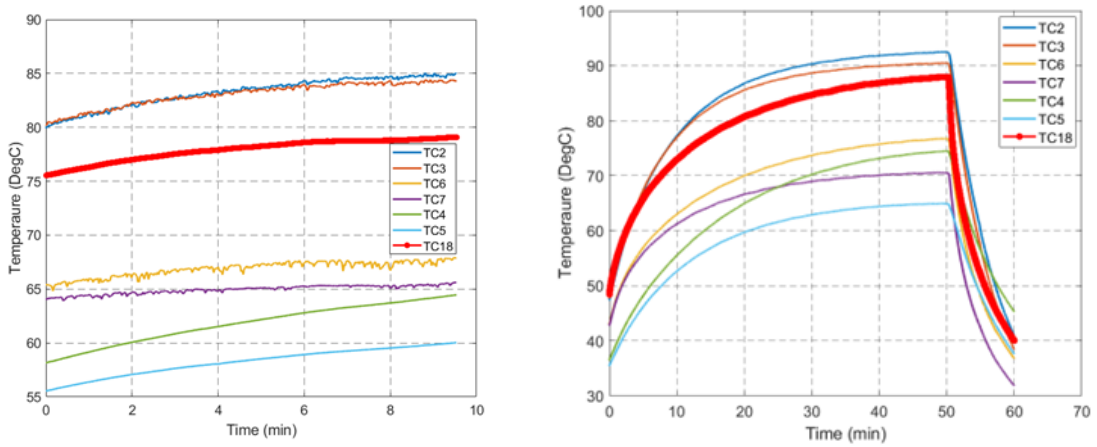
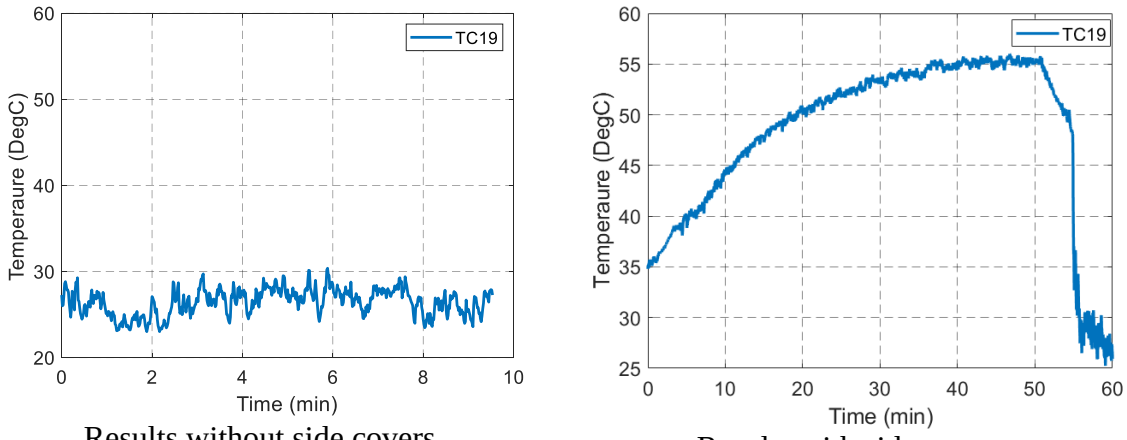


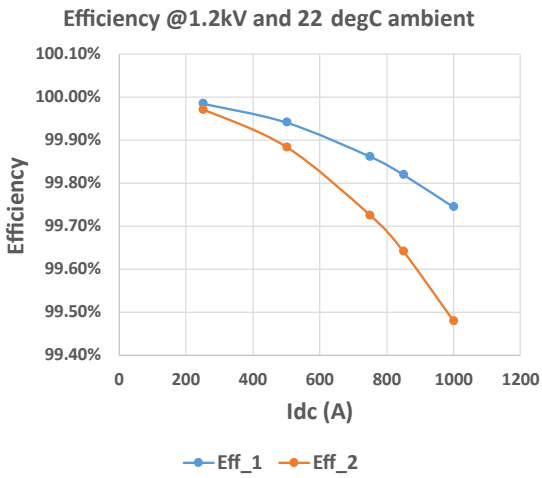
Figure 6-2. *Busbar Temperatures without Side Covers (Left) and with Side Covers (Right)*



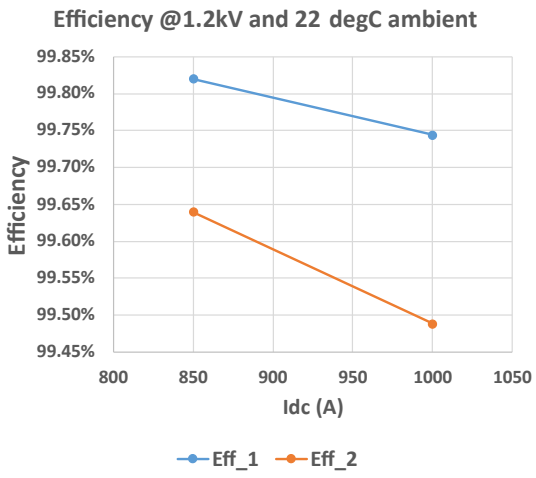
Results without side covers.

Results with side covers.

Figure 6-3. *Internal Temperature of the SSCB with and without the Side Covers*



Calculated efficiency without side covers.



Calculated efficiency with side covers.

Figure 6-4. *Calculated Efficiency of the SSCB with One or Two Series Connection and with/without Side Covers*

The same methodology for testing with the $22°C$ inlet coolant temperature was applied to the SSCB steady state test with the higher (but required, as per Table 1) coolant temperature of $50°C$. Under this inlet coolant temperature, the total power losses increase from approximately 6.2 kW to 7.1 kW, and once again, the bus-bar temperatures represent the highest and most limiting internal temperatures of the system. As a reference, Figure 44 illustrates the temperature rise due to the losses from the SSCB, i.e., both the inlet and outlet temperatures of the system. The bus-bar temperatures with and without the side covers is shown in Figure 6-5, with a peak temperature of $125°C$ experienced in the inner bus-bar assembly on the power module. Note that this temperature is still lower than the prediced temperature during the analysis phase of the project, where this point was estimated to be $136°C$, c.f. Figure 6-6. The impact of the internal temperature rise due to the closing of the SSCB package with the increased coolant temperature is illustrated in Figure 6-7, with the corresponding thermography pictures shown in Figure 6-8. Thus, with a closed cover and with an inlet coolant temperature of 50°C, an efficiency of >99.5% in the case of a single breaker, or ~99.4% with two breakers in series was obtained. Therefore, the critical temperatures observed during the steady state loading test at rated coolant temperatures are acceptable (lower than the dielectric breakdown temperature of the bus-bar coating), and the efficiency target has been met with the SSCB design.

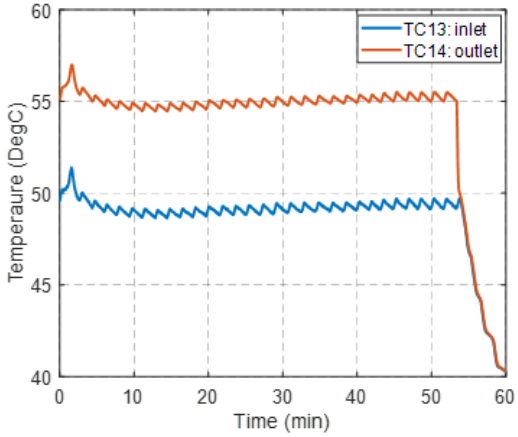


Figure 6-5. *Coolant Inlet and Outlet Temperatures without the Side Cover with 50C Coolant*

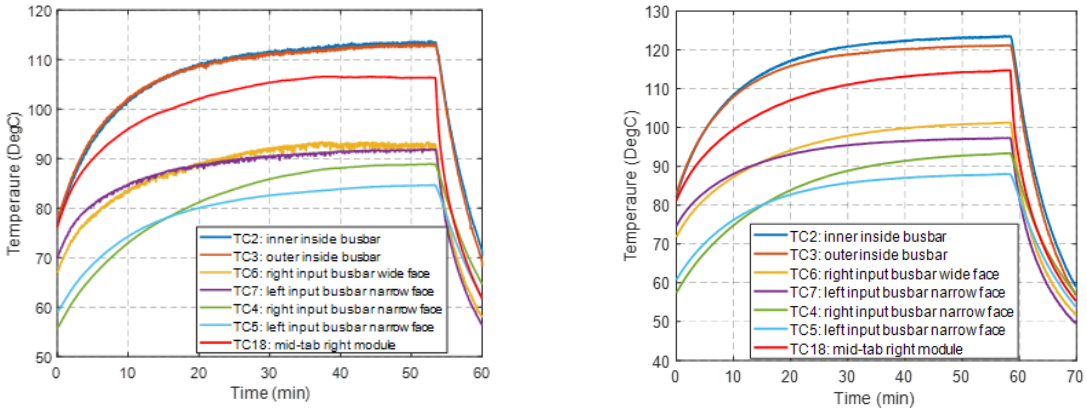


Figure 6-6. *2Busbar Temperature Measurements without (Left) and with (Right) Covers Under 50C Inlet Temperature*

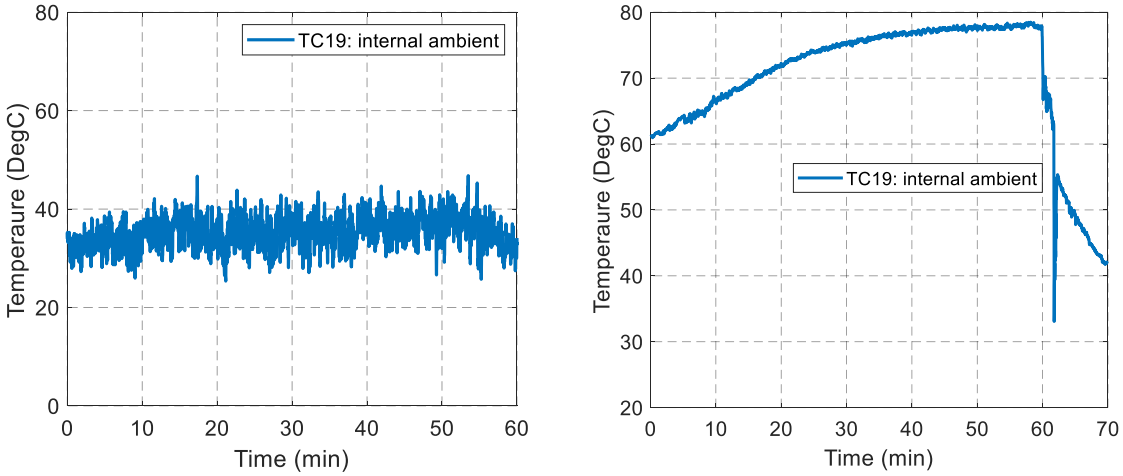


Figure 6-7. *Internal SSCB Temperature without (Left) and with (Right) Side Covers Under 50C Inlet Temperature*

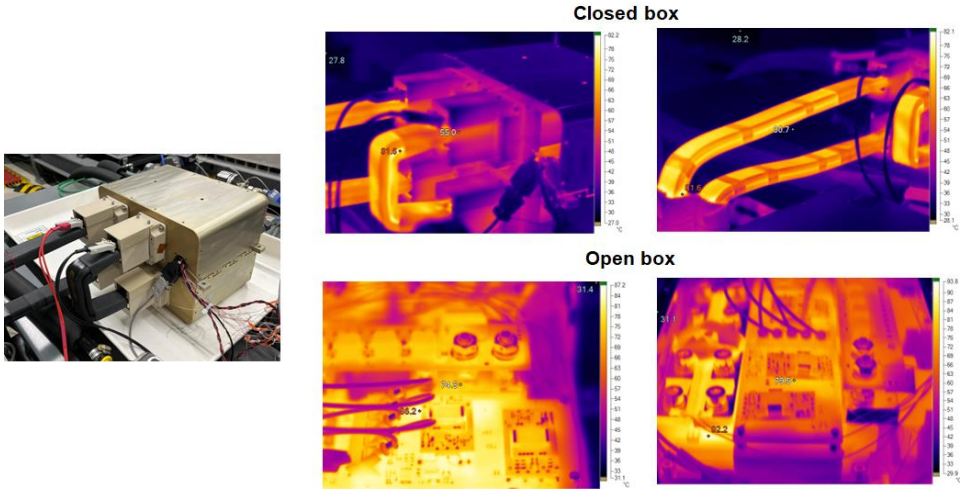


Figure 6-8. *Thermography of SSCB Under 50C Inlet Temperature with and without Covers*

6.2. Dynamic Testing

During a fault condition, the SSCB must be able to interrupt the line current safely and isolate the load or source within 100 us, as specified in Table 1. In the case of the NASA RTAPs SSCB, this interruption must also be done at equivalently high altitude, representing the application in an equivalent aviation environment. This validate phase is therefore broken into two segments: the validation of the fault clearing time and validation of the dynamic performance at emulated high-altitude conditions.

6.2.1. Fault Clearing Time Validation

The fault clearing validation test is performed on the dynamic test bench, as described in Section 5.2 of this report. However, an air-core inductor of 3 uH is used to emulate the grid inductance, such that the fault clearing time represents the worst-case scenario for the SSCB to clear under a faulted condition. Under ambient temperature, and a DC operating voltage of 1.2 kV, Figures 6-9 and 6-10 illustrate the fault clearing time for the top and bottom side SSCB path respectively. In this case, the fault is cleared within a worst case of 61 us, with a peak fault current of 2.43 kA and a voltage of 2.56 kV.

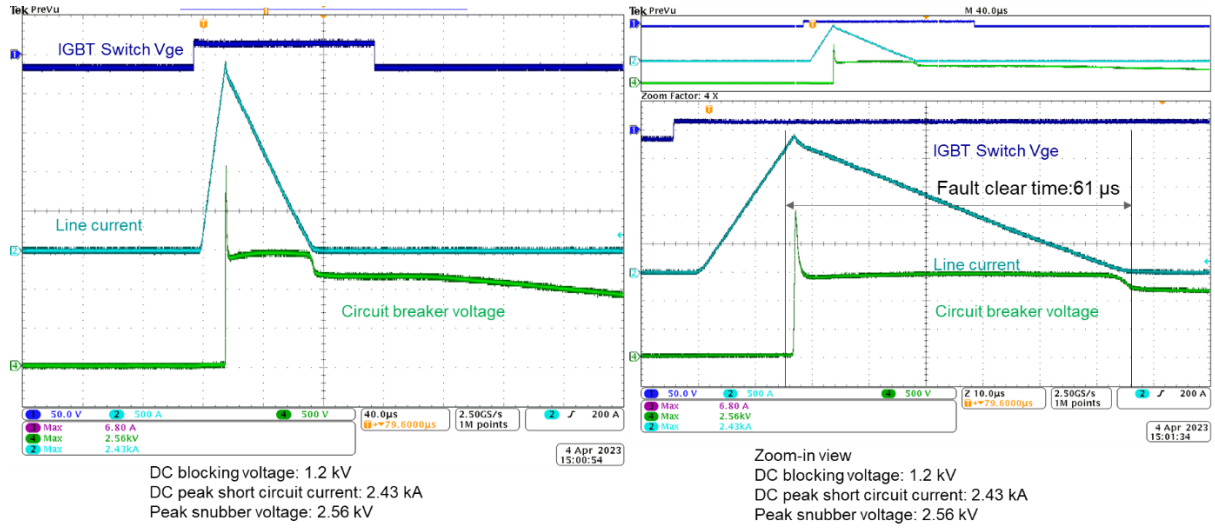


Figure 6-9. *Fault Interruption Test at 1.2 kV for the Top Side of the Breaker*

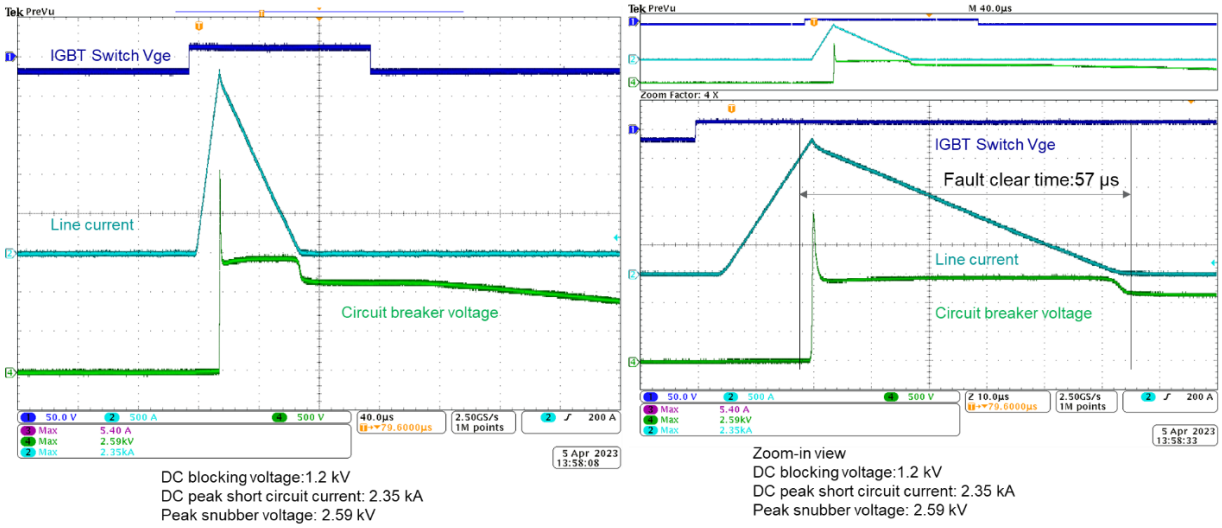


Figure 6-10. *Fault Interruption Test at 1.2 kV for the Bottom Side of the Breaker*

6.2.2. High Altitude Validation

With the fault interruption time at standard ambient pressure validated on the SSCB Gen 1-2 build, the last remaining validation is to examine the fault interruption performance at emulated high-altitude conditions, in this case 35 kft, as per Table 2-1. To meet this requirement, a low-pressure chamber was purchased and installed at RTRC with enough internal volume to fit the SSCB prototype. This low-pressure chamber has a rated differential pressure of -29.9 inHg and features 1" acrylic walls. However, owing to limitations of the pump used at RTRC, the differential pressure is limited to -23 inHg, which is equivalent to 38 kft at 15C.

While the SSCB can be pressurized to the required equivalent altitude and fault clearing time can be evaluated under these conditions, the biggest unknown in this scenario is whether PD is occurring. In this case, the presence of PD at high altitude under the actual application conditions would indicate that the SSCB dielectric spacing or the power module itself would require further development to meet modern aviation reliability standards. Therefore, it is imperative that the test bench be equipped with the capability to monitor PD during the testing. However, PD detection in this scenario is the most challenging, as the closed SSCB package removes the possibility of UHF or PMT sensors, and only the HFCT option is available. In this case, during the fault breaking event, the capacitive discharge currents dominate the ground current, thereby making the detection of PD significantly challenging.

To address this challenge, the team at RTRC partnered with FSU (Florida State University, Prof. Gian Carlo Montanari), who specializes in PD detection in power conversion equipment. The PD detection approach taken in this validation stage is based on using the HFCT (Rugged Monitoring, 0-16MHZ, 50A limit) on the ground terminal, which is connected to the heatsink. The Rugged Monitoring firmware was modified by the FSU team to adjust the filter points to specifically target the ground current waveform experienced during the fault interruption event. The methodology for detection worked around the principal of 'SRI – separation, recognition, and identification', as developed by the team at FSU for challenging PD detection scenarios. Accordingly, the measurement data is captured based on its time-frequency information and separated using based on a Principal Component Analysis (PCA) technique. The 'recognition' stage of the analysis is based off the establishing of a statistical PD reference that is pre-calibrated based off a twisted wire setup, and an identical voltage waveform from a high-voltage AC amplifier as experienced by the SSCB. This latter stage was completed at FSU prior to testing at RTRC. Last, the identification step requires matching through custom algorithms the pre-calibrated PD pattern to the separated data acquired during a fault interruption event. These pulse patterns can include a variety of PD events, i.e., internal, surface or corona, which can also be uniquely identified based on a specific pattern. A sample waveform of the Rugged Monitoring software used for the PD detection is shown in Figure 6-11, illustrating PD capture under DC voltage, and pulse width modulated voltages, as per Figure 6-12.

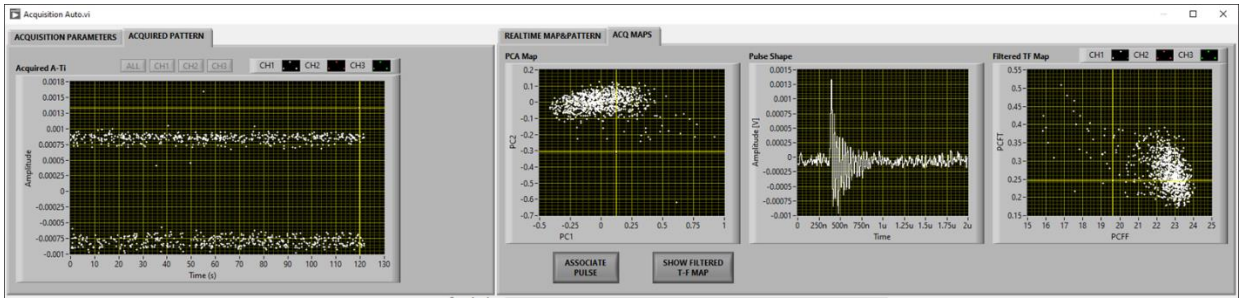


Figure 6-11. *PD Measurement Example under DC Voltage using the HFCT*

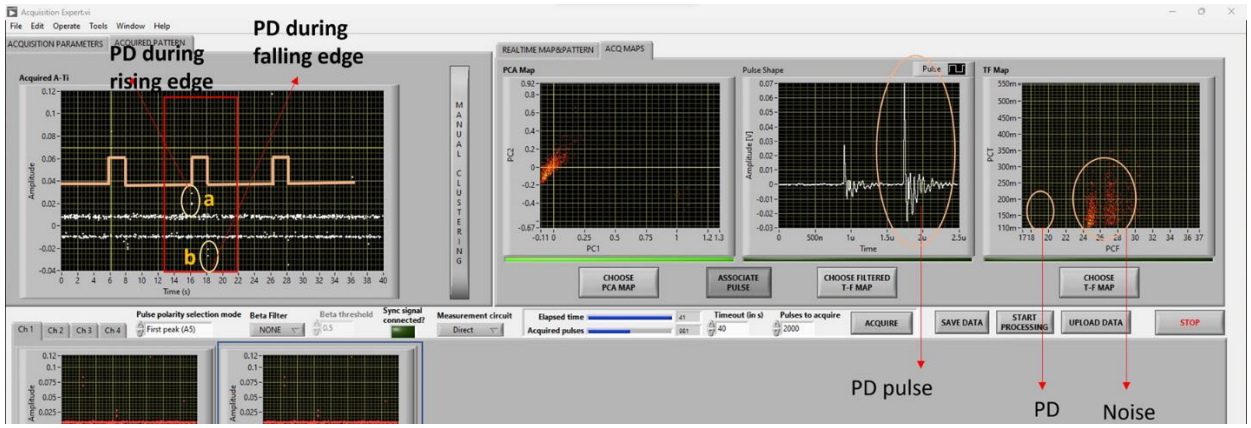


Figure 6-12. *PD Measurement Example under PWM Voltage using the HFCT*

The experimental test setup of the low-pressure chamber with the SSCB installed, along with the HFCT and the Rugged Monitoring (RM) equipment is shown in Figure 6-13. Note that the previous dynamic test bench is utilized with this validation step, but with the SSCB placed in the low-pressure chamber. Within the chamber, all the associated SSCB equipment is located, thereby emulating the high-altitude environment for the test. Prior to testing however, a high-voltage amplifier was used to verify the operation of the PD detection equipment using a standard twisted pair setup.

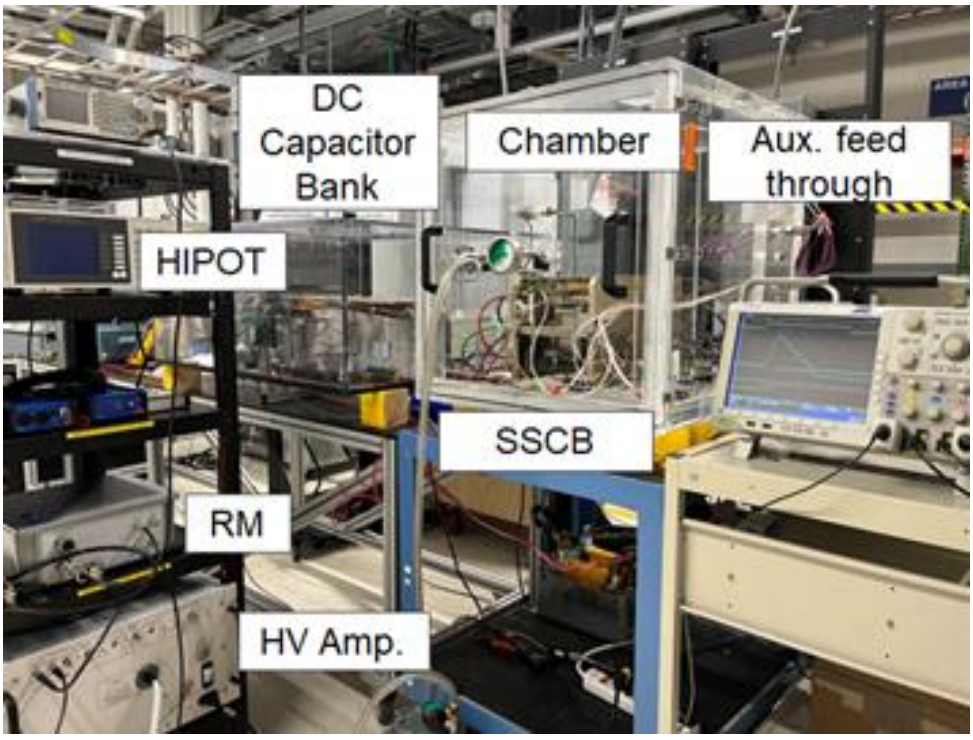


Figure 6-13. *Test Setup at RTRC with the Low-Pressure Chamber*

The validation methodology consisted of maximizing the probability of capturing PD by performing at least 20 tests per validation point, or at least 5-10 minutes in the case of DC voltage energization. The first test

occurs under DC voltage energization, at both sea-level ambient pressure (SAP), at the high-altitude emulated pressure (HAEP) of -23 inHg or 38 kft/15C. As a step-by-step approach, the team performed the following validation tests:

- Rated operating voltage (1.2 kV) for a duration of at least 5-10 minutes at SAP and check for partial discharge.
- Rated operating voltage (1.2 kV) for a duration of at least 5-10 minutes at HAEP and check for partial discharge.
- Fault interruption test at rated conditions (1.2 kV/2.5 kA peak) at SAP under a minimum of 20 repetitions and check for partial discharge.
- Fault interruption test at rated conditions (1.2 kV/2.5 kA peak) at SAP under a minimum of 20 repetitions and check for partial discharge.

The isolation voltage testing equipment is used in the first test to apply a constant DC bias for a long duration with the immediate ability to interrupt the voltage in case of excessive leakage current from the SSCB. Under both SAP and HAEP, after 5-10 minutes of operation, noise events were captured as illustrated in Figures 6-14 and 6-15, but no PD events were observed after post-processing/analysis.

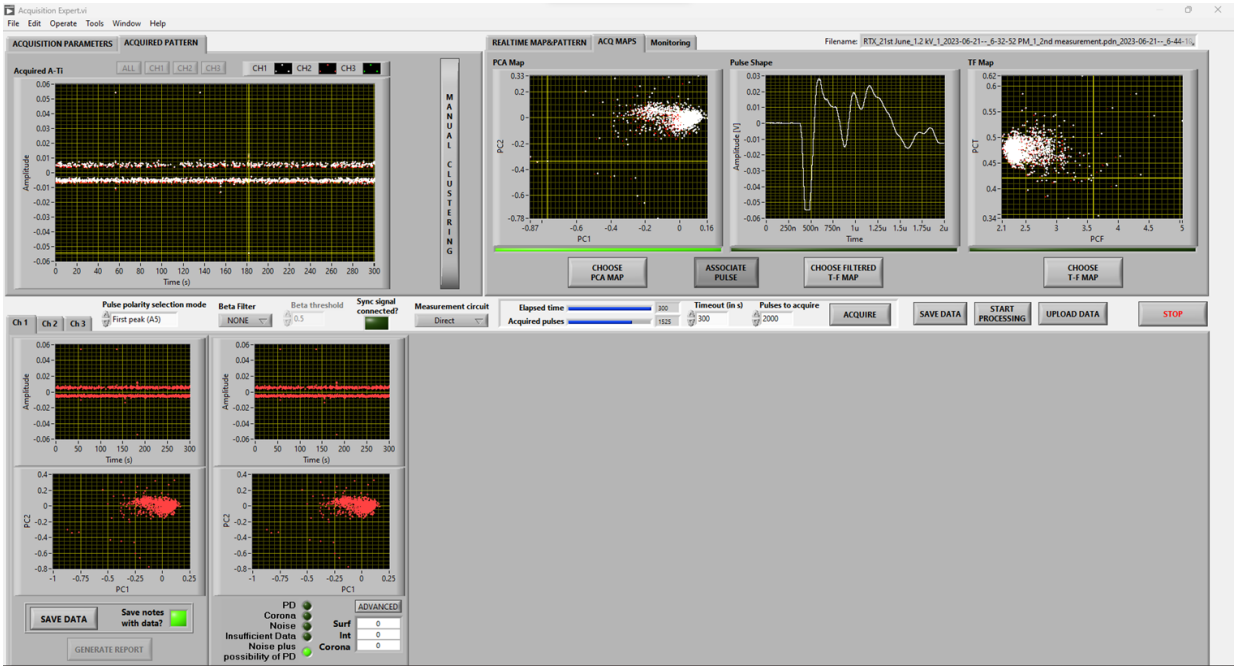


Figure 6-14. *DC Bias Test Under SAP*

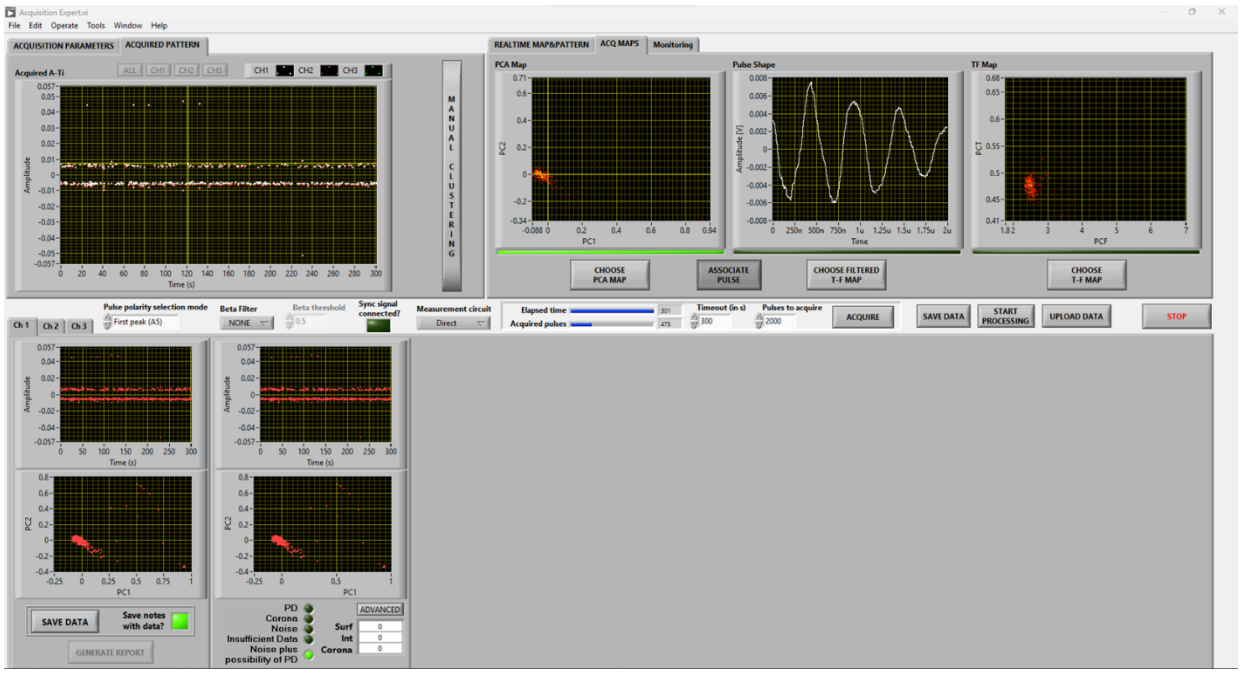


Figure 6-15. *DC Bias Test Under HAEP*

Under the fault interruption tests, the control sequence for the SSCB was modified to enable repetitive testing for each condition. Compared to the DC bias testing from Figures 6-14 and 6-15, the induced noise at turn off was substantial – increasing the risk of the capacitive discharge currents masking the PD events. Under the SAP conditions, one sample of the collected data is illustrated in Figure 6-16, which featured several data points that suggested the possibility of PD. In this case, each event was manually analyzed by the team (with the help from FSU). Examples of these datapoints are highlighted by the 'a', 'b' and 'c' reference points in Figure 6-16. However, none of these patterns matched classical or the pre-calibrated PD characteristic waveform, and hence, was classified as noise. All 20 tests obtained a similar result – several points of which could contain PD but were identified as noise upon manual inspection. Similarly, the HAEP condition produced identical results, but with even more events being flagged by the software as potential PD events. Nevertheless, on manual review, each data capture was representative of noise, i.e., did not even show a 'discharge' characteristic, as shown in point 'a' from Figure 6-16. One representative software screenshot for the HAEP test is shown in Figure 6-17, with the captured data highlighting one such noise capture. In all cases, the fault current interrupt was successful, and the clearance time was not impacted by the altitude, as illustrated in Figure 6-18.

In conclusion, based on the measurements and analysis by the team during the high-altitude validation tests, no PD events were captured under any operating condition. While the prior testing at OSU with just the power modules indicated that these components were unlikely to produce PD based on the usage profile of the SSCB, many other interfaces within the SSCB could also be suspectable to PD and eventual dielectric breakdown. Nevertheless, while the system level testing did not reveal any PD events, the fundamental AC PD testing of the power modules did reveal that PD could occur at the voltages employed in the experiment. This is because the AC test provides a continuous stress to the dielectric, unlike the non-repetitive and non-deterministic behavior typical of DC breakers. Hence, while the testing did not reveal any PD in the SSCB – even under an increased repetition of tests -- more standardized testing of power modules for DC distribution equipment is required to ensure that high reliability targets are met for the needs of future aviation applications.

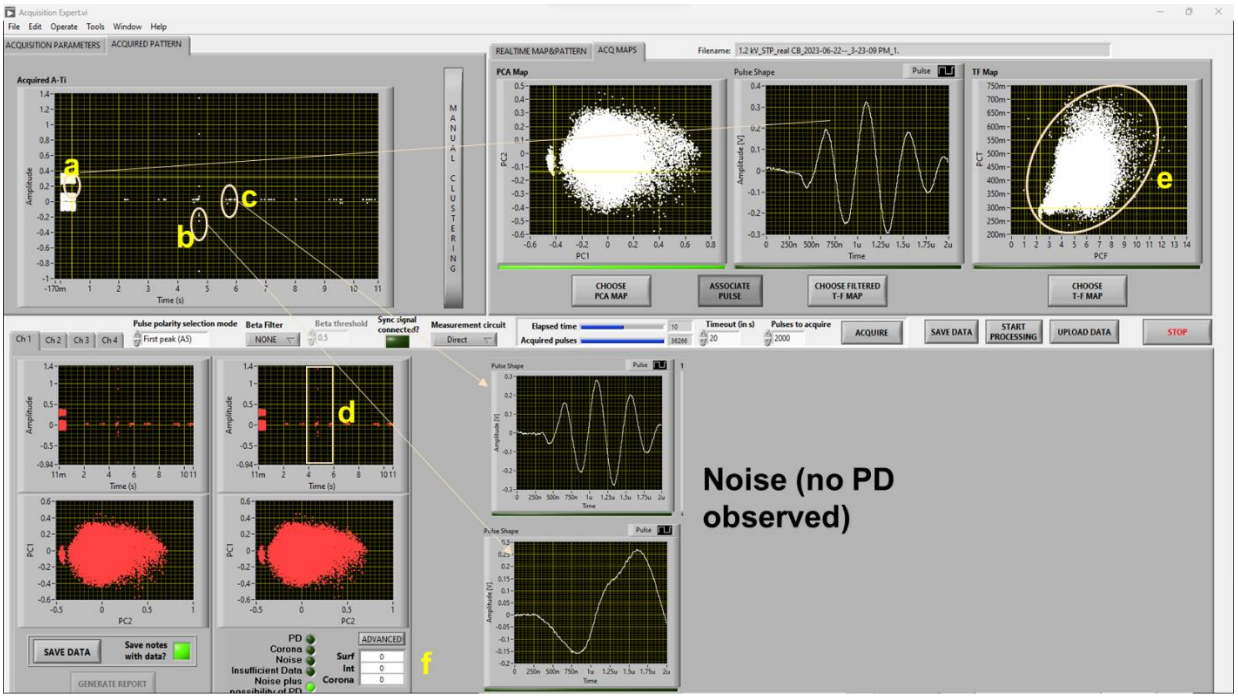


Figure 6-16. *Sample Fault Interruption Test with PD Monitoring at SAP*

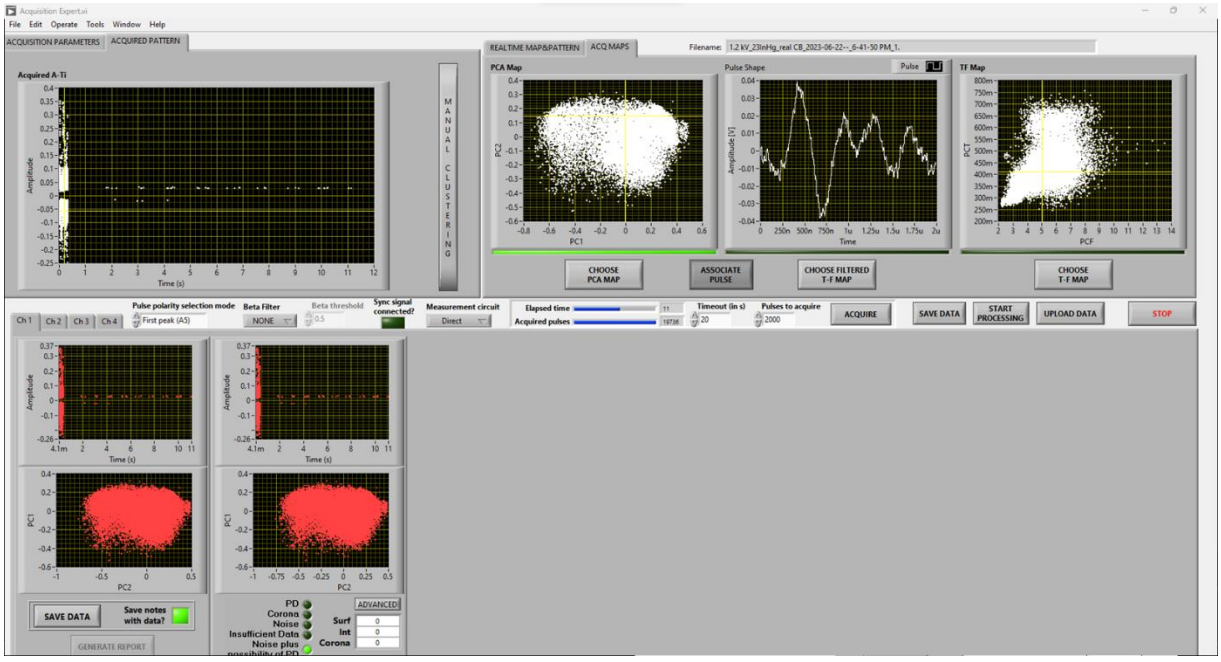


Figure 6-17. *Sample Fault Interruption Test with PD Monitoring at HAEP*

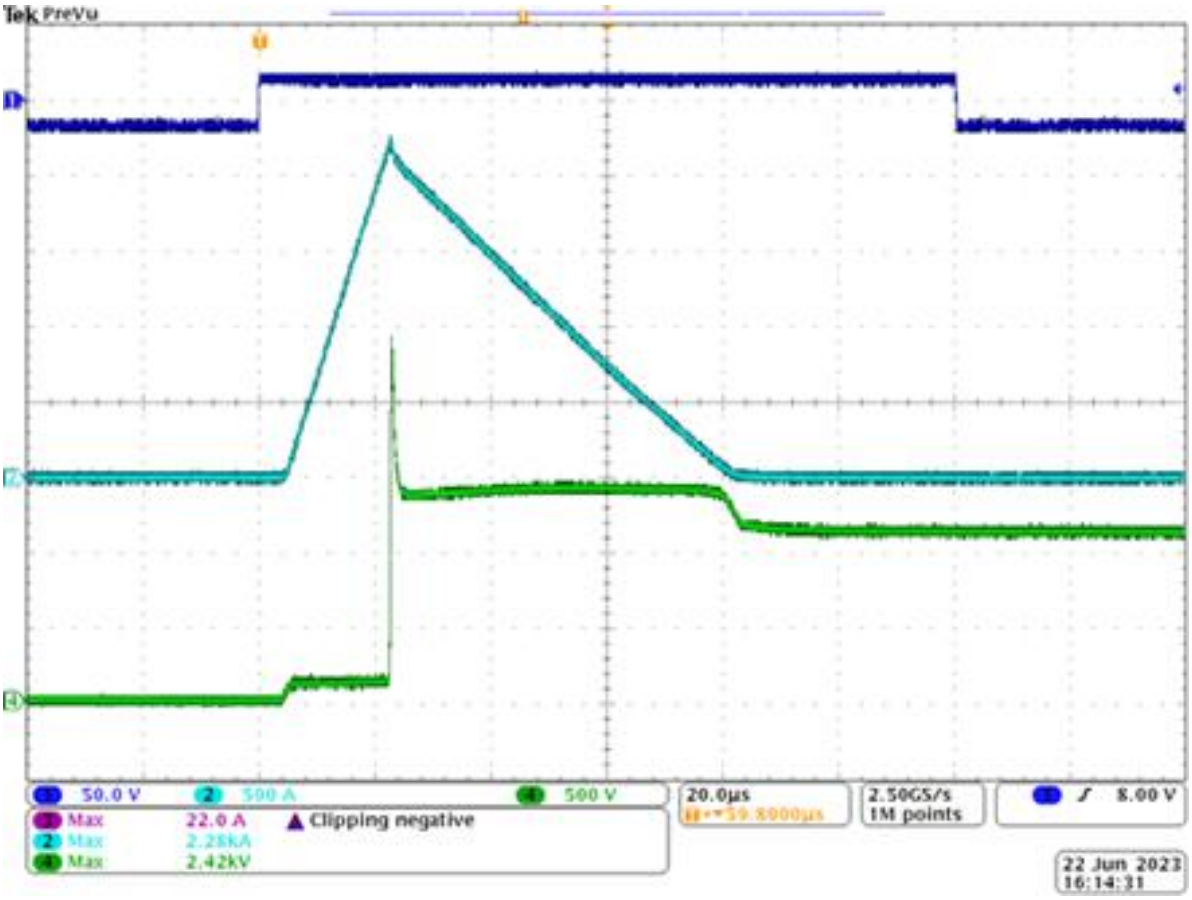


Figure 6-18. *Fault Interruption Waveform Captures at HAEP: Gate Voltage, Line Current, SSCB Voltage*

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7. CONCLUSION

The need for compact, efficiency and reliable DC power distribution equipment is paramount to enable the partial or full electrification of the propulsion system in future aviation systems. This project focused on the development of a 100 kW, >99.5%, solid-state circuit breaker with a rated voltage of 1.2kV, and a nominal power of 1.2 MW. The switching response target is less than 100 us, and the SSCB must be capable of 35 kft operation. Under these metrics, the team of Collins Aerospace, RTX Technology Research Center (RTRC), and Pratt & Whitney were successful in meeting and exceeding these metrics, with the final performance highlighted in the Table 1-1.

Exceeding these defined program metrics was a result of making several important contributions to the field of high-power DC distribution equipment, particularly the following:

- Development of voltage spacing for 1.2 kV DC operating voltages, with a peak of 2.5 kV during the breaking operation. The resulting design and packaging of the SSCB under these guidelines were benchmarked during the altitude validation stage of the project and no PD was detected during operation.
- Additive manufactured thermal management technologies which enabled an aggressive power density target, but also a balanced thermal profile across the power module. This balanced thermal profile aides in improving the utilization of the power semiconductor, enabling the lowest losses across the total semiconductor area.
- Ultra-fast and accurate current sensing technology by developing a combined DC-mid band hall effect sensor and high frequency Rogowski coil. The combined current sensor also featured extremely low mass and volume, thereby aiding the team towards meeting the weight target but also allowing for more flexible packaging options.

Finally, the team successively demonstrated both the steady-state operation of the SSCB to confirm the efficiency and safe maximum internal temperature, as well as under a fault breaking event under emulated conditions of 35 kft. Future work towards the SSCB developed under this project would be to transition towards manufacturability, integrate more features, i.e., DC arc detection, and examine the lifetime of the product under continual stress.

8. References

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