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A Radiation-Hard 8-Channel 15-Bit 40-MSPS ADC for the ATLAS Liquid Argon Calorimeter Readout

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ABSTRACT The custom design of a radiation-hardened, 8-channel, 40-MSPS, 15-bit resolution, 14.2-bit dynamic range, 11.4-ENOB ADC data acquisition ASIC fabricated in a commercial 65-nm triple-well CMOS technology is presented. The ADC is developed for and integrates seamlessly into the readout system for the ATLAS liquid argon (LAr) calorimeter in the high-luminosity large hadron collider (HL-LHC) upgrade at CERN, which will require a total of 364 936 ADC channels. A three-stage MDAC+SAR pipelined ADC architecture was designed to meet the physics requirements and scientific goals of the ATLAS experiment. The ADC is a fully self-contained data acquisition system that includes foreground calibration, digital data processing, digital control, and supporting circuitry. The measured performance shows the ADC achieves a competitive dynamic range and SNDR, and it meets or exceeds the ATLAS analog requirements. Radiation tolerance and scalability design considerations were implemented at the device-, circuit-, and system-level. Radiation-hardening-by-design techniques used include redundancy for digital circuits, the use of MiM capacitors, and a hybrid RC-DAC for the ADC core. The ADC ASIC was demonstrated to be robust against the effects of the intense radiation expected in the HL-LHC experimental environment.

INDEX TERMS DAQ, data acquisition, radiation-hard, radiation-tolerant, system-on-chip.

I. INTRODUCTION

THE HIGH-LUMINOSITY large hadron collider (HL-LHC) [1] at CERN is designed to produce up to a tenfold increase in the rate of proton-proton (pp) collisions

compared to the LHC, producing up to 200 simultaneous pp collisions for every bunch crossing. The increased luminosity will permit further scientific studies of fundamental particle physics, such as the Higgs Boson [2], [3], [4]. The tenfold

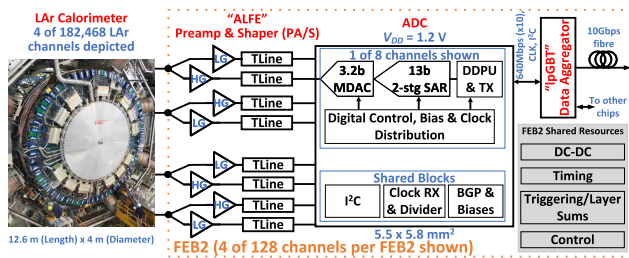


FIGURE 1. Simplified readout signal flow of the ATLAS LAr calorimeter with emphasis on the analog signal chain.

increase in collision rates requires the development of new readout electronics [5] for the ATLAS [6] liquid argon (LAr) calorimeter system.

The HL-LHC LAr readout architecture requires the development of a full-custom 8-channel ADC [7], [8], [9] to digitize each calorimeter channel at the HL-LHC bunch crossing frequency of 40 MHz. Designing a suitable ADC for this purpose imposes stringent analog accuracy, reliability, scalability, and system integration requirements that are both specific to the HL-LHC and not trivial to meet. Hence, there exist relatively few prior examples in the literature. The split-SAR ADC topology [10] has been investigated and a custom, pipelined ADC [11] has been used in similar applications but they do not meet scalability and radiation hardening requirements for the LAr readout upgrade.

In this article, we present an 8-channel, radiation-hardened-by-design (RHBD), 15-bit resolution, 14.2-bit (85.5-dB) dynamic range, 11.4-ENOB (70.3-dB SNDR), 40-MSPS ADC data acquisition system for the ATLAS LAr HL-LHC upgrade. An overview of the readout architecture is provided in Section II. The system and ADC requirements are summarized in Section III. The ADC architecture selection is discussed in Section IV, followed by circuit-level implementation details in Sections V and VI. Experimental results, including measurements of analog performance and radiation tolerance, are presented in Section VII, followed by comparison and conclusions in Sections VIII and IX.

II. OVERVIEW OF ATLAS LAR HL-LHC READOUT

The HL-LHC LAr readout signal path is shown schematically in Fig. 1. The ATLAS LAr calorimeter measures the energies of particles produced in the collisions in the HL-LHC. Particles traversing any of the 182 468 calorimeter cells ionize the LAr medium, resulting in triangular pulses of electrical current being produced. These pulses are transmitted out of the LAr cryostat by cables which are terminated on so-called Frontend Boards (FEB2) [5], [9], [12] being developed for the HL-LHC that reside in crates mounted directly on the cryostat feedthroughs. Each FEB2 reads out 128 calorimeter channels on two gain scales, requiring 256 independent ADC channels, implemented via 32 ADC ASICs of eight independent ADC channels each. The three custom ASICs in the signal chain are depicted in Fig. 1 (preamplifier/shaper, this 8-channel ADC, and data

aggregator) with supporting electronics mounted on the front-end boards. Power to the FEB2 is input at 48 V and distributed using on-board, radiation-hardened dc-dc converters and low-dropout regulators. The FEB2 boards are water-cooled to operate approximately at room temperature.

The custom “ALFE” preamplifier/shaper (PA/S) ASIC [13] shown in Fig. 1 terminates the signal cables, amplifies the current pulses and converts them to voltage, splits each signal into two overlapping linear gain scales (dubbed “high-gain” [HG] and “low-gain” [LG], with a gain ratio ~ 25 V/V), and applies shaping and analog matched filtering with an CR-RC² filter for improved SNR [14]. Data from both gain scales are processed off-detector and HG data is used if it has not saturated. To minimize interchannel cross-talk and due to constraints from the FEB2 layout, an unterminated transmission line of length ~ 20 cm exists between the PA/S outputs and ADC inputs. To avoid halving the signal dynamic range, this line cannot be terminated, so the ADC must address its own sampling kickback interacting with the unterminated line.

The conditioned signals are quantized by the “COLUTA” 8-channel ADC ASIC discussed here. The signals are quantized at a rate of 40 MSPS which is synchronous to the rate of pp collisions in the HL-LHC. To achieve the required performance, the ADC incorporates an on-chip digital data processing unit (DDPU) to apply calibrated bit weights to the quantized signals. The DDPU also formats each digitized sample into a 16-bit word, which is then serialized, timestamped, and transmitted at 640 Mb/s using the CERN low-power signaling (CLPS) specification [15]. Timestamping ensures all samples from all ADC channels are synchronous with each other. Each ADC ASIC outputs ten 640 Mb/s serial lanes, one for each ADC channel plus two for timestamp metadata.

The digital data from one FEB2 with 32 ADC ASICs (320 serial lanes, each at 640 Mb/s) are aggregated and packetized to multiple 10 Gb/s streams using the custom “low-power gigabit transceiver” (lpGBT) ASIC [16], [17], before being transmitted off-detector via 22 10-Gb/s optical links. Two additional lpGBT ASICs on each FEB2 also provide redundant clock and control signals. A low-jitter, 50% duty cycle 40 MHz and a nonprecision 640-MHz clock are distributed on the FEB2 for use as a precision sampling clock and for data serialization purposes, respectively. I²C networks are used to configure all the various ASICs. The digital data undergoes further matched filtering and correlation, depending on specific scientific goals.

III. ADC REQUIREMENTS

As described below, the ADC requirements are driven by the LAr calorimeter performance, the scientific goals of the HL-LHC program, and the HL-LHC experimental environment. We define resolution to be the full-scale input over the V_{LSB} , and dynamic range to be the full-scale rms over the ADC noise rms.

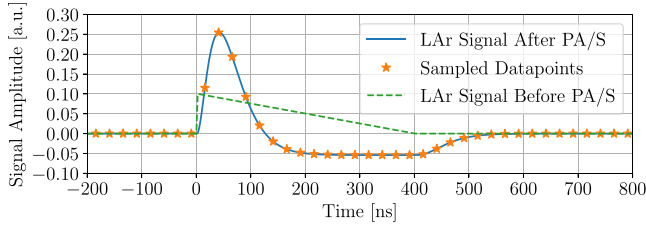


FIGURE 2. Raw unipolar LAr pulseshape before and the resulting bipolar waveform after preamplification and shaping, with arbitrary normalization. The sampling points for the ADC are spaced 25 ns apart.

A. ANALOG ACCURACY

The raw unipolar LAr pulse before shaping and matched filtering and the bipolar LAr pulse after the PA/S are shown in Fig. 2. The unipolar LAr pulse before the PA/S is difficult to quantify with adequate SNR. The positive and negative amplitudes of the shaped LAr pulse are proportional to the positive amplitude of the unipolar raw LAr pulse waveform. Each pulse is the signature of a subatomic particle interaction within the calorimeter. The rate of such pulses is proportional to the rate of pp collisions, and the amplitude is proportional to the energy deposited in an individual calorimeter cell by the interacting particle. The shaper's response is analytically known. The spectral content of the shaped LAr pulses predominantly reside between 5 and 8 MHz, because the chosen shaper filter's time constant is a design tradeoff between the so-called pileup noise [14] and the 40-MSPS sampling rate which is synchronous to the accelerator beam structure.

The quantization requirements are summarized in Fig. 3 where the intrinsic measurement uncertainty of the calorimeter relative to the energy of the particle being measured, $(\sigma(E)/E)$, is used to determine linearity and SNDR requirements for the ADC [18], [19]. This is done by setting $(\sigma(E)/E)^{-1}$ equal to $S/(N+D)$, where S is the signal power of interest and $N+D$ are noise and distortion powers of the quantizer. Full-scale of the PA/S output and the quantizer input is defined to be 2 V_{pp} differential. According to the detector specification in Fig. 3, a single quantizer with at least 94.1 dB (about 16 bits) of dynamic range and 43.5 dB of SNDR would be required to quantize the calorimeter signal without significantly degrading its signal fidelity [5].

Meeting these specifications with a single quantizer, while satisfying reliability and radiation-hardening requirements, is difficult. Instead, the requirement has been relaxed at the system level by splitting each LAr calorimeter channel into two overlapping gain scales that are simultaneously digitized with two independent ADC channels. Hence, the 182 468 calorimeter channels require 364 936 ADC channels. The high-gain (HG) channel has a 25× V/V amplification built into the PA/S, whereas the low-gain (LG) channel is unity gain, allowing the total 16-bit dynamic range to be covered using two ADCs. Scale errors between ADC channels are handled at the system level. HG and LG performance is plotted in Fig. 3, assuming that both channels

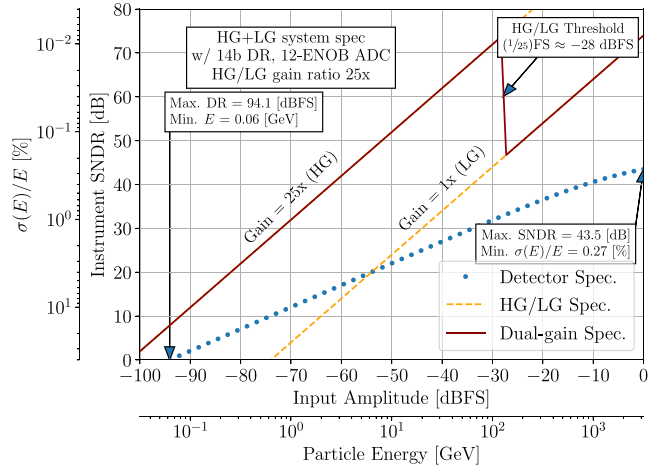


FIGURE 3. Intrinsic detector performance expressed as SNDR, HG and LG path specifications, and the combined dual-gain specification as a function of input dynamic range (DR).

are quantized using an ADC with 14 bits of dynamic range and 12 ENOB at full-scale, though there is sufficient margin to tolerate a performance of ≥ 11 ENOB. The single-quantizer specification of 16-bit dynamic range is thus relaxed to 14 bits under the HG/LG scheme, with design margin built in.

B. RELIABILITY AND RADIATION TOLERANCE

Due to their on-detector location, the FEB2 boards experience significant radiation exposure due to particles resulting from the collisions, and cannot be reasonably shielded from this radiation. The FEB2 boards are also inaccessible during operation and can be accessed for maintenance at most once per year. Furthermore, the HL-LHC is expected to operate for at least 12 years [20], with minimal downtime, in order to maximize its scientific output. Therefore, the 364 936 ADC channels must be “install-and-forget” and operate reliably for extended periods in harsh conditions.

The ADC must be RHBD, maintaining performance while withstanding (including some safety factors) a total ionizing dose (TID) of at least 1.4 kGy(Si), sustain 4.1×10^{13} n_{eq}/cm² nonionizing energy loss (NIEL), and tolerate 1.0×10^{13} hadrons/cm² capable of producing single-event upsets (SEUs) [5] over the 12-year operating lifetime. Such radiation dose rates are typically encountered by satellites in geostationary orbit [21].

Transient errors affecting one or a few data samples due to SEUs can be tolerated and corrected by offline data analysis since the LAr pulse shape is analytically known. However, persistent errors affecting many consecutive samples or failure mechanisms that require power cycling would incur downtime and cannot be tolerated. To minimize off-chip active components and their potential radiation vulnerability, all necessary functionalities are integrated on-chip and the ADC is integrated seamlessly between the PA/S and IpGBT ASICs.

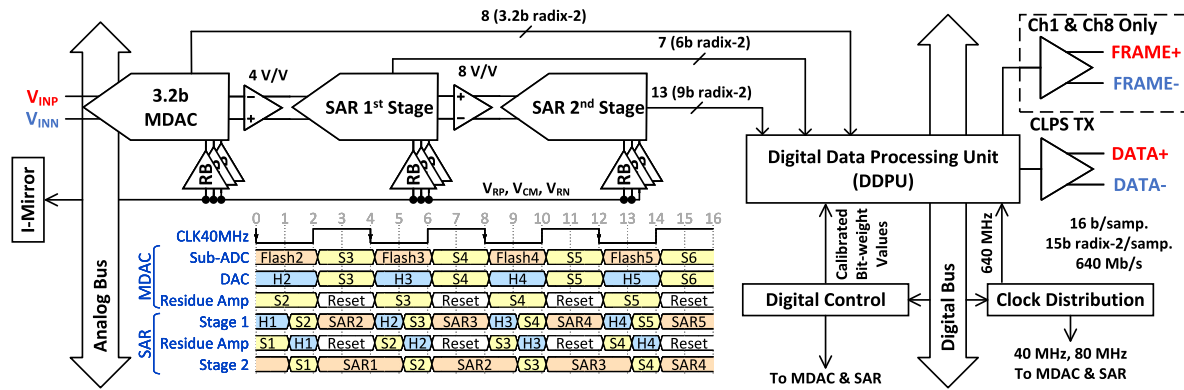


FIGURE 4. Block diagram and signal flow of each of the eight ADC channels. Analog current and voltage biases are provided by the analog bus; clocks and digital control signals are provided by the digital bus. The analog and digital buses connect the eight ADC channels to shared blocks (discussed in Section VI) within the ASIC, however each ADC channel operates independently of each other. The numerical suffices in the timing diagram indicate the sample number. “S” is short for Sample, “H” for Hold, and “SAR” and “Flash” indicate evaluation cycles.

C. CALIBRATION

Achieving the required analog performance requires determining and applying calibration constants to the ADC bits. The precise understanding of the detector response required to extract the best physics results relies on stable conditions, including calibration, over extended periods of data collection.

This requirement disfavors the use of background calibration schemes. In addition, any background calibration scheme that depends on the signal being quantized would be challenging since the LAr pulse shape is nonsinusoidal with a variable occurrence rate. In addition, the associated logic overhead is unfeasible to implement in the radiation environment. As a result of these considerations, foreground calibration is preferred, at the expense of some downtime to periodically calibrate all ADC channels. The foreground calibration could be performed between HL-LHC runs, during the operational downtime when new beams are being prepared.

Given the total volume of LAr readout data, which exceeds 300 Tb/s, it is essential for the calibration constants to be stored and applied on-chip by the DDPU embedded in each ADC channel. Therefore, all calibration hardware must be RHBD to avoid erroneous calibration parameters, for example, caused by SEUs, that would invalidate data. The calibration constants would be downloaded at the beginning of each HL-LHC run, which typically lasts of order one day.

D. SUMMARY

The ATLAS LAr calorimeter presents a unique set of performance, reliability, and scalability engineering challenges [5]. The increased luminosity of the HL-LHC imposes more stringent analog performance and radiation robustness requirements on the front-end readout electronics that directly interface with the detector. The calorimeter readout requires 364 936 independent ADC channels, each quantizing at a rate of 40 MSPS with ≥ 14 bits (84 dB) of dynamic range, ≥ 11 ENOB (68-dB SNDR) of linearity, and full-scale defined to be 2 V_{pp} differential. The 40-MSPS

sampling rate is set by the bunch crossing rate of energetic particles in the HL-LHC and is synchronized to the broader HL-LHC infrastructure. The ADC must be RHBD and radiation-induced failure mechanisms must be transient in nature, cannot require a power cycle for upset recovery, and performance degradation must not be excessive. Foreground calibration must be implemented on-chip for each channel, eight independent channels must be integrated onto a single chip, and the ADC must seamlessly interface with the PA/S and data aggregator ASICs.

IV. ADC ARCHITECTURE DESIGN

An 8-channel, 1.2-V only, 40-MSPS, radiation-hardened, three-stage pipelined MDAC+SAR ADC data acquisition ASIC has been implemented with 15 bits of resolution to achieve ≥ 14 bits of dynamic range and ≥ 11 ENOB in order to meet the physics requirements discussed in Section III. The data acquisition ASIC is implemented in a commercial, triple-well 65-nm CMOS process. Each of the eight channels is identical and operates independently. Each channel consists of a multiplying-DAC (MDAC), a two-stage SAR, a DDPU, and a digital control state machine. Fig. 4 shows the channel architecture in detail, as well as the function of each clock cycle. Samples are captured at the falling edges of the 40 MHz, 50% duty cycle sampling clock.

A. MDAC+SAR ARCHITECTURE

The ≥ 14 bit dynamic range specification determines the minimum required sampling capacitor to suppress kT/C noise. The architecture incorporates a 9-subrange (3.2 bits) MDAC before a 12-bit, two-stage SAR, with the MDAC used to relax the dynamic range requirement for the SAR. The MDAC is thermometer coded to guarantee monotonicity and its residue amplifier ensures sufficient linearity for the SAR to resolve 12 bits, with 1 bit of interstage redundancy. The MDAC and SAR are memory-less and their states are determined by the 40-MHz precision sampling clock and an

intermediate 80-MHz internal clock signal. Therefore, any radiation-induced upset will only affect an individual sample. Lastly, each stage incorporates separate reference buffers to mitigate interstage crosstalk via the references and all analog blocks are current biased.

B. DATA PROCESSING AND CALIBRATION

The DDPU and digital control blocks in Fig. 4 work together to logically and physically interface the ADC with the lpGBT control and data aggregator ASIC without additional off-chip components. The DDPU is necessary to efficiently combine and serialize different types of data given limited bandwidth and resources off-detector. Each channel is allocated 16 bits of data per sample which, depending on the operational mode of the DDPU, can represent the calibrated ADC data, metadata, or diagnostic/calibration information. In data acquisition mode, the DDPU sums the calibrated bit weights into a 15-bit binary number and formats it, along with an overflow bit, into a 16-bit word (detailed discussion is presented in Section V) that is transmitted off-detector for physics data analysis.

In calibration mode, the digital control inhibits the sampling of the input signal and operates the foreground calibration circuitry within the MDAC and SAR. The data is parsed by the DDPU and the calibrated bit weights are calculated off-chip. The resulting calibrated bit weight parameters are programmed back into the digital control for use in data acquisition. Calibration calculations are done off-chip to prevent radiation-induced errors in the calculation that would give erroneous data. Storage of the calibration parameters and digital control states are made radiation tolerant by design and do not utilize radiation-hard memory cells. The potential for radiation-induced errors during the programming of the digital control memory is mitigated at the system level by reading back the memory contents after programming, as well as periodically during data acquisition.

Lastly, the DDPU provides timestamping (FRAME output) information to the lpGBT data aggregator ASIC. Although each channel's DDPU has a FRAME output, only two are brought off-chip, as synchronization between channels on a single ASIC is guaranteed by design. Two FRAME outputs are provided since some ADC ASICs on each FEB2 transmit half of their output channels to each of two separate lpGBT ASICs. Timestamping ensures data synchronization between different ASICs and different FEB2 boards at the system level.

C. RADIATION HARDENING

The ADC is radiation hardened by design. SEUs impacting data need not to be factored into the SNR budget as long as the SEU happens rare enough and a slew of consecutive samples are not affected, as mentioned in Section III-B. The design goal is to minimize the probability that SEUs impact the data, ensure that a slew of samples are not affected, that any failure mechanisms are nondestructive and can be recovered without power cycling, and long-term performance

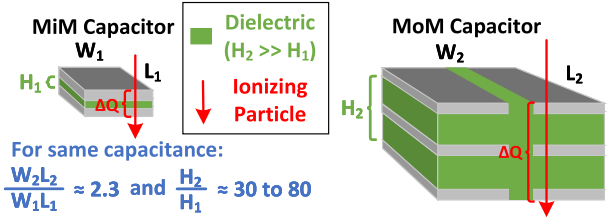


FIGURE 5. Cross section of an MoM versus MiM capacitor in the case of a single-event upset impacting the DAC.

degradation due to radiation is not excessive. First, while the 1.2-V core devices in the 65-nm foundry process used for this design have been extensively studied and demonstrated to be inherently radiation hard, the thick-oxide devices exhibited high sensitivity to TID and therefore are not used [22], [23], [24], [25], [26], [27], [28]. Other general RHBD techniques employed in the design are discussed in this section, with specific circuit-level implementation details given in Sections V and VI.

TID damage predominantly manifests as an increase in transistor V_{TH} and leakage current [23], with the latter mostly affecting transistors of small W and L . Therefore, minimum W and L transistors are avoided in analog circuits and logic cells with the smallest drive strength are avoided in digital synthesis. The conventional CMOS design practice of distributing biases as currents also helps to mitigate the impact of radiation-induced drift and mismatches in V_{TH} . Given a constant I_{DS} for a current mirror, V_{OV} remains constant and V_{TH} increases with TID [23]. Therefore, current mirrors used in bias distribution were designed such that $V_{GS} < V_{DD}$ and $V_{DSAT} < V_{DS} < V_{DD}$ across the TID specification.

Preventing SEU-induced errors in the analog circuitry predominantly involves minimizing the effect of ionizing particles on the capacitive DACs used by both the MDAC and SAR, as they occupy the most chip area. As an ionizing particle travels through the dielectric of a capacitor, such as in Fig. 5, it loses energy ΔE to the surrounding capacitor dielectric material [29]. ΔE is a function of the ionizing particle and energy, its trajectory, and the dielectric material's physical properties, and can be computed numerically [30], [31], [32]. The ΔE is typically proportional to the distance traveled, assuming the distance is significantly less than the ionizing particle's radiation length. The ΔE creates electron-hole pairs in the dielectric which manifests as a disturbance ΔQ in the charge held by the capacitor. The disturbance seen by the circuit is then $\Delta V = \Delta Q/C$. For a given value of C , a metal-insulator-metal (MiM) capacitor has a dielectric height that is approximately $30\times$ to $80\times$ thinner than a metal-oxide-metal (MoM) capacitor. Moreover, the MiM area is approximately $2\times$ smaller than the MoM. Therefore, the probability of an SEU in the MiM capacitor is halved, and assuming an SEU event, the resulting ΔQ would be $30\times$ to $80\times$ smaller than in an MoM. As a result, MiM capacitors are strongly

preferred [27], [28]. To further mitigate SEUs in the analog circuitry, capacitors smaller than about 2 fF are avoided, so that ΔV is minimized. However, this radiation-hardening measure increases the power consumption, due to the need to drive larger capacitances.

Radiation-induced destructive effects, such as latch-up, are avoided by the use of conservative layout rules as all transistors are within 15 μm of a V_{DD} or V_{SS} well tap. All transistors utilize a fully enclosed guard ring as its body terminal, except for standard logic cells which have their well taps as rows.

Predicting exactly how SEUs impact the ADC data is difficult as there are a myriad of possibilities. For example, a single ionizing particle can produce particle showers that can include heavy ions (or lighter elements) which deposit significantly higher (or lower) ΔE than the original particle. The ionizing particle can interact with the DAC, as described above, or hit an active element or junction anywhere else in the circuit. It also matters when ionization happens with respect to the operation of the particular circuit, such as whether the circuit is in sample or hold/quantization phase. It is also expensive and time-consuming to study each individual variable in situ using a radiation beam capable of producing SEUs, as real-time data acquisition, access to beam time, and statistics being the main limitations. Sub-blocks of this ADC were vetted by at least four previous tapeouts, each with their own radiation test, before culminating to the complete system shown here. Results from each radiation test were conclusive and consistent, and there was no need to deviate from the discussed design methodology and approach.

D. OTHER ARCHITECTURES CONSIDERED

A traditional MDAC-only pipeline architecture was not implemented because it would occupy excessive area and exceed the power budget, since each pipeline stage would require a residue amplifier. Similarly, a traditional SAR-only architecture was not implemented because a 15-bit, 40-MSPS SAR timing and comparator noise requirements would become too stringent and the capacitive DAC would become too large to meet the dynamic range requirement while maintaining the minimum DAC unit capacitance for radiation tolerance. Continuous-time delta-sigma (DSM) topologies [33], [34] are easier to drive from a transmission line, but they rely on over-sampling followed by decimation in the digital domain. The digital decimation filter relies on memory and multiply-add operations, and it is not clear how SEUs would affect the data or the amount of overhead needed to make the digital signal processing back-end to be sufficiently robust to SEUs. Therefore, a converter that processes one sample at a time is preferred. To achieve the necessary oversampling ratio for an effective 40-MSPS sampling rate, the required clock may exceed the 640-MHz clock frequency that can be provided by the HL-LHC infrastructure or require smaller technology nodes [35], [36], [37], [38], [39], [40], [41]. Nodes smaller than 65 nm

TABLE 1. MDAC+SAR bit weighting.

Bit Number	RDAC Ratio	CDAC Ratio	Comb. Ratio	Norm. Weight	Cum. Weight	Cum. Redun. Range
MDAC 1-8	1	1 / 8	1 / 8	4287		
Residue Amplifier Gain 4 V/V						
SAR first Stage	20 ^A	1	56 / 128	56 / 128	3584	8575
	19	1	32 / 128	32 / 128	2048	4991
	18	1	16 / 128	16 / 128	1024	2943
	17	1	10 / 128	10 / 128	640	1919
	16	1	6 / 128	6 / 128	384	1279
	15	1	4 / 128	4 / 128	256	895
	14	1	2 / 128	2 / 128	128	639
Residue Amplifier Gain 8 V/V						
SAR second Stage	13 ^A	1	7 / 32	448 / 2048	224	511
	12 ^A	1	4 / 32	256 / 2048	128	287
	11	1	2 / 32	128 / 2048	64	159
	10	1	1 / 32	64 / 2048	32	95
	9	48 / 64	1 / 32	48 / 2048	24	63
	8	32 / 64	1 / 32	32 / 2048	16	39
	7	20 / 64	1 / 32	20 / 2048	10	23
	6	12 / 64	1 / 32	12 / 2048	6	13
	5 ^B	8 / 64	1 / 32	8 / 2048	4	7
	4 ^B	4 / 64	1 / 32	4 / 2048	2	3
	3 ^B	2 / 64	1 / 32	2 / 2048	1	1
	2 ^B	1 / 64	1 / 32	1 / 2048	0.5	
	1 ^B	Comparator-only cycle		0.25		

^A Inter-stage redundancy.

^B Fixed (non-calibration) DAC weights.

are not viable options because of their cost and because their radiation-induced effects are not as well studied. The digital decimation filter in DSM topologies is logic intensive and may be impractical to implement while being radiation tolerant.

V. DESIGN OF SINGLE CHANNEL

Central to the MDAC+SAR approach is the inter- and intra-channel redundancy designed into each quantization step. Redundancy is required for foreground calibration to function and to maintain the required linearity of ≥ 11 ENOB throughout the pipelined stages. As tabulated in Table 1, certain bits overlap with the previous stage to provide redundancy. For example, the MDAC and SAR incorporate one bit of redundancy by using an MDAC gain of 4 V/V to map its residue ((1/8)th of full-scale) to half-scale of the SAR input. Subradix-2 DAC scaling provides intrastage redundancy where the SAR produces 20 subradix-2 bits and is summed to a 13 bit radix-2 code. The final MDAC+SAR arrangement yields an ADC with 15 bits of resolution to allow the required ≥ 14 bits of dynamic range.

A. MDAC CIRCUIT DESIGN

The MDAC has nine subranges (3.2 bits) and is designed to meet the dynamic range requirements and to handle the complex input impedance of the unterminated transmission line at the ADC input. Fig. 6 shows the circuit-level implementation of the MDAC stage, which comprises a thermometer DAC, a flash sub-ADC, reference buffers (two-stage OTAs in unity gain feedback), a residue amplifier, and a nonoverlapping clock generator. First, ϕ_r resets the charge

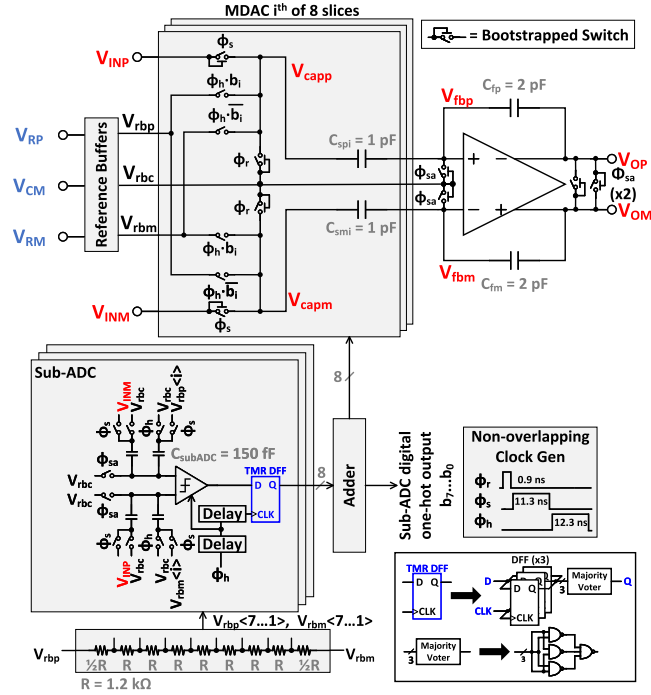


FIGURE 6. Implementation of the MDAC first stage and the radiation hardening design techniques employed.

on the sampling capacitors for about 0.9 ns at the beginning of the 11.3-ns sampling period (sample cycle in Fig. 4). Second, ϕ_s samples the input in both the DAC and sub-ADC simultaneously. Evaluation of the sub-ADC occurs at the beginning of ϕ_h (flash cycle in Fig. 4) and, finally, the sub-ADC digital output is used in setting the appropriate DAC level in ϕ_h where the SAR samples the amplified residue before the end of ϕ_h . Phases ϕ_s and ϕ_h are approximately equal in duration.

The main DAC and sub-ADC are thermometer coded to ensure monotonicity, using eight comparator thresholds to bin the sampled voltage into nine subranges (seven full subranges and two half-subranges). Each comparator threshold is associated with 1 of 8 slices (Fig. 6) and all slices in total present 8-pF single-ended sampling capacitance, C_{spi} and C_{smi} . The sampler presents about $41.9\text{-}\mu\text{Vrms}$ differential kT/C noise out of the total $75.2\text{-}\mu\text{Vrms}$ differential noise at the output of the MDAC, as reported by PSS/PNOISE simulation. Quantization noise is relatively insignificant at $(2\text{ Vpp})(1/2^{15}\sqrt{12}) \approx 17.6\text{ }\mu\text{Vrms}$. The estimated achievable dynamic range is $(2\text{ Vpp})(1/\sqrt{2}) \approx 1.41\text{ Vrms}$ of a full-scale, differential sinusoid divided by approximately $\sqrt{(75.2\text{ }\mu\text{Vrms})^2 + (17.6\text{ }\mu\text{Vrms})^2} = 77.2\text{ }\mu\text{Vrms}$ of differential noise which yields 85.2 dB or 14.2 bits of dynamic range, assuming none of the 2^{15} codes are missing. Bottom-plate sampling [42], [43] makes the DAC insensitive to parasitics on the top-plate nodes V_{fbp} and V_{fbm} , where the phase ϕ_s is the time delayed version of ϕ_{sa} by about 0.5 ns. All switches controlled by ϕ_s , ϕ_{sa} , and ϕ_r are bootstrapped switches [44] whereas the ϕ_h

switches are single nMOS or pMOS pass transistors for the (buffered) negative reference (V_{rbn}) or positive reference (V_{rbp}), respectively. The bootstrapped switches use the low-impedance side, such as the input signal or V_{rbp} , as the switch's reference to apply the bootstrapping. The ϕ_{sa} switch between V_{OP} and V_{OM} are two bootstrapped switches in parallel with opposing polarities to maintain differential balance. The input bootstrap switches are sized to minimize C_{SD} extrinsic capacitance when open [45], [46] and to minimize nonlinearity when closed [47]. Both phenomena cause harmonic distortion that cannot be calibrated in the digital domain [48], and hence need to be minimized in design.

Due to the presence of the unterminated transmission line at the input, as discussed in Section III, the reset phase, ϕ_r , is key to ensure linearity of the sampling circuit. The sudden opening and closing of the sampling switch into the sampling capacitor creates broadband kickback in the absence of termination. This is problematic when any high- Q elements immediately precede the ADC, such as a transmission line, the parasitic inductance from the bondwires, or a bandpass filter used in sinusoid testing. To address this, the reset phase momentarily closes a bootstrapped switch between the MDAC input and common-mode V_{rbp} while the input bootstrapped switch is open. This resets the charge in the sampling capacitors prior to sampling the input voltage. While high- Q ringing and reflections due to kickback are inevitable, the reset phase ensures time invariance such that the settling characteristic of the input network are identical for each sample regardless of the previous cycle [49], [50], [51]. Without the reset phase, the sampled charge would become signal-dependent as it is a function of the present voltage and the initial conditions of the sampling capacitor from the previous sample's hold phase and sub-ADC state. This signal-dependent behavior would manifest as harmonic distortion.

A clocked double-tail comparator is utilized in the sub-ADC [52]. A resistor string DAC generates the reference voltages for use in the flash sub-ADC. Metastability is avoided by using delay cells to asynchronously time the comparator and latching circuit [53]. Bubble errors are avoided by using digital adder cells to sum the sub-ADC thermometer code, making the digital data agnostic to the specific subranges [54]. Mismatch between the sub-ADC and the cap-DAC is tolerated thanks to interstage redundancy, as the MDAC output would still linearly settle if the residue output is slightly beyond the half-scale output. The sub-ADC data is stored in triple-majority redundant (TMR) registers to be robust against SEUs. Since the deposited energy from an ionizing particle can diffuse in the substrate and disrupt neighboring logic cells tied to the same majority voter (MV), the triplicated registers are spaced a minimum of $15\text{ }\mu\text{m}$ apart in the silicon.

The MDAC residue amplifier presents a closed-loop gain of 4 V/V to amplify the MDAC residue to $(1/2)$ full-scale of the SAR input, thereby providing 1 bit of interstage

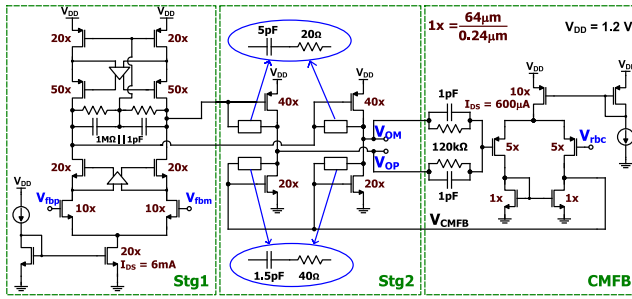


FIGURE 7. Circuit diagram of the MDAC residue amplifier.

redundancy. The MDAC residue gain would otherwise be 8 V/V for a system with no interstage redundancy, amplifying the residue from one subrange back to full-scale. The residue amplifier is integrated into the main DAC as part of the closed-loop feedback network. The MDAC residue amplifier (Fig. 7) is a two-stage OTA whose first stage is a gain-boosted telescopic stage. The second stage is Miller compensated for stability. To allow smaller V_{GS} , low- V_{TH} core 1.2 V devices are mostly used. The gain error is suppressed to maintain the linearity of the residue signal by designing for a loop gain of 86 dB. Proper driving of the SAR and settling during ϕ_h is achieved by designing for a unity-gain bandwidth greater than 300 MHz. A continuous-time, active common-mode feedback (CMFB) circuit with 50-dB common-mode rejection sets the dc operating point of the amplifier and the common-mode voltage seen by the SAR.

The nodes V_{rbp} , V_{rbc} , and V_{rm} in Fig. 6 represent the buffered references of V_{RP} , V_{CM} , and V_{RN} , respectively, for use in the MDAC that originate from the on-chip bandgap and reference generating circuit (Section VI-A) shared between all channels. As indicated in Fig. 4, the two SAR stages perform conversion at the same time while the MDAC is sampling the next sample. Hence, the MDAC and SAR utilize separate reference buffers to minimize channel-to-channel and stage-to-stage crosstalk. The reference buffers are two-stage, folded-cascode, Miller compensated OTAs in unity-gain negative feedback; the positive and common-mode buffers use an nMOS input pair variant and the negative buffer uses a pMOS input pair variant. The positive and negative buffers are responsible for driving each of the eight MDAC slices during the 12.5-ns hold phase, and the common-mode buffer is responsible for proper sampling and resetting of the residue amplifier during the 12.5-ns sample phase. Each buffer consumes approximately 7.8 mW with an open-loop gain of 40 dB and unity-gain bandwidth of 170 MHz. This allows the buffers to settle to 14-bit precision for an 8-pF load in 9.7 ns, which is under the 12.5-ns requirement of the MDAC.

B. TWO-STAGE SAR CIRCUIT DESIGN

To meet the SNDR requirement, the two-stage SAR following the MDAC is a 13-bit, 2-stage asynchronous SAR. Due

to the built-in redundancy indicated in Table 1, the SAR performs a total of 20 comparisons per sample to produce 8575 codes, while the MDAC is designed to use half of this range. The circuit-level implementation of the two-stage SAR is shown in Fig. 8. The first SAR stage allocates (1/4) of a 25-ns clock period (Fig. 4) to sample the later half of the MDAC residue amplification stage, (1/2) period to perform seven comparisons, and then (1/4) period to amplify the residue to the SAR second stage. The second SAR stage allocates (3/4) period to perform 13 comparisons. Most of the 25-ns clock cycle is allocated for SAR conversion in the second stage, as performing 13 comparisons places a stringent timing requirement on the maximum allowed time per conversion.

Similar to the MDAC, the SAR DAC utilizes bottom-plate sampling and bootstrapped switches for the input and V_{CM} , and individual nMOS (pMOS) for switching negative (positive) references. Bootstrapped switches are used in the SAR primarily for their low ON-resistance, rather than for their linearity across input voltages; switch linearity is not as crucial in the SAR because the voltage sampled by the SAR is already steady-state and driven by the MDAC residue amplifier. To save power and simplify the routing of the DAC, a split-capacitor DAC [55], [56] is used, as it does not need a common-mode reference. The SAR first-stage and second-stage single-ended unit capacitances are 17 and 9.6 fF, respectively. To mitigate SEU-induced errors, as discussed in Section IV-C, the SAR first-stage DAC is sized to be 2.17 pF (17 fF $\times$ 128 units from Table 1) single-ended. This is several times more than the capacitance needed to satisfy thermal noise requirements alone, and increases the power required by the MDAC to drive the SAR DAC.

The second stage utilizes a hybrid resistive DAC where a resistive DAC helps to scale the references for the lower 8 physical bits to keep the overall DAC size manageable for the residue amplifier to drive without spending excessive power. The second stage capacitive DAC employs reference scaling [57] to halve the full-scale voltage range. As discussed in Section IV-C, minimum-sized metal fringe capacitors cannot be used due to radiation vulnerability. The second stage has 12 DAC slices and a “free” bit (bit #1 in Table 1) is gained by strobing the comparator an additional cycle after the LSB capacitor slice is set. The SAR second-stage hybrid DAC is sized for a total capacitance of 307 fF (9.6 fF $\times$ 32 units) single-ended and a total resistance of 500 Ω (7.81 Ω $\times$ 64 units). Although resistors are assumed to be insensitive to SEUs, the unit resistance of the resistor string is minimized as any transient ΔV due to an SEU would cause the DAC to resettle according to the RC constant of the hybrid DAC. Lowering the hybrid DAC’s sensitivity to SEUs implies lowering R and dissipating more power in the reference buffer to drive the resistor string.

The SAR residue amplifier presents a closed-loop gain of 8 V/V with 2 bits of interstage redundancy, and is incorporated in the main DAC as part of the closed-loop feedback network. The SAR first stage resolves 2^6 coarse

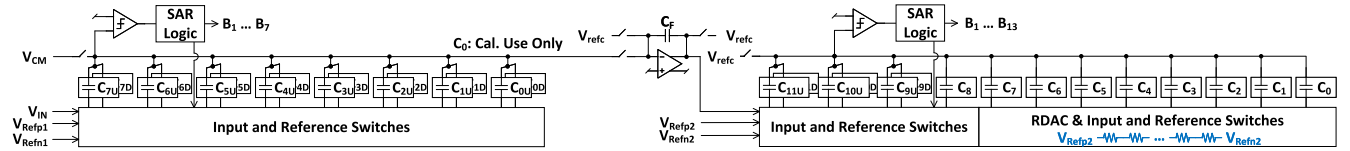


FIGURE 8. Circuit implementation of the two-stage SAR. Actual implementation is fully differential.

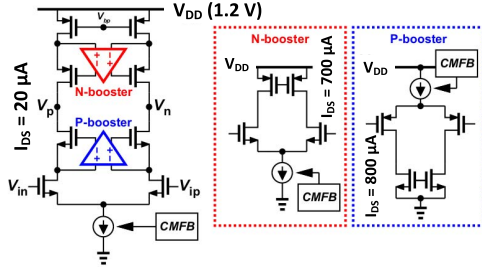


FIGURE 9. Circuit diagram of the SAR residue amplifier.

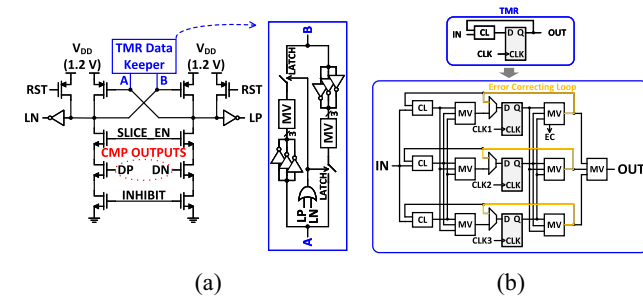


FIGURE 10. (a) TMR implementation of a dynamic logic latch used in the SAR. (b) TMR equivalent of a nonhardened finite state machine incorporating synchronous and combinational logic (CL) and MVs. CLK1, CLK2, and CLK3 are synthesized as separate clock trees but originate from the same clock signal.

LSBs, which is indicated in Table 1 by adding the SAR first stage bit weights and normalizing by the LSB of the SAR first stage. Accounting for the half-scale of the SAR second stage plus the two bits of interstage redundancy, the residue gain is $2^6/2^{1+2} = 8$ V/V. The SAR residue amplifier in Fig. 9 is a one-stage gain-boostered telescopic stage, similar to that of the MDAC. The CMFB utilizes a discrete-time, switched-capacitor architecture [58], [59], which is simpler to implement and stabilize than a continuous-time active CMFB. Although it takes multiple clock cycles to settle, any common-mode perturbation at the input is already suppressed by the active CMFB in the MDAC.

The SAR uses a clocked double-tail comparator and asynchronous logic. Current-mode logic is used in the SAR logic to meet the speed requirements. TMR keeper cells [Fig. 10(a)] are used to protect the stored data from SEU-induced bit flips. Should metastability occur in the SAR conversion cycle, the specific sample data is corrupt as the lower bits would not be resolved but the SAR logic state machine is reset by the next sampling edge. There is no dedicated circuitry to prevent metastability within the

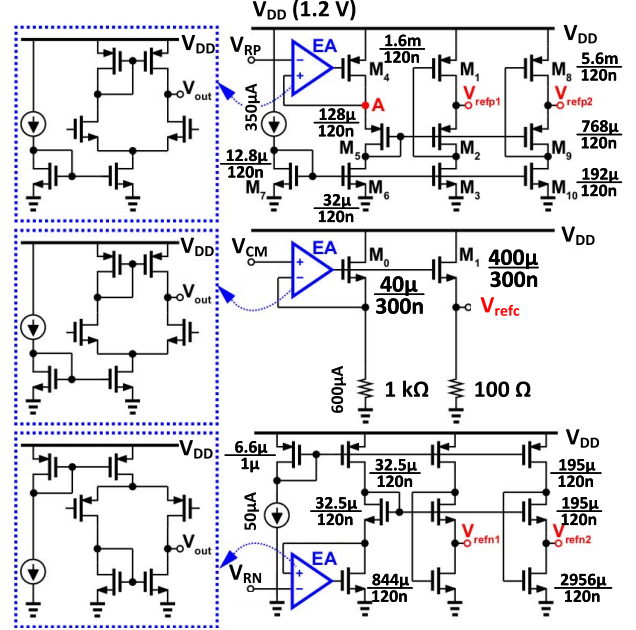


FIGURE 11. Circuit diagram of the SAR reference buffers. The references for the SAR first (V_{refp1} and V_{refn1}) and second (V_{refp2} and V_{refn2}) stages are separated to reduce cross-talk between stages.

SAR which would risk exceeding the maximum time per conversion in the asynchronous, self-timed SAR logic.

The positive and negative SAR reference buffers utilize a flipped-voltage-follower (FVF) [60], [61] topology, as depicted in Fig. 11, to meet the stringent settling requirements, given that 13 and 7 conversions must be done within a 25-ns clock period for the second and first stages, respectively. The FVFs are replica biased to relax the bandwidth and stability requirements of the error amplifier and to isolate the two SAR stages since they convert simultaneously.

C. DIGITAL BLOCKS

Each ADC channel incorporates a DDPU and a digital control block to apply calibrated weights to the quantized ADC data. The DDPU and digital control in each channel operate independently of each other, and integrate the ADC with the rest of the readout system.

The digital control block acts as a 544-bit volatile configuration memory for the operation of the MDAC and SAR, and provides calibrated bit weights to the DDPU. The memory registers persist once they are programmed via I²C once on power-up after calibration. As depicted in Fig. 10(b),

the state machine is designed with error correction [62], in addition to TMR. The state machine operates at 40 MHz and idle states are used to check the consistency of TMR memory and correct if necessary, whereas a non-TMR state machine would otherwise be idle. Periodically checking TMR consistency limits the time in which the memory is vulnerable to bit flips from SEUs before the data is refreshed. If data in a TMR-protected register goes without error checking for a prolonged period of time, a single-bit error can accumulate into double- or triple-bit errors, at which point the MV is “tricked” into “correcting” to the wrong bit value. To avoid one SEU-inducing particle causing double- or triple-bit flips, TMR-correlated logic cells are spaced a minimum of 15 μm apart in the silicon. To allow the running cumulative number of single-bit errors to be read out via I²C for informational and monitoring purposes, each MV produces an error count (EC) flag and all ECs are summed in a TMR counter.

The DDPU combines all MDAC and SAR bits to form a linear ADC transfer function, applies calibration weights, and serializes the digital result at a rate of 640 Mb/s per channel. Additionally, sample timestamping and identification metadata are generated by the DDPU to allow straightforward reconstruction of detector events from all $\sim 182\text{k}$ LAr channels. The DDPU circuitry is not triplicated because it is stateless and the data handled by the DDPU is refreshed at a minimum frequency of 40 MHz. Therefore, an SEU in the DDPU would, in the worst case, result in only one erroneous sample.

D. CHANNEL CALIBRATION

Static foreground calibration to correct for DAC weighting and interstage gain errors is implemented for each channel, while scale and offset errors between separate ADC channels are handled by the readout system-level calibration. Both the MDAC and SAR repurpose the existing circuitry when in calibration mode. This approach helps guarantee that conditions during calibration match the conditions during normal operation, and avoids the need of any external components or biases which would present a vulnerability to radiation. The built-in redundancy is necessary for the foreground calibration operation to converge, as the procedure is recursive starting at bit #6 in the SAR (Table 1) and ends with each of the MDAC thermometer-coded DAC slices. The first five bit weights in the SAR are fixed, and are used to calibrate the higher bits. The true weight of each calibrated bit can be downloaded via I²C and stored in the volatile, TMR-protected memory of the digital control registers, which the DDPU uses in regular operation to correct and reconstruct the binary data.

SAR DAC slice weight and interstage gain are calibrated by relying on the lesser DAC slices [63], [64]. Bits 1 and 2 have a normalized weight of less than 1 LSB because they only yield noise in normal operation; however, thanks to averaging, they can yield useful information in calibration mode. Calibration starts by forcing the positive reference to

positive-DAC (P-DAC) bit #6, while operating bits 5 and lower as a normal SAR where their designed weights are assumed to be exact, and while the N-DAC and higher bits stay stationary at common-mode. The weight of the DAC slice being calibrated, plus the comparator offset, cannot be more than the cumulative sum of the lower DAC slices; otherwise, an under/over-range condition occurs and the true DAC weight cannot be accurately quantized. Hence, a subradix-2 DAC arrangement with sufficient intrastage redundancy is necessary for this algorithm to converge. The negative reference is then forced and the resulting difference is taken which represents the weight of this DAC slice in the P-DAC. The process is repeated recursively for the higher bits, then repeated for the N-DAC while keeping the P-DAC stationary. The P-DAC and N-DAC in the fully-differential architecture are calibrated pseudo-differentially to cancel the effect of comparator offset.

Like the SAR, DAC weighting and interstage gain are calibrated in the MDAC [65], [66]. The MDAC calibration procedure relies on a calibrated SAR, so the SAR is calibrated first. MDAC calibration is then performed by forcing a specific subrange in the sub-ADC. The cap-DAC is configured to present a charge equivalent first to the lowest, and then to the highest, MDAC residue and the results are quantized by the SAR. Many samples are averaged and the difference is taken. The difference captures the size of each specific MDAC subrange and the interstage gain of the residue amplifier, and is robust against comparator, sub-ADC, and residue amplifier offset errors, as long as any under- or over-ranging values remain within the 1 bit of interstage redundancy.

VI. MULTICHANNEL INTEGRATION

The eight channels on each ASIC (Section V) are identical by design and operate independently. To avoid external components, allowing for better scalability and less radiation vulnerability, both the ADC analog inputs and digital data outputs are dc-coupled. Centralized, shared blocks include a bias and reference generator and clock receiver and divider, and their distribution networks.

A. REFERENCE GENERATION AND DISTRIBUTION

Fig. 12 depicts the dc biasing scheme for all eight channels. All biases originate on-chip from a Banba bandgap (BGP) [67] using diode-connected DTNMOS [68] devices for 1.2-V operation, which are enclosed-layout transistors (ELTs) for radiation robustness [22], [26].

To adapt to the strategy used by the PA/S ASIC which drives the ADC inputs, the voltages V_{RP} (nominally 1.1 V), V_{CM} (nom. 0.6 V), and V_{RN} (nom. 0.1 V) scale with $(V_{DD} - V_{SS})$ and use the on-chip BGP to maintain a fixed headroom away from V_{SS} and V_{DD} . Digitally programmable resistive DACs are used to fine-tune each voltage reference. The PA/S and ADC for a given channel are powered from the same off-chip voltage regulator, so that a given PA/S channel and ADC channel see the same full-scale

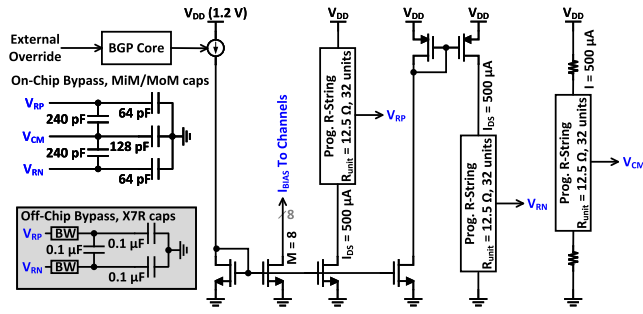


FIGURE 12. Schematic of the shared bandgap and reference generation circuit. “BW” represents the presence of a bondwire.

reference. Disturbances on $(V_{RP} - V_{RN})$ are minimized using on-chip and off-chip bypass capacitors. This approach, in combination with the resistive DACs, creates a low-pass corner whose time constant is set significantly above the duration of an LAr pulse being digitized (Fig. 2). Lastly, biases for analog blocks, such as amplifiers, are distributed as currents to all eight channels.

B. GENERATION AND DISTRIBUTION OF CLOCK PHASES

Fig. 13 shows the central clock divider and distribution circuitry shared among all eight channels. The central clock divider receives a low-jitter, 50% duty cycle, 40-MHz clock and a 640-MHz clock from the IpGBT data aggregator ASIC. The 40-MHz clock is used for sampling by the MDAC so it needs to have low jitter and low duty cycle distortion. The 640-MHz clock from the IpGBT is used for serialization purposes only by the DDPU as it is not a precise clock suitable for analog use. The central clock divider edge-aligns the received 640-MHz clock with the 40-MHz clock, such that the received clocks CLK40_IN and CLK640_IN can have arbitrary timing relations, which simplifies system implementation. The circuit also derives an intermediate 80-MHz clock phase for use in the SAR (quarter-duty cycle SAR operations in Fig. 4) and DDPU. The divide-by-8 circuit to derive the 80-MHz clock uses a TMR-protected Johnson counter to synchronize to the rising edge of the 40-MHz clock (C40_EDGE). The clock alignment monitor, composed of several DFFs, registers specific clock edges to signal a proper relationship between the 40, 80, and 640 MHz clock edges. Lastly, a redundant bunch-crossing reset (BCR) trigger signal is received to synchronize the timestamping counter inside all DDPUs. A binary clock tree distributes the 40, 80, and 640 MHz clocks and the BCR signal with equal clock skew between all channels.

To avoid having to distribute many clocks with precise duty cycles and skews, the MDAC and SAR nonoverlapping clock phases are generated within the MDAC and SAR blocks themselves. All other derived clock phases used within the MDAC and SAR are synchronous to the 40, 80, and 640 MHz clocks provided by the TMR-protected clock divider. All state machines inside the MDAC and SAR are

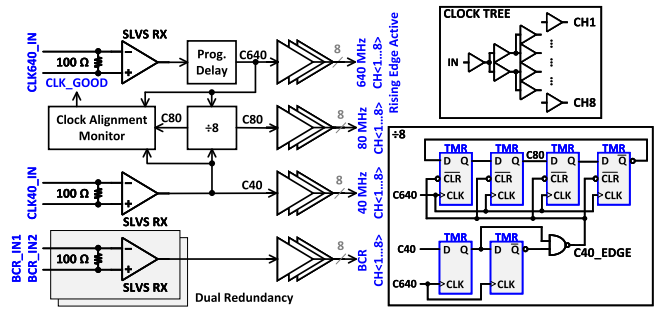


FIGURE 13. Block diagram of the shared clock distribution circuit and clock distribution scheme for all eight channels.

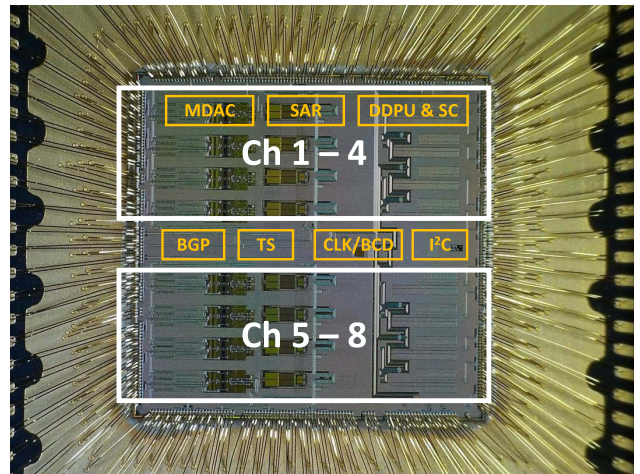


FIGURE 14. Micrograph of the 5.5 × 5.8 mm² chip packaged in a QFN package. The shared blocks in the middle, including the TS (test structures), clock divider and timestamping (CLK/BCD), I²C state machine, and the blocks in the top channel, are annotated.

reset by the 40-MHz clock cycle to guarantee that an SEU would only result in a single corrupt sample instead of a cascade of samples or worse. Only the MDAC and SAR nonoverlapping clocks, including the MDAC sampling clock, are sensitive to jitter and duty cycle distortion on the 40-MHz clock domain. To equalize the timing skew across all eight channels, the precision 40, 80, and 640 MHz, and BCR signals are distributed using a binary clock tree. Additive jitter and duty cycle distortion on the precision 40-MHz sampling clock is minimized by reducing the amount of logic and buffers in its path. Jitter and distortion are not concerned for the 80 MHz, 640 MHz, and BCR clocks, as all circuitry that use these clocks are synchronous and exclusively rising-edge sensitive. For example, the 80-MHz clock is guaranteed to have 50% duty cycle thanks to the Johnson counter’s synchronous design.

C. CHIP INTEGRATION

The chip die in Fig. 14 features 366 bondpads, and is wirebonded into either a 100-pin QFN package or a 196-ball BGA package; most wirebonds are either double-bonds, to reduce wirebond parasitics, or down-bonds to ground.

All eight ADC channels are identical by design. To reduce crosstalk, guard rings, employing the deep-N-well layer,

surround each major block, such as each MDAC, SAR, reference buffers, and the digital backend of each channel. The eight channels are split into two groups of four channels each, with shared blocks in the center.

The floorplanning and signal flow of the chip is done such that the sensitive analog signals, precision clocks, high-speed digital signals, and power traces on the front-end boards can be routed with minimal crosstalk. The left-hand side of the chip carries only sensitive analog signals, such as the analog input from the preceding PA/S ASIC and decoupling connections for the on-chip bandgap. The right-hand side of the chip carries only high-speed digital signals and interfaces with the succeeding data aggregator ASIC. The serializer and sampling clocks arrive from the bottom-right corner and are routed from there to between channels 4 and 5 for chip-wide distribution. Power arrives on the top and bottom sides of the chip, and is routed vertically within the chip. Power domains between the MDAC and SAR and between the top four and bottom four channels are separated to further mitigate crosstalk and to allow easier routing of sensitive analog signals in the center of the ASIC around the BGP. Bulk on-chip bypass capacitors exist for each V_{DD} domain.

VII. EXPERIMENTAL RESULTS

This section summarizes the results of measurements which were done to check if the ADC meets the requirements set forth in Section III, including the analog performance, robustness, reliability, and radiation tolerance. A total of 18 randomly chosen devices were packaged and tested out of 100 available devices from the MPW fabrication run. Results shown are for one channel on a random ASIC after calibration unless otherwise specified.

A. SINGLE-TONE SINUSOID PERFORMANCE

A single-tone sinusoidal signal up to the Nyquist frequency is used as a proxy for evaluating the analog performance of the ADC for use in the ATLAS LAr HL-LHC readout system. Analog performance using actual LAr pulses as input will be presented in a future publication about the ATLAS upgrade.

All sinusoid measurements were made with bandpass filters of the appropriate frequency. The test board includes a similar 20-cm, un-terminated transmission line as discussed in Section II. Fig. 15 summarizes single-sinusoid analog performance of the ADC. The SNDR remains above 11 ENOB (68-dB SNDR) at full scale across the Nyquist bandwidth and the simulated performance aligns closely with the measurements. The spectral performance near Nyquist becomes distortion-limited, with an SDR of 85.5-dBc near dc deteriorating to 77.5 dBc. Worst-case performance at -1 dBFS is with a 19-MHz input frequency, achieving 11.4 ENOB (70.3-dB SNDR). Example FFT results are shown in Fig. 15(c) and (d) for frequencies of 1 and 19 MHz, respectively.

Fig. 16 shows the sinusoid performance in the context of the LAr calorimeter performance and specification as

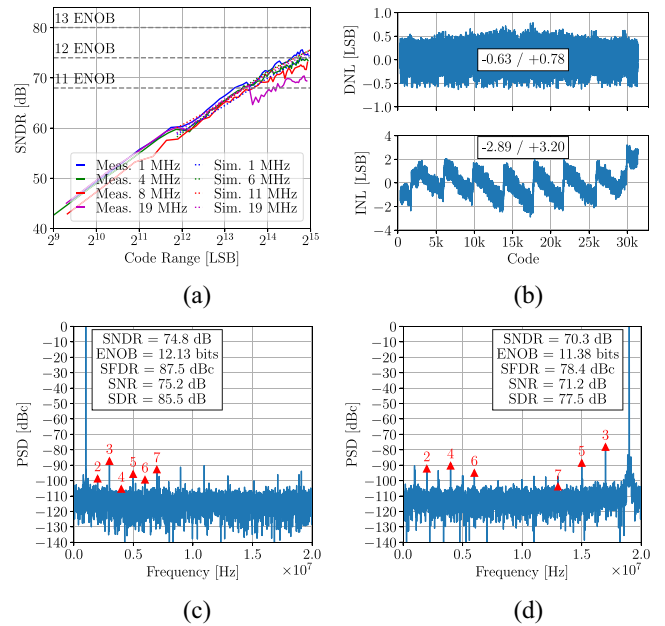


FIGURE 15. Sinusoid measurements of (a) SNDR versus amplitude; (b) INL/DNL derived from 80M samples of 2-MHz full-scale sinusoid data; 8000-point FFT at -1 dBFS and approximately (c) 1 MHz and (d) 19 MHz.

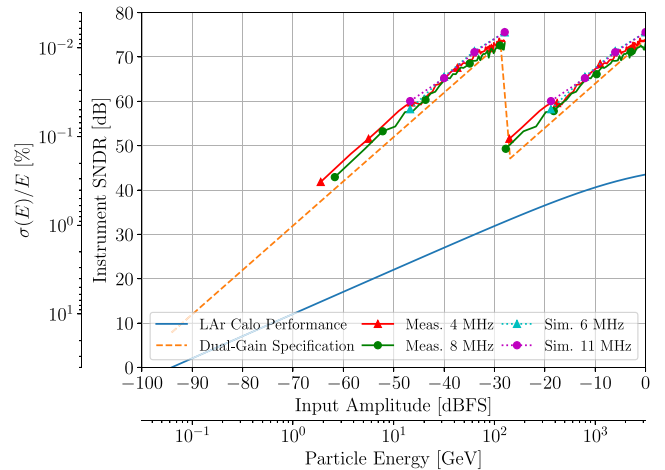


FIGURE 16. Simulated and measured SNDR performance with emulated HG/LG gain switching in context from Fig. 3, showing that the ADC performance exceeds the analog requirements of the readout system discussed in Section III.

described in Section III-A, demonstrating that the ADC exceeds the HG/LG two-gain system specification.

B. RESOLUTION AND DYNAMIC RANGE

There are no missing codes across the 2^{15} LSB resolution. As shown in Fig. 15(b), the measured DNL is constrained within approximately ± 0.8 LSB while the INL spans approximately $-2.9/+3.2$ LSB. This is expected as the ADC is an ≥ 11 ENOB ADC with a 15-bit code range. The artifacts from the eight MDAC subranges are clearly visible in the INL, as expected.

An ac-short was presented at the ADC input by shorting the differential inputs together and to a low-impedance dc

TABLE 2. Power breakdown.

Power Rail	Power [mW]		% of Total Chip Power
	per Channel	per Chip	
MDAC Analog	23.0	184.2	16.8
MDAC Ref. Buf.	33.9	271.5	24.7
SAR Analog	5.4	43.5	4.0
SAR Residue Amp	15.0	119.7	10.9
SAR Ref. Buf.	42.4	338.9	30.9
SAR Digital	1.2	9.8	0.9
Test Structures	1.7	13.3	1.2
CLK RX + DDPU	14.2	113.5	10.4
Bandgap	0.3	2.6	0.2
Total	137.1	1096.8	100

source set at the designed common-mode input voltage of 0.6 V. 10M consecutive samples were collected to measure the noise of the ADC. The resulting noise distribution had a range of 11 LSBs with no outliers and a standard deviation of 1.22 LSBrms. Given that there are no missing codes from the measured DNL data, the measured input dynamic range of the ADC is therefore $(2^{15} \text{ LSB})(1/\sqrt{2}) \approx 23170 \text{ LSBrms}$ of a full-scale sinusoid divided by the 1.22 LSBrms of measured noise. This equates to approximately 85.5 dB or 14.2 bits of measured dynamic range as predicted in Section V-A. The measured noise does not vary significantly with the input differential voltage.

C. POWER CONSUMPTION AND LOT TESTS

Table 2 summarizes the power consumption by circuit block and by channel. The ADC chip consumes a total power of 1.1 W, or 137.1 mW/channel, which is compatible with the power budget for the total system of 182k LAr channels.

Among the 18 devices, the measured minimum/average/maximum SNDR of the lot with a 5-MHz full-scale sinusoid was 69.5/71.6/73.0 dB and the total chip power consumption was 1.09/1.13/1.16 W, respectively. Performance between channels of a certain ASIC is indistinguishable from performance between ASICs.

D. RADIATION HARDNESS CHARACTERIZATION

Table 3 summarizes radiation robustness data on five randomly selected devices. These devices were soldered on individual testboards, designed such that only the packaged chip could be exposed to radiation. Irradiation using a monoenergetic beam of 229 MeV protons, directed at an angle approximately normal to the top of the chip, was performed at the Francis H. Burr Proton Therapy Center at Massachusetts General Hospital [69], [70]. As summarized in Table 3, each of the five ADC ASICs was separately exposed, over a period of typically a few hours, to a total number of energetic protons per unit area which would allow measurements confirming that the design exceeds the TID, NIEL, and SEU requirements over the HL-LHC operating lifetime (see Section III-B). During irradiation, all channels were operated at the nominal 1.2-V V_{DD} and 40-MSPS quantization rate. The instantaneous beam intensity was varied, and no dose rate-dependent effects were observed;

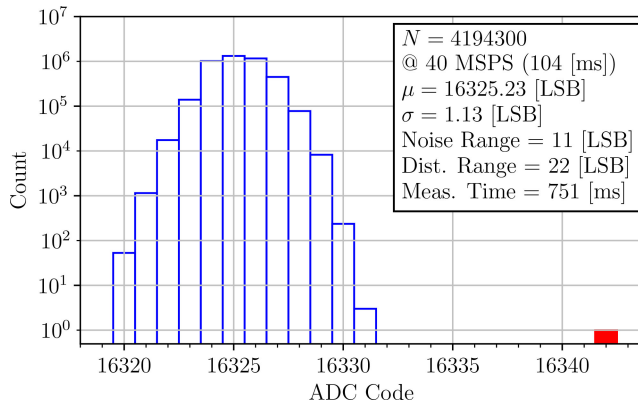
therefore the data is believed to be an accurate extrapolation of radiation robustness over the HL-LHC operating lifetime.

Full-scale 5-MHz sinusoid data, similar to Fig. 15, was taken on four of the eight channels before, during, and after irradiation on all five boards. Prior to irradiation, MDAC and SAR bit weights were foreground calibrated and before-irradiation sinusoid data was taken. After irradiation, only the MDAC was recalibrated followed by recording after-irradiation sinusoid data. Bias settings in the digital control block were kept constant before, during, and after irradiation. The worst-case MDAC calibrated bit weight deviated by no more than 10 LSBs out of the 2^{15} LSB full-scale and the worst-case performance degradation was no more than 0.5 ENOB between before- and after-irradiation. No latch-ups were observed, and the ADCs were never power cycled during irradiation. The ADC current consumption and temperature, using a PT1000 RTD sensor attached with thermal paste to the top of the QFN package, was monitored. The worst-case power consumption and temperature drift seen by each of the five ASICs were 16.4 mW and 2.3 °C, respectively.

Four of the eight channels were connected to an external differential DAC that cycled through dc values between negative and positive full-scale. At each DAC setting for one of the four channels, a continuous $2^{22} - 4$ samples, representing approximately 104 ms of data per channel, were histogrammed. This process was repeated throughout the radiation test. A filter was applied to the histograms to count the number of samples that fall more than 2 LSBs away from the main noise distribution; these outliers were then labeled as SEU candidates, such as the example shown in Fig. 17. The overhead of ADC data acquisition was the main limitation of statistics for this test, as one histogram represents 104 ms of continuous data but each measurement takes a total of 751 ms, including the time it takes to save the data onto a PC. No relationship between the external DAC code and SEU frequency was observed. These observed SEUs are representative of the entire analog quantization circuitry and the non-TMR DDPU circuitry. The in-beam data is contrasted against dry-run data (i.e., in the absence of intentional radiation), where the exact same procedures and setup were replicated in a nonradiation environment prior to radiation testing. ADC calibration and bias settings stored in the digital control block were kept fixed during histogramming in both in-beam and dry-run data to have a consistent comparison. Approximately 50 times more total samples were collected in the dry-run data than the in-beam data, but only 84 out of the 2.21×10^{12} dry-run data samples were flagged as SEUs using the same analysis procedure. These 84 potential “SEUs” in the dry-run data were samples that were more than 2 LSBs away from the main noise distribution. This can be caused by stochastic noise of the DAC or the ADC itself, metastability in the SAR, bit-error in the serial transmission of data from the ADC to the FPGA, or other rare mechanisms. While these 84 samples may be due to nonradiation effects, the $\sim 20\times$ increase in SEU samples

TABLE 3. Radiation data summary.

Chip No.	In-Beam Data						Dry-Run Data			
	Fluence [p/cm ²]	TID [Gy]	Valid Samples	SEU Samples	Single-Bit Errors	Double- and Triple-Bit Errors	Valid Samples	SEU Samples	Single-Bit Errors	Double- and Triple-Bit Errors
1	7.55×10^{13}	4.08×10^4	8.24×10^9	318	25319	4	5.54×10^{11}	15	0	0
2	5.02×10^{13}	2.71×10^4	1.15×10^{10}	378	17177	1	2.59×10^{11}	11	0	0
3	4.98×10^{13}	2.69×10^4	8.09×10^9	286	16568	4	7.10×10^{11}	25	0	0
4	5.47×10^{13}	2.96×10^4	8.87×10^9	490	17787	2	3.76×10^{11}	13	0	0
5	5.00×10^{13}	2.70×10^4	7.32×10^9	295	18320	0	3.10×10^{11}	20	0	0
Total	2.80×10^{14}	1.51×10^5	4.40×10^{10}	1767	95171	11	2.21×10^{12}	84	0	0


FIGURE 17. Single histogram with a single sample (in solid red) flagged as an SEU candidate, among the noise distribution (in blue outline). Note the logarithmic y-axis.

in $\sim (1/50)$ th of the data between the dry-run and in-beam data is attributed to SEUs caused by the irradiation.

The digital control block (Section V-C) is critical as it stores bias and calibration settings necessary for proper ADC operation. These settings are expected to persist throughout the operation of the ADC and thus are implemented with TMR [Fig. 10(b)]. EC counts from the TMR state machine implementation depicted in Fig. 10(b) of the TMR digital control block are summed throughout the irradiation and represent single-bit errors. These errors are benign, as the TMR registers are refreshed and corrected every 40-MHz period. However, some uncorrectable double- and triple-bit errors occur before the next clock cycle. These double- and triple-bit errors occur significantly less often, as expected for a TMR design. The double- and triple-bit errors are detected by periodically reading back all memory registers and comparing them to the initial programming. Interim ADC data is also discarded when such errors occur, since the ADC is then in an unknown state. The memory registers are then reprogrammed and data collection resumes. These in-beam digital control single- and multiple-bit errors are contrasted to zero such errors in dry-run data, as expected.

Extrapolating the error rates to all channels over the operational lifetime of the HL-LHC, it is expected that each of the ~ 364 k ADC channels will experience 540 SEUs in the data, where 75% will be within 20 LSBs and less than 1% of those SEUs will be at least 100 LSBs away from the correct value. Similarly, each ADC channel is statistically

expected to experience 0.018 instances of TMR corruptions in the digital control registers, which would necessitate a reprogramming of the ADC. These SEU rates are easily tolerable at the system level in the ATLAS application.

In summary, making the ADC robust against TID effects and latch-up mostly involve conservative layout and biasing techniques. Making the ADC robust against transient bit errors and SEUs mostly involve the use of large MiM capacitors in the analog circuitry and TMR, spacing out TMR registers, error-correcting state machines, and reducing the data's temporal and spatial footprints in the digital circuitry.

VIII. COMPARISON

The performance of this ADC is compared in Table 4 against other radiation-hardened by design (RHBD) ADCs with similar quantizer specifications. This ADC is to replace the aerospace-grade, commercial device AD9042S [71] used in the current LAr calorimeter readout [6] due to resolution and system (including density, power, and cost) reasons. The RHBD techniques are not without design tradeoffs, for example, the increased area, design complexity, and power consumption compared to non-RHBD counterparts. For example, triplication and large sampling capacitances directly increase area and the power needed to drive such capacitors. Error-correcting state machines and TMR digital logic infer complex state machines and necessitate faster clock speeds for functions that may otherwise be trivial to implement without RHBD techniques. Despite this, the ADC achieves a competitive Schreier figure-of-merit (FoM_S) of 151.9 dB when considering SNDR and total aggregate channel power consumption among RHBD ADCs, which includes overhead for RHBD circuit techniques, shared blocks, and system-level integration. The ADC achieves the most resolution with 15 bits compared to other RHBD and non-RHBD (14.0 bits [10], [72] and 13.0 bits [73]) ADCs. Furthermore, it is the only ADC in comparison to achieve 14.2 bits of dynamic range using a single 1.2-V supply. The ADC achieves a competitive SNDR across the Nyquist range, 70.3 dB at Nyquist, compared to other RHBD and non-RHBD (at Nyquist: 75.7 dB [72] and 70.9 dB [73]) ADCs. When compared to other RHBD ADCs, this is the only ADC that satisfies the analog performance requirements while being RHBD and containing on-chip features (e.g., calibration, references, and reference buffers) that make this ADC most easily scalable.

TABLE 4. Comparable works, rad hard ADCs.

	This work	JSSC19 (Xu) [10] ^c	NIMA17 (Kuppambatti) [11] ^d	AD9042S [71]
Process [nm]	65	65	130	BiCMOS
Architecture	Pipelined MDAC+SAR	Split Pipelined SAR	Pipelined MDAC+SAR	Pipeline
Resolution [bits]	15.0	14.0	12.0	12.0
Samp. rate [MS/s]	40	40	40	41
Analog BW [MHz]	Nyquist	Nyquist	Nyquist	100
V _{DD} [V]	1.2	1.2, 1.8	1.2, 2.5	5.0
V _{FS} [V _{diff}]	2.0	2.4	2.4	2.4
Agg. Power [mW/Ch.] ^a	137.10	22.20	50.00	735.00
# of ch.	8	1	2	1
SNDR [dB] @ DC	74.8	78.0	67.9	68.0
SNDR [dB] @ BW	70.3	74.4		
FoM _S [dB] ^b	151.9	163.9	153.9	149.3
Calibration	FG on-chip	BG off-chip	FG on-chip	Not discussed
On-chip References	Yes	No	Yes	Yes
On-chip Ref. Buffer	Yes	Yes	Yes	Not discussed

^a Aggregate power per channel. Entire chip power with all channels enabled, divided by number of channels.

^b [74]; FoM_S [dB] = SNDR [dB] @ BW + 10 × log₁₀ $\frac{BW [Hz]}{P_{Agg. W/ch.}}$

^c 40 MS/s data reported for comparison.

^d Reported with 10 MHz input frequency.

IX. CONCLUSION

A radiation-hardened by design, 8-channel, 40-MSPS, 15-bit resolution, 14.2-bit dynamic range, 11.4-ENOB ADC has been designed and validated for use in the ATLAS LAr calorimeter readout in the HL-LHC or other environments with ionizing radiation. The ADC was designed in a commercial, triple-well 65-nm CMOS process, with radiation hardening design techniques at the circuit and system level. Eighteen devices were characterized for analog performance; further validation of long-term analog accuracy and an extensive radiation testing campaign was undertaken. All results indicate that the design is suitable to be deployed to the scale of 45 617 chips for use in the ATLAS Detector. Work is ongoing to mass produce the ADC, continue lot quality-assurance validation, and package the chip dies in a more efficient BGA package.

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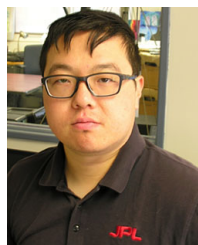
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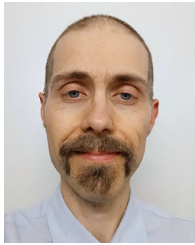


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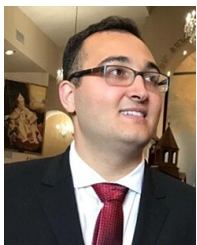
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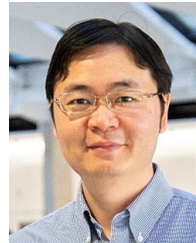
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