NASA-STD-8739.11 Tutorial
O1: Optoelectronics

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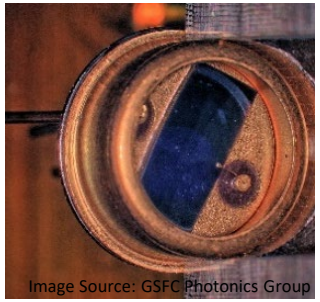
August 11, 2025

Acronyms

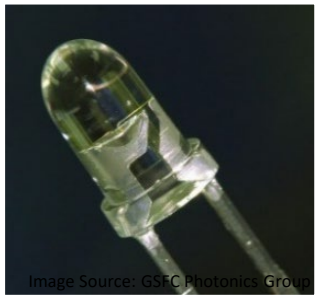
COTS	Commercial-Off-The-Shelf
EEEE	Electrical, Electronic, Electromechanical, Electro-Optical
ETW	Electronics Technology Workshop
GSFC	Goddard Space Flight Center
LED	Light Emitting Diode
MIL-SPEC	Military Specification
NASA	National Aeronautics and Space Administration
NEPP	NASA Electronic Parts & Packaging (Program)
SCD	Source Control Drawing
SME	Subject Matter Expert

Covered Part Type Description

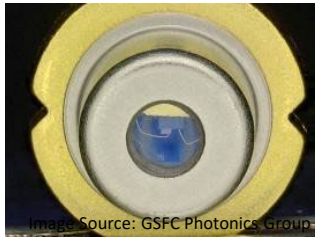
- This is a new category for 8739.11, which was not previously addressed in EEE-INST-002.
- This section covers hermetic and non-hermetic optoelectronic devices and establishes verification requirements to ensure parts meet applicable performance and reliability requirements for use in NASA space missions.
- Optoelectronics are components which interface between electrical and optical energy.
  - It can be included in parallel to other major optical component categories: waveguides (classic optics, fiber optics, etc.), passive optical components (optical switches, isolators), modulators, and hybrid integrated devices (optocouplers).
- The Optoelectronics portion of 8739.11 covers two generic groups of components: Photodiode Construction and Light Emitting Diode (LED) Construction
  - Laser diodes are covered under section L1.
  - Fibers are covered in section F1, free space optics are not covered.
  - Modulators and hybrid optical devices can take guidance from the Hybrid Microcircuit sections.
  - Due to rapid technology development of Photonic Integrated Circuits (PICs), this document is not enough guidance to establish a comprehensive test plan.



Photodiode



LED



Laser Diode

Key Considerations

- Many of the key considerations for Optoelectronics are similar to those found in the Detector Section of this document.
  a) Optoelectronic devices present new challenges due to the wide variety of technologies used for these parts, each with its own set of concerns.
     - An additional area of concern for optoelectronics is the potential for intermetallic degradation in the processes used for construction.
  b) Reliability at cryogenic temperatures may not be driven by the same mechanisms as for normal temperature ranges. These effects should be characterized for potential degradation mechanisms at the intended operating temperatures.
  c) Depending on optoelectronics device construction, parts storage at cryogenic temperatures may extend the life of some devices.
  d) Custom hybrid optoelectronic devices may be required for some missions. Such packaging could use novel attachment techniques and/or materials. These packages should be subjected to rigorous testing and/or analysis to determine acceptability for space application.

Major Changes from EEE-INST-002

- Section introduced in 8739.11
- Tables layout the standardized tests to be performed for screening and lot acceptance.
- Screening tables are broken out for each of the 2 construction types: Photodiode and LED.
  - The largest difference between their screening programs is the range of electrical and performance tests used for trending purposes. These tests are performed multiple times throughout screening and lot acceptance.

Table 2A. PHOTODIODE ELECTRICAL CHARACTERISTICS

Inspection/Tests As Defined in SCD 1/
Dark current (Leakage)
Forward resistance
Noise Spectral Density
Capacitance
Quantum Efficiency
Responsivity (As Applicable)
Other Key Performance Parameters (When required)

Table 2B. LIGHT EMITTING DIODE (LED) PERFORMANCE CHARACTERISTICS

Inspection/Tests As Defined in SCD 1/
Forward current
Pulse Forward Current
Forward Voltage
Reverse Voltage
Power Dissipation
LIV
Wavelength/Spectrum
K Factor

Major Changes from EEE-INST-002

- The newly creating testing tables in O1 of 8739.11 provide a general guideline for screening and lot acceptance of Optoelectronic components.
  - Due the wide variety of part types and applications, testing needs to be tailored to account for device characteristics and use conditions.
  - As a reminder, optoelectronics tend to not have hard failures in test outside of packaging (PIND, Hermeticity), therefore trending of device performance is necessary to uncover degradations curves and determine pass/fail criteria.

Major Changes from EEE-INST-002

- Lot Acceptance Testing (LAT) is broken out for hybrid and discrete optoelectronics components.
- LAT follows the same protocol for both types of devices:
  - Solderability
  - Survival Temperature Cycling
  - Steady State Life Test
  - Random Vibration

Major Changes from EEE-INST-002

- Derating requirements for Optoelectronics are shown. Prior to 8739.11, derating was derived from testing or from a general-purpose Diode derating in EEE-INST-002

Table 4. OPTOELECTRONICS DERATING REQUIREMENTS

Type	Stress Parameter	Derating Factor
All	Power	0.60
	Current	0.75
	Voltage **1/ 2/**	0.75
	Junction Temperature **3/**	0.80

Send email to address below for questions

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Backup