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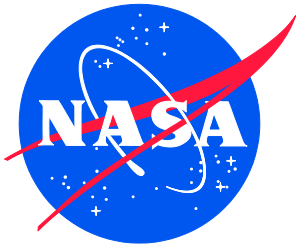

Cold Electronics for Lunar Missions

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August 2025

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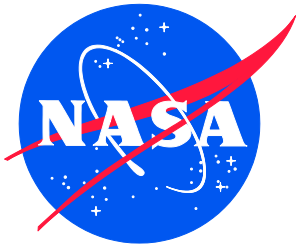

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August 2025

Acknowledgments

The NESC team would like to thank our consultants listed above and numerous people we have talked to from NASA, industry, academia, and other government labs and agencies during this assessment. The team would like to extend our thanks to Steve Rickman, Will Grier, William Birmingham, and Lisa Erickson at NASA as well as Milena Graziano, Sean Young, and Jacob Gehrett at the Applied Physics Laboratory for many discussions on thermal analysis and modeling and lunar environments. The team also would like to thank the following peer reviewers: Jeffery Farmer, Jim O'Donnell, Jeremiah McNatt, Steve Rickman, Wesley Powell, Joel Sills, Nicholas Uguccini, Peter Majewicz, Tim Barth, William Bluethmann, and Carolyn Mercer.

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NASA Engineering and Safety Center
Technical Assessment Report

Cold Electronics for Lunar Missions

TI-23-01873

NESC Lead, George Jackson
Technical Co-Lead, Yuan Chen
Technical Co-Lead, Raphael Some

July 17, 2025

Report Approval and Revision History

NOTE: This document was approved at the July 29, 2025, NRB.

Approved: Timmy Wilson Digitally signed by Timmy Wilson Date: 2025.08.15 13:30:20 -04'00' _____

NESC Director

Version	Description of Revision	Office of Primary Responsibility	Effective Date
1.0	Initial Release	George Jackson, Avionics Technical Fellow, GSFC	7/17/25

Table of Contents

List of Figures

List of Tables

Technical Assessment Report

1.0 Notification and Authorization

Mr. Kevin Somervill, Deputy Program Director for Technology Maturation at NASA Space Technology Mission Directorate (STMD), requested an independent assessment on the state of the cold electronics technologies and the gaps for applications and challenges under lunar environments, and provide NESC recommendations for cold electronics selection, evaluation, qualification and screening for lunar missions and forward work.

Key dates in the assessment life cycle are listed below.

Request Submitted	May 4, 2023
Initial Evaluation Approved	June 29, 2023
Assessment Plan Approved	September 21, 2023
Team Kickoff Meeting	October 16, 2024
Final Report Delivery and Stakeholder Update	July 17, 2025

In addition to Mr. Somervill, the stakeholders for this assessment include:

Wesley Powell, NASA STMD Principal Technologist for Avionics; Carolyn Mercer, Chief Technologist of NASA Science Mission Directorate (SMD); Florence Tan, Deputy Chief Technologist of NASA SMD; Dr. Peter Majewicz NASA Electronic Parts Program (NEPP); Susana Douglas, NASA Agency Electrical, Electronic, and Electromechanical (EEE) Parts Manager; and Program or projects needed to survive and operate under lunar environments.

2.0 Signatures

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Signatories declare the findings, observations, and NESC recommendations compiled in the report are factually based from data extracted from program/project documents, contractor reports, and open literature, and/or generated from independently conducted tests, analyses, and inspections.

3.0 Team Members

Name	Discipline	Organization/Host Center
Core Team		
George Jackson	NESC Lead	NESC/GSFC
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Kristen Boomer	Electrical Power Systems	GRC
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Acknowledgements

The NESC team would like to thank our consultants listed above and numerous people we have talked to from NASA, industry, academia, and other government labs and agencies during this assessment. The team would like to extend our thanks to Steve Rickman, Will Grier, William Birmingham, and Lisa Erickson at NASA as well as Milena Graziano, Sean Young, and Jacob Gehrett at the Applied Physics Laboratory for many discussions on thermal analysis and modeling and lunar environments. The team also would like to thank the following peer reviewers: Jeffery Farmer, Jim O'Donnell, Jeremiah McNatt, Steve Rickman, Wesley Powell, Joel Sills, Nicholas Uguccini, Peter Majewicz, Tim Barth, William Bluethmann, and Carolyn Mercer.

4.0 Executive Summary

NASA's goal of developing crewed and robotic lunar installations has created a need for cold capable electronic parts, subsystems, and systems that can operate in the lunar thermal environment (typically -233 degrees Celsius (°C) or below to +125 °C ambient). This assessment was commissioned to evaluate the state of cold capable electronic and packaging technologies, perform a gap analysis against the continuous use of these electronics with minimal or no thermal management on the lunar surface, provide NASA Engineering and Safety Center (NESC) guidance on the qualification of cold electronics, and to give NESC recommendations for the development and utilization of cold capable electronics. The assessment did not focus on the lunar radiation environment.

Key recommendations for the development and utilization of cold capable electronics:

The current architectural approach for avionics required to operate in extremely cold and wide environments (e.g., Mars or Deep Space) is to place the electronics in a warm electronics box (WEB) and cable out to actuators and sensors that are custom designs built for these extreme environments **[F-4]**. The NESC team believes that it would be highly beneficial and, in some cases enabling, to lunar surface missions if specific electronics assemblies could be located outside the WEB. However, no cold capable electronics architectures that are generally applicable to the lunar surface environment have been implemented or even studied to the degree necessary to initiate the detailed design of such an architecture **[F-5]**. Therefore, the NESC team concluded that a practical first step to implementing a cold capable avionics architecture is to implement a hybrid system with a WEB and selective technologies and subsystems outside of the WEB. The NESC team recommends that Science Mission Directorate (SMD)/Space Technology Mission Directorate (STMD) implement an evolutionary strategy to develop a cold capable electronics ecosystem that supports hybrid and hibernation avionics architectures (R-3). Additionally, the team recommends that STMD/SMD develop cold electronic elements for representative mission environments and plan for mission infusion opportunities (R-4). A phased evolutionary approach with identified development of high value technologies and demonstration/infusion examples are described and outlined in Section 7.10.

Qualification guidance on cold electronics and packaging:

No existing standards support the qualification of the electronics and packaging for the lunar environment temperature range of -233 °C to +125 °C (40 to 398 Kelvin (K)). Actual worst-case temperatures, depending on specific mission location, platform configuration, electronics location and orientation within the platform, and mission operations, could be significantly lower and will need to be identified by the project. Guidance on qualification of the cold custom electronics, commercial off-the-shelf (COTS)/military (MIL) electronics, and packaging were developed and are summarized in Section 7.9 (R-2). A given project will need to apply the appropriate guidance based on their Mission, Environment, Application, and Lifetime (MEAL) and risk posture. There is an additional recommendation for NASA Electronic Parts Program (NEPP) to develop NASA qualification standards for cold electronics and packaging, perform cold electronics testing/characterization, develop packaging guidelines, and to host a cold electronics database (R-5).

The intended audience of this report are NASA personnel and commercial practitioners who develop parts, subsystems, and systems for lunar surface missions.

5.0 Assessment Plan

The NESC team performed the following tasks, which were in the initial request.

- Captured the state of the art in NASA, industry, academia, and other communities in cold capable electronics and their applications and challenges for lunar environments.
- Described the current or best practices in selecting and qualifying cold electronics and identified gaps in technology selection and evaluation processes for lunar missions.
- Provided NESC recommendations for cold electronics selection, evaluation, qualification, and screening for lunar missions, as well as forward work.

6.0 Problem Description and Background

NASA's goal of developing long term crewed and robotic lunar installations has created a need for electronics that can operate in the lunar thermal environment. Though some of the electronics in question will be housed within a thermally controlled environment (e.g., in a lunar habitat or a robotic platform WEB), it would be either enabling or advantageous to many systems if their electronics could withstand the lunar environment without extensive thermal mitigation. Previous work began developing and evaluating various electronics for the extreme temperatures found on the lunar, Europa/Icy Moons, and Mars surfaces. The NESC team was tasked to assess the state of the cold capable electronics and packaging technologies, perform a gap analysis of the continuous use of these electronics with minimal or no thermal management on the lunar surface, and provide recommendations and guidelines, to the extent possible, for utilization and development of cold capable electronics. The assessment was focused on the thermal aspects of the problem, and radiation tolerance needs to be verified and characterized for any combined effects on an as-needed basis for their target environments.

7.0 State of Cold Electronics Technologies and Gap Analysis

Section 7.1 provides the scope of this assessment and key definitions. Section 7.2 describes the lunar environments of interest, assumptions for temperature ranges, and several thermal cycles and/or shocks expected for different types of lunar missions in these environments. Section 7.3 reviews various avionics architectures and delineates some of the advantages of distributed and hybrid architectures that are enabled by cold capable electronics, which in turn lead to a prioritization of cold capable electronic parts, assembly and subsystem developments. Sections 7.4 through 7.8 describe the states of the art or practice, qualification and evaluation approaches, and gap analyses in the areas of COTS electronics, custom electronics, passives, packaging and materials, and power systems respectively. Section 7.9 provides a description of evaluation and qualification methodology and NESC guidance on cold electronics qualification.

7.1 Scope of Assessment and Key Definitions

The goal of this assessment was to evaluate the potential continuous use of these electronic parts and assemblies with minimal or no thermal management on missions of up to 20 years in all regions of the lunar surface (e.g., permanently shadowed regions (PSRs) and equatorial). The assessment attempts to define an 80% solution and one that is workable for general electronics parts and assemblies. The defined scope of the assessment was to capture the state of cold electronics in NASA, industry, and academia; their applications and challenges for lunar environments; identify gaps; provide NESC guidance for cold electronics selection, evaluation,

qualification, and screening for lunar missions; and provide NESC recommendations for technology advances and follow-on actions to close the gaps.

The following are key definitions in this report.

Electronics:

- **Cold Electronics and Cold Capable Electronics** are used interchangeably in this report and refer to both cold operable electronics and cold tolerant electronics, which are defined below. In this assessment, the temperature range is extended to include cryogenic temperatures and wide temperature range for lunar environment.
  - Cold Operable Electronics - Electronic technologies, parts, assemblies, subsystems, and their packaging that are capable of operating stably in environment having a lower limit below the military specified minimum temperature of -55 ℃ (218 K) and can be successfully "cold-start". The military specifications are -55 to +125 ℃ (218 to 398 K) per MIL-PRF-38535, paragraph A.3.1.3.20.,

Table 7.1-1 Typical Specified Temperature Range

Standards	Temperature Range
Military standards and specifications www.dsp.dla.mil/Specs-Standards	-55 to +125 °C
Automotive Electronics Council (AEC) standards www.aecouncil.com	between -40 to +85 °C and -40 to +150 °C
Joint Electron Device Engineering Council (JEDEC) standards www.jedec.org	-40 to +85 °C

  - Cold Tolerant Electronics - Electronics technologies, parts, assemblies, subsystems, and their packaging with ability to tolerate repeated cycles into cryo-temperatures without significant degradation. It is primarily an issue of packaging materials compatibility at the part and circuit assembly level. "Cold tolerance" is distinctly separate from "cold operable," in that "cold tolerance" does not deal with operation of the electronics in and across the temperature range, but rather their ability to survive if thermal cycled or shocked while in a quiescent or unbiased state. Thermal Cycle Resistant Electronics and Cold Survivable Electronics are two other terms used in other literature.
  - Cold Start - In the context of electronics intended cryo-temperature operations, the term "cold start" is the condition where an electronic part or subsystem is unpowered and is at thermal equilibrium with the cold environment. This is considered the worst-case condition for starting the circuit at cryo-temperatures.
  - Cryogenic Temperature or Cryo-temperature - When common atmospheric gases are condensed into a liquid state at a temperature that is below the normal gas-liquid transition point (a.k.a. boiling point). Cryogenic Society of America defines the *Cryogenic Temperature* range from -150 °C (123 K) to absolute zero (-273 °C (0 K)). Note that the term cryo-electronics has been used in the study of superconductivity and quantum computing. Neither superconductivity nor quantum computing applies to this assessment
- **COTS/MIL -** Any commercial, automotive, space, or military off-the-shelf parts which are not designed specifically for cold operation below -55 °C (218 K).

Architectures:

- **Centralized Architecture -** The physical location of most of the avionics. A centralized architecture for a cold environment (e.g., the lunar surface) would use a single, centrally located WEB that provides a benign temperature range for the electronics. An occasional part (e.g., a focal plane readout or a position sensor) might be located external to the WEB and may or may not have heaters and/or other thermal control elements associated with it, but mostly the avionics are housed in the WEB.
- **Distributed Architecture -** The physical location of most avionics subsystems. The subsystems are distributed around the vehicle or platform to be optimally located for mechanical, operational, and electrical purposes and not in a centralized WEB. The electronics are assumed to have minimal to no thermal management support and are therefore required to be robust and reliable in the extreme thermal environment of the lunar surface.
- **Hybrid Architecture -** A physical distribution of the avionics such that while most of the avionics is housed in a WEB, there are significant elements of subsystems that are located outside the WEB and subject to the lunar surface environment. Examples include the low-noise amplifier (LNA) and Power Amplifier of a radio frequency (RF) system, both of which might be mounted at the antenna, while the rest of the RF system is housed in the WEB.
- **Lunar Power Hibernation Architecture -** This is an architecture specifically intended to address the need of solar powered spacecraft to survive the 354 hour long and extremely cold lunar night (including a nearly 5 month long lunar polar winter). *This concept has no WEB* and virtually all elements of the spacecraft are exposed to the lunar night environment. When solar array output ends at lunar dusk and the battery charge is too low or temperatures are too cold for battery cells to operate, the system shuts down and hibernates until the solar arrays are illuminated at lunar dawn.

Level of integration:

- **Assembly -** A board/substrate populated with multiple packaged parts and passives.
- **Parts -** A part refers to a single packaged electronic device. Parts can be active or passive in its electrical behavior and may contain multiple dies or devices if they are contained in a single package.

7.2 Target Thermal Environments

In this section, target thermal environments are defined for this assessment. The environments are specified as:

- Thermal environment in the various regions of the lunar surface (e.g., lunar equatorial region, mid-latitude regions, polar regions, PSRs).
- Range, number, and rate (fast/slow) of thermal cycles experienced in various types of missions (e.g., exploration rover, habitat, in situ resource utilization (ISRU) mining and processing).
- Thermal environment experienced by the electronics *without* an active thermal management system on various types of platforms (e.g., rover, habitat, excavator).

- Thermal Hibernation, a special case in which the electronics are allowed to soak, in a quiescent or unbiased state, to reach equilibrium with the worst-case cold environmental temperature of the region in question and can then successfully and correctly initialize upon application of power.
- It should be noted that, for the purposes of this assessment, the temperatures and thermal cycles specified below are not the worst-case extreme temperature ranges that might be experienced by surface platform electronics, but rather an "80% worst case" that can be used for general purpose electronics selection and preliminary evaluation and qualification planning during the early development phase when mission specific data are not available. Actual worst cases for specific equipment, depending on a host of factors, could be significantly worse or better.

Much of the following discussion was developed by the Applied Physics Laboratory (APL) Lunar Surface Innovative Initiative (LSII) in a study report "Assessment on Cold Electronics for Lunar Missions" commissioned by this assessment. The full report is attached as Appendix A and summarized below. In Appendix B, additional information was provided by the NASA Lunar and Mars Environments Analysis Team (LUMENATE), which can be contacted for additional information regarding thermal design considerations, modeling techniques, and environmental; factors for assets emplaced on the lunar surface.

The orbital period of the Moon around the Earth is approximately 27.3 days, but as the Moon and the Earth are changing their positions with respect to the Sun, it takes approximately 29.5 days to observe a full lunar cycle. This results in a lunar equatorial region that is illuminated for approximately 354 hours, followed by an approximate 354 hours of continuous darkness. Moreover, the Moon has a spin axis that is inclined by 1.5 degrees from the normal to the plane of the Moon's path around the Sun. This geometry allows for extreme surface thermal hot cases at the equator (almost 127 °C/400 K) and complex illumination conditions at the poles which vary by seasons, location, and local topography. Additional determinants of the lunar surface thermal environment include:

- Due to lack of atmosphere, lunar surface temperature is primarily determined by the effective solar irradiance which is closely tied to latitude dependent solar incidence angle and local terrain slope, as well as thermal radiation exchange with the lunar regolith which is region dependent. Mare regions are relatively flat and the regolith there has higher solar absorptivity resulting in hotter surface temperatures. Highland regions typically contain steeper terrain (e.g., mountains and craters) and the regolith has higher solar reflectivity resulting in cooler surface temperatures.
- Minimum temperatures occur prior to local sunrise and are dependent on the adjacent terrain (e.g., solar occlusion, view factor to surface), thermophysical and thermo-optical properties of the lunar regolith, and the specific platform upon which an asset is mounted (influences adjacent regolith radiation exchange and view factors to space
- In the equatorial region, differences between the near side and far side temperatures are not significant and show the same variation between maximum and minimum extremes.
- The coldest locations on the lunar surface are found at the bases of large impact craters at the poles where incident solar illumination is perpetually absent. These locations are known as

PSRs. Temperatures inside PSRs can vary, but conventional practice is to assume a worst-case for this region.

- During daytime hours, local shadowing can occur due to terrain and platform geometries. This is particularly true for polar regions, where the sun never rises very high in the sky and topographical features can induce lengthy shadows that can last for hundreds of hours.
- The thermal inertia (defined as the resistance to temperature changes when subjected to heat sources) of the lunar regolith is so low that even brief shadows can result in near nighttime temperatures adjacent to otherwise illuminated terrain. The inverse is also true in that shadowed regolith can rapidly increase in temperature when illuminated for brief periods.
- Elements with significant stand-off distances such as vertical solar array technologies (VSATs), human-rated landers, and communication towers will be required to withstand extreme variations across their structures [ref. 1] (and potentially electronics) due to varying illumination durations which are dependent on separation height from the Lunar surface. This is especially true in Lunar polar regions where the Sun maintains proximity to the horizon; large gradients will be experienced both across the height and width of tall structures.

7.2.1 Thermal Environment Experienced by the Electronics

Several sources, including NASA Human Landing System Lunar Thermal Analysis Guidebook [ref. 2], provide extensive information regarding thermal modeling techniques for the Lunar environment which can readily be applied for electronics development applications. Measurement of lunar surface as well as platform temperatures have been taken by various missions including in extreme regions such as far side of the Moon and the floor of the Von Karman Crater. Appendix A contains specific temperature measurements made on several platforms in these extreme regions. These measurements were obtained via the Lunar Reconnaissance Orbiter (LRO) Diviner Lunar Radiometer Experiment which has a spatial data resolution is 240 meters per pixel and temperature value error of ±5 ºC [ref. 3]. For polar regions where terrain topology is extremely complex and the solar elevation angle stays near the horizon, the relatively low spatial data resolution of the Diviner instrument can reduce its utility for estimating surface temperatures at a specific mission location.

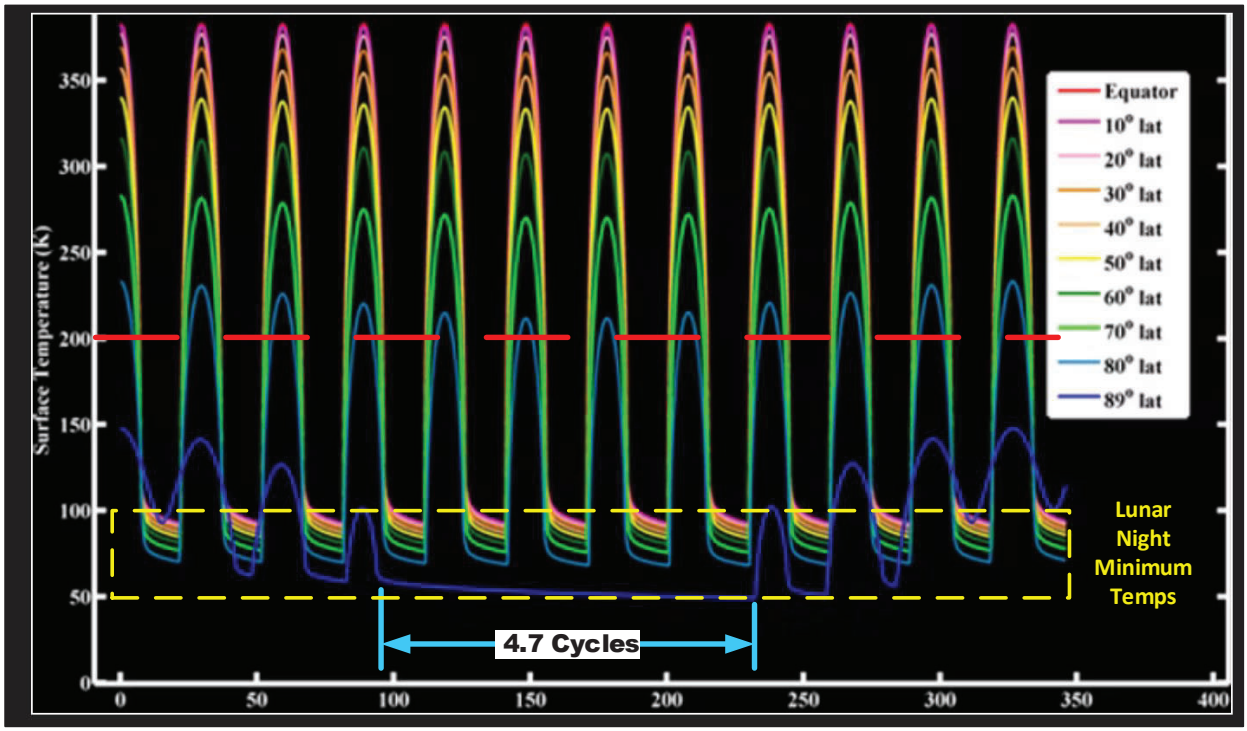

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Figure 7.2-1. Lunar Reconnaissance Orbiter DIVINER Surface Temperature Data Thermal model calculations of monthly and annual lunar surface temperature variations at various lunar altitudes.

The LRO data, shown in the Figure 7.2-1, shows lunar surface daylight temperatures have a very cold and wide range (-173 °C (100 K) to ~127 °C (~400 K)) over polar to equatorial latitudes. Lunar nighttime temperatures have a much narrower range. Non-polar surface assets will be exposed to an approximately the 354-hour lunar night with minimum temperatures that fall between -204 °C (69 K) to 178 °C (95 K) depending on latitude. The red dashed line indicates where lithium-ion (Li-ion) battery cells freeze ~-73 °C (200 K). The yellow dashed line bounds the range of lunar night temperatures for all latitudes. Note that both the coldest minimum (~-223 °C (50 K)) and warmest minimum (~-173 °C (100 K)) temperatures appear at the polar latitudes (see dark blue 89° latitude line). This is due to the moon's ~1.5-degree inclination to the sun that creates a seasonal effect on surface temperatures at the poles. Polar missions can exploit the long daylight and short night cycles of the lunar polar summer by locating assets at points that experience near continuous solar illumination due to their high vantage point relative to adjacent terrain. However, polar missions can be confronted with, depending on the mission location, surviving a lunar polar winter where a lunar night may span 4.7 lunar cycles with temperatures sinking to below -223 °C (50 K).

There is insufficient measured lunar surface thermal data spatial resolution and no universal generic thermal model that can be used by early mission system and avionics developers to determine the thermal environmental extremes over lunar surface regions for platform or electronics outside of the WEB. At present, the avionics community generally uses the lunar regolith surface temperature in the regions of interest and assumes these are the worst-case temperatures seen by the electronics ***[F-1]****.*

In Appendix B, the NASA LUMENATE uses a simplified thermal model to provide some insight into the potential differences between regolith surface temperatures and the effective thermal environment exposed to electronics outside of a WEB. One of the examples is shown in Figure 7.2-2 for a specific lunar south pole location, where regolith surface temperature range is -228 to -143 °C (45 to 130 K) and the electronics temperature is -238 to 52 °C (35 to 325 K) for typical electronics optical properties. Appendix B contains additional information and analyses, including modeling details and assumptions. As shown in Appendix B, the regolith surface temperatures only serve as a starting point when mission details required for accurate thermal environment determination are unavailable. *Accurately identifying worst-case and actual thermal environments requires knowledge of the specific mission location, mission date range, platform configuration, electronics location and orientation within the platform, and mission operations **[F-2]***.

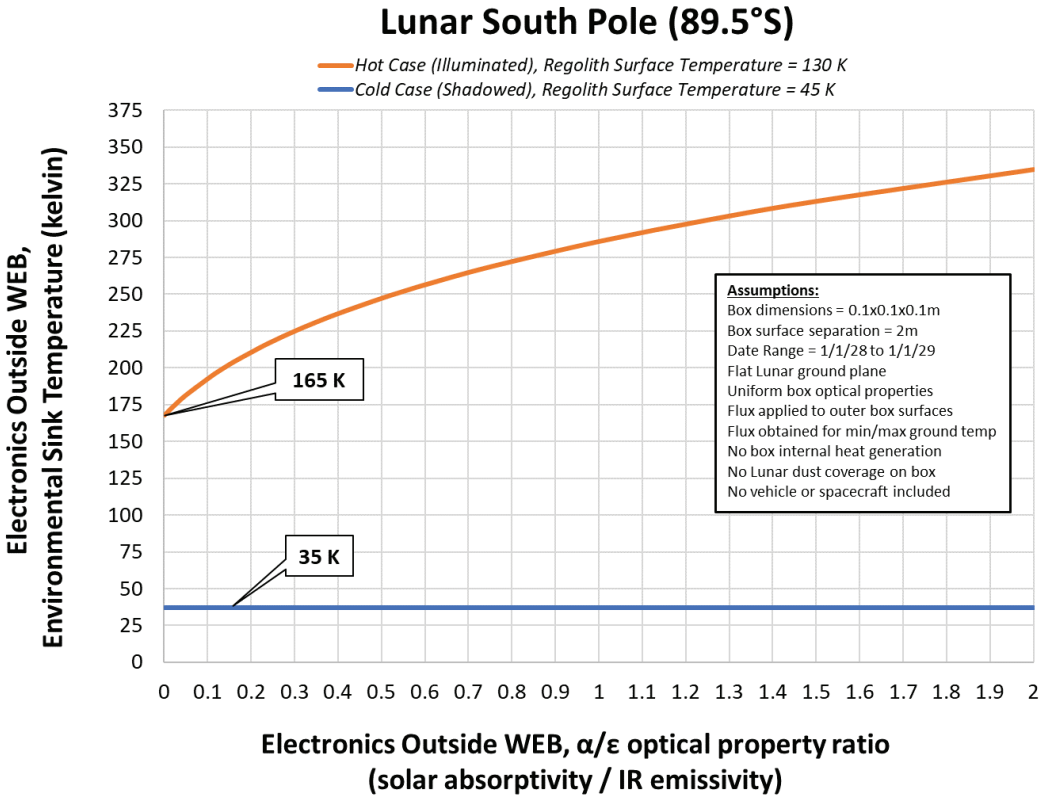

Figure 7.2-2. An Example of Thermal Environment for a Specific Platform Configuration and Specific Lunar South Pole Location

So, while the use of regolith temperatures is clearly an oversimplification, it is a useful first-step approximation of the worst-case for the cold end of the thermal range, although it is likely that some electronics may be exposed to even colder effective environmental temperatures. The electronics in a WEB are normally subjected to a more benign thermal environment. One significant exception being when cold soaked due to hibernation or initial startup after landing/deployment, when it is reasonable to assume that the avionics will have reached equilibrium with effective environmental temperature prior to operation. Colder temperatures may be seen, relative to the surface temperature, for example, if the part is placed above the regolith and oriented to have a view of deep space. It also noteworthy that regolith surface

temperatures as cold as -248 °C (25 K) have been measured in PSR. This assessment covered most electronics applications and accepted that in some cases more extreme thermal conditions may be experienced by specific electronic elements, which will have to be treated differently, either by providing some minimal thermal management or by qualifying to a project-determined temperature range.

The warm end of the thermal range is often assumed to be the worst-case regolith temperature. This is an oversimplification due to factors including electronics internal heat generation, incident solar flux, and reflected and emitted thermal radiation from the lunar surface. Those factors are likely to warm the electronics beyond regolith surface temperatures if no thermal management is provided. Temperatures could be biased higher because of lunar dust deposition and the resulting change in surface thermo-optical properties.

It is not uncommon that avionic developers need to start the process of reviewing, evaluating and selecting electronics technologies for an application when MEAL specifications are not available. For the purposes of this assessment, the NESC team recommends using the following generally accepted regolith surface temperatures *as the starting point* for cold electronics on lunar surface missions when no MEAL specifications [ref. 4] are not available, and engage thermal subject matter experts (e.g., NASA LUMENATE) as early as possible in the process to help define the expected temperature extremes to be experienced by the electronics outside of a WEB.

Based on empirical data, as well as scientific analyses to date, generally accepted regolith surface temperatures in different lunar areas are [Appendix A]:

- Permanently Stationed Platforms:
  - Equatorial -180 to +125 °C (93 to 398 K)
  - Mid Latitudes -145 to +80 °C (128 to 353 K)
  - Poles -223 to -193 °C (50 to 80 K)
  - PSR -233 °C (40 K) (Not absolute worst cases, but an educated assumption for the 80% case)
- Mobile Platforms:
  - Transport in/out of PSR -233 to -40 °C (40 to 233 K)
  - Roving broadly, -145 to +120 °C (128 to 393 K)

7.2.2 Thermal Cycles

For stationary platforms, one can assume slow thermal cycles with extremely low ramp rates and long dwell times that can be worst case by standard Military Standard (MIL STD 883) and NASA standards for electronics thermal cycling (e.g., ~ 5-25 °C/min). For mobile platforms, however, when crossing through shadow, it is possible that due to a lack of atmosphere the electronics may experience a fast thermal cycle (i.e., a thermal shock) which is a rapid transition between the warm and cold temperatures (e.g., > 100 °C/min). Without additional measurement or analysis, the NESC team cannot confidently specify a ramp rate for these thermal shock events but the Military and NASA standards for thermal shock can be used for a reasonable approximation of expected worst case conditions experienced by the electronics.

Regarding the number of thermal cycles that different missions might experience, the NESC team found several canonical reference missions that may be used to bound parameters of mission duration and number of thermal cycles/shocks experienced [Appendix A, refs. 5, 6, 7].

- For stationary platforms such as habitats or power generation stations, the NESC team expects a 20-year mission duration, and thus the number of slow cycles is approximately 12 lunar day-night cycles/year x 20 years. Note that the complex shadow environment on the south pole may result in more than 12 cycles per year.
- For mobile platforms there is a similar slow thermal cycle regime, but because the platform might wander in and out of shadow during its lifetime, a number of fast thermal cycles (or thermal shocks) need to be added. In this case, the fast thermal cycle is once into shadow and once out of shadow where the transition from low to high or high to low temperature is extremely fast and the time spent in shadow or light is sufficient to allow the electronics to reach thermal equilibrium. Assuming that these fast thermal cycles only occur during the daylight period of the lunar day, and that such a shadowed area might be encountered (and arbitrarily chosen) 14 times during that period, then it is approximately 14 fast cycles/lunar day x 12 lunar days/year x 20 years.
- For ISRU mining operations, the NESC team assumed a 10-year mission duration, and excursions between the PSR region and the adjacent polar region with a 10-hour cycle (i.e., in and out of the PSR every 10-12 hours, approximately 2x28 fast thermal cycles/lunar day x 12 lunar days/year x 10 years [Appendix A, refs. 5, 6, 7]).

7.3 Avionic Architectures for Cold Environment

7.3.1 State of the Art

In reviewing various architectures for lunar surface platforms, this assessment draws on experience from Mars projects as well as various technology developments and studies (e.g., Europa Lander, Cold Rover, Mars Rovers (Mars Exploration Rover (MER) and Mars Science Laboratory (MSL)), Distributed Motor Controller for Mars Rovers, MUSES-CN Rover, Commercial Lunar Payload Services (CLPS) Cold Arm). Additionally, this assessment commissioned a study by the Applied Physics Laboratory (APL) Lunar Surface Innovation Initiative (LSII) team (Appendix A), which summarized much of the data from these references and categorized electronic elements with respect to utility for future lunar surface missions.

With the exceptions noted herein, little avionics system architecture work has been done in implementing extreme cold electronics meeting the thermal environments specified in section 7.2. The exceptions are applications of individual parts such as an operational amplifier for Jet Propulsion Lab's (JPL's) Mars Rover Motor Control subsystem, which is required to be resident at the motor, various infrared focal plane read out parts (which are similarly required to reside in the cryogenic environment of the focal plane), and various Mars Rover cameras. These are mostly custom, one-off parts that do not address the broader issue of cold capable electronics or avionics architectures.

Studies of cold rovers for Mars [ref. 8] and similar applications have been performed. For the most part, these have not been implemented and while the studies to date show feasibility, they do not necessarily define an evolutionary path toward a fully cold capable architecture. Further, these studies have generally been for a Mars environment and for landers and rovers. While these provide useful information for a Lunar Cold Capable Avionics Architecture, they fall far short of the requirements for a lunar surface mission set.

A notable exception is the Lunar Power Hibernation & Recovery Architecture introduced in a GRC study in 2022 [ref. 9].

STMD ranked "survive and operate through the lunar night" as the number one "shortfall" in capability [ref. 10]. The lunar power hibernation is a near-term approach that employees cold electronics to meet the shortfall ***[F-3]****.* It is an architectural approach that integrates cold electronics and Li-ion cells capable of surviving multiple freeze/thaw cycle into a power architecture that can hibernate and survive the lunar night and successfully recover at lunar dawn. It was developed specifically for the low-cost robotic missions of the CLPS program but is applicable to a broad range of lunar missions and provides an evolutionary step requiring only specific parts of the power system to be cold operable while allowing the remainder of the system to be cold survivable.

Hibernation is a strategy that addresses the problem of a lack of power generation at night and insufficient energy storage to maintain operating temperatures for standard electronics in the extreme cold environment (-173 °C to -223 °C (100 K to 50 K)) of the lunar night [ref. 11]. In this architectural approach, the bulk of the electronics are not required to operate in extreme cold but are only required to survive the cold without degradation (i.e., most of the avionics including the flight computer and the battery cells). The cold operational electronics are limited to a portion of the power management and distribution subsystem as required to perform a reliable cold-start and to operate at lunar dawn temperatures.

To minimize the changes to existing spacecraft, cold-operable electronics are limited to portions of the power system essential for hibernation recovery (i.e., solar arrays, main bus control, and battery management). These elements represent the core of the cold-operable electronics needed for dawn recovery. This approach minimizes the electronics redesign and requalification effort, thus enabling an evolutionary approach to cold operational avionics systems. Li-ion batteries are cold survivable but are limited in operation since they lose the ability to charge or discharge at a temperature well above the lunar night temperatures. The success of the power hibernation approach depends on the use of cold electronics for reliable recovery of the battery.

The diagram in Figure 7.3-1 illustrates the lunar power architecture and some of the cold electronics functions needed to recover from a lunar hibernation. The diagram shows systems operable at cryo-temperatures in yellow, most notably the main bus controller (MBC). These systems must be cold-capable and able to achieve a cold start at lunar dawn. The remaining electronics are required to be tolerant of cryo-temperatures, but not expected to operate until nominal temperatures are regained.

When the arrays are initially illuminated at lunar dawn, the hardware will be at its coldest point in the cycle. At very low temperatures, solar arrays will generate substantially higher open circuit voltages than at normal temperatures [ref. 8]. To protect the arrays and power bus from overvoltage damage, it is necessary to manage the array output shortly after the array is illuminated. A simple overvoltage shunt circuit capable of a cold-start and operating at lunar dawn temperatures provides overall protection. Normally a spacecraft starts upon connecting the battery power to the main bus at which point the power system executes a power-up sequence. However, in the case of hibernation recovery at lunar dawn, the battery will be frozen and isolated from the main bus after experiencing a lunar night. Further, avionics and other loads are intentionally inhibited and remain in a passive unpowered state until the main bus is fully stabilized. The MBC, capable of a cold start at extreme cold temperatures and operating on the solar array output alone, is required to start the power-up sequence and is the essential element to the recovery process. As the sun rises the photovoltaic (PV) array power output continues to increase. The MBC must begin to regulate arrays while the avionics is still unpowered, and the

battery is hibernating. The MBC begins to methodically distribute power to heaters as the array output climbs. The MBC slowly raises the temperature of the batteries and the other hibernating systems to their respective operational temperature range. Without a battery to stabilize the power bus, it is important that the loads are activated in a stable manner. To avoid instability, large reactive loads, such as motors, are inhibited until the battery is warm and ready to be connected to the main bus.

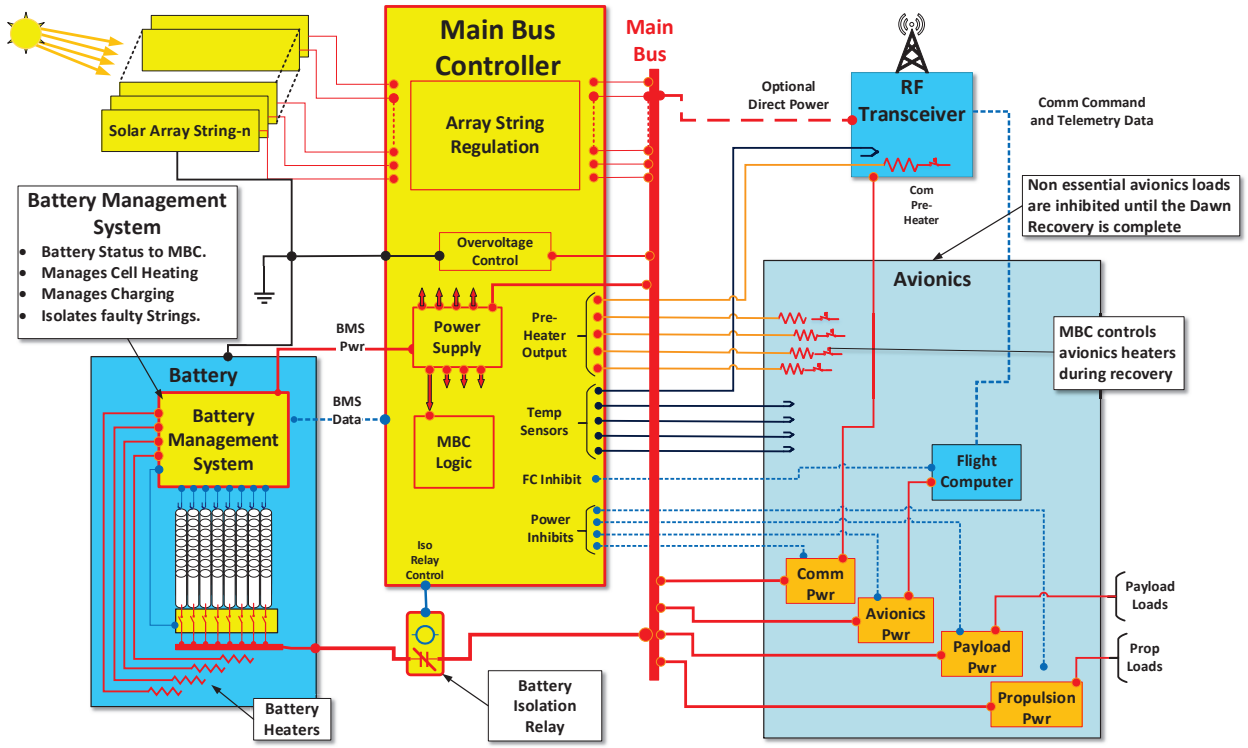

Figure 7.3-1. Lunar Power Hibernation Architecture employing Cold Electronics without a WEB

To manage the battery recovery, a Battery Management System (BMS) is required to monitor the recovering battery through the cell thaw process, and thus must be operational before the battery is thawed. The battery cells will not warm uniformly without some form of active temperature control. Cells at significantly different temperatures will have differing states of charge and cell voltages. Warm cells will tend to charge colder cells. Charging of very cold cells degrades the electrodes and damages the cells. Therefore, the BMS will manage the thermal recovery to assure the battery cell temperatures are uniform. As cells thaw and recover their normal state of charge (SOC), the BMS may need to check the individual cell state and, if necessary, perform cell balancing. As the battery temperature is returned to its normal operating state, the BMS reports the battery voltage and SOC to the MBC.

If the MBC detects a significant mismatch in main bus and battery voltage after thawing the battery, then the BMS may need to perform a battery “pre-charge” cycle to match the main bus to assure that the battery does not disrupt the main bus when reconnected. When voltages match, the MBC commands the isolation relay to reconnect the battery to the bus thus stabilizing the power system.

Once avionics are warmed up to operating temperatures, the MBC then begins methodically activating the power distribution system to power up the avionics. The highest priorities are

mission dependent but are likely to be the radio transmitter, flight computer, and data network. With the flight computer active, the power management can be taken over by a software module in the flight computer. With the data system, flight computer and RF communications reestablished the spacecraft can resume interaction with mission control as necessary for the mission.

Motor control is the area where cold electronics have been studied the most and at least partially implemented. With the possible exception of the hibernation architecture above, this may be the most compelling application for cold capable electronics in Mars and Lunar missions, primarily for rovers and similar vehicles, which have many motors and actuators. The NESC team found three significant efforts in this area[1]:

1. The Motiv company's motor controller for the JPL STMD Cold Arm project utilizes mostly existing off-the-shelf parts. For this project, Motiv developed a cold capable power converter -part for this specific application. The Motiv Cold Arm motor controller was tested to -180 °C and provides a strong existence proof for cold capable electronics and the potential utility of both custom and COTS parts. It is not generally applicable to the broader lunar surface mission set as it was designed to provide capability for the defined CLPS mission.
2. The initial Mars Program Distributed Motor Controller Technology Development developed a fully functional prototype of a cold capable distributed motor controller with all electronics capable of being mounted adjacent to rover motors. While a prototype was developed and tested, it was never fielded due to the complexity and perceived unreliability of the subsystem due to the large number of parts and the complexity of the design. The motor controller was implemented with readily available discrete parts comprising thousands of parts in an extremely complex design and an even more complex fabrication process.
3. The Follow-On Mars Program Distributed Motor Controller Technology Development developed a single cold capable mixed signal application specific integrated circuit (ASIC) that replaced the majority of the of discrete parts in the original Mars Distributed Motor Controller and simplified both the design and the fabrication process. The ASIC was implemented in 0.5 micrometer (μm) Silicon Germanium (SiGe) technology and fundamentally changed the design of this motor control subsystem. Although the ASIC was tested between -125 °C and +85 °C (148 K and 358 K) and was demonstrated in a prototype system to be of significantly higher efficiency than commercially available motor controllers of the day, due to budget limitations, it was never implemented in a full prototype or qualified for use in the Mars environment. Neither the technology nor the subsystem was fully developed. This technology project, however, is the closest the NESC team found to a part/subsystem implementation that can provide an example of a hybrid architecture and a paradigm for an evolutionary approach to cold capable avionics architectures. It utilized a warm box to house the main power conversion and computing elements of the system and a cold capable mixed signal miniaturized module that housed the local power conditioning and control, actuator, and sensor electronics. The module, about the size of a thick credit card, utilized chip on board technology to mount the above-mentioned ASIC and associated discrete elements to optimally perform local sensing and control of actuators. The module also implemented a dual redundant serial bus to communicate with the WEB-housed computing system. This architecture allowed use of extant off-the-shelf computing and power generation parts and subsystem assemblies within the WEB while distributing the

[1] Based on discussions with JPL and industry engineers.

actuator-associated electronics. Thus, the amount of copper penetrating the WEB was minimized and the digitization of low-level sensor signals and modulation of motor power signals was placed as close as possible to the actuators. Not only was the amount of harnessing and connectorization minimized, but it also optimized the EMI/C environment, thus significantly improving subsystem performance as well as SWaP-C. The fundamental principles of architecture optimization, developed and demonstrated in the Follow-On Mars Program Distributed Motor Controller Technology Development paved the way for cold capable avionics architecture evolution and a roadmap for the development of cold capable electronics parts.

Finally, a notable exception to the above was the JPL MUSES-CN Nano-Rover, a very small, extremely low power rover developed for a one-month asteroid exploration and sample acquisition mission. The rover had no thermal management system and was designed to withstand a temperature range of -180 °C to +110 °C (93 K to 383 K). It was successfully tested in a thermal vacuum chamber to those temperatures. The rover utilized selected COTS parts and custom packaging. It did not use a battery, relying instead of ambient solar illumination for power. Although the MUSES-C mission was cancelled, and thus the rover not finally qualified or flown, this technology development project does validate that, at least for short duration missions without significant thermal cycling, it is possible to develop such a system by utilizing carefully selected COTS parts and clever packaging [refs. 12, 13].

It is also noteworthy that the Mars Helicopter, while not designed for hibernation or cold operation, did survive a Mars winter, during which it "froze" (i.e., the battery was not able to maintain survival temperature throughout the winter, causing the electronics to experience the Mars winter temperature and the battery to freeze). Upon receiving sufficient solar illumination and warming conditions, the helicopter was able to resume operation.

The current architectural approach for avionics required to operate in extremely cold environments, such as Mars or Deep Space, is to place the electronics in a WEB and cable out to actuators and sensors that are custom designs built for these extreme environments ***[F-4]****.* While it is desirable to eventually enable all the avionics to be cold capable, an intermediate or interim evolutionary step would be to prioritize the avionic subsystem elements that provide maximum benefit if allowed to operate outside the WEB.

The WEB itself is usually highly insulated to ensure that heat from internal heaters and electronics is retained. This results in a potential for overheating due to electronics self-heating. Further, the requirement to cable through the WEB walls to access external sensors and actuators incurs the penalty of a large gap in the WEB thermal barrier that must be accounted for. Additionally, for systems which are required to hibernate, internal heaters are typically needed in the WEB, and possibly in any external electronic parts, due to a general inability of electronic parts to correctly start up and initialize in the cold environment, even if they can operate well in the cold once active as well as reliability concerns (e.g., due to hot electron injection effects) in long term operation of these parts in the cold.

Aside from work in avionics, there are some efforts focused on developing electronics for other cryogenic applications. For example, the Advanced Energy Technology Platform (AETP) program funded by the government of New Zealand is supporting the development of cryogenic electronics, for use with hydrogen storage and superconducting motor applications for large scale transport [refs. 14, 15, 16, 17]. This includes evaluating commercially available Gallium-Nitride

(GaN) High Electron Mobility Transistors (HEMTs) at -196 °C (77 K), developing new nanocrystalline based inductors optimized for cryo-temperatures, as well as design of full switched mode power converters capable of operating under these conditions. Many of these parts and design approaches can be transferred to lunar applications.

7.3.2 Gap Analyses

The gap between what is required per Section 7.2 and the state of the art per Section 7.3.1 is essentially that no cold capable avionics architecture meeting requirements like those of lunar surface missions has yet been fully implemented. Studies and technology readiness level (TRL) 3[2] prototypes show the feasibility of such an architecture, but none has yet been fully built, qualified, or fielded.

Given the state of the art as described in 7.3.1 above, the gap analysis is relatively straightforward. *No cold capable electronics architectures that are generally applicable to the lunar surface environment have been implemented or even studied to the degree necessary to initiate the detailed design of such an architecture **[F-5]**.* Basic principles and optimization approaches leading to an evolutionary roadmap to cold capable architectures are evident and have been initially validated by studies and technology developments aimed at Mars-capable avionics subsystems and the hibernation power subsystem.

*From an architecture implementation perspective, given the lack of cold capable electronics technology maturation, it is impractical to immediately implement a fully cold capable avionics architecture for lunar surface systems **[F-6]**.* Rather, the NESC team recommends an evolutionary approach. Estimating relative difficulty of development (and therefore development costs) versus benefits to future projects, it was deemed prudent to prioritize the cold electronics technologies and products to be developed. In determining maximum benefit and return on investment, several primary considerations emerged:

- Minimizing any thermal paths through the walls of a WEB.
- Minimizing noise and electrical path length of small signals between instrument transducers and support electronics.
- Minimizing noise and electrical path length of large signal excursions (and thus potential EMI/C) between support electronics and actuators.
- Supporting the maximum number of platforms and missions with the minimum number/cost of electronics developments.
- Maximizing near-term return on investment (ROI) to prove the efficacy of this approach and encourage continued funding for these developments by NASA as well as other entities including industry and Department of Defense (DOD).
- Focusing on near-term needs (i.e., items that will enable or enhance missions expected to be developed/fielded in the next 5 to 10 years).
- Enabling key steppingstone hybrid architectures such as the hibernation architectures.

[2] https://esto.nasa.gov/trl/

7.4 COTS Cold Electronics

7.4.1 State of the Art or Current Practice

COTS parts offer advantages for use in cold environments (e.g., lunar missions) in some aspects of such projects. They are significantly lower in cost, easier to procure and offer a broad range of functionalities and capabilities. Furthermore, technology analysis and experimental data suggest that many COTS/MIL parts are capable of operation, and not just storage, at temperatures well beyond the manufacturer specified temperature limits.

In the last 20 years the potential for COTS/MIL operation in cold has been explored by NEPP for a wide range of parts including resistors, capacitors, discrete parts like diodes and transistors, and both analog and digital integrated circuits, as well as hybrid parts containing integrated circuits and discrete parts. Most of this work has been done at Glenn Research Center (GRC) with some at JPL, Goddard Space Flight Center (GSFC), and Langley Research Center (LaRC). This and other published test results for cold operation of COTS/MIL were reviewed in 2018 under a JPL internal research task [ref. 18] and organized in a table containing data for approximately 200 parts. The table is being updated and will be hosted by NASA Electronics Parts and Package Program. It will be made available to the community as part of this study. These data provide an initial knowledge base from previous exploration of COTS/MIL usage in cold environments.

More recently, quantum computing has driven the development, design, and evaluation of electronics for operating at temperatures in the single digit Kelvin temperature range [refs. 19, 20]. However, the focus has been on the characterization of technologies for use in ASICs such as LNAs. Therefore, that work has little impact on the general findings from 2018 for COTS/MIL parts. The specific ASIC papers, however, will be added to the table.

In recent years, significant advancement has occurred in enhancement-mode GaN-based HEMTs. GaN HEMTs have matured significantly in commercial use and are now widely utilized in smaller and more efficient power converter chargers for laptops and smartphones. This wide usage signals a broader community understanding of key failure mechanisms and concomitant improvement in process control capabilities, thus, this is a prime area for exploration of new COTS/MIL options for space. Several papers have been published by universities demonstrating success in operating GaN HEMT in cryo-temperatures [refs. 21, 22]. Also, at least one vendor has begun providing the community with MIL qualified, radiation tolerant, discrete GaN HEMT [ref. 23].

For most part types of interest to NASA missions, pathfinder data that describes how the baseline technology performs in cryogenic environments may already exist. In this case, the data may point to one or more COTS/MIL candidates that show promising performance and are worthy of further evaluation. Such data can be used to make an initial assessment of the parts technology's performance in cryo-temperature ranges and whether COTS/MIL parts, implemented in these technologies, may be able to satisfy the mission needs or if custom parts will be required.

When operating COTS/MIL parts in cryo-temperatures, some performance and reliability changes will result. This is especially true when the gap between the COTS/MIL design temperature and the target cryo-temperature is quite large.

Some part performance parameters may improve in the cold while others degrade. The change is part-specific and often lot-specific as COTS parts are not designed for cryogenic operation. Therefore, testing in the specific operational environment is required for optimal part selection.

Less complex parts such as passive and discrete parts may have physics-based or chemistry-based descriptions for performance shift in cold temperatures. For example, various types of COTS/MIL diodes (including high current, small signal, Zener, Schottky, and SiGe diodes), tested between -190 °C and 25 °C (83 K and 298 K), all show similar shift of the forward bias current-voltage curve as predicted by the diode current equation, but details of curve shape and the amount of shift are dependent on diode design and fabrication technology.

Similarly, COTS/MIL power metal oxide semiconductor field effect transistors (MOSFETs) all show decrease in on-state resistance as temperature drops due to reduction in phonon vibrations, but the curve is different for parts from different vendors.

There are some COTS/MIL resistor and capacitor types that have cryo-temperature performance very similar to room temperature [ref. 18], so they would be viable candidates for use if the passives are further tested for reliability under actual use conditions. Passives' behavior in cold and selection criteria will be discussed in more detail in Section 7.6.

Some parts technologies have significant limitations at low temperatures. Silicon-based bipolar junction transistors (BJTs), for example, suffer from a decrease in current gain (β) as temperature drops below -196 °C (77 K). These parts, therefore, should be avoided for low temperature application. For this reason, silicon-based complementary metal oxide semiconductor (CMOS) integrated circuits should be checked for the presence of BJTs. This may be a challenge for COTS. In contrast, in some COTS parts, SiGe heterojunction bipolar transistors (HBTs), which is an excellent option to use instead of BJTs, as their direct current (DC) gains increase as temperature drops, may have been used. This technology is therefore also a key option for custom electronics for cold and discussed more in Section 7.5 [ref. 18].

Integrated circuits, both analog and digital COTS/MIL, have been explored for their potential utility in cold environments.

Mixed signals seem to be limited by analog circuits. An option may be to separate digital and analog parts to be able to choose the best cold performing parts for each case, but at the cost of less available board real estate.

Microcontrollers and field programmable gate arrays (FPGAs) are important to run the system or spacecraft, and COTS/MIL testing reveals that many COTS/MIL FPGAs start to behave poorly at temperatures as high as -123 °C (150 K). There are some candidates such as the Artix7 FPGA, which seem to have good performance down to -269 °C (4 K) except for increased jitter[3].

Hybrid circuits, especially direct current to direct current (DC-DC) converters, and voltage regulators are an important part of power systems and discussed in more detail in Section 7.8. COTS/MIL parts from 9 different vendors were evaluated and some begin to show abnormal behavior at -40 °C (233 K) while others were able to perform normally until -178 °C (95 K)[4]. Detailed element analysis of the constituent parts is recommended before testing to rule out known problematic technologies such as silicon BJTs [ref. 18].

[3] Based on discussions with JPL and industry engineers.

[4] Based on discussions with JPL and industry engineers.

7.4.2 Gap Analyses

Although much of the data collected through these studies is promising, there are several limitations that should be addressed before these parts can be selected for flight use. Most of the data have been focused on demonstrating capabilities at the temperatures of interest. Little to no data exist addressing reliability at these temperatures. The traditional high temperature acceleration may not be appropriate or sufficient here. Further, most testing of parts for operation at cryo-temperatures has not considered self-heating, wherein part temperature is raised due to thermal dissipation of the power expended by part operation.

This reliability data deficiency is partially due to the increased amount of testing and characterization needed to extend COTS/MIL operation into cryo-temperatures by as much as 123 °C/K below their design limits. Such a large temperature extension requires significant characterization and testing. *When COTS/MIL parts are used outside of their datasheet specified thermal range, reliability and stability are not ensured and the lot-to-lot variation in operational parameters are expected to be significantly higher than in normal operation* ***[F-7]****.*

There is a lack of cold start data in the literature. Most of the capability studies are continuous operation studies where temperature is gradually lowered until abnormal behavior is observed. Cold start test data would be critical to eliminate self-heating effects ***[F-8]****.*

7.5 Custom Cold Electronics

7.5.1 State of the Art

For the Mars Science Laboratory (MSL) Rovers, NASA's Thermal Cycle Resistance Electronics (TCRE) Program developed a custom cold capable quad operational amplifier as an integrated circuit that is capable of operating between to -180 °C to 80 °C (93 K and 353 K). To meet the radiation requirements of Mars, the quad operational amplifier was designed in a radiation hardened process 0.35-μm silicon on insulator (SOI) CMOS [ref. 24]. In addition, the TCRE Program characterized performance of selected number of COTS parts at temperatures as low as -150 °C (123 K). This evaluation was performed to understand the COTS operating temperature margin as compared to what was advertised in their catalog. Through these characterizations, the TCRE program identified a set of COTS parts that were capable of operating at temperatures as low as -150 °C (123 K), suitable for Martian nights [ref. 25]. These parts, together with the cold capable quad operational amplifiers, were used to build the electronics for the "cold encoder" modules for the MSL Rovers. The TCRE program also developed the technology for packaging and assembly of the cold encoder electronics that made it possible for the electronics to operate on the Mars surface for long durations without any thermal protection [ref. 26]. This effort was necessary because the cold encoder modules needed to be positioned at the exterior of MSL actuators (without any thermal protection) for sensing and electrical encoding the position of their shafts.

The present state of practice for custom cold electronics is determined mainly by the following activities:

1. The recent development in cold and wide operating temperature range (i.e., -180 °C to 120 °C (93 K to 393 K)), radiation-hardened, custom electronics using SiGe bipolar CMOS (BiCMOS) technology (SiGe HBT + Si CMOS) for space exploration applications (which includes both naturally radiation tolerant and low temperature capable 90 nanometer (nm) SiGe HBTs) [ref. 27];

2. The development effort of CMOS-only (e.g., 180 nm or 90 nm) electronics for sense and control of cryogenic detectors (e.g., infra-red (IR) focal plane arrays (FPAs)), capable of operating over a narrow, low-temperature range of -180 °C to -150 °C (93 K to 123 K) [refs. 28, 29]; and
3. Use of Fully Depleted SOI CMOS for cryogenic applications [refs. 30, 31].

Under NASA COLDTech and LuSTR, several analog, digital and RF circuits were developed using the commercially available Global Foundries 90 nm SiGe process technology. A sparse library of RF, analog and digital circuits were developed and demonstrated to be radiation hard to 5MRad and capable of operating down to -180 °C (93 K) ***[F-9]****.* The goal is to establish a sustainable ecosystem enabling the design of complex cold and wide temperature SiGe cryogenic circuits for space applications. For this purpose, the results of the effort include a publicly available library of prototype SiGe circuits. While most of the building block circuits are implemented using SiGe HBTs or SiGe HBTS plus on-die CMOS, it also includes a small number of monolithically integrated 90-nm CMOS-only building blocks [ref. 32].

The previously mentioned 180-nm CMOS effort has been carried out by several industrial organizations (e.g., Teledyne) for sense drive and control of cryogenic FPAs [ref. 20]. These efforts have limited scope that cover only digital multiplexing and specific circuits for sensing and control of cryogenic detectors. The modeling, design methods, and elements of these CMOS circuit libraries are considered proprietary and not publicly available.

For cryogenic applications, the drift of the CMOS transistors as a function of temperature is a parameter that limits the design choices. The fully depleted silicon on insulator (FDSOI) CMOS offers access to the body of the individual transistors. This feature can be used to exploit “back bias” the body of the transistors to compensate for gate threshold voltage drift of the CMOS transistors as a function of temperature [refs. 30, 31].

Common to both cold electronics efforts (i.e., those utilizing SiGe BiCMOS and CMOS technologies) is the use of commercial manufacturing foundries. In both cases, the designs are realized through the following [refs. 32, 33, 34]:

- Extraction of empirical models for the performance of the transistors at the temperature range of interest. These models are technology specific. The models cannot be ported across technology generations (including evolution from the lower to higher resolution in the same foundry), or from one process technology to another.
- Development of temperature specific transistor design rules to enhance parts lifetime and minimize changes in transistor performance due to hot carrier injection (HCI) at low temperatures. These rules need to be empirically evaluated as a function of process technology whenever there is a process enhancement or scaling of the process node.
- Creation of new circuit topologies that compensate for any observed transistor anomalies in the temperature range of interest. Significant challenges exist in creation and design of cold and wide temperature circuits for all electronics applications including analog, mixed signal, digital, memory and RF. The limited choice of models for temperature circuit simulations for applications beyond the military specification temperature of -55 °C to +125 °C (218 K to 398 K) makes it more difficult and time consuming to create these circuits.
- Development of new qualification methods for cold electronic technologies and products used in cold and wide temperature applications.

7.5.2 Gap Analyses

The custom electronics development is summarized and compared in the Table 7.5-1.

Table 7.5-1. Custom Electronics Development Summary

Technology/ Process	Available	Cold Analog & Mixed Signal	Cold RF	Cold Digital	Cold High Density Digital SOC	Cold Circuit Library	Desired features for cold Electronics	Current State of Development
Bulk CMOS (180 nm) TSMC, UMC	Off-Shore	Yes	No	No	No	Not available	• CMOS, • Low cost	• Mature process. • High Volume. • No Cold Device Model • No Cold Circuit Library
PD SOI CMOS (0.35) Honeywell	On Shore	Yes	No	No	No	Quad Op Amp	• CMOS • Rad hard, • Cold characterizati on data	• Mature Process, • Low Volume • Available to selected customers.
FD SOI (22nm GF)	Off Shore	Maybe	Maybe	Yes	Yes	No	• CMOS • Access to the body of transistors	• Mature process • High volume, • No cold device models • No cold circuit library
SiGe BiCMOS (90nm GF)	On Shore	Yes	Yes	Yes	No	Yes (Primitive)	• SiGe HBT which does not suffer from carrier freezeout • CMOS	• Mature process • High volume, • Cold device models • Cold digital and analog circuit library based on ECL • Cold RF circuit Library

The library of 90 nm SiGe analog, digital, and RF circuits for cold space applications developed under the COLDTech and LuSTR projects is not able to address the overall performance needs necessary to support the cryogenic and wide temperature range circuit functions needed for lunar applications ***[F-10]****.*

- For analog applications:
    - The SiGe analog cell library is limited to primitive functions and does not have all the functional blocks necessary to build high performance mixed-signal circuits such as ADCs and DACs for space applications, precision sense/control of instruments, or drive/actuation of effectors.
    - The CMOS-only building blocks developed by commercial institutions are not publicly available for broad use.
- For digital applications:
    - The library of SiGe based standard cells can only support lower speed applications (below 50 megahertz (MHz)). More effort is needed to develop high-speed, low-power digital circuits.

    - Digital standard cell libraries in advanced 90 nm CMOS-only technology nodes rapidly exhaust their voltage headroom at lower temperatures due to the increase in their threshold voltages. New circuit topologies that obviate this headroom limitation can be used to generate a library of digital elements suitable for NASA's cryogenic applications.
    - The FDSOI CMOS properties for analog applications for cryo-temperatures and the potential ability to exploit back bias for temperature compensation are not well known.
- For RF applications:
    - The existing effort demonstrated high performance SiGe RF building blocks (at X-band, 8-12 gigahertz (GHz)), but these building blocks are not yet employed for development of complex RF electronic functions such as wide temperature transmitter and receivers. In addition, the library of RF blocks is not complete, and requires expansion into multiple RF Bands (e.g., Ka band) as well as extensions for additional functionality. While the extant set of RF building blocks provides a high confidence, a complete RF system cannot yet be built from the existing set of RF blocks.
- Appendix C lists the elements in the current SiGe library and the timeline of their development, fabrication, and testing.
- There is a lack of manufacturer supported tools, simulation models, and design rules for development of advanced cold and wide temperature range circuits:
    - Simulation models, design rules, and technology files for extreme cold and wide temperature electronics, are technology-node and foundry specific. They are developed by the research and user groups developing these non-standard electronic libraries. These files are not supported or endorsed by the foundries and are not as comprehensive as the technology rule decks typically provided by the foundries. In the absence of full foundry-supported design files, a lengthy and iterative design and fabrication process is used for design and optimization of low temperature electronics. Provision of the types of rule decks, normally supplied by the foundries, would make development of these electronic parts more efficient, lower cost, and improve the probability of first pass success.
- Technology scaling and obsolescence:
    - Cryogenic transistor modeling and characterization work needs to continue for the next generation commercial integrated circuits (IC) technologies on an on-going basis to address the commercial obsolescence of technologies. NASA originally sponsored research on the development of the cold and wide temperature electronics on 0.5µm SiGe BiCMOS technology. Today, this older technology node is no longer available via cost-effective multi-project wafer foundry runs. Similarly, NASA's current effort in establishing infrastructure in 90-nm SiGe BiCMOS process technology will need to be migrated downstream to the future generations of the technology as those come on-line.
- There is a lack of proven practices and standards for qualification of commercial technologies and products for cryogenic applications:
    - Current steps in development of cold temperature products include characterization of transistors for the temperature range of interest and the development of models and design rules. These efforts only provide essential information for the design of circuits suitable for operation in their specified temperature ranges. Once the product

is fabricated, full qualification of the low temperature products is still required. At present, the product qualification for cold temperature electronics is based on the extension of current IC product qualification practices to the cold and wide temperature ranges of interest, utilizing arbitrary margins that vary from project to project. This method is costly and discourages the development of cold electronics. To encourage industry to consider custom low temperature electronics, a low cost, highly optimized and universally agreed upon set of standards are needed for qualification of low temperature technologies and products.

7.6 Passives for Cold Environment

7.6.1 State of the Art

In the design of electronics, the term "passive parts" refers to parts that are not semiconductors but are based on the fundamental electrical properties of inductance (L), capacitance (C), and resistance (R). Passive parts are essential to an analog circuit's ability to manipulate electrical signals because they transform, store, or dissipate energy. They apply to virtually all analog electronics circuits from RF communications, sensors, instrumentation and control, electrical power generation, power conversion, and electro-mechanical drive systems.

Passive parts, particularly reactive (i.e., inductive and capacitive) parts, are rarely used alone in a circuit. The following are commonly used combinations and their applications. Resistor-Capacitor (RC) circuits are often used in concert with semiconductor-switches for timing pulses and frequency generation. Resistor-Inductor (RL) circuits are commonly used for high frequency applications where the inductor allows DC to pass but blocks high frequency current. Inductor-Capacitors (LC) circuits often use LC natural resonance properties for stable oscillators and system reference clocks. These circuits are used as signal filters and to suppress transients. Power systems use LC parts for a variety of voltage conversion applications and are often employed in combination with semiconductor switching for pulse width modulation (PWM) power controls.

Typically, passive parts used in spaceflight missions are military grade with a temperature rating of -55 °C to +125 °C (218 K to 398 K). Part-level tests have been performed to characterize the performance of passives over a range of frequencies and temperatures below the manufacturers' rated operating temperature. The testing performed included parametric characterization, low temperature exposure in liquid nitrogen, and limited thermal cycling over an extended temperature range. Results varied somewhat depending on parts construction and materials used in each part, but overall, several promising candidate passive part types have been identified through this testing. More specific findings for each category of passive part are detailed below.

Crystal Oscillators are a unique element that are sometimes considered "passive." They are used to provide a well-defined and accurate frequency reference for various types of circuits from digital to RF. Crystal Oscillators that operate at cryo-temperatures are commercially available.

7.6.1.1 Resistors

Resistors are commonly used to limit current flow (e.g., limiting the current to an LED). Resistors in series can act as voltage dividers and thus serve to set the bias voltage on transistors. These are used to set the feedback voltage and thus set the gain on amplifiers. Resistors are often used as line terminal resistance or as shunts to dissipate circuit energy as thermal load. Resistors typically have a positive Temperature Coefficient of Resistance (TCR) due to the increase in

electron thermal scattering with increasing temperature. Thus, a resistor will typically decrease in resistance with decreasing temperature. TCR depends on the resistor material and certain materials minimize the TCR. Note, the TCR may not be constant over a wide temperature range.

Table 7.6-1 is based on earlier NEPP funded work and compares the performance of various resistors [ref. 36].

Table 7.6-1. Performance of Various Types of Resistors at Low Temperatures

Type	Value (Ω)	Temp Coeff (ppm/°C)	Resistance (Ω) at 25 °C	Resistance (Ω) at -190 °C	Change in Res (%) at -190 °C
Metal Film	10	±25 to ±200	10	9.99	0.0
	1K	±50	999.15	1001.86	0.3
Wirewound	10	±30	9.7	9.62	-0.9
	1K	±30	984.8	979.31	-0.6
Thin Film	33	±250	33.07	34.32	3.8
	1K	±100	995.41	1007.88	1.3
Thick Film	100	±100	99.99	105.42	5.4
	1K	±100	998.7	1003.22	0.5
Carbon Film	10	±350	9.96	10.46	5.1
	1K	-450	980.3	1035.83	5.7
Carbon Composition	15	n/a	14.65	16.34	11.6
	1K	n/a	1013.29	1296.54	28.0
Ceramic Composition	10	-1300±300	9.49	10.99	15.8
	1K	-1300±300	993.09	1167.51	17.6
Power Film	10	-20 to +50	10	10.48	4.9
	1K	-20 to +50	996.2	1037.06	4.1

“Thermistors” are specialized resistance parts specifically designed to be sensitive to temperature and are available as positive temperature coefficient (PTC) and negative temperature coefficient (NTC) types.

- PTC Thermistors are formulated from materials that have non-linear sensitivity to temperature and are commonly used as circuit protection parts.
- NTC Thermistors, unlike common resistors, are based on semiconductor materials and typically used in temperature sensing.

Thermistors for measurement in cryo-temperature applications are available commercially from vendors that specialize in cryogenic control equipment. Thermistors can be used in electronic temperature compensation circuits where resistance changes with temperature can compensate for a drift in a part’s electronic parameters due to temperature changes.

General findings are listed below:

- Resistors with a low TCR such as Wire-wound and Metal Film resistors have low sensitivity to temperatures and are available commercially.
- Thermistors (PTC, NTC) may be useful as temperature compensation parts to stabilize analog circuits over a wide temperature range.
- Thermistors for cryo-temperature applications are available commercially.

7.6.1.2 Capacitors

Capacitor performance at cryo-temperatures depends heavily on the permittivity of the dielectric material between the capacitor plates. Permittivity is related to the ability of a material dipoles to

align with the electric field. If the material's dipole alignment is inhibited at cryo-temperatures, then permittivity, and thus capacitance, is reduced. Capacitor dielectrics must be characterized at cryo-temperatures to determine if their parameters shift significantly. In Table 7.6-2, the changes in the Capacitance and Dissipation Factor are indicated [ref. 36]. Note that Negative-Positive-Zero (NP0), Polypropylene, Polyphenylene Sulfide (PPS), and Mica[5] all indicate that properties remain largely unchanged at cryo-temperatures.

Table 7.6-2. Relative Change in Capacitor Properties from Room to Cryogenic Temperatures

Material	Ceramic NP0	Ceramic X7R/ Y5Y/ Z5U	Poly-propylene Film	PPS Film	Poly-ester	Poly-carbonate	Mica	Electro-lytic	Solid Tantalum
Capacitance	Stable	Major Decrease	Stable	Stable	Slight Decrease	Slight Decrease	Stable	Major Decrease	Slight Decrease
Dissipation Factor	Stable	Major Increase	Slight Decrease	Stable	Slight Decrease	Slight Decrease	Stable	Major Decrease	Major Increase

Furthermore, the performance of electrolytic capacitors is influenced by the shifting properties of the electrolyte used in the construction of the capacitor. Wet electrolytic capacitors are unsuitable for use in cryogenic applications, due to the freezing of the electrolyte. Solid electrolytic capacitors can see considerable shifts in both capacitance and equivalent series resistance (ESR) but will not suffer the extreme effects wet electrolytic capacitors do when they freeze.

Recent NASA funded work demonstrated high energy density capacitors that are insensitive to temperatures. These capacitors are based on polymer dielectric formed using Radiation Crosslinked Acrylate Monomers.

General findings are listed below:

- Air gap capacitors are insensitive to temperature but have low capacitance compared to dielectric caps of similar size and weight.
- Generally, wet electrolytic capacitors are not suited to cryo-temperature operation because of electrolytes will freeze.
- Solid electrolytic capacitors can operate under cryo-temperatures but may experience substantial parameter shifts.
- Capacitors that exhibit the best temperature immunity, such as Class 1 multilayer ceramic capacitors (MLCCs), are only available in smaller values (less than 1 uF).
- A number of capacitors with low sensitivity to temperature are available commercially.
- Radiation Crosslinked Acrylate Monomer dielectric capacitors have been tested down to -269 °C (4 K). These appear suited for cryo-temperature applications but may need to be custom manufactured.

7.6.1.3 Inductors

The core material of an inductor heavily influences their properties at cryo-temperatures. Inductors can be simple coreless (air core) coils, or they may be coils wrapped around a core material. Air core inductors show an inherent immunity to temperature changes, due to their lack of a metallic core. Solid cores are generally made of metal laminations or powdered metallic materials in a binder matrix to prevent eddy current losses and are a highly customizable part of

[5] Negative-Positive-Zero (a type of ceramic material), Polypropylene - another material, PPS - PolyPhenylene Sulfide - yet another, Mica - a mineral also used in capacitor construction.

an inductor. Cores also serve to contain the magnetic field while coreless inductors form open magnetic fields that can interfere with other parts. Core materials include iron powder, manganese-zinc ferrite, molybdenum permalloy powder, nickel-zinc ferrite, silicon steel, and many proprietary material blends. Characterizing a selected inductor core material behavior at cryo-temperatures is essential to circuit modeling and design analysis. In Table 7.6-3, the changes in core properties are compared [ref. 36].

Table 7.6-3 Comparison of Core Materials at Cryogenic Temperature with Room Temperatures

Core Material	Molybdenum Permalloy Powder	High Flux Powder	Kool Mu Powder	Nano-Crystalline	Amorphous	Ferrite
Permeability	Stable	Stable	Decreases	Increases	Stable	Major Decrease
Loss	Increases	Stable	Stable	Increases	Increases	Major Increase
Saturation	-	-	-	Increases	Increases	-

General findings are listed below:

- For cryo-temperature applications, air core inductors are largely insensitive to temperature however they have relatively low inductance, and the open magnetic fields can interact with nearby materials.
- Compared to air core inductors, solid cored inductors provide greater inductance and greater field containment; however, core material properties may be more sensitive to temperature changes.
- Ferrite cores generally exhibit large shifts in inductance and not well suited to cryo-temperatures applications.
- High Flux exhibits both a stable permeability and loss over the tested temperature range.
- Kool Mu decreases in permeability.
- The amorphous and nanocrystalline cores have similar or even higher permeability and saturation flux density at cryo-temperatures though the magnetic loss increases.
- Nanocrystalline magnetic cores are well suited for inductors used in power converter applications and have been evaluated down to -196 °C (77 K) with only some loss in linearity.

7.6.2 Gap analyses

Resistor, capacitor, and inductor suitable for cryo-temperature operations may be available as COTS/MIL parts but require further characterization tests at cryo-temperatures ***[F-11]****.*

7.7 Electronic Packaging for Cold Environment

7.7.1 State of the Art

7.7.1.1 Technology Overview

Electronic packaging provides a means of electrical interconnection between active electronic parts (such as transistors or integrated circuits), passive electronic parts (such as resistors or capacitors), sensors, actuators, antennas, and other electronic systems. In addition, electronic packaging provides mechanical protection, chemical protection, and thermal dissipation paths. The selection of packaging technologies, processes and materials is dependent upon the

electrical, thermal, functional, mechanical, and environmental requirements of the system. System level reliability is determined by the characteristics of each of these elements under use conditions, and is dependent upon packaging design, manufacturing processes, and design life. The reliability of these packaging elements can be challenging for cold temperature electronic packaging due to the stresses induced at interfaces resulting from the differences in coefficient of thermal expansion (CTE) between materials and the wide temperature differences between the high and low temperature extremes of the application. In practice, these stresses are addressed through the careful selection of materials with closely matched coefficients of thermal expansion as well as mechanical design compensation for the known expansion differences. It should be noted that the zero-stress condition is not room temperature but rather fabrication processing temperature. For this reason, low melting point solders are particularly attractive. When two elements are joined together (joint), the strength and modulus of each material within the assembly additionally impacts the stress distribution within the joint. Connectors and cabling for cryo-temperatures are commercially available and designed to withstand large thermal excursions to cryo-temperatures while maintaining mechanical durability and electrical characteristics. Connection points to the printed circuit board assembly are treated as joints in the discussion below; however, stress relief details and implementation strategies are beyond the scope of this discussion. While many well-designed assemblies can withstand limited thermal excursions, repetitive thermal cycling over a large temperature range can lead to fatigue failure of joints and interfaces. For lunar environments, certain applications will require extended operation at very low temperatures while others must withstand multiple thermal cycles over a wide temperature range. Additional challenges may result from the concomitant application of vibration at low temperatures or the intermittent application of high temperatures that modify material properties. A review of available literature on cold electronic packaging is provided in Appendix D. While some research has been done in extreme low temperature materials systems for applications such as Mars surface landers and rovers, as well as quantum computing and unique scientific applications such as read out integrate circuits (ROICs) for deep infrared telescopes, these do not cover the thermo-mechanical environment expected for long duration missions to the lunar surface in the regions defined in Section 7.2.

7.7.1.2 Summary

A summary of relevant technologies for different environments outlined in Section 7.2 is provided below. For a more detailed description of these studies please see Appendix D. Thermal ranges have been separated to highlight the impact of fatigue and elevated temperature exposure (Group 1) and extreme low temperature exposure alone (Group 2) on the selection of materials and technologies for cold temperature electronic packaging.

Group 1: Wide cold temperature cycle

Permanently Stationed Platforms:

- Equatorial -180 to +125 ℃ (93 to 398 K)
- Mid Latitudes: -145 to +80 ℃ (128 to 353 K)

Mobile Platforms:

- Roving Broadly -145 to +120 ℃ (128 to 393 K)

Studies for Europa and lunar applications indicate that CTE matching of parts is critical for this temperature regime. Pure Indium (In) may be problematic due to the upper limit of this

temperature range, potentially resulting in creep within joints as well as the growth of intermetallic compounds [refs. 38, 39, 40]. Standard printed circuit boards were used for several studies but required structures to accommodate stresses resulting from CTE differentials.[refs. 41, 42] Leaded parts have demonstrated survival using traditional Lead-Tin (PbSn) solders; however, there may be issues with leadless devices or column grid arrays [refs. 43, 44]. Fatigue of PbSn solder joints may become an issue for large thermal cycle applications. 50In50Pb solder joints may be a good alternative solder technology, but care must be taken to properly implement this material since process requirements are different from traditional solders. Various material options have been demonstrated for attachment of die at this temperature range; however, care must be taken to ensure the proper thickness, pattern, and cure conditions, especially for polymers.[refs. 41, 45] This is particularly important for attachment of larger substrates and devices. Polymer encapsulants for wire bonds and underfills for flip chip arrays may cause premature failure, due to the stresses imparted on the encapsulated interconnects as a result of the applied temperature [ref. 45]. Certain filled molding compounds may work but require further investigation to determine if the fillers initiate fatigue cracks within the polymer or interface cracks with the lead frame, leading to device failure [ref. 46]. Further work is required to define material properties for the entire temperature regime. This will allow the development of proper models for stress analysis and accurate definition of accelerated test parameters. Screening of different package types, considering the mechanics of failure, would be valuable in developing a database of proven packaging configurations. Finally, most studies are limited to a few hundred cycles. Applications that require greater than 500 cycles require more testing to verify suitability of the packaging technologies.

Group 2: Extreme low temperature exposure

Permanently Stationed Platforms:

- Poles -223 to -193 °C (50 to 80 K)
- PSR -233 °C (40 K)

Mobile Platforms:

- Transport in/out of PSR -233 to -40 °C (40 to 233 K)

This application condition is like the cryogenic detector applications. CTE differences and processing temperature will have a significant impact on reliability and performance. Pure In is particularly attractive since it retains ductility at such temperatures and has a low processing temperature. InPb alloys should be considered for the attachment of parts. As shown with the detector support electronics discussion detailed in Appendix D, standard Sn63Pb37 solder may also be a viable alternative for systems that can accommodate the higher processing temperature. Multiple substrate layers may be required to accommodate the CTE differences between the device and the printed circuit board if this option is selected. High density flip chip attachment between Si die and Si interposers using In bump bonds have a rich history at this temperature. Au wire bonding and thin Al wire bonding have been implemented between interposers and the next layer of interconnects. The use of high-density packages, however, may be problematic. Testing of different high density packaging technologies is warranted. Even though cycling may not be required for the application, it will be required for ground testing. Applications that require cycling and/or concomitant application of vibration loads have not been addressed and will need testing. As discussed above, further work is required to define material properties for the entire temperature regime, to allow the development of proper models for stress analysis, and the definition of accelerated test parameters [refs. 47, 48].

The thermal cycle life of electronic assemblies is addressed in NASA standards under the category of hardware that is susceptible to thermally induced structural fatigue. As stated in GSFC-STD-7000B, "General Environmental Verification Standard (GEVS) for GSFC Flight Programs and Projects", which is used by multiple centers, thermal cycle testing "shall be performed on prototype hardware. The life test should normally be performed at the worst case (limit level) predicted temperature extremes for a number of thermal cycles corresponding to the required mission life. However, if required by schedule considerations, the test program may be accelerated by increasing the temperature cycle range (and possibly the temperature transition rate) provided that stress analysis shows no unrealistic failure modes are produced by the accelerated testing" [ref. 49]. Such stress analysis of electronic assemblies requires accurate material properties for the assembly elements over the entire temperature range. For electronic assemblies, these material properties are not readily available. The European Space Agency standard, ECSS-Q-ST-70-61C, "Space product assurance: High reliability assembly for surface mount and through hole connections" discusses the qualification of packaged assemblies in detail. Temperature limits for the test must cover the minimum and maximum temperatures observed by the hardware in the intended mission profile and ground testing. The number of thermal cycles for electronic packaging hardware qualification must cover all on-ground and in-orbit thermal exposures with a safety margin of at least 2x. As with GEVS, the test program may be accelerated by increasing the temperature cycle range. The modified Coffin-Manson (Norris-Landzberg) equation can be used for the calculation of the equivalent thermal cycles. The coefficients used for the equation defined in the standard are valid for SnPb solder joints as the failure point [ref. 50]. Such equivalent thermal cycles are either to accelerate thermal cycles, reducing the amount of time required for test, or to limit fatigue damage of parts by reducing the temperature range and increasing the number of cycles. JPL design practices require that electronic hardware be capable of "surviving thermal cycle environments that are three times the service life, which includes the planned preflight ground testing environments, worst-case expected mission cycles with worst-case flight temperature excursions, operational self-heating, and power on-off temperature cycling." A package qualification process similar to that applied at JPL is provided by Ghaffarian [ref. 43]. For each of the fatigue susceptible processes discussed, the process begins with determination of total cycles and temperature limits of the application. This is most often performed by the project thermal engineer. In certain cases, there are very few extreme cycles and many cycles in a much narrower temperature range. For these cases it is important to break down the number of cycles and the ranges. MEAL for the purposes of electronic packaging is generally concentrated on thermal cycle life [ref. 51].

7.7.2 Gap Analyses

There are two major gaps in the current state of technology.

- *Limited published studies exist with a low number of thermal cycles (less than 100 cycles) over wide cold temperature ranges (minimum temperature below -120 °C and delta of 205 °C (153 K and delta of 205 K) and for a limited number of packaging solutions, generally not addressing COTS, high speed processing, high frequency or high-density solutions **[F-12]**.* This is particularly the case for large cycle count (greater than 100 cycles) applications.

  A summary of the state of electronic package technology and achievable thermal cycling levels following evaluation and modification is provided in Table 7.7.2-1 below.

The three values in parentheses are defined as:

- Current knowledge of the assembly surviving a certain number of thermal cycles over a specified temperature range and application
- Using current knowledge, the achievable number of thermal cycles over a specified temperature range and application.
- Over a specified temperature range and application, the number of thermal cycles achievable through test and potential modification of current best design.

Specifically, numbers assigned for the above values are:

- (5,5,5) (Very High, 1000-2000 Cycle, 1000-2000 Cycles)
- (4,4,4) (High, 500-1000 Cycles, 500-1000 Cycles)
- (3,3,3) (Moderate, 200-500 Cycles, 200-500 Cycles)
- (2,2,2) (Low, 100-200 Cycles, 100-200 Cycles)
- (1,1,1) (Very Low, <50 Cycles, <50 Cycles)
- M refers to modification of package assembly

Examples of how to interpret Table 7.7.2-1:

- For a ceramic quad flat pack (CQFP) leaded package with a size greater than 0.5 inch (greater than 100-350 leads) under -180 to 25 °C, the matrix is (1, 2, 4M) which means ([current knowledge of the package surviving over -180 to 25 °C is very low], [expected survival is 100-200 cycles over -180 to 25 °C], [by testing the assembly and modifying as needed, it is possible to increase the survival to 500-1000 cycles over -180 to 25 °C])

Table 7.7.2-1. State of Electronic Package Technology (mounted onto printed circuit board) and achievable cold temperature thermal cycle survivability levels

Type↓/TC Range→	-55°C/125°C	-100°C/125°C	-180°C/125°C	-220°C/85°C
SMD Passives: Resistors, capacitors, diodes, inductor (no modification) <0806 size & leaded type > 1206 size	 (5, 5, 5) (3, 3, 3)	 (4, 4, 5) (3, 2, 3)	 (2, 2, 5) (2, 2, 2)	 (1, 2, 5) (1, 1, 2)
Crystal Oscillators/RF: Ceramic leaded pkg, LCC/QFN <0.4 inch <20 leads or no-lead >0.5 inch >20 leads or no Lead	 (4, 4, 5M) (3, 2, 5M)	 (2, 4, 5M) (2, 1, 5M)	 (1, 3, 4M) (1, 1, 4M)	 (1, 2, 4M) (1, 1, 4M)
Ceramic Microcircuit, ASIC, Memory: CQFP, leaded package <0.4 inch <50 leads >0.5 inch >100-350 leads	 (5, 5, 5) (5, 4, 5M)	 (3, 4, 5M) (3, 3, 5M)	 (2, 3, 5M) (1, 2, 4M)	 (1, 3, 5M) (1, 1, 3M)
Ceramic CGA FPGA: (no modification) <0.8 inch <500 Columns >1 inch >700-1700 Columns	 (5, 5, 5) (4, 4, 4)	 (2, 4, 4) (3, 3, 3)	 (2, 3, 3) (2, 2, 2)	 (1, 2, 2) (1, 1, 1)
COTS BGA FPGA & memory: <0.8 inch <200 >0.8 mm Pitch >1 inch >400-1900 balls 1mm Pitch	 (5, 4, 5M) (3, 4, 4M)	 (2, 3, 4M) (1, 2, 3M)	 (1, 2, 3M) (1, 1, 3M)	 (1, 1, 3M) (1, 1, 2M)
COTS BGA FPGA & memory: <1 inch <200 balls 0.8-0.4 mm Pitch	 (3, 3, 4M)	 (2, 3, 4M)	 (1, 2, 3M)	 (1, 1, 3M)
COTS/Class P Microcircuit, ASIC, Memory: QFP, leaded package <0.4 inch <50 leads >0.5 inch >50-100 leads	 (5, 5, 5) (4, 4, 4)	 (2, 3, 4M) (1, 2, 3M)	 (1, 2, 3M) (1, 1, 2M)	 (1, 1, 3M) (1, 1, 2M)

- Traditional packaging design and implementation strategies may not be sufficient to meet the thermomechanical fatigue requirements or performance requirements of the application; however non-standard material solutions can be challenging to implement reliably. *Accurate material properties, such as CTE, strength and modulus, for the relevant electronic packaging elements over the entire temperature range as well as processing guidelines for these materials are critical and not readily available **[F-13]**.*

7.8 Power Systems and Energy Storage and Electronics for Cold Environment

7.8.1 State of the Art of Power Systems

In the discussion of power applications found in Appendix E the NESC team determined that power generation, power regulation, power distribution, and power loads involve essentially every electronic circuit type. This includes sensors, analog amplifiers, analog to digital and digital to analog conversion, voltage references, frequency oscillators. digital logic controls, and feedback controls, power switching and PWM regulation, voltage transient suppression, and passives parts. The main distinction is power applications involve high voltages, high currents and exposure to high voltage transients as well as extremely low temperatures.

Cold electronics for power applications can apply to both lunar robotic missions and human missions. The current generation of Commercial Lunar Payload Services (CLPS) landers only expect to operate for a single lunar cycle. The reason for such a short operating life was (a); the expectation that battery cells will not survive the lunar night cycle, and (b): the expectation that electronics cannot physically tolerate and reliably operate at temperatures that may be as cold as

-173 °C to -223 °C (100 K to 50 K) [ref. 52]. Since then, NASA GRC demonstrated that small Lithium-Ion cells can tolerate the freeze/thaw cycle and recover when warmed. Lunar power hibernation is a strategy to survive the extreme cold environment of a 354-hr lunar night that is dependent on cold electronics to restore systems at lunar dawn [ref. 53].

For human missions such as the Artemis program's Human Lander Systems (HLS), many parts of the vehicles are exposed to cryogenic propellant temperatures for long durations starting in tanking operations in Earth orbit, loitering in lunar orbit, and operating on the lunar surface. The capability to operate electronics without constant heating can reduce power consumption while reducing overall power system mass.

7.8.1.1 Power Applications in a Lunar or Cryogenic Environments

This section identifies the electrical power functions found on both robotic and human scale lunar lander missions. The intent is to determine what power functions require cold electronics. This section is regarded as a summary of what is covered in Appendix E.

- **Photovoltaic Solar Array:** Photovoltaic solar arrays are typically composed of Silicon or Gallium-Arsenide/Germanium and can be affected by improved carrier mobility at cold temperatures but may also begin to suffer from carrier freezeout as temperatures drop even lower [ref. 54].
- **Solar Array Regulation:** The electronics employed depend on the regulation approach. For simple spacecraft a direct energy transfer (DET) approach is used where the array delivers current directly to the main bus. To regulate the voltage a sequential switching shunt regulation (S3R) scheme is used to shunt excess power away from main bus [refs. 55, 56]. This regulation scheme may employ a simple set of Op-Amp comparators to enable/disable the switching elements. A more sophisticated regulation scheme optimizes the efficiency of the voltage-current operating point of the array output This scheme is often referred to as Max Power Point Tracking (MPPT). In this case, a digital algorithm may be used to manipulate the operation of the voltage converters attached to each array string. The algorithm assures that all converters output a set voltage to the bus despite variations in string output [ref. 56]. Therefore, cold electronics in array regulation may involve a combination of digital, analog, and switching devices.
- **Array Pointing/Tracking:** In this case, the cold electronics are used for detecting the sun position and for pointing and continuously tracking the sun position. Motor control and drive electronics with position and speed feedback are required. These will need to operate at temperatures down to -223 °C (50 K).
- **Main Bus Control and Power Distribution:** The main bus control electronics plays a key role for a spacecraft that uses hibernation as a lunar night survival strategy. Since the main bus connects the solar array, batteries and distribution elements, it is essential to the startup of the spacecraft. Normally, a spacecraft powers up on batteries. However, in a hibernation recovery scheme, the main bus powers-up on solar array output at lunar dawn. The battery is assumed frozen and isolated from the bus. This requires that the main bus minimizes loads and, instead, prioritizes the array output on providing heater power to the batteries and any other devices that need to be warm to operate. Therefore, the main bus electronics must be capable of independently starting up and operating at temperatures that may be as low as -223 °C (50 K). Upon reaching operating temperature, the battery is reconnected to the main bus. Power distribution to loads may require voltage conversion circuit and a specialized power converter controller. Individual power channel switching typically involves analog

circuits that detect and isolate faulted circuits to protect the main bus [ref. 58]. Therefore, power distribution may require a combination of passive energy storage devices, as well as digital and analog devices that can operate at temperatures down to -223 °C (50 K).

- **Battery Management System**: In the last two decades, Li-ion technology, particularly small cylindrical COTS 18650 cells, have come to dominate spacecraft battery design. Furthermore, the small cell format has been demonstrated to successfully tolerate multiple freeze/thaw cycles in lab tests at GRC and by the Mars Ingenuity Helicopter. Li-ion cells will freeze around -73 °C (200 K) which is well above the minimum night temperature -223 °C (50 K). For a spacecraft recovering from hibernation, the BMS will need to activate and support the MBC by monitoring temperatures and voltages and regulating internal battery heaters [ref. 53]. The BMS may be composed of analog, digital and power switching electronics that have cold start capability and the ability to operate at lunar dawn temperature.
- **High Power Motor Drives:** Spacecraft currently in development are seeing a dramatic shift in their propulsion systems from traditional hydraulic and mechanical actuators toward an all-electric approach. Compact, high-torque electric motors developed for the electric vehicle industry have migrated into spacecraft applications, including thrust vector controls (TVC) actuators, high power cryocoolers for propellant boil off control, and electric propellant turbopumps. These applications have very high current demands and will need to have batteries and drive electronics mounted close to the motors to minimize bus disturbance. Typically, these motors are brushless DC motors that require specialized motor controllers for regulating motor torque, speed, and phase commutation [ref. 60]. For lunar robotic missions, the main application is the wheel drive motors for rovers where both the wheels and motors are exposed to the lunar surface environment. To minimize the transmission of electromagnetic interference due to motor commutation and drive signals the motor drive electronics is best located close to the motors. In this case both the motors and the supporting drive electronics are directly exposed to the cold lunar environment. For large scale human missions such as Artemis, motor electronics may be close to cryogenic propellants and thus need to operate at cryo-temperatures.
- **Transient Voltage Suppression:** The increasing use of high-power electric motors and actuators for large flight systems creates large voltage transients. In the case of thrust vector control actuators, their frequent motion reversals that may cause current reversals and voltage spikes. This creates a need for substantial filters and Transient Voltage Suppression (TVS) devices that share the cryogenic operating environment. Most TVSs are variants of Zener diodes that rely on a preset breakdown voltage to limit voltage transients. Each type has a temperature coefficient that governs how the breakdown voltage changes with temperature [ref. 61]. Another protection device for off-nominal situations is a Metal-Oxide Varistor (MOV) commonly constructed from Zinc oxide (ZnO) that conducts only above a preset voltage. MOV devices are comparatively insensitive to temperature [ref. 62].

7.8.1.2 Types of Cold Electronics Circuits for Power Applications

Analog Cold Electronics in Power Applications: Analog circuit operate in the linear region and are very sensitive to variations in operating temperature. The temperature dependent parameter drift can be substantial for cryogenic applications, and device-to-device interfaces can drift to a point where they are no longer compatible, and operations become unstable. Integrated circuits may account for drifts in parameters due to temperature changes, through device

materials and structures or specialized temperature compensation techniques. For COTS/MIL analog IC devices, internal temperature compensation rarely extends beyond the 125 °C to -55 °C (398 K to 218 K) range. For complex analog circuits, it may only take a drifting voltage reference or a reference oscillator to trigger a circuit-wide malfunction. Since so many analog functions are sensitive to temperature it is essential that temperature compensation techniques be extended across the entire lunar environment range.

The transistor technology has a huge impact on the device sensitivity to temperature. For example, Bipolar Junction Transistors (BJT) made in silicon have properties that are dependent on temperature and can be used as temperature measuring devices. Unfortunately, they are prone to severe carrier freezeout effects – a phenomenon in semiconductor devices where there is a reduction of free electrons in the device as temperature drops. Due to freezeout, the gain of the BJT will drop very low as the temperature drops, and in many cases simply cease to operate even at temperatures above liquid nitrogen levels. However, research indicates that BJTs made in silicon carbide may fare much better, with gains that can survive the drop in temperature.

Meanwhile, silicon field effect transistors (FET) are substantially less sensitive. Complementary MOSFET or CMOS technology, and particularly FDSOI versions of CMOS, are capable of operation down to a few degrees Kelvin. They are still prone to parameter drift, but FDSOI CMOS offers the ability to exploit “back bias” to compensate for gate threshold voltage drift. FDSOI CMOS is, however, susceptible to hot carrier damage at extremely low temperatures [refs. 30, 31].

SiGe is an alternative that has reliable performance at extremely low temperatures. SiGe exploits HBTs which are not prone to hot carrier damage. Fairly complex IC can be rendered in SiGe. Section 7.5 discusses the state of the art in Analog SiGe, and SOI CMOS.

Digital Cold Electronics in Power Applications: Digital electronics transmit signals as simple binary states (or transitions between states) which makes them innately less sensitive to variations in signal voltage and to noise. It also makes digital circuits somewhat insensitive to temperature. Modern digital electronics are dominated by CMOS transistor technology which is also less sensitive than bipolar devices. As noted in the analog section, FDSOI CMOS back bias feature allows the device to adjust for threshold voltage drift. Standard CMOS and FDSOI CMOS are likely the best solutions for very large-scale ICs at extremely low temperatures, but, depending on the process node, as in analog applications, may also be prone to hot carrier damage. Section 7.5 provides additional discussion of the state of the art of these technologies.

Mixed Signal Cold Electronics in Power Applications: Mixed signal refers to a circuit that incorporates both digital and analog functions. Mixed signal ICs are often used as specialized devices, such as motor controllers, that involve several analog signal inputs and outputs but are managed by a digital controller. The primary issue with a COTS/MIL mixed signal device for cryo-temperature applications is the tendency of the analog portion of the circuit to behave erratically or become unstable at decreasing temperatures while, in many cases, the digital functions may continue to operate normally. It may be necessary to build custom mixed signal devices. Note that SiGe, can be mixed with CMOS technology and enable digital, analog and RF functions to be integrated into complex ICs that are suitable for these applications. See section 7.5 for further discussion of the state of the art in these technologies.

Cold Electronics Power Switching: Transistor technology for switching applications may be silicon MOSFETS, but wide bandgap materials such as silicon-carbide, or Gallium-nitride are

used for higher performance. However, silicon -carbide MOSFETs typically see a dramatic increase in on-resistance at cryo-temperatures and may not be suitable for use in power conversion. In contrast, *GaN High Electron Mobility Transistors HEMT have demonstrated that they are stable across a wide temperature range down to -223 °C (50 K*) ***[F-14]*** [ref. 63].

Cold Passives (Inductors, Resistors, Capacitors) in Power Applications: Passive device cryogenic performance generally depends on material properties and device construction.

For power, inductors and capacitors are typically paired to create a resonant LC circuit that can boost or reduce voltage depending on the circuit configuration. They are most often used with switching transistors in a PWM regulated circuit. Generally, liquid, or wet electrolytic capacitors are not suited for cryogenic operation since their electrolyte will freeze, so solid electrolytic capacitors are recommended where bulk capacitance is required. Class 1 ceramic capacitors can tolerate low temperatures, but generally have lower capacitance limits. Capacitors based on Radiation Crosslinked Acrylate Monomers appear promising for power applications at cryo-temperatures.

Simple air-core inductors can operate at cryo-temperatures but have low inductance. Solid-core COTS inductors can see substantial parameter drift at cryo-temperatures. Inductor cores based on nano-crystalline or amorphous materials appear to be the best suited for power applications at cryo-temperatures. See Section 7.6 for further discussion of passive devices.

7.8.1.3 Power System Gap Analyses

Based on the preceding, with respect to the environmental conditions of 7.2, the NESC team found the following technology gaps:

Photovoltaic Solar Arrays

- Solar array characterization data for operation down to -223 °C (50 K) is required.
- Design rules are required for solar arrays surviving multiple lunar night cycles.
- There is a need to assess the risk of thermal shock at lunar dawn.

Solar Array Regulation Electronics

- Cryo-temperature characterization test data for sequential switching shunt regulator parts is needed.
- Cryo-temperature characterization test data for MPPT digital controls, analog and power switching parts is needed at cryo-temperature down to -223 °C (50 K).

Solar Array Pointing & Tracking Functions

- Optical sun sensors for cryo-temperature operations are needed.
- Hall effect sensors for cryo-temperature operations are needed.

Spacecraft BMS Cold Electronics

- Demonstration of a charge control and battery management unit capable of a cold start and operation at 50 K is needed. (Note there is STMD funded work at GRC called “ICE-CHILL” project.)
- Battery management guidelines for hibernation recovery are needed.

Power Distribution

- A microcontroller/FPGA proven to cold-start and operate at cryo-temperature down to 50 K is needed.
- High voltage inductive, resistive, capacitive (LRC) passives proven to cold-start and operate at cryo-temperature down to 50 K are needed.
- Analog fault detection, fault isolation and current limiting circuits for cryo-temperature operations are needed.

High-Power Electric Motor Applications

- A microcontroller suited for DC-DC PWM voltage control at cryo-temperatures is needed.
- A 3-phase motor commutation controller suited for cryo-temperature operations is needed.
- Hall Effect motor sensors suited for cryo-temperature operations OR an alternative sensor-less scheme (requires digital signal analysis) is needed.

High Voltage Transient Suppression

- Characterization data for TVS diodes and MOV devices at cryo-temperatures are needed.

Analog Electronics for power applications at cryo-temperatures

- There are no published guidelines on analog temperature compensation techniques for cryo-temperature applications.
- Silicon-Germanium properties for analog applications at cryo-temperatures are not well known in industry.
- FDSOI CMOS properties for analog applications for cryo-temperatures and the potential ability to exploit back bias for temperature compensation are not well known.

Digital Electronics for power applications at cryo-temperatures

- There is a need for further evaluations of COTS digital devices for cryo-temperature cold start and operations at 50 K.
- SOI-CMOS properties for digital applications at cryo-temperatures and the potential to exploit back bias for temperature compensation are not well known in industry.

Mixed Signal Devices for power applications at cryo-temperatures.

- An approach for COTS devices that combines digital and analog circuits at cryo-temperatures, and that addresses the problem of analog circuits becoming unstable at cryo-temperatures, is needed.
- Determination of an optimal semiconductor technology for mixed signal applications at cryo-temperatures is needed.

Power Switching Transistors for power applications at cryo-temperatures

- Gallium-Nitride properties at cryo-temperatures are not well known in industry.

- An approach to qualifying GaN devices for long operating life in cryo-applications is needed.

LRC Passives for power applications at cryo-temperatures

- Some COTS passives are suitable for cryo-temperature operations. Some passives may require special fabrication. However, no comprehensive guideline of LRC passives properties for power applications at cryo-temperatures to 50 K appears in literature.

7.8.2 Cold Electronics: Energy Storage

This section addresses the potential of achieving lunar night survival based on existing COTS Li-ion and ultimately operation during the lunar night using new cell technologies. The Lunar power hibernation strategy assumes the cells freeze when the lunar night temperature drops below -73 °C (200 K) and that the spacecraft is completely passive until lunar dawn illuminates the solar arrays. This section further discusses the potential of new cell chemistries and electrodes to extend the operational range and enable operations further into the lunar night. This section provides a summary of what is covered in Appendix E.

7.8.2.1 Surviving the lunar night with COTS 18650 Lithium-Ion Cells

The small format 18650 Lithium-Ion COTS cell is widely used throughout the space industry and has been used for flight applications since 2001[6]. Batteries built from 18650 and the larger 21700 cells appear in even the largest spacecraft such as Europa Clipper. In 2018 a paper by the Indian Space Research Organization (ISRO) suggested that 18650 Li-ion cells could tolerate a freeze/thaw cycle and recover their charge capacity when warmed to normal temperatures [ref. 64].

In 2019 NASA GRC in-house testing of COTS 18650 Lithium-Ion cells appear to freeze at approximately -73 °C (200 K) with cell voltage dropping to 0 Volts. The cells thaw and voltage recovers when warmed back to room temp. When tested at one atmosphere, a tendency to rupture of pressure relief burst discs was observed. It was determined that cryogenic cooling of cells creates a negative pressure relative to one atmosphere and any seal shrinkage allows external gas to enter the cell to be trapped and subsequently expand and over-pressurize the cells when warmed to normal temperatures. This over-pressure problem was eliminated when cells were tested in space vacuum environment. Subsequent cell tests successfully tolerated multiple freeze/thaw cycles and recovered their charge capacity at room temperature. *It is best to perform cryo-testing of 18650 cells in a vacuum environment since it assures that cells maintain a positive internal pressure and prevents external gas ingestion and eliminates risk of over-pressurization when returned to normal temperatures* ***[F-15]****.*

Work continues at GRC to develop a full-scale battery capable of surviving the lunar night. Two researchers funded under STMD Space Technology Research Grant, Early Career Faculty have been working to further understand and characterize the mechanics of the freeze/thaw cycle and its long-term effect on battery operational life. In this case, the researchers are taking the cells down to -223 °C (50 K). Their work so far indicates that the changes in Li-ion electrolyte chemistry during freezing are reversed in the thaw process with minimum degradation observed. Both investigators note that the freeze/thaw cycles have a small impact on cell life. In fact, they

[6] Based on NESC team knowledge, conversations within NASA, and/or with industry and academia.

find that high charge/discharge rates tend to have a greater impact on operating life than the hibernation cycle.

In 2025, new STMD funded effort under the NASA Early Career Initiative program called ICE-CHILL leverages the ECF work to advance toward a multicell battery. This GRC effort is aimed at building a multicell hibernation battery with a cold electronics-based battery management system to manage the battery recovery. The work will also involve the development of test protocols, procedures, and test parameters to assure that Li-Ion batteries intended for lunar hibernation can reliably recover.

The ability to survive the freeze/thaw cycles has been demonstrated in flight operations by the Mars Helicopter "Ingenuity" [ref. 65]. In this case, COTS high power Sony VTC4 18650 cells survived exposure to Martian night temperatures of approximately -80 °C (193 K) and recovered when warmed to Martian daytime temperatures. These cold operations were part of an extended mission following completion of the primary mission, and the cells were never tested under these conditions prior to flight.

*In summary, Li-ion cells, specifically18650 cells, were demonstrated to tolerate freeze/thaw cycles down to -223 °C (50 K) and recover their voltage and charge capacity when warmed back to room temperature. Similar small format cells (e.g., 20700, 21700, 22700 etc.) manufactured by similar processes may also tolerate the freeze/thaw process but will require cryotemperature testing **[F-15]**.* Lunar Power Hibernation involves passively surviving the lunar night and recovering at lunar dawn. For future missions, employing cold electronics hibernation should be considered a baseline capability. Note that this capability does not only enable surviving the 354-hour lunar night; it also the enables surviving the Lunar Polar Winter where the night stretches to 4.5 months of darkness and temperatures sink to -223 °C (50 K).

7.8.2.2 Advancing Li-ion Cell Technology to Operate Deeper into the Lunar Night

Operating in a hibernation mode represents a step in the evolution to enabling cold electronics. To realize cold capable electronic systems, batteries must be able to operate through the lunar night *during the cold soak periods*. Although no non-nuclear approach will operate through a 4.5 month long lunar polar winter, it may be possible to span the 354-hour lunar night with a combination of cell technologies, appropriate battery module sizing and design strategies.

The Li-ion cell liquid electrolyte serves as a medium to transport ions between the anode and cathode during charging and discharging. The transport processes are all thermally activated, and therefore depend on a sufficient temperature to enable a reasonable rate capability. Current COTS cells are limited to operations in the -20 °C (253 K) to +30 °C (303 K) range at moderate rates (e.g., discharge at C/5) [ref. 66]. The C rate represents to the time to discharge the full capacity of the cell at 1 hour, with C/5 representing a discharge of the cell over 5 hours. Wider temperature operation from -40 °C (233 K) and +60 °C (333 K) can typically be achieved, however discharging rates are very limited.

Altering the electrolyte chemistry is the easiest way to improve low temperature performance without changing the cell manufacturing process. Altering the electrolyte to maintain low viscosity at low temperatures is one way to improve ion transport performance. Another approach is to suppress the freezing/melting point. A liquid electrolyte (e.g., methyl propionate (MP)) with a melting point of -88 °C (185 K) could provide a wider operating range. This can allow discharging at low rates (typically 50 to 100-hour discharge rates) down to temperatures as

low as -80 °C (193 K) and discharging at moderate rates (C/5) to as low as -60 °C (213 K) and even -90 °C (183 K) at very low rates (<C/100). Cells operating at these temperatures were demonstrated at JPL [ref. 67].

Charging batteries at low temperatures and sufficiently high rates can result in lithium ions forming metal particles on the anode surface rather than intercalating into the anode. Plating can create lithium dendrite structures, which can puncture separators and create internal shorts, ultimately destroying the cell. Different approaches involving new electrolytes and additives have been investigated for reducing the propensity of plating to occur at low temperatures, [ref. 68]. Operationally, lunar night operations would only involve discharging, while charging could be handled in daylight, when solar power is abundant, and heaters could be employed to raise the temperature to a point favorable for charging.

An alternative approach is to employ liquified gas electrolytes, supporting operation between -60 °C (213 K) and +60 °C (333 K). This is typified by the technology demonstrated and is based on the use of gases such as 1,1-difluoroethane [ref. 69]. These electrolytes can be combined with standard COTS battery cell electrodes, to support discharge down to -60 °C (213 K).

Alternative electrodes based on conversion processes (where the ion transporting current reacts or alloys with the anode instead of intercalating within its layers) show promise in extending performance to lower temperatures. These conversion processes lend themselves to more facile kinetics relative to intercalation, potentially enabling higher rates to be achieved at lower temperatures, and cells with conversion electrodes have been tested at JPL and shown to operate down to -60°C (213 K) [ref. 66]. Cells using sodium as an anode in a conversion cell have shown operation as low as -80 °C (193 K) in prototype laboratory cells, achieving 100 low-rate cycles at -60 °C (213 K). More development is needed to mature this technology to the level of full operational cells [ref. 71].

7.8.2.3 Energy Storage Gap Analyses

The following gaps **[F-17]** were found by the NESC team in assessing energy storage at lunar surface temperatures:

- There are no known Li-ion cell technologies that can operate at < -90 °C (183 K). Cells cannot be charged at these temperatures due to issues with Li plating. Li-ion cells cannot be discharged at high rates (> C/50) at temperature < -40 °C (233 K).
- The effects of low temperature cycling on battery life are not well understood. There is a paucity of data and inadequate models for evaluation of the effects of plating on lifetime as well as the mechanical effects of multiple freeze-thaw cycles.
- Traditional intercalation electrodes based on graphite and used for most current Li-ion cells limit the performance of cells. Alternatives, including conversion electrodes, based on lithium titanate, silicon, lithium metal or on electrochemically active liquid systems, offer approaches for operating at < -80 °C (193 K) and have been recently studied but are at TRL < 3 for use in space applications. More research and development are needed in this area, with a focus on developing full, flight-like cells for testing at low temperatures.

  Electrochemical methods for energy storage are unlikely to support adequate operation cryo-temperature due to fundamental limitations with thermally activated processes.

7.9 NESC Guidance on Cold Electronics Qualification

7.9.1 No Existing Qualification Standard for Cold Electronics

Qualification is the process of demonstrating that a product can meet the specified requirements, such as those on performance, quality, reliability, environments, and safety.

No existing standards support the qualification of the electronics and packaging for the lunar environment temperature range of -233 °C to +125 °C (40 K to 398 K). The existing processes for parts and assembly qualification approach can be adapted for the extreme cold and wide environment of the lunar surface in a relatively straightforward manner with special attention to thermal margin for low temperature end ***[F-16]****.*

There are several qualification standards, specifications, and associated documents currently in use across various segments of the technical community, specifying different temperature ranges, shown in Table 7.1-1 in Section 7.1. Lunar surface temperature ranges are beyond the specifications of the existing qualification standards and, in some cases, even beyond the specifications for process and technology qualifications.

Qualification is typically performed at part and/or assembly levels and has two approaches: stress-test-driven and knowledge-based driven [ref. 72].

Most qualification standards utilize the stress-test driven approach. These are based on a standardized set of stress tests that are applied to the electronic parts and their associated packaging. The stress tests are designed to be capable of stimulating and precipitating the electronic device and packaging failures in an accelerated manner compared to use conditions.

Knowledge-based qualification differs from the stress-test-driven approach in that, rather than relying on generic stress parameter values, it is based on additional sources of information (e.g., physics-of-failure modelling [ref. 73]) application specific knowledge [ref. 74] and use condition information.

Several studies, investigations and use cases have been documented for the evaluation and qualification of commercially available COTS/MIL electronics, as well as custom electronics, targeted at applications beyond the -55 °C to +125 °C (218 K to 398 K) MIL temp range [ref. 7]. In these studies, COTS/MIL electronic parts and assemblies were treated as black boxes. Since these studies were typically limited to small sample sizes, the test results were likely lot or manufacturer specific. In contrast, custom electronic parts, packaging and assemblies typically went through more comprehensive evaluation and qualification processes, with concomitantly higher costs.

The general approach is to evaluate, test and qualify the electronics, including packaging, at the part or assembly levels, through functional testing and long-term stress testing over the application operating conditions plus margin. In these qualifications, existing standards for determining margin or margins derived from “design-for-reliability” approaches were used.

7.9.2 NESC Guidance on Cold Electronics Qualification

The NESC guidance on cold electronics qualification for lunar missions are summarized in this section. The guidance was based on the current knowledge of the cold electronics and packaging as well as the current/best practices as well as some lessons learned (e.g., JWST) in electronics and packaging qualification. Note that, as indicated in Section 6.0, radiation tolerance is not a focus of the assessment and radiation evaluation is a separate process and not included in the

guidance. Included are qualification guidance for custom electronics, COTS/MIL electronics, electronic packaging, and passives. Qualification of batteries for lunar environments is a separate topic and not included in this assessment.

The assumption of the stress-test-driven qualification is that the failure mechanisms under the use conditions and stress conditions applied during testing are the same, and that these failure mechanisms are thermally activated and accelerated. However, beyond a certain thermal stress condition, dominant failure mechanisms can change. Therefore, a stress-test-driven standard cannot be used to qualify electronics outside of its specified application range without fully understanding the failure mechanisms.

The NESC team recommends the integration of stress-test-driven and knowledge-based approaches, with a focus on physics of failure, operational environment knowledge, and the application of principles of design-for-reliability. The stress-test-driven approach provides a uniform set of qualification stress tests, while knowledge-based reliability qualification is based on applications and physics of failures, and so there is no "pre-defined" qualification plan, and the details of the qualification may be different for different applications while the approach and methodology remain the same. The necessary caveat to this recommendation is that the effectiveness of the knowledge-based reliability qualification approach is only as good as the knowledge one has.

The top-level NESC guidance on cold electronics qualification is outlined in Figure 7.9-1.

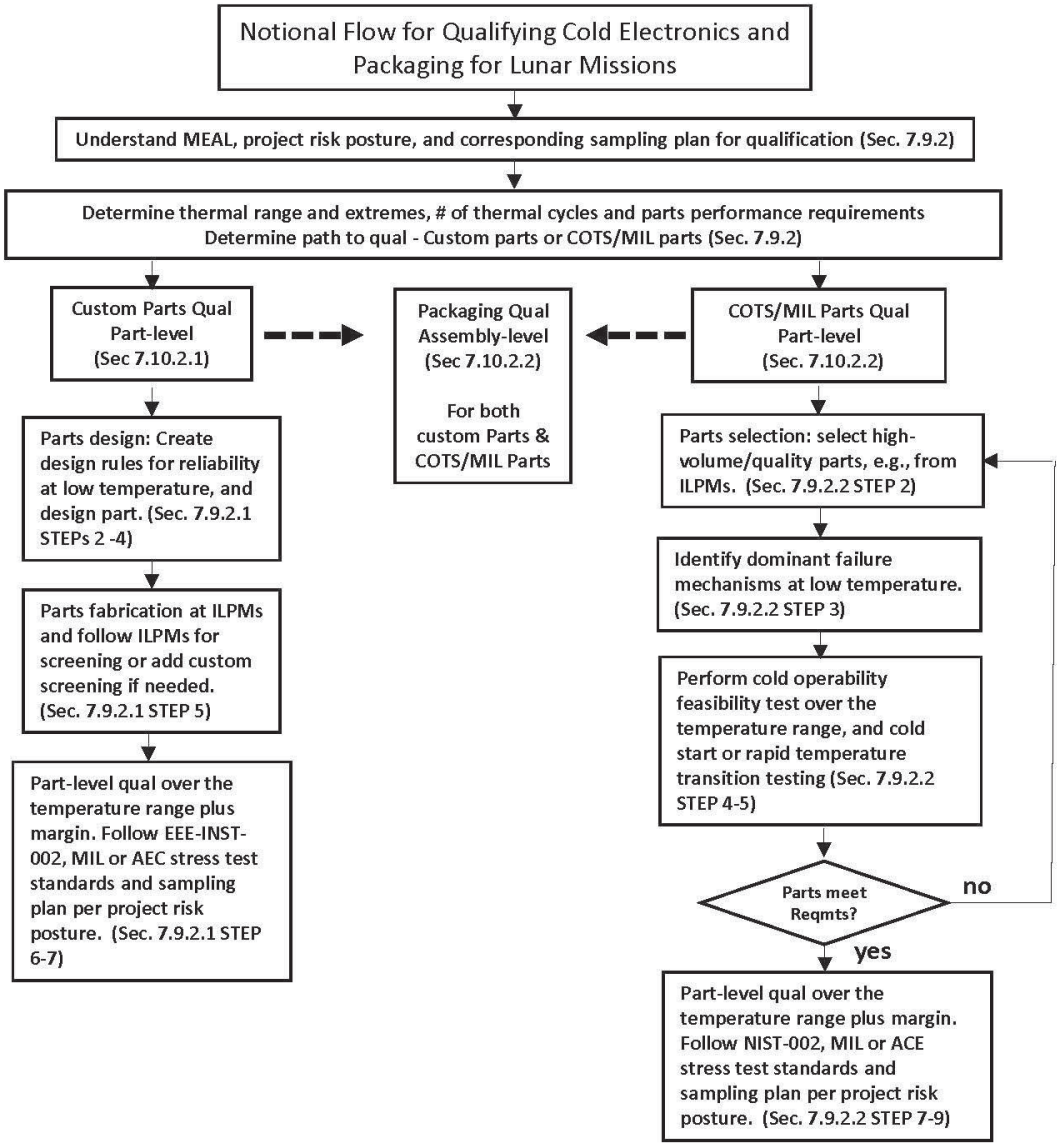

Figure 7.9-1. Top-Level NESC Guidance on Cold Electronics Qualification. Note radiation evaluation is a separate process and not included in the guidance.

7.9.2.1. Qualification for Custom Cold Semiconductor Electronics at Part-Level

Qualification of custom electronics intended to be operated beyond the thermal ranges guaranteed by the technology on which they are based, needs to be founded on the knowledge-based approach. This requires more knowledge of physics of failure mechanisms, statistic nature of the reliability testing, design of experiment, acceleration modeling, device reliability modeling, circuit reliability models, packaging reliability parameters, and part/assembly use conditions. The qualification process includes the following steps.

1. Step 1: Understand MEAL and risk posture [ref. 75] as well as associated reliability test sampling plan [ref. 76].

- Work with the project to determine thermal range and extremes, number of thermal cycles the electronics will be exposed to and thermal margin for qualification. Note that the thermal margin at the low cryo-temperature end needs to be realistic.
- Define and understand performance requirements and acceptance criteria.
- Do not limit qualification parameters especially when evaluating leading and/or new technologies.

2. Step 2: Identify potential failure mechanisms and modes for the chip and the package.
   - Select specific test structures and perform reliability testing at various temperatures and electrical bias conditions. For the package, thermal cycling and shock testing may be needed.
   - The predetermined reliability testing sampling plan in Step 1 should be followed.
   - Testing temperature range should cover the operating temperature range plus margins.
   - Acceleration factor and activation energy are to be extracted from the test data for the dominant failure mechanisms and modes over the entire temperature range.
   - Note: understanding dominant failure mechanism(s) at low temperature is the key in this Step. For example, hot carrier injection degradation in MOSFETs is significantly enhanced at low temperature due to increased carrier mobility and energy, leading to more interface trap formation and reduced transistor lifetime [ref. 77].
3. Step 3: Develop and update design rules to address the specific failure mechanisms and modes over the use condition range. Identify any additional testing necessary. For example, design rules may require transistors with larger channel length to mitigate hot carrier injection degradation at low temperature [ref. 24].
4. Step 4: Design or revise the electronic circuitry using the updated design rules.
5. Step 5: Manufacture the custom parts at a high-volume manufacturer site, preferably an Industry Leading Parts Manufacturer (ILPM) [ref. 78].
   - Follow ILPM screening process.
   - May need to perform additional screening if ILPMs are not selected, such as burn-in or utilization of a known good die (KGD) approach.
6. Step 6: Define stress tests at part-level, including bias conditions and durations, thermal cycling and shock. Stress tests should be based on expected failure mechanisms, acceleration models and use conditions.
   - The predetermined reliability testing sampling plan in Step 1 should be followed.
   - The general approach is to evaluate, test and qualify through functional testing and long-term stress testing of the part, including packaging parts or assemblies, over the application operating conditions plus thermal margin.
   - Stress tests should follow a flow like those from Mil-STD, JEDEC and/or AEC, with the temperature ranges determined by application operating condition plus a margin dependent on MEAL and project risk posture.
   - Stress tests should include additional testing identified in Step 2.
7. Step 7: Establish baseline performance from the qualification tests and analyze the test results to determine if the technology, part, or assembly meet the application requirements.
8. Step 8: Perform a risk assessment to manage and mitigate the risk, and to determine if the risk level is acceptable.

7.9.2.2 Qualification for COTS/MIL cold electronics at part-level

This section gives the delta qualification recommended for utilizing COTS/MIL in cold environments where the part or assembly has previously been qualified for general mission use (e.g., based on the historic NASA-EEE-INST-002 or its update NASA-STD-8793.11 (in finalization)). Current standard COTS/MIL qualification, as stated in INST-002, is to apply the referenced MIL-SPEC required testing to the COTS/MIL parts.

For the temperature range of -180 to +125 °C (93 K to 398 K), which covers equatorial, mid latitudes and roving broadly on the moon, screening and qualification, as outlined below, is recommended for COTS/MIL parts. While many COTS/MIL parts have been designed with large thermal margins and have been shown to be able to perform to lower than design temperatures, down to even -180 °C (93 K), there is a dearth of experience in qualifying these parts below -180 °C (93 K). Therefore, a study to explore this area and produce a guideline is recommended.

For the delta testing to mitigate the risk of operation in cold, we recommend the following:

1. Step 1: Understand MEAL, risk posture, and associated reliability test sampling plan.
    - Work with the project to determine thermal range and extremes, number of thermal cycles the electronics will be exposed to, and thermal margin for qualification. Note that the thermal margin at the low cryo-temperature end needs to be realistic.
    - Define and understand performance requirements and acceptance criteria.
    - Do not limit qualification parameters especially when evaluating leading and/or new technologies.
2. Step 2: Part selection. Review the manufacturing process and design of the part. Focus on quality control and reliability qualification through the design and manufacturing process, utilizing ILPM review process or the MIL Spec process. Also, check that the part packaging does not have known cold temperature limitations. This step is to verify that the part is well-designed and well-built with sufficient margins, and thus suitable for operation in a thermal environment beyond its specifications.
3. Step 3: Identify potential failure mechanism and modes. Do not accept intermittent problems as no trouble found.
    - Since COTS/MIL parts are already designed and built by the manufacturer, the primary source of failure mechanisms and modes is inherent and cannot be mitigated during the design and manufacturing process as would be done for custom electronics in the preceding section.
    - If no information is available from the manufacturer, alternate routes to finding key failure mechanisms and modes will need to be used, including IEEE Xplore library.
    - Where cold acceleration of failure mechanisms is indicated (e.g., silicon CMOS hot carrier injection), the resulting reduction in part lifetime needs adequate characterization and mitigation, either in the design or in specified usage (e.g., may need duty cycle limits). This analysis includes mechanical failures for the package.
    - The information gathered will also need to be augmented/verified by stress testing.
4. Step 4: Perform cold operation feasibility testing such as:
    - A slow, monitored ramp, such as 3 deg/min, to the target cold test temperature, with at least 10 K margin added to the expected operating cold temperature. Key operating parameters for the parts should be monitored for 24 hours before temperature ramp to establish a baseline, as well as during the temperature ramp.

- Upon reaching the target cold test temperature, at least 24 hours of continuous operation with stable performance at the target cold test temperature should be demonstrated on at least 3 samples.

5. Upon return to room temperature operation, at least 24 hours of stable operation at room temperature with no detectable degradation in key performance parameters should be demonstrated.
6. Step 5: Perform additional feasibility testing as determined in Step 1
   - Cold start: If, based on MEAL and design architecture, cold start is a necessary capability, this testing can be done in conjunction with Step 4 by executing at least 10 complete shutdowns, pause to ensure part is fully shut down, and restart sequences. This should be demonstrated on at least three samples.
   - Rapid temperature transition: if fast temperature change during operation is a necessary capability, such as for operation in a mobile platform, then temperature stabilization characterization is recommended to determine if the part is capable of stable operation through fast temperature transitions. Post-stress tri-temp testing and destructive physical analysis is needed, as well as visual inspection for cracks.
   - Package feasibility: Thermal shock and thermal cycling test is needed to confirm sufficient mechanical stability to support MEAL. For example, NASA-INST-002 provides standard reference package mechanical/workmanship tests which can be used as a starting point from which to extend the cold temperature limit.
7. Step 6: Analyze the results from the feasibility tests. Perform a risk assessment to manage and mitigate the risk, and to determine if the risk level is acceptable against the defined requirements.
8. Step 7: If the part is selected for use, qualification should be lot specific. COTS/MIL performance outside of the product specifications, in this case low temperature performance, rely on process margins outside of what is monitored by the manufacturer. Therefore, lot to lot variations should be expected, including radiation performance and reliability. Selection of parts with broad applicability and lot buys would allow for amortization of qualification cost.
9. Step 8: Define stress-based qualification tests, including bias conditions and durations, based on expected failure mechanisms, acceleration models and use conditions, to determine if the part meets or exceeds the application requirements.
   - The predetermined reliability test sampling plan in Step 1 should be followed.
   - Stress tests should follow those from NASA-INST-002 (extending to cold temperatures) supplemented by MIL-STD, JEDEC, AEC, and peer reviewed literature depending on MEAL and project risk posture.
   - Stress tests should include the additional testing identified in Step 1.
   - Acceleration factor and activation energy are to be extracted or confirmed by collecting sample test data for the dominant failure mechanisms and modes over the entire temperature range, including margin.
   - Package-focused stress testing such as thermal cycling and thermal shock should be included.
10. Step 9: Screening test should include tri-temp testing to the target temperature. Hot and cold burn-in should both be conducted, especially for known cold accelerated mechanisms.

7.9.2.3. Life Cycle Qualification for Cold Electronics Packaging at Assembly-Level

At the system level, assembly reliability under thermal stress depends on the reliability of its constituent elements— package, PCB (printed circuit board), and interconnects — and its global/local interfaces (attachments). Reliability then is defined by the characteristics of these three elements — package (e.g., die, substrate, solder joint, and underfill), PCB (e.g., polymer, copper (Cu), plated through hole, microvia), solder joints (e.g., via balls, columns) — together with the use conditions, the design life, and the acceptance failure probability.

For the extreme low cryo-temperature environments of lunar applications, thermomechanical modeling for life cycle projection becomes inaccurate due to continuous electronics shrinkage with the use of higher density interconnections (HDIs) and new configurations as well as the use of new materials. However, modeling could be used for parametric studies to determine their relative effects and developing an effective design of experiment (DOE). Experimentally, it is required to first establish temperature limitations with subsequent thermomechanical fatigue life adequacy for a mission. From initial evaluation and modeling, a knowledge of potential failure mechanisms could be determined and fed into the original design of the assembly and materials selection to avoid known potential premature failures during costly life cycle qualification testing. The qualification process for cold electronics packaging may include the following steps [ref. 79].

1. Step 1: Understand MEAL. For the purposes of electronic packaging, thermal life cycle refers to the temperature range and number of cycles within the MEAL requirements. The total number of cycles includes assembly and rework operations (after initial reflow or curing), ground testing, and mission thermal fluctuations (environmental and power cycling considered).
2. Step 2: Prior to testing, the following should be completed.
    - A test plan should be developed by the project with inputs from the reliability engineer. This test plan should include:
    - A number of test coupons using flight configurations and build processes.
    - An approved test facility should be identified followed by conducting a facility survey, an ESD survey, an operational safety survey and test setup.
    - A test procedure with documentation should be prepared by the project with guidance from the reliability team. The procedure should include test parameters and failures/anomalies definitions as well as frequency of data recording during test.
    - Test hardware should be mounted in the same manner as used for flight.
    - A test dry run should be performed to optimize the test parameters to meet the established requirements. The team should confirm fail-safe settings for the chamber temperature limits to protect the hardware in the event of a malfunction.
    - Pre-test functional tests of the test hardware should be performed and recorded.
3. Step 3: Thermal cycling should be performed according to the test procedure. The hardware should be exposed with agreed margin (1.5-3 times) to the number of equivalent thermal cycles to which the hardware is exposed from the time of post-fabrication to the end of mission life.
    - To mimic flight like thermal fluctuation, a maximum ramp rate of 5°C/minute or lower is appropriate for most electronics assemblies. The reliability team should work with the thermal engineer to confirm that this rate is appropriate.

- The test article should be brought to equilibrium with an additional dwell time for covering sufficient aging/creeping occurrence before ramping to the next temperature.
- For power cycling, generally, exercised it during hot dwell time.
- Temperature should be monitored at sensitive locations and logged.
- Hardware should be inspected before, several times during testing and after testing.
- Test hardware should be representative of the flight hardware, including design, attachment, materials, device types, coating, heat sinks and processes. It should include all potential failure sites and the capability to monitor the performance at such locations. Hardware can be a full flight like assembly or representative test coupons.
- Test hardware physical and mechanical inspection methods should be identified in the test plan.

One control sample should be reserved for destructive physical analysis, if possible.

4. Step 4: A test report documenting results of the assembly level thermal cycling, failure analyses, deviations, inspection reports, images, and lessons learned should be reviewed and approved by the project and reliability team.

7.10 Discussion of a Phased Evolutionary Development, Potential High-Value Technologies, and Technology Demonstration/Infusion Examples

In this section, the NESC team discusses the potential for a phased evolutionary approach to development of an ecosystem for cold capable avionics. The NESC team identifies elements that can be developed and demonstrated most readily with the most impact to the broad range of lunar missions and explores several example demonstrations and mission infusions. This report concludes with an example of a lunar rover utilizing a hybrid avionics architecture whose subsystems are derived from the developments previously described. The discussion below draws on the architectural principles outlined in section 7.3, the mission environments of 7.2, and the technologies identified in sections 7.4 through 7.8.

7.10.1 Phased Evolutionary Approach

As discussed in section 7.3, it is expensive in budgetary resources, risk, and schedule to attempt the development of a complete distributed cold capable avionics suite. A more measured approach, focusing on those elements of an avionics system that provide the most benefit for the lowest cost and risk may be a more practical approach. This would result in a series of avionics elements and subsystems that could be used to implement a series of hybrid architectures with increasing cold capable content, eventually leading to either a fully distributed architecture or an optimized hybrid avionics suite suitable for use in a broad range of platforms and missions. It should be noted that cold capable avionics, as envisioned by the NESC team, would have utility beyond the lunar surface. Other platforms and environments that would benefit include LEO/MEO/GEO orbiters; Mars landers, rovers, helicopters; Icy Moons landers, orbiters, rovers; and potentially other deep space environments and platforms for science, exploration and human habitation. Additionally, as there is no electronic ecosystem capable of reliable sustained operation below -55 °C (218 K) or of cycling through such temperature ranges, there may be other markets such as scientific instruments and quantum-based systems for these electronics. The following sections show examples of potential high-value developments (i.e., cold capable avionics elements with minimal cost/risk/schedule developments, maximal benefit to missions/platforms, and that are expected to be generally applicable to a broad range of

environments, missions, and platforms). Subsequent paragraphs discuss some potential space-based demonstrations, infusions, and procurement approaches.

7.10.2 Potential High Value Developments

In reviewing the state of the art in avionics, as delineated in sections 7.4 through 7.8, the NESC team identified the following electronic elements as being amenable to relatively rapid development and as having maximal benefit to missions.

The RF elements of an X-Band radio, RADAR, or RF Instrument transmit and receive chains. Much of this work has already been accomplished through the NASA SMD COLDTech and LuSTR projects[7]. The core circuits have been designed, tested, and validated over temperature and radiation. The primary requisite additions are the transmit chain power amplifier and the packaging. Implementation of the remaining elements and integration of these elements into an ASIC is relatively straightforward. The team believes that this is the most advanced cold capable technology and the lowest cost/shortest path to a viable product.

The RF Elements of a Phased Array Antenna for radio, RADAR or RF Instrument. The necessary advance in this technology development over just the RF receive and transmit chains in the previous paragraph is the addition of a phase shifter element and developing the actual antenna housing the Transmit/Receive Module array. Given the current state of the art in cold capable X-Band RF, this addition is relatively straightforward and minimal risk as well as relatively low cost with minimal additional schedule impact.

A final note regarding the RF elements discussed at the top of this section: while most of the work done to date in cold capable RF has been in X-Band, given this starting point, it is relatively straightforward to adapt the relevant circuits to S, Ka, Ku Bands as well. While the team does not recommend this as a first action, it should be noted that these developments are not deemed to be of high risk or cost, assuming successful development and demonstration of the X-Band system.

A Power System Hibernation Controller. The development of such a controller can leverage the analog library of elements previously funded by NASA SMD through the COLDTech and LuSTR. The underlying technology for this circuit library, which includes RF, Analog and some digital elements is a commercially available SiGe technology. Unlike the RF elements in the above paragraphs, this subsystem would require the development of a suite of analog and digital circuits as well as the use of COTS GaN drivers/switches. While some of the analog circuits have been developed and tested, additional circuits will be required. In addition, the digital circuits developed by the COLDTech program are aimed at the extreme radiation (5 MegaRad Silicon) environment of Europa orbit and not suitable for use in other environments due to tradeoffs in speed-power product, real estate footprint, and complexity of design, layout, external interface, and integration. Instead, the COTS SiGe technology upon which the cold capable RF and analog circuit library is based includes a CMOS digital library that may be suitable as is or with minimal adaptation of the design tools.

As noted above, in the Power System Hibernation Controller, the development of digital elements utilizing the available SiGe COTS library, with potentially some adjustment of the ASIC design tools (or the way in which they are used), offers an opportunity to develop digital

[7] COLDTech | Glenn Research Center | NASA, Lunar Surface Technology Research (LuSTR) - NASA

and mixed signal ASICS and Systems on Chip (SOCs). One of the most useful digital chips is an FPGA. State of the art FPGAs are extremely complex SOCs with onboard processors, working memory, Serializer Deserializer (SerDes), and thousands of programmable elements that can be configured into a very wide variety of circuits, subsystems and processors. Implementation of FPGAs of this complexity and the libraries and tools required to effectively utilize the onboard resources is a bridge too far for this exercise. However, smaller, less complex FPGAs of the type used in most spacecraft today for everything from glue logic to custom processors, is likely within the scope of a moderately funded project. The same is true for relatively small single or multi-core microcontrollers such as are used in virtually every science instrument, radio, and other spacecraft subsystem for subsystem control, self-test, automated and autonomous operations, and system interconnect interface. Any or all of these could be taken on separately and then integrated into the Power System Hibernation Controller as well as the distributed motor controller described below.

A distributed Motor Controller would be the next most complex element in this list of potential developments. A distributed motor control system utilizes small modules located at the actuators (and associated sensors). The main computing elements, power conditioning and distribution, overall subsystem control and coordination, are housed in the WEB. This development will require mixed signal ASICs, most likely implemented as an SOC combining digital bus interfaces, analog sensor interfaces, microcontroller, ADC/DAC, RDC, power & commutation control, waveform shaping, and GaN H-Bridge drivers. A module containing such an ASIC, GaN H-Bridges, ancillary discrete parts will need to be developed with appropriate packaging to withstand the thermo-mechanical environment adjacent to the actuator(s).

A bonus subsystem that would be applicable to many, if not all, platforms but might not be of the highest priority is the housekeeping sensor system. Most platforms will require hundreds to thousands of small housekeeping sensors and potentially a few very large and complex sensors. Many, if not most, of these sensors will, of necessity, reside in the external environment. The system would benefit from a reduction in required cabling between these external housekeeping sensors and the multiplicity of data collection/reduction points. Sometimes termed an REU, or "remote engineering unit," a typical REU module might manage 32 to 64 such sensors, providing power or stimulation as necessary to the sensors, collecting sensor data, digitizing, data reduction, and transmitting the data, via the spacecraft interconnect, to the C&DH subsystem. Locating these sensor interfaces, drivers, data concentrators/reducers close to the sensors minimizes cable mass, complexity, cost, risk, and EMI/C issues. Like the motor controller described above, a mixed signal ASIC would be optimum. Such an ASIC would comprise a digital bus interface, a series of sensor interfaces with associated analog mux/demux unit, ADC(s), current drivers, voltage references, and the like, but is somewhat dependent on the types of sensors utilized to meet platform health, status, and environmental awareness requirements.

Ground based demonstrations and qualification will be required for each of these cold capable elements to ensure reliable operation in the intended application as well as to gain the confidence and acceptance of the user community (i.e., the mission system designers). Qualification should be performed per Section 7.9 with the temperatures and other environmental conditions preferentially being the environments noted in Section 7.2 as this would allow immediate infusion into the most demanding of missions. Demonstrations in a "flat sat" or representative functional- simulation environment, with the cold capable elements in a thermal-vacuum chamber at representative environmental conditions would be useful in gaining the confidence of

potential users. Validation of functionality in the intended mission application and robustness to the lunar surface environment through these types of ground-based demonstrations is key to successful adoption of the technology and products.

7.10.3 Infusion Examples

In this section we describe several options for rapid infusion of products stemming from the examples of 7.10.2, above.

7.10.3.1 CLPS-Based Infusions

In these examples, the CLPS landers are targeted for technology infusions. While this may be optimal from a demonstration perspective, we also list some other potential infusion platforms that might be more readily available.

The first and perhaps simplest infusion would be the implementation of cold capable RF comm Tx/Rx chains mounted at the antenna. In addition to improved EMI/C and SNR during normal day/dusk operation, the radio and one or more instruments or payloads relevant for night operation, might be powered through the lunar night by a relatively small battery, in a super-insulated box, with trickle charge powered temp sensors and heater. The target of the night mission operations might consist of a periodic transmission of a health and status telemetry string and one or two low power instruments. Another application of RF comm would be to provide an early indication the spacecraft has survived a hibernation cycle at lunar dawn. While the spacecraft is recovering, a RF tone or simple pre-programmed message from the power controller could alert ground control that spacecraft power recovery is in process.

A follow-on infusion might be the implementation of the phased array antenna allowing electronic beam steering and multi-beam formation and eliminating the need for a gimballed/motorized antenna assembly and minimizing EMI/C and noise. If there are multiple such CLPS landers, surface or orbital assets available within line of sight, transmission/response could be to these assets as well, thus initiating the implementation of a communication network or grid.

Infusion of hibernation, consisting of waking up the system on solar array output, warming batteries to operating temperature, reconnecting the batteries to the power system, determining system health and status, activating power distribution to loads, then turning over control to the C&DH, is relatively straightforward once the hibernation controller is available.

Finally, a distributed motor controller could be infused with application to either a motor-actuated antenna or a robotic arm. In addition to improving harnessing mass, complexity, reliability, WEB insulation efficiency, a sufficiently sized battery/power system in the WEB, with just enough computing to allow the generation of motor positioning commands instrument operation deeper into the lunar night would be enabled. Any or all of these potential technology infusions could be implemented in one or more landers but given the cost/risk profiles of the CLPS program, it might be useful to consider a series of such infusions where each infusion builds on previous cold capable electronics infusions, leading to the ability to optimize a set of hybrid architecture for various platforms and missions.

7.10.3.2 Alternative Demonstration Methods

While a CLPS lander-based infusions might be optimal for many reasons, both environmental and programmatic, other vehicles might be more readily available and provide equally attractive infusion targets. LEO small sats are relatively inexpensive and boom or antenna mounted

electronics could see temperatures as low as -155 °C during the Earth-shadowed portion of a 90 min orbit. The ISS is reported to see temperatures below -180 °C in some shadowed areas. Infusions of cold capable electronics into these platforms such as ISS and commercial LEO would provide similar advantages to lunar surface missions and would also serve as confidence builders for manifesting these electronic elements into a broad range of missions.

7.10.4 Example Hybrid Rover Architecture

Finally, we discuss a hybrid avionics architecture, comprising the cold capable elements above, in addition to a traditional WEB for most of the avionics, that is suitable for use in a lunar rover mission. For this example, the rover is assumed to be powered by solar illumination (i.e., not powered by an RTG, and therefore required to hibernate during the solar night). It is also assumed that the rover is autonomous or semi-autonomous s, requiring only infrequent commanding from Earth or Lunar-based human crew and thus requiring significant onboard computing resources. The rover is, however, required to maintain frequent and high data rate communication with either Earth or Lunar base station for mission data and rover state (telemetry) monitoring. It is also assumed that this rover can implement autonomous, rapid traverse to cover a great deal of exploration over a relatively short time. The base station, meanwhile, is also assumed to be highly automated or autonomous to quickly react to exploration data and telemetry by issuing commands updating mission priorities and constraints. Mission life for this rover is 10-20 years and it is assumed that there will be brief excursions into shadowed regions (e.g., craters but not extended excursions which would require large additional energy resources).

First, we assume that most of the avionics will be housed in a typical WEB, allowing the use of state of the art non-cryogenic (e.g., COTS/MIL, computing, power conditioning and distribution, electronics). As a note, these electronics must have some minimal (20krad) TID tolerance, be SEL immune to the GCR background (e.g., to SEL = 75), have a nominal 20-year life under the relatively benign conditions of the WEB, and provide a high degree of SEE immunity or the equivalent real time operational fault tolerance capability.

The following are the recommended cold operational elements to be utilized for maximal benefit to the rover mission:

1. Distributed motor control modules that provide motor control and position sensor interface at the motor. For this subsystem, the main computing capabilities for controlling the large number of motors and other actuators can be in the WEB, with only the motor winding power modulation and commutation electronics, sensor interfaces and digitization electronics, and digital communication bus interfaces to the WEB being cold operational and located at the motors. This would require the development of single custom ASIC in SiGe containing most of the required circuitry and selection or development of several discrete parts such as final motor GaN H-Bridge drivers SiGe pre-drivers, resistors, capacitors, substrate and housing. In addition, a position sensor such as resolver or Hall Effect Encoder, brake position sensors, and similar elements are needed for any such platform. Development of these elements minimize the WEB thermal insulation breach due to copper wiring of the harness that would otherwise be required to bring hundreds of wires through the WEB walls. It also minimizes the EMI due to large current pulses being transmitted from within the WEB, adjacent to other digital, RF and analog circuitry, across 10s of meter of harness to the motors. Finally, it minimizes EMI and the degradation of various actuator-associated small

signals that would otherwise be transmitted over 10s of meters of wire to the WEB interior for eventual digitization and processing.

2. RF communication system receiver low noise amplifier and transmitter high power amplifier (i.e., RF receive and transmit chains). Similar to the motor controller subsystem above, these two electronic elements, if placed at the antenna, instead of in the WEB, minimize noise and EMI, while maximizing sensitivity. They would be implemented as custom ASICs in SiGe and can be S, X, K, or Ku band as required for the mission. Similar to the SiGe ASIC in the motor control subsystem, existing work done by COLDTech and LuSTR can be leveraged for this development. If RADAR is required for the mission, these elements are also applicable to the RADAR instrument. In addition, the low noise amplifier may also be applicable to other sensors and exploration or scientific instruments.
3. RF phase shifters. Phase shifters are used in an antenna mounted array to provide muti-beam and beam-steering capabilities. As with the ASICs above, they are implemented in SiGe and leverage the technology developed under COLDTech and LuSTR. This type of antenna (a.k.a. phased array antenna) is applicable to both communication and RADAR subsystems and provides electrical (versus mechanical) pointing of the RF signal as well as the ability to generate multiple RF signals from a single antenna. For many missions of this type, this phased array capability may be greatly enhancing or enabling. Having the elements mounted at the antenna is the only feasible approach to implementing a phased array.
4. Power Hibernation and Recovery. This includes digital main bus control, power conditioning and distribution, cold survivable batteries, battery management, and solar array regulation. Cold operational batteries are not expected to be available within the 5 to 10-year time horizon of this mission, thus hibernation through the lunar night will be required. For this, we will require GaN circuitry for power management and control, a SiGe microcontroller to manage the power system and cold survivable Li batteries. All of these elements are readily developed by leveraging existing work in SiGe, GaN and Li ion batteries. The hibernation power subsystem will provide the capability for the rover to autonomously hibernate at sunset, awake at sunrise, thermally condition its batteries, initialize and continue on its mission lunar day after lunar day for the 10 to 20-year mission life.
5. Identification of required instruments for this mission is beyond the scope of this section but it is likely that drilling, sampling, chemical composition analysis and the like would be needed. The cold operational elements in 1-4 (e.g., motor control, sensor interface, LNA) above should provide a basis for these capabilities as well. While additional, SiGe and GaN ASICs may be required, development of these elements should be relatively straightforward starting from the circuit elements above.

In summary, this example shows an evolutionary hybrid platform for lunar surface operations leveraging existing developments of cold operational technologies and circuits as well as high performance rad tolerant COTS that is relatively affordable, readily available, and which paves the way to future fully cold operational systems.

7.11 Technology Interchange Meeting

On April 30 through May 1, 2025, a Technology Interchange Meeting (TIM) was held at Caltech to present a preliminary version of Sections 7.1 through 7.9 to the industrial, academic and NASA community and to solicit comments and feedback on the needs, state of the art and gap

analysis in each of the technical areas. TIM attendance was available both in person at Caltech and virtually via Webex. The TIM was announced on the NESC website. The team also contacted known organizations that might be interested in the assessment. Upon registration and selection of in-person or virtual attendance, the registered individuals were provided with a copy of the preliminary version of the assessment report. Over 110 people 43 industry, academia, and government agencies joined the TIM.

The first day's agenda consisted of an introduction explaining the goals and overview of the assessment (i.e., Section 7.1), followed by a summary of each of Sections 7.2 through 7.9 presented by that section's principal author (see agenda in Appendix F). Summaries were brief as it was assumed that attendees had read the preliminary report. At the end of each section summary, the attendees were asked to comment, question or otherwise respond to what had been presented. In the case of Section 7.3, for example, one of the attendees commented on MUSES-CN, while another commented on the CLPS Cold Arm. As another example, *industry is looking for guidance on cryogenic testing and an open website that can be used to share the cryogenic test data from industry and government is strongly desired* ***[F-18]***. Productive discussion was held on each section with both clarification from authors and feedback from attendees.

The second day's agenda consisted of another round of section-by-section questions and answers, comments, and discussion, followed by an opportunity for attendees to present their organization's interests, technologies, concerns, and general comments. Attendees, upon registration had been given an opportunity to sign up for 15-minute time slots for these presentations and all slots were allotted. This provided opportunities for those organizations working on, or planning to work on, cold capable technologies and products to hear about needs from organizations that were interested in building cold capable systems. It also provided further opportunity for industry and academia to provide the assessment team with broad ranging feedback, comments, and critique beyond the specific technical areas in the preliminary report.

Overall, attendance was good, as was participation from both in person and remote attendees. The feedback and comments were then folded into the final report.

Appendix F comprises the agenda and the presentations from the NESC assessment team.

8.0 Findings, Observations, and NESC Recommendations

8.1 Findings

Findings are provided below:

F-1. There is insufficient measured lunar surface thermal data spatial resolution and no universal generic thermal model that can be used by early mission system and avionics developers to determine the thermal environmental extremes over lunar surface regions for platform or electronics outside of the WEB. The community generally uses the lunar regolith surface temperature in the regions of interest and assumes these are the worst-case temperatures seen by the electronics.

F-2. Accurately identifying worst-case and actual thermal environments requires knowledge of the specific mission location, platform configuration, electronics location and orientation within the platform, and mission operations.

F-3. STMD ranked "survive and operate through the lunar night" as the number one "shortfall" in capability. The lunar power hibernation is a near-term approach that employs cold electronics to meet the shortfall.

F-4. The current architectural approach for avionics required to operate in extremely cold environments (e.g., Mars or Deep Space) is to place the electronics in a WEB and cable out to actuators and sensors that are custom designs built for these extreme environments.

F-5. No cold capable electronics architectures that are generally applicable to the lunar surface environment have been implemented or even studied to the degree necessary to initiate the detailed design of such an architecture.

F-6. From an architecture implementation perspective, given the lack of cold capable electronics technology maturation, it is impractical to immediately implement a fully cold capable avionics architecture for lunar surface systems.

F-7. When COTS/MIL parts are used outside of their datasheet specified thermal range, reliability and stability are not ensured and the lot-to-lot variation in operational parameters are expected to be significantly higher than in normal operation.

F-8. There is a lack of cold start data in the literature. Most of the cold-capability studies are continuous operation studies where temperature is gradually lowered until abnormal behavior is observed. Cold start test data would be critical to eliminate self-heating effects.

F-9. Under NASA COLDTech and LuSTR, several analog, digital and RF circuits were developed using the commercially available Global Foundries 90 nm SiGe process technology. A sparse library of RF, analog and digital circuits were developed and demonstrated to be radiation hard to 5MRad and capable of operating down to -180 °C (93 K).

F-10. The library of 90 nm SiGe analog, digital, and RF circuits for cold space applications developed under the COLDTech and LuSTR projects does not address all capabilities necessary to support the cold and wide cold temperature range circuit functions needed for lunar applications.

F-11. Resistors, capacitors, and inductors suitable for cryo-temperature operations may be available as COTS/MIL parts but require further characterization tests at cryo-temperatures.

a. Resistors with a low TCR (temperature coefficient of resistance) such as Wire-wound and Metal Film resistors have low sensitivity to temperatures and are available commercially.

b. Solid electrolytes capacitors can tolerate cryo-temperatures but can experience substantial parameter shifts.

c. Several capacitors with low sensitivity to temperature are available commercially.

d. Radiation Crosslinked Acrylate Monomer dielectric capacitors have been tested down to -269 °C (4 K). These appear suited for cryo-temperature applications but may need to be custom manufactured.

e. Ferrite cores generally exhibit large shifts in inductance and not well suited to cryo-temperatures applications.

f. Nanocrystalline magnetic cores are well suited for inductors used in power converter applications and have been evaluated down to -196 °C (77 K) with only some loss in linearity.

F-12. Limited published studies exist with less than 100 thermal cycles over wide cold temperature ranges (minimum temperature below -120 °C and delta of 205 °C/K) and for a limited number of packaging solutions, generally not including COTS, high speed processing, high frequency or high-density solutions.

F-13. Accurate material properties, such as CTE, strength and modulus, for the relevant electronic packaging elements over the entire cold and wide temperature range as well as processing guidelines for these materials are critical and not readily available.

F-14. GaN High Electron Mobility Transistors HEMT have demonstrated that they are stable across a wide temperature range down to -223 °C (50 K).

F-15. Li-ion 18650 cells should be tested in a vacuum environment, since it assures that cells maintain a positive internal pressure and prevents external gas ingestion and eliminates risk of over-pressurization when returned to normal temperatures.

F-16. Li-ion cells, specifically18650 cells, were demonstrated to tolerate freeze/thaw cycles down to -223 °C (50 K) and recover their voltage and charge capacity when warmed back to room temperature. Similar small format cells (e.g., 20700, 21700, 22700 etc.) manufactured by similar processes may also tolerate the freeze/thaw process but will require cryo-temperature testing

F-17. Energy storage:

a. Li-ion batteries can be discharged as low as -60 to -90 °C (213 K to 183 K). At low rates, however, they cannot be charged at these temperatures due to issues with Li plating. Li-ion cells cannot be discharged at high rates (greater than C/50) at temperature < -40 °C (233 K).

b. The effects of low temperature electrical and thermal cycling on battery life are not well understood. There is a paucity of data and inadequate models for evaluation of the effects of plating on lifetime as well as the mechanical effects of multiple freeze-thaw cycles.

c. Traditional intercalation electrodes based on graphite and used for most current Li-ion cells limit the performance of cells. Alternatives, including conversion electrodes, based on lithium titanate, silicon, lithium metal or on electrochemically active liquid systems, offer approaches for operating at < -80 °C (193 K) and have been recently studied but are at TRL < 3 for use in space applications.

d. Electrochemical methods for energy storage are unlikely to support adequate energy storage at cryo- temperature due to fundamental limitations with thermally activated processes.

e. Electrochemical methods for energy storage are unlikely to support adequate energy storage at cryo- temperature due to fundamental limitations with thermally activated processes.

F-18. No existing standards support the qualification of the electronics and packaging for the lunar environment temperature range of -233 °C to +125 °C (40 to 398 K).

F-19. The existing processes for parts and assembly qualification approach and processes can be adapted for the extreme cold environment and wide temperature ranges of the lunar surface environment in a relatively straightforward manner with special attention to qualification thermal margin for the low temperature end.

F-20. Industry is looking for guidance on cryogenic testing and an open website that can be used to share the cryogenic test data from industry and government is strongly desired.

8.2 Observations

O-1. Passives:

a. Thermistors (PTC, NTC) may be useful as temperature compensation devices to stabilize analog circuits over a wide temperature range.

b. Thermistors for cryo-temperature applications are available commercially.

c. Air gap capacitors are insensitive to temperature but have low capacitance compared to dielectric caps of similar size and weight.

d. Generally, electrolytic capacitors are not suited to cryo-temperature operation because the electrolytes will freeze.

e. Expect capacitors suited to cryo-temperature operations to have low capacitance compared to electrolytic caps.

f. For cryo-temperature applications, air core inductors are largely insensitive to temperature however they have relatively low inductance, and the open magnetic fields can interact with nearby materials.

g. Compared to air core inductors, solid cored inductors provide greater inductance and greater field containment; however, core material properties may be sensitive to temperature.

8.3 NESC Recommendations

The following NESC recommendations are directed to NASA STMD, NASA SMD, Planetary Exploration Science Technology Office (PESTO), NASA Exploration Systems Mission Directorate (ESDMD), NEPP, and program or projects needed to survive and operate under lunar environments.

R-1. Recommend using the following generally accepted regolith surface temperatures *as the starting point* during early mission and system development when Mission, Environment, Application, and Lifetime (MEAL) specifications are not available, and engage thermal subject matter experts (e.g., the NASA Lunar and Mars Environments Analysis Team (LUMENATE)) as early as possible in the process to help define the expected temperature extremes to be experienced by the electronics outside of a WEB. ***(F-1, 2)***

- Permanently Stationed Platforms:
  - Equatorial -180 to +125 °C (93 to 398 K)
  - Mid Latitudes -145 to +80 °C (128 to 353 K)
  - Poles -223 to -193 °C (50 to 80 K)
  - PSR -233 °C (40 K) (Not absolute worst cases, but a good assumption for the 80% case)
- Mobile Platforms:
  - Transport in/out of PSR -233 to -40 °C (40 to 233 K)
  - Roving broadly, -145 to +120 °C (128 to 393 K)

R-2. Recommend lunar surface mission projects, and parts, subsystem, and system developers follow qualification guidance on cold electronics and packaging, outlined and described in Section 7.9. ***(F-18, 19)***

R-3. Recommend SMD/STMD implement an evolutionary strategy to develop a cold capable electronics ecosystem that supports hybrid and hibernation avionics architectures**.** A phased evolutionary approach with identified development of high value technologies and demonstration/infusion examples are outlined in Section 7.10. ***(F-3, 4, 5, 6, 9, 10)***

R-3.1 Recommend SMD/STMD develop Design Reference Missions (DRMs) for the class of missions expected to be developed in the next 5-10 years, and that these DRMs assume architectures be of the hybrid variety, with specific emphasis on maximizing the currently available cold capable electronic parts and assemblies. ***(F-4, 5, 6)***

R-4. Recommend STMD/SMD develop cold electronic elements for representative mission environments and plan for mission infusion opportunities. ***(F-3, 4, 5, 6, 9, 10)***

R-4.1. Recommend STMD/SMD expand the digital, analog, power, and RF library of SiGe circuit libraries, models and associated packaging to enable the development of all types of cold capable avionics ASICs. ***(F-8, 9)***

R-4.2. Recommend STMD/SMD develop freeze/thaw tolerant Li-ion batteries based on small cylindrical format cells (i.e., 18650) with cold electronics to manage the thermal recovery from lunar night hibernation for future lunar mission. ***(F-14, 15, 16)***

R-4.3. Recommend STMD/SMD develop a lunar power hibernation and recovery architecture that integrates solar arrays, cold electronic main bus controls, with cold

tolerant Li-ion batteries capable of surviving the lunar night and recovering at lunar dawn. ***(F-3, 14, 15, 16)***

R-4.4. Recommend STMD/SMD work on advancing the TRL of cells capable of lunar cold and wide temperature performance to a sufficient level testing under flight-like conditions. ***(F-17)***

R-5. Recommend NEPP:

R-5.1 Develop qualification standard for COTS/MIL and custom cold electronics and packaging technologies down to 1) -233 °C (40 K) and 2) -180 °C to +125 °C (93 to 398 K) temperature ranges. ***(F-18, 19)***

R-5.2 Collect and host cryogenic testing data on electronics and packaging on the NEPP website. ***(F-20)***

R-5.3 Evaluate and test commonly used COTS/MIL parts, including GaN HEMT parts, for lunar missions as part of the PEAL program. ***(F-7, 8, 11, 14)***

R-5.4 Develop packaging design and processing guidelines for cold and wide temperature range electronics, addressing the gaps described and outlined in Section 7.7.2. ***(F-12, 13)***

R-5.5 Develop packaging implementation guidelines with test verification for COTS component package selection based on package type and size, temperature regime, number of thermal cycles and package materials outlined in Section 7.7.2. to assist parts selection and next level (assembly, board) design. ***(F-12, 13)***

9.0 Alternate Technical Opinion(s)

No alternate technical opinions were identified during the course of this assessment by the NESC assessment team or the NESC Review Board (NRB).

10.0 Other Deliverables

No unique hardware, software, or data packages, other than those contained in this report, were disseminated to other parties outside this assessment.

11.0 Recommendations for the NASA Lessons Learned Database

No recommendations for NASA lessons learned were identified as a result of this assessment.

12.0 Recommendations for NASA Standards, Specifications, Handbooks, and Procedures

Refer to R-5.1 Develop qualification standard for COTS/MIL and custom cold electronics and packaging technologies down to 1) -233 °C (40 K) and 2) -180 °C to +125 °C (193 to 398 K) temperature ranges. ***(F-18, 19)***

13.0 Definition of Terms

Finding	A relevant factual conclusion and/or issue that is within the assessment scope and that the team has rigorously based on data from their

	independent analyses, tests, inspections, and/or reviews of technical documentation.
Observation	A noteworthy fact, issue, and/or risk, which is not directly within the assessment scope, but could generate a separate issue or concern if not addressed. Alternatively, an observation can be a positive acknowledgement of a Center/Program/Project/Organization's operational structure, tools, and/or support.
Problem	The subject of the independent technical assessment.
Recommendation	A proposed measurable stakeholder action directly supported by specific Finding(s) and/or Observation(s) that will correct or mitigate an identified issue or risk.

14.0 Acronyms

°C	Degrees Celsius
AEC	Automotive Electronics Council
APL	Applied Physics Laboratory
ASIC	Application Specific Integrated Circuit
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BJT	Bipolar Junction Transistor
BMS	Battery Management System
CLPS	Commercial Lunar Payload Services
CMOS	Complementary Metal Oxide Semiconductor
COTS	Commercial Off-The-Shelf
CTE	Coefficient of Thermal Expansion
DC	Direct Current
EEE	Electrical, Electronic, and Electromechanical
EMI	Electromagnetic Interference
ESDMD	Exploration Systems Mission Directorate
FDSOI	Fully Depleted Silicon on Insulator
FET	Field Effect Transistors
FPA	Focal Plane Arrays
FPGA	Field Programmable Gate Arrays
GEO	Geosynchronous Orbit
GRC	Glenn Research Center
HBT	Heterojunction Bipolar Transistors
HCI	Hot Carrier Injection
HEMT	High Electron Mobility Transistors
HLS	Human Landing System
IC	Integrated Circuits
In	Indium
IR	Infra-Red
ISRO	Indian Space Research Organization
ISRU	In Situ Resource Utilization
JEDEC	Joint Electron Device Engineering Council
JPL	Jet Propulsion Lab

K	Kelvin
KGD	Known Good Die
krad	One Thousand Rad
LC	Inductor-Capacitors
LNA	Low Noise Amplifier
LRC	Inductive, Resistive, Capacitive
LSII	Lunar Surface Innovative Initiative
MBC	Main Bus Controller
MEAL	Mission, Environment, Application, and Lifetime
MER	Mars Exploration Rover
MHz	Megahertz
MIL	Military
µm	Micrometer
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOV	Metal-Oxide Varistor
MP	Methyl Propionate
MPPT	Max Power Point Tracking
MSL	Mars Science Laboratory
NEPP	NASA Electronic Parts Program
NESC	NASA Engineering and Safety Center
nm	Nanometer
NP0	Negative-Positive-Zero
NTC	Negative Temperature Coefficient
PbSn	Lead-Tin
PESTO	Planetary Exploration Science Technology Office
PPS	Polyphenylene Sulfide
PSR	Permanently Shadowed Region
PTC	Positive Temperature Coefficient
PV	Photovoltaic
PWM	Pulse Width Modulation
RC	Resistor-Capacitor
RF	Radio Frequency
RL	Resistor-Inductor
ROI	Return on Investment
Si	Silicon
SiGe	Silicon Germanium
SMD	Science Mission Directorate
SOC	System on Chips
SOI	Silicon on Insulator
STMD	Space Technology Mission Directorate
TCR	Temperature Coefficient of Resistance
TCRE	Thermal cycle Resistance Electronics
TID	Total Ionizing Dose
TRL	Technology Level
TRL3	Technology Level 3
TVS	Transient Voltage Suppression

WEB	Warm Electronics Box
ZnO	Zinc Oxide

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