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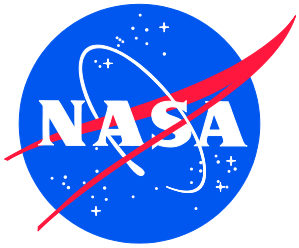

Cold Electronics for Lunar Missions

Appendices

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August 2025

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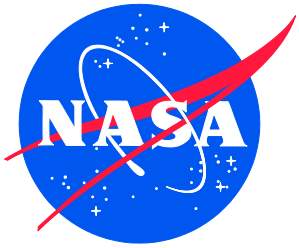

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NASA Engineering and Safety Center
Technical Assessment Report

Cold Electronics for Lunar Missions
Volume 2 (Appendices)

TI-23-01873

NESC Lead, George Jackson

Technical Co-Lead, Yuan Chen

Technical Co-Lead, Raphael Some

July 17, 2025

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Appendix A: Assessment on Cold Electronics for Lunar Missions

APL LSII SI Deliverable

JOHNS HOPKINS APPLIED PHYSICS LABORATORY

STUDY REPORT:

Assessment on Cold Electronics for Lunar Missions

Date: March 11, 2025

Version 1.0

Authors: Milena Bobea Graziano, Brian Schratz, Wesley Fuhrman, Lindsey Tolis, Sean Young, Jacob Gehrett, Andrew Gerger, Samalis Santini de León, and Jason Arcido

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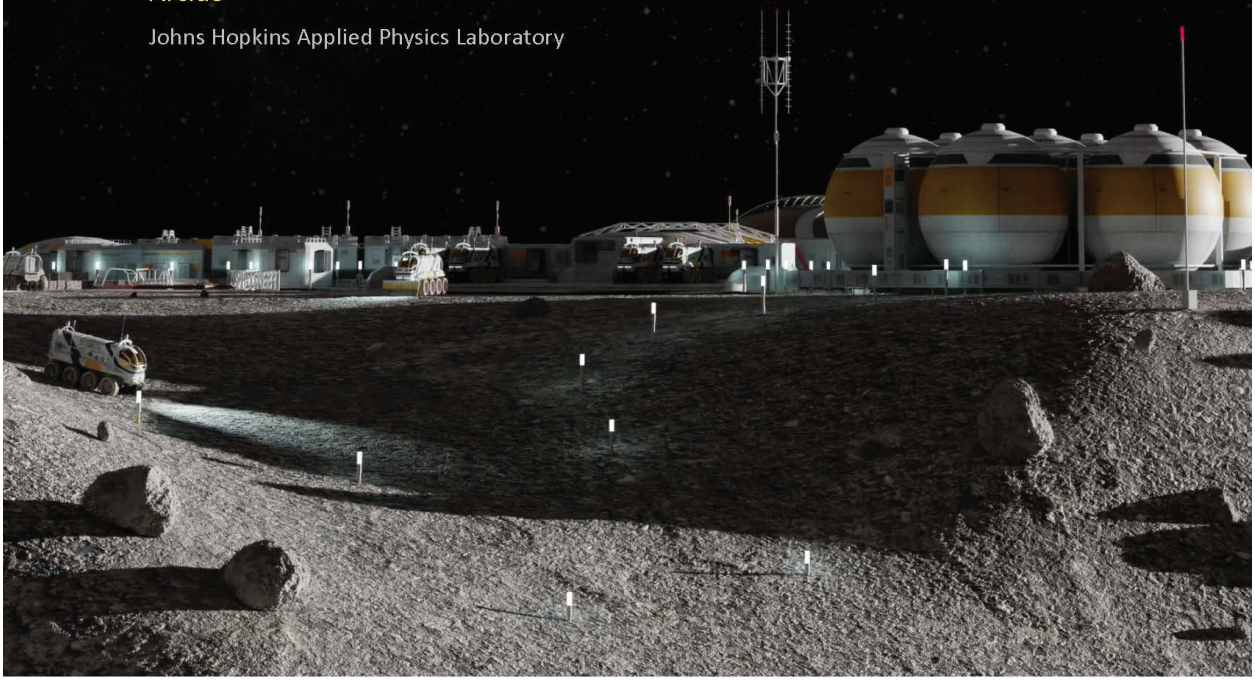

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INTRODUCTION

Extreme thermal environment electronics represent a subset of technologies that are engineered to withstand and/or operate at temperatures either above or below the common commercial and/or military standard specification temperature ranges, such as -55°C to +125°C for electrical connectors [1, 2]. For Moon and Mars surface exploration, it is operation at the extreme cold temperature range that would be desirable to secure the survival, function, and long life of landers, payloads, instruments, and similar systems. In fact, for very specific mission objectives and/or applications, the development of space-grade, cryo-operable electronics would be enabling – it would reduce or eliminate the need for active heating systems, extend mission durations, reduce energy consumption and mass, simplify system designs, and enable operations at very harsh locations, such as the permanently shadowed regions (PSRs). However, the development of cryo-operable electronics is likely to require significant investments as these technologies will demand modifications to standard materials, new manufacturing processes, complex higher-assembly integration, and extensive testing and qualification programs.

NASA's Engineering and Safety Center (NESC) has assessed how cold electronics can align with broader agency gaps and strategic priorities. This report assesses thermal challenges, necessary electronics, performance risks, and system-level trade-offs to define a strategic development approach.

ELECTRONICS FOR LUNAR ENVIRONMENTS

A wide range of technologies are demanded for the successful development of lunar surface infrastructure capabilities, such as [3]:

- Surface power
- In-situ resource utilization (ISRU)
- Excavation
- Construction
- Cross-cutting capabilities, e.g. dust mitigation, extreme access, interoperability, and extreme environments

These applications demand survival and operation in a wide range of extreme thermal environments induced by:

- Solar irradiation (daytime heating)
- Lack of sunlight (nighttime)
- Illumination conditions due to topography and/or surface assets, e.g. lander shadows and permanently shadowed regions (PSRs)
- Cryogenic fluid environments

Lunar Surface Temperatures

The orbital period of the Moon around the Earth is 27.3 day, but as the Moon and the Earth are changing their positions with respect to the Sun, it actually takes 29 days to observe a full lunar cycle. This results in a lunar equatorial region that is illuminated for approximately 354 hours, followed by approximately 354 hours of continuous darkness. Moreover, the Moon has a spin axis that is inclined 1.5 degrees from the normal to the plane of the Moon's path around the Sun [4] . This geometry allows for dramatic thermal and illumination conditions at the poles that can vary according to the season, location, and local topography [5]. Consequently, the Moon's surface

has extreme temperatures between day and night, ranging in average temperatures from -178°C to +124°C at the equator and -223°C to -73°C in the polar regions (very cold extremes are at PSRs) [6, 7]. Table 1 summarizes some literature reports for different lunar regions.

Table 1. Average lunar surface temperatures for various regions, as reported in literature.

Lunar Region	Minimum Temperature	Maximum Temperature
Equator	-130°C [8]; -179°C [6]	+120°C [6, 8]
Polar Regions (Poleward of 85°)	-250°C [9], -223°C [6]	65.85°C [9], -71°C [6]
Central Permanently Shadowed Regions (PSRs)		
Faustini	-243°C [10]	-203°C [10]
Haworth	-253°C [10]	-228°C [10]

Some other notes on the lunar surface temperatures:

- Due to the lack of atmosphere, the lunar surface temperature is primarily determined by the effective solar irradiance, which is closely related to latitude and solar incidence angle [11].
- Minimum temperatures occur prior to local sunrise and are dependent on the thermophysical properties of the lunar regolith and near-surface structure [6].
- In the equator, the differences between the nearside and farside temperatures are not significant (determined by solar irradiation), and show the same variation between maximum and minimum extremes [11]. According to D. Zhang et al., "*because the lunar farside is not affected by earthshine, the night temperature is about 0.5 K lower than that at the lunar nearside*" [11].
- According to J.-P. Williams et al., "*temperatures between noon and midnight at the equator vary by ~290 K while at 85° latitude, the temperature variation is reduced to ~120 K*" [6].
- The coldest regions of the Moon are on the floors of large impact craters at the poles (PSRs), whose main heat source is emitted infrared radiation from distant interior sunlit crater walls (reason why thermal cycling on the PSRs has a significant seasonal component) [10, 12].
- Temperatures at PSRs are very heterogeneous; the temperatures presented on the table are for the extreme cold areas for these two crater examples [10].

Temperature Variations Due to Illumination

Like with the Apollo program, a lot of recent lunar exploration missions have experienced operational and design constraints due to the thermal and illumination conditions on the Moon [13]. Lunar surface activities are often limited to the early lunar morning and late lunar afternoon, with no planned extensions beyond the 14-Earth-day lunar day [13]. However, even during the lunar day, there are risks to visibility and hardware stability due to terrain-induced and hardware-produced shadows. Depending on the time of the day, nearby topographical features, and lunar surface system or extravehicular activities (EVA), these shadows can last several hours or be transient throughout the lunar day, leading to dramatic changes in temperature and more thermal cycles than those expected from the natural lunar day-to-night transitions. The thermal inertia of the regolith is so low that even brief shadows can result in near nighttime temperatures adjacent to otherwise illuminated terrain [14].

Similarly, illumination in the lunar south pole is highly dependent on the local topography [15, 16]. Rapid change in illumination may be induced by topography that is well below the resolution of current digital elevation maps [17]. Furthermore, surface illumination maps are difficult to use directly in validation and verification (V&V) owing to the shallow angle of illumination, which can be less than the size of the solar disc. Regions of highest interest in the lunar south pole region are extremely dependent on illumination for both for mission-enabling solar power and/or thermal systems and for science experiments to be conducted at adjacent shadowed regions. Specific details of landing sites drive substantial changes to system design, concept of operations (CONOPS), and thermal requirements.

Elements with significant stand-off distances, such as vertical solar array technologies (VSATs) can improve on illumination profiles during periods when the solar angle is especially low, but will have to withstand portions of their system in starkly varying illumination, with implications to thermal management.

Translation to Hardware and Electronics

Literature reports on remote sensing of lunar regolith temperatures is extensive – but how do these translate to hardware temperatures for systems that will be on the Moon? Several considerations for thermal modeling are presented in the NASA HLS-UG-001 Human Landing System Lunar Thermal Analysis Guidebook, including the following [18]:

- Radiative heat sources, such as direct solar insolation, sunlight reflections, and emitted infrared radiation
- Conduction heat sources, such as surface assets and subsurface heat flow
- Thermophysical properties of the lunar regolith, such as its composition and low thermal conductivity
- Local geomorphology and topography, affecting solar visibility, duration and length of shadows, and reduction of visible sky to radiate heat into (very important for polar craters)
- Thermophysical properties of the lunar surface system in question

Thermal modeling can begin with simple geometric models of a lunar system, with little to no terrain features, and be matured as the design of the system is progressed and the target location is defined. Initial conditions of the lunar surface and subsurface layers can be determined by running cyclic steady state models (assume surface and subsurface temperatures are the same) [18]. This works very well for locations with little seasonal variation, such as the Moon's equator, where the initial conditions can be defined with respect to the Moon's diurnal cycle and the cyclic steady state could be reached within a reasonable modeling timeframe [18]. However, for polar surface regions, accurate thermal models can get very cumbersome and time-expensive. For this section, we leverage some of the reported hardware temperatures in lunar landed systems to aid our understanding on how measured lunar regolith temperatures translate to system design needs.

CHANG'E-4

Chang'E-4 (CE-4) landed at the farside of the Moon, at the eastern floor of the Von Karman crater [19]. This lander had several temperature sensors that recorded the thermal profile of the lander at specific locations, both contacting and non-contacting the lunar floor [19]. The negative temperature coefficient (NTC) resistor locations and recorded physical temperatures are listed in Table 2.

Table 2. Thermistor sensor temperatures recorded on the CE-4 lunar lander.

Sensor ID	Location	Min. Recorded Temperature	Max. Recorded Temperature
T1	Under One of the Rover Transfer Mechanism Ends (Metallic Substrate), Touching the Lunar Regolith at ~3 mm Max. Depth	~78 K (-195.15°C)	~300 K (26.85°C)
T2	Under One of the Rover Transfer Mechanism Ends (Metallic Substrate), Touching the Lunar Regolith at ~3.6 mm Max. Depth		
T3	Under One of the Rover Transfer Mechanism Ends (Metallic Substrate), Touching the Lunar Regolith at ~2 mm Max. Depth		
T4	Under One of the Rover Transfer Mechanism Ends (Metallic Substrate), Touching the Lunar Regolith at ~2 mm Max. Depth		
T5	On the Lander Side Panel, Not Touching the Lunar Regolith	~110 K (-163.15°C)	~250 K (-23.15°C)
T6	On One of the Cushioning Mechanism, Not Touching the Lunar Regolith		
T7	On One of the Lander Footpads, Not Touching the Lunar Regolith		

Some observations on hardware:

- Maximum daytime temperatures measured by the CE-4 sensors were around +27°C, lower than that predicted by Diviner; this can be attributed to shading on the sensors by the lander [19, 20].
- The nighttime temperatures measured by the CE-4 sensors are higher than those recorded by Diviner, likely due to thermal heating from the lander (which could have also affected the transfer mechanism) [19].
- Deeper embedded sensors or those covered by lunar dust recorded different physical temperatures than those just lying on the lunar surface (effect of direct heat conduction between the mechanism and the lunar regolith) [19].
- According to Y. Liu et al., "*even during the lunar day, substantial temperature disparities exist between sunny and shaded areas. Consequently, instruments aboard the lander are inevitably affected by this thermal environment*" [20].
- With a thermal management system, the operational thermal ranges for instruments on the CE-4 rover was -40°C to +50°C, while camera photodetectors were expected to be below +30°C [20].

CHANG'E-5

Chang'E-5 (CE-5) landed on the Moon on December 1, 2020 at the youngest basaltic unit to the northeast of the Mons Rümker in the Oceanus Procellarum [20]. The landing time was close to the lunar noon, and the landing area was fully illuminated [20]. The CE-5 lander had five temperature sensors mounted on the auxiliary pillars of the lander [20]. Which the exception of the sensor Number 3 (installed on the body of the auxiliary pillars), the sensors Number 1, 2, 3, and 5 were on the separation nuts at the junction where the auxiliary pillars connect to the body of the lander [20]. Some observations reported in literature:

- Sensor 4 was on the southern face of the lander and on the sunny side; it recorded the most rapid and highest temperature changes, with recorded temperature range of -1°C to +97°C [20].
- Sensors 1 and 3 (shaded side) recorded a stabilized temperature range approximately between -27°C and +12°C, and -18°C to +15°C, respectively [20].
- Sensors placed on the eastern (number 2) and western (number 5) sides of the lander (sunny side) experienced temperature variations approximately between -13°C to +56°C, and -16°C to +72°C, respectively [20].

ALIGNMENT WITH NASA'S TECHNOLOGY GAPS

Science Technology Mission Directorate (STMD) Civil Space Shortfalls

The need for electronics and associated components that can either survive or operate in extreme cold temperatures was evaluated against technology gaps identified in the STMD Civil Space Shortfalls [21, 22]. Select examples include:

1552	Extreme Environment Avionics
1597	Power for Non-Solar-Illuminated Small Systems
1545	Robotic Actuation, Subsystem Components, and System Architectures for Long-Duration and Extreme Environment Operation
792	In-space and On-Surface, Transfer of Cryogenic Fluids
498	Broad and dependable supply chain for space-qualified robotic hardware, electronics, and associated software
1595	Energy Storage to Enable Robust and Long Duration Operations on Moon and Mars

Throughout this report, *mission-enabling technologies* are those that are essential for mission success, providing fundamental capabilities without which the mission cannot be accomplished. Mission-enhancing technologies improve upon the current state of the art, offering increased efficiency, reliability, performance, or other benefits that enhance mission effectiveness but are not strictly required for mission viability.

Table 3 lists select shortfalls for the applicability for lunar missions and how cold electronics development could either enable or enhance their realization. Note that the utility of cryogenic electronics increases in the absence of radioactive energy sources, such as radioisotope heating units (RHUs), radioisotope power systems (RPSs), or fission power sources—particularly when systems are required to operate or even survive the lunar night. This needs assessment assumed no leverage of a thermal management system for an electronics unit that would allow it to operate and/or hibernate in a controlled thermal environment, e.g., warm box.

Table 3. Review of cryogenic-capable electronics for the realization (enabling) or enhancement of several NASA STMD Civil Space shortfalls technologies. This list is a subset of all shortfalls that are relevant to the topics discussed throughout this white paper. For all other shortfalls not included in this table, the reader can assume that the development of cryo-capable electronics is not enabling to closing the technology area, and only enhancing if there are instances where the technology is targeted to survive and/or operate through the lunar night.

Shortfall ID	Shortfall Title	Shortfall Ranking (Integrated List)	Cryo-Capable Electronics are Enabling?	Cryo-Capable Electronics are Enhancing?	Comments
1618	Survive and Operate Through the Lunar Night	1	Yes	Yes	Excessively Broad; Unclear on Impact by Cold Electronics, but Most Likely Enabling

Shortfall ID	Shortfall Title	Shortfall Ranking (Integrated List)	Cryo-Capable Electronics are Enabling?	Cryo-Capable Electronics are Enhancing?	Comments
1596	High Power Energy Generation on Moon and Mars Surfaces	2	No	Yes	Nuclear or Solar Power Generation for this Gap Potentially Needed for Electronics that Must Exhibit Lunar Night Survivability and/or Operation
1554	High Performance Onboard Computing to Enable Increasingly Complex Operations	3	No	Yes	Potentially Needed for Electronics that Must Exhibit Lunar Night Survivability and/or Operation
1557	Position, Navigation, and Timing (PNT) for In-Orbit and Surface Applications	4	No	Yes	Potentially Needed for Electronics that Must Exhibit Lunar Night Survivability and/or Operation
1545	Robotic Actuation, Subsystem Components, and System Architectures for Long-Duration and Extreme Environment Operation	5	Yes	Yes	Component Technologies for Robotic Operations That Can Survive and Operate in Extreme Cold, e.g., Electric Motors, Gearing, Drive Train Components, High Dynamic Range Sensors, Power Storage and Distribution, Computing and Avionics Structures
1552	Extreme Environment Avionics	6	Yes	Yes	Need to Operate Reliably in Harsh Thermal Environment and Survive the Lunar Night Without Active Thermal Control
1519	Environmental Monitoring for Habitation	7	No	No	Dependent on Storage Temperature Range (Thermal Controls)
709	Nuclear Electric Propulsion for Human Exploration	8	No	No	
1304	Robust, High-Progress-Rate, and Long-Distance Autonomous Surface Mobility	9	No	Yes	Potentially Needed for Electronics that Must Exhibit Lunar Night Survivability and/or Operation
1520	Fire Safety for Habitation	10	No	No	Dependent on Storage Temperature Range (Thermal Controls)
1531	Autonomous Guidance and Navigation for Deep Space Missions	11	No	No	
1591	Power Management Systems for Long Duration Lunar and Martian Missions	12	Yes	Yes	Requests Further Advancement of Replaceable / Low-Maintenance Systems; Must Ensure Reliability for Long Duration Operations

Shortfall ID	Shortfall Title	Shortfall Ranking (Integrated List)	Cryo-Capable Electronics are Enabling?	Cryo-Capable Electronics are Enhancing?	Comments
702	Nuclear Thermal Propulsion for Human Exploration	13	No	No	
1559	Deep Space Autonomous Navigation	14	No	No	
1527	Radiation Countermeasures (Crew and Habitat)	15	No	No	
1526	Radiation Monitoring and Modeling (Crew and Habitat)	16	No	No	
879	In-space and On-Surface, Long-duration Storage of Cryogenic Propellant	17	No	Yes	Sensors Needed for Cryogenic Tanks
1548	Sensing for Autonomous Robotic Operations in Challenging Environmental Conditions	18	Yes	Yes	Demands Advances in Sensor Hardware for Robotic Mobility and Manipulation; Particular Interest on High Dynamic Range Force Sensors and Active Perception Sensors Suitable for the Harsh Lunar Environment
1558	High-Rate Communications Across the Lunar Surface	19	No	Yes	COTS and Heritage COMMS Components are Not Cryo-Capable
1626	Advanced Sensor Components: Imaging	20	No	Yes	
792	In-space and On-Surface, Transfer of Cryogenic Fluids	21	Yes	Yes	Electronic Elements Needed for Cryogenic Fluid Transfer Operations, Such as Cryogenic Flow Meters and Cryo-Couplers
1525	Food and Nutrition for Mars and Sustained Lunar	23	No	No	
1571	Navigation Sensors for Precision Landing	24	No	No	
1573	Terrain Mapping Capabilities for Precision Landing and Hazard Avoidance	25	No	No	

Shortfall ID	Shortfall Title	Shortfall Ranking (Integrated List)	Cryo-Capable Electronics are Enabling?	Cryo-Capable Electronics are Enhancing?	Comments
1562	Advanced Algorithms and Computing for Precision Landing	26	No	No	
1597	Power for Non-Solar-Illuminated Small Systems	27	Yes	Yes	Related Shortfalls Include Low Temperature Batteries and Freeze-tolerant Thermal Components
1568	Entry Modeling and Simulation for EDL Missions	28	No	No	
1516	Water and Dormancy Management for Habitation	29	No	No	
1524	Crew Medical Care for Mars and Sustained Lunar	30	No	No	
1546	Robotic Mobile Manipulation for Autonomous Large-Scale Logistics, Payload Handling, and Surface Transport	31	No	Yes	
1592	High-Power, Long-Distance Energy Transmission Across Distributed Surface Assets	32	Yes	Yes	Superconducting Cables and Supporting Electronics Desirable for Permanently Shadowed Region (PSR) Operation
1542	Metrics and Processes for Establishing Trust and Certifying the Trustworthiness of Autonomous Systems	33	No	No	
1390	Power and Data Transfer in Dusty Environments	34	Yes	Yes	Connectors Exposed to Space Need Cryo-Capability; Related Shortfalls Demand Cryo-Operation
1532	Autonomous Planning, Scheduling, and Decision Support to Enable Sustained Earth-Independent Missions	35	No	No	
610	Solar Electric Propulsion - High Specific Impulse	36	No	No	
1563	Aerocapture for Spacecraft Deceleration and Orbit Insertion	37	No	No	
1560	High-Rate Deep Space Communications	38	No	Yes	More Relevant for Deep Space than Lunar

Shortfall ID	Shortfall Title	Shortfall Ranking (Integrated List)	Cryo-Capable Electronics are Enabling?	Cryo-Capable Electronics are Enhancing?	Comments
1194	Prediction Modeling of Cryogenic Fluid Dynamics and Operations	39	No	No	
498	Broad and dependable supply chain for space-qualified robotic hardware, electronics, and associated software	40	Yes	Yes	Bespoke Use of Supply Chain Sensitivities
1430	Small Spacecraft Propulsion	41	No	No	
1588	Protect Earth from Destructive Natural Impacts (Planetary Defense)	42	No	No	
1565	Assessment and Validation Capabilities for Integrated Precision Landing Systems	43	No	No	
1608	Surface-based lunar logistics management for near/mid-term missions	44	No	Yes	
1610	Surface-based food management for sustained lunar evolution	45	No	No	
361	Surface Mating Mechanisms	46	No	Yes	
844	Passive Dust Mitigation Technologies for Diverse Applications	47	No	No	
1438	Autonomy, Edge Computation, and Interoperable Networking for Small Spacecraft	48	No	No	
1553	Foundational Technologies for Future Avionics Devices and Systems	49	No	Yes	
1578	Extraction and Separation of Water from Extraterrestrial Surface Material	53	Yes	Yes	Lunar Extraction Hardware and Associated Electronics

Shortfall ID	Shortfall Title	Shortfall Ranking (Integrated List)	Cryo-Capable Electronics are Enabling?	Cryo-Capable Electronics are Enhancing?	Comments
1595	Energy Storage to Enable Robust and Long Duration Operations on Moon and Mars	57	Yes	Yes	New Technologies that Provide Cryo-Capable Electronics Would Enable Missions that Demand Operation and Survival of Lunar Night
1535	Autonomous Vehicle, System, Habitat, and Infrastructure Health Monitoring Management	72	Yes	Yes	Sensors for Health Monitoring of Lunar Surface Structures Might be Exposed to the Lunar Surface Environments, and Must be Cryo-Capable Related Shortfall to Have Monitors Survive Dormancy
1226	Cryogenic Liquefaction	76	Yes	Yes	Cryocoolers and Associated Electronics
1621	Cryogenic Cooling for Science Instrumentation	77	Yes	Yes	Range is 4K to 5K; Novel Cryocoolers, Valves, Actuators
1555	Next Generation Avionics Architectures	99	No	No	
384	Excavation of Hard/Compacted/Icy Material	104	Yes	Yes	Lunar Core Drilling Hardware and Associated Electronics; Related Shortfalls Include Detectors for Subsurface Ice, Long-duration Resource Evaluation in Extreme PSR Environment (Cryogenic), and Long-duration Lunar System Survival and Reliability
1533	Autonomous Robotic Sample Identification, Classification, Collection, Manipulation, Verification, and Transport	105	Yes	Yes	Similar to Other Robotic Shortfalls
705	Low Power Nuclear Electric Propulsion	122	No	No	
1550	Crew Audio/Visual Interfaces for Long Duration Missions Beyond LEO	136	No	No	
1408	Advanced deployable load-bearing structures	150	No	Yes	Needed if electronics are embedded in the structure (health monitoring, deployment sensors, etc.) and not within a warm box.

Shortfall ID	Shortfall Title	Shortfall Ranking (Integrated List)	Cryo-Capable Electronics are Enabling?	Cryo-Capable Electronics are Enhancing?	Comments
755	Cross-Discipline Fluid Management Technologies	164	Yes	Yes	
1579	Extraction and Separation of Non-Water Volatile Resources from Lunar Regolith	169	Yes	Yes	Lunar Extraction Hardware and Associated Electronics
1436	Lunar Surface Power Generation from ISRU Derived Sources	178	No	Yes	Manufacturing Tools and Products May Need to be Cryo-capable

NASA's Moon to Mars (M2M) White Papers

NASA recently released an updated M2M Architecture Concept Review, along with white papers on various topics, e.g., lunar surface cargo, lunar mobility drivers and needs, architecture-driven technology gaps, and science goals [23, 24, 25, 26, 27, 28]. Cold electronics **could be mission-enabling** for the following highlighted objectives:

- **Extending Lifespan of Systems**
  - The ability to operate without extensive heating during extreme cold reduces wear and energy use, enabling extended mission durations on both the Moon and Mars.

- **Enabling New Science**
  - Access to shadowed and cold regions on both celestial bodies provides opportunities for unique scientific discoveries related to volatiles, geology, and astrobiology [25, 28]

- **Reducing System Complexity**
  - Reducing the need for active thermal regulation simplifies design and reduces mass, enabling more payload capacity for science and exploration

Cold electronics development **would be enhancing** lunar missions for these capabilities:

- **Mobility Systems**
  - Electronics capable of withstanding extreme cold could enhance autonomous and teleoperated mobility systems, crucial for transporting cargo and supporting infrastructure across lunar regolith and harsh terrain [23, 24]
  - Cryogenic-resistant systems would enable longer operational life during extended lunar nights, enabling longer distances from fixed facility/base power sources [24]
  - South-Polar Aitken (SPA) basin sample return requires long-lived, long-distance roving capabilities coupled with robotic sampling and large cargo sample return via crewed Artemis missions [25]

- **Payloads and Related Instrument Infrastructure**
  - Instruments deployed in shadowed craters or permanently shadowed regions (PSRs) would benefit from electronics that can function effectively at low temperatures. These areas are key to studying volatiles [23, 25]
  - Cryogenic electronics could be integral to the development of the Lunar Geophysical Network (LGN) concept, the lunar architecture would require long-lived (6-10 years) surface assets (i.e., power and thermal control) [26].

- **Sample Handling and Preservation**
  - Systems for collecting, storing, and analyzing cryogenic volatile samples, such as lunar ice, would require robust electronics to maintain integrity during storage and transport [25, 26]

- **Power and Thermal Management**
  - Electronics capable of operating under extreme cold could reduce the reliance on active thermal management systems, such as electric heaters, thereby conserving energy and extending mission durations [23, 27]

National Cislunar Science and Technology Action Plan

On December 2024, the White House Office of Science and Technology Policy (OSTP) released an updated version of their National Cislunar Science and Technology Action Plan [29]. This document is meant to outline the "*science and technology objectives for realizing U.S. leadership in Cislunar space, including the Moon*" [29]. This section highlights those goals that would be enabled and/or enhanced by the development of cold electronics.

- **Research and Development for Long-term Growth in Cislunar space**
  - One of the main strategic objectives of the action plan
  - More specifically, Section 1.1 *Enabling Enduring Human Presence*, Statement 1.1.6 of the action plan states the need to "*conduct research and gather data on the effects and appropriate mitigations of ongoing natural and artificial hazards to humans and machines in Cislunar space, including radiation, space weather events, microgravity, partial gravity, micrometeoroids, debris due to rocket plume impingement on regolith, and Lunar dust.*"
  - While the thermal environment is not explicitly listed, cold-operable and/or cold-tolerant electronics could help achieve long-term lunar surface exploration

- **ISRU Robotic Technologies**
  - According to Section 1.1 Enabling Enduring Human Presence, Statement 1.1.3, it is desirable to "*advance research, development, and demonstration of capabilities using materials sourced from the Moon.*"
  - Similarly, Statement 1.1.4 mentions the goal to "*advance research and development of robotic exploration and operational capabilities, including robotic rovers and robots for habitat assembly, regolith processing, or any other high priority activity on or around the Moon that can be more efficiently, cost-effectively or safely done by robots*"
  - Regardless of the location on the Moon, if meant to be operational for long periods, exposed electronics in these robotic systems will need to be able to survive extreme cold

- **Environment-resilient Communication Systems**
  - According to Section 1.1 Enabling Enduring Human Presence, Statement 1.1.5, it is desirable to "*advance design and development of high-performance atomic clocks and oscillators, including technology that enables use in space environments—such as frequency combs and microwave links—to enable robust communication infrastructure, research in fundamental sciences and astronomy, and position, navigation, and timing systems in Cislunar environments*"
  - If these are planned to be fixed assets on the Moon, these will need to survive cold of lunar night
- **Science-enabling Technologies**
  - According to Section 1.2 *Advance Cislunar Science*, Statement 1.2.4, it is necessary to "*advance technologies and develop associated practices and guidelines to preserve the Lunar environment for future scientific activities, including radio astronomy from the radio-quiet, far side of the Moon and exploration of Lunar polar regions. Activities may include but are not limited to identification of the scientifically valuable regions of the electromagnetic spectrum*"
  - Statement 1.2.5 refers to the need to "*advance technologies to enable characterization of the presence, form, and extent of Lunar resources*"
  - Statement 1.2.6 adds the need to "develop technology to mitigate environmental impacts to Cislunar space that might harmfully limit future use"
  - Section 4.2 Ensure Capabilities are Scalable and Interoperable with Private and International Actors, Statement 4.2.3 declares that we must "*identify priority technology demonstrations to enable modernized and expanded sensing, ranging and timing technologies, as well as techniques that enable integration of new space-based operations with existing infrastructure*"

- This matches the goals and the role of cold electronics as argues in the M2M white paper section

- **Position, Navigation, and Timing (PNT) Capabilities**
  - In alignment with M2M architecture goals, the action plan stresses the need for developing a lunar surface communication and PNT that is *"capable of scaling to support long term science, exploration, and industrial needs"*
  - Permanent surface networks on the lunar surface will be subject to cold environments of lunar night.

KEY ELECTRONICS CONSIDERATIONS

Heritage Mars Missions and Future Lunar Applicability

Historically, missions such as the solar-powered Mars Exploration Rovers (MER) and the radioisotope-powered Mars Science Laboratory (MSL) provide valuable lessons in designing vehicles for cold, hostile planetary environments. MER demonstrated how robust insulation, radioisotope heating units (RHUs), and carefully managed solar power could sustain electronics through Martian nights (~12 hours), whereas MSL's radioisotope power source offered both electrical power and a steady supply of waste heat to warm its components.

Although these approaches were highly effective on Mars, future lunar missions face far harsher temperature swings, especially during the ~14-day lunar night. Longer unlit periods, colder surface temperatures, and increasingly distributed electronics make direct application of prior rover-based thermal designs less effective. In particular, while radioisotope or other active heating systems may still play a role on the Moon, emerging opportunities to develop electronics that can survive and operate in cryogenic temperatures are crucial. These cryogenic-capable systems can reduce dependence on local heat sources, mitigate the penalties of long-duration thermal management, and open up more flexible mission concepts—extending operational lifetimes and enabling broader scientific and exploration objectives.

Furthermore, many planned lunar architectures anticipate multi-year or multi-decade activities, amplifying qualification challenges for standard electronics. By adopting cryogenic electronics, subsystems can handle the Moon's extreme temperature cycles without demanding the same level of constant heating support. Identifying which electronics warrant near-term development for cold-capable operation requires a careful assessment of the mission's thermal constraints, reliability needs, and power allocations across diverse subsystems.

System Architecture Categories

The extreme lunar thermal environments necessitate strategic decisions regarding the placement and protection of electronic systems. Three primary architectures—centralized, distributed, and hybrid—offer distinct trade-offs in terms of thermal management, power efficiency, and system complexity.

CENTRALIZED ARCHITECTURE

The centralized electronics architecture places nearly all mission-critical electronic components within a Warm Electronics Box (WEB) to maintain controlled thermal conditions. This approach minimizes exposure to extreme

temperatures, leveraging insulation and internal heating to ensure the long-term survival and functionality of sensitive systems.

Characteristics:

- Majority of electronics housed in a thermally controlled environment.
- Only essential components such as sensor focal planes, mobility electronics (e.g., motor controllers, encoders), and RF front ends are external to the WEB.
- Modeled after successful designs such as the Mars Exploration Rovers (MER) and Mars Science Laboratory (MSL), where the WEB played a critical role in thermal management and reliability.

Advantages:

- Simplifies thermal management and shielding.
- Enhances component longevity and reduces radiation exposure.
- Well-established and flight-proven methodology.

Disadvantages:

- Requires extensive cabling to connect remote sensors and actuators.
- Increased mass and thermal inertia can lead to inefficiencies.
- Limited flexibility in integrating advanced cold-tolerant electronics.

DISTRIBUTED ARCHITECTURE

A distributed architecture disperses electronics across the system, with minimal reliance on a centralized WEB. This implies that all or most electronics must be designed to withstand extreme cold conditions, utilizing advanced materials and thermal strategies.

Characteristics:

- Electronics positioned at or near their operational locations (e.g., actuators, instruments, communication elements).
- Requires cold-tolerant components capable of operating in extreme lunar or planetary environments.
- Could be paired with multi-node thermal protection strategies, including Radioisotope Heater Units (RHUs) for critical components.

Advantages:

- Point-of-load benefits: High-current-output power converters can be placed near their loads, reducing losses and cabling mass.
- Improved signal integrity: Instrument amplifiers located close to sensors minimize low-level signal losses and noise, similar to Low-Noise Amplifiers (LNAs) in communication systems.
- Potential reduction in system mass by eliminating centralized enclosures.

Disadvantages:

- Increased complexity in power distribution and thermal management.
- Demands extensive qualification of cold-capable electronics.

A hybrid approach blends elements of both centralized and distributed architectures. The majority of electronics remain in a controlled thermal environment, while key components that offer significant advantages are placed in external cold environments.

Characteristics:

- Retains one or more WEBs for core avionics and high-sensitivity electronics.
- Select cold-capable subsystems, such as LNAs near communication antennas or mobility electronics near actuators, operate outside the WEB for efficiency.
- Strategic use of small RHUs (~1W) to maintain acceptable temperatures for critical cold-exposed components.

Advantages:

- Optimized thermal and power management: Components benefit from controlled conditions where necessary while still achieving point-of-load efficiencies for power delivery and signal integrity.
- Reduced cabling mass: Minimizes long wiring runs by placing power and signal electronics closer to their operational sites.

Disadvantages:

- More complex system integration than a fully centralized design.

AREAS OF PRIORITIZATION

To determine which electronics require prioritization for cryogenic development, use cases were examined across various subsystems. The following areas were identified as requiring cold electronics solutions:

Mobility and Actuation Systems

- Robotic actuation components: Motors, gears, and subsystems for long-duration surface mobility (rovers, robotic arms)—particularly those far from an active heat source.
- Navigation and positioning sensors: Particularly optical or force sensors or encoders that are required to be externally mounted.
- Autonomous guidance electronics: To enable long-distance traverses in cryogenic conditions

Science and Instrumentation

- Cryogenic detectors for volatiles, regolith composition, and astrophysical observations
- Cryogenic sample handling and analysis: Systems for collecting and preserving volatile-rich samples in extreme cold environments
- Improving heritage instruments to remove the need for survival heaters, or warm-up operational heaters

Power and Energy Storage

- Low-temperature battery technologies (e.g. electrolytes) to survive lunar night cycles, and operate at cold temperatures
- Cryogenic power management and power distribution systems that can function in PSR-based solar farms or nuclear-powered surface systems

Packaging and Passives

- Passive components (resistors, capacitors, inductors) with suitable dielectrics must be verified for sub cryogenic lunar operation. Standard flight-rated passives rarely specify performance below -55°C
- Multi-year reliability in repeated thermal cycles is a known challenge. Up-screening COTS parts can involve lengthy qualification campaigns, especially when designing for 20-year lifetime.

Communication Systems

- Cold-tolerant RF and optical communication electronics
- Cryogenic atomic clocks for enhanced navigation in the absence of GPS-like systems

THERMAL PERFORMANCE AND INNOVATION OPPORTUNITIES

Performance Risks Without Thermal Support

Baseline assessments indicate that without thermal mitigation:

- Electronic failures occur due to thermal contraction, cracking, and resistance changes in circuits.
- Batteries become inoperable due to electrolyte freezing.
- Lubricants degrade, increasing wear on motors, gears, and actuators.
- Sensor noise, drift, and degradation increase due to temperature-sensitive components.

NASA's shortfall #498 ("Broad and dependable supply chain for space-qualified robotic hardware, electronics, and associated software") identifies that no robust supply chain currently exists for cryogenic-rated avionics. Commercial Off-the-Shelf solutions for "deep cryo" are limited. Some COTS instruments (e.g., camera sensors) can survive short-term exposures to -100°C if properly tested, but repeated or extended operation often demands custom packaging. Minimal or no flight heritage for "COTS cryo chips" presents a risk. Long and deep thermal cycles risk microcracking (damage and/or degradation) or shifts in performance.

System-level Solutions

System-level thermal solutions may reduce the need for some cryogenic electronics:

- Passive thermal strategies: Multilayer insulation (MLI), vacuum-layered insulation, thermal capacitors/Phase change materials, advanced coatings, and heat pipes.
- Leverage advances in Radioisotope Power Sources (RPS):
- Commercialization: NASA is expanding its role to facilitate the commercialization of RPS [30]
    - Constant Rate Production (CRP): DOE and NASA agreed to transition the delivery of RPS from a mission-driven approach to a CRP approach, to provide shelf-ready, flight-quality components readily available for NASA mission use [30].
    - Regulatory Considerations: NASA is working with regulatory bodies to streamline the launch approval process [30]
    - Lightweight Radioisotope Heater Units (LW RHUs): NASA and DOE are re-establishing LWRHU production to support missions requiring passive heating (~1W/unit) rather than power generation. ESA's Rosalind Franklin Mars rover will receive up to 40 LWRHUs as part of NASA's contribution [30].
- Hybrid thermal/electronic solutions: Integrated RHUs for critical subsystems, minimizing electronic redesign.
- Smaller systems with radioactive power sources (e.g. Curiosity and Perseverance Mars Rovers) can leverage waste heat via heat pipes to reduce cryogenic requirements.
- Minimizing parasitic heat routing

PRIORITIZED COLD ELECTRONICS INVESTMENTS

System-level thermal solutions offer broad advantages, but prioritizing cold electronics in specific applications can be beneficial. For example, missions targeting permanently shadowed regions require particular thermal management to maintain the cryogenic environment essential for scientific objectives, such as cryogenic volatile sampling.

Based on mission feasibility and impact, the following cold electronics technologies offer the highest return on investment:

Tier 1 (Mission-Enabling, Highest Priority)

1. Cryogenic-capable actuators and sensors: Required for PSR ISRU, long-duration science, and lunar rovers. Handling cryogenic volatiles or robotic excavation in low temperatures. Cryogenic sample return.
2. Low-Temperature Energy Storage: Freeze tolerant and cold-operable batteries to support extended lunar night operations.
3. Cryogenic propellant storage: sensors, valves, control & power electronics necessary for managing cryogenic propellants.
4. Extreme environment avionics: Computing, storage, and control systems survivable at -150°C to -200°C. Note that such components have traditionally been enclosed in a warm electronics box (WEB) with thermal management—removing the requirement for cryogenic electronics.

Tier 2 (Mission-Enhancing, High Priority)

1. Cryogenic instrumentation for science payloads: Including low-temperature spectrometers, volatile analyzers, and radiation-hardened sensors.
2. Low-temperature RF communication and networking electronics: For PSR-based relay stations. High-rate communications.
3. Cryogenic-resistant mechanical systems: Bearings, lubricants, and mobility components.

CONCLUSIONS AND RECOMMENDATIONS

This assessment illustrates that electronics able to survive and/or operate under extreme lunar temperature conditions are increasingly essential for meeting NASA's broader architecture gaps and strategic priorities. Such "cold electronics" could reduce reliance on active heating, minimize power consumption and mass, and extend mission lifetimes—particularly in the harsh environment of the lunar surface, and particularly in the colder extremes of permanently shadowed regions.

The development of cryogenic electronics for lunar applications also presents an opportunity for extending mission capabilities beyond the Moon to other planetary bodies such as Mars, Europa, and Titan. Many of the architectural challenges addressed by lunar cryogenic technologies—such as operating in extreme cold, mitigating thermal cycling stresses, and reducing reliance on active heating—align with the environmental demands of deep-space destinations.

The challenges of designing for extended lunar operations in diverse environments can be addressed with a twofold approach:

1. System-Level Thermal Strategies: Thermal management solutions—such as enhanced insulation, passive thermal strategies, robust enclosures, or leveraging radioisotope heating (RHUs, RPS) where appropriate—can provide an alternative or complementary path for some applications.

2. Targeted Cold-Capable Electronics: Key avionics, actuation components, sensors, and other subsystems that can reliably perform at cryogenic temperatures would allow missions to remove or scale back thermal enclosures and survival heat sources. This directly aligns with NASA's identified shortfalls in extreme environment avionics, low-temperature energy storage, and cryogenic instrumentation for science payloads.

By blending cryogenic electronics development with well-considered thermal strategies, NASA can respond to demanding mission scenarios—particularly for long-duration lunar activities, in-situ resource utilization, or missions to permanently shadowed regions. Ultimately, a careful, use-case-driven prioritization of cold electronics promises not only to close key technology gaps but also to bolster system reliability, mission performance, and future exploration objectives.

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Appendix B Lunar Thermal Assessment Report

LUnar and Mars ENvironments Analysis Team (LUMENATE)

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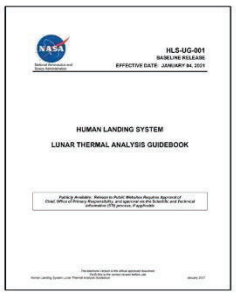
Will Grier (LaRC-D206), will.j.grier@nasa.gov

Lunar Thermal Assessment for NESC Cold Electronics Report

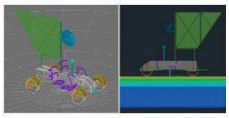
July 1st, 2025

LUnar and Mars ENvironments Analysis Team (LUMENATE)

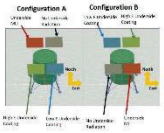
- **The LUMINATE team delivers specialized Lunar and Martian thermal environmental modeling expertise to NASA and commercial partners:**
  - Develop, maintain, and disseminate guidance documentation and reference models for performing thermal analysis for Lunar and Martian environments
  - Address critical environmental knowledge gaps identified during system development efforts and missions
  - Improve and create advanced thermal analysis techniques and capabilities that support diverse missions and systems
  - Provide thermal modeling expertise to ensure mission success in challenging extraterrestrial thermal environments
- **Current duties include:**
  - Update the Lunar Thermal Analysis Guidebook (LTAG)
  - Develop a Mars Thermal Analysis Guidebook (MTAG)
  - Develop novel thermal analysis capability for the Artemis III mission to obtain environmental sink temperatures to inform EVA planning



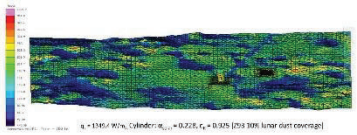
HLS-UG-001 Lunar Thermal Analysis Guidebook[1]



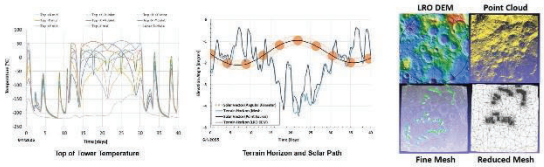
Thermal Sensitivity of LTV Wheels, Will Birmingham (MSFC-EV34)[3]



Lunar Latitude and Terrain Radiator Sensitivity, Will Birmingham (MSFC-EV34)[4]



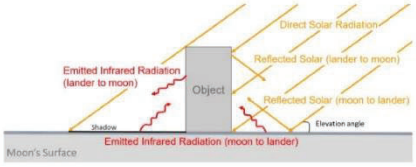
Lunar Surface 3D Terrain Modeling, Lisa Erickson (JSC-EC611)[2]



Tall Tower Lunar Thermal Analysis, Will Grier (LaRC-D206)[5]

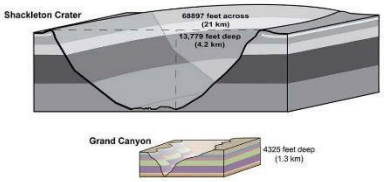
Lunar Thermal Environment

- The Lunar surface thermal environment is complex and significantly more extreme than Earth's in both magnitude and variation due to the following characteristics[1]:
  - Regolith thermophysical and optical properties
    - Low thermal inertia, high IR emissivity, high solar absorptivity
  - Lack of an atmosphere
    - Radiation dominant heat exchange, unobstructed incident solar flux
  - Rotational period
    - ~29 Earth days with ~14.5 day nighttime duration
  - Axial tilt to the ecliptic plane
    - 1.54°, complex solar illumination environment at the poles
  - Complex and location dependent topology
    - Deep craters and high peaks



Radiation Exchange on Lunar Surface[1]

- The regolith surface temperatures are not the effective thermal environment that components near or on the surface will experience; accurately identifying worst case thermal environments for assets on the Lunar surface requires knowledge of the specific mission location:
  - Maximum incident solar elevation angle
    - Latitude and local ground slope dependent
  - View factor to surface
    - Nearby terrain topology, vehicle occlusion, height above surface
  - Regional regolith thermophysical and optical properties

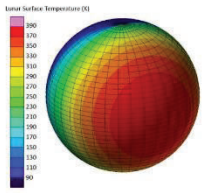


Shackleton Crater vs Grand Canyon[6]

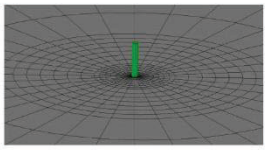
Lunar Thermal Modeling Capability

- A universal generic thermal model that captures worst case regional Lunar thermal environments does not currently exist

- The current version of the HLS Lunar Thermal Analysis Guidebook and associated NESC Academy tutorial videos provide guidance on developing simplified and mission site specific Lunar surface thermal models[1][7]
  - HLS-UG-001 Lunar Thermal Analysis Guidebook Baseline_STI.pdf
  - Lunar Thermal Analysis Guidebook, Part 1 | NESC Academy Online
  - Lunar Thermal Analysis Guidebook, Part 2 | NESC Academy Online
  - Lunar Thermal Analysis Guidebook, Part 3 | NESC Academy Online

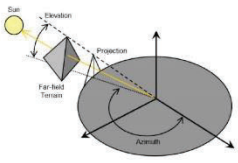


Lunar Surface Temperatures[1]



Simplified Flat Plane Surface Model[1]

- This study uses a simplified thermal model with a flat ground plane as a stand in for the Lunar surface to provide insight into the potential differences between regolith surface temperatures and the effective thermal environment exposed onto representative electronics
  - A flat ground plane does not capture universal worst case hot or cold conditions due to the thermal impacts of location specific ground slope, surrounding terrain, and solar elevation
  - Data provided in this package shows electronics can get much colder or hotter than the ground temperature



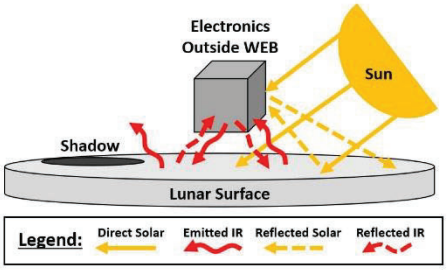
Far Field Terrain Impacts[1]

Detailed Site-Specific Terrain Mesh[1]

Environmental Sink Temperature

Definitions:

- **Electronics Outside of Warm Electronics Box (WEB):** Electronic components mounted external to mechanical enclosures which are therefore directly exposed to the space thermal environment.
- **Environmental Sink Temperature:** The effective temperature of the surrounding environment that acts as a thermal sink for radiative heat transfer from a surface. Represents the complex radiation environment as a single equivalent temperature.
- **IR Emissivity (ε):** The fraction of infrared energy that is emitted from a surface relative to a perfect blackbody at the same temperature, ranging from 0 to 1. IR absorptivity is equivalent to IR emissivity at the same temperature and radiation wavelength (per Kirchhoff's Law). A surface with high IR emissivity will absorb most incident infrared energy and emit most of that absorbed infrared energy.
- **Solar Absorptivity (α):** The fraction of incident solar energy absorbed by a surface, ranging from 0 to 1. A surface with high solar absorptivity absorbs most incoming solar energy, and low absorptivity indicates high solar reflectance.
- **α/ε Ratio (Alpha-to-Epsilon Ratio):** The ratio of solar absorptivity to infrared emissivity. A low α/ε ratio surface absorbs little solar energy and emits most absorbed heat (desirable for thermal rejection). A high α/ε ratio indicates high solar absorption with poor heat rejection capability.



Environmental Sink Temperature Calculation[16,17]

$$0 = \alpha_s Q_s + \varepsilon_{IR} Q_{IR} - \varepsilon_{IR} \sigma T_\infty^4$$

$$T_\infty = \left(\frac{1}{\sigma} \left(\frac{\alpha_s}{\varepsilon_{IR}} Q_s + Q_{IR} \right) \right)^{0.25}$$

Parameter	Symbol	Unit
Solar Absorptivity	α_s	N/A
Solar Flux	Q_s	W/m²
IR Emissivity	ε_{IR}	N/A
Infrared (IR) Flux	Q_{IR}	W/m²
Environmental Sink Temp.	T_∞	K
Stefan-Boltzmann Constant	σ	W/m²K⁴

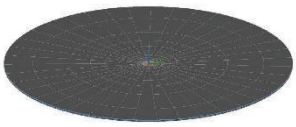
Simplified Model Overview

- **Used Thermal Desktop to analyze the thermal environments (environmental sink temperature) imparted onto electronics outside of a WEB that is exposed to the environment in Lunar polar, mid-latitude, and equatorial locations**
  - Investigated date range: 1/1/2028 to 1/1/2029
  - Electronics modeled as 0.1x0.1x0.1m arithmetic node cube with uniform optical properties
    - Optical property ratio (α_s / ε_{IR}) varied over a representative range (~80% of systems)
    - No internal heat generation
  - Simplified flat ground plane with radius of 150m representing the Lunar surface
  - Electronics are separated from ground plane by 2m
- **Lunar environment defined using LTAG, DSNE, and JPL Horizons data** [1][8,9]
  - Time varying and location dependent solar vector and solar flux from JPL Horizons[9]
  - Surface IR emissivity and solar absorptivity (incident angle dependent)[10,11]
    - highland directional α_s (polar) and mare directional α_s (mid-latitude & equatorial)
  - Surface density (depth dependent)[12,13]
  - Surface thermal conductivity (depth and temperature dependent)[12,13]
  - Surface specific heat (temperature dependent)[14]
  - Solar diameter (subtended) angle (0.53°)[1]
  - Subsurface ground heat flow (~0.018 W/m²)[15]
- **Not included in thermal model**
  - Site specific terrain (local slope, adjacent hills, craters)
  - Vehicle geometry or occlusion (lander, platform, etc)
  - Regolith dust deposition onto electronics (alters optical properties)
  - Earthshine (0 to 0.15 W/m²) and eclipses (~hours)[1]

Analyzed Locations

Location	Latitude	Longitude
Polar	-89.47°	-138.01°
Mid-Latitude	±45°	0°
Equatorial	0°	0°

Arithmetic Node Cube, Electronics Outside WEB

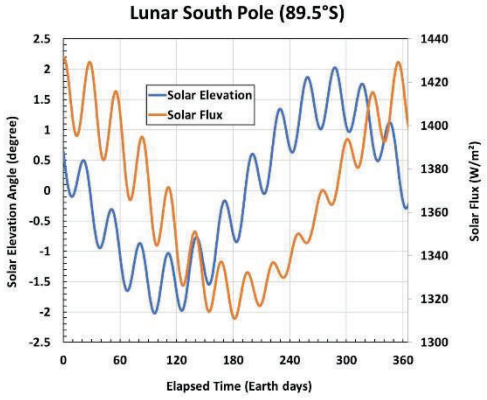


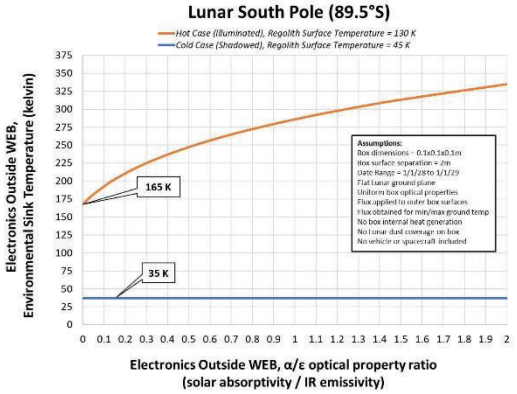
Flat Ground Plane, Lunar Surface

Location: South Pole

- Near the Lunar poles the solar elevation angle remains low with the sun circling close to the horizon. This creates a low solar incident angle relative to the terrain, resulting in relatively cool ground temperatures despite direct sunlight.
- The electronics are exposed to differential incident heat flux: side faces receive solar illumination, the bottom face receives heat from the lunar surface, and the top face predominantly radiates to deep space with minimal solar input
- Environmental sink temperature vs. optical property ratio trends were derived from analysis timesteps selected based on peak Lunar surface temperatures (hot case = 130 K & cold case = 45 K). These timesteps provided the incident flux values (IR and solar) used in the sink temperature calculation

Solar Absorptivity (α_s)	IR Emissivity (ε_{IR})	Ratio ($\alpha_s/\varepsilon_{IR}$)
0.1	0.9	0.1
0.35	0.7	0.5
0.5	0.5	1
0.7	0.35	2

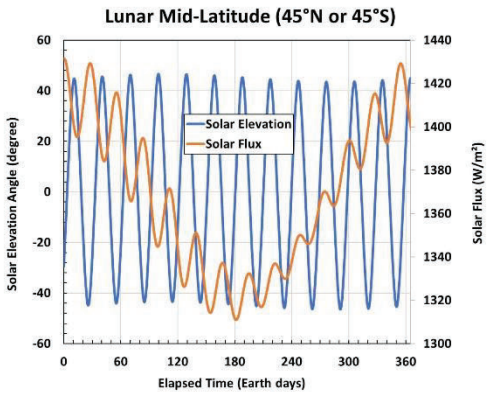


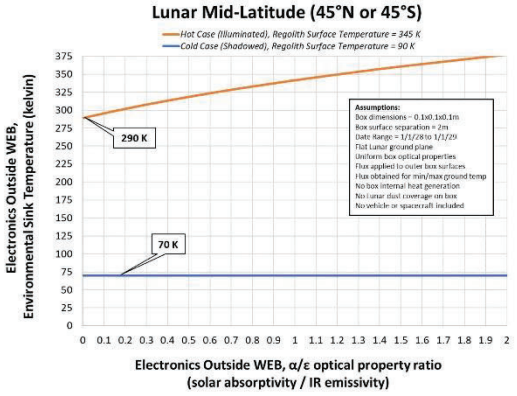


Location: Mid-Latitude

- At lunar mid-latitudes the solar elevation angle varies throughout the day with the sun arcing higher across the sky than at the poles generating relatively higher surface temperatures
- The electronics side faces receive alternating periods of direct and indirect solar illumination, the bottom face received heat from a surface subject to wider temperature swings, and the top face periodically receives direct sunlight
- Environmental sink temperature vs. optical property ratio trends were derived from analysis timesteps selected based on peak Lunar surface temperatures (hot case = 345 K & cold case = 90 K). These timesteps provided the incident flux values (IR and solar) used in the sink temperature calculation

Solar Absorptivity (α_s)	IR Emissivity (ε_{IR})	Ratio ($\alpha_s/\varepsilon_{IR}$)
0.1	0.9	0.1
0.35	0.7	0.5
0.5	0.5	1
0.7	0.35	2

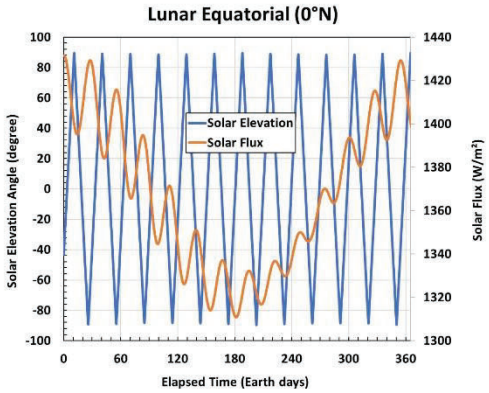


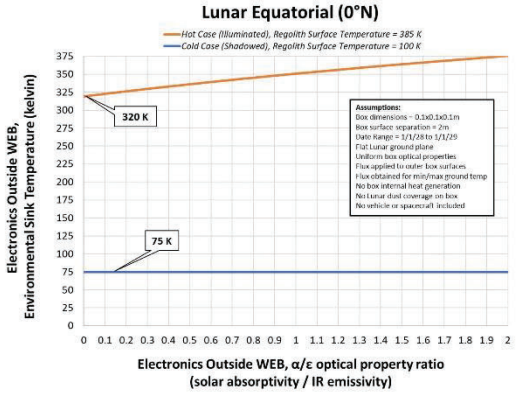


Location: Equatorial

- At the lunar equator, the solar elevation angle reaches zenith during local noon with near-perpendicular solar incident angles with the terrain generating high surface temperatures
- The electronics side faces receive directional solar illumination as the sun moves overhead, the bottom face exchanges heat with a surface that reaches extremely high daytime temperatures, and the top face receives maximum solar input during lunar noon
- Environmental sink temperature vs. optical property ratio trends were derived from analysis timesteps selected based on peak Lunar surface temperatures (hot case = 385 K & cold case = 100 K). These timesteps provided the incident flux values (IR and solar) used in the sink temperature calculation

Solar Absorptivity (α_s)	IR Emissivity (ε_{IR})	Ratio ($\alpha_s/\varepsilon_{IR}$)
0.1	0.9	0.1
0.35	0.7	0.5
0.5	0.5	1
0.7	0.35	2





NESC Report Recommendations

- Regolith surface temperatures are not the effective thermal environment that components near or on the surface will experience
  - Accurately identifying worst case thermal environments for assets on the Lunar surface requires knowledge of the specific mission location and vehicle integration
    - Effective electronics temperatures could be much hotter or colder than Lunar surface temperatures
- A universal generic lunar surface thermal model capturing absolute worst-case regional thermal environments does not currently exist
  - The lunar surface thermal environment varies significantly by location due to differences in terrain features, regolith compositions, and solar incidence angles. Additionally, the specific vehicle integration will further impact the thermal environment due to factors including reflections from vehicle surfaces and partial occlusion from the environment.
  - It may be possible to develop a thermal model that captures regional absolute worst-case environments, but this effort requires detailed terrain modeling and result validation with Lunar solar illumination models.
- It is recommended that cold tolerant electronics developers perform the following to obtain relevant qualification limit temperatures:
  - Gather mission specific information (e.g., surface location, vehicle type, hardware integration scheme, electronics surface optical properties)
  - Consult a thermal analyst to perform analysis using a lunar specific thermal model that includes surface terrain features
    - The current version of the HLS Lunar Thermal Analysis Guidebook and associated NESC Academy tutorial videos provide guidance on developing simplified and mission site specific Lunar surface thermal models
- This study outlines the variables that impact the effective thermal environment an electronics will be exposed to on the Lunar surface
- Data provided in this package shows an electronics can get much colder or hotter than the ground temperature depending on the:
  - Region of the Lunar surface in which the electronics resides
  - Optical properties of the electronics

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Appendix C Summary of SiGe Library Developed under NASA COLDTech and LuSTR

Background:

The NASA SiGe COLDTech Project (2021-2025, PI John D. Cressler, Georgia Tech) demonstrated that SiGe technology can satisfy NASA's need for a diverse set of electronics infrastructure (RF + Analog + Digital) for Ocean Worlds Surface Missions (5 Mrad and -180ºC on Europa), culminating in a X-band (8-12 GHz) RF receiver demonstration as a pathfinder. Those results are easily extensible to a broad set of lunar missions, including light side, dark side, and shadowed polar crater deployment, **using the same parts, and without a protective warm box**.

Circuit Technology:

The GlobalFoundries 90 nm SiGe 9HP BiCMOS technology is a robust, commercially available foundry electronics technology that combines 300 GHz SiGe HBTs with Si CMOS technology for diverse applications. Each foundry run requires 7-9 months of fabrication time.

Available SiGe Electronic Infrastructure and Design Ecosystem:

- Deep MPW tapeout experience with Global Foundries SiGe 9HP
- Exhaustive RF measurement capability (to 10K and 67 GHz)
- Transistor models and simulation test benches
- Library circuit component documentation and design files

Available RF Circuit Component Library: (to 10K + 5Mrad TID radiation)

- X-Band RF Receiver (LNA, mixer, VCO, IF amp)
- X-Band Low Noise Amplifier (LNA)
- X-Band Down-Conversion Mixer
- X-Band Voltage-Controlled Oscillator (VCO)
- X-Band RF Power Detector
- X-Band Phase Locked Loop (PLL)
- X-Band Divide-By-2 Frequency Divider
- X-Band Phase Detector
- IF Amplifier
- X-band RF Single-Pole Double-Throw (SPDT) Switch
- X-band Phase Shifter
- A Variety of Multi-purpose Analog Bias Blocks
- Ka-Band LNA (in fab at present)

SiGe Analog Library (COLDTech & LuSTR):

- 1.8-V BiCMOS Low Drop Out (LDO) Regulator w/ PMOS Pass Device
- 3.3-V BiCMOS Linear Voltage Regulator (LVR) w/ NPN Pass Device
- 1.2-V CMOS Time-Interleaved Ringamp LDO
- 1.8-V BiCMOS OpAmp w/ Pseudo Class-AB Output Stage

- 3.3-V BiCMOS OpAmp w/ Pseudo Class-AB Output Stage
- 3.3-V BiCMOS PTAT Current Reference
- 1.8-V BiCMOS Fixed Inversion-Coefficient Current Reference
- 1.2-V CMOS Constant-gm Current Reference
- 3.3-V BiCMOS Curvature-Compensated Bandgap Voltage Reference
- 1.8-V BiCMOS Comparator
- 3.3-V BiCMOS Comparator

SiGe ECL Standard Cell Library (COLDTech):

- 3.3-V ECL INV (Inverter/ Buffer)
- 3.3-V ECL_OR (2-input OR/NOR)
- 3.3-V ECL AND (2-input AND/NAND)
- 3.3-V ECL_XOR (2-input XOR/XNOR)
- 3.3-V ECL MUX21 (2-to-1 Multiplexer)
- 3.3-V ECL_DFFSR (D-Flipflop w/ set reset capability)
- 3.3-V ECL Reference (Reference circuit that supplies a bias voltage to establish 10uA tail current in ECL cells)
- 3.3-V ECL_Simple_Reference
- 3.3-V ECL Voltage_Reference (Supplies a fixed common-mode voltage level centered between ECL logic levels (e.g., needed for ECL OR))
- 3.3-V ECL_TIE_HI (Supplies a logical ECL_HI signal)
- 3.3-V ECL TIE_LO (Supplies a logical ECL_LO signal)
- 3.3-V ECL_INV_PAD_BUFFER (1mA tail current I/O pad buffer)
- 3.3-V Simplified ECL_Memory_Controller (limited I/O)

Pasrt designed for a full SiGe BiCMOS SRAM system (COLDTech):

- 1.2-V PMOS-only SRAM Bitcell
- 3.3-V input stage / 1.2-V output stage ECL Write Amplifier (also useful as LV SiGE PECL 3.3V-to-1.2V translator)
- 1.2-V input stage / 3.3-V output stage ECL Sense Amplifier (also useful as LV SiGE PECL 1.2V-to-3.3V translator)
- 3.3-V Address Decoder (synthesizable using SiGe ECL Standard Cell Library)
- 1.2-V 6T Standard SRAM Bitcell (CMOS) (demo-only, not intended for reliable extreme cold, rad hard)
- 3.3-V Simple Reference

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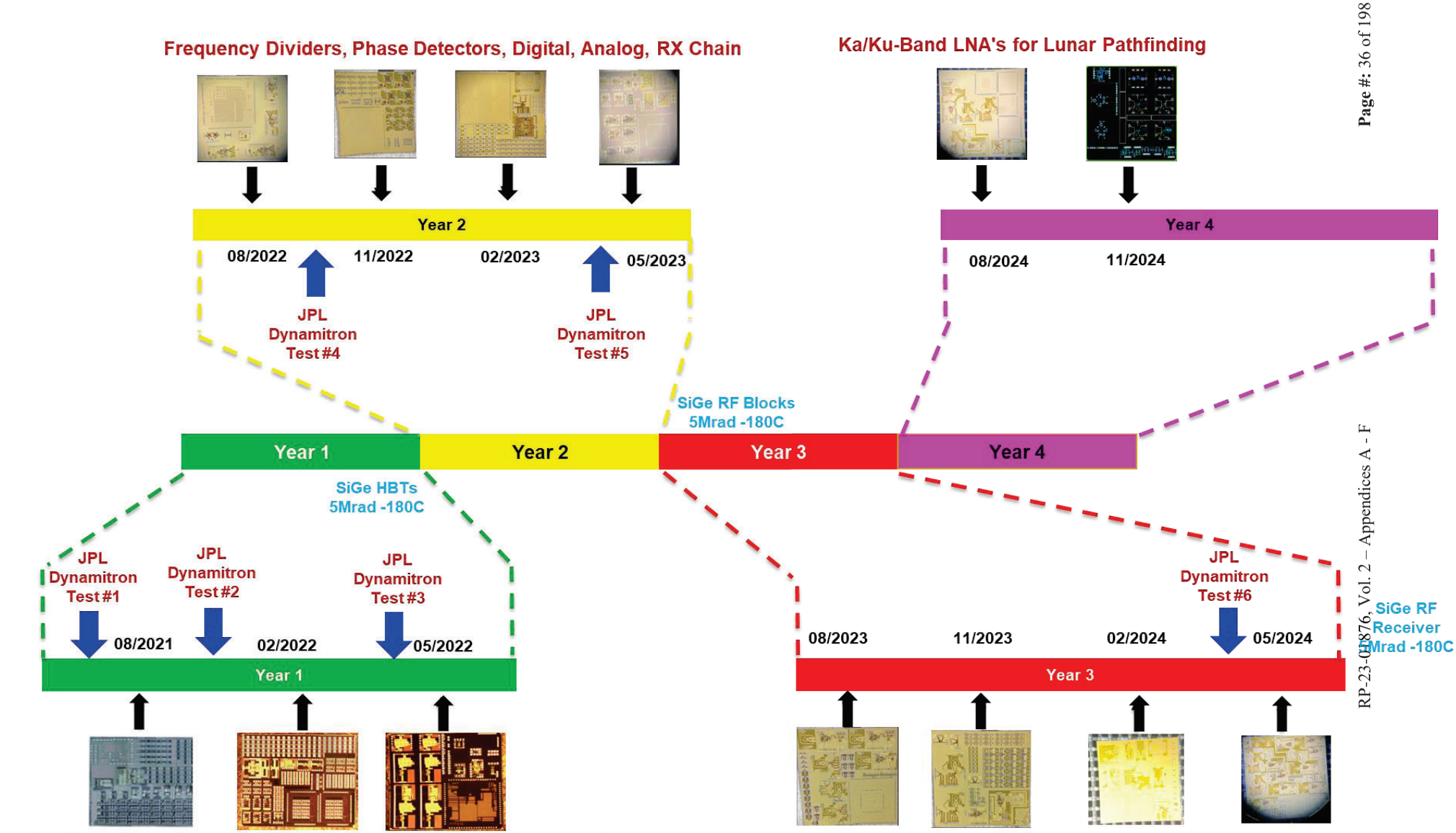
Frequency Dividers, Phase Detectors, Digital, Analog, RX Chain
Ka/Ku-Band LNA's for Lunar Pathfinding
Year 2
08/2022
11/2022
02/2023
05/2023
JPL Dynamitron Test #4
JPL Dynamitron Test #5
Year 4
08/2024
11/2024
SiGe RF Blocks 5Mrad -180C
Year 1
Year 2
Year 3
Year 4
SiGe HBTs 5Mrad -180C
JPL Dynamitron Test #1
JPL Dynamitron Test #2
JPL Dynamitron Test #3
JPL Dynamitron Test #6
08/2021
02/2022
05/2022
08/2023
11/2023
02/2024
05/2024
Year 1
Year 3
SiGe RF Receiver 5Mrad -180C
SiGe HBTs, LNA, VCO, Digital, Analog, Mixer, RX Chain, Ring Oscillators
Phase Locked Loop, RX Chain, Device Structures, IF Amp, Digital, Analog

Appendix D: Electronic Packaging for Cold Environment

D.1 Technology Overview

Electronic packaging provides a means of electrical interconnection between electronic devices and the outside world as well as providing mechanical protection, chemical protection, and thermal dissipation paths. The selection of packaging technologies, processes and materials is dependent upon the electrical, thermal, functional, mechanical, and environmental requirements of the system. System level reliability is determined by the characteristics of each of these elements under use conditions and it is dependent upon packaging design, processing, design life and the acceptance probability of failure. The reliability of these packaging elements can be particularly challenging for cold temperature electronic packaging due to the stresses induced at interfaces resulting from the coefficient of thermal expansion (CTE) differences of materials and the wide temperature difference between the high and low temperature extremes of the application. In practice, these stresses are addressed through the careful selection of materials with closely matched coefficients of thermal expansion as well as mechanical design compensation for the known expansion differences. It should be noted that the zero-stress condition is not room temperature but rather processing temperature. For this reason, low melting point solders are particularly attractive. Strength and modulus of the different materials within the assembly additionally impact the stress within joints. While many well-designed assemblies can withstand limited thermal excursions, repetitive thermal cycling over a large temperature range can lead to fatigue failure of joints and interfaces. For lunar applications, certain applications will require extended operation at very low temperatures while others must withstand multiple thermal cycles over a wide temperature range. Additional challenges may result from the concomitant application of vibration at low temperatures or the intermittent application of high temperatures that modify material properties.

As mentioned above, the selection of viable materials for cold electronic packaging is significantly influenced by the changes in mechanical and thermal behavior of different materials at lower temperatures. The well-known phenomenon of tin pest, in which white β-tin transforms to the structurally weak (powder) α-tin below 13.2 °C (286.2 K), has traditionally been addressed through the addition of Pb. With the emergence of Pb-free solders, alternate alloying elements and processing may be required [Cornelius, Peng, Christian]. With respect to mechanical properties of PbSn alloys, Kostenets showed that pure Sn was brittle at -196 °C (77 K) and –253 °C (20 K), while pure Pb remained ductile at both temperatures. The tensile strength of PbSn alloys was found to increase whereas ductility decreased. Kalish et al. [Kalish, 1948] evaluated the behavior of multiple Sn-alloy at low temperatures delineating the results in numerous plots and metallurgical micro-sectional images. Generally, strength increased with a decrease in temperature prior to embrittlement for Sn and SnPb alloys. Alloys containing more than 10% Pb remained ductile at progressively lower temperatures as the Pb content increased. Ji et al. and Zhou et al. evaluated the fracture mechanisms and constitutive relations of eutectic SnPb at cryogenic temperatures and found that ductile fracture transitioned to brittle fracture between -150 °C (123 K) and -196 °C (77 K) [Ji-2021, Zhou-2024]. Due to the impact of strain rate and microstructure on the mechanical properties of PbSn alloys at cryogenic temperatures, there can be a significant range in published strength values [An]. In and several In alloys are known to maintain ductility to cryogenic temperatures and are often used in low temperature applications for die attach. Compared to pure In, InPb solders offer improved flow properties and

strength for the attachment of parts at cryogenic temperatures. InPb solders remain ductile down to -269 ℃ (4.2 K) [Dunn 2016, Fink]. Humpston et al. provide a brief overview of In solder alloy flow characteristics, properties and failure modes [Humpston-two ref]. Cheng et al. evaluated Cu-In and Ni-In intermetallic growth during low temperature thermal cycling, finding that increased intermetallic thickness resulted in the mechanical behavior of the joint being dominated by the brittle intermetallic [Cheng, 2009-two]. Issues related to In intermetallic formation with thick or unlimited Au have been found [Hlava]. Liu, et al. found electromigration of In solder used in the packaging of high power lasers to result in catastrophic failure [Liu]. The fatigue behavior of In in cryogenic temperatures was evaluated by Chang and McCluskey. Researchers found that In solder fatigue due to creep/stress relaxation was the dominant failure mechanism under temperature cycling, and interfacial fracture of the AuIn intermetallic layer was the dominant failure mechanism below -55 ℃ (218 K) for intermetallic layers greater than 15 μm [Chang 2009]. Dunn et al. [Dunn, Fink] evaluated the modulus, tensile, and ductility behavior of electronic packaging materials at room temperature, -196 ℃ (77 K) (liquid nitrogen), and -268.8 ℃ (4.2 K) (liquid helium) as a function of temperature. Test results presented for SnPb and Sn-based solder alloys, polyimide/epoxy glass fiber and Thermount PCB materials, and various conformal coat polymers. For Sn-based SAC305 (96.5Sn3Ag0.5Cu) solder, the test results indicate that the temperature dependence of Young's modulus and elongation were similar to that of eutectic SnPb solder. Ductility was significantly reduced from room temperature to -268.8 ℃ (4.2 K) and -196℃ (77 K) for both solder alloys, with both transitioning from ductile to brittle fractures. The ultimate tensile strengths of SnPb and SAC305 solders increased significantly from room temperature down to -268.8 ℃ (4.2 K) and then increased moderately from -268.8 ℃ (4.2 K) to -196 ℃ (77 K). For polymers, the glass transition temperature can indicate a significant difference in strength, modulus and thermal expansion. Kirschman et al. reviewed multiple metallic and polymer-based die attach materials for use at cold temperatures and found multiple options for Mars applications. In a review of devices, packaging and materials for cryogenic optoelectronics, Bardalen et al. discussed the difference in cryogenic properties of unfilled and filled polymers. While the fillers reduce the CTE of epoxies and result in a less significant change in modulus at cryogenic temperatures, it can negatively impact the fracture toughness [Bardalen]. Researchers also discussed the impact of die attach thickness on the stress imparted to brittle materials such as Si die, stating that a thicker die attach can result in die cracking. The selected curing point implemented for polymers should be considered carefully. While a higher temperature cure may result in a closer CTE match with the assembled parts, the additional stress imparted due to the added temperature differential can impact the reliability of the assembly.

Select studies have evaluated the package level reliability of systems at cold temperatures. A detailed evaluation on the thermal cycle reliability of chip on board technology for the Mars environment (-120 ℃ (153 K) to 85 ℃ (358 K)) was performed by Tudryn et al. [Tudryn], Shapiro et al. [Shapiro], and Chen et al. [Chen]. The test matrix for these studies included numerous substrates (polyimide, thick film on Al_2O_3, and low temperature cofired ceramics), encapsulants (epoxy, silicone, and parylene), die attachments (epoxy, silicone and In-based solder), wire bonds, and solder joints. Following 1500 thermal cycles from -120 ℃ (253 K) to 85 ℃ (358 K), researchers found the main reliability challenge to be wire bonds encapsulated with rigid, unfilled polymer encapsulants. No failures were observed for the parylene coated wires and no die attach failures were observed. Modeling of the different assemblies found the lowest stress conditions to be with the low temperature cofired ceramic, which exhibited the lowest

CTE of the different substrates. Following the initial experiments, a second set of test structures were developed to evaluate chip on board technologies for power applications. Test structures included passive devices attached using In-based solder as well as large diameter Al wire bonds for power devices. Multiple failures were observed for 20 mil (500 μm) Al wire bonds and no failures for 5 mil (125 μm) Al wire. The higher strength of the larger diameter wire combined with the high coefficient of thermal expansion of Al and resulting stresses were found to be the source of the failure. Additional failures were observed within In-based solder attachment to the passive devices. This was attributed to the device termination. For both die attach and substrate attach, the pattern of the attachment layer can significantly influence the reliability of the assembly. The adhesion of polymers to parts can additionally influence the reliability of the joint. If different polymers are used for the same assembly (e.g., conductive polymers isolated from one another by a non-conductive polymer) the higher strength, higher CTE material may influence the adhesion of the lower strength material. This effect was observed for the attachment of a device designed for solder attachment. Each of these examples highlight the importance of finite element modeling to determine the optimal configuration. However, accurate material properties over the entire temperature regime are critical for such models.

Ghaffarian et al. [Ghaffarian] compared the thermal cycle solder-joint reliability for surface mount technology (SMT) packages including column grid array (CGA) to hand soldered plated through-hole (PTH) ceramic pin grid array (PGA) assemblies cycled under the following conditions (-55 °C to 100 °C (218 K to 373 K), ΔT=155), (-55 °C to 125 °C (218 K to 398 K) ΔT=180), and (-120 °C to 85 °C (153 K to 358K), ΔT=205). Researchers showed that solder joint degradation was dependent on temperature and temperature differential of thermal cycles. For the extreme cold temperature cycle and the extreme stress condition, failure occurred at the braze site, while the failure site remained within the column for the lower stress condition. Suh et al. similarly found that leadless SMD-0.2 packages exhibited cracking susceptibility when cycled below -35 °C (238 K) for metal lid parts and below -65 °C (208 K) for ceramic lid parts [Suh]. Other SMD parts exhibited similar susceptibility for ceramic cracking when attached to boards and cycled. The level of stress transmitted to the part is dependent upon board flexure and thickness. This again points to the importance of accurate mechanical models.

Sivaswamy et al. [Sivaswamy] evaluated SiGe wire bond and flip chip hybrid assemblies in sealed alumina packages for lunar applications, assuming a lunar temperature range of -180 °C (93 K) to 125 °C (398 K). For this assessment, researchers applied up to 400 liquid to liquid thermal shock cycles (-196 °C (77 K) to 125 °C (398 K)). The SiGe die were attached to multilayer Cu thin film conductors with polyimide dielectric using wire bonds (100% In preform attach and AlN substrates) or flip chip (In50Pb50 solder balls and Si or Si_3N_4 substrates) electrical connections. Either wire bonded to AlN substrates (multilayer Cu thin film/polyimide). No underfill was used for the flip chip assemblies. Two premature wirebond failures were observed due to In contamination from die attach and lid failure (resulting in leakage of test liquid). No die or substrate attach (pure In onto Al_2O_3 package) failures were observed and no flip chip attach failures were observed following 400 cycles. Yokoyama et al. evaluated Si die flip chip attached to Si substrates using pure In solder and found no failures following 100 thermal cycles from 30 K to 300 K (-243 °C to 27 °C) [Yokoyama]. Flip chip assemblies of GaAs die attached to Al_2O_3 substrates using SnPb, InSn, InPb, and pure In solder joints were exposed to 300 shock cycles from 77 K to 300 K (-196 °C to 27 °C) by Yamamoto et al. [Yamamoto]. SnPb bumps started to fail at just under 100 cycles, the InPb and InSn solder

bumps both started to fail at about 200 cycles and the pure In bumps did not fail after 300 cycles. Tong et al. demonstrated that Parylene application resulted in a 2x improvement in SnPb flip chip solder joint reliability following thermal cycling from 77 K to 300 K (-196 ℃ to 27 ℃) [Tong].

Hunter et al. [Hunter] and Bolotin et al. [Bolotin] evaluated system in package technologies for Europa applications, with a thermal cycle range of -184 ℃ to 85 ℃ (89 K to 358 K) for 100 thermal cycles. Researchers tested daisy chain ball grid array (BGA) packages with Sn63Pb37 solder balls that were assembled onto polyimide daisy chain test boards with electroless nickel electroless palladium immersion gold (ENEPIG) plating using Sn63Pb37, In50Pb50 and conductive epoxy. Researchers utilized staking and underfill for select assemblies. No failures were observed for BGAs attached with Sn63Pb37. Six of the BGAs attached with In solder (4 of which were the largest package size) failed between 50 to 100 cycles. There was no correlation, positive or negative, with the use of staking or underfill. Researchers suggested that the failure could be due to either immature assembly process or material properties. The BGA assemblies attached with conductive epoxies were still under test at time of publication. Research has shown that the addition of In to Sn based solder can impact the melting point, microstructure and mechanical properties of the joint [Sharif, Luktuke]. Understanding the microstructure of the joint is particularly important for highly cycled low temperature assemblies. As shown by several of the discussed investigations, the volume fraction and mechanical properties of intermetallic compounds can influence the joint as much as the mechanical properties of the parent joint material.

The reliability of commercial plastic packages for lunar applications was investigated by Johnson et al. [Johnson] Researchers studied two quad flat no lead (QFN) packages (a single 6mmx6mm and a single 7mmx7mm) as well as a ceramic quad flat J-lead (CQFJ) package (16mm x 16mm) assembled onto 1.6mm thick single sided Megtron6 Boards (ENIG finish), using eutectic Sn/Pb solder. Micro-D Sub connectors were additionally modified for cryogenic thermal cycling and connected to the boards. The assemblies were cycled from 440 K to 12 K (167 ℃ to -261 ℃) at a ramp rate of 2.85 K per minute (K/min) (2.85 ℃/min). No failures have been observed for the CQFJ packages following 70 cycles. No 7mm x 7mm failures were observed; potential failure within the connector and associated solder connections are being investigated. Solder joint failures were observed for the 6mm x 6mm package. Detailed finite element analyses of the solder joints, including the fillet height, length, and all other parts of the assembly are underway as of writing. Due to the lack of material information on frame, over-mold compound, and the PCB material, researchers are currently performing mechanical testing of these materials to improve the accuracy of the models.

Infrared detectors and superconductor systems represent two applications that require continuous operation at deep cryogenic temperatures. A detailed description of the packaging for a representative heritage infrared focal plan arrays is provided by Bai et al [Bai]. In this example, the detector is attached to the read out integrated circuit using In bump bonds. This hybrid array is in turn attached to a SiC pedestal, which employs a 3-point mount with adjustable spacers/shims for attachment into a mosaic focal plane. Ti mounting feet and molybdenum (or Cu/W) spacer shims are attached to the SiC using threaded Invar inserts that are epoxied into the SiC pedestal. Invar inserts epoxied into the SiC pedestal are used for additional mechanical attachments. Electrical interconnects are provided by Au wire bonds to a rigidflex circuit (Cu traces). Ceramic and tantalum capacitors are also mounted onto the rigidflex (attachment

material is not discussed). The rigidflex circuit also carries the ceramic and tantalum filter capacitors that must be close to the ROIC to achieve lowest noise. The assembly uses 85-pin and 37-pin Airborn Nano-series connectors. This assembly is limited to an upper use temperature of 300 K (27 ℃) and has exhibited long term reliability at cryogenic temperatures. Holmes et al. [Holmes] discussed assembly of support electronics for detector modules. Researchers employed a combination of closely CTE matched interface layers for the Si device and mechanical compensation for higher level assembly. The Si ASIC is mounted onto a Si fanout substrate which is then mounted onto an Invar table support structure. All are mounted using an epoxy with embedded glass beads to control bond thickness. Electrical interconnections are provided by Al wirebonds to the fanout substrate and Au wirebonds to the Arlon85N (Cu conductor) printed wiring board (PWB) with passive pasts and a 91-pin Airborn nanoconnector. The PWB has a hole and slot that is held to the Al chassis with fasteners that constrain vertical movement but allow horizontal movement to accommodate CTE mismatches during the temperature cycle. Although not strictly stated, the work suggests that the passive devices were assembled using Sn63Pb37 solder and standard vapor phase reflow. The design employs several mechanical features to control thermal stresses in the parts. The full assembly was exposed to 5 thermal cycles between 115 K and 323 K (-158 ℃ to 50 ℃), followed by qualification vibration.

D.2 Package Qualification Overview

Qualification of packaging technologies for flight applications over a specified temperature range is most often determined through thermal cycling of the assembly or unit. There is not currently a single thermal cycle life requirement used by all NASA centers. As outlined in SMC-S-016, Air Force Space Command Space and Missile Systems Center Standard Test Requirements for Launch, Upper-Stage and Space Vehicles (5 September 2014), “The thermal cycle test imposes environmental stress screens in an ambient pressure environment to detect flaws in design, parts, processes, and workmanship. The thermal cycle qualification test demonstrates robustness of the electrical and electronic unit design, operation over the design temperature range, and the ability to function during subsequent acceptance testing. The thermal cycle acceptance test demonstrates workmanship integrity and the ability of the unit to survive and operate properly in the maximum expected conditions of its life cycle.” Thermal cycle temperature margins in SMC-S-016 are defined as follows: Acceptance refers to the maximum and minimum predicted temperatures (or a minimum range of -24 to 61 ℃ (249 K to 334 K)), Protoqualification is 5 ℃ (5 K) beyond acceptance (or a minimum range of -29 to 66 ℃ (244 K to 339 K)), and Qualification is 10 ℃ (10 K) beyond (or -34 to 71℃ (239 K to 344 K)).

GSFC-STD-7000B, “General Environmental Verification Standard (GEVS) for GSFC Flight Programs and Projects”, which is used by multiple centers, states that allowable flight temperatures correspond to the individual unit operational and non-operational limits that are based on hardware capability, not thermal analysis predictions, and are as broad as possible. Protoflight is 10 °C (10 K) beyond AFT limits. As an alternative to Protoflight testing of flight hardware, projects can test dedicated hardware to a Qualification limit of 15 ℃ (15 K) above and below AFT and test flight hardware at an Acceptance test level of 5 ℃ (5 K) above and below AFT, assuming that there are no differences between qualification and flight hardware. While the standard recommends testing to these limits for all flight hardware, it recognizes that the full 10 ℃ (10 K) may not be possible with cryogenic hardware (< 120 K) (-153 ℃) for some passive cryogenic systems, in the extreme cryogenic range, due to test setup limitations, and performance testing limitations outside the normal temperature range. While long transitions to cryogenic

temperatures may have structural effects on passive cryogenic hardware, operational conditions must be considered when determining cryogenic system cycling conditions. Individual standards at other NASA centers call out similar test margins for testing of flight hardware; however, the number of cycles is intended to demonstrate workmanship integrity and the ability to operate properly. GEVS separately discusses hardware that is susceptible to thermally induced structural fatigue (such as solar arrays). In this case, thermal cycle testing "shall be performed on prototype hardware. The life test should normally be performed at the worst case (limit level) predicted temperature extremes for a number of thermal cycles corresponding to the required mission life. However, if required by schedule considerations, the test program may be accelerated by increasing the temperature cycle range (and possibly the temperature transition rate) provided that stress analysis shows no unrealistic failure modes are produced by the accelerated testing." Packaging qualification is not discussed separately. MIL-STD-883-1010.9, "Department of Defense Test Method Standard-Environmental Test Method for Microcircuits-Temperature Cycling" outlines temperature ranges and a test methodology for evaluating assemblies.

For the European Space Agency, ECSS-Q-ST-70-61C, "Space product assurance: High reliability assembly for surface mount and through hole connections" discusses the qualification of packaged assemblies in detail. It is worth noting that this standard additionally includes several lessons learned, such as the likelihood of ceramic chip capacitor cracking due to board flexure, that could be very useful to avoid unnecessary failures. The minimum and maximum board temperatures seen by the component in the intended mission profile and ground testing must be covered. The corresponding number of thermal cycles for the on-ground qualification and in-orbit environment shall be covered at least with a safety margin of 2. The modified Coffin-Manson (Norris-Landzberg) equation can be used for the calculation of the equivalent thermal cycles. The coefficients used for the equation defined in the standard are valid for SnPb solder joints as the failure point [ECSS-Q-ST-70-61C]. Equivalent thermal cycles are either to accelerate thermal cycles, reducing the amount of time required for test, or to limit fatigue damage of parts by reducing the temperature range and increasing the number of cycles. JPL design practices require that electronic hardware be capable of "surviving thermal cycle environments that are three times the service life, which includes the planned preflight ground testing environments, worst-case expected mission cycles with worst-case flight temperature excursions, operational self-heating, and power on-off temperature cycling." A package qualification process similar to that applied at JPL is provided by Ghaffarian [Ghaffarian, 2024]. For each of the fatigue susceptible processes discussed, the process begins with determination of total cycles and temperature limits of the application. In certain cases, there are very few extreme cycles and many cycles in a much narrower temperature range. For these cases it is important to break down the number of cycles and the ranges. Mission Environment Application Life (MEAL) for the purposes of electronic packaging is generally concentrated on thermal cycle life [NESC-MEAL].

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Appendix E: Power and Energy Storage Electronics for Cold Environments

E.1 Power System Applications of Cold Electronics

This appendix addresses the topics first discussed in section 7.8. but in greater detail and with supporting figures. The following section covers power options for lunar missions and where cold electronics plays a potential role. We consider the primary power functions, the types of circuits that are required and where use of cold electronics is applicable. For lunar missions, the electrical power systems (EPS) break down to the following functions:

- Power Generation
- Energy Storage
- Main Bus & Power Distribution
- High Power Electric Motor Drives

In this discussion, Power Generation is limited to Photovoltaic Solar arrays. Energy storage is unique in that it involves electrochemistry that is very sensitive to temperature and drives much of the thermal design of space systems. The main bus and power distribution manage spacecraft power by controlling power generation, controlling energy storage charge and discharge functions, and controlling power to the spacecraft loads. Although electric motors are not commonly considered part of an Electric Power System EPS, we are including high power electric motors drive electronics because of the dramatic impact they have on a spacecrafts power quality and stability. In the Artemis program, there is a trend toward high power electric motor drives, to replace traditional hydraulic and mechanically driven mechanisms. Aside from the expanded demand for electrical power these all-electric drives have very high peak power demands and impose voltage transients that have a profound impact on the power architecture. Note that all these electric drives will be exposed to the lunar night and polar environments, and some operate near or in contact with cryogenic propellants. Cold-electronics technologies designed for compatibility with these cold environments will assure reliable operation for lunar missions.

E.1.1 Cold Electronics for Lunar Power Hibernation & Recovery for Lunar Night Survival

For lunar nights, the lunar power hibernation strategy was developed specifically for the low-cost robotic missions of the Commercial Lunar Payload Services (CLPS) program. The current generation of CLPS landers only expect to operate for a single lunar cycle. The reason for such a short operating life is the lack of existing electronics that are proven to physically tolerate and reliably operate at temperatures that may be as cold as -173 °C to -223 °C (100 K to 50 K) (Williams et al, 2017). Hibernation is a strategy that addresses the absence of night power generation and the practical limits of energy storage, when designing a system to survive the extreme cold environment of a 354-hr lunar night (Oeftering, 2022). The normal approach would be to use large batteries sized to power heaters for the duration of the lunar night. Unfortunately, this consumes mass reserved for the payload.

Alternatively, a spacecraft power system can hibernate through the night and reactivate at dawn using a smaller battery and retaining its payload capacity. Note that hibernation is initiated when the battery SOC reaches a lower limit at which point the battery is disconnected and science payloads and communications is lost for the balance of the lunar night. Use of hibernation is

based on the demonstrated ability of COTS Li-ion cells to tolerate a cryogenic freeze-thaw cycle while retaining its charge capacity. Prior work that demonstrated that 18650 cylindrical cells are capable of tolerating the freeze/thaw cycle down to -223 °C (50 K) is further discussed in the Energy Storage section D2.

The hibernation approach is based on the expectation that high quality electronic construction will likely tolerate the lunar night temperatures for a limited number of cycles. However, there is little data available that suggests they are capable of reliably cold starting and operating at those temperatures. Therefore, recovery from hibernation depends on the cold-electronics to manage the recovery process. To illustrate the need for cryo-electronics for a solar powered lunar mission, we will walk through the following lunar hibernation dawn recovery sequence.

Prior to lunar dawn, all systems are unpowered, and the battery is isolated from the main bus. The Spacecraft is at the lowest temperature of the cycle and the battery cells are most likely frozen. The following is the is the hibernation recovery sequence.

- At dawn the solar arrays are illuminated, and the array open circuit voltage will quickly climb.
- An over-voltage protection circuit shunts excess array voltage to keep it within safe limits.
- When the array voltage is stable, the main bus controller (MBC) initializes and regulates the array output.
- The MBC selectively applies power to the Battery Management System (BMS) and supplies power for pre-heater circuits to warm up the battery and avionics.
- The BMS is powered up independently of the battery by the MBC which then monitors the battery temps and voltages and will manage the warming process until cells reach their normal operating temperature
- At battery operating temps, the BMS pre-charges the battery, as needed, to match the main bus voltage.
- When voltages match, the MBC reconnects the battery to stabilize the main bus.
- Once all the avionics reach their operating temperatures, the MBC enables power distribution to power-up the avionics and starts-up the systems.

E.1.2 Lunar Power Generation: Photovoltaic Solar Arrays

Solar Array (photovoltaic) power generation remains the dominant means of generating power because it is light weight, simple design, and proven reliability at a relatively low cost. Solar arrays have been shown to tolerate extremely cold temperatures. Solar array power has a negative temperature coefficient down to approximately -160 °C (113 K) (depending on cell type) therefore, solar cell power output increases as temperature decreases (Boca 2019). Like all semiconductors, electron mobility increases as lower temperatures reduce thermal scattering. However, below -160 °C (113 K) temperature, cell output will begin to diminish due to non-thermal scattering mechanisms along with decreased carrier population due to carrier freezeout.

Note that in 2024 the JAXA SLIM lunar lander successfully survived -170 °C (103 K) and transmitted data after each of three lunar night cycles.

Findings: Photovoltaic Solar Arrays

- Photovoltaic solar arrays are semi-conductors and thus can be expected to have a similar behavior to other electronics when exposed to extremely cold temperatures.

- Solar Array Cryo-Tolerance: The bare devices are tolerant of the extreme cold albeit there is a concern for thermal shock damage. Cold tolerance depends on the packaging materials and methods.
- Solar Array Cryo-Operability: PV cells should cold start and operate at cryo-temperatures. However, further investigation, beyond this assessment, is needed to fully characterize array behavior and limitations for the lunar surface environment.
- Generally, solar array output increases with colder temperatures due to a drop in internal resistance. Cold array open circuit voltage is dramatically greater than a warm array.
- Some form of over-voltage protection is needed to prevent electronics damage and potential arcing.

E.1.3 Main Bus Power: Solar Array Regulation Electronics

Solar arrays can produce excessive power when user loads are light. Solar arrays are composed of PV cells in series called "strings" to achieve a desired voltage. These strings are then combined in parallel to a achieve a desired current output and drive the spacecraft power bus. For space applications, solar array power regulation often employs a direct energy transfer (DET) method involving Sequential Shunt Switching Regulator (S3R). Alternatively, a more modern approach is to use a Maximum Power Point Tracker (MPPT) that involves an intervening converter to help maximize the performance of the arrays while stabilizing the bus voltage.

Solar Array Overvoltage Protection: Normally a spacecraft starts up when battery power is applied. However, in the lunar power hibernation scenario the batteries are frozen and must be isolated from the main bus. As the arrays begin generating power at lunar dawn the main bus relies entirely on power from the arrays without a battery to moderate voltage swings. PV solar arrays tend to generate substantially higher open-circuit voltages at extreme cold temperatures.

Therefore, an over-voltage protection circuit can be employed to shunt excess power to reduce the voltage. The overvoltage protection set-point would be set well above the normal operating voltage, so it does not interfere with normal operations. In hibernation recovery process, this circuit must be capable of operating at lunar dawn temperatures. Once the power regulation circuits are active this protection is no longer needed. This function may be provided by a simple analog circuit tied directly to the main bus.

Findings: Solar Array Overvoltage Protection

- A simple analog circuit can prevent damage from high open circuit voltages.
- Si MOSFETS, or GaN HEMT high-voltage high-power switching parts are available as COTS.

Solar Array Sequential Shunt Switching Regulator

(S3R) is a form of Direct Energy Transfer (DET) where, normally, multiple array strings are connected to main bus and thus deliver power directly (Mohapatra et. al., 2024, İnce et.al., 2023). When the array input exceeds the current demands of the loads, the excess power is shunted and radiated as heat. The S3R depends on an upper voltage setpoint to determine when array strings need to be shunted. Often the strings selected to be shunted are in a fixed sequence. Similarly, as loads exceed the array input and the main bus voltage drops, the shunting sequence is reversed. Normally, batteries connected to the main bus will suppress the switching transients and help stabilize the bus.

To assure batteries are charging while the array is illuminated, the main bus upper set point is above the battery's voltage and thus receives charge current. Whenever all the string outputs are connected, and the array output still falls short due to high current demand, the battery discharge current normally makes up the shortfall.

S3R regulation can be performed by an all-analog circuit. In its default state, all array strings are connected to the main bus. This assures that the power system is self-starting without a battery. It is well suited for mission with hibernation cycles or missions where there is a risk of a dead battery. Further, S3R is not dependent on an operating flight computer.

All parts must also tolerate the voltage and current transients that attend S3R regulator switching. For Power Hibernation the electronic circuits must also be both cryo-tolerant and cryo-operable.

Findings: Sequential Shunt Switching Regulator (S3R)

- S3R Regulator is a form of direct energy transfer and provides a simple solar array regulation scheme may be crafted by simple analog op-amps, voltage reference devices, and various discrete diodes, switching transistors, resistor and capacitors. All need to be capable of a cold start and operate reliably at -223 °C (50 K).

Solar Array Regulation: Maximum Power Point Tracker (MPPT)

This method of array regulation employs a circuit to maximize array output for a given set of array conditions including illumination, temperature, and even adjustments for array degradation effects (Schirone et al. 2024). The array strings are not directly connected to the main bus; power is transferred via an intervening converter circuit that isolates the array from the main bus. The circuit effectively manipulates its load impedance so that the array voltage and current coincides with a "maximum power point" where array output is most efficient. The array output voltage may, however, be above or below the desired main bus voltage thus the DC-DC converter adjusts its output to match the desired main bus voltage. This makes it easier to combine the output of multiple strings while also eliminating the switching transients seen in S3R systems. The MPPT is managed by a digital algorithm that monitors multiple array sensors and calculates the maximum power point.

Findings: Maximum Power Point Tracker Array Regulation

- MPPT is a more complex regulation scheme involving DC-DC conversion stage and circuits that adjust the load impedance on the array output.
- MPPT must provide step-up/step-down converters to maintain main bus voltage as array voltage varies with temperature.
- MPPT requires a digital microcontroller/FPGA to execute the MPPT control algorithm.
- The digital controls must cold start and operate reliably at -223 °C (50 K) and likely requires a custom controller rendered in Si Fully Depleted Silicon on Insulator (FDSOI) CMOS or SiGe.
- Analog instrumentation and low power controls may need some form of temperature compensation to adjust for analog parameter drift with decreasing temperatures and assure a successful cold start.
- Low power LRC passives with low parameter drift at cryo-temperatures are available commercially.

E.1.4 Main Bus Power: Spacecraft Battery Management

Rechargeable batteries allow the spacecraft to store energy and act as a source of power when the power generation is non-functioning (e.g., solar array in the dark). Energy storage also allows power to be supplied when the power demand exceeds the output capability of the power generation. Lithium-Ion batteries are the most common form of energy storage for both robotic and human spacecraft.

Lunar long day-night cycles pose a tough problem for the Solar Array/Battery power architecture. For lunar operations, the mass of the energy storage required to survive an entire 354-hour lunar night is the main problem. The battery must store enough energy to support operations but also provide heater power to keep the battery at a suitable operating temperature. For a small spacecraft to survive the lunar night the battery mass dominates spacecraft mass in relation to a typical payload capacity. For small robotic spacecraft the best option may be to go into power hibernation until lunar dawn, if night lunar operations are not required. Recent testing demonstrated that cylindrical Li-Ion cells that can survive a freeze-thaw cycle. Surprisingly the cells also recover their initial charge capacity when restored to normal temperatures.

Typically, initial spacecraft power up is initiated by connecting the battery power to the main bus often at spacecraft separation. Typically, solar arrays are not yet deployed at initial start-up, so the power system is entirely dependent on the batteries. However, for Lunar surface operations where the spacecraft may be recovering from a hibernation cycle, the start-up will depend on the solar array. (*Discussed further in Lunar Power Hibernation section*)

As noted in the Power Generation section, batteries are essential not only for storing energy to be used when generation is unavailable, but also for stabilizing the main bus. Further, batteries often allow the main bus to support short-term high-power demands that greatly exceed the normal power generation capacity. Most missions have modest power demands with occasional high demand events (e.g., landing, ascent, orbital maneuvers) that can require many times the power of steady state operations. Virtually all missions employ batteries both for energy storage and meeting peak loads. A wider discussion of energy storage capabilities and needs at low temperatures, particularly related to the effect of cell chemistries on low temperature performance, is provided in the Energy Storage section below.

Battery Charge Functions: A main bus control function (often a part of the flight computer) controls the array deployment and then attitude control points arrays at the sun. Array power is managed and matched with the spacecraft power demand. Solar array regulation schemes can manipulate the main bus voltage to assure that batteries are charged when solar illumination is high. For large spacecraft with multiple busses and batteries, dedicated charge/discharge control units are used.

Lithium-Ion batteries have high charge capacity but are notorious for becoming dangerous if charge currents exceed their charge rate limitations (JSC-20793 Rev D). This is particularly true at low temperatures where ion mobility is low and excess charge current results is excessive heating and potential ion damage to the electrodes. Lithium-Ion cells require a constant current and a constant voltage charge schemes at different phases of the charge cycle. For Lunar power hibernation and recovery, the charge controls must be inhibited while the battery cells are frozen at lunar dawn.

Battery Thermal Management Functions: For power hibernation, the BMS is powered independent of the battery by the main bus. Note that at lunar dawn, in the early phases of hibernation recovery, the main bus is operating directly off the solar array alone (not stabilized by a battery), therefore, the BMS power supply will need to tolerate and filter out the main bus power voltage transients.

For Lunar surface applications the BMS functions include battery SOC control, voltage and temperature monitoring, and management of the thermal recovery of the battery following a hibernation cycle (Oeftering 2022).

In daylight, the battery will have varied exposure to the Sun's heating and will likely have hot and cold sides. Keeping the temperatures among the cells (and thus cell voltage) uniform improves performance while minimizing degradation. This implies that the battery BMS must manage the distribution of temperature through multiple heaters that apply heat, as needed, to assure a uniform temperature rise. The BMS will need multiple closed loop temperature controls. Once a normal safe operating temperature is achieved the BMS will need to evaluate the condition of the cells and the overall SOC. If the battery SOC is too low to safely reconnect without disruptive surge currents, then the BMS may perform a pre-charge to match the main bus voltage. When all conditions are met, the BMS signals the MBC to reconnect the battery.

After many cycles, the cells degrade non-uniformly and may exhibit varied cell to cell charge characteristics. This may require the BMS to perform charge balancing to assure all cells are uniformly charged. For fault detection and battery safety, embedded sensors will be needed to detect a failed cell and isolate it to prevent a thermal runaway and the destruction of entire battery and the mission. Note that JSC established that 18650 cells at a SOC of 40% or less will not go into thermal runaway when shorted due to insufficient energy.

The above functional description of the BMS implies a suite of electronic devices. The BMS will require digital controller to execute control algorithms and provide a data link to enable it to exchange data and commands with the Main Bus Controller and coordinate heater power.

Findings: Battery Thermal Management & Charge Control

- Battery management will benefit from a combination of analog and digital electronics capable of a cold start at temperatures as low as -223 °C (50 K).
- Battery Management must be capable of tolerating main bus power input that is not stabilized by a battery.
- Battery charge control must be inhibited until cells are warmed to their normal operating range.
- Battery Management must manage the thermal conditioning to assure that all cells warm up uniformly, particularly at the freeze/thaw point where cells voltages change rapidly.

References

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E.1.5 Main BusPower: Power Distribution

The Main Bus manages the interactions between Power Generation, Energy Storage, and Power Distribution. Power Distribution channelizes power and protects the main bus from load faults. Power Distribution also provides voltage conversion as needed.

Main Bus Controller: In a simple spacecraft the “main bus” connects the Power Generation to the Energy Storage and the Power Distribution elements of the system. The Main Bus requires control circuits that can coordinate the solar array output, assure that main bus power meets the load demands and coordinate the charging of batteries (Oeftering 2022). For lunar missions that need to survive multiple day/night cycles including long hibernation cycles, the main bus electronics are responsible for initial power start-up at lunar dawn, which is also the coldest point of the cycle. In the extreme cold, the main bus electronics will need to manage electric heaters and methodically bring the spacecraft batteries up to an operating temperature. The main bus will need to provide array power to a dedicated BMS that manages the recovery of the batteries SOC.

Findings: Main Bus Controller

- Main Bus Controller is responsible for monitoring Solar Array output and managing the power recovery process when array output is sufficient to support a stable start up.
- Main Bus Control will need a combination of analog and digital electronics capable of a cold start at temperatures as low as -223 °C (50 K) at lunar dawn.
- Main Bus Controller will require LRC passives for analog circuits and transient filters suitable for cryo-temperatures.
- Main Bus Controller must coordinate array regulation and power loads to assure stable operation.
- Main Bus Controller must supply power to the BMS.
- Main Bus Controller must manage power for pre-heating of batteries and avionics for hibernation recovery.
- Main Bus Controller must communicate and process commands and data with Solar Array Regulator, BMS and Flight Computer and power distribution.

Power Distribution Functions (PDU)

Modern power distribution systems involve more than simple On/Off switching of circuits. They are responsible for the organized start-up of avionics and flight computers. They monitor loads and provide status to flight computers. For large power systems step-down voltage conversion is required. In recent years, there is an emphasis on power quality that involves suppressing or tolerating voltage transients, assuring that faults are properly isolated from the main bus and maintain stability margins between power sources and loads (NASA GP 10009, SAE AS5698).

DC-DC Power Converters: For many applications a voltage converter is used to assure that the avionics receives a stable voltage even if the main bus voltage is not stable. For example, if the arrays are in eclipse and the battery voltage drops the converter will automatically boost the voltage to a nominal level. For large systems the main bus voltage may be set at a high voltage and the PDU must step-down high voltage to lower secondary bus voltages suited to powering avionics loads.

The actual converter circuit is composed of a small number of discrete elements including, transistor switches, diodes, capacitors, inductors, and occasional resistors. Some DC-DC converters employ transformers to provide galvanic isolation. Typically, a dedicated microcontroller monitors output feedback and provides PWM control of the switching elements. Most discrete parts are available in materials suited for cryo-operations. It is important the inductor magnetics and capacitors are suited for operation over wide temperature. The control ICs will need to be tested and qualified for cryo-operation.

Power Distribution Switching: The power distribution units employ switching to "channelize" the power so each avionics subsystem can be powered separately. Switching is remotely commanded to facilitate sequential starts, enable load shedding and power balancing. Power Switching usually employs a simple FET switch and a FET driver. Typically controlled by a unit level digital controller that provides ON, OFF, and RESET commands.

Overcurrent Fault Detection and Isolation: The PDU typically provides fault (short) detection and fault isolation (trip) function much like a conventional circuit breaker but with the additional ability to reset on command. The PDU channels Includes overcurrent detection that monitors a current sensor and "Trips" the circuit by overriding the FET Driver input and forcing the FET to turn off (Tripped State) to isolate the faulted load. Note, unlike common fuses and breakers, distribution switching does not rely on thermal mechanisms for the trip function, so the isolation circuit is innately less sensitive to thermal conditions. Modern power distribution units employ automatic "current limiting" as part of fault isolation function.

Current Limiting significantly alters the basic trip function. An overcurrent detection circuit triggers a current limiting circuit that then throttles the current to a preset limit. The current limiting changes the FET transistor from operating in the saturated region "ON" to operating in the linear region. With the current limited, the trip function no longer monitors current but rather monitors the voltage drop across the switch circuit. In case of a severe short-circuit, the voltage-drop will be large and the circuit trips immediately. However, minor over-currents or brief transients that fall within preset current and time limits, the over-current will be tolerated without a trip. Current limiting tends to desensitize the system to transients while keeping fault currents isolated from the main bus and improving overall power quality (NASA GP 10009).

Power distribution employs analog devices that are subject parameter shifts at cryo-temperatures and thus will need to be qualified for cryo-operations.

Findings: Power Distribution

- PDU Power will need to cold start at lunar dawn and manage isolated power channels for avionics and various loads.
- Digital controller is needed to execute start sequence and support load management, and status communications that is suited to cryo-temperature operations.
- Analog instrumentation and circuits must be capable of cold-start and cryo-temperature operation.
- PDUs may need to provide voltage conversion depending on the power architecture.
- PDUs distribute the power via remotely controlled switched channels.
- Analog circuits are needed to provide fault detection and fault isolation to individual channels.
- Analog current limiting circuits help isolate transients and improve spacecraft power quality.
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E.1.5 High-Power Electric Motor Applications

In the latest generation of spacecraft, we have seen a dramatic shift from traditional mechanical and hydraulic power systems to all electric power. Modern rare earth magnets for high torque motors and high-speed electronics for power modulation and regenerative braking makes use of distributed motors feasible. Further we are seeing need for electrically driven cryopumps to combat propellant boil off and enable in space cryogenic propellant storage. There are some cases where electric motors may be used for cryo-propellant engine turbopumps. This implies that motors and their drive electronics will be exposed to cryogenic temperatures.

High Power Electric Actuators: The development of high-power, light-weight rare earth Permanent Magnet Brushless DC (BLDC) motors and fast acting motor control ASICs, enable nearly instantaneous speed and torque control. The advent of very large reusable boosters owes their success to the application of lightweight, very responsive electric actuators for engine thrust vector control (TVC). These same electric actuators will be used to land Artemis Lunar Landers. This places the actuators and drive electronics in the lunar environment.

Propellant Cryo-Cooling Motors: Unlike Apollo, the Artemis Human Landing Systems (HLS) program is using cryogenic propellants for all phases of flight. Artemis is also the first time we expect to see in-space refueling of cryogenic propellants. Tanker spacecraft and in orbiting refueling stations are part of the architecture. The Lunar landers require storing propellants in LEO and lunar orbit for several months. To minimize propellant boil-off losses, we need to combat cryogenic propellant boil-off with Cryo-coolers to chill and condense propellant vapors into liquids. A lander may employ multiple cryocoolers each requiring several kilowatts of power. This requires motor drive electronics in-close proximity to cryo-propellants.

High Power Motor Control Electronics: Motor Control circuit will be a mixed signal device that has digital functions and analog inputs for reading in motor sensors and analog output for controlling the motor drive power switches. A mixed signal microcontroller can process motor hall effect sensor inputs to determine the rotor position and manage the electronic commutation of 3 phase inverter FETs. Motor speed is also extracted from the sensor inputs and the controller manipulates the input voltage via a PWM power converter to manage the motor speed. LRC parts are available in materials that have low sensitivity to cryo-temperatures. Three phase inverters require switching transistors (Si and GaN) that are suited to cryo-temperatures. Motor position and speed feedback involve hall effect sensors and supporting analog instrumentation. These will need to be qualified for cryo-temperatures. Alternatively, there is a “sensorless” approach that uses digital signal processing to extract position and speed from the motors back EMF characteristics without Hall effect sensors. The *Infineon Motix IMD70xA Integrated Motor Controller*, for example, is based on the ARM Cortex-M0 32-bit microcontroller and provides many motor control functions including safety functions that protect the motor and the battery power source (Infineon Technology, 2024).

Regenerative Braking Electronics: Regenerative braking now appears on large spacecraft with electric actuators particularly for TVC applications. In this case, the momentum of the actuator and the mass of the hardware being moved will cause the motor to act as a generator. Regenerative braking puts the power back onto the DC bus. The path to the main bus requires that the outputs of the 3 motor phases be combined and back fed into a bi-directional converter. The intent is to use the regenerative current to return energy to the batteries. Although batteries may have a high output current capability their input or charging current capability is likely

much smaller. This means the regenerative current cannot be absorbed quickly by the battery and the bus voltage spikes. To suppress the overvoltage spikes and capture the energy, a bank of capacitors may be required.

Regenerative Braking uses many of the same parts as the motor drive circuit. To capture the regenerative power may require high-voltage capacitors composed of materials that maintain performance at cryo-temperatures.

Findings: High-Power Actuator Motor Drives

- High power motors and actuators are becoming prevalent for large scale human lunar lander missions,
  - Advanced motor technologies are displacing hydraulic and mechanical power transmission for responsive high-power actuators for thrust vector control.
  - High-power electric turbo-pumps are being considered for pumping cryogenic propellants for lunar lander engines.
  - Electric cryo-coolers for boil-off suppression are in current designs placing electronics in proximity to cryogenic propellants.
  - High-power motors generate high voltage/current transients, particularly if they involve regenerative braking, threaten the stability and power quality of the power bus.
  - Many of these applications are in the cold lunar environment, or operating in proximity to cryo-propellants, or both.
- Digital Motor Microcontroller, or FPGA suited to cryo-temperature applications are needed.
  - Runs a control algorithm processes motor direction, position & speed feedback.
  - Generates 3ph timing and commutation logic and manages PWM motor power.
  - Requires a digital micro-controller rendered in Silicon or Silicon-Germanium
- Analog Motor Control circuits (Hall Effect, feedback signal amps, A/D &D/A, Voltage reference), suited to cryo-temperature applications are needed.
  - 3ph Motor FET Drivers and FET switching.
  - DC-DC PWM motor power regulator (discrete switching transistors & LRC parts).
- High power LC parts for transient filters suitable for cryo-temperature may involve a mix of COTS and custom fabrication.

E.1.6 High Voltage Transient Suppression

Because of the growing use of electric motors used in direct drive actuators, pumps and compressors, we are observing very large voltage transients on power buses. This is further aggravated by the use of regenerative braking that can cause current reversals and voltages spikes.

> Note: The NASA Gateway GP 10009 *Electrical Power Quality Spec* specifically calls out, “Large inductive loads, such as large solenoids, stepper motors, valves, contactors, etc., require voltage transient suppression to control EMC emissions and reverse energy requirements.”

To assure high power quality and stability, high voltage transient suppression devices suited to cryotemperature operations are needed.

Voltage Transient Filters: Transients can be suppressed by adding a series inductor (L) and shunt capacitor (C) components to a power line to attenuate voltage transients by acting as a high

impedance to high frequency transients. LC filters can also remove voltage ripples from switching power supply and converter outputs. There are LC components that will tolerate cryo-temperatures however parameter drift over a wide temperature range must be considered in their selection.

Transient Voltage Suppression TVS devices: Another approach is to use a Transient Voltage Suppression (TVS) device that shunts any transient voltage over a preset limit. These are typically semiconductor diodes devices that normally exhibit a high impedance that do not alter the power circuit's behavior unless an overvoltage occurs.

Zener Diode: Zener diodes are commonly used to clamp a voltage at a specific value. When a reverse bias voltage is applied and reaches a specific breakdown voltage (Zener Voltage) the diode conducts current acting as a voltage regulator. The Zener diode has an unusual temperature coefficient behavior where the coefficient may be positive or negative based on the Zener voltage. This is due to two competing effects, the avalanche effect and the tunneling effect. At Zener voltages above 5V, the avalanche effect dominates with a Positive Temperature Coefficient (V_{BD} Decreases with Decreasing temperature). At Zener voltages below 5V the tunneling effect dominates and thus a Negative Temperature Coefficient (V_{BD} Increases with Decreasing temperature) (Basit, et al, 2013).

TVS Diodes (Transorb): A transorb is similar to a Zener diode and conducts when the breakdown voltage is exceeded. The transorb is specifically designed for fast response and to handle large voltage transients. The temperature sensitivity is assumed to be similar to Zener diodes.

Punch-Through Diode is regarded as better suited for very low voltage applications such as 3-volt or 1-volt circuits than a Zenner diode. Punch Through diodes have a positive temperature coefficient so as temperature decreases their breakdown voltage decreases. Relative to other diode types, the Punch-Through diode breakdown voltage exhibits a low temperature coefficient, thus their temperature characteristics are less sensitive to temperature.

Metal-Oxide Varistor (MOV) is regarded as a non-linear resistor where its nominal high resistance drops when a threshold voltage is exceeded and conducts large currents to suppress a high voltage. They are bi-directional and work for both AC and DC circuits. ZnO based varistor breakdown voltage has a very small dependence on temperature which may make them suitable for cryo-temp operations (Lawless et al,1988).

Findings: High Voltage Transient Suppression

- The increasing use of high-voltage electric motors for direct drive applications requires a wider use of high voltage transient suppression devices.
- LC transient filters components suited for cryo-temperatures will likely require a mix of COTS and custom fabricated components.
- Transient Voltage Suppression is often based on diodes with a set breakdown voltage.
- Zener Diode have a breakdown voltage temperature coefficient and can be positive or negative depending on operating voltage.
- Transorb is similar but designed for fast response and high voltages.
- Metal-Oxide Varistor (MOV) is regarded as a non-linear resistor constructed from ZnO and aimed at high voltages applications with low sensitivity to temperature.
- Many TVS devices have not been fully evaluated for cryotemperature operation.

E.1.7 Analog Electronics for Power Applications at Cryotemperatures

Analog circuits operate in the linear region and are very sensitive to variations in operating parameters due to temperature changes. In fact, many temperature sensors exploit this sensitivity to provide accurate temperature measurements. Analog ICs often have special "temperature compensation" circuits that senses temperature and provide feedback to alter the circuit parameters in a way that counteracts the effects of temperature change. Temperature compensation rarely extends beyond the 125 °C to -55 °C range. Circuits rendered from semiconductors with low sensitivity to temperature such as Silicon-Germanium and Gallium-Nitride should provide reliable cryotemperature performance.

SiGe and GaN devices are not as widely used as silicon and tend to be applied to niche applications. In the case of SiGe, it is used in millimeter wavelength wireless communications device including 5G applications. NASA Space Technology Mission Directorate (STMD) funded work has demonstrated SiGe integrated circuits that are suitable for cryogenic temperature applications. However, custom fabrication is required. STMD funded work has also demonstrated the GaN devices are suitable for operation at cryogenic temperatures. GaN devices are becoming increasingly prevalent in commercial power switching applications and high-power RF applications where it competes with SiC. However, GaN appears to be available only as discrete devices and not as more complex ICs.

Although Si BJTs suffer from carrier freezeout, Si MOSFETs (particularly FDSOI (Fully Depleted Silicon on Insulator) devices) are proving to be effective at cryotemperatures. FDSOI CMOS has the unique ability to use "Back Bias" to adjust gate threshold voltages as a means of temperature compensation. FDSOI CMOS can be used for both digital and analog applications and is already produced as complex IC devices (Cassé et al. 2020, Bensouiah, 2022).

Findings: Analog Electronics for Power Applications at Cryotemperatures

- Si BJT devices are prone to carrier freeze-out and least desirable for cryo-applications.
- Si MOSFETs are more suited to cryo-temperatures than Si BJT devices.
- Si FDSOI CMOS has a back-bias capability that may be useful as a temperature compensation technique. FDSOI is also available as highly integrated devices.
- SiGe semiconductors is preferred for low-power cryo-temperature applications, and they have been produced as analog ICs. However, SiGe will likely require custom fabrication.
- GaN HEMT devices are available as COTS, and are efficient and stable over a wide temperature range and demonstrated to reliably cold-start as low as 10 K.

E.1.8 Digital Electronics for Power Applications at Cryotemperatures

Digital electronics transmit signals as simple binary states which makes them innately less sensitive to variations in signal and to noise. It also makes the circuits less sensitive to low temperature. Generally, bulk CMOS technology is most widely used for microprocessor scale logic. Some versions of the ARM architecture have been produced in FDSOI CMOS.

Findings: Digital Electronics for Power Applications at Cryotemperatures

- Very large-scale silicon digital ICs are widely available as bulk CMOS devices.
- Some COTS digital microcontrollers and FPGAs have demonstrated cryo-temperature operation.

- Si FDSOI CMOS has been shown to work at very low cryotemperatures. It has a back-bias capability that may be useful as a temperature compensation technique. FDSOI is also available as highly integrated devices.
- SiGe digital devices should perform well at cryotemperatures, but they are not widely available and will require custom fabrication.

E.1.9 Mixed Signal Devices for Power Applications at Cryotemperatures.

Many modern microcontrollers and Application Specific Integrated Circuits (ASIC) devices have a digital core with analog features such as, analog-digital and digital-analog converters, signal amplifiers, comparators, voltage references, and load drivers. These are commonly built into a single die. Tests have shown that digital functions work at cryotemperatures while the analog functions in the same circuit may act erratically particularly in cold-start situations. This implies that a COTS mixed signal device may not be suited for cryotemperatures.

Findings: Mixed Signal Devices for Power Applications at Cryotemperatures.

- Mixed signal FDSOI CMOS transistor devices with back bias capability may be effective for cryotemperature devices.
- SiGe digital devices should perform well but the available level of integration is limited.
- SiGe devices will likely require custom fabrication.

E.1.10 Power Switching Transistors for Power Applications at Cryotemperatures

Simple discrete switching elements are often used for ON/OFF switching of high voltages, pulse width power modulation, and motor phase commutation and speed control. They may be driven by either digital or analog circuits by acting through a gate driver circuit. As simple devices there are multiple semiconductor options.

Findings: Power Switching Transistors for Power Applications at Cryotemperatures

- Si Bipolar devices are prone to carrier freeze-out and least desirable for cryo-temperature switching applications.
- Si MOSFETS generally see a modest increase in gate threshold voltage as they approach 50 K and exhibit decreasing breakdown voltage.
- SiGe semiconductors is preferred for cryo-temperatures at low-power but are less suited for high power due to low breakdown voltage.
- Silicon-carbide MOSFETs may not be well suited to cryo-temperatures due to larger increases to on-resistance and gate threshold voltage compared to their silicon counterparts.
- GaN HEMT devices are efficient, suited to high power, stable over a wide temperature range, and demonstrated to reliably cold start as low as 10 K.
- GaN is generally available as COTS discrete devices.

E.1.12 LRC Passives for Power Applications at Cryotemperatures

Cryogenic performance of passive devices (inductors, resistors, and capacitors) is based on the material thermal properties and structure of the device construction.

Findings: LRC Passives for Power Applications at Cryotemperatures

- Metal film and wire wound resistors are insensitive to temperature and are available as COTS.

- Electrolytic capacitors based on liquid electrolyte are not suitable for cryotemperature applications.
- Capacitors using dielectric materials that are relatively insensitive to temperature are available as COTS parts however, they generally have less capacity than electrolytic capacitors.
- Capacitors based on Radiation Crosslinked Acrylate Monomers can maintain high performance at cryogenic temperatures and are available. Requires custom fabrication.
- Air-core inductors will operate at cryotemperatures but have low inductance.
- Nano-crystalline and amorphous inductor cores appear best suited to cryotemperature operation.

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E.2.1 Energy Storage

Energy storage is used on all spacecraft today for several critical functions including load levelling to support peak power demands, and for providing power during eclipse periods or nighttime operations. With the advent of high reliability lithium-ion batteries in 1991 and their first infusion into space applications in 2001, this technology is used in conjunction with solar array and radioisotope thermoelectric generator (RTGs) power generation for all missions today. Battery modules are comprised of multiple cells to provide the overall capacity and voltage required for an application, with the voltage determined by the number of series cells in a string and the overall capacity determined by the number of strings combined in parallel. For example, a 28 volts (V) battery would typically target a string length of eight cells to achieve a voltage range of 24 to 32.8V, since the rated voltage range for most cells is in the 3.0 to 4.1V range.

Multiple strings are then combined to meet the required energy balance for the power system design. The performance of the battery is largely dictated by the cell design and chemistry, which includes the selection of the cathode, anode and electrolyte materials. In particular, these factors have a strong influence on the performance of the cell, particularly with regard to temperature. Cell capacity (Ah) is calculated from the product of discharge duration (hours) and current (Amps) in a constant-current discharge. Discharge rates are often expressed as "C-rates." A C-rate is a measure of the rate at which a battery is discharged relative to its maximum capacity. A 1C rate means that the discharge current will discharge the entire battery in 1 hour, and C/5 rate represents discharging the cell over five hours.

Battery cells are available in two basic formats, prismatic and cylindrical. Early flight batteries were typically comprised of prismatic cells that were custom designed and fabricated for space applications. Some missions, such as Dragonfly and Psyche, still use this format although it is becoming less common. Today, commercial-off-the-shelf (COTS) cylindrical cells have been widely adopted for space applications. These COTS cells are the same type used in many terrestrial electrical vehicles and consumer electronics.

Cylindrical COTS cells are available in a standard form factor that is 18 mm in diameter and 65 mm in height (18650 format) in the 2.8-4.0 Ah range or increasingly in a geometry that is 21 mm in diameter and 70 mm in height (21700 form factor) in the 4.5-5 Ah range. The value of these cells comes in the high reliability offered by the large-scale manufacturing processes used to fabricate them. Also, they contain safety features such positive thermal coefficient and current

interrupt devices, that are lacking in larger prismatic cells. Cells typically undergo an extensive parts screening processes to identify cells that will comprise the flight lot, with flight battery vendors such as ABSL maintaining proprietary protocols for manufacturing flight batteries.

When designing and selecting batteries for operation at low temperatures, it is important to consider if the cells only need to be *survivable* (that is experience a non-operational extended cold soak at temperatures below the rated limited of the cell) or if they need to *operate* (that is charge and discharge) at the low temperature. A further consideration for operation is whether they are both *charged and discharged* at low temperature, or if they are only discharged at low temperature. Recent lab testing [1, 2] as well as flight experience (such as on the JAXA SLIM Lunar Lander and the Mars Ingenuity Helicopter [3]) have clearly demonstrated that COTS cells can undergo multiple freeze-thaw cycles in an non-operational state with little to no impact on performance. The effect of long-term freeze-thaw cycling, freeze-thaw rates, and other such variables on performance have yet to be quantified. Cells modified with low temperature electrolytes can also be charged at higher temperatures (typically > 0 °C) and then discharged at low temperatures with little impact on overall performance (albeit with limitations on the rate capability). This could occur in lunar environments, for example, where charging may occur in full sunlight and then driving may occur in dark or shadowed regions. There is also self-heating of batteries during discharge, which can provide some improved performance in cold environments. Full operation (charging and discharging) of battery cells at low temperature, however, presents significant challenges.

Unlike solid-state devices, lithium-ion batteries feature a liquid electrolyte which serves as a medium to transport ions between the anode and cathode during charging and discharging. Lithium-ions are intercalated and deintercalated from the anode and cathode during these charge/discharge cycles. These transport processes are all thermally activated, and therefore adequate performance depends on maintaining a sufficient temperature to enable a reasonable rate capability. Typically, cells are rated for operation in the -20 °C to +30 °C range at moderate rates (e.g., discharge at C/5) []. Wider temperature operation out to -40 °C and +60 °C can typically be achieved, however, this comes with a limitation in the rate capability when discharging cells at low temperatures, and cycle life if operating for extended periods at the high temperature end.

To maintain operation within the typical cell design limits, significant efforts are directed toward thermal design of the battery in flight applications. An early example of this approach was implemented on the Mars Exploration Rovers, which utilized a thermal enclosure based on aerogel insulation, radioisotope heating units (RHUs) as well as survival heaters. Thermal switches were used to maintain the proper temperature balance at the battery. The battery on the Opportunity Rover survived for 14 years of operation using these thermal design approaches. The Mars Science Laboratory (MSL) and the Mars 2020 rover battery design included titanium bipod standoffs to limit thermal conduction between the rover and the battery, with thermal power provided by heat generated from the Multi-Mission Radioisotope Thermoelectric Generator.

A more recent example is the battery on the Farside Seismic Suite (FSS), which will operate on a commercial lunar lander. The battery temperature in this case is regulated using the Planetary and Lunar Environment Thermal Toolbox Elements (PALETTE) technology [5]. This technology features an inner enclosure isolated by titanium tubes and surrounded by spacer-less multi-layer insulation layers, with an effective emittance e* of < 0.01. In addition to these

features, a passive reverse operation differential-thermal-expansion thermal switch (ROD-TSW) and miniature loop heat pipe (LHP) are installed in series to provide a variable conductance thermal path from the inner enclosure to the outer enclosure. This technology prevents the battery from becoming too hot or cold (i.e., with the allowable flight temperature range being -8ºC to +35ºC), in the extreme lunar environment. This is contrasted with the battery on the Lunar Environmental Monitoring Station (LEMS) seismometer mission, in which the COTS battery will be operated down to -35 °C, thereby limiting its cycle life. Although careful thermal management of batteries is a viable approach, there are situations were minimizing this need results in system benefits. This could be through lower mass and complexity (i.e., no need for thermal loops or thermal isolation hardware) or though low energy (by reducing heater loads).

The performance of cells is largely dictated by the cell chemistry, which in the case of COTS Li-ion technology means the use of a graphite anode, a metal oxide cathode (such as $LiNi_{0.8}Mn_{0.1}Co_{0.1}O_2$) and a lithium-ion salt (such as $LiPF_6$) dissolved in a blend of organic carbonates for the liquid electrolyte. Typical carbonates include ethylene carbonate (EC), propylene carbonate (PC), and dimethyl carbonate (DMC). The capacity and overall performance of the cell is largely dictated by the electrode couple, and it is difficult to deviate from the state-of-the-art technologies that are incorporated into well-manufactured COTS cells. The most logical component to alter to improve wide temperature performance is the electrolyte since it is easier to customize and incorporate into existing cell designs. The conductivity of the electrolyte drops at low temperature due to viscosity effects and reduced transport of the ions, and the performance at low temperature can be improved by altering the electrolyte to minimize the impact of these phenomena.

Liquid electrolyte parts such as methyl propionate (MP) with a melting point of -88 °C and boiling point of +80 °C impart a wider operating range upon the cell. This can allow discharging at low rates (typically 50-100 hour discharge rates) down to temperatures as low as -80 °C, and discharging at moderate rates (C/5) to as low as -60 °C. Cells operating at these temperatures were demonstrated with JPL internal R&TD programs, a DOE-funded project, as well as part of the Europa Lander battery development project, and are undergoing further development with the Army (Figure D-1).

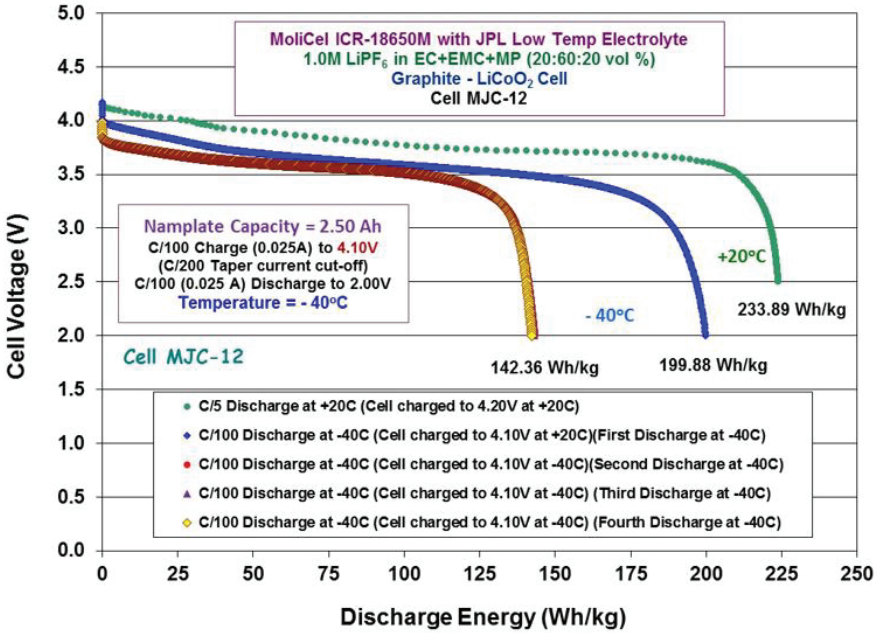

Figure D-1. High specific energy at -40 °C observed when using a low-rate charge and discharge (100 hours) with Moli 18650 cells using modified low temperature electrolytes. No lithium plating observed when charging to 4.10V at -40 °C using low-rate charge [6].

However, charging at low rates still presents significant challenges, due the process of lithium *plating* (Figure D-2). This is a phenomenon whereby the lithium ions in the cell do not properly intercalate into the graphite anode, but rather form metallic particles on the surface of the anode. This phenomenon can lead to a rapid degradation of the cell performance and presents significant reliability and safety challenges since plating can occur in the form of dendrites, which can puncture the polymer separator which isolates the anode and the cathode. This can lead to an internal short within the cell. This can in turn cause the cell to lose charge over time, or in the extreme, lead to rapid internal cell heating and an eventual catastrophic venting of the cell. Different approaches have been investigated for reducing the propensity for plating to occur at low temperatures, such as designing new electrolytes and additives [7].

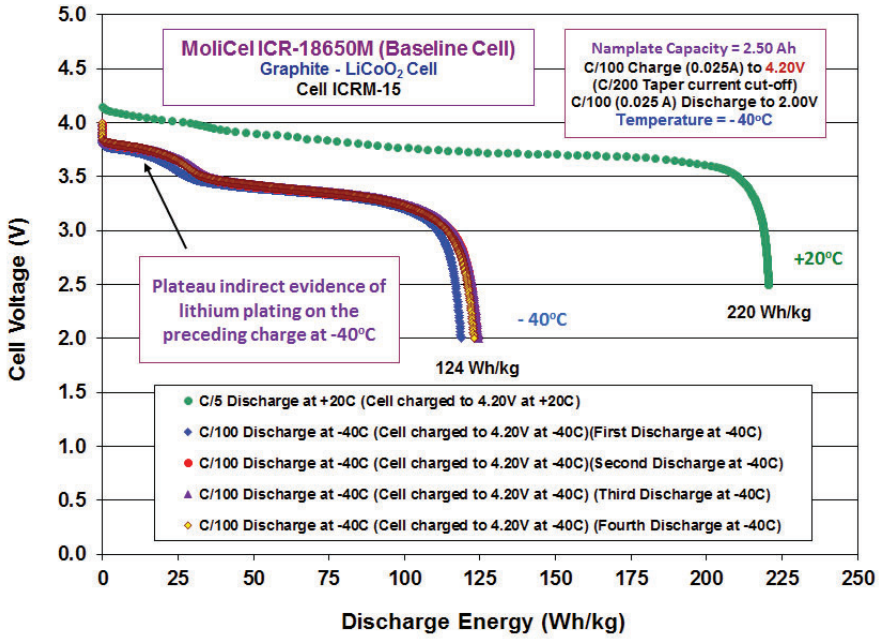

Figure D-2. Baseline Moli 18650 cell with standard electrolyte displaying evidence of plating during low temperature charging The voltage plateau seen at the early stages of discharge is evidence of plating [6]

An alternative approach to using carbonate-based liquid electrolytes is to employ liquified gas electrolytes, supporting operation between -60 and +60 °C. This is typified by the technology demonstrated by South8 Technologies (San Diego, CA) and is based on the use of gases such as 1,1-difuoroethane. These electrolytes can be combined with standard COTS battery cell electrodes, to support discharge down to -60 °C. Charging at temperatures below -20 °C still presents challenges, however (Figure D-3).

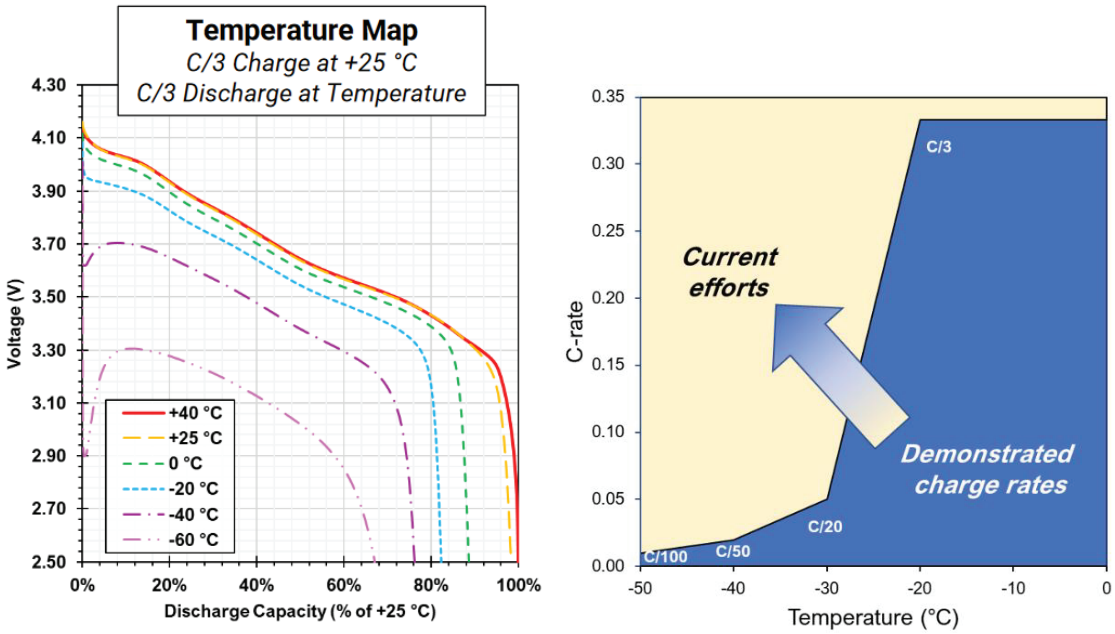

Figure D-3. South8 cells showing discharge down to -60 °C after charging at +25 °C (left)

and map of allowable charge rates and temperature showing charging at only very low rates at <-30 °C is possible (2.7 Ah 18650 cell with graphite anode and NMC811 cathode) [8]

Li-ion cells are currently being manufactured featuring higher silicon content at the anodes, and recent testing indicates that these silicon anodes can support discharging at temperatures as low as -60 °C, offering a higher specific energy relative to cells using pure graphite anodes [9]. Other alternative electrodes based on conversion processes (where the ion transporting current reacts or alloys with the anode instead of intercalating within its layers) have shown promise in extending performance to lower temperatures. These conversion processes lend themselves to more facile kinetics relative to intercalation, potentially enabling higher rates to be achieved at lower temperatures. Research in alternative conversion electrodes has been performed by various groups under the support of NASA Early Career Faculty program, and some of these systems have shown promise. Cells using sodium as an anode in a conversion cell have shown operation as low as -80 °C in prototype laboratory cells, achieving 100 low-rate cycles at -60 °C. More research and development are needed to mature this technology to the level of full operational cells [10].

As indicated, low-rate operation in the -60 to -90 °C range likely represents a limit to battery cells utilizing standard intercalation electrodes and is only possible at very low rates (Figure C-4). Double-layer capacitors or supercapacitors also can offer operation to temperatures < -40 °C [11]. Although the technology offers a much lower specific energy relative to lithium-ion battery technology (5-20 Wh/kg vs. 250-300 Wh/kg), it does not suffer from plating concerns. This is due to the fact that capacity is stored at the electrochemical double-layer, formed at the interface of a liquid electrolyte and two high surface area electrodes. The most critical electrolyte design factors are minimizing the solvent viscosity and achieving a high dielectric constant to avoid the precipitation of the electrolyte salt at low temperatures. It does not depend on thermally activated processes related to intercalation and chemical conversion of the electrodes. Higher rates are also possible relative to Li-ion technology. Cells with modified electrolytes can operate at < -40 °C (Figure D-5). It is possible to combine the two technologies into a battery-supercapacitor hybrid design, to offer advantages of both technologies.

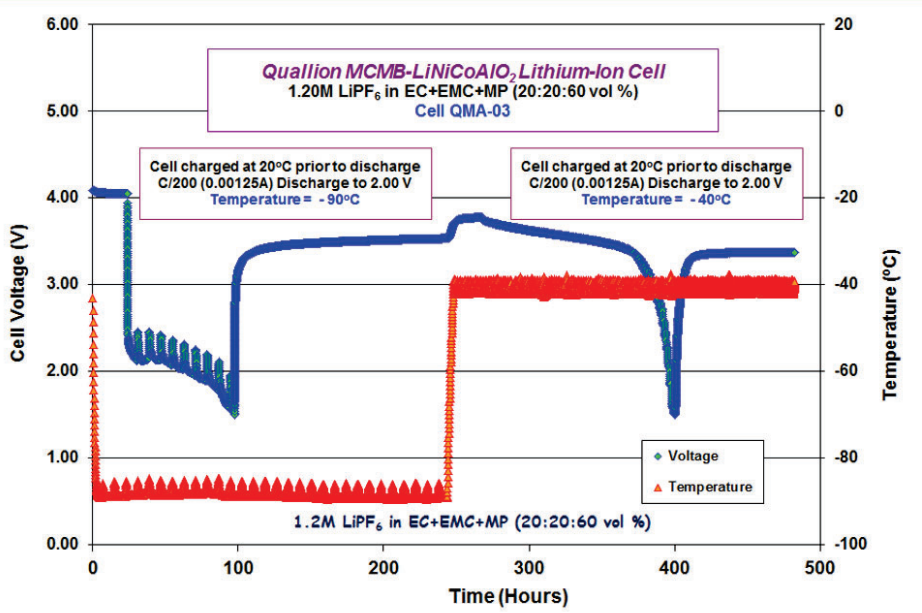

Figure D-4. Quallion BTE cells (0.25 Ah) using modified low temperature electrolyte. Cells were charged at +20 °C and discharged as low as -90 °C over 200 hours [6]

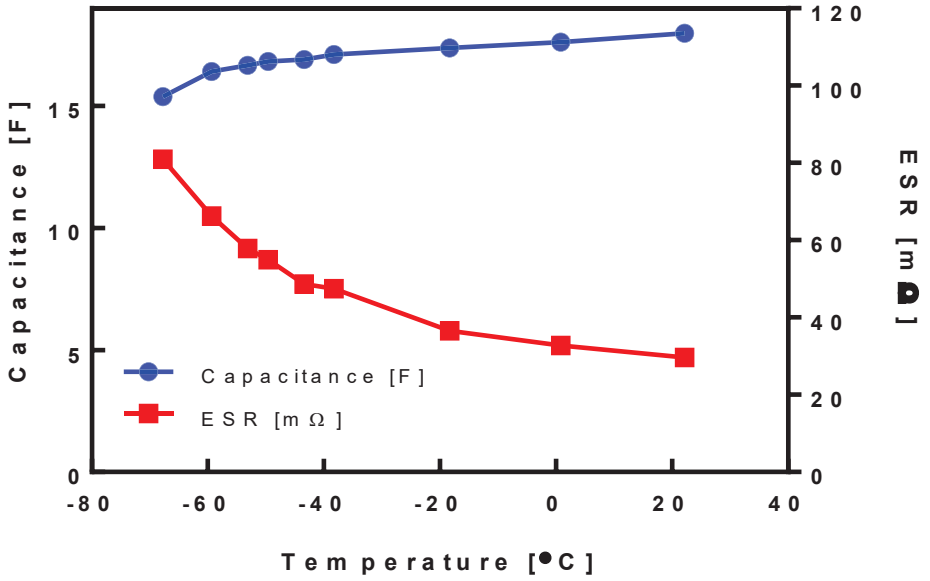

Figure D-5. Custom double-layer capacitor modified for low temperature operation to -70 °C [12]

E.2.2 Energy Storage: Battery Hibernation

The power hibernation approach, discussed earlier, is based on the ability of COTS 18650 Li-ion cells to tolerate a freeze/thaw cycle and recover its initial charge capacity once the cells are returned to their normal operating temperature. The first description of Li-ion cells successfully surviving a freeze/thaw cycle at cryogenic temperatures was reported by the Indian Space

Research Organization (ISRO) in 2018 (Nandini, et al, 2018). This work suggested that a lunar spacecraft could survive the lunar night by hibernating until the next lunar day. In 2019, NASA (GRC) performed some initial tests at LN2 temperatures but had mixed results.

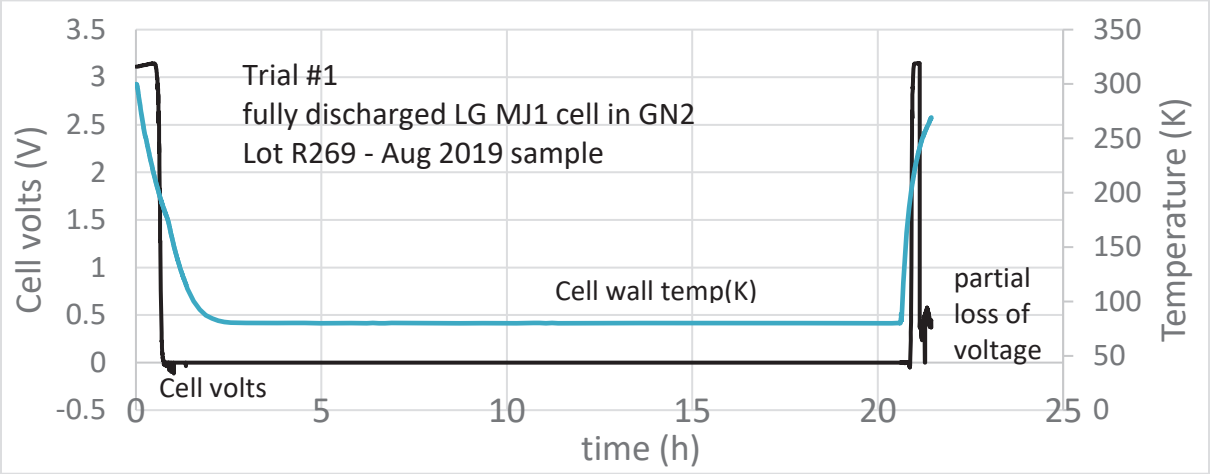

Figure D-6. Preliminary Hibernation Testing in GN2 at 80 K, 1 Atmosphere.

In GRC's preliminary tests with GN2 chilling at 1 atmosphere a cell voltage abruptly drops to zero volts at roughly -70 °C (200 K). This is explained by the electrolyte freezing and thus the electrochemical activity ceases. When the temperatures were raised the cell voltage recovered again at roughly -70 °C (200 K). Some cells recovered without incident however 2 out of 5 experienced a sudden open circuit failure or a ruptured the built-in burst disc. Subsequent examinations revealed that the open circuit was cause by a distortion of the burst disk that caused an internal circuit interruption device (CID) to break the contact due to an internal overpressure. The cell with the ruptured burst disk was a consequence of an internal overpressure event that was high enough to exceed the burst disc limit. A cutaway section of an 18650 cell is shown in Figure D-6 that illustrates the CID, Burst Disc, safety features and seal construction.

Destructive analysis revealed no evidence of an electrical short, no evidence of overheating, and no evidence of a chemistry or electrode damage. An analysis of the cell materials revealed that the polypropylene seal, that also serves to isolate the positive cell cap, will shrink at three times the rate of the other materials. Thus, it was suspected that the cell seals were allowing atmospheric gas to enter the cell when cooled. Since the internal pressure would also become negative relative to the outside atmosphere, outside gases would be drawn into the cell and condense. When warming, the cell's seal would rapidly expand and trap the condensed gas. As temperatures returned to normal the pressure rises and distorts the burst disc enough to trip the CID device and eventually ruptures the burst disk.

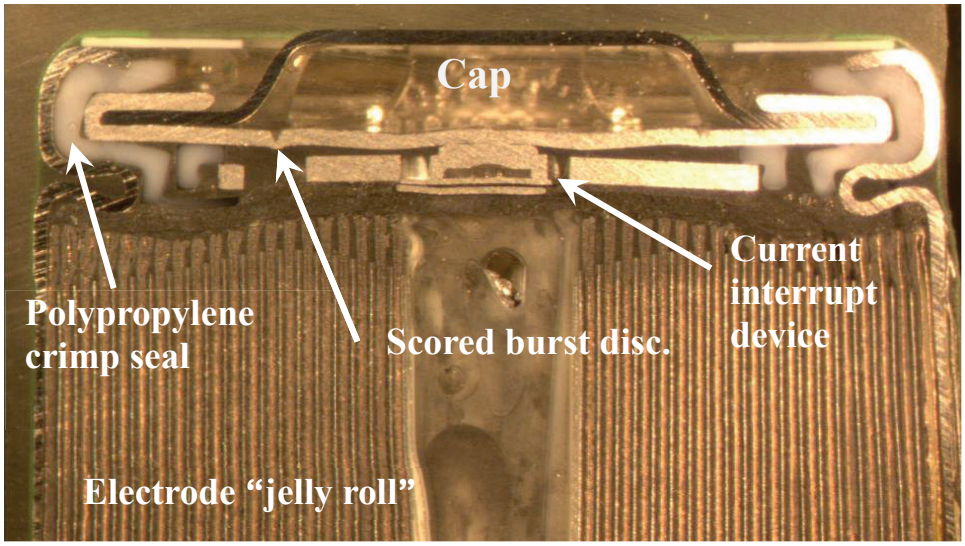

Figure D-7. COTS 18650 Cell Construction Details

GRC further investigated the ISRO work and determined that they had tested in a vacuum rather than in one atmosphere. GRC refined test rig for full vacuum and found that all cells recovered successfully without damage. GRC concluded that for cryogenic tests on COTS 18650 cells, it is essential to perform the tests in a vacuum to maintain a positive internal pressure on the seal. All subsequent freeze/thaw tests in vacuum have since been successful.

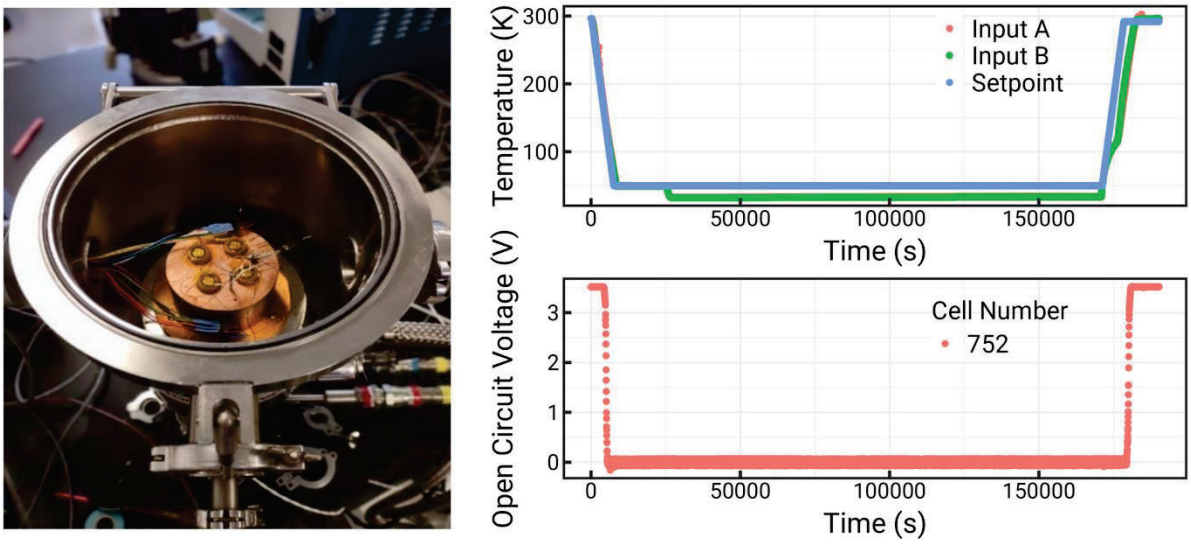

Figure D-8. Hibernation Testing 18650 Cells
in cryocooled vacuum chamber down to -223 °C (50 K)

In 2023 GRC tested cells from NASA's Strategic Reserve Stock of 18650 cells that are normally reserved for space flight missions. Cells were chilled down to 50K and recovered. The observed change in charge capacity after a hibernation cycle ranges from -0.1% to -1.1% (Miller, 2023).

As noted earlier the Mars Helicopter Ingenuity (including six Sony VTC4 18650 Li-on cells) reached temperatures of approximately -80 °C (193 K) and was able to fly upon warming to the allowable flight temperatures for approximately 341 freeze-cycles (sols). This further

demonstrates Li-Ion 18650 cell tolerance of freeze-thaw cycles. Note that the helicopter cells operated at an atmospheric pressure that was less than 1% of Earths atmospheric pressure. Therefore, the cell likely maintained a positive internal pressure against the seals that prevented any significant gas intrusion into the cells.

Recent STMD STRG Early Career Faculty Research ECF22: In 2022 the STMD Space Technology Research Grant-Early Career Faculty Program awarded Prof Zhu of University of California at Santa Barbara and Prof Hatzell of Princeton University research grants to investigate the freeze/thaw characteristics of lithium-ion cells and their long-term effects on cell performance. The PIs are investigating and characterizing the cell Freeze/Thaw process. They are trying to determine how the cells successfully recover from the freeze thaw cycle. Further, they are examining the internal chemistry, electrolyte/electrode interactions, and physical structure of the Li-ion cell using two different techniques.

ECF22 P.I. Prof Zhu is focused on the thermo-mechanical degradation that may limit electrode operating life. She employs Micro-Raman and transient grating spectroscopy (TGS) techniques for analyzing chemical property changes (Zhu 2024). In addition, she uses acoustic time-of-flight (ToF) to detect changes in the material speed of sound as a material transition from liquid to solid.

As the electrolyte freezes, certain constituents freeze first and this causes the portion that does not freeze to be forced into pockets of high concentration that eventually freezes. These concentrations appear to dissolve back into solution when the electrolyte thaws and thus the process is reversible. Further potential structural changes during the freezing process are apparently reversed upon thawing. Prof Zhu tested cells through a series of charge/discharge cycles with and without freeze thaw cycles and did not see a clear difference in capacity change.

ECF22 P.I. Prof Hatzell is using a Synchrotron X-ray computer tomography (XCT) imaging technique to image the freeze thaw process in real time (Hatzell, 2024). She is focused on the cell electrochemistry and changes during the freeze thaw process. A series of 150 charge/discharged cycles (1C) with interleaved freeze thaw cycles indicated very little degradation. X-ray computed tomography imaging of the cells “jelly roll” structure appears normal when 1C was used in combination with freeze-thaw cycles.

However, a distinct degradation of charge capacity is observed if charge/discharge rates are raised to (4C). XCT imaging of cells operated at 4C rates revealed distinct deformation occurred without a freeze/ thaw cycle. Further, cells operated at 4C and then a subjected to freeze/thaw cycle exhibited additional deformation in the inner layers. Suggesting 4C cycles alters the materials making them more prone to distortion during a freeze/thaw cycle.

Both PI’s have independently determined that, assuming a low charge/discharge rate, the Freeze/Thaw cycle barely effects the rate of degradation in charge capacity over many cycles. Testing at varied states-of-charge (SOC) suggests that the SOC does not seem to have a significant effect on charge capacity after freeze/thaw cycles. However, at high charge/discharge rates the cell experiences interior jelly roll degradation that is further aggravated by freeze/thaw cycle.

This suggests that we should expect that COTS cylindrical cell Li-Ion batteries to survive and provide a substantial number of hibernation cycles provided that the charge/discharge rates are limited to 1C. ECF22 work continues through the end of 2025.

GRC is developing a specialized BMS to manage the recovery of Li-Ion batteries coming out of hibernation. This work is done under a STMD Early Career Initiative project named ICE-CHILL

Findings: Energy Storage: Battery Hibernation

- COTS Cylindrical 18650 Li-Ion cells have been demonstrated to survive a freeze/thaw cycle down to -223 °C (50 K) and recover their charge capacity when returned to normal temperatures.
- No discernable degradation of charge capacity was noted.
- COTS cells with polymer seals are unreliable at cryogenic temperatures and risk ingesting and trapping condensed gases and resulting in overpressure damage at normal temperatures if operated in at I atmosphere. Perform hibernation cycles in a vacuum.
- Investigations by two STMD PIs on Li-Ion freeze/thaw behavior confirmed that degradation rate was very small and has a small effect on overall cell life.
- High charge/discharge rates (4C) have a dramatically more pronounced effect than the freeze thaw cycle on cell operating life.
- Provided charge/discharge rates are kept low (1C) we can expect COTS Li-Ion cells to tolerate many hibernation cycles.

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E.3 Gap analyses

Photovoltaic Solar Arrays

- Need full scale solar array test data for operation down to -223 °C (50 K).
- No design rules for solar arrays surviving multiple lunar night cycles.
- Need to assess the risk of thermal shock at lunar dawn.

Solar Array Regulation Electronics

See gaps below,

Solar Array O/C Overvoltage Protection

- No guidelines for handling of high open circuit voltage.

Solar Array Regulation: Sequential Shunt Switching Regulator

- AS3R regulation circuit at spacecraft scale tests at cryo-temperatures is needed.
- Cryo-Temperature characterization test data for shunt regulation parts is needed.

Solar Array Regulation: Maximum Power Point Tracker (MPPT)

- Cryo-Temperature characterization test data for MPPT digital controls, analog and power switching parts is needed at cryo-temperature and capable of a cold start at 50 K.
- A demonstration of MPPT array regulation at spacecraft scale in cryo-temperature and capable of a cold start at 50 K is needed.

Spacecraft BMS Cold Electronics

- Need to demonstrate a charge control and battery management capable of a cold start and operation at 50 K. (Note there is STMD funded work at GRC called "ICE-CHILL" project.)
- Need battery management guidelines for hibernation recovery.

Main Bus Controller

- Would benefit from a microcontroller/FPGA proven to cold start and operate at cryo-temperature down to 50K.
- Need high voltage LRC passives prove to cold start and operate at cryo-temperature down to 50 K.

Power Distribution Unit (PDU)

- Would benefit from a digital microcontroller proven for cryo-temperature operations.
- Need power conversion controls and parts for cryo-temperature operations.
- Need Analog fault detection, fault isolation and current limiting circuits for cryo-temperature operations.

High-Power Electric Motor Applications

- Need Microcontroller for motor control proven for cryo-temperature operations.
- Need 3-phase motor commutation controller suited for cryo-temperature operations.
- Need Hall Effect motor sensors suited for cryo-temperature operations OR an alternative sensor-less scheme (requires digital signal analysis).
- Need DC-DC PWM voltage control circuit suited for cryo-temperature operations.

High Voltage Transient Suppression

- Need characterization data regarding TVS devices, Transorbs, Punch Through Diodes and MOV devices at cryo-temperatures.

Analog Electronics for power applications at cryotemperatures

- There are no published guidelines on analog temperature compensation techniques for cryotemperature applications.
- Silicon-Germanium properties for analog applications at cryogenic temperatures are not well known in industry.
- FDSOI CMOS properties for analog applications for cryogenic temperatures and the potential ability to exploit back bias for temperature compensation is not well known.

Digital Electronics for power applications at cryotemperatures

- Need further evaluations of COTS digital devices for cryo-temperature cold start and operations at 50K. Many have been demonstrated to 77K (LN2) but few have demonstrated cold start at 50K.
- SOI-CMOS properties for digital applications at cryo-temperatures and the potential to exploit back bias for temperature compensation are not well known in industry.

Mixed Signal Devices for power applications at cryotemperatures.

- Need an approach for COTS devices that combine digital and analog circuits at cryo-temperatures.

- Need to determine a semiconductor of choice for mixed signal applications at cryo-temperatures.

Power Switching Transistors for power applications at cryotemperatures

- Gallium-Nitride properties at cryogenic temperatures are not well known in industry.
- Need an approach to qualifying GaN devices for long operating life for cryo-applications.

LRC Passives for power applications at cryotemperatures

- There have been a number of studies that evaluated passive devices at cryotemperatures. Some COTS passives are suitable for cryogenic temperature operations. Some passives require special fabrication. However, no comprehensive guideline of LRC passives properties for power applications at cryotemperatures to 50 K appears in literature.

Energy Storage

- Li-ion batteries can be discharged as low as -60 to -90 °C at low rates, however, they cannot be charged at these temperatures due to issues with Li plating.
- Li-ion cells cannot be discharged at high rates at temperature < -40 °C.
- The effects on battery lifetime during electrical and thermal cycling at low temperatures are not well understood, with inadequate data and models to evaluate the effects of plating on lifetime as well as the mechanical effects of multiple freeze-thaw cycles.
- Traditional intercalation electrodes based on graphite and used for most Li-ion cells today limit performance of cells. Alternative and conversion electrodes based on lithium titanate, silicon, lithium metal or on electrochemically active liquid systems offer approaches for operating < -80 °C and have been recently study but are at TRL < 3 for use in space applications.
- Electrochemical methods for energy storage are unlikely to support adequate energy storage at cryo-genic temperature, due to fundamental limitations with thermally activated processes.

Energy Storage: Power Hibernation

- The polymetric seals on COTS 18650 and similar cells shrink substantially at cryo-temps an allow external atmosphere to enter and become trapped causing a overpressure failure when returned to normal temperatures. An improved cell seal suitable for cryotemperatures is needed.
- Need new procedures and test parameters for hibernation and recovery of Li-Ion batteries.
- There has been no lunar mission explicitly designed to exploit a power hibernation strategy.

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8.

9. R. Tamaki, “Liquified Gas Electrolytes for Next-Generation Batteries for Extreme Cold Temperature Operations,” 2024 Space Power Workshop, Torrance, CA.

10. E.J. Brandon, J.-P. Jones, W. West, M. Smart and H.L. Seong, “Evaluation of Silicon-Anode Cells for Space Applications,” Interagency Power Group Meeting, Austin, TX, Feb. 19-21, 2025.

11. C. Wang, A.C. Thenuwara, J. Luo, J. et al. “Extending the low-temperature operation of sodium metal batteries combining linear and cyclic ether-based electrolyte solutions,” Nat. Commun. 13, 4934 (2022). https://doi.org/10.1038/s41467-022-32606-4

12. E.J. Brandon, W.C. West, M.C. Smart, L.D. Whitcanack and G.A. Plett, “Extending the Low Temperature Operational Limit of Double-layer Capacitors,” *J. Power Sources*, 170, 225 (2007). https://doi.org/10.1016/j.jpowsour.2007.04.001.

13. E.J. Brandon, K.J. Billings, K. B. Chin et al., “Design of Supercapacitors for Wide Temperature Operation,” 2019 Spring Materials Research Society Meeting, Phoenix, AZ.

Appendix F Technical Interchange Meeting and Presentations

Attendees from the following organizations:

Aerospace
AFRL
Alpha Core, Inc.
Amentum
Analog Devices
APL
Aspen Consulting Group
Athens Consulting, LLC
Boeing
CACI International
CoolCAD Electronics
Crane Aerospace and Electronics
DPA Components Int'l
Frequency Management International (FMI)
Frontgrade Technologies
Georgia Tech
Honeybee Robotics
Honeywell
IDA
Infineon Technologies
Intelligent Fiber Optic Systems Corporation (IFOS)
Iris Technology Corporation
Kyocera AVX
Lockheed Martin
MDA
Micron Technology
MIT Lincoln Laboratory
Motiv Space Systems
NASA GSFC/GRC/LaRC/JPL/JSC/MSFC
NASA NEPP/NESC/STMD
Northrop Grumman Corporation
Presidio Components, Inc.
Rensselaer Polytechnic Institute
STMicroelectronics
Tap Engineering
Topline Corporation
TTM Technologies
University of Tennessee
USAF
Vanderbilt University
Viasat
Vishay
Vorago
Voyager Technologies

Background, Goals and Objectives

- The NASA Engineering and Safety Center (NESC) is conducting an assessment of the state of cold capable electronics for future lunar surface missions. The intent is to enable the continuous use of electronics with minimal or no thermal management on missions of up to 20 years in all regions of the lunar surface.
- The scope of the assessment is to capture the state of cold electronics at NASA, academia, and industry, applications and challenges for lunar environments, and gap analyses of desired capabilities vs the state of the art/practice, and provide guidance for cold electronics selection, evaluation and qualification and recommendations for technology advances and follow-on actions to close the gaps. A draft report of the assessment will be shared with attendees a week before the meeting. Attendees are urged to read the report beforehand.
- The goal of the TIM is to capture your feedback with regards to the findings of the report, especially in the areas below:
  - Technologies, new or important studies or data that we missed.
  - Gaps (i.e. requirements vs available capabilities that we missed).
  - Additional recommendations, suggestions, requests, that we missed.

Agenda

Day 1, April 30, 2025

8:00 – 9:00	Sign-in
9:00 – 10:00	Introduction – Y. Chen
10:00 – 11:00	Environment and Architectural Considerations – R. Some
11:00 – 12:00	Custom Electronics – M. Mojarradi
12:00 – 13:00	Lunch
13:00 – 14:00	Power Architecture – R. Oeftering
14:00 – 14:30	Energy Storage – E. Brandon
14:30 – 15:30	COTS/MIL Electronics – J. Yang-Scharlotta
15:30 – 16:00	Passives – R. Oeftering
16:00 – 17:00	Materials & Packaging and Qualification (Packaging) – L. Del Castillo
17:00 – 17:30	Qualification (Electronics) – Y. Chen and J. Yang-Scharlotta
18:30	Dinner

Day 2, May 1, 2025

8:00 – 9:00	Sign-in
9:00 – 12:00	Review and discussion of key findings
12:00 – 13:00	Lunch
13:00 – 15:30	Follow on work concepts & discussions. 15 min each from industry primes and subsystem developers What would you like to see developed and how would it impact your future missions/platforms?
15:30 – 17:30	Follow on work concepts & discussions

15 min each from technology & component developers, academia, government agencies, etc.

What would you like to be funded to do and what are benefits to NASA/missions?

18:00 – 18:15 Wrap up – Y. Chen

Included in this appendix is all of the presentations from the NESC team during the TIM:

NESC Technical Assessment Meeting on Cold Electronics for Lunar Missions
TI-22-01873

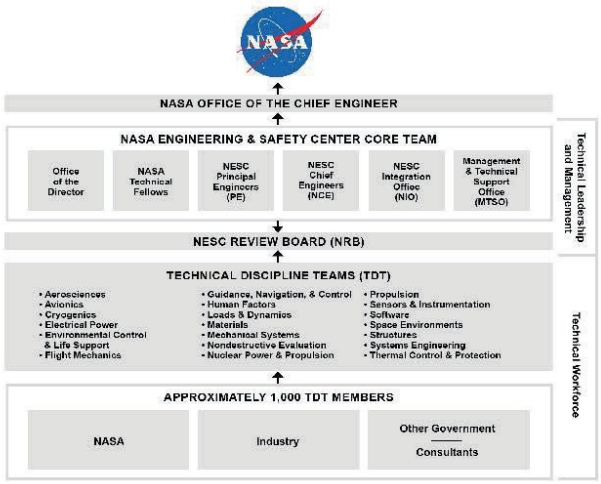
Introduction - NASA Engineering and Safety Center (NESC) Assessment on Cold Electronics for Lunar Mission

George Jackson and Yuan Chen

Section 1.0, 3.0, 5.0, 6.0, 7.0, 7.1

What is the NASA Engineering and Safety Center?

- NASA Engineering and Safety Center – NESC
  - NASA Engineering and Safety Center – NASA
- The NESC was established in July 2003 in response to the observations of the Columbia Accident Investigation Board (CAIB) that specified a need for *independent* technical reviews of NASA's programs.
- "NESC's mission is to perform value-added independent testing, analysis, and assessments of NASA's high-risk projects to ensure safety and mission success."



Outline

- NESC - NASA Engineering and Safety Center
- Assessment request (Section 1.0)
- Assessment plan (Section 5.0)
- NESC assessment team (Section 3.0)
- (Background (Section 6.0))
- Main section (Section 7.0)
- Key definitions (Section 7.1)
- [NESC Findings, Observations and Recommendations (Section 8.0) to be included in NESC final report]
- Why are we here – the purpose of the TIM

Assessment Request (1.0) and Assessment Plan (5.0)

- Dr. Kevin Somervill, Deputy Program Director for Technology Maturation at STMD requested an independent assessment on the state of cold electronics technologies and the gaps for applications and challenges under lunar environments and provide NESC recommendations for cold electronics selection, evaluation, qualification and screening for lunar missions and forward work.
- Assessment plan
  - Capture state of cold electronics at NASA, industry, academia, and its applications and challenges for lunar environments.
  - Perform gap analyses.
  - Provide NESC guidance for cold electronics selection, evaluation, qualification, and screening for lunar missions, and recommendations for technology advances and follow-on actions to close the gaps.
- 6-month task, final report in late May 2025

NESC Assessment Team (3.0) and Topic Areas

- Six technology topic areas + qualification
  - Architecture
  - Custom cold electronics
  - COTS/MIL cold electronics
  - Passives
  - Packaging
  - Power electronics
    - including energy storage for start of art assessment
  - Qualification
    - 3 areas - custom electronics, COTS/MIL electronics and packaging

Name	Discipline	Organization/Host Center
Core Team		
George Jackson	NESC Lead	NESC/GSFC
Yuan Chen	Technical Co-Lead, Electronics, Cryo	NESC/LaRC
Raphael Some	Technical Co-Lead, Electronics, Cryo	JPL
Mohammad Mojarradi	Electronics, Cryo	JPL
Rich Oeftering	Power Architecture, Cryo	GRC
Erik Brandon	Energy Storage	GPL
Linda Del Castillo	Packaging Materials, Cryo	JPL
Jean Yang-Scharlotta	Electronic Component, Cryo	JPL
Consultants		
John Cressler	Electronics - SiGe, Analogue, Digital, Cryo	Georgia Tech
Ben Blalock	CMOS, Analog, Digital, Cryo	University of Tennessee
Wayne Johnson	Electronics - Packaging, Cryo	Auburn University
Zheyu Zhang	GaN, Power, Cryo	Rensselaer Polytechnic Institute
Kristen Boomer	Electrical Power Systems	GSFC
Shri Agarwal	NEPAG, Industry Study	JPL
Peter Majewicz	Reliability and Quality Assurance	GSFC
Susana Douglas	Electrical Systems	GSFC
Business Management		
Becki Hendricks	Program Analyst	MTSO/LaRC
Assessment Support		
Anissa Proctor	Project Coordinator	Barrios/LaRC
Linda Burgess	Planning and Control Analyst	AMA/LaRC
Emily Anthony	Technical Editor	AS&M/LaRC

State of Cold Electronics Technologies and Gap Analysis (7.0)

- Section 7.1 – scope of this assessment and key definitions.
- Section 7.2 – lunar environments.
- Section 7.3 – avionics architectures.
- Section 7.4 – COTS/MIL cold electronics.
- Section 7.5 – custom electronics.
- Section 7.6 – passives.
- Section 7.7 – packaging.
- Section 7.9 – NESC guidance on cold electronics qualification.

Key definitions (Section 7.1) - I

- **Cold Electronics** - Electronic technologies, components, subsystems, and their packaging that are capable of operating in the temperature environments lying below the military specifications of -55 °C to +125 °C. In this assessment, the temperature range is extended to include cryogenic temperatures.
- **Cold Operable Electronics** - The ability of an electronics to operate stably in cryo-temperature conditions and across the entire temperature range in question. Specifically, the ability of a device to successfully "cold-start" when the device temperature is in equilibrium with the cryo-temperature environment is considered the lower limit of the devices cryo-operable range.
- **Cold Tolerant Electronics** - The ability of the electronics to tolerate repeated cycles into cryo-temperatures without significant degradation. It is primarily an issue of packaging materials compatibility at the component and circuit assembly level. "Cold tolerance" is distinctly separate from "cold operation," in that "cold tolerance" does not deal with operation of the electronics in and across the temperature range, but rather their ability to survive if thermal cycled or shocked while in a quiescent or unbiased state.
- **COTS/MIL** - Any commercial, automotive, space, or military off-the-shelf components which are not designed specifically for cold operation below -55 °C.

Agenda – Day 1, April 30th, 2025

8:00 – 9:00	Sign-in
9:00 – 10:00	Introduction – Y. Chen
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11:00 – 12:00	Custom Electronics – M. Mojarradi
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14:00 – 14:30	Energy Storage – E. Brandon
14:30 – 15:30	COTS Components – J. Yang-Scharlotta
15:30 – 16:00	Passives – R. Oeftering
16:00 – 17:00	Materials & Packaging and Qualification (Packaging) – L. Del Castillo
17:00 – 17:30	Qualification (Electronics) – Y. Chen and J. Yang-Scharlotta
18:30	Dinner at TBD, need a head count by lunch time for reservation

Agenda – Day 2, May 1st, 2025

- 8:00 – 9:00 Sign-in
- 9:00 – 12:00 Review and discussion of key findings
- 12:00 – 13:00 Lunch
- 13:00 – 15:00 Follow on work concepts & discussions

  Please be prepared to discuss: 15 min each from industry primes and subsystem developers
  - What would you like to see developed and how would it impact your future missions/platforms?
- 15:00 – 17:30 Follow on work concepts & discussions

  Please be prepared to discuss: 15 min each from technology & component developers, academia, government agencies, etc.
  - What would you like to be funded to do and what are benefits to NASA/missions?
- 17:00 – 17:30 Wrap up – Y. Chen

Why Are we here? Purpose of the TIM

- Share what we have captured.
- Capture your comments and additional needs.
  - Anything we have missed
  - Any comments you would like to provide
  - Any questions you may have
  - Any specific need you may have that we can help or work together to address
  - Anything we can help you to achieve your lunar exploration goals
- Please hold your questions until the end of each presentations.
- .
- There are still 15 min slots for day 2 – if you want to make a presentation, please let us know and we'll fit you in.

NESC Technical Assessment Meeting
Cold Electronics for Lunar Missions
TI-22-01873

7.3 Architectures for Cold Environments

Raphael Some
Jet Propulsion Laboratory, California Institute of Technology
rsome@jpl.nasa.gov

Bottom Line Up Front

- Minimal Work Has Been Done on Cold Capable Architectures
- Hybrid Architectures Are Optimal For Most Applications
  - WEB for Majority of Avionics
  - Relatively Small Subset of Avionics Elements Outside WEB
- An Evolutionary Approach is Optimal and Practical
  - Ecosystem of Cold Operable Electronics
  - A Hybrid Architecture
  - Market Development

Outline

- Definitions
- Historical Data
- Hybrid Architectures are Optimal
- Evolutionary Approach is Most Practical
- Questions

Definitions

- Centralized Architecture: Everything lives in the Warm Electronics Box (WEB)
- Distributed Architecture: No WEB, Everything Lives In The Cold
- Hybrid Architecture: Most Electronics Lives In The WEB
- Hibernation: System Shuts Down At Lunar Night, Powers Up And Resumes Operation At Lunar Daybreak
- Cold: Generally Below -55C, But Of More Interest To This Study are Temperatures Ranges Down To -180C or -223C
- Cold Operational: Able To Operate In The Cold, Including Cold Start
- Cold Tolerant: Able To Reliably Survive Mission Life Thermal Cycles
- Cold Start: Initialize and Operate From Power Off Cold Soak

Historical Data

- Minimal Work Has Been Done On Cold Architectures
  - JPL Cold Rover Studies
  - JPL Thermal Cycle Resistant Electronics (TCRE) Study
  - JPL Distributed Motor Controller Technology Development
  - Motiv CLPS Cold Arm Motor Controller Power Converter
  - GRC CLPS Hibernation Architecture and Power Controller
  - Various Science Instruments, e.g., for IRFPAs, Telescopes
- Similarly, Few Cold Components Have Been Fielded
  - FPA & ROICs
  - Cold Motor Encoder

Hybrid Architectures are Optimal

- Hybrid Architectures
  - Focus On Maximum Benefit For Minimal Cost & Risk
  - Optimum Near-Term Approach For Cold Environments
- Technical Drivers
  - Minimize Thermal Paths Through WEB walls
  - Minimize Noise and EMI/EMC
    - Minimize Small Signal Noise, Transmission Path and Electrical Distance
    - Minimize Large Signal Transmission Path And EMI/C
- Programmatic and Business Drivers
  - Utility Over Large Number of Applications, Platforms, Missions
  - Near Term Return On Investment (ROI)

Evolutionary Approach is Most Practical

- Evolve A Hybrid Architecture
- Start With Low Hanging Fruit
  - Components Readily Available
  - Lowest Cost and Shortest Schedule To Minimum Viable Product (MVP)
  - Easiest To Integrate (Infuse, Accommodate) Into Existing/Coming Platforms
- Enable Key Steps to Optimum Hybrid Architecture
  - Easiest to Most Difficult
  - Most Impactful (Mission Enabling/Highly Enhancing) To Less Impactful (Nice To)

Questions

- What Did We Miss WRT Previous Work In Cold Architectures?
- Is A Hybrid Architecture A Reasonable Way To Proceed Or Should We Go For Broke With A Fully Distributed Approach?
  - Which Subsystems Or Elements Are Candidates for Hybridization?
  - Which Components Are Candidates for Hybridization?
- Is An Evolutionary Approach Optimum Or Should We Go Directly To A Fully Implemented Hybrid Architecture?
  - Which Subsystems or Elements are Candidates for Early Development and Fielding?
  - Which Subsystems or Elements Should Be Left For Later?

NESC Technical Assessment Meeting
Cold Electronics for Lunar Missions
TI-22-01873

7.2 Target Environments

Raphael Some
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Bottom Line Up Front

- There are no agreed upon generic models for avionics thermal environment on the lunar surface
- Regolith temperatures are generally known and used to set worst case bounds
- Several generic design reference missions (DRMs) have been defined by NASA and the community
- For this assessment, worst case regolith temperatures are used for electronics boundary conditions
- For this assessment mission life and mission life thermal cycles were derived from the DRMs

Outline

- Factors of Interest
- Assumptions, Limitations, Concerns
- Regolith Temperatures
- Platforms/Mission Thermal Cycles
- Questions

Factors of Interest

•Thermal environment in the various regions of the lunar surface, e.g., lunar equatorial region, polar regions, permanently shadowed regions (PSR).

•Range, number and type (fast, slow) of thermal cycles experienced in various types of missions, e.g., exploration rover, habitat, ISRU mining and processing.

•Thermal environment experienced by the electronics without an active thermal management system on various types of platforms, e.g., rover, habitat, excavator.

•Thermal Hibernation, a special case in which the electronics is allowed to soak, in a quiescent or unbiased state to the point where in reaches the worst case temperature of the region in question and can then successfully and correctly initialize upon application of power.

Assumptions, Limitations, Concerns

- No Generic or Agreed Upon Thermal Models
- Thermal Environment is Driven by
  - Lack of Atmosphere
  - Solar Irradiance
  - Regolith Thermal Properties
  - Shadow
- Regolith Temperatures are Generally Used for Worst Case Environment
- Electronics Thermal Environment Driven by:
  - External Thermal Environment
  - Platform Thermal Properties
  - Energy I/O

Regolith Temperatures

- Permanently Stationed Platforms:
  - Equatorial -180 to +125C
  - Mid Latitudes -145 to +80C
  - Poles -233C to -193C
  - PSR -233C
- Mobile Platforms:
  - Transport in/out of PSR -233 to -40C
  - Roving broadly, -145 to +120C

Platform/Mission Life Thermal Cycles

- Stationary Platforms
  - 20 Year Mission Life
  - Slow Thermal Cycles
    - Driven by Lunar Day/Night Cycle
    - Slow Ramp Rates
    - Long Dwell Times
    - **2880 Slow Cycles Over Mission Life**
- Mobile Platforms
  - 20 Year Mission Life
  - 28 Excursion Per Lunar Day
  - Slow Thermal Cycles –
    - **2880 Slow Cycles Over Mission Life**
  - Fast Thermal Cycles
    - Driven by Light-Shadow Transitions
    - Fast Ramp Rates (i.e., Thermal Shock)
    - Dwell Times Sufficient to Come to Equilibrium
    - 1 Transition per Excursion Average
    - **6720 Fast Cycles over Mission Life**

Platform/Mission Life Thermal Cycles

- ISRU Mining In Permanently Shadowed Regions (PSRs)
  - 10 Year Mission Life
  - 1 Excursion every 10-12 Hours
  - **6720 Fast Thermal Cycles Over Mission Life**

Questions

- Did We Miss Any Types of Platforms and Mission Types?
- Were Our Thermal Assumptions/Assertions Reasonable?
- Generic, Parameterized Thermal Models:
  - Do Any Exist That The Team Is Not Aware Of?
  - Would Such A Model Be Of Use?
    - Early Thermal Analysis
    - Refined As Mission, Platform, Electronics Designs Mature
  - What Simplifications, Abstractions, Level of Fidelity,... Would Be Useful?
    - Maintain Utility While Simplifying Use
- Should All Future Missions Be Required To Collect Thermal Data Throughout The Mission Life

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TI-22-01873

7.5 Custom ASICS for Low Temp

Mohammad Mojarradi
Jet Propulsion Laboratory, California Institute of Technology
Mohammad.Mojarradi@jpl.nasa.gov

Bottom Line Up Front

- Commercial CMOS, SOI CMOS and SiGe BiCMOS technologies can be used to develop low temperature **fully custom** ASICs:
  - Teledyne used commercial CMOS technology for development of low temperature (-180C) System for Image Digitization, Enhancement, Control And Retrieval (SIDECAR) ASIC for IR detectors
  - For Mars applications JPL used the 0.35 um rad hard SOI CMOS process to develop a quad cold temperature op amp capable of operating to -180C
- NASA has invested in developing design files, low temperature simulation models and a limited cell library for two generations (0.5 um and 90 nm) SiGe BiCMOS technology
- Commercial FDSOI CMOS technology is exhibiting great potential for making cold capable digital CMOS Circuits
- Current process for developing low temperature ASIC is iterative, requires process specific device characterization, design rule and model development

Outline

- Using SiGe Electronics for Lunar Surface Missions
  Professor John Cressler, Georgia Tech
- Lessons learned from 10 years of *design* of low temperature circuits using commercial CMOS, SOI CMOS and SiGe BiCMOS processes
  Professor Ben Blalock, Univ. of Tennessee
- Discussions and gap analysis

Gap Analysis

- Manufacturer supported design tools and simulation models for present and next generation commercial technologies
- Limited and primitive cell library for analog applications
- High-speed low power standard cell library for digital applications
- Circuit topologies addressing the voltage headroom problem at low temperatures (including techniques that use of body bias)
- A rich library of RF building block
- Proven and standardized practices for qual of ASIC's

Using SiGe Electronics for Lunar Surface Missions

John D. Cressler[1], Ben Blalock[2], Linda Del Castillo[3], Rafi Some[3], and Mohammad Mojarradi[3]

[1] School of Electrical and Computer Engineering, Georgia Tech
(404) 894-5161 / cressler@ece.gatech.edu
[2] University of Tennessee, Knoxville
[3] Jet Propulsion Laboratory, California Institute of Technology

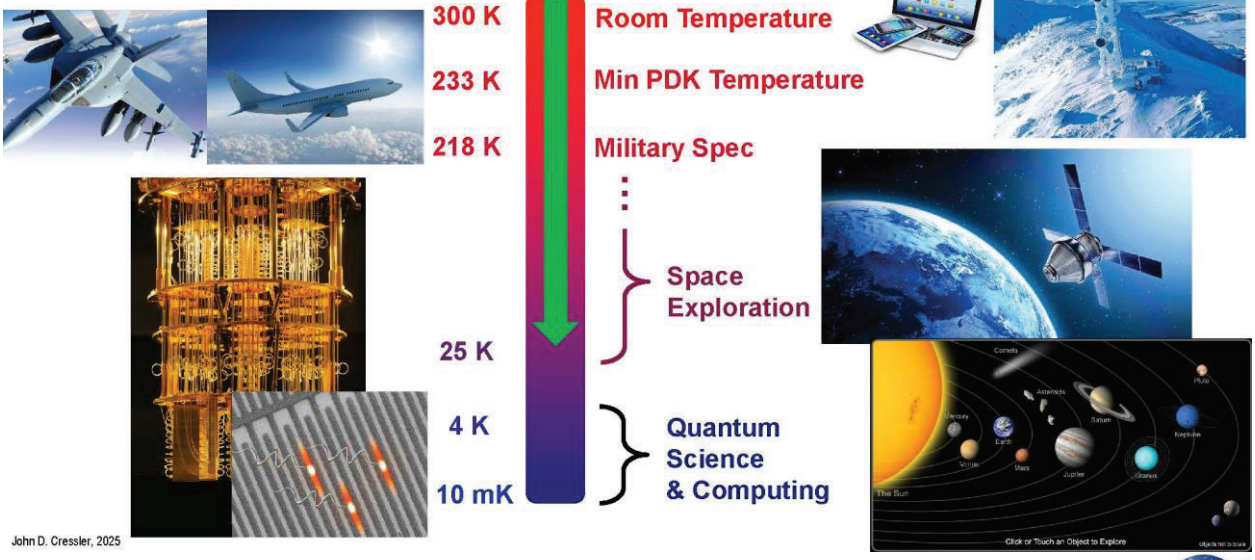
NASA COLDTech Grant # 80NSSC21K1000
Erica Montbach, Project Manager, Ted Wilcox and Jonny Pellish, Technical Liaisons
NASA Engineering and Safety Center (NESC) Cold Electronics Technical Assessment
April 30, 2025

Jet Propulsion Laboratory, California Institute of Technology — Georgia Tech

Outline

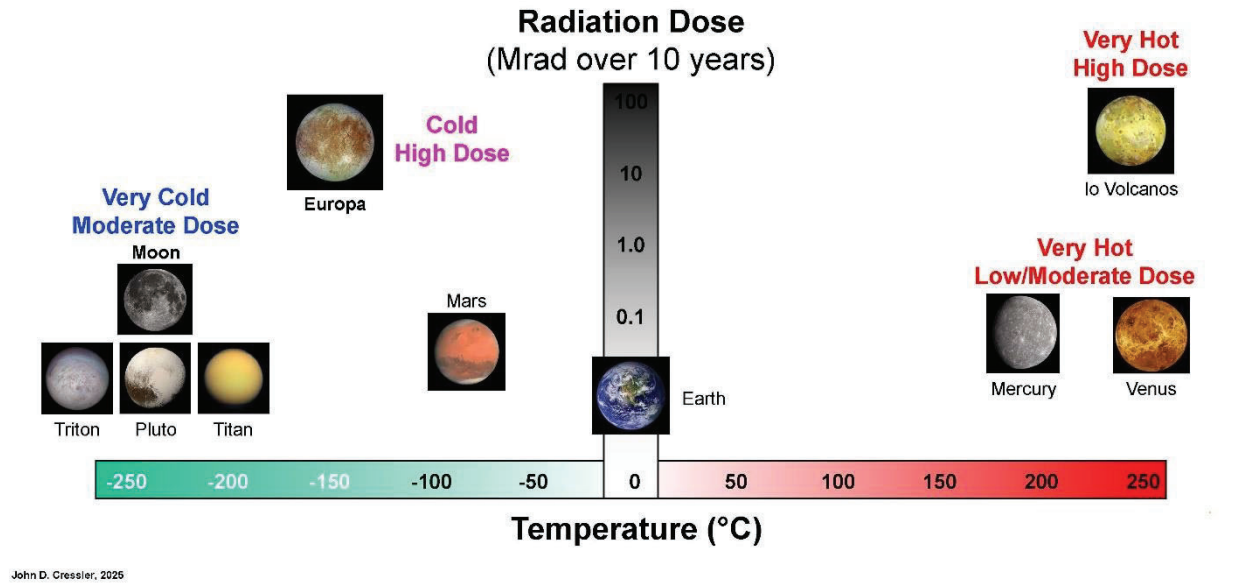
- Motivation
- A SiGe Electronics Primer
- NASA SiGe COLDTech Objectives
- Successes and Challenges
- Insertion Opportunities for Lunar Systems
- Takeaways

Low-Temperature Map of Electronics



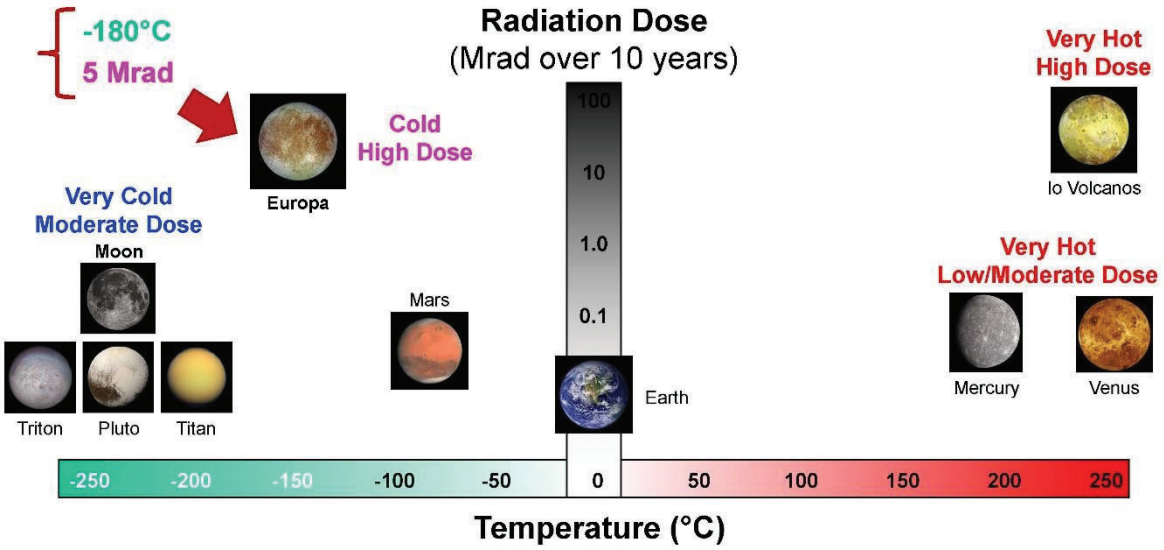
Extreme Environments

NASA COLDTECH: Environmentally-Invariant SiGe Electronics for On-Surface Ocean Worlds



Europa Environment = Worst Case

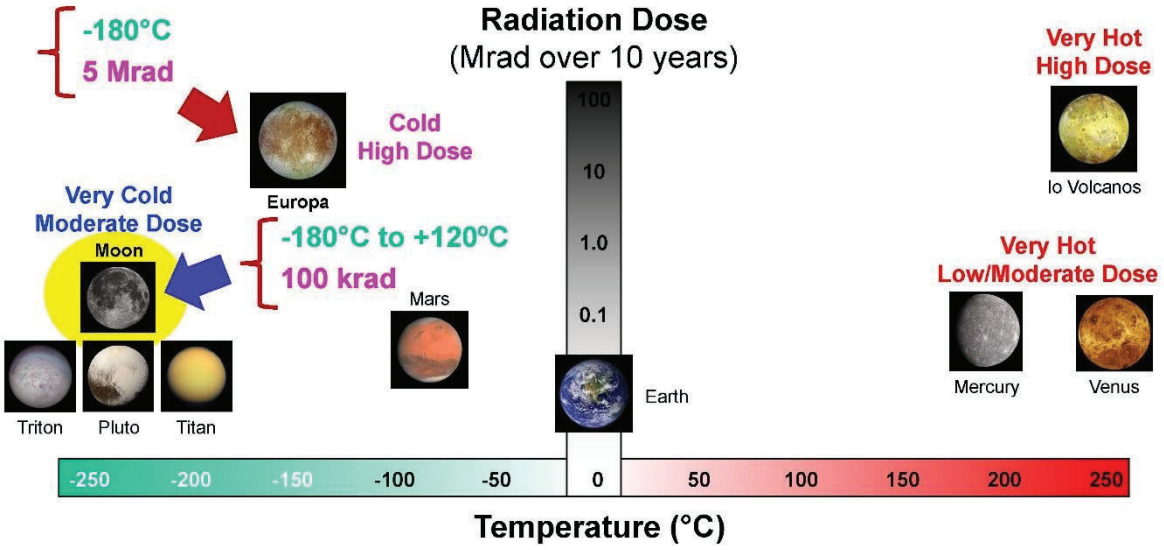
NASA COLDTECH: Environmentally-Invariant SiGe Electronics for On-Surface Ocean Worlds



John D. Cressler, 2025

Europa Environment Enables Lunar Surface

NASA COLDTECH: Environmentally-Invariant SiGe Electronics for On-Surface Ocean Worlds

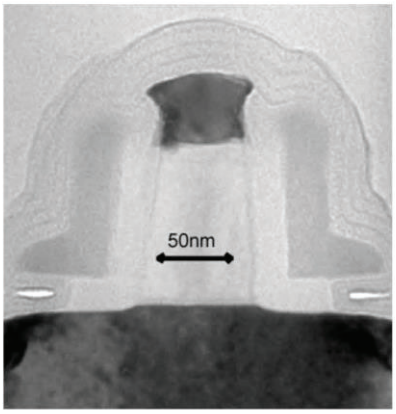


John D. Cressler, 2025

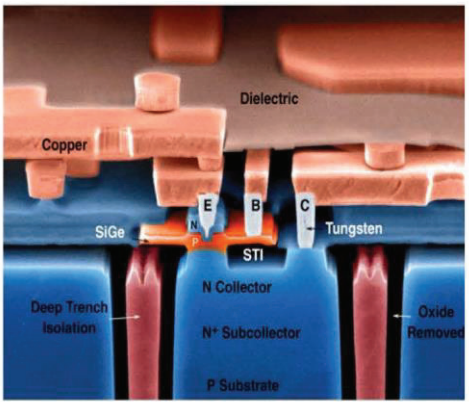
Strain Engineering in Silicon

Georgia Tech

Strained Si CMOS



SiGe HBTs



Strain-Enhanced Si-based Transistors

Close Cousins!

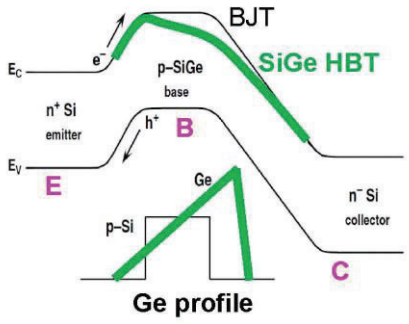
John D. Cressler, 2025

The SiGe HBT in a Nutshell

Georgia Tech

The Idea: Put Graded Ge Layer into the Base of a Si BJT

- smaller base bandgap increases electron injection ($\beta\uparrow$)
- field from graded base bandgap decreases base transit time ($f_T\uparrow$)
- base bandgap grading produces higher Early voltage ($V_A\uparrow$)



Ge profile

$$\left.\frac{\beta_{SiGe}}{\beta_{Si}}\right|_{V_{BE}} \equiv \Xi = \left\{\frac{\tilde{\gamma}\tilde{\eta}\,\Delta E_{g,Ge}(grade)/kT\; e^{\Delta E_{g,Ge}(0)/kT}}{1-e^{-\Delta E_{g,Ge}(grade)/kT}}\right\}$$

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\tilde{\eta}}\frac{kT}{\Delta E_{g,Ge}(grade)}\left\{1-\frac{kT}{\Delta E_{g,Ge}(grade)}\left[1-e^{-\Delta E_{g,Ge}(grade)/kT}\right]\right\}$$

$$\left.\frac{V_{A,SiGe}}{V_{A,Si}}\right|_{V_{BE}} \equiv \Theta \simeq e^{\Delta E_{g,Ge}(grade)/kT}\left[\frac{1-e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT}\right]$$

III-V HBT Properties + Si Processing Maturity!
SiGe = Bandgap Engineering in Si!

John D. Cressler, 2025

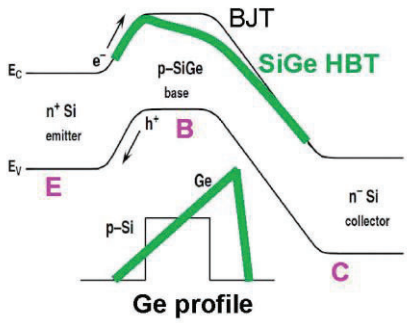
8

The SiGe HBT in a Nutshell

Georgia Tech

The Idea: Put Graded Ge Layer into the Base of a Si BJT

- smaller base bandgap increases electron injection ($\beta\uparrow$)
- field from graded base bandgap decreases base transit time ($f_T\uparrow$)
- base bandgap grading produces higher Early voltage ($V_A\uparrow$)



$$\left.\frac{\beta_{SiGe}}{\beta_{Si}}\right|_{V_{BE}} \equiv \Xi = \left\{\frac{\tilde{\gamma}\tilde{\eta}\,\Delta E_{g,Ge}(grade)/kT\; e^{\Delta E_{g,Ge}(0)/kT}}{1-e^{-\Delta E_{g,Ge}(grade)/kT}}\right\}$$

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\tilde{\eta}}\frac{kT}{\Delta E_{g,Ge}(grade)}\left\{1-\frac{kT}{\Delta E_{g,Ge}(grade)}\left[1-e^{-\Delta E_{g,Ge}(grade)/kT}\right]\right\}$$

$$\left.\frac{V_{A,SiGe}}{V_{A,Si}}\right|_{V_{BE}} \equiv \Theta \simeq e^{\Delta E_{g,Ge}(grade)/kT}\left[\frac{1-e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT}\right]$$

III-V HBT Properties + Si Processing Maturity!
SiGe = Bandgap Engineering in Si!

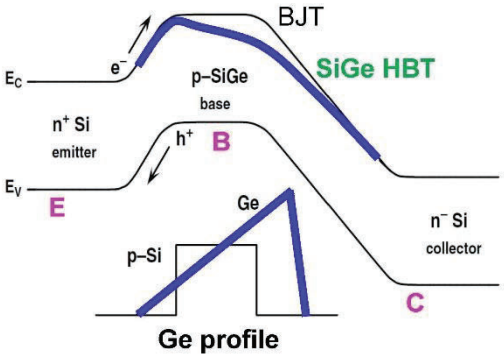
John D. Cressler, 2025

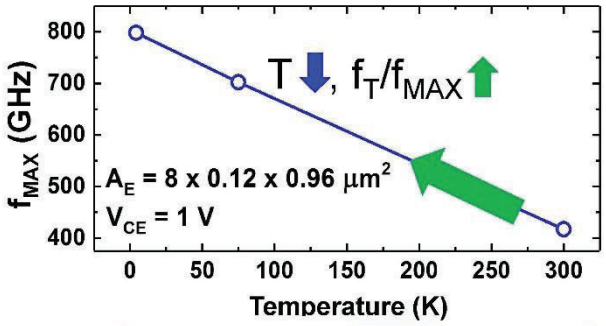
9

SiGe HBTs Naturally Suited for Cryo-T

NASA COLDTECH: Environmentally-Invariant SiGe Electronics for On-Surface Ocean Worlds

- **SiGe HBTs Achieve Better Performance With Cooling**
  - drift field more effective at lower T → shorter transit time
  - as T↓, f_T/f_{MAX}↑ g_m↑ current gain↑, noise↓
- **Demonstrated f_{MAX}: 800 GHz at 4.2 K (417 GHz at 300 K) - Operable to 70 mK**





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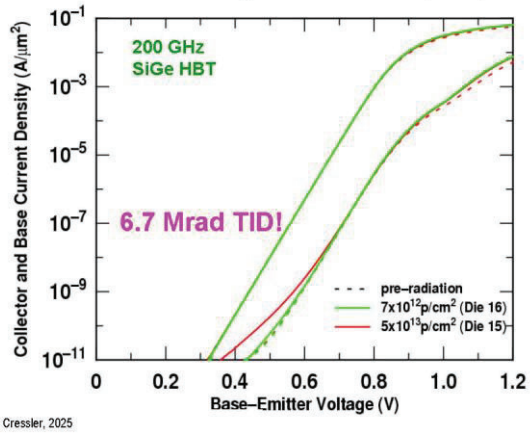
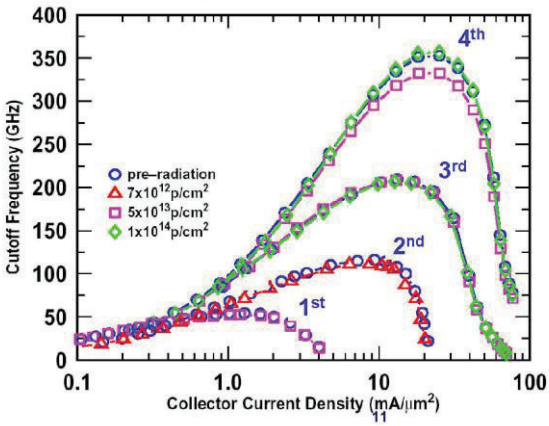
Total-Ionizing Dose (TID) Tolerance

- **Multi-Mrad Total Dose Hardness (with no intentional hardening!)**
  - ionization + displacement damage very minimal over T; no ELDRS!
- **Radiation Hardness Due to Epitaxial Base Structure (not Ge)**
  - thin emitter-base spacer + heavily doped extrinsic base + very thin base

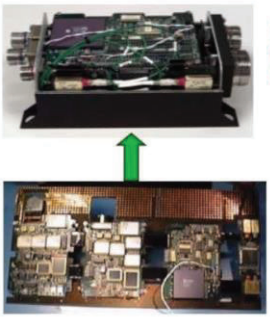




Outline

- Motivation
- A SiGe Electronics Primer
- **NASA SiGe COLDTech Objectives**
- **Successes and Challenges**
- **Insertion Opportunities for Lunar Sytems**
- **Takeaways**

Legacy: Lunar SiGe ETDP (5 years, $12M)



The X-33 Remote Health Unit, circa 1998

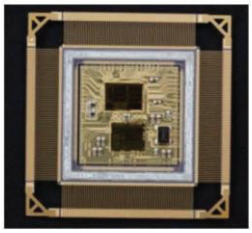
The ETDP Remote Electronics Unit, circa 2009

REU in connector housing!

Analog front end die

Digital control die

Conceptual integrated REU system-on-chip SiGe BiCMOS die



Project Ended 2010

Specifications

- 5" x 3" x 6.75" = 101 in^3
- 11 kg
- 17 Watts
- -55°C to +125°C

Goals

- 1.5" x 1.5" x 0.5" = 1.1 in^3 **(100x)**
- < 1 kg **(10x)**
- < 2 Watts **(10x)**
- **-180°C to +125°C, rad tolerant**

Used IBM SiGe 5AM Technology (1st generation)

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SiGe COLDTech Project Objectives (Europa)

NASA COLDTECH: Environmentally-Invariant SiGe Electronics for On-Surface Ocean Worlds

- **Demonstrate that SiGe Technology Can Satisfy NASA's Need for a Diverse Set of Electronics Infrastructure (RF + Analog + Digital) for Ocean Worlds Surface Missions** (and which will then span all of NASA's solar system needs; e.g. lunar)

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- **Develop a Library of SiGe Analog / RF / Digital Building Blocks for NASA Use:**
  - X-band RF receiver for on-surface communication links
  - analog bias circuits and amplifiers
  - digital library for synthesis
  - SRAM for memory
  - synthesized legacy generalized memory controller as a Pathfinder

No Warm Box or Shielding

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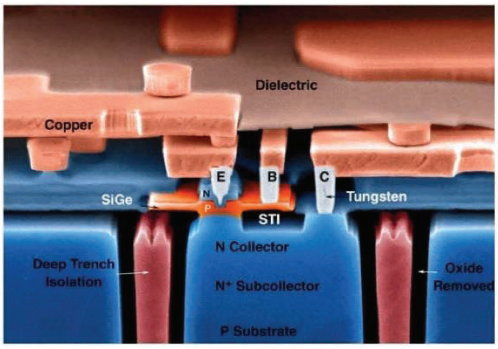
  No Warm Box or Shielding
- **Develop Design Ecosystem for NASA Use**
  - transistor models and simulation test benches
  - library documentation + design files
  - best practices for testing/validation

SiGe BiCMOS Technology

- **GlobalFoundries 9HP Technology Provides 90 nm SiGe HBTs and CMOS**
  - SiGe HBT f_T / f_{max} = 300 / 350 GHz, BV_{CEO} = 1.7 V
  - Process Design Kit (PDK): All the Bells and Whistles!
  - Cu BEOL (topside thick Al) metallization + Tons of Rs and Cs for Design



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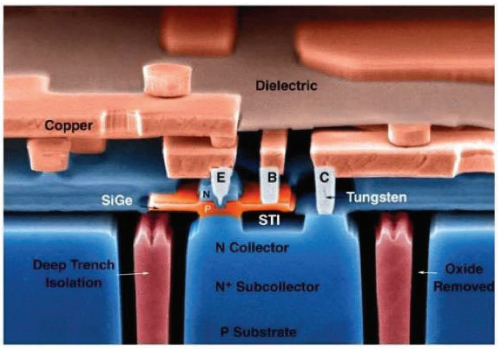
  - Process Design Kit (PDK): All the Bells and Whistles!
  - Cu BEOL (topside thick Al) metallization + Tons of Rs and Cs for Design
- **Unique Properties of SiGe HBTs**
  - Excels at RF and Analog
  - High Gain, High Speed, and Low Noise
  - Naturally Suited for Cryo-Temperatures
  - Can Handle 5 Mrad TID Radiation, as Built!
  - SEL Hard, as Built!
  - **Integrated Systems with on-Die CMOS**
  - **SiGe for Analog/RF + CMOS for control**
  - Available as MPW (cost effective)
  - Long Duration SiGe Platform



SiGe COLDTech Project Objectives (Europa)

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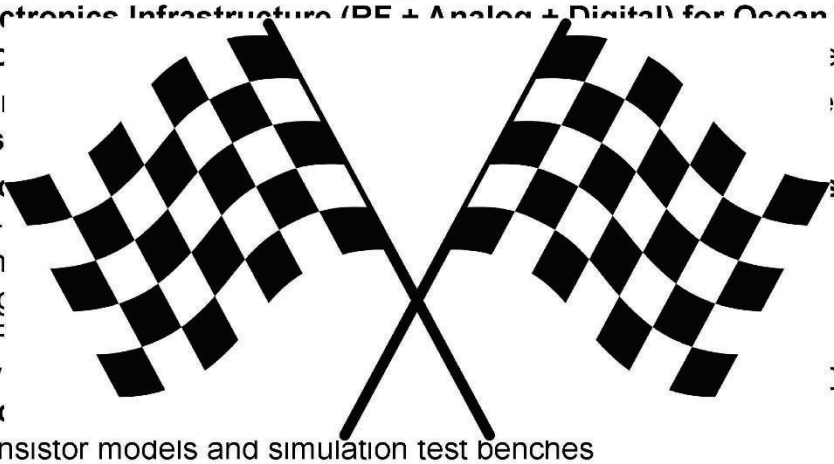
- **Demo** …**rature + Intens**
- **Devel** …**s for NASA Use:**
  - X-
  - an
  - dig
  - SF
  - sy …nder

No Warm Box or Shielding



- **Devel**
  - transistor models and simulation test benches
  - library documentation + design files
  - best practices for JPL Dynamitron

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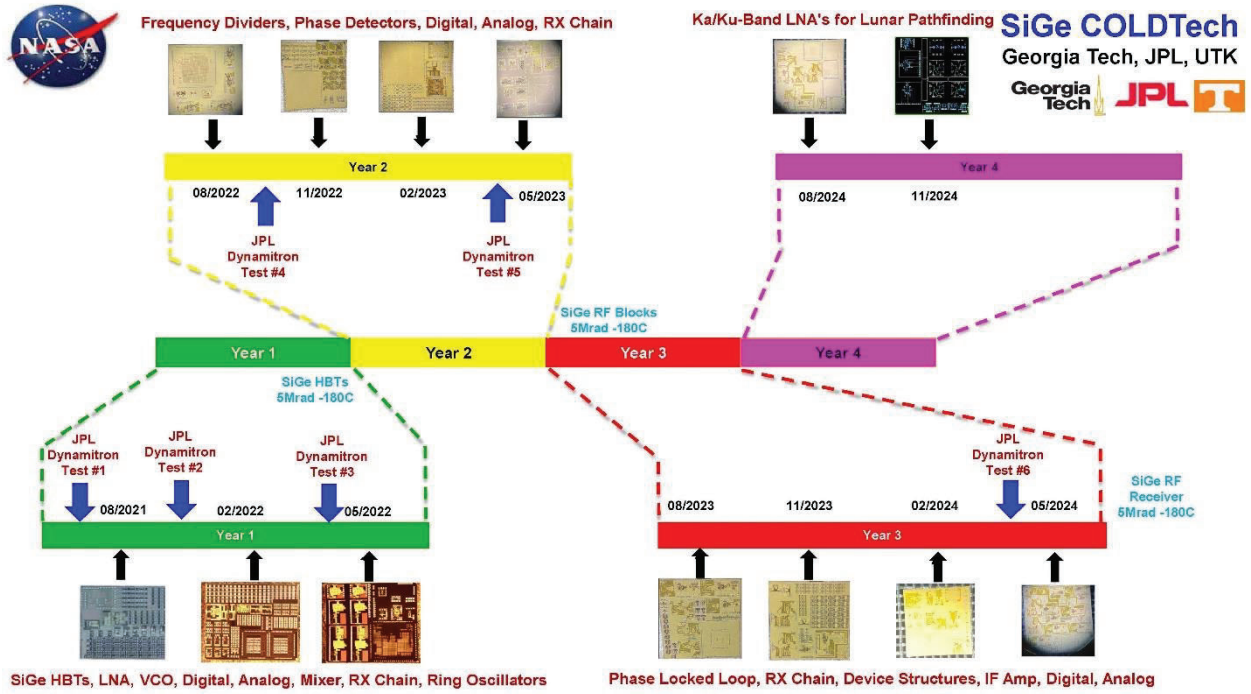
Leveraging Fabrication Space (GF SiGe 9HP)

Georgia Tech

- **13 Different MPW Tapeouts over 4 Years! (Multi-$M leveraging)**

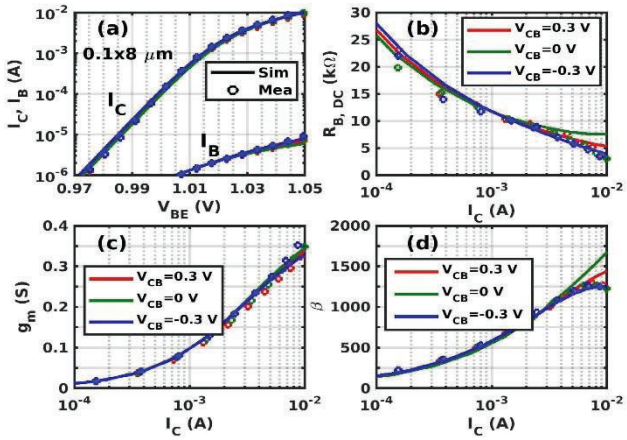
- **SiGe HBTs**
- **Modeling Structures**
- **Reliability Structures**
- **RF Building Blocks + Integrated X-band RF Receiver**
- **Analog Building Blocks**
- **Digital ECL**
- **Synthesized Memory Controller for M0 Microcontroller**
- **Ka/Ku LNAs for Lunar Apps**
- **Much More . . .**

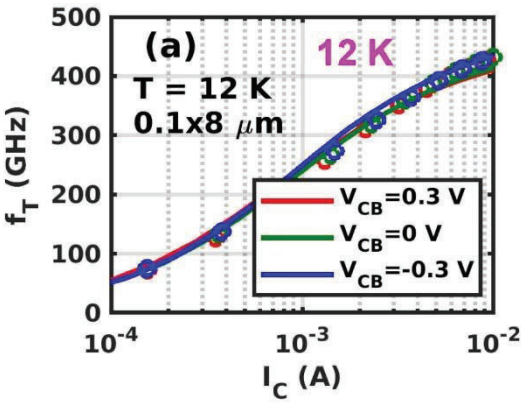


Large-Signal Cryo-T Compact Models

NASA COLDTECH: Environmentally-Invariant SiGe Electronics for On-Surface Ocean Worlds

- **Simple, Converges at Cryo-T, Well-Calibrated to Data (HICUM)**





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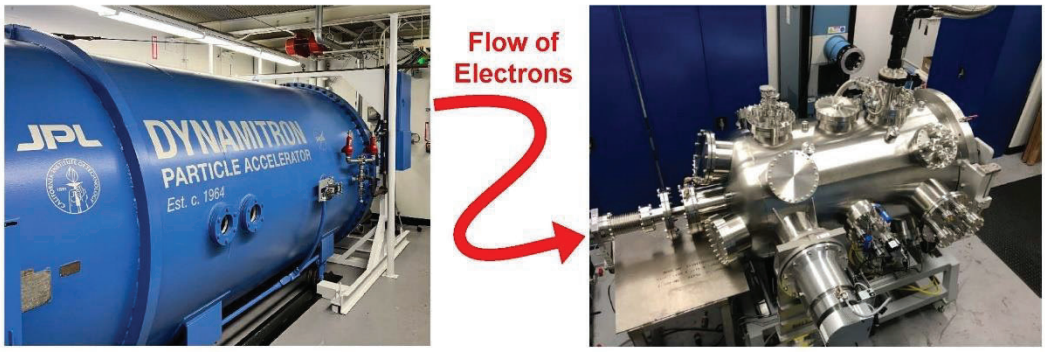
Dynamitron Particle Accelerator (JPL)

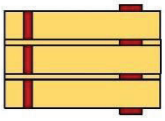
- **Electron Particle Accelerator to Emulate Europa Surface**
  - temperature range from -200°C to 100°C
  - large variety in dose rate: 24.5 to 1225 rad[Si]/s
  - allows for repeatable, in-situ electron exposure at cryogenic temperatures



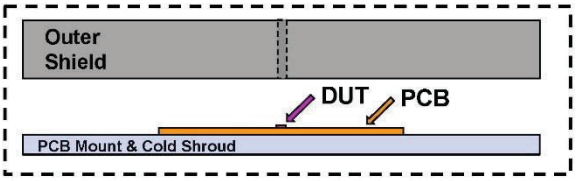
Mitigation of iESD

Idea:
1. All RF Traces with Via Fencing
2. Thinner PCB
3. More Shielding

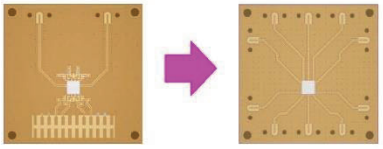
→ iESD Amplitude ↓ Parts Survive to Dose ↑



Thin PCB

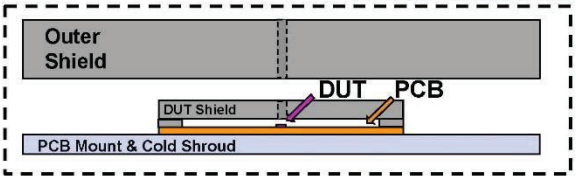


New PCB



- 50 Ω RF Traces
- Via-Fences

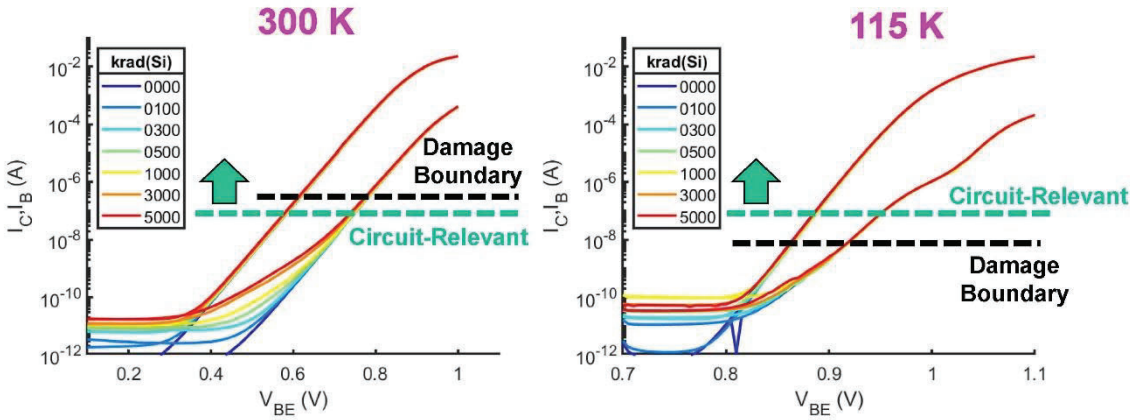
New Shield



Z. Brumbach *et al.*, IEEE 2024 Aerospace Conf.

Test Goals Satisfied: 5 Mrad(Si) Results

- Some Base Current Non-ideality at 115 K (Expected)
- TID Response Improves at Low-Temperatures to 5 Mrad (Great News!)



J. Teng *et al.*, IEEE 2022 NSREC

Example RF Circuit Documentation (X-band VCO)

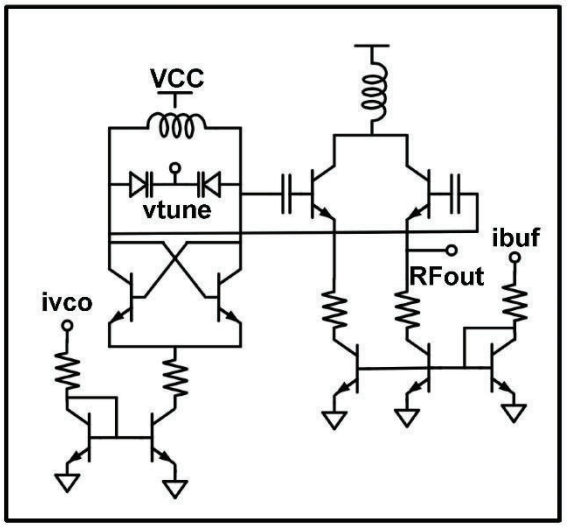
Circuit Description

- 9-10 GHz VCO with differential common collector buffer
- No performance degradation at 5 Mrad

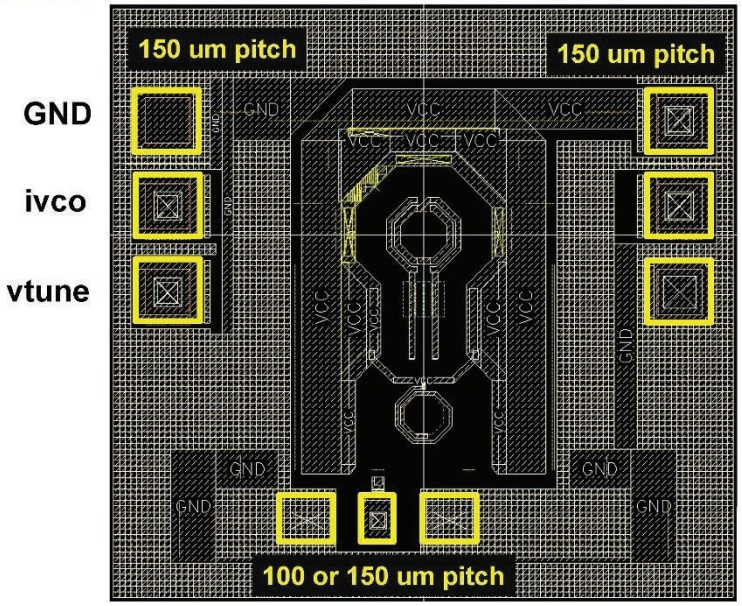
Application Notes

- Biases ivco and ibuf are designed to connect directly to VCC. For testing purposes they are broken out in the layout.

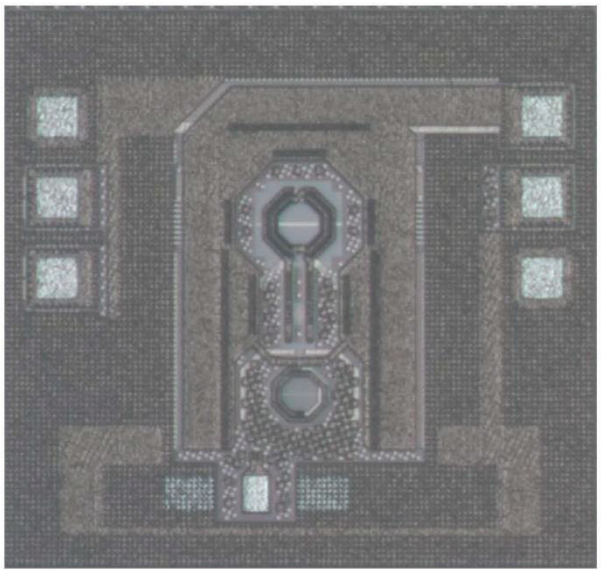
Circuit Schematic



Pad Detail



Die Photo



Performance Summary

NASA COLDTECH: Environmentally-Invariant SiGe Electronics for On-Surface Ocean Worlds

Metric	298 K	93 K	25 K	15 K	Notes
Tuning Range (GHz)	9.19 - 10.15	9.69 - 10.35	10.16 - 10.55	10.26 - 10.59	
Simulated Phase Noise (dBc)	-109.7	-115.2			@ 1 MHz
VCO Power (mW)	9.00	8.81	8.67	8.73	VCO core + buffer

Output Power (50 Ω, dBm)	-14
Area (um)	1090 x 1030

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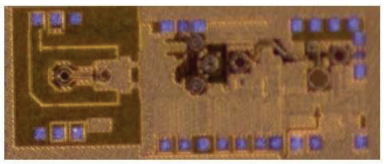
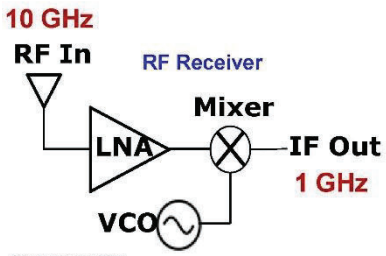
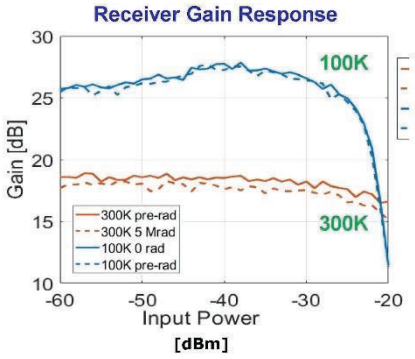
Recent Success! RF X-Band SiGe Receiver

NASA COLDTECH: Environmentally-Invariant SiGe Electronics for On-Surface Ocean Worlds

- 300K Gain of ~17 dB, 100K Gain of ~26 dB
  - 1 dB gain degradation at 5 Mrad[Si] at 300K, - 0 dB at 100K
  - cable loss not accounted for yet (expect ~6 dB improvement)
  - SEL immune, extensive SEE testing at LBNL and NRL







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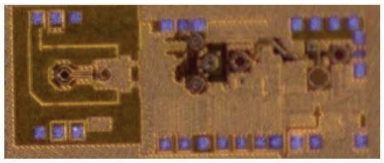
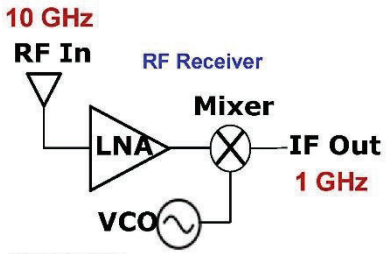
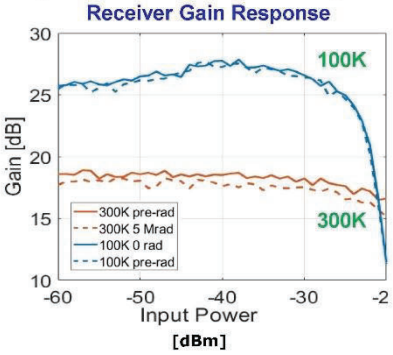
  - SEL immune, extensive SEE testing at LBNL and NRL
- NF < 1.0 dB at 100K
- Passes RF Data (QPSK) with Low Error (EVM)

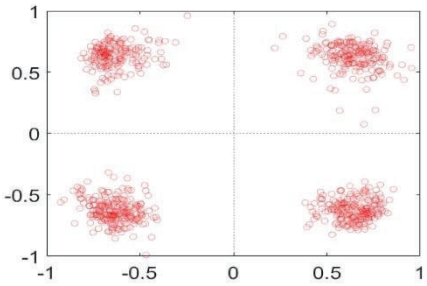




Receiver Gain Response



Data Output after 5 Mrad at 100K



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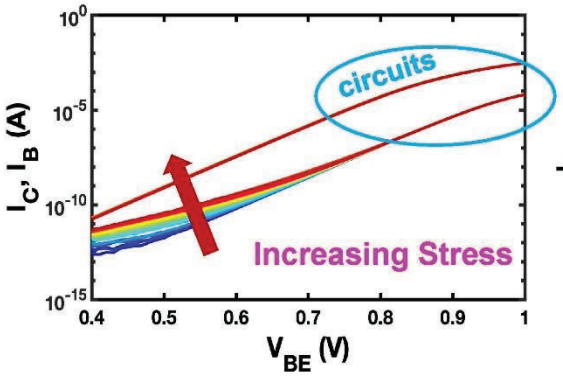
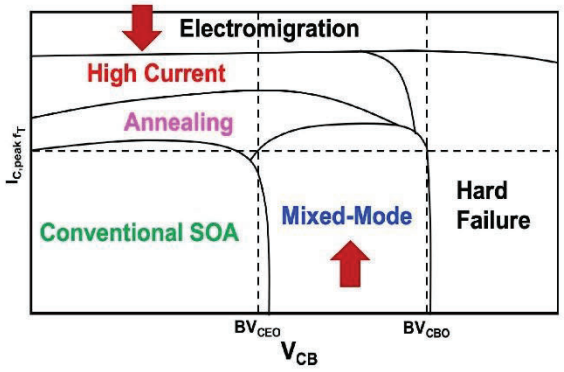
SiGe HBT Electrical Reliability

- **Traps Generated at Oxide Interfaces by Hot Carriers**
  - hot carriers generated within device
  - hot carriers redirected towards sensitive interfaces
- **Base Leakage Current Increases With Traps**
- **Key Damage Regions: Mixed-Mode, High Current**





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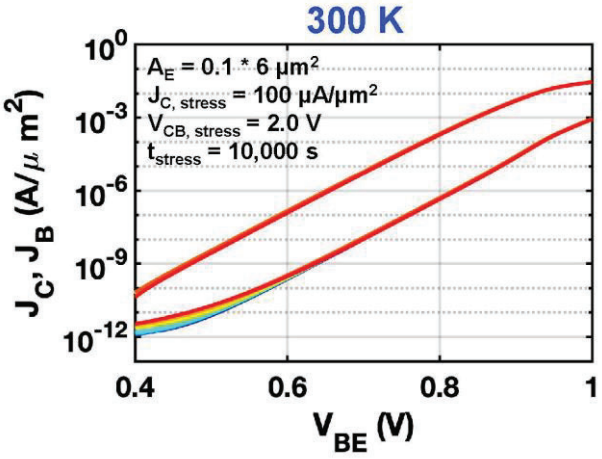
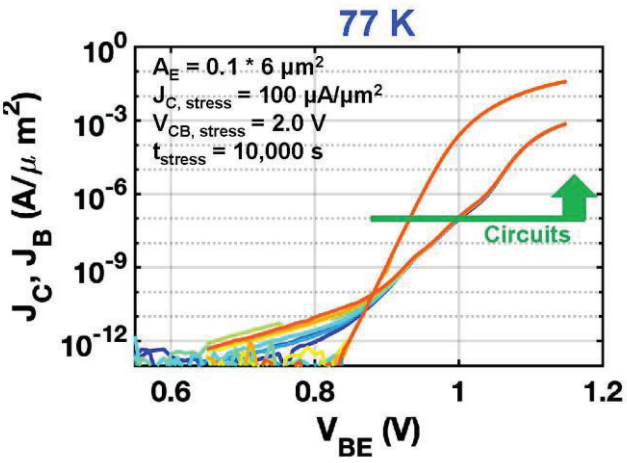
Reliability: Mixed-Mode Stress

- **No Damage at Circuit Relevant Bias at 300K or 77K (Great News!)**





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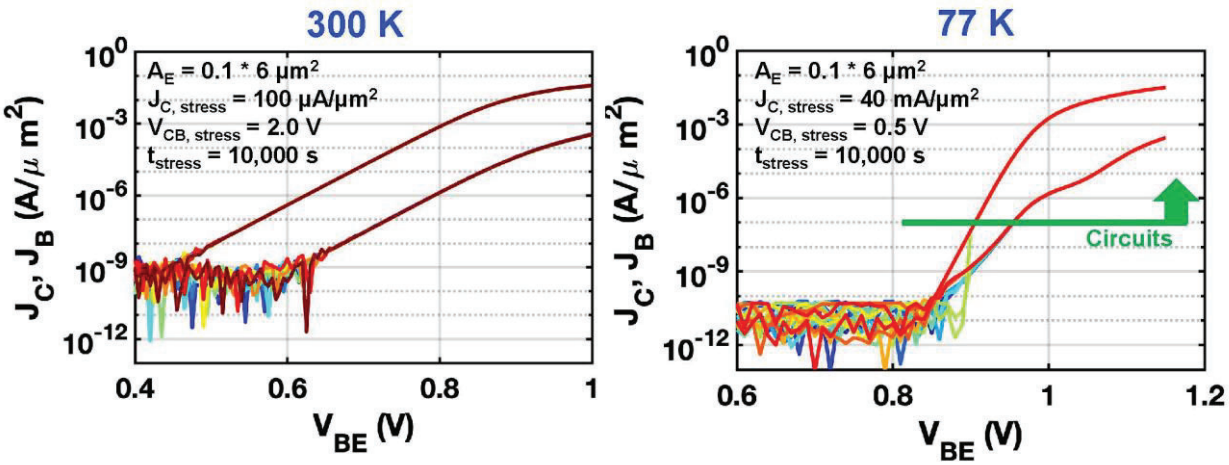
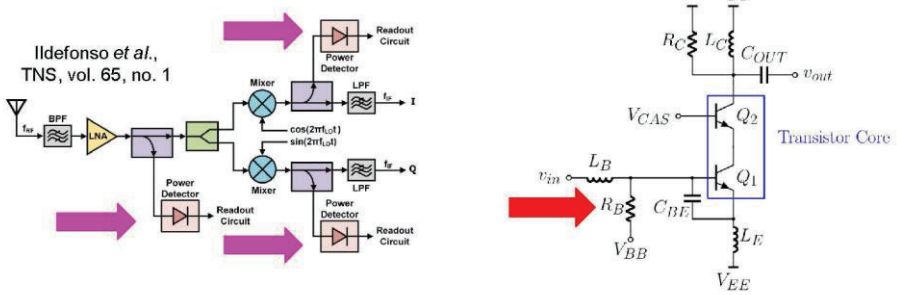
Reliability: High Current Stress

- **No Damage at Circuit Relevant Bias at 300K or 77K (Great News!)**



SEE Mitigation at RF Component Level

- **Conversion of SET to SEU Depends on Amplitude and Duration**
  - trade-off of amplitude / duration depends on intended environment
  - can use excess bandwidth in LNA / mixer to reduce SET duration
- **Circuit Topology Can Be Used to Mitigate SETs**
  - inductors instead of resistors ensure DC voltages at transistor remain constant
  - biasing transistors can be distributed to reduce impact of single SETs



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Lunar Insertion Opportunities

- **Accomplishments**
  - library of Analog / Digital / RF SiGe Components (-180ºC + 5 Mrad Operation)
  - **X-band (8-12 GHz) RF receiver** capable of QPSK communications

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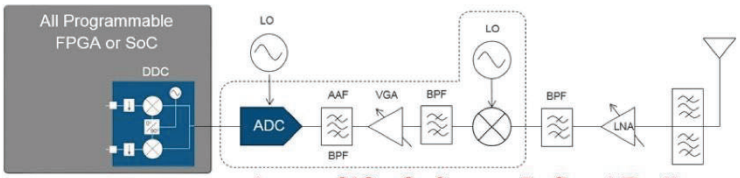
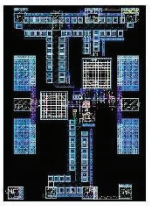
- **Accomplishments**
  - library of Analog / Digital / RF SiGe Components (-180ºC + 5 Mrad Operation)
  - **X-band (8-12 GHz) RF receiver** capable of QPSK communications
- **Insertion Opportunities (Lunar Day or Night or PSC)**
  - **Reasonable Targets:** SiGe cold radio, cold phased arrays for comm or radar
  - operates outside warm box, without shielding (enables distributed sensors)
  - withstands lunar night (-180ºC), lunar day (+120ºC) and radiation (100 krad)
  - operates in permanently shadowed polar craters (-230ºC)
  - enabling for on-surface sensor links + comm/radar during lunar day/night



Lunar SiGe Software-Defined Radio



Lunar SiGe
Ka Band LNA

Takeaways for Lunar Systems

- **SiGe = Si** (integration, cost, reliability, models, PDKs, etc.)
- **SiGe is Capable of Extreme Levels of Performance** (THz is coming!)
- **This Performance Enables a Robust Set of Tradeoffs** (NF, power, etc.)
- **Monolithic CMOS Available To Use Where It Brings System Leverage**

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- **SiGe Electronics Viable for BOTH Ocean Worlds and Lunar Surface**
  - **SiGe ideally suited for radiation + low temperatures**
  - **SiGe can handle 5 Mrad TID and -180°C** (Europa surface)
  - **SiGe can handle -180°C to 120°C and 100 krad** (lunar day / night)
  - **SiGe can handle -250°C and 100 krad** (shadowed polar craters)
  - **Analog, RF and digital circuits library demonstrated**
  - **Working Towards a SiGe Design Eco-system**

Many Lunar Opportunities!

John D. Cressler, 2025 13

My Gang

John D. Cressler, 2025 44

Lessons Learned from 20+ Years of Cold-Capable Analog/Mixed-Signal IC Design

Prof. Ben Blalock and ICASL team members Sean Bouma, Steve Corum, Von Hermoso, Nolan Robinson, Alex Seaver, Md Omar Faruk, and Langdon Skarda

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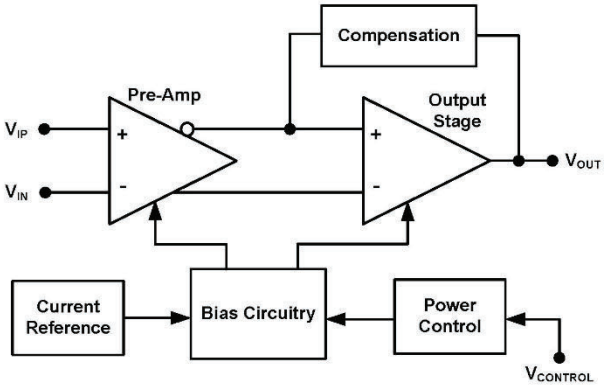
MARS QUAD OPERATIONAL AMPLIFIER

JPL

- *Curiosity* (and later, *Perseverance*) required op amps that could withstand the Martian surface environment.
- Martian surface environment: 1) daily temperature swings: −120°C to 20°C, 2) light atmosphere, some radiation
  - Hot carrier effects (HCE), worsened by cold Martian surface conditions and voltage stress, challenge long term CMOS reliability
  - 5-V supply voltage requirement on 3.3-V CMOS technology
  - UTK designed circuit topologies within Mars QOA to manage voltage stress for every transistor
  - Mission reuse specifications required −180°C to 120°C operational capability and radiation hardness
  - UTK developed a new biasing technique for analog amplifiers, constant inversion coefficient biasing [1], to provide optimal performance tradeoff over wide temperature.



Mars QOA Two-Stage Architecture

[1] "Wide-temperature integrated operational amplifier," U.S. Patent No. 7,514,998 (April 7, 2009)

2

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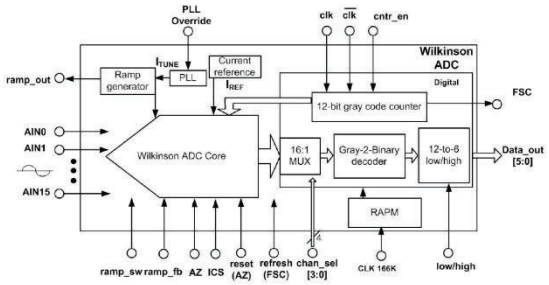
WILKINSON ADC FOR SIGE EDTP

ADC Specifications
- 16 input channels supported (parallel operation w/ simultaneous sampling)
- 20-KSps sampling rate
- 12-bit accuracy
- Input range of 0 to 1.2V
- Operation over a wide temperature range of –180ºC to 125ºC
- Required to operate in lunar surface environment conditions
- Clock frequency of 85 MHz to operate Gray code counter
- Shared ramp generator and counter lower power consumption



Design blocks of Wilkinson ADC
- Ramp generator
- Auto-Zeroed (AZ) comparators (16)
- Counter
- Current reference
- 2.5-V regulator (RAPM)
- Digital section
- Pulse Width Locked Loop (PWLL)

Features of Wilkinson ADC
- Radiation aware power management (RAPM) scheme to detect and mitigate SEL within the digital backend of the ADC
- LVDS transmitter and receiver for the ADC clock
- PWLL based temperature compensation scheme for the ADC's ramp generator
- Voting logic within the counter FFs to mitigate SEU
- Radiation-hardened-by-design (RHBD) digital cells are employed within RAPM block
- Low power ramp generator (≈ 125 µW)
- Low power auto-zero comparator (≈ 95 µW)
- Low power Gray-code counter (≈ 1.3 mW)

WILKINSON ADC for SiGe EDTP

Device-Level and Circuit-Level Design Strategies:
- Analog front-end circuits use $4\times L_{min}$ (or longer) NMOS devices to mitigate hot carrier effects (HCE). In physical layout, generous application of guard rings used to mitigate single-event latchup (SEL).
- Short *L* design required in digital section of ADC for low-power/high-speed/compact area tradeoff optimization using standard cell library
- 2.5-V supply selected for digital section to maintain long-term reliability at cold temperature (lower voltage to mitigate hot carrier effects)
- Majority voting logic incorporated into Gary code counter design to mitigate (single-event upsets) SEUs

The RAPM system:
- Provides 2.5-V power needed for digital backend section of the ADC
- In the event of radiation induced SEL, this power management scheme will automatically collapse the supply rail voltage to the digital section of the ADC to mitigate SEL, and then restore digital power to 2.5 V.
- Designed to withstand high frequency current transients associated with digital (e.g. the Gray code counter)

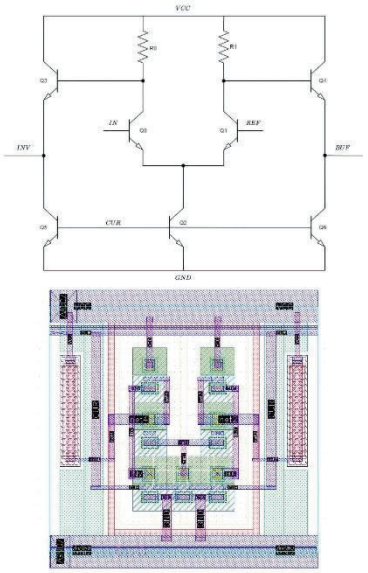
Pulse Width Locked Loop (PWLL) based temperature compensation of ramp generator [2]:
- To temperature compensate ramp rate, the PWLL dynamically adjusts *dv*/*dt* (ramp slope) rather than compensating only the bias current over temperature
- PWLL has been designed to generate a temperature, supply voltage, and process independent *dt* while *dv* is guaranteed by a bandgap voltage reference
- UTK's PWLL scheme provides auto temperature calibration for integration-style ADCs

Performance:
- DNL within ±0.5 LSB from −180ºC to 120ºC
- DNL (< 0.5 LSB) and SNR (> 60 dB) show negligible change following ionizing irradiation (up to 300 krad proton and 300 krad X-ray).
- This ADC demonstrates device-, circuit-, and system-level design techniques to enhance temperature capability and radiation immunity!

[2] K. Tham, C. Uliganathan, N. Nambiar, R. L. Greenwell, C. L. Britton, M. N. Ericson, J. Halleman, and B. J. Blalock, "PVT Compensation for Wilkinson Single-Slope Measurement Systems," *IEEE Transactions on Nuclear Science*, vol. 59, no. 5, part 3, 2012, pp. 2444-2450.

SiGe 3.3-V EMITTER COUPLED LOGIC DIGITAL STANDARD CELL LIBRARY

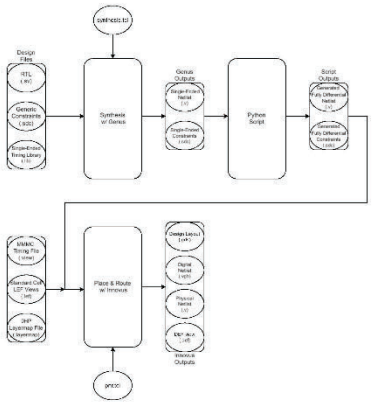
- Exploration of extreme cold and radiation environments pose a **significant challenge** for many commercial electronic devices fabricated in **traditional CMOS processes**
- Leveraging "*old school*" **ECL** for "*new school*" ***extreme*** harsh environments (e.g., Europa surface)
  - ECL operates through "steering" the tail current flowing between two sides of an input differential pair resulting in a voltage difference between the outputs
  - Harnessing the benefits associated with SiGe Technology, we decrease bias tail current from ~1mA down to only 10uA for extremely ***Low Power ECL***
  - Also, SiGe provides increasing Device Current Gain (β) and Transition Frequency (f_T) as temperatures drop
- 3.3-V ±10% supply voltage allows for compatibility with industry standards
  - Carefully addresses voltage stress issues associated with HBT devices through circuit topology



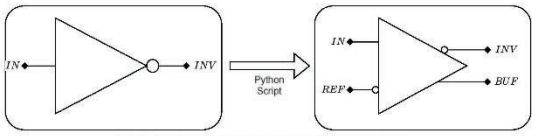
ECL_INV Schematic/Layout

ECL SYNTHESIS PROCESS DEVELOPMENT FOR COMPLEX DIGITAL SYSTEMS

- Fully Differential architecture of ECL cells pose challenges for industry available EDA tools from Cadence, Synopsis, etc. optimized for CMOS processes
  - Expect single-ended digital signals swinging from 0V to VDD
  - Does not support inserting auxiliary cell bias circuitry (Voltage References)
- Generation of required files for ASIC Design flow
  - Cell Timing Files (.lib) (Single-Ended/Fully-Differential)
  - Verilog Cell Views (.v) (Single-Ended/Fully-Differential)
  - Physical Cell Layout Views (.lef) (Fully-Differential)
- High-Level Procedure Overview:
  1. Synthesize RTL using single-ended ECL Views (similar to CMOS logic) to obtain a single-ended gate level netlist
  2. Use ECL python script to modify the single-ended netlist into a fully-differential netlist which includes necessary ECL bias circuitry
  3. Perform Place and Route (PnR) on fully-differential netlist



ECL Synthesis Design Flow Chart



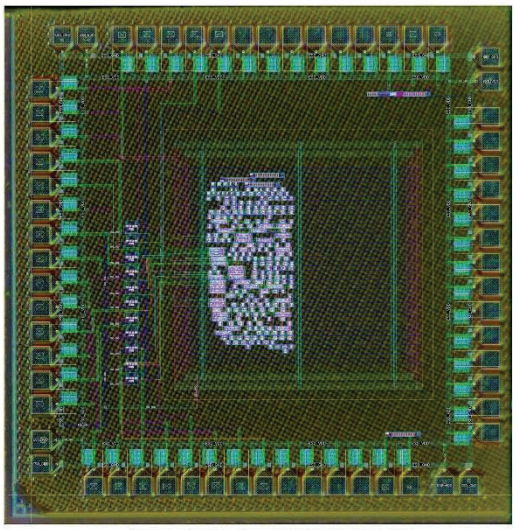
ECL Python Script Gate Conversion

ECL MEMORY CONTROLLER

- Synthesis of fully ECL-based Memory Controller as a *pathfinder* demonstration for complex digital systems using ECL
- Simplified version with decreased I/O count to facilitate testing
- Objective: Synthesize a simplified version of the memory controller to showcase proper initialization/startup using ECL

Cell	Cell Count
ECL_Simple_Reference	3
ECL_Voltage_Reference	1
ECL_INV	102
ECL_OR	92
ECL_XOR	6
ECL_AND	1
ECL_DFFSR	33
ECL_TI_HI/LO	22
Total	260

Memory Controller Stats	
Inputs	19
Outputs	14
Core Area (mm^2)	1.1 x 1.1
Die Area (mm^2)	2.0 x 2.0
Clock Freq. (MHz)	10



August 2024 Memory Controller Die

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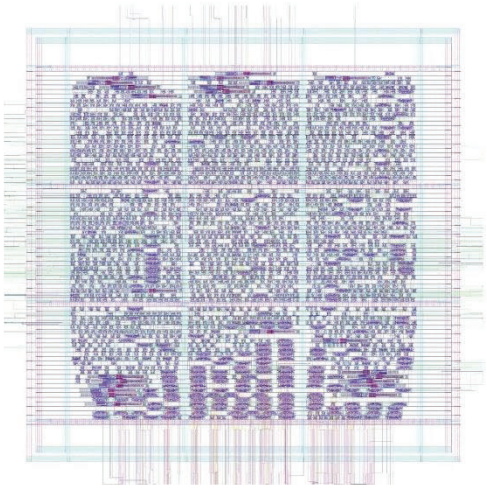
EXPANDING ON ECL SYNTHESIS

- The developed ECL Synthesis workspace provides a robust methodology for synthesizing fully ECL-based complex digital systems
  - Compatibility with industry tools for CMOS synthesis
  - Cryogenic capable digital library with hot carrier effect immunity for long term reliability
  - Wide-temperature capable (e.g., −180°C to +125°C)
  - Inherits the radiation hardness of SiGe technology
  - 100 MHz capable operating frequency
  - Demonstration of low current density, synthesizable ECL
  - Differential signal path enhancing EMI resistance and noise immunity



Full Memory Controller Layout (2mm x 2mm Core Area)

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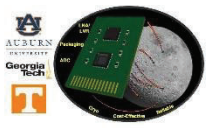
THE RINGAMP LDO (RLDO)

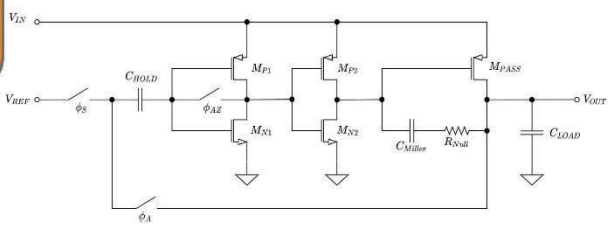


The Ring Amplifier:
- Digital solution to the Analog Amplifier scaling problem.
- Naturally scalable due to CMOS inverter-based design and Inherently high bandwidth.
- Fundamental Ringamp is a Ring Oscillator that is biased into stability.
- 1st stage inverters designed for poles located beyond UGB.
- Output stage inverter pole (dominant pole) designed for the required phase margin (feedback stability).

RLDO Design [1,2]:
- Two-stage ringamp acts as error amplifier.
- Two periods of operation; sample & amplify.
- C_{HOLD} is sample & amplify capacitor and perfectly matched to itself!

Sample Operation:
- ϕ_S, ϕ_{AZ}=Closed; ϕ_A=Open;
- 1st stage inverter is biased to the switching point V_{M1}.
- C_{HOLD} charged to $V_{HOLD} = V_{REF} - V_{M1}$;
- V_{OUT} is unregulated. Sample duration short to minimize V_{OUT} drop.
- Minimum sample duration is approx. 4-5 $\tau_{C_{HOLD}}$. PVT Sensitive!!!

Amplify Operation:
- ϕ_S, ϕ_{AZ}=Open; ϕ_A=Closed;
- Two-stage ringamp regulates V_{OUT}.
- Amplify period is as long as possible and limited by C_{HOLD} leakage.



Simplified schematic of Ringamp LDO [3, 4].

Additional Design Considerations:
- Ideally, inverters are designed for V_M at mid-rail.
- 1st stage inverter optimized for high speed and low noise.
- 2nd stage inverter optimized for high gain and slew rate.
- To minimize V_{OUT} drop during sampling period, τ_{MPASS} should be much larger than $\tau_{C_{HOLD}}$.

[3] J. Sangid, "A Ringamp-Assisted, Output Capacitor-less Analog CMOS Low-Dropout Voltage Regulator," Ph.D. dissertation, The University of Tennessee, Knoxville, TN, May 2022.
[4] S. Corum, "A Case Study in CMOS Design Scaling for Analog Applications: The Ringamp LDO," Master's thesis, The University of Tennessee, Knoxville, TN, Dec. 2023.

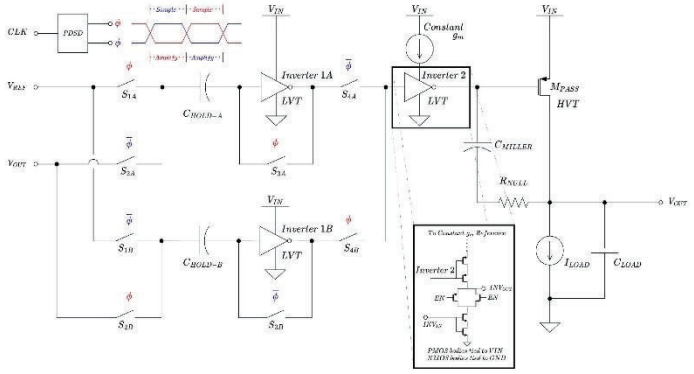
TIME-INTERLEAVED RLDO

An RLDO For The Lunar Environment:
- The ringamp is not inherently stable across wide temperatures.
- Biasing and compensation techniques can improve ringamp performance over temperature.
- UTK's Time-Interleaved RLDO implements techniques to normalize performance over temperature and is the only known RLDO designed for wide-temperature!

Time-Interleaved Design:
- 1st stage inverter/SAH networks are time interleaved.
- $T_{SAMPLE} = T_{AMPLIFY}$, and is only limited by C_{HOLD} charge leakage. Eliminates sample period PVT sensitivity!!!
- Results in improved PSR, simplified PVT tolerant clock control, and V_{OUT} is always regulated!!!

Wide-Temperature Design [5]:
- Dom. pole stage (2nd stage) biased w/ constant-g_m current reference.
- 2nd stage contribution to GB is temperature invariant.
- M_{PASS} contribution to GB is temperature invariant, if A_{MPASS} is sufficiently large.
- Unfortunately, 1st stage temperature variations not addressed yet.

$$GB = \frac{A_1 \cdot A_{MPASS} \cdot g_{m2}}{C_{O2}} = \frac{A_1 \cdot A_{MPASS} \cdot g_{m2}}{C_{MILLER} \cdot (1 + |A_{MPASS}|)}$$



Time-Interleaved RLDO Simplified Schematic.

Additional Cryo-Considerations:
- Inverters designed with LVT devices to mitigate increased V_{TH}.
- Non-minimum NMOS Gate Lengths for hot-electron mitigation.

Additional Hot Considerations:
- M_{PASS} designed w/ HVT PMOS for improved gain at low load conditions.
- C_{HOLD} is increased from previous RLDO iterations to mitigate V_{OUT} droop caused by gate leakage.

[5] K. Yamashita, B. Hershberg, K. Yoshioka and H. Ishikuro, "A 4.6–400 K Functional Ringamp-Based 250 MS/s 12 b Pipelined ADC With PVT-Robust Unity-Gain-Frequency-Aware Bias Calibration," in IEEE Journal of Solid-State Circuits, vol. 59, no. 3, pp. 740-752, March 2024

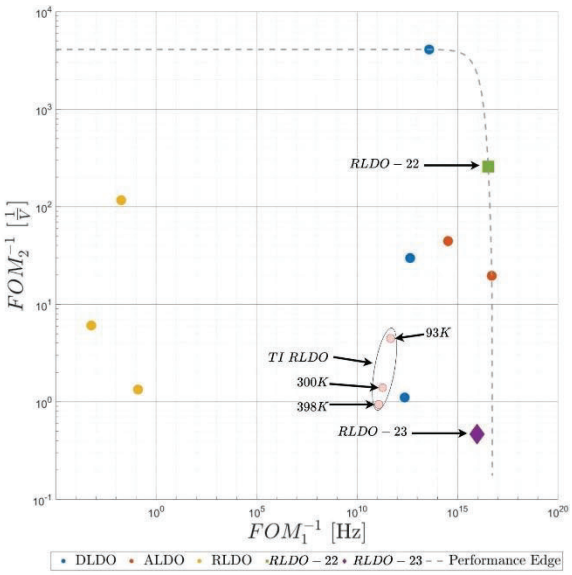
TI RLDO SIMULATION RESULTS

TI-RLDO PEX simulation results across temperature.

Parameters	Unit	*TI RLDO 93K*	*TI RLDO 300K*	*TI RLDO 398K*
Year		-	2024	-
Technology	[nm]	-	90	-
Temperature	[K]	93	300	398
V_{IN}	[V]	-	1.2	-
V_{OUT}	[V]	-	0.8	-
I_{OUT}	[mA]	-	30	-
I_Q	[µA]	114.4	229.6	283.3
V_{DO}	[mV]	-	200	-
C_{TOTAL}	[pF]	-	14	-
Δt_{edge}	[ns]	-	**0.1**	-
ΔV_{OUT}	[mV]	380.9	608	722.1
T_{SETTLE}	[ns]	**36.3**	**51.2**	**58.4**
PSR at 100 kHz	[dB]	48.3	41.8	40.2
GB at Max. Load	[MHz]	**59.8**	**43**	**40.1**
FOM_1 *	[fs]	1530	4890	7160
FOM_2 †	[V]	0.218	0.698	1.023
Active Area	[mm^2]	-	0.045	-

$$* \; FOM_1 = \left(\frac{C_{TOTAL} \cdot \Delta V_{OUT}}{I_{O,MAX}}\right)\left(\frac{I_Q}{I_{O,MAX}}\right) \quad [6]$$

$$\dagger \; FOM_2 = \left(\frac{\Delta t_{edge}}{1\,ps}\right)\left(\frac{\Delta V_{OUT} \cdot I_Q}{I_{O,MAX}}\right) \quad [7]$$



FOM comparison graph with previous ICASL RLDOs (180 nm RLDO-22 [3], 90 nm RLDO-23 [4]) and TI-RLDO simulated performance plotted against State-of-the-Art LDOs.

[6] Hazucha, T. Karnik, B. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area Efficient Linear Regulator with Ultra-Fast Load Regulation," *IEEE Journal of Solid State Circuits*, vol. 40, no. 4, pp. 933-940, 2005.
[7] J. Guo and K. N. Leung, "A 6-µW Chip-Area-Efficient Output-Capacitorless LDO in 90-nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp.1896–1905, 2010

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COLD TEMPERATURE TESTING LESSONS LEARNED

Problems	Solutions
1. Performance of typical commercial passives degrades dramatically at low T .	1. Use capacitor materials that are shown to maintain capacitance and ESR at cryogenic temperatures such a tantalum polymer or NP0/C0G ceramic [8][9]. Use precision metal film resistors.
2. Cabling parasitics into and out of the temperature chamber prevent reliable high-speed transient or AC measurements.	2. Well bypass supplies using cryo-capable capacitors. Use properly terminated cryo-capable COTS Op-Amps for signal buffering coaxial cables.
3. Difficult to identify cold-capable active/linear COTS parts for supporting test functions.	3. Evaluate active/linear COTS components at cryogenic temperatures.
4. Charge carrier freezeout limits the cold performance of bipolar IC technologies.	4. SiGe BiCMOS and CMOS components offer best solutions.
5. Cryogenic test boards can undergo excessive mechanical strain, especially when interfacing with a cold finger.	5. Prefer indirect interfaces between heat sink and DUT, including gas, liquid immersion, or vertical PCB stackups with thermally conductive vias.

[8] Harald Homulle, Edoardo Charbon, "Cryogenic low-dropout voltage regulators for stable low-temperature electronics", *Cryogenics*, Volume 95, 2018, Pages 11-17, ISSN 0011-2275, https://doi.org/10.1016/j.cryogenics.2018.09.006
[9] M. Song, J. Y. Yang-Scharlotta, M. Ashtijou and M. Mojarradi, "Evaluation of commercial-off-the-shelf (COTS) electronics for extreme cold environments," *2018 IEEE Aerospace Conference*, Big Sky, MT, USA, 2018, pp. 1-12, doi: 10.1109/AERO.2018.8396695.

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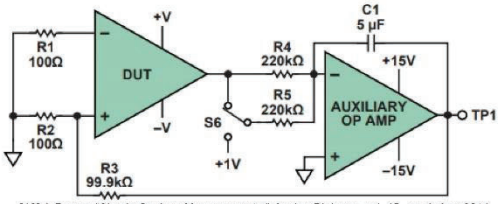
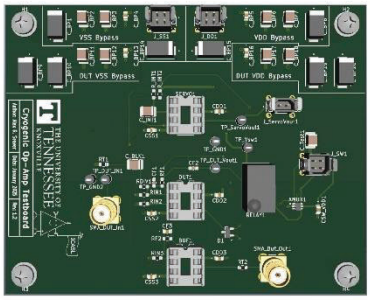
CRYOGENIC-CAPABLE COTS OP-AMP TEST BOARD

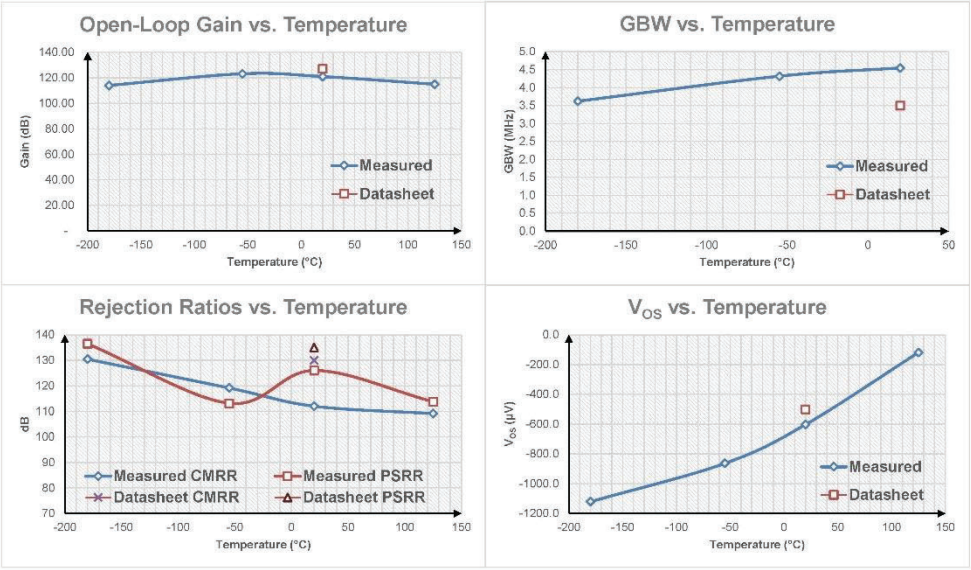
- Cold-capable board designed to test COTS op amps:
  - + Input offset voltage
  - + DC open-loop gain
  - + DC CMRR and PSRR
  - + AC Gain-Bandwidth product
- Temperature stable passives:
  - + Tantalum-Polymer and NP0/C0G ceramic capacitors
  - + High precision metal film resistors
  - + Electromagnetic relay for signal routing
- Keeping devices on the same board inside the cold chamber reduces cabling parasitics and enables AC BW testing
- Will be expanded to include testing capability for ICASL's custom IC op amps



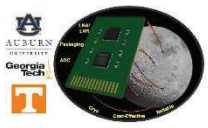
[10] J. Bryant, "Simple Op Amp Measurements," *Analog Dialogue*, vol. 45, no. 4, Apr. 2011.



MEASUREMENT RESULTS: TLV271 (ONSEMI)



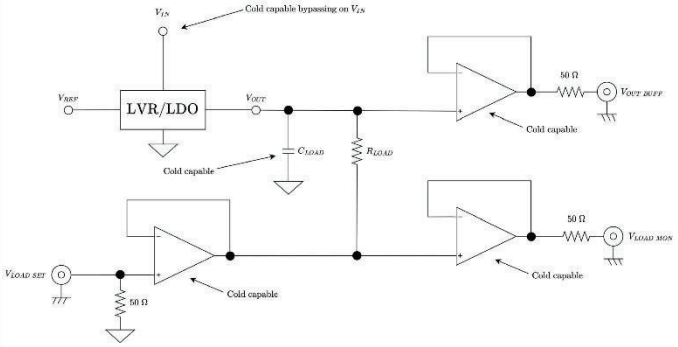
WIDE-T LVR/LDO CHARACTERIZATION



Features:
- Applicable experiments include: Line Regulation, Load Regulation and Load Current Step Response.
- Temperature stable passives and cold capable COTS Op-Amps used throughout design.
- This configuration allows the load capacitance to range from a few pF to hundreds of µF. Critical feature for testing TI-RLDO.
- This configuration allows a wide range of static and dynamic current load conditions.

Operation:
- The Op-Amp driven by $V_{LOAD\ SET}$, is used to apply a load current applied to V_{OUT}.
- The Op-Amp driving $V_{OUT\ BUFF}$, is used to buffer V_{OUT}.
- The Op-Amp driving $V_{LOAD\ MON}$, is used to buffer $V_{LOAD\ SET}$ to validate experimental conditions within the temperature chamber.

Validation:
- Test board validated down to −180ºC.
- 3.3-V SiGe BiCMOS LVR validated down to −180ºC.



Cold-Temperature LVR/LDO Characterization Board Simplified Schematic.

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ACKNOWLEDGEMENTS

This work was supported by:

- The Jet Propulsion Laboratory
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- NASA LuSTR program, under Grant 80NSSC22K0740

NASA COLDTech

JPL

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Questions?

NESC Technical Assessment Meeting
Cold Electronics for Lunar Missions
TI-22-01873

Cold Electronics: Power System Applications

Richard C. Oeftering

Power Architecture and Analysis Branch

NASA Glenn Research Center

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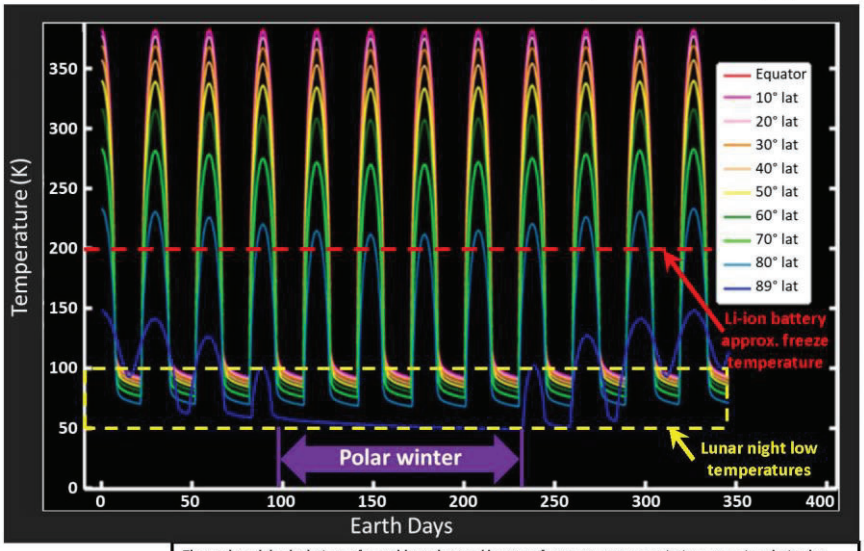
Cold Electronics: Power Systems Applications

Cold Electronics for Lunar Missions

- CLPS Lunar Robotic Missions - Power Hibernation
- Cold Electronics Power Applications
  - Solar Arrays & Array Regulation
  - Battery Management and Charge Control
  - Main Bus & Power Distribution
  - High Power Motor Drives
  - High Voltage Transient Suppression
- Cold Electronics Technologies

Cold Electronics: Power Systems Applications



Thermal model calculations of monthly and annual lunar surface temperature variations at various latitudes.
Image permissions per Dr. N Petro/NASA GSFC, Dr. D Paige/UCLA

LRO Diviner Data

Day: 200-400 K high temps based on latitudes (0° to 80°)

Night: 50-100 K low temps based on latitudes (0° to 89°)

Lunar Night Duration

Non-Polar Latitudes

~14.75 Days / 354 Hours

***Polar Latitudes*:**

(above 89° latitude)

"Polar Winter" roughly 4 ½ months of dark due to lunar inclination (1.53° relative to the sun). Cold soak to 50K

Cold Electronics: Power Systems Applications

Lunar Robotic Mission Context

- CLPS (Commercial Lunar Payload Services) Program
  - Intended to encourage the development of a commercial space services.
  - Low-cost missions & short development cycles
  - Relatively low experience developers with high risk of early failures.
  - All missions, so far, have been solar powered.
  - Initial CLPS missions were not required to survive the lunar night.
- Nuclear and Radioisotope solutions are out of reach to keep mission cost down and minimize safety risks.
- Missions, so far, have either not recovered from the lunar night or recovered with limited capability.
- "Surviving the Lunar Night" is the highest on the CPLS list of technology gaps.
- Some proposed solutions involve a consumable that could provide additional cycles until the consumable is exhausted.

Cold Electronics: Power Systems Applications

Conventional Wisdom: (Partially True)

- *Batteries are the weak-link, cells will freeze and likely be damaged.*
- *Circuits boards won't tolerate the thermal cycles without damage.*
- *Semiconductor devices will not operate in the extreme cold.*

However: Li-Ion cells of 18650 format were found to tolerate the freeze/thaw process and recover their charge capacity when returned to normal temperatures.

- Initial work performed by the ISRO (Indian Space Research Organization) in 2017.
- Confirmed by tests performed by NASA Glenn Research Center in 2019.

Implications: Spacecraft can hibernate through the lunar night and recover when solar illumination and heating returns at lunar dawn.

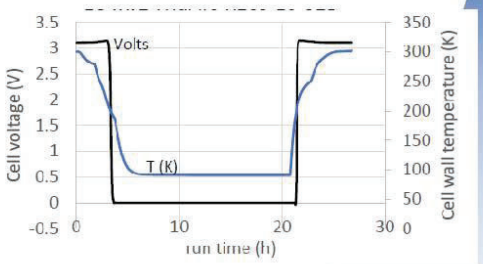
Cold Electronics: Power Systems Applications

Why 18650 cells?

- 18650 cell is widely used for both small and large spacecraft batteries.
- NASA/Air Force Strategic Procurement buys 18650 in lots of tens of thousands.
  - Highly controlled sourcing and chain of custody. (counterfeit cell issue)
  - Highly controlled storage and cell testing

Early GRC Tests Demonstrated

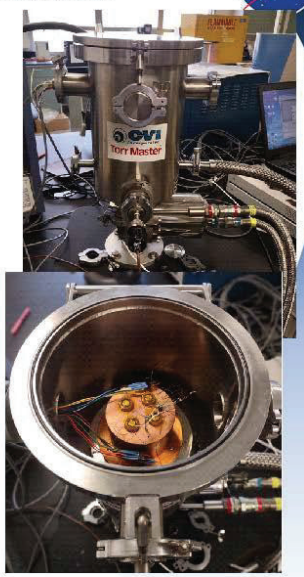
- Li-Ion 18650 cells tolerate freeze/thaw cycle
- Voltage drops to zero when frozen ~200K (-73°C)
- Cells tested to 77K (-196°C) in a vacuum
- Recovers its state-of-charge (SOC) when warm
- Cells tested in vacuum recovered reliably



Cold Electronics: Power Systems Applications

Recent GRC Testing: Li-ion Batteries Survive 50K

- Demonstrated several freeze/thaw cycles on NASA JSC's Strategic Reserve 18650 Li-Ion cells, Dwell times of 14 days.
- Investigated performance at 0%, 20%, and 40% SOC
- Little to no loss of capacity
- Cells Tested **LG INR18650 M36 / Molicel INR18650-M35A**



STMD STRG ECF22 Topic 2: *Hibernation and Recovery of Solar-Powered Systems for Lunar Missions*

- 2 ECF22 PIs Dr Zhu (UCSB), Dr Hatzell (Princeton)
- Thorough characterization of the Li-Ion cell freeze/thaw process
- Electro-chemical and thermal-mechanical characterization and modelling

Current Findings:

- Confirmed Cell Chemistry freeze/thaw process is **Reversible.**
- Some Freeze/Thaw degradation occurs in first few cycles then levels out.
- Cell life expectancy is not dramatically less than normal cell cycles.
- Running cells at high currents is much more degrading.

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Cold Electronics: Power Systems Applications

Further Evidence of Hibernation and Recovery Success

Mars Helicopter "*Ingenuity*" demonstrated hibernation and recovery in the Mars environment. Cells exposed to Freeze/Thaw cycles.

Assuming Li-Ion cells survive the Lunar Night, What about the spacecraft electronics? *Good Question*

Spacecraft Cold Electronics must:

- Physically tolerate the extreme temperatures and thermal cycles.
- Reliably "Cold-Start" at cryo-temperatures.
- Provide stable operation, preferably, from 126°C to -223°C (400K to 50K) temperature range.

5/16/2025

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Cold Electronics: Power Systems Applications

Implications for CLPS lunar robotic spacecraft development.

- A number of CLPS landers have already been developed, qualified, and flown.
- CLPS developers rely on heritage instruments and electronics to minimize development cost.

Does surviving the lunar night take CLPS back to the drawing board:

- Do we discard existing designs to adopt cold electronics?
- Does it dramatically increase in system complexity?
- Does it consume payload capacity?
- Is there an *evolutionary approach* that would allow a cost-effective transition?

Cold Electronics: Power Systems Applications

Lunar Power Hibernation and Recovery Approach

- Involves passively surviving the lunar night by going into hibernation (all systems shutdown) when battery charge capacity reaches preset low limit battery is isolated.

Recovery at Lunar Dawn Requires:

- Generally, avionics remains passive until the power system completes the recovery process.
- Power electronics must be capable of cold start and stable operation on solar array output alone.
- Utilize array power to thermally restore the battery to operating temperatures.
- Managing the battery recovery and reconnecting it to the main bus.
- Thermally restoring the avionics to operating temperatures.

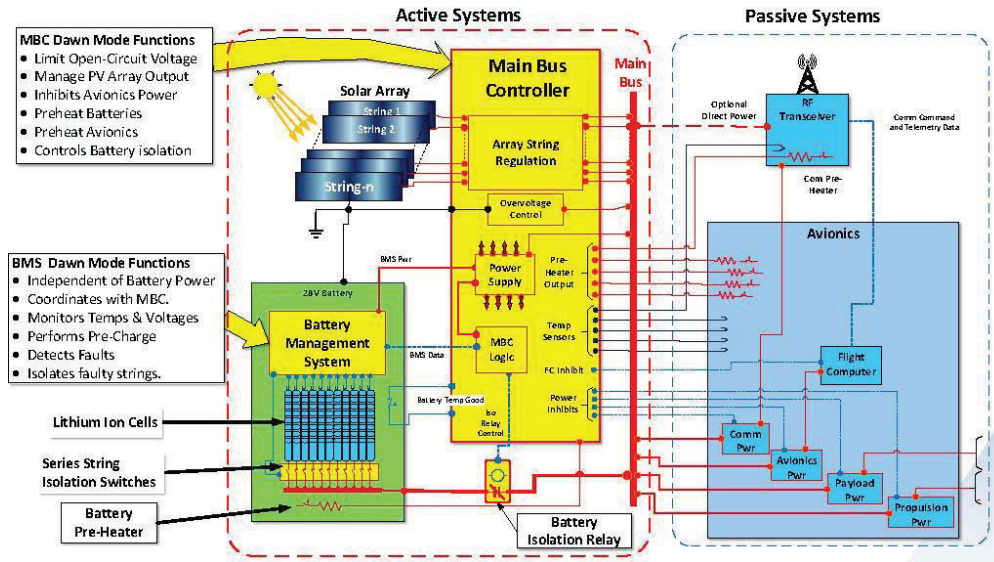
Cold Electronics: Power Systems Applications

Hibernation Approach is intended to enable multiple lunar cycles.

- Employs cold-electronics in key functions.
- Attempts to minimize spacecraft redesign and development costs.
  - Assumes Li-Ion cells can tolerate multiple Freeze/Thaw cycles.
  - Assumes Solar Arrays can operate at cryo-temperatures.
  - Assumes existing electronics can be requalified to tolerate lunar temperatures.
  - Potentially enables the developers to use the existing solar arrays.
  - Potentially enables the developers to use the existing battery with modifications.
  - Restricts the requirement for cold-start and cryo-operations to main bus power.
  - Minimizes the impact on payload capacity.

- **Surviving the Lunar Night should be a baseline capability.**

Cold Electronics: Power Systems Applications



Cold Electronics: Power Systems Applications

In the following charts

- We breakdown electrical power systems into their basic elements.
- Describe their internal functions (emphasis on supporting power hibernation)
- Identify cold-electronic circuits (Digital, Analog, Discrete Devices, Passives)
- Identify issues and technology gaps

Cold Electronics: Power Systems Applications

Solar Array Power Generation

- Photovoltaic Solar Arrays are composed of semiconductor materials. Therefore, like electronics, performance is affected by temperature.
- Lunar Dawn is the coldest point of the lunar cycle.
- Output voltage increases with decreasing temperature due to increased electron mobility.
  - Efficiency rises until it peaks between -140°C to -170°C (133K to 103K).
  - Efficiency then declines as temperatures continue to decrease and carrier freezeout reduces available electrons.
  - Open circuit voltages are expected to be higher at cold temperatures.
- Over-voltage protection may be needed at lunar dawn.

Gaps

- Need characterization of array performance and OC voltages for Lunar Dawn temperature -173° to -223°C (100K-50K).

Cold Electronics: Power Systems Applications

Solar Array Regulation: Sequential Switching Shunt Regulator (S3R)

- Small spacecraft tend to use simple switching regulation schemes
- Arrays are arranged in parallel strings that are normally connected to the main bus.
- Switches shunt the output when main bus voltage exceeds preset limits.
- Array strings are shunted based on a preset sequence.

Cold Electronics (All need to be capable of a cold start.)

- S3R scheme employs analog op-amps as voltage comparators, voltage reference devices, diodes, switching transistors and various passives.

Gaps

- Cryo-Temperature characterization test data for S3R components is needed.

Cold Electronics: Power Systems Applications

Solar Array Regulation: Max Power Point Tracking (MPPT)

- Large modern spacecraft utilize array regulation that maximizes array efficiency.
- MPPT forces the array current/voltage to match the maximum power point for a given conditions. MPPT does this by varying the duty ratio of a DC-DC converter as a way of manipulating the impedance the array sees.

Cold Electronics

- The MPPT is managed by a digital algorithm that monitors array sensors and calculates the maximum power point and coordinates multiple voltage converters.
- Converters typically use a Pulse Width Modulation (PWM) regulation, switching elements, inductors, capacitors, various analog control devices.

Gaps

- Cryo-Temperature characterization of voltage converter components and supporting analog devices and Passives (Inductors, Capacitors)
- Need to demonstrate MPPT regulation cold-start and operation down to 50K

Cold Electronics: Power Systems Applications

Battery Management System: Charge Control

For small spacecraft battery charging is often managed by manipulating the voltage of the main bus. $V_{Bus} > V_{Batt}$ charges, while $V_{Bus} < V_{Batt}$ discharges.

- Li-Ion batteries need a Constant Current/Constant Voltage charge scheme.
- Hibernation & Recovery cells may be frozen at lunar dawn (0 volts output).
  - Battery is isolated from the main bus to prevent charging cold cells.
  - Cell charging is inhibited until warmed to normal operating temperatures.

Cold Electronics

- Battery CC/CV charge control needs digital and analog electronics capable of a cold start and operations to -223°C (50K).

Gaps

- Need to demonstrate a battery charge control cold start and operation at 50K.
- Need battery charge management guidelines for hibernation recovery protocol.

Cold Electronics: Power Systems Applications

Battery Management System: Thermal Control

For **Hibernation & Recovery** the BMS has an added role of managing the thermal recovery of the battery at lunar dawn.

- Differences in cell temperature can cause warm cells to charge cold cells.
- BMS coordinates heaters to assure cells warm-up uniformly.

Cold Electronics

- Thermal control requires digital and analog controls along with power switching capable of a cold start at temperatures as low as -223°C (50K).
- Note STMD funded work at GRC, called “ICE-CHILL”, is developing a BMS

Gaps

- Need to demonstrate a battery thermal control capable of a cold start and operation at 50K.
- Need battery thermal management guidelines for hibernation recovery protocol.

Cold Electronics: Power Systems Applications

Main Bus Controller (MBC):

For **Hibernation & Recovery**, the MBC manages the array regulation, enables battery management, controls battery isolation, and inhibits/enables avionics power.

- MBC cold-starts and operates on array output without a battery to stabilize the bus.
- MBC manages Array Regulation
- Inhibits large reactive loads, (motors) to avoid bus instability
- MBC manages power to recovery heaters.
- MBC coordinates with BMS for battery thermal recovery and charge control.
- MBC reconnects the battery via the isolation switch and enables power distribution.

Cold Electronics: Power Systems Applications

Main Bus Controller (MBC):

Cold Electronics

- MBC needs digital and analog controls instrumentation and power switching components capable of a cold start at -223°C (50K).
- MBC may require transient filters (passives) and transient voltage suppression (TVS) devices suitable for cryo-temperatures.

Gaps

- Need an integrated MBC ground demonstrator with Solar Arrays, Battery Management, and Power Distribution to demonstrate Hibernation Recovery.

Cold Electronics: Power Systems Applications

Power Distribution: Power distribution often involves stepping down main bus voltage, channelizing power, and assuring high power quality.

- Main bus can often have significant voltage swings and voltage transients
- DC-DC voltage conversion with filtering assures stable voltages.
- Channelized Power Enables load management switching. ON/OFF/RESET
  - Channels automatically isolate overcurrent faults.
  - Current Limiting suppresses current transients and reduce nuisance trips.
- **Cold Electronics:**
  - Digital controllers execute start-sequence and support load management.
  - DC-DC Conversion: Digital/analog controls, power switching, passives, filters
  - Analog controls detect faults and provide current limiting.
- **Note:** Fault trips based on thermal devices may not be reliable.

Cold Electronics: Power Systems Applications

Power Distribution: Gaps

- Analog fault detection, fault isolation and current limiting circuits need temperature compensation for reliable cryo-temperature operation.

Cold Electronics: Power Systems Applications

High Power Motor Drives:- Propellant Motors:
Artemis Human Landing Systems (HLS) program is using cryogenic propellants for all phases of flight.

Artemis In-Space Refueling Architecture
- Artemis architecture involves in-space refueling of cryogenic propellants
- Includes orbiting refueling stations with supporting tanker spacecraft
- The human lunar landers require storing propellants in LEO and Lunar Orbits

Recompression of Boil-Off gases .
- Compressors condense propellant vapors to minimize boil-off losses.
- Requires several kilowatts of power each.
- Requires motor drive electronics in-close proximity to cryo-propellants.

Cold Electronics: Power Systems Applications

High Power Motor Drives - High Power Electric Actuators:
NASA observing a shift from hydraulic to all-electric actuators.
- Landing of large reusable boosters owes their success to the application of lightweight, very responsive electric actuators for engine thrust vector control (TVC).
- These same electric TVC actuators will be used to land Artemis Lunar Landers.

High power eTVC actuators are made feasible by.
- High-power, light-weight permanent magnet Brushless DC (BLDC) motors,
- Fast acting motor control ASICs
- Distributed high power li-Ion batteries.
- Electronically controlled **Regenerative Braking**.
- Enable nearly instantaneous direction and speed changes.

Actuators and their drive electronics will be in the lunar environment.

Cold Electronics: Power Systems Applications

High Power Motor Drives

Cold Electronics

- Digital Microcontrollers for motor control algorithms
- DC-DC PWM power control including Power Passives.
- 3-phase motor commutation control
  - Hall Effect sensors
  - OR Sensorless schemes require digital signal processing
- Regenerative Braking Controls

Gaps:

- Need Hall Effect sensors suited for cryotemperatures
- Need Motor Drives proven for cryotemperature operation

Cold Electronics: Power Systems Applications

Transient Voltage Suppression: We are observing very large power bus voltage transients due to high-power electric motors for TVC. Regenerative Braking further aggravates the problem with current reversals and (+) voltages spikes.

Cold Electronics

Transient Filters: High voltage passives (Inductor, Capacitors, Resistors) can filter ripples but adds reactive impedance to the bus.

Transient Voltage Suppression (TVS) Device

- Transient Voltage Suppression (TVS) devices shunt excessive transient voltages.
- TVS devices are normal high-impedance but become low impedance when voltage exceeds a breakdown voltage **(V_{BD})** .
- TVS Breakdown Voltage **(V_{BD})** typically varies with temperature.
- V_{BD} Temperature Coefficient maybe **+ or -**

Cold Electronics: Power Systems Applications

Transient Voltage Suppression:

Zener Diode: Zener diodes are commonly used to clamp a voltage at a specific value.

- Two competing effects depending on the Zener Voltage **(V_Z),**
  - V_Z > 5V Avalanche Effect Dominates :
    - *Positive* Temperature Coefficient (V_{BD} Decreases with Decreasing T)
  - V_Z <5V Tunneling Effect Dominates :
    - *Negative* Temperature Coefficient (V_{BD} Increases with Decreasing T)

Transorb: Like a Zener but specifically designed for fast response and high voltages.

- Positive V_{BD} Temperature Coefficient (V_{BD} Decreases with Decreasing T)

Punch-Through Diode: Suited for very low voltage applications (3-volt or 1-volt).

- Positive V_{BD} Temperature Coefficient (V_{BD} Decreases with Decreasing T)

Cold Electronics: Power Systems Applications

Transient Voltage Suppression:

Metal-Oxide Varistor (MOV) Regarded as a non-linear resistor.

- Nominal high resistance drops when a threshold voltage is exceeded
- Conducts large currents to suppress a high voltage.
- MOV are Bi-Directional and work for both AC and DC circuits.
- ZnO based varistor $\mathbf{V_{BD}}$ has a very small dependence on temperature.
- MOVs may be suitable for cryo-temp operations as is.

Gaps

- Need comprehensive characterization of Transient Voltage Suppression devices for cryo-temperatures down to 50K.

Cold Electronics: Power Systems Applications

Analog Electronics for Power Applications at cryo-temperatures

Compared to digital or switching circuits, analog circuits are more sensitive to temperature.

- Analog signals are processed with transistors operating their linear region.
- Operating parameters that shift with temperature compromise signal integrity.
  - Analog circuits are highly dependent on stable reference voltages.
  - Drifting reference voltages can change the behavior of an analog circuit.
  - At cryotemperatures, severe parameter drift can cause erratic behavior.
- Analog ICs sometimes have built in "temperature compensation" to counteract the effects of temperature change. (particularly for reference voltages)
  - Temperature compensation rarely extends beyond the 125°C to -55°C range.
  - Compensation is more often applied to high side of the range.

Cold Electronics: Power Systems Applications

Analog Electronics for Power Applications at cryo-temperatures

Semiconductors: Most semiconductors conductivity improves with decreasing temperatures due to reduced thermal scattering thus increasing electron mobility.

- As temperatures drop into the cryogenic region the reduced thermal energy reduces the number of electrons in the conduction band (Carrier Freezeout).
- At extremely low temperatures the low thermal energy electrons (slower) are more susceptible to "charge or ionic scattering" and degrades electron mobility.
- Achieving high performance at cryogenic temperatures involves:
  - Techniques for sustaining electron population in absence of thermal generated electrons.
  - Avoiding the effects of charge scattering

Cold Electronics: Power Systems Applications

Analog Electronics for Power Applications at cryo-temperatures

Transistor Type: The type of transistor has a huge effect on low temperature performance. FET based devices continue to work at temperatures where bipolar devices fail. CMOS and HEMT transistors are less sensitive to temperature.

Semiconductor Devices suited for analog power applications down to 50K

- Silicon FDSOI (Fully Depleted Silicon-On-Insulator) CMOS may exploit "back bias" capability to compensate for temperature parameter drift.
- Silicon-Germanium HBT innately capable of extremely low temperatures. (requires custom fabrication).
- Gallium-Nitride HEMT (High Electron Mobility Transistors) the 2D Electron Gas (2DEG) reduces dependence of thermally generated carriers.

Cold Electronics: Power Systems Applications

Analog Electronics for Power Applications at Cryo-temperatures

Gaps:

- Need published guidelines on analog temperature compensation techniques for cryo-temperature applications at both component and circuit board level.
- Silicon-Germanium properties for analog applications at cryogenic temperatures are not well known
- FDSOI CMOS properties for analog applications for cryogenic temperatures and the potential use of "back bias" for temperature compensation is not well known.
- Lack of available GaN beyond simple discrete devices limits applications.

Cold Electronics: Power Systems Applications

Digital Electronics for Power Applications at Cryo-temperatures

Digital microcontrollers or FPGAs are widely used for spacecraft power systems to provide solar array management, battery management, power conversion, power distribution, along with housekeeping and command & data handling.

- Digital electronics transistors operate in the saturation region and are less sensitive to temperature.
- CMOS technology is most widely used for microprocessor scale logic.
- Some COTS digital microcontrollers and FPGAs have demonstrated cryo-temperature operation.
- FDSOI-CMOS may be well suited to digital applications at cryo-temperatures

Gaps

- Need further evaluations of COTS digital devices for cold-start and operations at 50K.

Cold Electronics: Power Systems Applications

Mixed Signal Devices for Power Applications at Cryo-temperatures .

Many microcontrollers and ASIC devices have a digital core with analog features such as, signal amplifiers, comparators, voltage references, A/D and D/A converters and load drivers. Motor controllers are an example of a mixed signal device.

- COTS mixed signal tests at cryotemperatures have shown that digital functions work while the analog functions act erratically particularly in cold-start operation.
- COTS mixed signal device may not be suited for cryotemperatures.
- May need to keep Digital and Analog devices separate.

Gaps:

- Need an approach for mixed signal devices at cryo-temperatures.
- Need to determine a semiconductor of choice for mixed signal applications at cryo-temperatures.

Cold Electronics: Power Systems Applications

Power Switching Transistors for Power Applications at Cryo-temperatures

Simple discrete switching elements provide high-speed switching for pulse width modulation of power, and motor phase commutation.

- Si MOSFETS at 50K become less efficient and exhibit decreasing breakdown voltage.
- SiGe HBT is well suited to cryo-temperatures but have low breakdown voltage.
- Silicon-Carbide has decreasing efficiency at cryo-temperatures.

- **Gallium-Nitride (GaN) HEMT** devices are efficient and stable over a wide temperature range and demonstrated cold-start as low as 10K.
- GRC testing of GaN devices in 2017 revealed that GaN exhibits usually flat response to temperature in the range from Room Temperature to -196°C (77K) when compared to Si and SiC.

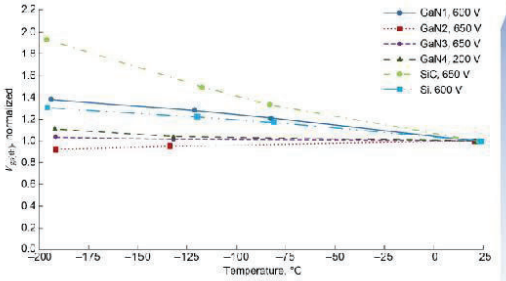


Figure 11.—Normalized gate-to-source threshold voltage ($V_{GS(th)}$) for GaN, SiC, and Si devices.

Cold Electronics: Power Systems Applications

Power Switching Transistors for power applications at cryotemperatures

STMD Funded work by Prof Zhang of Rensselaer Polytechnic Institute investigates Gallium-Nitride HEMT devices for the 400K to 50K temperature range.

- Characterizing COTS GaN device performance.
- Performing reliability studies of COTS GaN devices
- Developing a Physics Informed Models
- Developing GaN based power circuits suited for power hibernation applications.

Gaps:

- GaN is widely available as COTS discrete devices.
- GaN cryogenic performance are not well known in industry.
- Should investigate the potential of complex All-GaN ICs.
- Need GaN qualification protocol for long operating life for lunar applications.

Cold Electronics: Power Systems Applications

Passives for Power Applications at Cryotemperatures

Inductors, Resistors, Capacitors (LRC) Passives are essential for high-power applications. Their cryogenic performance is based on the material properties.

Studies have evaluated passive devices at cryotemperatures.

- Certain COTS passives are suitable for cryogenic temperature operations.
- Metal film and wire wound resistors are insensitive to temperature
- Liquid Electrolytic capacitors are not suitable for cryotemperature applications.
- Capacitors suited to cryotemperatures tend to have less capacitance
- Capacitors based on Radiation Crosslinked Acrylate Monomers can maintain high performance at cryogenic temperatures. Requires custom fabrication.
- Nano-crystalline and Amorphous Inductor cores are best suited to cryotemps.

Gaps:

- Need a comprehensive guideline of power LRC passives at 50K

Cold Electronics: Power Systems Applications

Summary

Cold Electronics for Power Applications:

- Enables Hibernation and Recovery for robotic missions
- Immediately applicable to extending operational life CLPS Missions
- Hibernation should be considered a baseline capability for future CLPS Missions
- Analog Electronics are sensitive to temperatures and need
  - Temperature compensation techniques for wide temperature range operation.
  - Employ semiconductors/transistors technologies suited to cryotemperatures
- Switching Devices and Passives appear to have COTS solutions.

High power motors/drive electronics in cold environments.

- Power & Motor Controller ICs are often mixed signal devices.
- May need Transient Voltage Suppression.
- GaN appears suited for power switching at cryotemperatures.

NESC Technical Assessment Meeting
Cold Electronics for Lunar Missions
TI-22-01873

Section 7.8 Energy Storage

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Bottom Line Upfront

- Energy storage in the form of batteries is critical to all missions but significant challenges operating at temperature <-20°C
- COTS Li-ion battery cells require careful thermal management to keep within data sheet values; operating outside these limits requires testing
- Customizing Li-ion cells can allow low-rate discharge as low as -60°C, however, higher rate discharge and charging in general at reduced temperatures remain significant challenge
- Breaking through this limit will require the development of fundamentally new batteries chemistries (low TRL development)
- Current goal is to evolve to wider temperature operation through modifications to existing chemistries combined with thermal management, with longer term investments in new battery chemistries

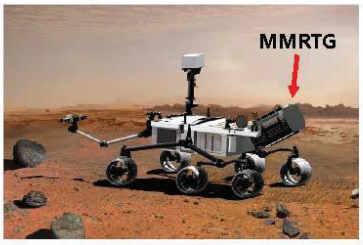
1

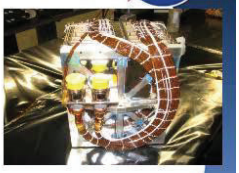
Outline

- Background
- Survival vs. Operation
- State of practice
- Li plating concerns
- Advanced low temperature chemistries
- Gap Analysis

Background

- **Energy storage is used on all spacecraft today**
  - Load levelling to support peak power demands
  - Power during eclipse periods
  - Power for nighttime operations
- **Charged with solar arrays or radioisotope thermoelectric generators (RTGs)**
- **Since 2001 when it was first used on the ESA PROBA-1 spacecraft, Li-ion battery technology use in space has been growing and is now the predominant energy storage technology**
- **Battery modules use series/parallel strings of individual cells**
  - Number of cells in string determines battery voltage
  - Number of strings determines battery capacity





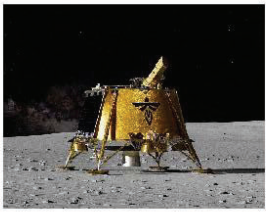
Curiosity Rover with RTG and Li-ion battery module using prismatic cells

Europa Clipper with solar arrays and Li-ion battery module using small cylindrical cells

Survival vs. Operation at Cryogenic Temperatures

Japan's SLIM moon lander, including battery, survived three freeze-thaw cycles on the lunar surface

Mars Helicopter battery survived 341 freeze-thaw cycles on the surface of Mars



Blue Ghost Lander did not survive a lunar night

CLPS lander will likely require a hibernation mode for future missions

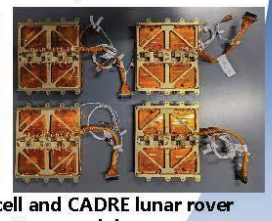
- **Survival can be achieved by waking up and "thawing" after a freeze cycle**
- **Operation during cold soaks requires thermal management or advanced cell chemistry**

4

State of Practice (1/2)

- Space rated battery cells are available in two basic formats, prismatic and cylindrical
- Early flight batteries were typically comprised of prismatic cells that were custom designed and fabricated for space applications
- Some recent missions, such as Dragonfly and Psyche, still use this format although it is becoming less common
- Today, commercial-off-the-shelf (COTS) cylindrical cells have been widely adopted for space applications
- These COTS cells are the same type used in many terrestrial electrical vehicles and consumer electronics

Custom Yardney prismatic Li-ion cells and MER battery module



Saft Li-ion cell and CADRE lunar rover battery modules

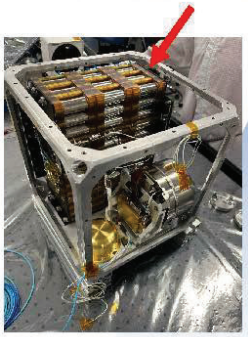
COTS Sony 18650 Li-ion cells used on Ingenuity Helicopter

5

State of Practice (2/2)

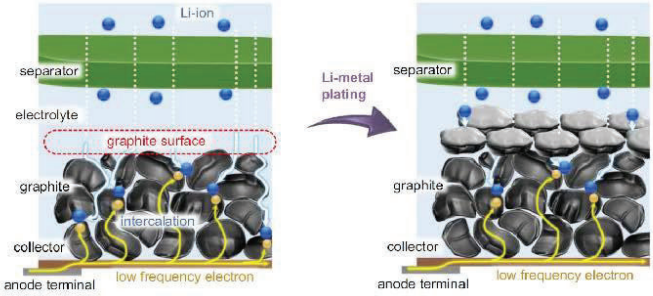
- **Batteries tend to drive thermal design of the power system**
- **Mars Exploration Rover prismatic cell battery**
  - Two radioisotope heating units per battery
  - Aerogel insulation
  - Thermal switches
  - Survival heaters
  - Modified cell electrolyte
- **Farside Seismic Suite (FSS) 18650 cylindrical cell battery**
  - Features Planetary and Lunar Environment Thermal Toolbox Elements (PALETTE) technology with inner and outer enclosures
  - Inner enclosure isolated by titanium tubes and surrounded by spacer-less multi-layer insulation layers
  - Variable conductance thermal path from the inner enclosure to the outer enclosure
  - Survival heaters
- **Typical low temperature limits for COTS cell is -20°C**
- **Widening the allowable flight temperatures (AFTs) for the cells reduces mass and power overhead as well as complexity associated with thermal management, even if not cryogenic capable**

MER prismatic cell battery module



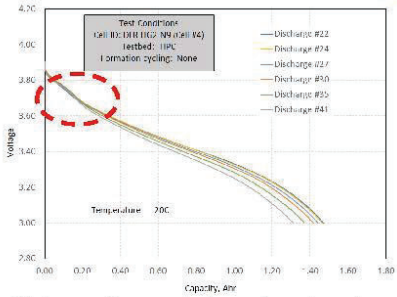
FSS small cell battery module

Li Plating During Charging at Low Temperatures



Schematic view of lithium plating on graphite anode during charging

Nature Communications | (2023) 14:7275 (open source)

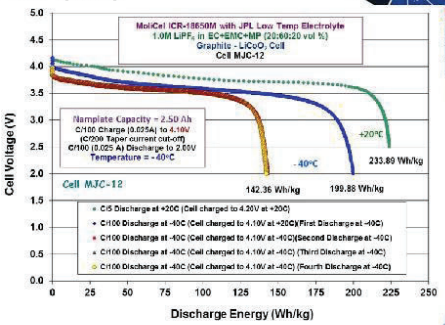


Voltage plateau during after charging at -20C (COTS Li-ion cell)

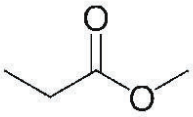
- Conventional COTS Li-ion battery anodes display signs of lithium plating during charging
- Li metal does not intercalate into electrode, but "plates" as a metal on the surface
- Can build up dendrites which can puncture battery separator, leading to internal cell shorting and safety concerns
- Observed as voltage plateau in the discharge curve

Advanced Li-ion Chemistries (1/3)

- Performance of cells is largely dictated by the cell chemistry, which in the case of COTS Li-ion technology means the use of:
  - Graphite anode
  - Metal oxide cathode (such as $LiNi_{0.8}Mn_{0.1}Co_{0.1}O_2$) and
  - Lithium-ion salt (such as $LiPF_6$) dissolved in a blend of organic carbonates for the liquid electrolyte
- Capacity and overall performance of the cell is dictated by the electrode couple: difficult to deviate from the state-of-the-art technologies that are incorporated into well-manufactured COTS cells
- Most logical component to alter to improve wide temperature performance is the electrolyte since it is easier to customize and incorporate into existing cell designs.
- Melting point of the electrolyte needs to be reduced to prevent freezing
- The conductivity of the electrolyte drops at low temperature due to viscosity effects and reduced transport of the ions, and the performance at low temperature can be improved by altering the electrolyte to minimize the impact of these phenomena
- Lithium plating is a concern during charging at low temperature
- Discharging down to -90°C has been demonstrated



High specific energy at -40°C observed when using a low-rate charge and discharge (100 hours) with Moli 18650 cells using modified low temperature electrolytes. No lithium plating observed when charging to 4.10V at -40°C using low-rate charge



Methyl propionate electrolyte component has a m.p. of −88 °C

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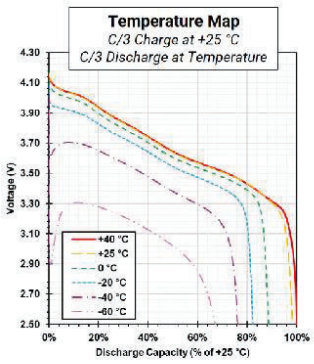
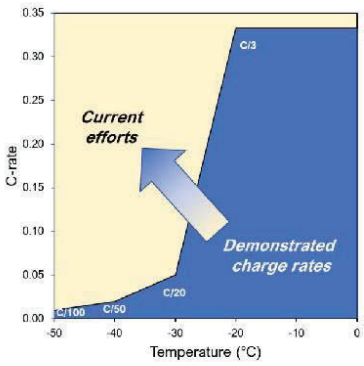
Advanced Li-ion Chemistries (2/3)





- Option to use gas electrolytes in place of traditional liquid electrolytes
- South8 gas electrolyte cells above, showing discharge down to -60°C after charging at +25°C (left) and map of allowable charge rates and temperature, showing charging at only very low rates at <-30°C is possible (2.7 Ah 18650 cell with graphite anode and NMC811 cathode)

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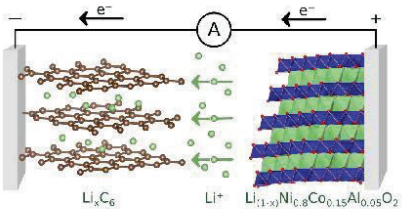
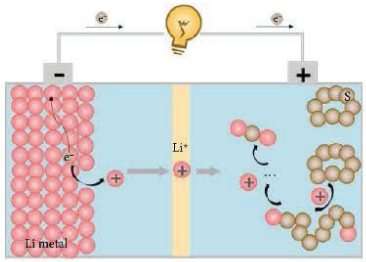
Advanced Li-ion Chemistries (3/3)



Conventional Li-ion: Intercalation electrodes



Li-metal anode/conversion cathode

Sulfuryl chloride fluoride (SO_2ClF)
m.p. -125°C, b.p. 7°C

chlorodifluoromethane ($CHClF_2$)
m.p. -175°C, b.p. -41°C

- Conversion electrodes that react and undergo phase changes during operation (Li metal, sulfur, silicon, etc.) often do not suffer from the same rate limitations of intercalation electrodes used in COTS cells
- Limited cycle life and low TRL
- Could be combined with advanced or non-traditional electrolytes for both rechargeable and primary cells

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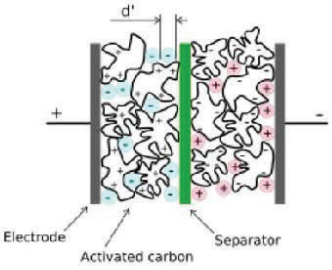
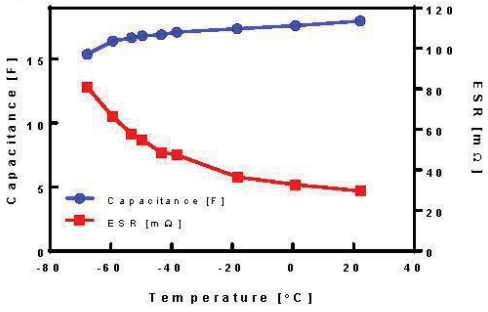
Double Layer Capacitors (Supercapacitors, Ultracapacitors)

Electrochemical double-layer



Charge stored at surface of two high surface area carbon electrodes



Custom double-layer capacitor modified for low temperature operation to -70°C

- Double-layer capacitors can offer operation to temperatures <-40°C
- Capacity stored at the electrochemical double-layer, formed at the interface of a liquid electrolyte and two high surface area electrodes (no plating concerns)
- Critical electrolyte design factors: minimize solvent viscosity and achieving a high dielectric constant to avoid the precipitation of the electrolyte salt at low temperatures
- Does not depend on thermally activated processes related to intercalation and chemical conversion of the electrodes
- Higher rates are also possible relative to Li-ion technology
- Much lower specific energy relative to lithium-ion battery technology (5-20 Wh/kg vs. 250-300 Wh/kg)

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Gap Analysis

Gap 1. Li-ion batteries can be discharged as low as -60 to -90°C at low rates, however, they cannot be charged at these temperatures due to issues with Li plating

Gap 2. Li-ion cells cannot be discharged at high rates at temperature <-40°C

Gap. 3. The effects on battery lifetime during electrical and thermal cycling at low temperatures are not well understood, with inadequate data and models to evaluate the effects of plating on lifetime as well as the mechanical effects of multiple freeze-thaw cycles

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Gap Analysis

Gap 4. Traditional intercalation electrodes based on graphite and used for most Li-ion cells today limit performance of cells. Alternative and conversion electrodes based on lithium titanate, silicon, lithium metal or on electrochemically active liquid systems offer approaches for operating <-80°C and have been recently study but are at TRL<3 for use in space applications.

Gap 5. Electrochemical methods for energy storage are unlikely to support adequate energy storage at cryogenic temperature, due to fundamental limitations with thermally activated processes.

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NESC Technical Assessment Meeting
Cold Electronics for Lunar Missions
TI-22-01873

Section 7.4 – COTS/MIL Cold Electronics

Jean Yang-Scharlotta
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Bottom Line Up Front

- Extending the operation temperature for COTS and MIL components **not designed for cold operation** has been another primary methods to support cold operation
- Significant test literature has been generated by NASA and other to demonstrate operation capability in cold environments below the -55°C MIL SPEC low temperature limit for a wide variety of **off-the-shelf** parts
- There are inherit risks and limits in operating components outside of their designed temperature ranges, which needs to be managed by careful technology selection, characterization and qualification
- Some electrical parameter deviations is to be expected. Therefore, identifying the mission temperature requirements, as well as application specific requirements and tolerance of the whole system for the electrical parameter deviations at cryogenic temperatures is necessary to design the qualification.
- Since the cold operation is not designed-in and rely on design margin, performance at cold can have high variation from lot to lot
- Some general trends do exist based on technology and architecture

Outline

- Overview of Literature Survey
- *Technologies*
  - *MOSFETS*
  - *Si BJT & SiGe HBT*
  - *GaN*

- *Integrated Circuits (examples shown, complete list will be hosted by NASA NEPP website)*
  - FPGA
  - Micro-controller
  - Memory
  - OP amps
  - ADC
  - DCDC

Literature Survey Findings

- Integrated circuit component data available on
  - FPGA
  - Micro-controller
  - ADC
  - DCDC
  - OP amps
  - Transistors
  - Diodes
  - Memory

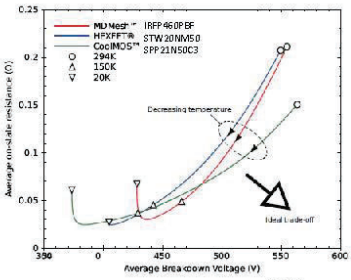
- Variety and quantity of parts shown to function at extreme cold suggest that utilization of COTS for cold capable electronic systems is feasible with careful selection, testing and validation

- Most of published data focused on functionality and very limited data available on reliability

- Cold start data is also limited

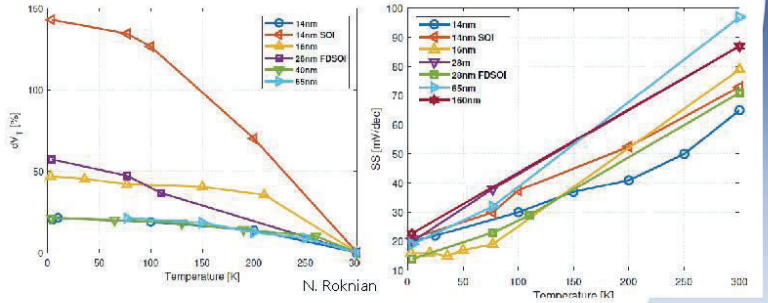
MOSFETS

- MOSFETS continue to function at cold temperatures allowing both power MOSFETS and highly scaled CMOS ICs to work at cold with some deviations in key parameters



K. K. Leong

Power MOSFETS from 3 different vendors all show functionality down to 20K

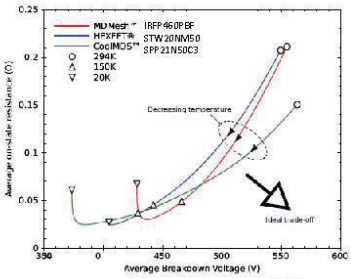


N. Roknian

Submicron MOSFETS across technologies all show similar increase in threshold voltage and effective mobility along with a decrease of the subthreshold slope

MOSFETS

- MOSFETS continue to function at cold temperatures allowing both power MOSFETS and highly scaled CMOS ICs to work at cold with some deviations in key parameters



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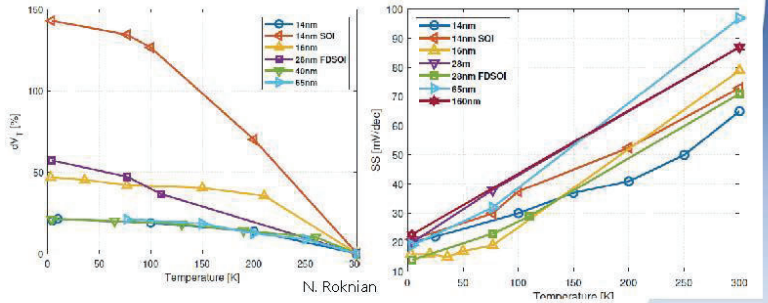
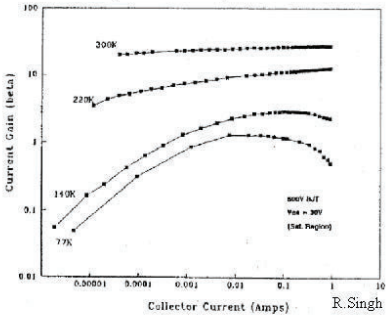


N. Roknian

Submicron MOSFETS across technologies all show similar increase in threshold voltage and effective mobility along with a decrease of the subthreshold slope

Si BJT and SiGe HBT

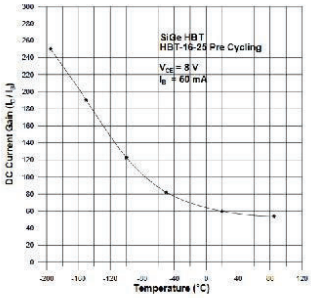
- Si BJTs current gain degrades rapidly with cold
- SiGe heterojunction bipolar transistors (HBT) actually sees increase in current gain with cold



R.Singh

Si BJTs exhibit a **strong decrease** of the DC current gain, beta (β=Ic/Ib), and a large increase in the base resistance

DC gain (I_C / I_B) as a function of temperature for a SiGe Heterojunction Bipolar Transistor (HBT)



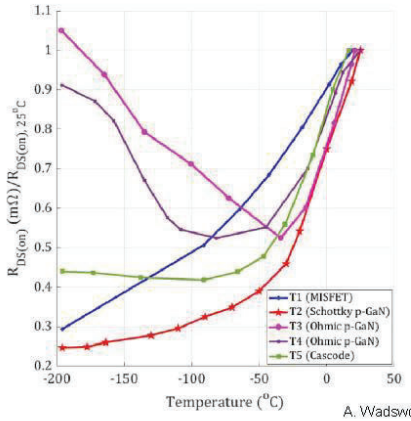
R. L. Patterson

HBT DC gain increase with drop in temperature but **actual increase is very technology dependent** due to exponential dependence of gain on actual Ge content in the base

J. C. Bardin

GaN

- Enhancement mode GaN high electron mobility transistors (HEMT) technology has matured recently now found in a variety of consumer and automotive power applications and there is at least one vendor providing MIL SPEC GaN HEMT
- GaN HEMT of various gate technologies were tested and all have lower or similar Rds(on) at cold than at room temp.



A. Wadsworth

Fig 4. GaN HEMT $R_{DS(ON)}$ Temperature Variation

FPGAs

- A variety of FPGAs have been shown to function at cold temperatures with performance deviations, a few will function at temperature as low as 4K

Part ID	Technology	Operable Low Temp Limit	Comments
AC3S250 [72]	CMOS (90nm)	123 K	Functional <2% change in power down to 123 K. No data available below 123 K.
AGL1000 [72]	CMOS (130nm)	123 K	Functional digital modem to 143 K, core power drops 30% at 133 K.
AGL125 [72]	CMOS (130nm)	123 K	Functional and reprogrammable to 133 K. Cloc stability issues at 153 K. No data available below 123 K.
AGLN250V2 [72]	CMOS (130nm)	123 K	Functional with 10X current drop at 143 K. Flash freeze functional with 100X in reduction in standby current. No data available below 12 K.
Arria GX [42]	CMOS (90nm)	77K	Screening test included configuration (JTAG & Active Serial), embedded memory, high speed transceiver, I/O interface. No data available below 77K.
Arria II [42]	CMOS (40nm)	N/A	Not selected for cryogenic application after col screening. No data available for failure criteria.
Artix-7 [44] XC7A100T-2FTG256I	CMOS (28nm)	4K	See Table 7 for functional data at cold temp..
Artix-7 [48] XC7A50T-2FGG484C	CMOS (28nm)	4 K	Mostly functional down to 4 K. But the commo mode and differential output voltage decrease dramatically below 50 K (likely linked to internal bandgap voltage reference offsets at lo temp). See Table 6 for functional data at cold temp.

	Artix-7		Spartan-6		Spartan-3	
	300 K	4 K	300 K	4 K	300 K	4 K
V_{IH} single-ended LVCMOS (V)	1.16	1.22	2.39	2.51	1.50	1.61
V_{IL} single-ended LVCMOS (V)	1.09	1.11	2.14	2.24	1.42	1.47
V_{IH} differential LVDS (mV)	5	18	11	11	18	13
V_{IL} differential LVDS (mV)	-39	-55	18	-33	-39	-35
Pull-up resistance (kΩ)	20	17	10	7.7	10	6.6
Differential resistance (Ω)	96	86	101	93	108	105
Differential output voltage (mV)	435	42	372	1569*	387	582*
Common-mode differential output voltage (mV)	1120	227	1242	1202*	1056	1652*

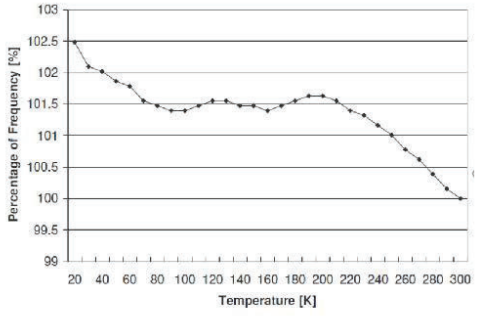
H. Homulle

Comparison of AMD FPGA IO parameters between room temp and 4 K. Common mode voltage of 1.2V used for LVDS

Microcontrollers

- Microcontroller- CMOS microcontroller has been shown to function down to 20K with some internal clock frequency shift.

Part ID	Technology	Operable Low Temp Limit	Comments
PIC16876A DIP [23]		150 K	No data available.
ATTiny26 SMD [23]	CMOS 8-bit RISC architecture	20 K	Internal clock freq. variation (Fig. 15) at deep cryogenic temperature can cause synchronization issue between internal clock and UART bus speed. No data available below 20 K.
ATMega16 SMD [23]	CMOS 8-bit RISC architecture	20 K	Internal clock freq. varies with temp. No data available below 20 K.

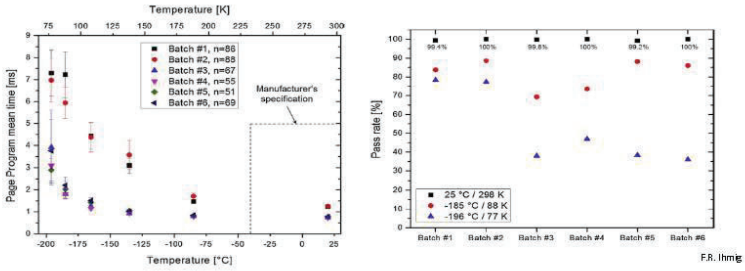


P. C. van Niekerk

Internal clock frequency deviation of the Microchip ATTiny26 as a function of temperature

Memories

- Flash memories have been shown to work consistently at 77K



F.R. Ihmig

- Same manufacturer, each batch is a single lot from a single technology and manufacturing location.
- Over 3600 parts tested
- Program time and pass rate for extreme low temperature operation are very batch dependent.

- Most parts fail for program or erase, which require higher voltages

large batch-to-batch variation can be the norm as one seeks to use COTs components outside of the specified temperature range

Op Amps

- Test results for op amps tend to vary at cold and show some technology correlation

Part ID	Technology	Operable Low Temp Limit	Comments
AD627 [38]	BiCMOS	153 K	Non-significant variation in performance down to 153K. No data available below 153 K.
AD8572 [38]	CMOS	153 K	Functional but abnormal behavior in offset voltage and spot noise observed at 153K. No data available below 153 K.
ADC8652 [88]	CMOS	77 K	Cold screened and selected for 77 K application. No data available below 77K.
ADA4807-4 [41]	BJT	N/A	Not selected for cryogenic application after cold screening. No data available for failure criteria.
CHT-OPA [48]	SOI	83 K	Maintained very good operation between down to 83 K. The limited thermal cycling had no effect on the performance of the amplifier. No data available below 83 K.
HT-1104 [49]	SOI	78 K	Good functionality down to 78 K. No data available below 78K.
HTOP-01 [49]	SOI	83 K	Good functionality down to 83 K. No data available below 83 K.
ICL7611 [40], [43]	CMOS	4 K	Open-loop gain, input offset voltage, input referred noise voltage, and quiescent current were characterized.
LM2904WH [69]	CMOS	123 K	Good functionality down to 123 K. No data available below 123 K.
LM412 [23]	BJT with JFET input	120 K	Tested in the inverting amplitude configuration with gain of 10. Failure criteria: clip in output swing, decrease in gain bandwidth.
LM6144 [38]	BJT	213 K	Significant degradation in gain bandwidth.

Analog to Digital Converter

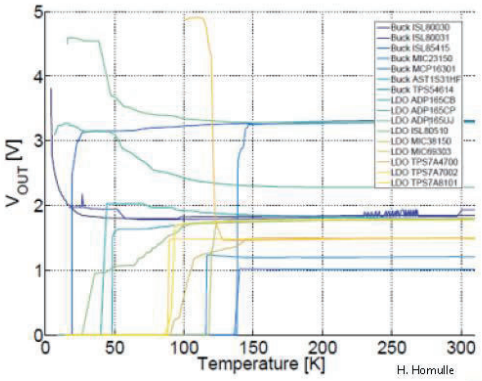
- Several ADCs shown to operate down to near LN3 temperature (77K), typical degradations include lost of accuracy and loss of internal reference.

Part ID	Technology	Operable Low Temp Limit	Comments
AD4000 (16bit) [61]	CMOS (180nm)	N/A	Not selected for cryogenic application after cold screening. No data available for failure criteria.
AD6645 (14bit) [70]	Complementary BJT	93 K	Loses 5~6 bits of accuracy at 93K. No data available below 93 K.
AD7274 (12bit) [61]	CMOS (350nm)	77K	Based on preliminary long term reliability test, projected lifetime is ~$6X10^6$ years at 2.5V, 150 yrs at 3.6V for 77K operation (based on I_{cc} drop of 1% as degradation criteria). [63]-[64]. Cold screening yield 100%. No data available below 77K.
AD7276 (12bit) [61]	CMOS (350nm)	N/A	Not selected for cryogenic application after cold screening. No data available for failure criteria.
ADS7049-Q1 (12bit) [61], [64]	CMOS (500nm)	77 K	Cold screening yield 100%. No data available below 77K.
ADS7808 (12bit) [74]	CMOS	83 K	Operable down to 83 K with external voltage reference. Fluctuation in internal reference voltage observed ~198 K. No data available below 83 K.
ADS7883 (12bit) [61]	CMOS (180nm)	77 K	Cold screening yield 100% Missing code with large input signal at 77K. No data available below 77K.
ADS9225 (12bit) [75]	CMOS	93 K	Functional down to 93 K. Performance degradation observed at low temp (Fig. 18). No data available below 93K.
LTC1419 (14bit) [73]	CMOS	83 K	Operable down to 83 K with 1.25V external reference. Internal Vref drops from 2.5 V to 0.906V ~213 K. Noticeable increase in offset between the input and measured output voltage was observed (Table 9). No data available below 83 K.

Voltage Regulator

- Voltage regulator test literature shows many candidates can function down to ~150K but significant change in Vout can occur below 150K

Part ID	Type	Operable Low Temp Limit	Comments
1003S12HN [67]	Buck	93 K	Oscillation in input current observed at 133 K under heavy loading.
24S3.15HE [67]	Buck	233 K	Although the module ceased to work at 233 K during steady state, it worked down to 173 K when tested under a step change in load from full to no-load and vice-versa.
ADM7151 [82]	LDO	77 K	Cold screened and selected for 77 K application. Sight decrease in output voltage at 77 K (<2%). No data available below 77 K.
ADM7155 [82]	LDO	77 K	Cold screened and selected for 77 K application. Sight decrease in output voltage at 77 K (<2%). No data available below 77 K.
ADP165CB [71]	LDO	163 K	Failure criteria: 2.5% margin on the voltage at 300 K (Figure19).
ADP165CP [71]	LDO	125 K	Failure criteria: 2.5% margin on the voltage at 300 K (Figure19).
ADP165UJ [71]	LDO	99 K	Failure criteria: 2.5% margin on the voltage at 300 K (Figure19).
ASD10-12S3 [67]	Buck	113 K	Vout dropped to 2.4 V at 133 K. Chip functioned down to 113 K.
AST1S3HF [71]	Buck	117 K	Failure criteria: 2.5% margin on the voltage at 300 K (Figure19).
CHT-LD-033 [83]	LDO	78 K	Slight decrease (~1%) in output voltage at 78K with high input (Fig. 20). Stable overall performance down to 78K. No data available below 78 K.



Gaps

- Reliability characterization is very limited, qualification is needed based on mission temperature, time, and application tolerance to specific parameter change due to temperature
- Cold start characterization is needed to be part of the qualification plan if this is a function required by the mission

Questions

- Anything we've missed wrt parts tested at low temp.?
- Anything we're not aware of wrt behavior of xistors & components at low temp.?
- Which COTS parts/part types would be of most interest to the community for near to mid-term missions?
- Testing optimization methods?

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TI-22-01873

Cold Electronics: Passive Devices

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Power Architecture and Analysis Branch
NASA Glenn Research Center
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5/16/2025

Cold Electronics: Passive Devices

Passives Devices: Inductors, Resistors, Capacitors (L,R,C)
Non-Semiconductor, passive components are essential for analog electronics since the days of vacuum tubes.

- Particularly essential for radio frequency, and electrical power applications.
- The construction materials selection affects performance.
- In cryo-temperature applications the material property dependence on temperature often governs how the passive's performance changes with temperature.
- Many cryotemperature applications have multiple COTS solutions.

Cold Electronics: Passive Devices

Passive Devices: Resistors

- Resistors have a positive Temperature Coefficient of Resistance (TCR)
- The table below is based on NEPP funded work performed by NASA GRC.

Performance of Various Types of Resistors at Low Temperatures

Type	Value (Ω)	Temp Coeff (ppm/°C)	Resistance (Ω) at 25 °C	Resistance (Ω) at -190 °C	Change in Res (%) at -190 °C
Metal Film	10	±25 to ±200	10	9.99	0.0
	1K	±50	999.15	1001.86	0.3
Wirewound	10	±30	9.7	9.62	-0.9
	1K	±30	984.8	979.31	-0.6
Thin Film	33	±250	33.07	34.32	3.8
	1K	±100	995.41	1007.88	1.3
Thick Film	100	±100	99.99	105.42	5.4
	1K	±100	998.7	1003.22	0.5
Carbon Film	10	±350	9.96	10.46	5.1
	1K	-450	980.3	1035.83	5.7
Carbon Composition	15	n/a	14.65	16.34	11.6
	1K	n/a	1013.29	1296.54	28.0
Ceramic Composition	10	-1300±300	9.49	10.99	15.8
	1K	-1300±300	993.09	1167.51	17.6
Power Film	10	-20 to +50	10	10.48	4.9
	1K	-20 to +50	996.2	1037.06	4.1

R. Patterson, A. Hammoud, and S. Gerber, "Performance of Various Types of Resistors at Low Temperatures," Test Report, 2001.

Cold Electronics: Passive Devices

Passive Devices: Resistors: Performance of Various Resistors at 25°C (298K) and -190°C (83K)

- **Metal Film** TCR values vary (+/- 25ppm to +/-200ppm) but selected resistors can provide near 0% change in resistance
- **Wire Wound** TCR (+/- 30ppm) provides less than 1% change in resistance.
  - *Note:* Select wire wound resistors using bifilar winding or Ayrton-Perry winding techniques to minimize inductance.
- **Thin Film, Thick Film, Carbon Film, Power Film:**
  - Exhibited widely ranging TCR values. Provided an intermediate range of resistance shift. (0.5 % to 5.7%)
- **Carbon Composite and Ceramic Composite:**
  - Exhibited a huge range of TCR values with substantial resistance shifts of (11.6% to 28%). Not recommended.
- Resistors suited for cryo-temperature operation are available as COTS.

Cold Electronics: Passive Devices

Passive Devices: Resistors

Thermistors: special class of resistors employing materials with high TCRs and thus sensitive to temperatures.

- Thermistors are available with both Positive and Negative Temperature Coefficient.
  - PTC Thermistors are formulated to have non-linear sensitivity to temperature are commonly used as circuit protection devices.
  - NTC Thermistors, unlike common resistors, are based on semiconductor materials and typically used in temperature sensing.
- Thermistors can be used in electronic temperature compensation circuits where resistance changes with temperature is used to compensate for electronic parameter drift.
- Temperature compensation is often limited of -55 °C to +125 °C and most often focused on the high temperature side.

Cold Electronics: Passive Devices

Passive Devices: Capacitors

- "Air Gap" capacitor is not affected by temperature but has low capacitance relative to is size.

Capacitance dependence on temperature

- Capacitance depends on the permittivity of the dielectric material between the plates.
- Permittivity is related to the ability of a material dipoles to align with the electric field.
- Cryogenic temperatures may inhibit dipole alignment, reduce permittivity, and reduce capacitance.

Capacitance and Dissipation Factor between RT and -196°C (77K)

Material	Ceramic NP0	Ceramic: X7R	Ceramic: Y5Y	Ceramic: Z5U	Poly-propylene	PPS Film	Poly-ester	Poly-carbonate	MICA	Electro-lytic	Solid Tantalum
Capacitance	Stable	Major Decrease	Major Decrease	Major Decrease	Stable	Stable	Slight Decrease	Slight Decrease	Stable	Major Decrease	Slight Decrease
Dissipation Factor	Stable	Major Increase	Major Increase	Major Increase	Slight Decrease	Stable	Slight Decrease	Slight Decrease	Stable	Major Decrease	Major Increase

H. Gui et al., "Review of Power Electronics Components at Cryogenic Temperatures," in IEEE Transactions on Power Electronics, vol. 35, no. 5, pp. 5144-5156, May 2020, doi: 10.1109/TPEL.2019.2944781.

- Stable (unchanged) between RT at Cryo-temperatures.

Cold Electronics: Passive Devices

Passive Devices: Capacitors

Electrolytic Capacitors

- (Liquid) Electrolytic Capacitors will freeze and are not suited for cryo-temperature operation.
- Solid Tantalum Electrolytic Capacitors will tolerate the environment but have substantial parameter shifts, particularly at high frequency.
  - Capacitance is reduced
  - ESR (equivalent series resistance) climbs.

New Thin Film Capacitors

- Capacitors based on **Radiation Crosslinked Acrylate Monomer** dielectric by PolyCharge America has been tested down to -200°C (73K)
- Slight reduction in Capacitance, Improved Dissipation Factor, Improved ESR at cryotemperatures.
- Substantially higher energy density than common MLCC
- These capacitors appear suited for cryotemperature power applications.
- May need to be custom manufactured.

Cold Electronics: Passive Devices

Passive Devices: Inductors

- Simple coreless or "air-core" inductors are immune to cryo-temperatures effects.
  - They have low inductance for their size.
  - They also have an open magnetic field that can interact with other components.
- Solid cores can increase the inductance and provide wider bandwidth performance but may introduce some losses.
  - Cores also serve to contain the magnetic field and avoid interference with other devices.
  - Solid cores are generally made of metal laminations or powdered metallic materials in a binder matrix to prevent eddy current losses.
  - Core materials include iron powder, manganese-zinc ferrite, molybdenum permalloy powder, nickel-zinc ferrite, silicon steel, and many proprietary material blends.
  - Core material properties may be sensitive to temperature.

Cold Electronics: Passive Devices

Passive Devices: Inductors

- In the Table below, the changes in core properties from RT to -196°C(77K) are compared
- Ferrite cores exhibit large shifts in inductance and loss and not suited to cryo-temperatures applications,

Comparison of Core Materials at Cryogenic Temperature with Room Temperatures

Core Material	Molybdenum Permalloy Powder	High Flux Powder	Kool Mu Powder	Nano-Crystalline	Amorphous	Ferrite
Permeability	Stable	Stable	Decrease	Increases	Stable	Major Decrease
Loss	Increases	Stable	Stable	Increases	Increases	Major Increase
Saturation	-	-	-	Increases	Increase	-

H. Gui et al., "Review of Power Electronics Components at Cryogenic Temperatures," in IEEE Transactions on Power Electronics, vol. 35, no. 5, pp. 5144-5156, May 2020, doi: 10.1109/TPEL.2019.2944781.

- Nano-crystalline and Amorphous magnetic cores are stable or improve slightly at cryo-temperatures.
- Proprietary powder blend "High Flux" appears to be the most stable over the temperature range.

Cold Electronics: Passive Devices

Passive Devices: Gaps

- Need to further investigate thermistors as temperature compensation devices for cryo-temperatures
- Many Resistors and Capacitors suited to cryo-temperatures are available as COTS. However, their properties at cryo-temperatures are not widely published by manufacturers.
- Radiation Crosslinked Acrylate Monomer film capacitors have good cryo-temperature properties but may require custom fabrication.
- Inductor core materials with low sensitivity to temperature are available commercially but cryotemperature performance is not widely published.

In Summary

- **There appears to be multiple options for COTS passive devices**
- **May need to account for parameter shift over a wide temperature range.**
- **May need custom manufacturing for best performance.**

NESC Technical Assessment Meeting
Cold Electronics for Lunar Missions
TI-22-01873

Section 7.7 Electronic Packaging for Cold Environment

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Bottom Line Up Front

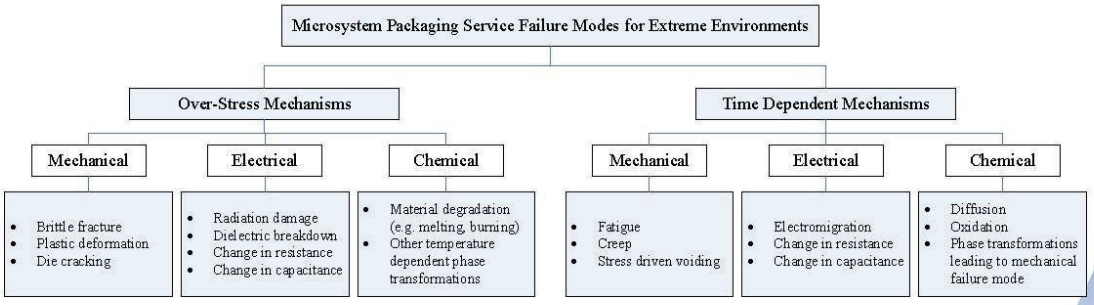
- *Published studies on the thermal cycle reliability of electronic packaging technologies over wide cold temperature ranges only cover a limited number of packaging solutions, such as chip on board technology for power applications or a limited number of plastic package configurations. These will not address all of the configurations required by COTS or custom solutions. This is particularly the case for large cycle count applications.*

- The development of reliable electronic packaging for cold temperatures is challenging due to the high stresses that can result from differences in coefficient of thermal expansion (CTE) between adjacent materials and the wide temperature extremes of the application.
- At the design level, traditional packaging approaches may not be sufficient to meet the thermomechanical fatigue requirements or performance requirements of the application; however non-standard material solutions can be challenging to implement reliably.
- Accurate material properties, such as CTE, strength and modulus, for the relevant electronic packaging elements over the entire temperature range are critical and not readily available.
- Understanding the key failure mechanism for the assembly over the entire temperature range is essential.

Outline

- Background
- Technology Summary
- Gap Analysis
- Qualification Overview
- Questions for Audience

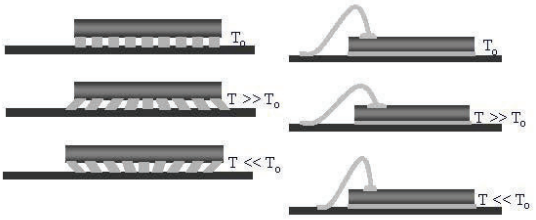
Failure Modes

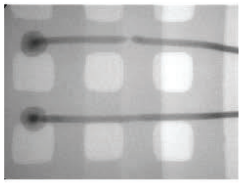


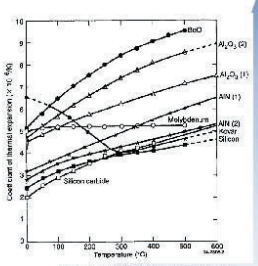
- Wide Low Temperature: fatigue, which is influenced by phase transformations, embrittlement, and especially coefficient of thermal expansion differences, is the primary failure source

Fatigue

- Failure of electronic packages exposed to the low temperature thermal cycles is dominated by fatigue.
- Fatigue is the phenomenon of material failure under cyclic loading conditions.
- For electronic packaging, fatigue generally results from large temperature fluctuations and coefficient of thermal expansion (CTE) differences between adjoining materials.
- Examples of sites at which fatigue becomes a problem are solder joints, die attachment points, and wirebonds.





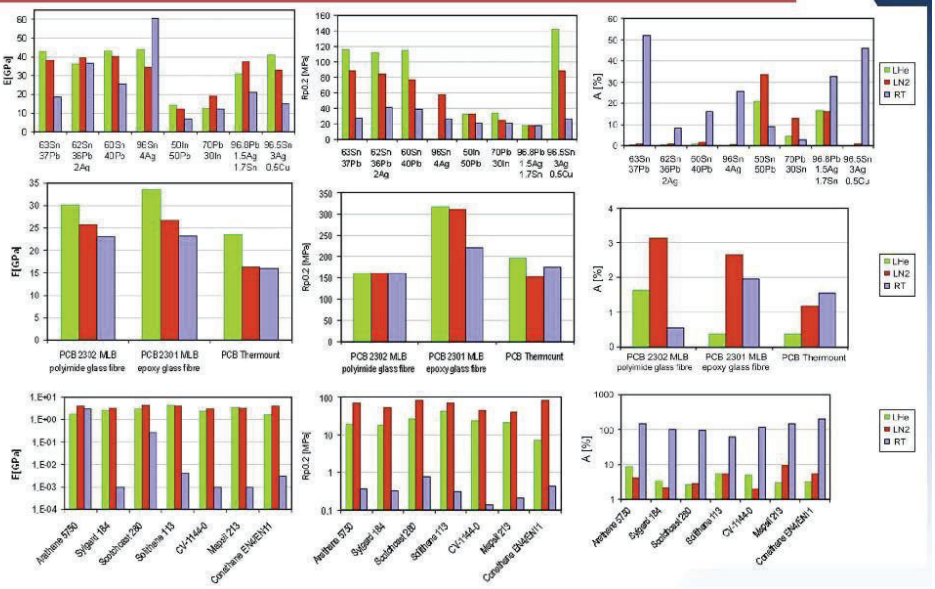


"High Temperature Electronics," F.P. McCluskey, R. Grzybowski, T. Podlesak, eds., CRC Press, Boca Raton, 1997.

5

Influence of Temperature on Packaging

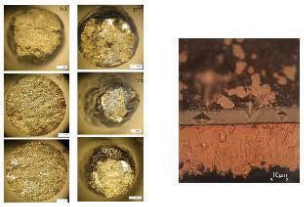
- At cryogenic temperatures, mechanical stresses on the die and the various interconnects are exacerbated by the increased temperature differential with respect to processing temperature as well as the change in material properties at cryogenic temperatures.
- Polymer encapsulants can become rigid, thereby increasing the stress on wirebonds during thermal cycling. This can result in fatigue failures.



Dunn, B.D., *Matl. and Proc. for Spacecraft and High Rel. App.*, 2016.

Influence of Temperature on Packaging

- Attachment points like columns for a ceramic column grid array can fail as a result of stresses resulting from the CTE difference between the package and the PCB. Such failures can be influenced by the selection of package material, board material, underfill, and process parameters.
- The influence of alloy composition and temperature on the tensile strength of PbSn alloys is shown.



Fink, M., Fabling, T., Scheerer, M., Semerad, E., Dunn, B., "Meas. of Mechanical Prop. of Elec. Matl. at Temp. Down to 4.2K," *Cryogenics*, vol. 48, 2008, p. 497-510.

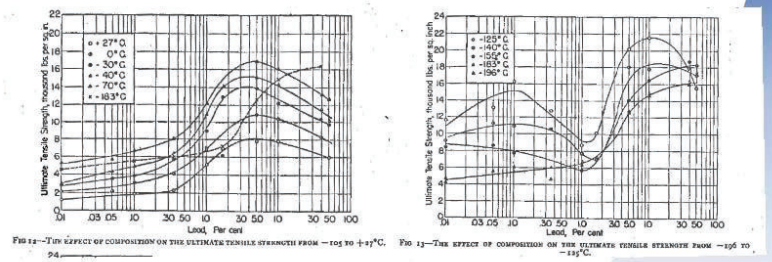
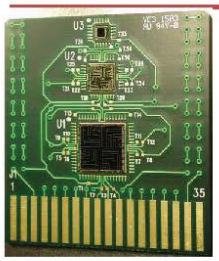
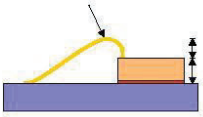


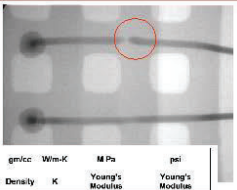
Fig 12—The effect of composition on the ultimate tensile strength from −105 to +27°C. Fig 13—The effect of composition on the ultimate tensile strength from −196 to −125°C.

Kalish, H.S., and Dunkerley, F.J., "The Low Temperature Properties of Tin and Tin-lead Alloys," *American Institute of Mining and Metallurgical Engineers Technical Publication No. 2442*, 1948.

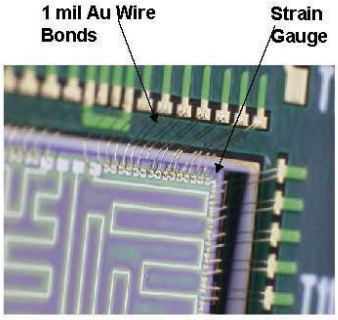
Device Packaging-Mars (Chip on Board)







Material Properties		ppm/°C CTE	gm/cc Density	W/m-K K	M Pa Young's Modulus	psi Young's Modulus
Substrate	Al_2O_3	8.1	3.87	25.12	1.06E+06	1.58E+07
Substrate	LTCC	6.0	3.87 [2]	14.65	1.00E+06	1.45E+07
Substrate	Polyimide	15	1.937	0.445	1.65E+04	2.44E+06
Die Attach	Epoxy	216	4.788	40	2883	4.18E+05
Die Attach	Silicone	340	1.17	1.26	1.1	1.60E+02
Die Attach	Indium 100%	33	7.31	86	1.08E+04	1.64E+06
Die	Si	2.6	2.33	146.5	4.70E+04	6.82E+06



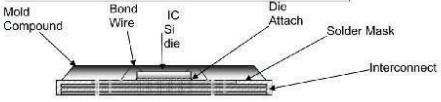


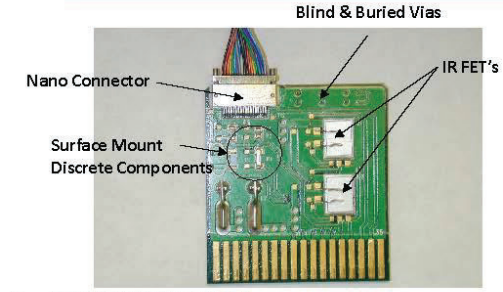
Figure 1. Typical COB package.

A. A. Shapiro, C. Tudryn, D. Schatzel, and S. Tseng, "Electronic Packaging Materials for Extreme, Low Temperature, Fatigue Environments," IEEE Transactions on Advanced Packaging, May 2010, Vol.33, No.2, pp.408-420.

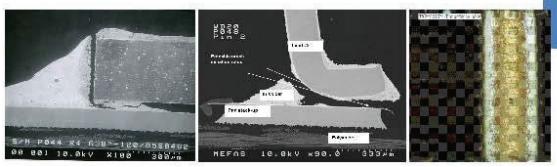
C.D. Tudryn, B. Blalock, G. Burke, Y. Chen; S. Cozy, R. Ghaffarian, D. Hunter, M. Johnson, E. Kolawa, M. Mojarradi, D. Schatzel, and A. Shapiro, A., "Low Temperature Thermal Cycle Survivability and Reliability Study for Brushless Motor Drive Electronics," Proceedings of the 2006 IEEE Aerospace Conference, Big Sky, MT.

Substrate Materials	Die Attach Materials	Coating Materials
Polyimide		
Die attach 1	Epoxy Die Attach	
	Encapsulant 1	Epoxy Encapsulant
	Encapsulant 2	Parylene
	Encapsulant 3	Silicone
Die attach 2	Silicone	
	Encapsulant 1	Epoxy Encapsulant
	Encapsulant 2	Parylene
	Encapsulant 3	Silicone
Die Attach 3	In	
	Encapsulant 1	Epoxy Encapsulant
	Encapsulant 2	Parylene
	Encapsulant 3	Silicone
Al2O3		
Die attach 1	Epoxy Die Attach	
	Encapsulant 1	Epoxy Encapsulant
	Encapsulant 2	Parylene
	Encapsulant 3	Silicone
Die attach 2	Silicone	
	Encapsulant 1	Epoxy Encapsulant
	Encapsulant 2	Parylene
	Encapsulant 3	Silicone
Die attach 3	In	
	Encapsulant 1	Epoxy Encapsulant
	Encapsulant 2	Parylene
	Encapsulant 3	Silicone
LTCC		
Die attach 1	Epoxy Die Attach	
	Encapsulant 1	Epoxy Encapsulant
	Encapsulant 2	Parylene
	Encapsulant 3	Silicone
Die attach 2	Silicone	
	Encapsulant 1	Epoxy Encapsulant
	Encapsulant 2	Parylene
	Encapsulant 3	Silicone
Die attach 3	In	
	Encapsulant 1	Epoxy Encapsulant
	Encapsulant 2	Parylene
	Encapsulant 3	Silicone

Device Packaging-Mars (Power)



- 3 Dominant Failure Modes
  - MOFETs - Heavy Al wire (20 mil) lifting from pad
  - Nano-Connector - Leads lifting off substrate (In solder)
  - Resistor - solder joint cracking (SnPb finish attached with In solder), Au endcaps not failing



Substrate	Die Attach	Al wire (mil)	Resistor Attach	R1 (1206)	R2 (805)	R4 (1506)	Coating
Polyimide	Ag-filled epoxy	20	Ag-filled epoxy	SnPb	SnPb		Silicone 2
	Ag-filled epoxy	20	Ag-filled epoxy	SnPb	SnPb		Parylene C
	In80/Pb15/Ag5	20	In80/Pb15/Ag5	Au[4]	SnPb		Silicone 2
	In80/Pb15/Ag5	20	In80/Pb15/Ag5	SnPb	SnPb	Au	Parylene C
	Silicone 1	5	In80/Pb15/Ag5	Au	SnPb		Silicone 2
	Silicone 1	5	In80/Pb15/Ag5	Au	SnPb		Parylene C
Thick Film Al_2O_3	Ag-filled epoxy	20	Ag-filled epoxy	SnPb	SnPb	Au	Silicone 2
	Ag-filled epoxy	20	Ag-filled epoxy	SnPb	SnPb	Au	Parylene C
	In80/Pb15/Ag5	20	In80/Pb15/Ag5	SnPb	Au		Silicone 2
	In80/Pb15/Ag5	20	In80/Pb15/Ag5	SnPb	Au		Parylene C
	Silicone 1	5	In80/Pb15/Ag5	SnPb[3]	SnPb	Au[3]	Silicone 2
	Silicone 1	5	In80/Pb15/Ag5	Au	SnPb		Parylene C
LTCC	Ag-filled epoxy	20	Ag-filled epoxy	SnPb	SnPb	Au	Silicone 2
	Ag-filled epoxy	20	Ag-filled epoxy	SnPb	SnPb	Au	Parylene C
	In80/Pb15/Ag5	20	In80/Pb15/Ag5	SnPb	Au		Silicone 2
	In80/Pb15/Ag5	20	In80/Pb15/Ag5	SnPb	Au		Parylene C
	Silicone 1	5	In80/Pb15/Ag5	SnPb	SnPb		Silicone 2
	Silicone 1	5	In80/Pb15/Ag5	SnPb	SnPb		Parylene C

- C.D. Tudryn, B. Blalock, G. Burke, Y. Chen; S. Cozy, R. Ghaffarian, D. Hunter, M. Johnson, E. Kolawa, M. Mojarradi, D. Schatzel, and A. Shapiro, A., "Low Temperature Thermal Cycle Survivability and Reliability Study for Brushless Motor Drive Electronics," IEEE Aerospace Conference, 2006, Big Sky, MT.
- Y. Chen, C. T. Weber, M. Mojarradi and E. Kolawa, "Micro- and Nano-electronic Technologies and Their Qualification Methodology for Space Applications under Harsh Environments", Proceedings of the Society of Photo-Optical Instrumentation Engineers (SPIE) 8031, 80311Y, April, 2011; doi:10.1117/12.884680

Device Packaging-Europa

- Seventeen test vehicles were assembled using daisy chain BGA's and attached to a polyimide daisy chain test board with ENEPIG finish were exposed to -184°C to +85°C for 100 thermal cycles.
- A test matrix for the thermal cycle evaluation including daisy chain part information, attach material and underfill type.
- Sn63-Pb37 and In Alloy attached modules successfully passed thermal cycles with <20% change in resistance.

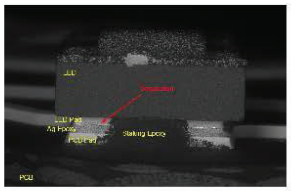
Daisy Chain Test Vehicle

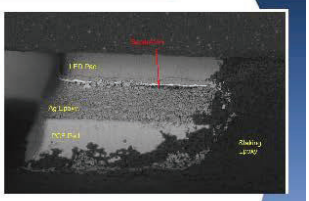
SN	Attach	Under	TC	PBGA676	CABGA196	CVBGA360	CVBGA432	CTBGA228	CTBGA84	#Data Channels
001	Sn63	Mix	N	3	0	0	0	0	3	0
002	Sn63	-	Y	3	2	1	1	1	3	11
003	Sn63	-	Y	3	1	1	1	1	3	10
004	Sn63	P	Y	3	2	1	1	1	3	11
005	Sn63	P	Y	3	1	1	1	1	3	10
006	Sn63	UF1	Y	3	3	2	2	2	4	16
007	Sn63	UF2	Y	3	3	2	2	2	4	16
008	In	Mix	N	3	0	0	0	0	3	0
009	In	-	Y	3	2	2	2	2	3	14
010	In	P	Y	3	2	2	2	2	3	14
011	In	UF1	Y	3	1	1	1	1	4	11
012	In	UF2	Y	3	1	1	1	1	4	11
013	3104	Mix	N	3	0	0	0	0	3	0
014	3104	-	Y	3	2	2	2	2	3	14
015	3104	P	Y	3	2	2	2	2	3	14
016	3104	UF1	Y	3	1	1	1	1	4	11
017	3104	UF2	Y	3	1	1	1	1	4	11
Total:				51	24	20	20	20	57	

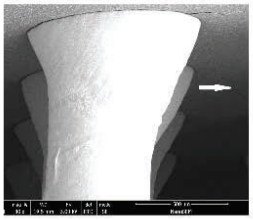
L. Del Castillo, M. Ashtijou, B. Rhym, R. Ghaffarian, J.Y. Yang, D. Hunter, E. Sunada, M, Mojarradi, "Electronic Packaging and Passive Devices for Low Temperature Space Applications," *IEEE Aerospace Conference*, March 3-10, 2018.

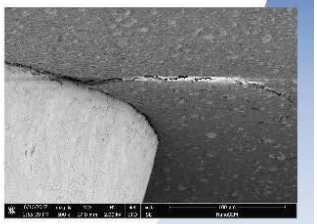
Packages and Interfaces

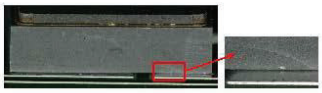
- Ceramic packages can exhibit cracking due to overstress at low temperatures.
- Material combinations for attachment and processes must take into account the specific configuration of the device and assembly.











E. Suh, A. Hanelli, "SMD Package Crack Susceptibility Issue," SAE CE-12 Space Subcommittee Meeting, 5-20-2021

Technology Summary-Environment Categories

Category 1: Wide low temperature cycling

- Permanently Stationed Platforms:
  - Equatorial -180 °C to +125 °C (93 K to 398 K)
  - Mid Latitudes: -145 °C to +80 °C (128 K to 353 K)
- Mobile Platforms:
  - Roving Broadly -145 °C to +120 °C (128 K to 393 K)

Category 2: Extreme low temperature

- Permanently Stationed Platforms:
  - Poles -233 °C to -193 °C (40 K to 80 K)
  - PSR -233 °C (40 K)
- Mobile Platforms:
  - Transport in/out of PSR -233 °C to -40 °C (40 K to 233 K)

Category 1 Technology Summary

- Coefficient of thermal expansion (CTE) matching of components is critical for this temperature regime.
- Pure In may be problematic due to the upper limit of this temperature range, potentially resulting in creep within joints as well as the growth of intermetallic compounds.
- Standard printed circuit boards were used for several studies but required structures to accommodate stresses resulting from CTE differentials. Leaded components have demonstrated survival using traditional PbSn solders; however, there may be issues with leadless devices or column grid arrays. Fatigue of PbSn solder joints may become an issue for large thermal cycle applications.
- InPb solder joints may be a good alternative solder technology, but care must be taken to properly implement this material since process requirements are different from traditional solders.
- Various material options have been demonstrated for attachment of die at this temperature range. Care must be taken to ensure the proper thickness, pattern, and cure conditions, especially for polymers.
- Polymer encapsulants for wire bonds and underfills for flip chip arrays may cause premature failure. Certain filled molding compounds may work but require further investigation to determine if the fillers initiate fatigue cracks within the polymer or interface cracks with the lead frame, leading to device failure.
- Most studies are limited to a few hundred cycles. Applications that require greater than 500 cycles require more testing to verify suitability of the packaging technologies.

13

Category 2 Technology Summary

- This application condition is similar to the cryogenic detector applications.
- CTE differences and processing temperature will have a significant impact on reliability and performance.
- Pure In is attractive since it retains ductility at cryogenic temperatures and has a low processing temperature.
- InPb alloys should be considered for the attachment of components.
- Sn63Pb37 solder may be a viable alternative for systems that can accommodate higher processing temperatures.
- Multiple substrate layers may be required to accommodate the CTE differences between the device and the printed circuit board if this option is selected.
- High density flip chip attachment between Si die and Si interposers using In bump bonds have a rich history at this temperature.
- Au wire bonding and thin Al wire bonding have been implemented between interposers and the next layer of interconnects. The use of high-density packages, however, may be problematic.
- Testing of different high density packaging technologies is warranted. Even though cycling may not be required for the application, it will be required for ground testing.

14

Qualification of Electronic Packaging

- At the system level, assembly reliability under thermal stress depends on the reliability of its constituent elements— package, PCB (printed circuit board), and interconnects — and its global/local interfaces (attachments).
- Reliability then is defined by the characteristics of these three elements — package (e.g., die, substrate, solder joint, and underfill), PCB (e.g., polymer, copper (Cu), plated through hole, microvia), solder joints (e.g., via balls, columns) — together with the use conditions, the design life, and the acceptance failure probability.
- For lunar, extreme low cryogenic temperature environment, thermomechanical modeling for life cycle projection become inaccurate because of changes in material properties with temperature, continuous electronics shrinkage with use of higher density interconnections (HDIs) and new configurations as well use of new materials.
- Modeling could be used for parametric study to determine the relative effects for developing an effective design of experiment (DOE).
- Experimentally, one must first establish temperature limits with subsequent thermomechanical fatigue life adequacy for a mission.
- From initial evaluation and modeling, a knowledge of potential failure mechanisms could be determined and fed into the original design of the assembly and materials selection to avoid known potential premature failures during costly life cycle qualification testing.

Qualification of Cold Electronic Packaging (Assembly level)

- The qualification process for cold electronics packaging may include the following steps.
  - Step 1: Determine MEAL (Mission, Environment, Application and Lifetime). For the purposes of electronics packaging, thermal life cycle refers to the temperature range and number of cycles within the MEAL requirements. The total number of cycles include assembly and rework operations (after initial reflow or curing), ground testing, and mission thermal fluctuations (environmental and power cycling).
  - Step 2: Prior to testing, the following should be completed.
    - Prepare a test plan that includes a number of test coupons that use flight configurations and build processes.
    - Identify an approved test facility and conduct appropriate surveys for the facility and test setup.
    - Prepare and document a test procedure that includes test parameters and failures/anomalies definitions as well as frequency of data recording during test.
    - Test hardware should be mounted in the same manner as used for flight.
    - Perform a test dry run to optimize the test parameters to meet the established requirements. Confirm fail-safe settings for the chamber temperature limits to protect the hardware in the event of a malfunction.
    - Perform and record pre-test functional tests of the hardware.

Qualification of Cold Electronic Packaging (Assembly level)

- The qualification process for cold electronics packaging may include the following steps.
  - Step 3: Thermal cycling should be performed according to the test procedures. The hardware should be exposed with agreed margin (1.5-3 times) to the number of equivalent thermal cycles to which the hardware is exposed from the time of post-fabrication to the end of mission life.
    - To mimic flight like thermal fluctuation, a maximum ramp rate of 5 C/minute is appropriate for most electronics assemblies.
    - The test article should be brought to equilibrium with an additional dwell time to cover sufficient thermal degradation before ramping to the next temperature.
    - For power cycling, generally, power should be applied during hot dwell time.
    - Temperature should be monitored at sensitive locations and logged.
    - Hardware should be inspected before testing, several times during testing and after testing.
    - Test hardware should be representative of flight hardware, including design, attachment, materials, device types, coating, heat sinks and processes. It should include all potential failure sites and the capability to monitor the performance at such locations. Hardware can be a full flight like assembly or representative test coupons.
    - Test hardware physical and mechanical inspection methods should be identified in the test plan.
    - One control sample should be reserved for destructive physical analysis, if possible.
  - Step 4: A test report documenting results of the assembly level thermal cycling, failure analyses, deviations, inspection reports, images, and lessons learned should be reviewed and approved by the project and reliability team.

Gap Analysis

- Work has been done for several flight missions to cold environments that has not been published. Understanding design configurations that worked reliably as well as root cause for designs with known failures is required to inform the development of cold electronic packaging guidelines.
- Processing guidelines for the use of low temperature attachment materials is needed to avoid workmanship issues resulting from incompatibility of materials or current assembly processes.
- Work is required to define packaging material properties for the entire temperature regime to allow the development of proper models for stress analysis and to define accelerated test parameters.
- Work to date has been limited to a few hundred cycles at most. Applications that require thousands of cycles or greater than 500 cycles require more testing to verify suitability of packaging technologies.
- Testing of electronic packaging assemblies exposed to large cycle count low temperature thermal cycles is needed to determine which materials, packages and designs provide the most reliable cold temperature packaging solutions. Such testing will yield a database of proven packaging configurations as well as applicable models that consider the mechanics of failure.

Questions for the Group

1. Do you have any low temperature electronic packaging concerns that were not covered?
2. Any other aspects of packaging evaluation (or even, selection?) that are important when preparing for a Lunar mission?
3. Where are the gaps in these processes as they relate to PQV for lunar environments?

NESC Technical Assessment Meeting on Cold Electronics for Lunar Missions
TI-22-01873

7.9 NESC Guidance on Qualification for Cold Electronics and Packaging

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Bottom Line Up Front

- Provided NESC guidance for qualification of cold electronics and packaging
  - Custom cold electronics
  - COTS/MIL cold electronics
  - Packaging – presented during previous section by Linda Del Castillo
- NESC guidance
  - Not NASA standard.
  - NESC team plans to make a recommendation for a NASA standard
- Please ask questions and provide your feedback.

Outline

- Gap analyses
- NESC guidance on cold electronics qualification
  - Custom cold electronics
  - COTS/MIL cold electronics
  - Packaging – (presented during previous section by Linda Del Castillo)

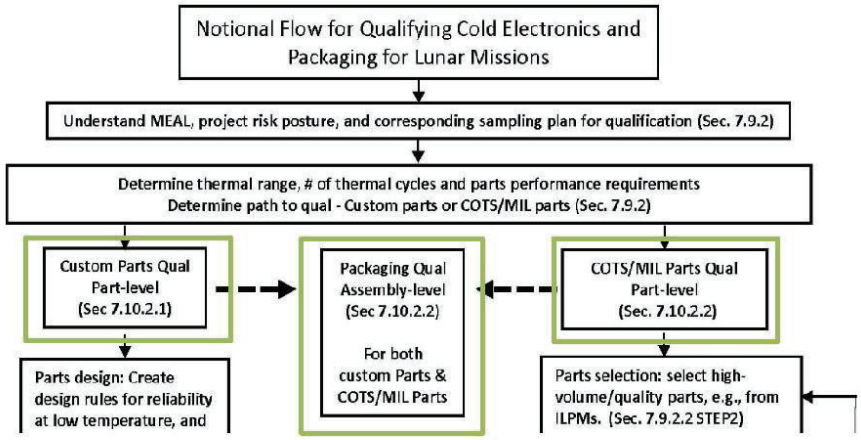
Definition

- **COTS/MIL** - Any commercial, automotive, space, or military off-the-shelf components which are not designed specifically for cold operation below -55 °C.

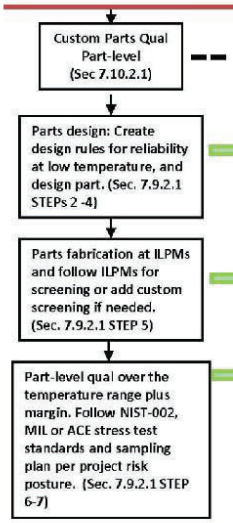
Gap Analyses

- No existing standards support the qualification of the electronics and packaging for the lunar environment temperature range of -230 °C to +120 °C.
  - Military standards: -55 °C to +125 °C, AEC standards: -40 °C to +150 °C, JEDEC standards: -40 °C to +85 °C.
  - Lunar surface temperature ranges are beyond the specifications of the existing qualification standards and even beyond the specifications for process and technology qualifications.
- Qualification - at part and/or assembly levels and has two approaches: stress-test-driven and knowledge-based driven
  - Stress-test driven: a standardized set of stress tests.
  - Knowledge-based: additional sources of information, application specific knowledge and use condition information.
- Studies on both custom electronics and COTS/MIL electronics beyond -55 °C to +125 °C.
  - COTS/MIL electronics treated as black boxes. Test results were likely lot or manufacturer specific.
  - Custom electronic parts, packaging and assemblies typically went through more comprehensive evaluation and qualification processes, with concomitantly higher costs.

NESC Guidance on Col Electronics Qualification – Overview



NESC Guidance on Custom Cold Electronics Qualification – Process Flow



- **Step 1:** Understand MEAL, risk posture and associated reliability test sampling plan. Determine thermal range and number of thermal cycles the electronics will be exposed to. Define performance requirements.
- Parts design: Create design rules for reliability at low temperature, and design part. (Sec. 7.9.2.1 **STEPs 2 -4**)
- Parts fabrication at ILPMs and follow ILPMs for screening or add custom screening if needed. (Sec. 7.9.2.1 **STEP 5**)
- Part-level qual over the temperature range plus margin. Follow EEE-INST-002, MIL or AEC stress test standards and sampling plan per project risk posture. (Sec. 7.9.2.1 **STEPs 6-7**)
- **Step 8:** Perform a risk assessment to manage and mitigate the risk, and to determine if the risk level is acceptable.

NESC Guidance on Custom Cold Electronics Qualification – Part Design

- Step 2: Identify potential failure mechanisms and modes for the chip and the package.
  - Select specific test structures and perform reliability testing at various temperatures and electrical bias conditions. For the package, thermal cycling and shock testing may be needed.
  - The predetermined reliability testing sampling plan in Step 1 should be followed.
  - Testing temperature range should cover the operating temperature range plus margins.
  - Acceleration factor and activation energy are to be extracted from the test data for the dominant failure mechanisms and modes over the entire temperature range.
  - Note: understanding dominant failure mechanism(s) at low temperature is the key in this Step. For example, hot carrier injection degradation in MOSFETs is significantly enhanced at low temperature due to increased carrier mobility and energy, leading to more interface trap formation and reduced transistor lifetime.
- Step 3: Develop and update design rules to address the specific failure mechanisms and modes over the use condition range. Identify any additional testing necessary. For example, design rules may require transistors with larger channel length to mitigate hot carrier injection degradation at low temperature.
- Step 4: Design or revise the electronic circuitry using the updated design rules.

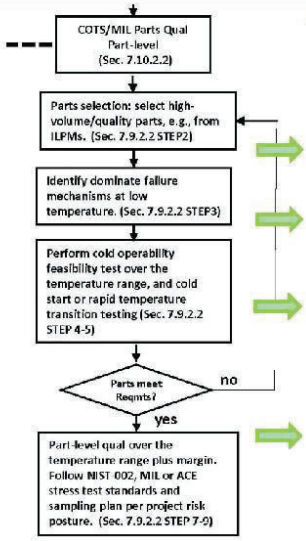
NESC Guidance on Custom Cold Electronics Qualification – Part Fabrication

- Step 5: Manufacture the custom parts at a high-volume manufacturer site, preferably an Industry Leading Parts Manufacturer (ILPM).
  - Follow ILPM screening process.
  - May need to perform additional screening if ILPMs are not selected, such as burn-in or utilization of a known good die (KGD) approach.

NESC Guidance on Custom Cold Electronics Qualification – Part Qual

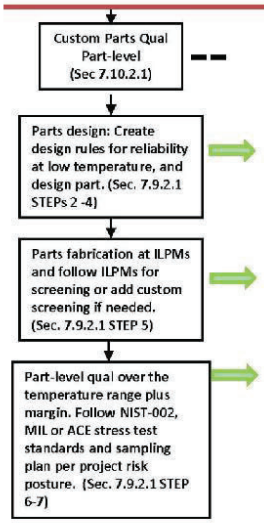
- Step 6: Define stress tests at part-level, including bias conditions and durations, thermal cycling and shock. Stress tests should be based on expected failure mechanisms, acceleration models and use conditions.
  - The predetermined reliability testing sampling plan in Step 1 should be followed.
  - The general approach is to evaluate, test and qualify through functional testing and long-term stress testing of the part, including packaging components or assemblies, over the application operating conditions plus thermal margin.
  - Stress tests should follow a flow similar to those from Mil-STD, JEDEC and/or AEC, with the temperature ranges determined by application operating condition plus a margin dependent on MEAL and project risk posture.
  - Stress tests should include additional testing identified in Step 2.
- Step 7: Establish baseline performance from the qualification tests and analyze the test results to determine if the technology, part, or assembly meet the application requirements.

NESC Guidance on COTS/MIL Cold Electronics Qualification



- **Step 1:** Understand MEAL, risk posture and associated reliability test sampling plan. Determine thermal range and number of thermal cycles the electronics will be exposed to. Define performance requirements.
- Parts selection: Review the manufacturing process and design of the (Sec. 7.9.2.2 **STEP 2**)
- Identify dominate failure mechanisms at low temps. (Sec. 7.9.2.2 **STEP 3**)
- Perform cold operability feasibility tests (Sec. 7.9.2.2 **STEP 4-5**)
- Part-level qual over the temperature range plus margin. Follow EEE-INST-002, MIL or AEC stress test standards and sampling plan per project risk posture. (Sec. 7.9.2.2 **STEPs 7-9**)

NESC Guidance on Custom Cold Electronics Qualification – Process Flow



- **Step 1:** Understand MEAL, risk posture and associated reliability test sampling plan. Determine thermal range and number of thermal cycles the electronics will be exposed to. Define performance requirements.
- Parts design: Create design rules for reliability at low temperature, and design part. (Sec. 7.9.2.1 **STEPs 2 -4**)
- Parts fabrication at ILPMs and follow ILPMs for screening or add custom screening if needed. (Sec. 7.9.2.1 **STEP 5**)
- Part-level qual over the temperature range plus margin. Follow EEE-INST-002, MIL or AEC stress test standards and sampling plan per project risk posture. (Sec. 7.9.2.1 **STEPs 6-7**)
- **Step 8:** Perform a risk assessment to manage and mitigate the risk, and to determine if the risk level is acceptable.

NESC Guidance on COTS/MIL Cold Electronics Qualification

Step 2: Part selection- verifying part quality

- Review the manufacturing process and design of the part, focusing on the quality/process control and reliability qualification through the design and manufacturing for the part
- Use Industry Leading Parts Manufacturer (ILPM) review process or the MIL Spec process as reference
- Check that the part packaging does not have known cold temperature or temp cycling limitations

Step 3: Identify potential failure mechanism, modes and associated acceleration factors

- The component's original design and manufacturer would be the best source for info followed by literature
- Components utilizing known cold-sensitive technologies (such as Silicon BJTs) may be deprioritized
- This information is also needed to design qualification test
- Cold accelerated failure mechanisms such as hot carriers can cause reduced lifetime in cold and would need to be tested specifically for parts that are susceptible.

NESC Guidance on COTS/MIL Cold Electronics Qualification

Step 4: Perform cold operation feasibility testing

- Feasibility test parameters are informed by MEAL from step 1
- Key parameters to test are ramp rate, dwell time and critical operating parameters.
- Test should extend beyond the desired operating cold temperature to provide margin
- An example feasilibity test might include
  - 24 hrs of control data for critical parameters at room temperature
  - ramp down of temperature at a rate representative of MEAL to an equilibrium test temperature which includes margin
  - Monitor critical parameters while operating component at the test temperature for 24 hrs
  - Ramp up to room temperature
  - Monitor critical parameters to look out of family behavior which may indicate damage from the cold operation

Step 5: Perform additional capability tests as indicated by MEAL from step 1

- Cold start capability can be demonstrated by multiple complete shut down and power up at test temperature followed by measurement of key parameters at cold and room temperatures
- Rapid temperature transition capability can be tested by thermos shock test.
- Package stability can be tested by thermos shock and thermal cycling test as indicated by MIL Spec

NESC Guidance on COTS/MIL Cold Electronics Qualification

Step 6: Evaluate feasibility test results for selection as design candidate

- Perform a risk assessment to manage and mitigate the risk, and to determine if the risk level is acceptable against the defined requirements.
- For example, is there some critical parameter shift at cold? If so, is it stable, consistent across samples and acceptable for intended application?

Step 7: If the component is selected for use, lot specific qualification is recommended to support this out-of- specification use of the component

NESC Guidance on COTS/MIL Cold Electronics Qualification

Step 8: Define stress-based qualification tests

- Qualification tests can be destructive or test to fail and designed to determine if the part meets or exceeds the application requirements.
- Key factors to consider include bias conditions and durations, expected failure mechanisms, acceleration models and use conditions.
- The predetermined reliability test sampling plan in Step 1 should be followed.
- Stress tests should follow those from NASA-INST-002 (extending to cold temperatures) supplemented by Mil-STD, JEDEC, AEC, and peer reviewed literature depending on MEAL and project risk posture.
- Stress tests should include the additional testing identified in Step 1.
- Acceleration factor and activation energy are to be extracted or confirmed by collecting sample test data for the dominant failure mechanisms and modes over the entire temperature range, including margin.
- Package-focused stress testing such as thermal cycling and thermal shock should be included.

Step 9: Define screening tests

- Screening test for all parts should include tri-temp testing to the target temperature.
- Hot and cold burn-in should both be conducted, especially for known cold accelerated mechanisms.

Questions

- What qualification approach, standard, or test have you been using for cold electronics?

Electronics at Assembly Qualification Methods & Extreme Cold

by

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Jet Propulsion Laboratory
National Aeronautics & Space Administration
California Institute of Technology

Lunar Cold Electronics Technical Assessment Meeting
(Apr 30 – May 1, 2025)

Jet Propulsion Laboratory
California Institute of Technology

Outline

- **Packaging Technologies Trends**
  - BGAs/DSBGA and CGAs
  - Small Leaded Part (TSSOP)
- **MEAL and Reliability**
  - Standard Life Thermal Cycle TCL/PQV)
  - Physics of Failure (PoF)
  - Examples of failures under extreme cold
- **New Qualification Method (νHALT)**
  - Cold Step, Hot Step, TC
  - Ruggedization
    - Key for Lunar cold application
- **NASA HALT Guideline posted on the NEPP website**
- **Questions?**

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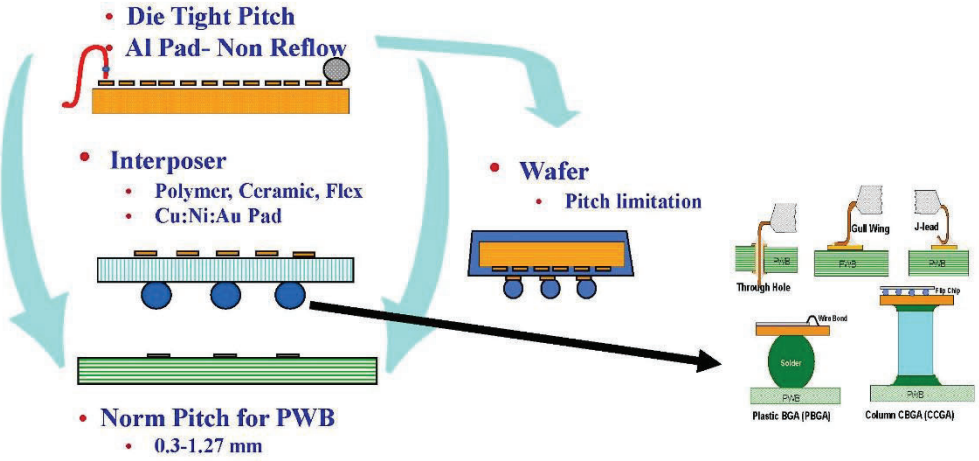
Packaging Concepts
(Shrink it, Bump it (BGA/CGA))



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Ball Grid Array (BGA) Guidelines
(Further Shrink it, DSBGA)

National Aeronautics and Space Administration

NASA Guidelines for Ball Grid Array (BGA) and Die-Size BGA (DSBGA) Selection and Application

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Pasadena, California

https://nepp.nasa.gov/docs/tasks/076-Packaging-Assurance/Guidelines-BGA-DSBGA-Ghaffarian-2022July20-CL22-3574.pdf

Single-Electronics Packaging Technologies

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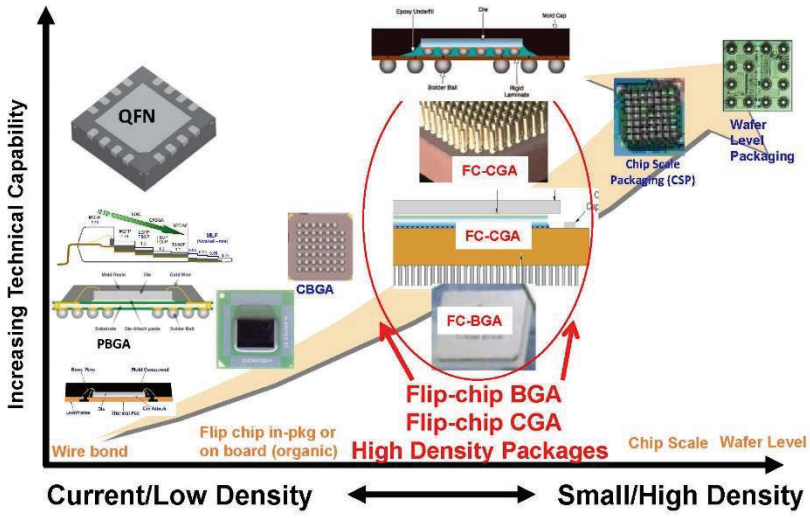

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>LCCC-20 Fails Early at Assembly QFN for RF/High Power

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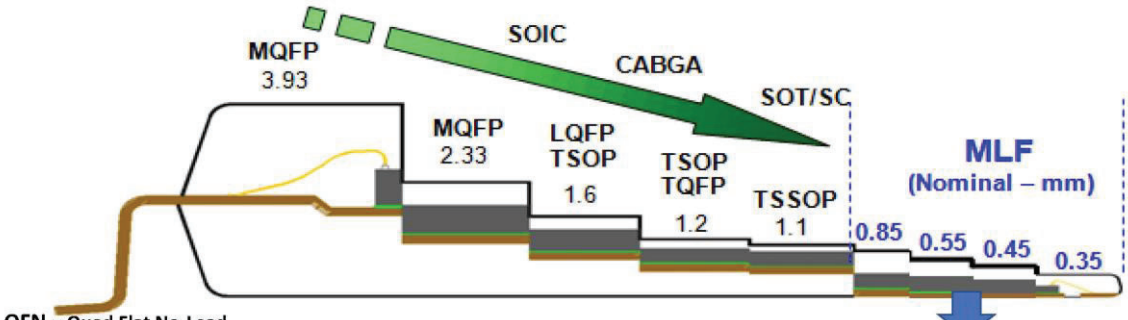
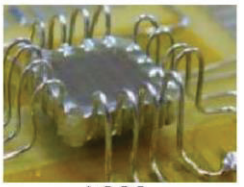
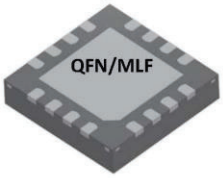


QFN = Quad Flat No-Lead
MLF = Micro Lead Frame
BTC = Bottom Termination Component
TSSOP: Thin Shrink Small Outline Package
LCCC = Leadless Ceramic Chip Carrier
LQFP = Low Profile Quad Flat Package
MQFP= Metric QFP
CABGA= Chip Array Ball Grid Array (BGA)



LCCC



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6

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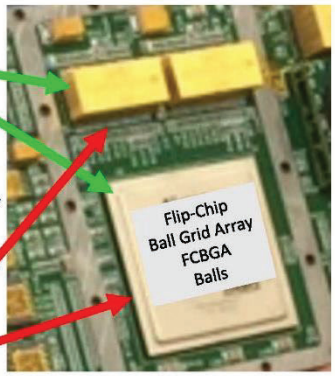
Reliability under Thermal Cycle

Electronics Packaging Assembly

Know Your Part/Package

Know Your PCB/Finish

Know Your Interconnect



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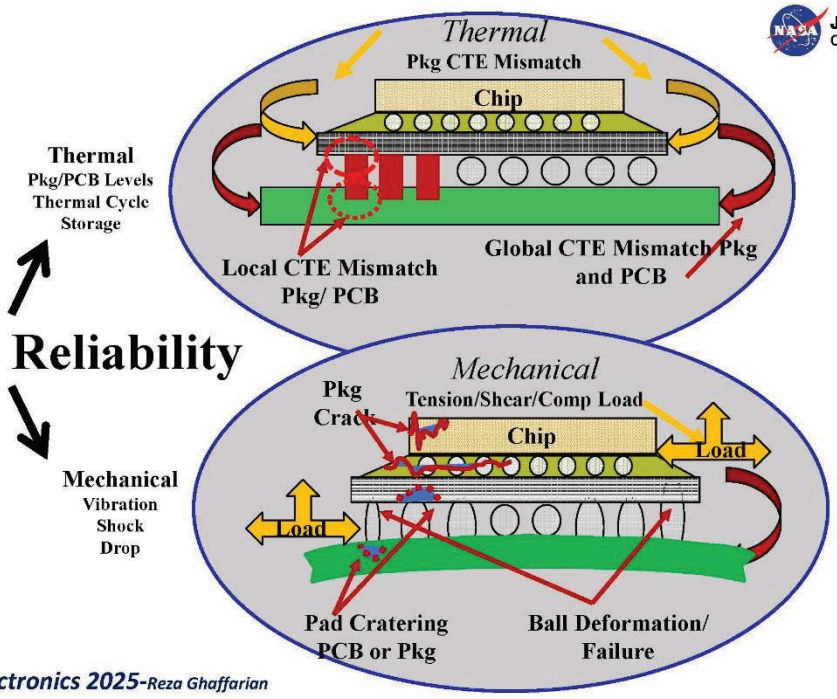

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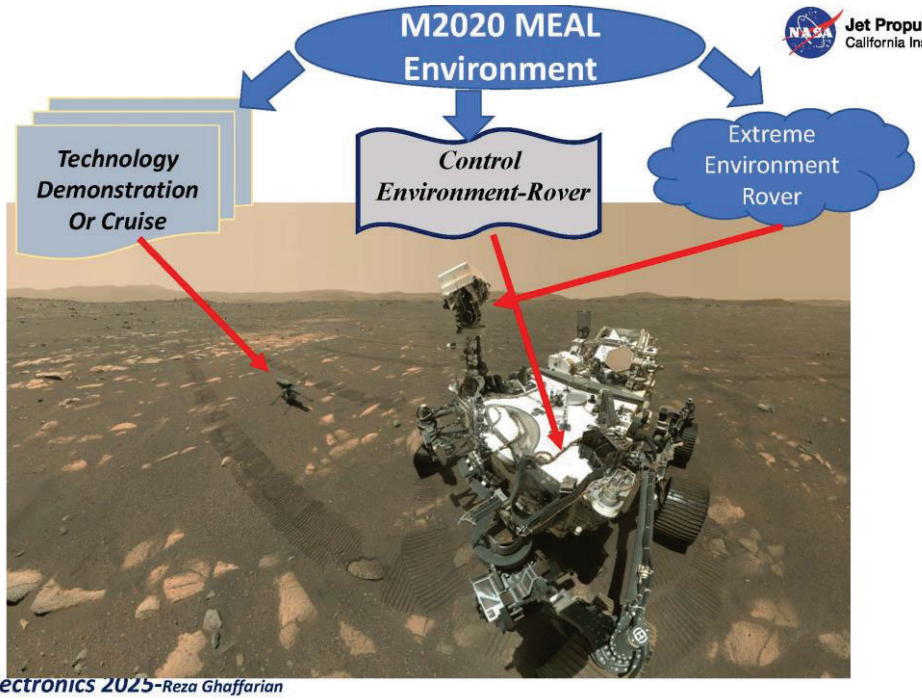

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M2020 Camera
Cryogenic TC/Long Exposures

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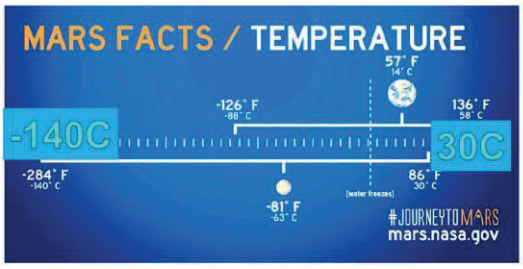

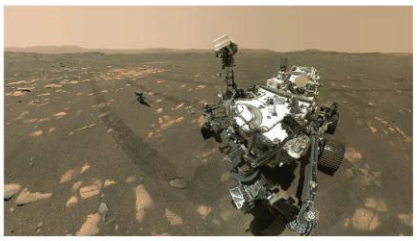

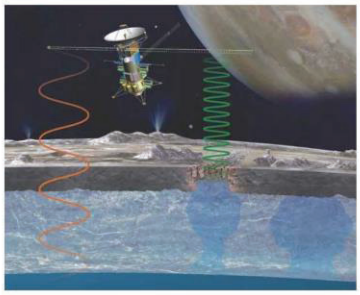

Jupiter-Europa
~ -240°C

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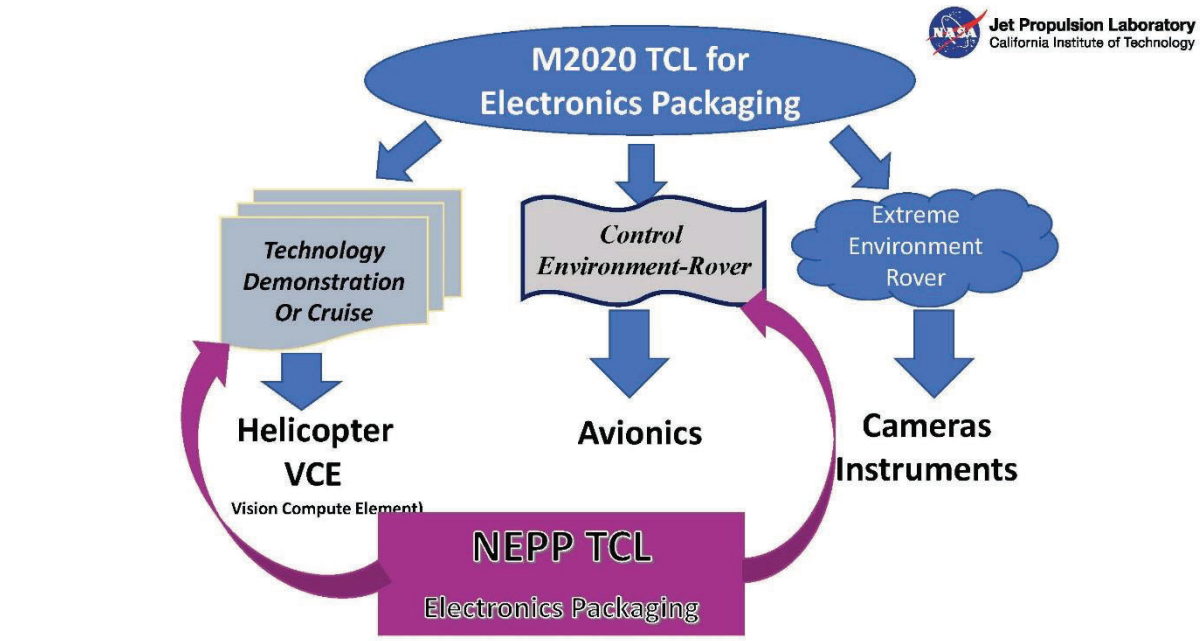

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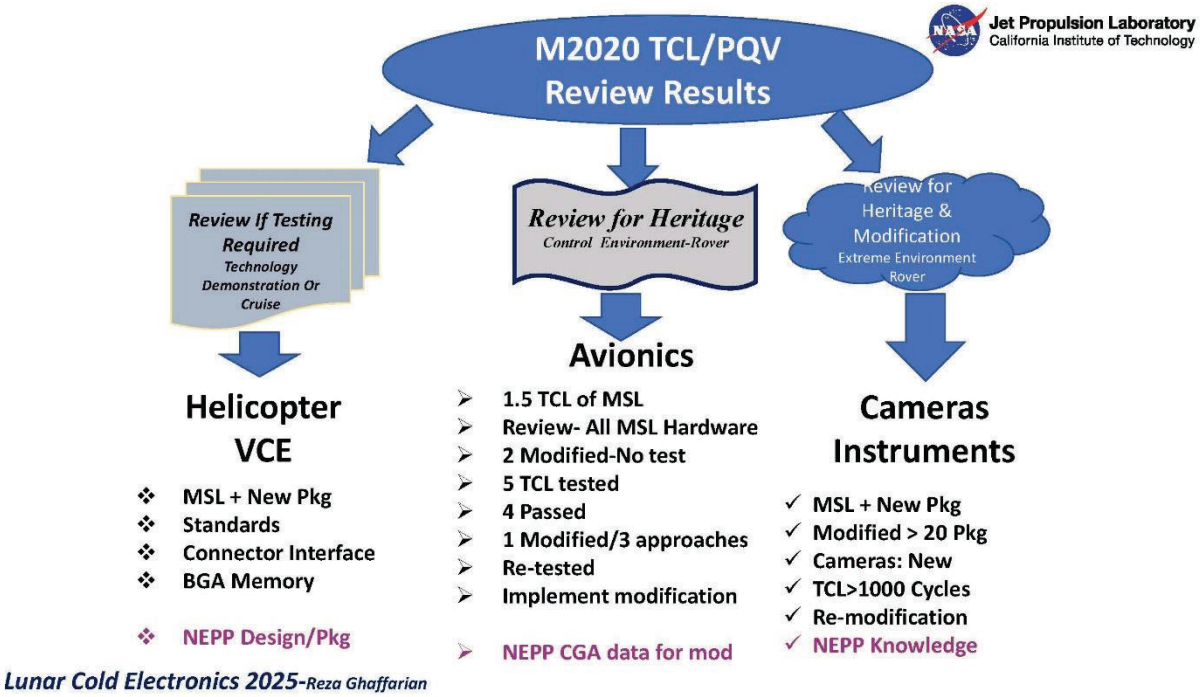

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Reliability: TC Global/Local

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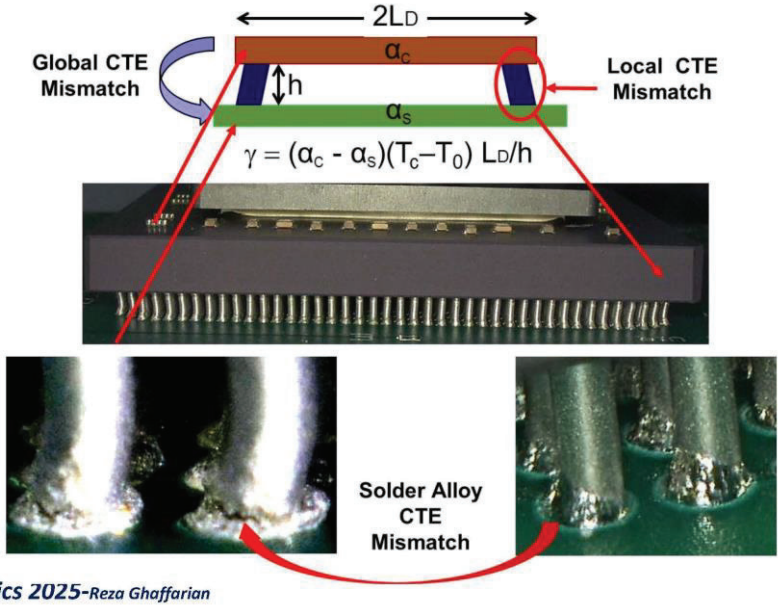

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Solder Fatigue Models for TC Accel

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$$N_f(50\%) = \frac{1}{2}\left[\frac{2\varepsilon'_f}{\Delta D}\right]^m$$

$$\Delta D = (\alpha_c - \alpha_s)(T_c - T_0)\, L_D/H$$

Appears to be simple!
W/O
Physics of Failure (PoF)
Model: Semi-analytical, Semi-empirical

New Approach $N_f \sim W^c$

Engelmaier-Wild Model

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Solder Fatigue-Energy Method
Stress-Strain Hysteresis

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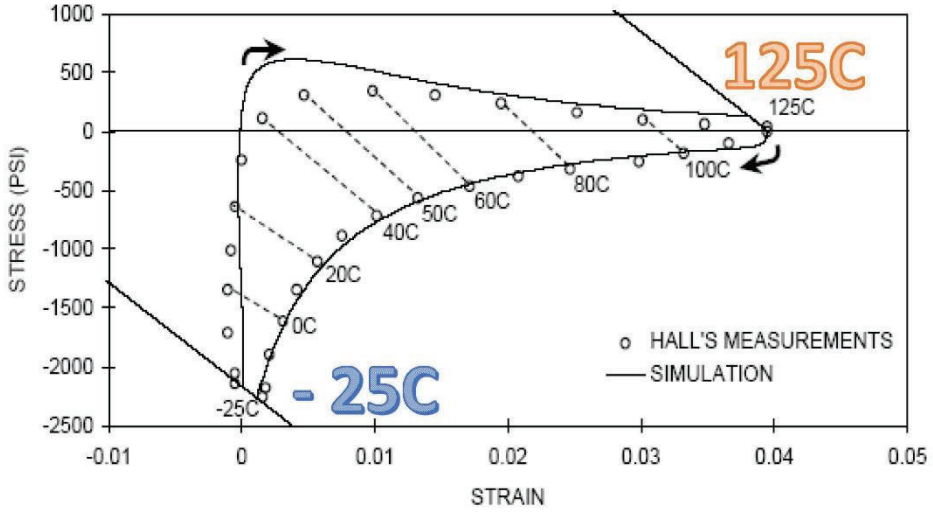

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Accel TC for Solder

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$$\Delta D = \Delta\alpha \; \mathbf{\Delta T} \; LD/H$$

ΔT = 0 to 100C	***Creep (time dependent)***
ΔT = -55C to 100C	Creep + Fatigue
ΔT = -55C to 125C	Excess creep + Fatigue
ΔT = -65C to 150C	Excess creep + Fatigue
ΔT = -120C to 85C	Mild creep + Excess Fatigue
ΔT = -196C to 25C	***Low creep + Excess Fatigue***

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SnPb Properties with Temp Affects PoF

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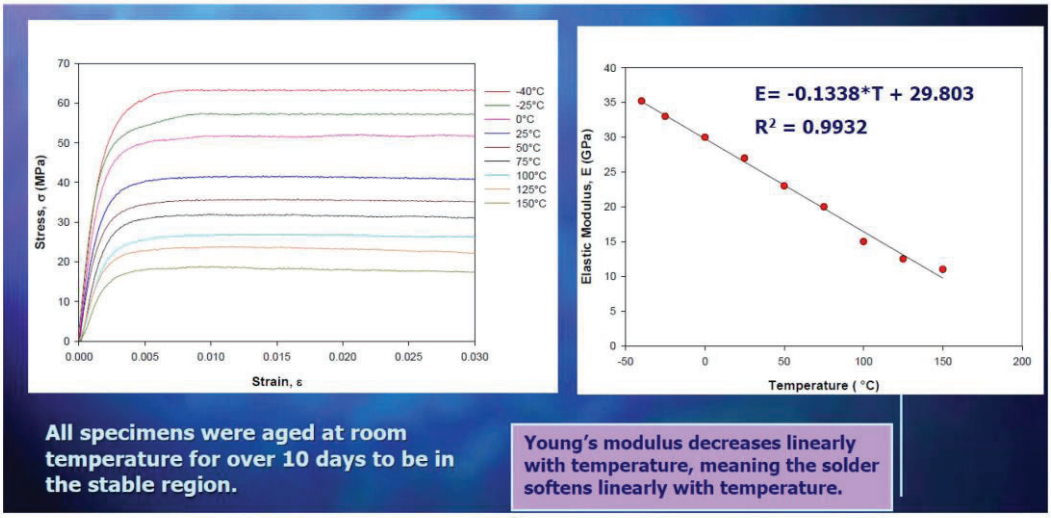

Reference: CAVe3-2005

CGA 1144 TC Reliability

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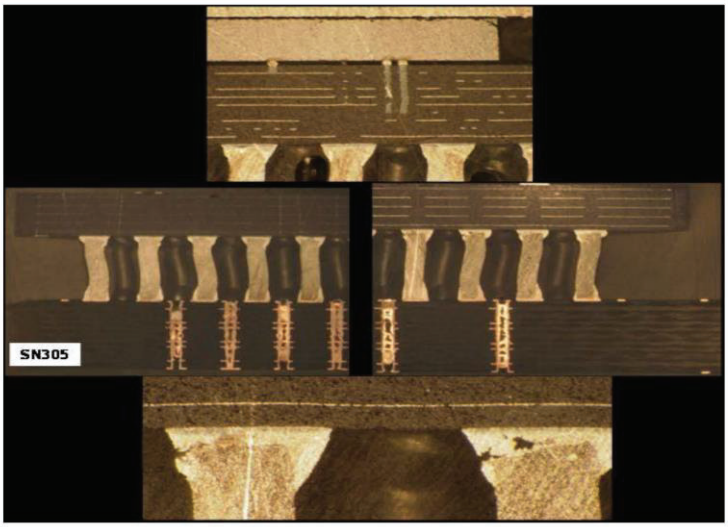
X-sections: –55C/125C



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CGA 1144 TC Reliability Harsh TC

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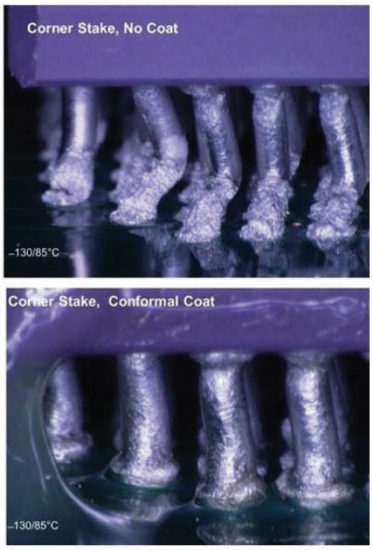
–130C/85C, W/O & W Coat/Stake



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LCCC Solder Joint Failure: Harsh TC

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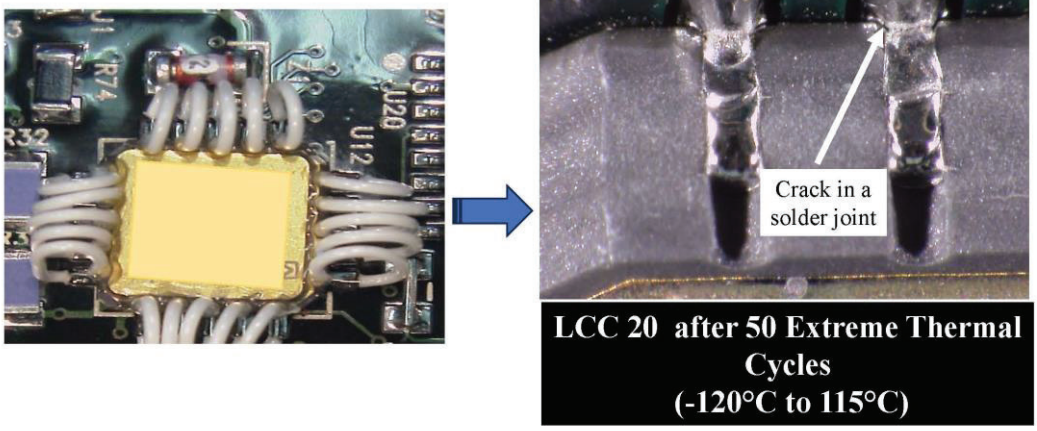
Mitigation: Bond & Use Jumper Wires



LCC 20 after 50 Extreme Thermal Cycles (-120°C to 115°C)

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PGA Assembly Reliability

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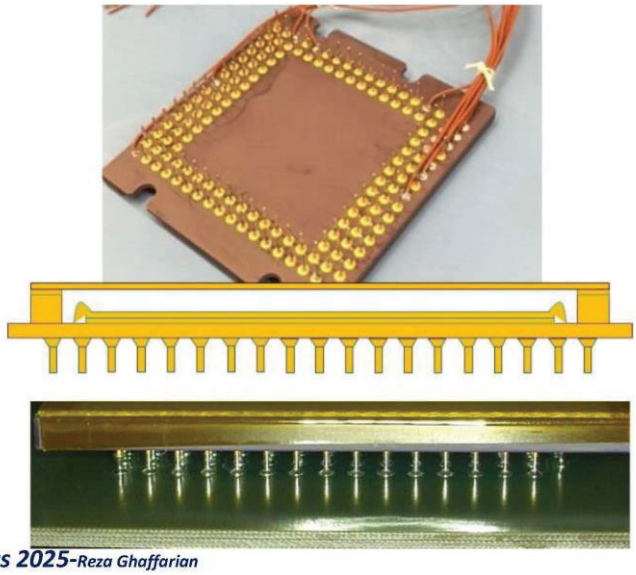

Harsh Thermal Cycles (TC-H) Change in PoF

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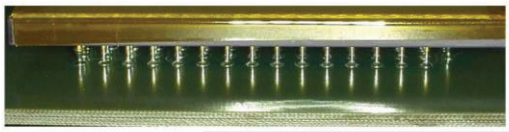
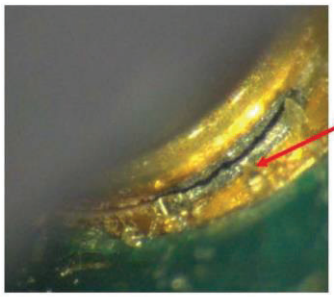
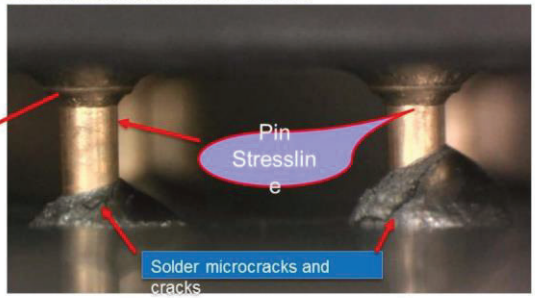
- –135C/70C, ΔT=205
- PGA Pin Height = 50 mils







Material CTE Measurements

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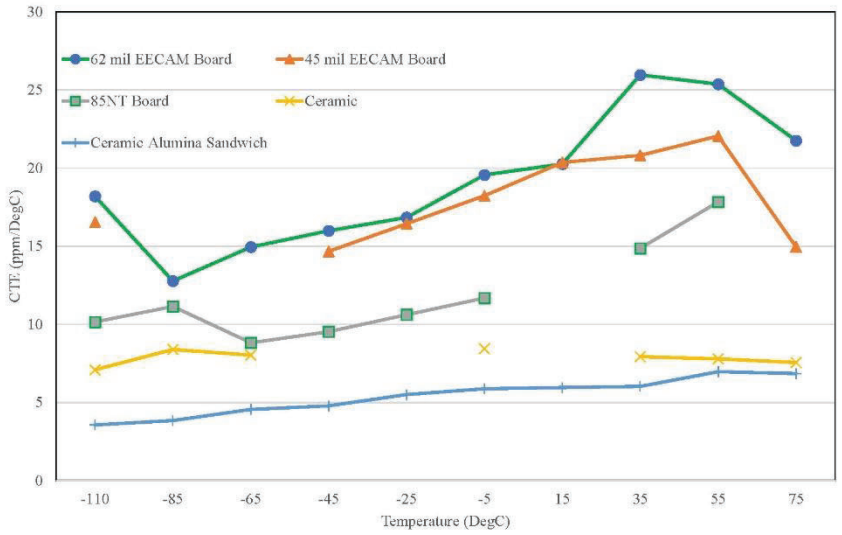

Modeling Predictions

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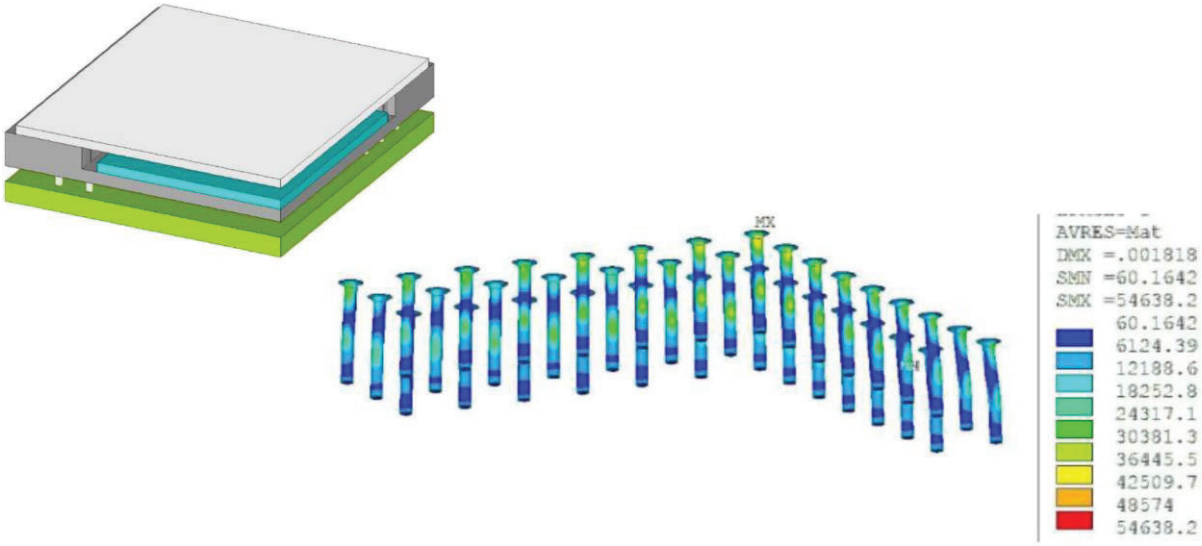

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Microcracks Initiate at Corners Ideal PoF

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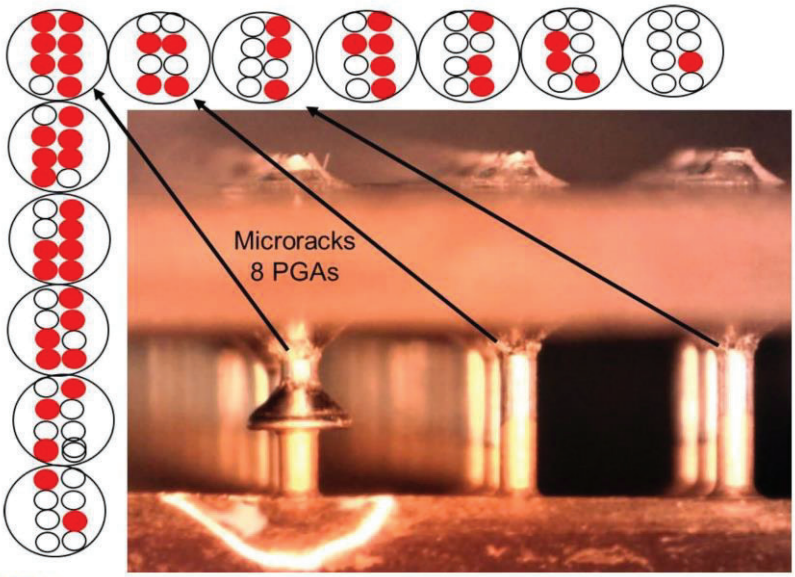

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Initial Crack at Corners

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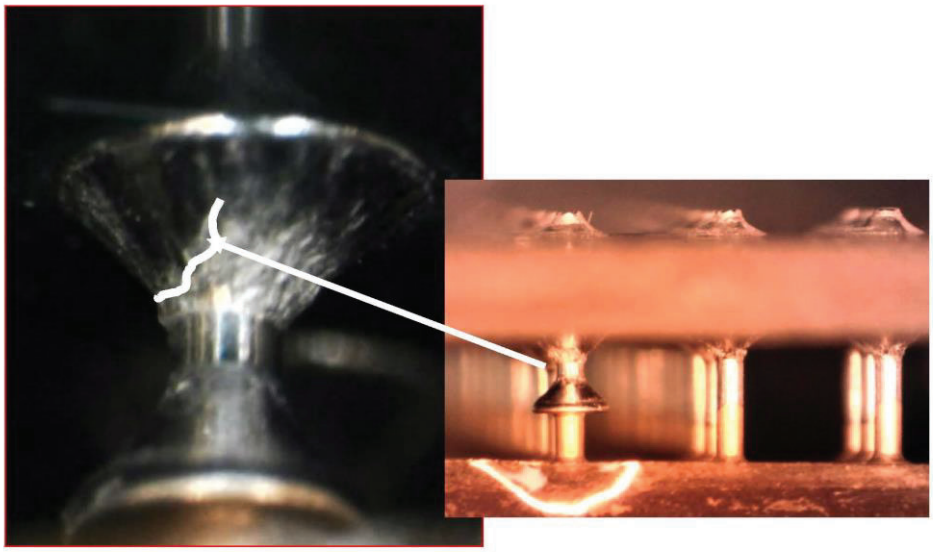

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Sample Return Tube

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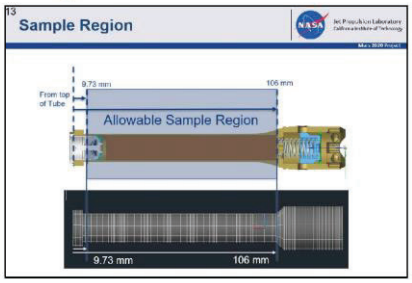

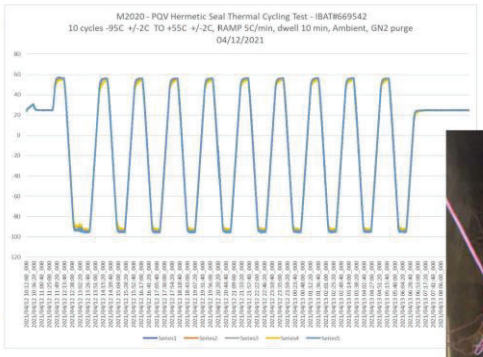

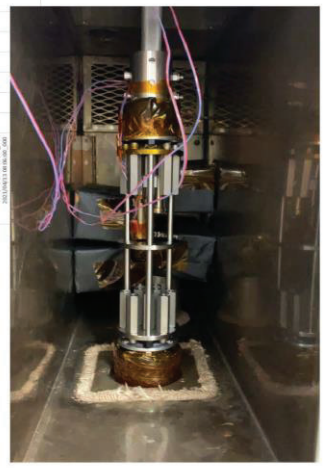

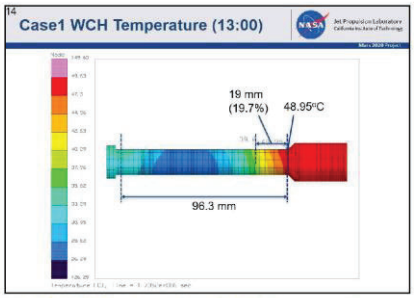

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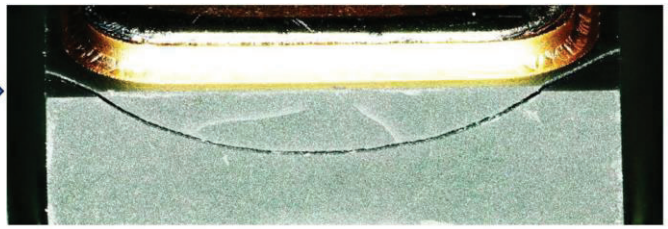
SMD Metal-Lid Failed - Mild ΔT

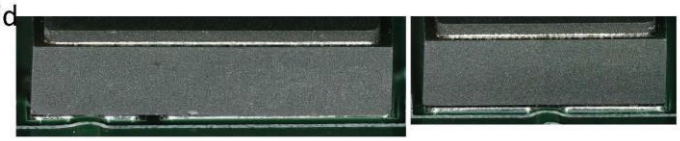
Ceramic-Lid Ok

Metal-Lid SMD Passed (-55/125C), but Failed Milder ΔT

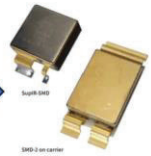
Mitigations: Limited

- Use Ceramic-Lid SMD
- Do NOT use Metal-Lid SMD
- Increase PCB thickness for Ceramic-Lid
- Increase solder thickness
- Use Ribbon Version





Use Ribbon Versions



Supplier to evaluate as the effect of loss of hermeticity for SMDs per added Mil requirement?

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SMD: Types with Metal- Ceramic-Lid

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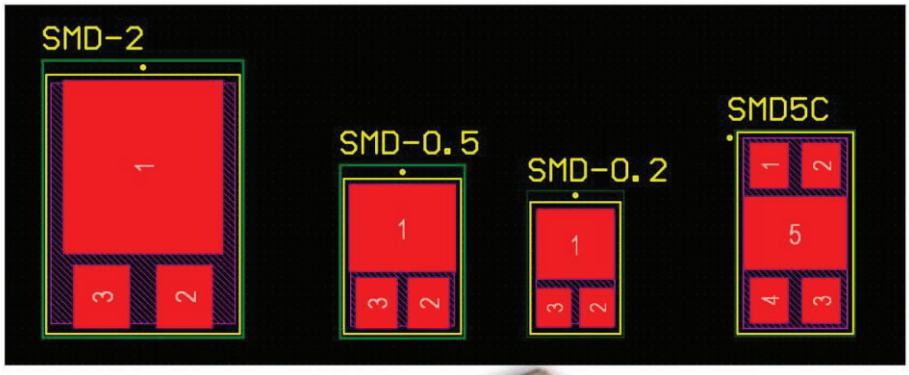

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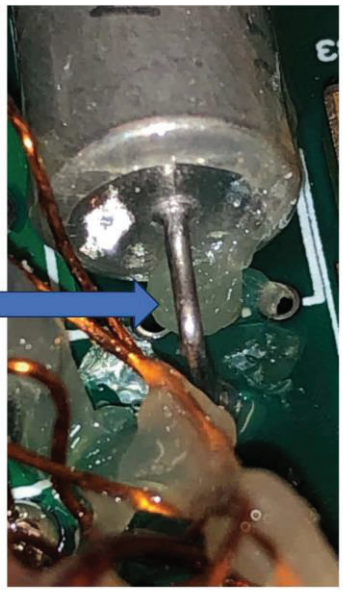
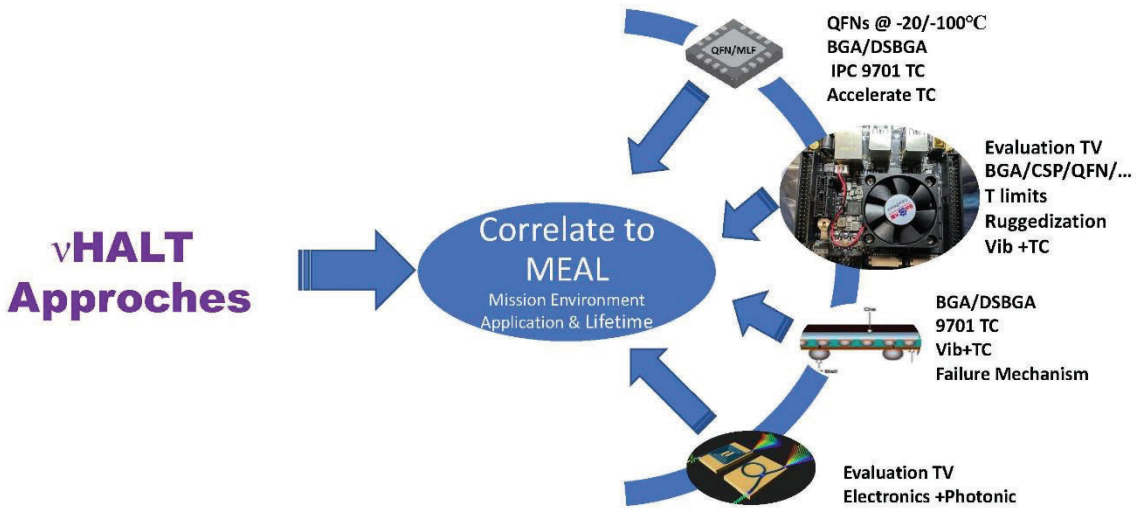
Excessive Coating

- **More is better!**
  - Over coat/bridge
  - Lead pulled out under cold TC
- **Mitigation:**
  - **Train QA**
  - **Involve SME**





Cold Thermal Step Stress to -100°C

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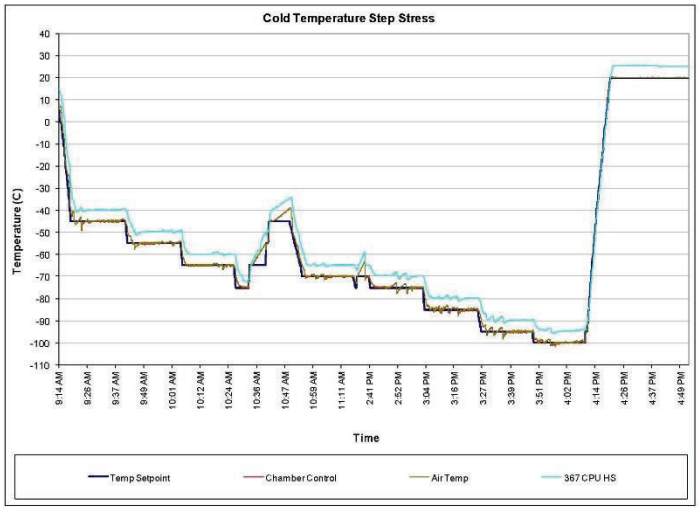
- ✓ **The unit operational to -65°C**
- At -75°C, the UUT had a kernel paging errors and became unresponsive.
  - ✓ **Unit recovered at -45°C**
- Lowered to -75°C, the unit became unresponsive, but was still online.
- The unit still online at -100°C, but was unresponsive.
- The unit brought to RT and was power cycled as it did not recover on its own



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Ruggedization: Standard Parts

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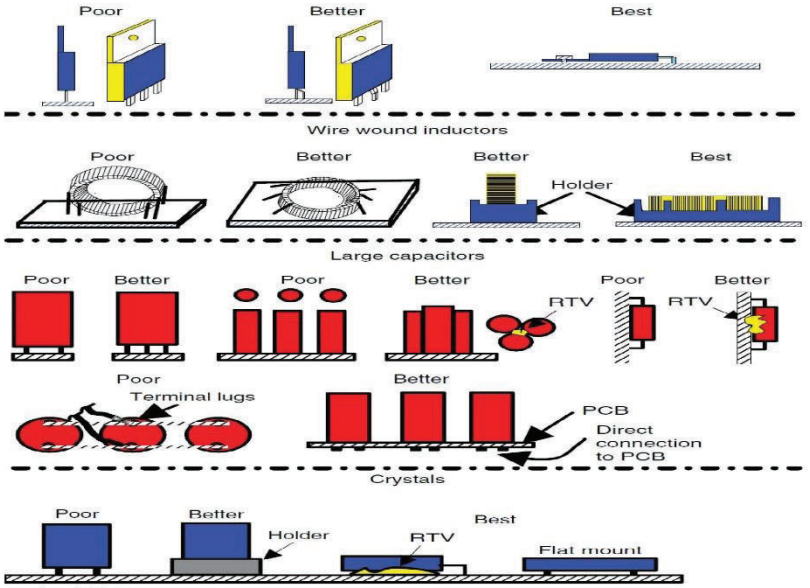
FILE: COMPMNT1.DRW



Book: Next Generation HALT and HASS

Summary

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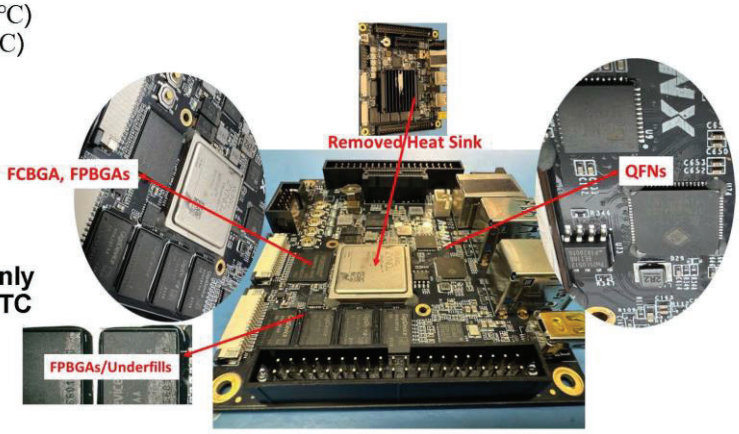
- **Establish Temp Limits**
  - ✓ Low/High Temp Limits
  - ✓ Functional under TC (-30°C/70°C)
  - ✓ Functional under TC (-40°C/85°C)
- **Completed Ruggedization**
  - ✓ Fan Removal & Ruggedization
  - ✓ Corner/Full filling
  - ✓ Heat Sink Bonding
- **Vibe +TC after Ruggedization**
  - ✓ **2 TV under thermal Cycling only**
  - ✓ **4 TV under Combined Vibe + TC**
- **Failure Analysis**
  - ✓ Visual inspection
  - ✓ X-sectional evaluation
- **Released Guidelines on HALT**



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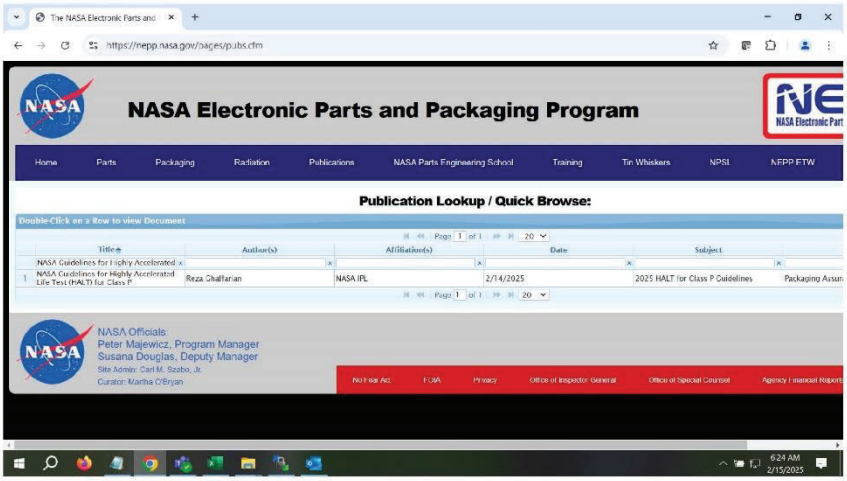
Guideline on HALT for Class P
Report Posted on the NEPP Website

Here is the direct link:
https://nepp.nasa.gov/docs/tasks/076-Packaging-Assurance/Guidelines-HALT-for-Class-P-2025Feb14-CL25-0617.pdf
Also, you can use the NEPP searchable by clicking on the "Publications" tab and typing in the title of the publication:



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Mars Perseverance Rover Status

Image of the Day: 4/16/2025
Sol 1452 Mastcam-Z mosaic of Pine Pond region with planned arm work area after sol 1478 drive (credit NASA/JPL-Caltech/ASU/MSSS/K. Powell with edits by D. Sallurday)]