



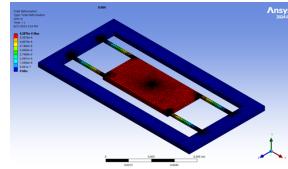
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Modeling and Experimental Evaluation Comparing Normal to c-plane Stress-Strain of Two-Step ICP Etched Microstructures.

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Simple Cantilever test structure for confirming closed form solution and Ansys model agree with literature values of Youngs modulus as most was for 6H vs 4H SiC in this work. [1,2]

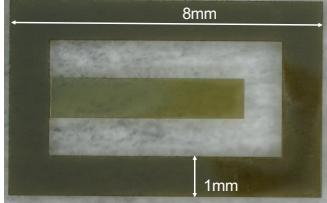
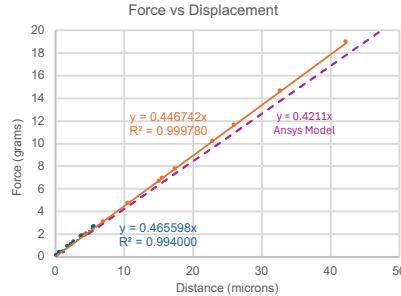
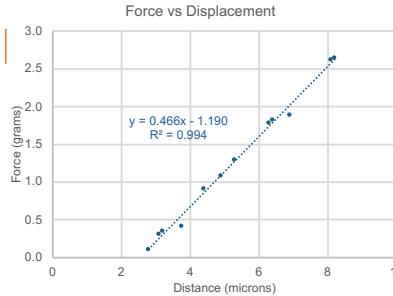


Image of test setup. A linear encoder with 0.5-micron resolution was used with a 98cm beam to divide the displacement by 5. Image insert shows the position of the down force measure with a digital scale with 0.1mg resolution. **The largest error is the accuracy of the position of the force.**

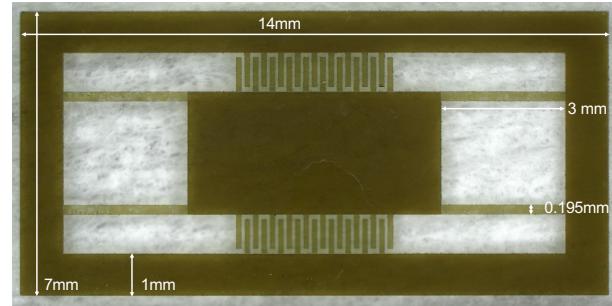


First attempts of measuring force vs deflection centered on using a stylus profilometer. The first unit had a magnet-based stylus attachment that would slip as force increased. The second unit could not hold position or return to the same location. Both were limited to only 15mg force. Both could do small surface micro machined cantilevers but not large bulk devices.

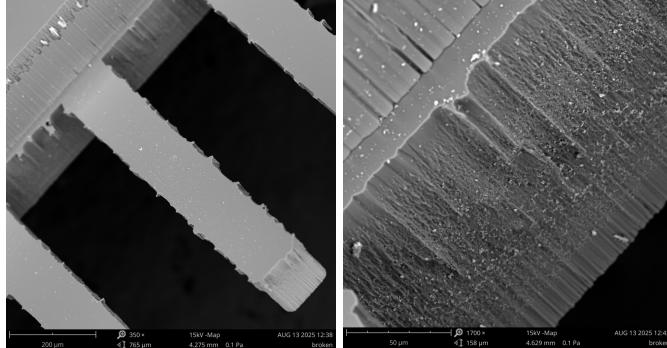
Below as the hand turned micrometer would increase position, the digital scale would measure force. The x off-set would have to be subtracted from the regression.



Simplified topology of a **seismometer** beam structure. This test structure is to verify that larger area and mostly released proof mass structures can be fabricated in SiC as has been fabricated in Si. [3,4] A **simpler design was used to enable easier modeling**.



To confirm the deformation was only that of the cantilever, a control experiment was performed by driving the stylus into the perimeter of the SiC frame and measuring the compliance of the test setup. This is labeled in blue as **Control** below with the same Simple Cantilever data sets. Additional in **Green** is the experimental data from the Seismometer and the **Ansys Model** in purple for forces normal to the center of the device. The real device would measure force in the c-plane. **The model was off by a factor of 2 in stiffness**. Also, the compliance of the setup is approaching experimental values below 20 grams.



Above is a back scatter SEM image at 15kV of the vernier like features in the seismometer test structure after the proof mass was removed. This structure is intended to be a deflection limit. The first etch of this wafer was in PlasmaPro 100 Cobra ICP RIE system using a Ni electroplated mask. This etch wall can be seen in the top left part of the image. It has a slight misalignment with the back side etch which leaves a shelf showing no trenching at the bottom edge of the etch. There is some waterfalls as the Ni mask eroded during the etch.

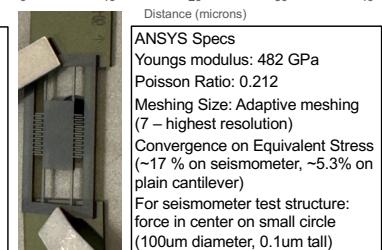
Above is a back scatter SEM image at 15kV at higher magnification of the second or back side etch that was through the wafer. It was done in a parallel plate etcher as an over etch in the wafer would damage the electrostatic chuck if performed in the ICP. The poorer side wall quality with worse waterfalls can be seen even though both etches used the same electroplated mask process. Again, the ICP etch can be seen in the upper left for comparison.

The differences between the as drawn features and the etched features were only a few microns, meaning thinner beam widths should be possible.

$$E = \frac{FL^3}{3ymaxI} \quad (1)$$

$$I = \frac{wt^3}{12} \quad (2)$$

L = 4.54 mm
w = 1.00465mm
t = 159.7μm
Wafer thickness = 367.7μm
ICP etch depth = 208.0μm
E = 421 ± 50GPa



Future Work

- Use a carrier wafer so both etches can be performed in ICP.
- Switch to SiO₂/electroplated copper for etch mask.
- Make thin and/or narrower beams for more deflection at less force.
- Make test structures more complex than the simple beam to understand where the factor of 2 difference in the Ansys model is coming from for the seismometer.
- Make a dedicated setup that is more rigid, has xy positioning, and piezoelectric z stage drives for improved resolution.
- Measure deflection in the c-plane with a shaker table at 500 °C.

Purpose of this work

In the past few years, NASA Glenn has increased the maximum operable temperature of complex 4H-SiC electronics by optimizing the back end of the line (BEOL) processes and materials. TaSi₂ interconnects, with a relatively low CTE, were tailored to be low stress at temperature. Bond pads used iridium interfacial stack (IrIS) metal [6] of TaSi₂/Pt/Ir/Pt, with a high CTE and residual stress, but were structurally anchored to the SiC. Interconnects were buried with LPCVD TEOS SiO₂ and Si₃N₄ with no high CTE metal on top. These unique solutions have demonstrated 60 days operation at Venus surface conditions [7] and (in air ambient) over a year operation at 500 °C [8] and over 100 hours at 800 °C [9,10]. MEMS sensors are needed for the same conditions and **our group will leverage these advancements in electronics, making the sensors in SiC with the same BEOL robust steps and materials, enabling monolithic integration of sensors with electronics and a unique SiC-based solution**.

[1] Tim K Hossain et al 2006 *J. Micromech. Microeng.* **16** 751

[2] R. S. Okojie et al. *Journal of Microelectromechanical Systems*, vol. 20, no. 5, pp. 1174-1183, Oct. 2011.

[3] Information at <https://www.imperial.ac.uk/news/196333/imperial-professor-tom-pike-provides-sensors/>

[4] R. Martin & W. Pike, Patent 6,196,067 B1.

[5] J. H. He et al. *Materials Science and Engineering A* **423** (2006) 143-142.

[6] D. Spry, IRIDIUM INTERFACIAL STACK (IRIS), US Patent 9,013,002, 2015.

[7] P. Neudeck et al., *IEEE Journal of the Electron Devices Society* (7), pp. 100-110, 2019.

[8] P. Neudeck et al., *Journal of Microelectronics and Electronic Packaging* 15 (4): 63-70, 2018.

[9] P. Neudeck et al., *Proc. 2018 IMAPS Int. Conf. High Temperature Electronics*, p. 71

[10] P. Neudeck and D. Spry, *Mat. Sci. Forum* 1004 (2020) 1057.