Leveraging High-Level Synthesis to Migrate Motor Control Algorithms from Microcontroller to FPGA

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Abstract

As motor control algorithms become increasingly complex, traditional microcontroller-based implementations are reaching computational limits that prevent the controller from operating at the required speed. This paper presents a novel workflow leveraging High-Level Synthesis (HLS) to migrate motor control algorithms from a microcontroller implementation to a Field-Programmable Gate Array (FPGA) implementation. The proposed approach utilizes the free Vitis HLS software to automatically convert Embedded Coder-generated C code from a Simulink model into Hardware Description Language (HDL) code suitable for FPGA deployment.

Introduction

Why move motor control from microcontrollers to FPGAs for electric aircraft?

Algorithms are outgrowing microcontrollers. Advanced motor control algorithms for aeronautics are reaching the computational limits of microcontrollers

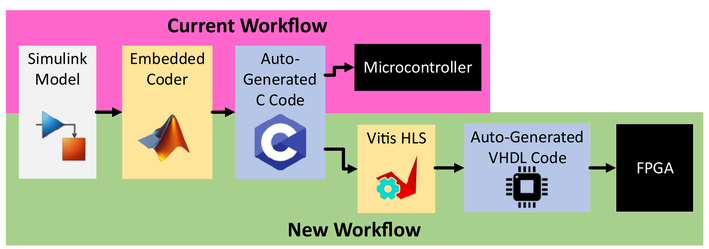
Cryogenic motor drives must deliver near-pure sinusoidal stator currents. Even small current ripple can cause losses that risk quenching superconducting windings

Filters don't fix spatial harmonics. LC filters mitigate switching harmonics, but low-frequency spatial harmonics near the fundamental frequency need to be tuned using dedicated control loops—each adds real-time computational load.

FPGAs unlock parallel processing. Parallel execution at higher operating frequencies can be used to run multiple control loops simultaneously

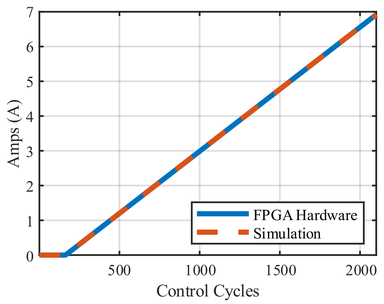
Practical migration path. High-Level Synthesis (HLS) converts Simulink-derived C to VHDL, reducing manual HDL coding effort while preserving algorithm fidelity

Methodology

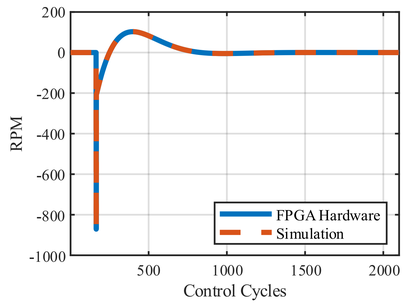


Results

Hardware testing confirmed that the FPGA implementation of the controller maintained the functional behavior of the original Simulink model.



Commanded q-axis Current (Iq*)



Speed (in RPM) Measured by the Observer

HLS Optimizations

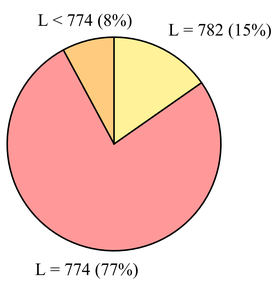
The Vitis HLS software provides optimization pragmas. Pragmas guide the tool's hardware micro-architecture without changing the algorithm's functional behavior.

Base Model:
- Motor controller model without any HLS pragmas applied

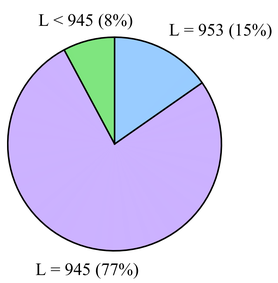
Optimized Model:
- Motor controller model with HLS pragmas applied
- Pragmas are used to limit the number of hardware instances of the sinf(), cosf(), atan2f(), and rt_hypotf() functions
- Intended to decrease FPGA resource utilization, accepting that doing so would likely increase the controller's latency

Latency

The model's latency is the number of FPGA clock cycles required for the model to complete one control cycle. Both controller models run on the FPGA using a 100MHz clock, which has a 10ns clock period.



Latency, L, in FPGA clock cycles, for the **base model**



Latency, L, in FPGA clock cycles, for the **optimized model**

FPGA Resource Utilization

	Base Model	Optimized Model	Resource Change
LUT	51,579	38,398	-26%
LUTRAM	751	539	-28%
Flip-Flops	43,367	32,010	-26%
Block RAM	9.5	6.5	-32%
DSP Slices	128	80	-38%

Look-Up Tables (LUTs): the fundamental combinational logic elements of an FPGA. They are the primary resource used for control logic

LUTRAM: refers to LUTs configured as small distributed memory rather than logic

Flip-Flops (FFs): sequential storage elements that hold binary states and synchronize logic operations between clock cycles

Block RAM (BRAM): dedicated on-chip memory blocks that provide larger and more efficient storage than LUTRAM

Digital Signal Processing (DSP) Slices: specialized arithmetic units essential for signal processing, filtering, and computationally intensive algorithms

Conclusions

This work demonstrates that HLS tools provide a practical, cost-effective pathway for migrating motor control algorithms from standard microcontrollers to FPGAs.

The proposed workflow preserves established Simulink-based processes while unlocking the high-performance capabilities of FPGA hardware.

Integrating free tools like Vitis HLS into this workflow improves efficiency, accelerates development, and reduces costs associated with the development of advanced motor control systems.

The scalability and reliability of this approach is validated by the successful migration of the full motor control algorithm.

The next step is to integrate the FPGA controller with power electronics to drive a physical motor, verifying that our control implementation is practically sound as indicated by comparison with simulation.

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