AC AND DC FAULT MANAGEMENT FOR MEGAWATT ELECTRIFIED AIRCRAFT ELECTRICAL POWERTRAINS

TASK 2: POWER QUALITY FILTERING USING NANO-CRYSTALLINE SOFT MAGNETIC INDUCTOR

FINAL REPORT

Prepared for
NASA Glenn Research Center
21000 Brookpark Road
Cleveland, OH 44135
Attention: Andrew Woodworth

Prepared by
Raytheon Technologies Corporation
Pratt & Whitney
400 Main Street
East Harford, CT 06118 USA

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ACRONYMS

	A
AC	Alternating Current
ADC	Analog to Digital Converter
	C
CA	Collins Aerospace
CM	Common Mode
COTS	Component/Commercial off the Shelf
	D
DC	Direct Current
DM	Differential Mode
DPT	Double Pulse Tester
	E
EAP	Electrified Aviation Propulsion
EMI	Electromagnetic Interference
EMC	Electromagnetic Compatibility
	F
FFT	Fast Fourier Transform
FEA	Finite Element Analysis
	G
GRC	Glenn Research Center
GSE	Generalized Steinmetz Equation
	L
LCR	Inductance Current Resistor
	N
NASA	National Aeronautics and Space Administration
	P
PWM	Pulse-Width Modulation
P&W	Pratt & Whitney
	R
RC	Resistor Capacitor
RTAPS	Research and Technology for Aerospace Propulsion Systems
RTRC	RTX Technology Research Center
RTX	Raytheon Technology Corporation
	S
SM	Soft Magnetics
SiC	Silicon Carbide
	T
TC	Thermocouple

1. EXECUTIVE SUMMARY

The NASA RTAPS program on AC and DC Fault Management for Megawatt Electrified Power Train is a multi-year joint project with Pratt & Whitney (P&W), Collins Aerospace (CA), and RTX Technology Research Center (RTRC). This research program focuses on the high-voltage distribution issues that present a significant technological obstacle in the adoption of Electrified Aviation Propulsion (EAP) systems. One challenge to the adoption of high-voltage distribution systems with power electronic converters is the need for filter elements to limit the generation and propagation of noise, protect the cable systems from premature aging and prevent against excessive heating within subcomponents due to high-frequency induced currents. While increased distribution voltages aide in reducing the cable mass for a fixed power system, the associated mass with the filtering elements for power electronic converter can grow with increasing distribution voltages – thereby mitigating any benefit associated with increasing the distribution system voltage. To enable high-voltage distribution systems with high system specific power densities, new magnetic materials must be developed. Therefore, the second task of the NASA RTAPS program is associated with the design and application of advanced soft magnetic components for Megawatt class electric propulsion systems, specifically the motor drive system.

This report covers the collaborative work between NASA Glenn Research Center (GRC), RTRC, P&W and CA in the development of three types of magnetic components over the span of the three-year program. These critical magnetic components are the DC side EMI filter, which limits the propagation of harmful electromagnetic noise to the rise of the distribution system, and the AC side damping with the dv/dt filter, which limits the fast rise time of the power electronic converter output voltage to limit the degradation on the cable/motor insulation systems. Each of these components are investigated from component level design and are optimized at the system level with a combined modelling and testing effort. In the final experimental evaluation of the NASA developed soft magnetic material with a dv/dt filter, a commercial-off-the-shelf (COTS) magnetic core and the GRC magnetic core are optimized and loaded at 320Arms to evaluate their difference in performance. After a run time of 30 minutes in a MW-class motor driver at RTRC, the NASA GRC cores were found to not only offer a lower temperature rise of nearly $25°C$, but also a reduction in measured core loss of 25% (12.75W to 9.5W).

2. INTRODUCTION

Magnetic filtering forms a critical element in interfacing the power electronic converter with the rest of the electrical system. Fast voltage transitions, that exist when synthesizing the objective AC voltage from the DC bus voltage through high frequency Pulse-Width Modulation (PWM), can lead to breakdown of the insulation in motor windings, reflected voltages across the cable system, and electromagnetic interference (EMI) that can disrupt the operation of other components within the network. Further, as the permeability of magnetic components is relatively low compared to the permittivity of electrical components, such as capacitors, the energy storage density of filters used for power electronic converters results in bulky components. Thus, it is typical that the EMI filter and dv/dt filter, of which the latter is responsible for slowing the voltage transition rate of the output voltage, form a significant portion of the total drive volume in the modern more electric aircraft. Moreover, due to the volumetric form factor of magnetic components – often being composed of wires with poor filling factors within the magnetic window of the core – suffer from poor thermal performance, which is only further exasperated by the elevated ambient condition in aviation environments. Thus, the development of new filtering technology is mandatory in order to make strides to support the ambition of further electrification in future aviation systems.

In this task, RTRC has partnered with NASA GRC to develop the high-performance filter components, leveraging GRC's expertise on advanced nanocomposite magnetic materials and fabrication processes with RTRC's experience in the application of magnetic components in aviation environments. This work began in 2021 and continued until December of 2023. Primarily, this task under the NASA RTAPS program is broken down into four key developmental efforts:

- Soft magnetic core characterization at high temperatures.
- Dv/dt filter specification, modeling, and design in a MW motor drive system.
- EMI specifications, component design and validation test.
- Filter power loss estimation and thermal performance evaluation.

3. SOFT MAGNETIC FILTER DESIGN AND EVALUATION

This section covers the design of the dv/dt filter, damping and EMI filters. The outcome of this section to establish a methodology for the design of these filter elements prior to developing a testing framework to be addressed in proceeding sections.

3.1. Filter Specification and Modeling of Transmission Line Effect

In a typical electric propulsion drive train, the airframe hosted motor drives may be likely connected to motors through long feeder cables. Motor drives increasingly employ fast switching SiC modules to minimize switching losses of the semiconductor devices and improve the drive efficiency. However, the fast-switching transient, i.e., high dv/dt, can lead to up to three times the nominal voltage seen at the motor terminals -- depending on the cable length and the PWM modulation pulse pattern. Hence a dv/dt filter is needed to slow down the high dv/dt edges, attenuate the reflected voltage on the motor side and reduce the motor insulation requirements due to the overvoltage.

In the approach taken by the RTRC team, several limitations in matching the tested voltage reflection waveform in terms of peak voltage, oscillation frequency and damping speed are first identified, which are not well covered in literature. A parametric design optimization based on widely adopted LCR topology is adopted, which not only alleviates the voltage stress of motor terminals but also minimizes the power loss of the passive damping resistor. As the dv/dt filter parameters are tightly affected by the cable length and geometry, a model based design approach is carried out with two major steps: 1) first, utilizing the existing 7 meter target cable in RTRC lab to develop the transmission line effect model and build a corresponding 7 meter test rig for model validation, 2) extend the verified high fidelity model to the envisioned final electric propulsion demonstration system, where 120-130 ft long cables are needed. Lastly, design and verify the dv/dt filter for such a system through the pure simulation model, which is then tested in the down-scaled lab test rig.

3.1.1. Modeling of Transmission Line Effect in Motor Drive System

Cable impedance characterization: to develop a better estimate of the required dv/dt filter inductor requirements, the envisioned aerospace cable needs to be characterized. The per unit parameters used in the above models are typically obtained from cable impedance measurement using short-circuit and open-circuit approaches. Due to the frequency-dependent characteristics of the impedance, schemes on how to derive these key line parameters with the frequency of interests (from low frequency to high frequency end) are reported and illustrated in Fig. 2-1. One challenge is to decouple the self and coupling inductance in multiple phase cables, and another is to properly measure the frequency-dependent cable ac resistance with high accuracy across several or tens of MHz range. RTRC's partner, Stony Brook University, assisted in this cable testing effort.

The cable characterization setup is shown in Fig. 3-2, and the cable impedance is measured using a Bode 100 Analyzer and later double confirmed with a Keysight impedance analyzer. The 3-phase equivalent circuit model of the cable is shown in Fig. 3-3 and the extracted parameters are listed in Table 3-1. The impedance measurement and the model validation results are shown in Fig. 3-4 for different test configurations.

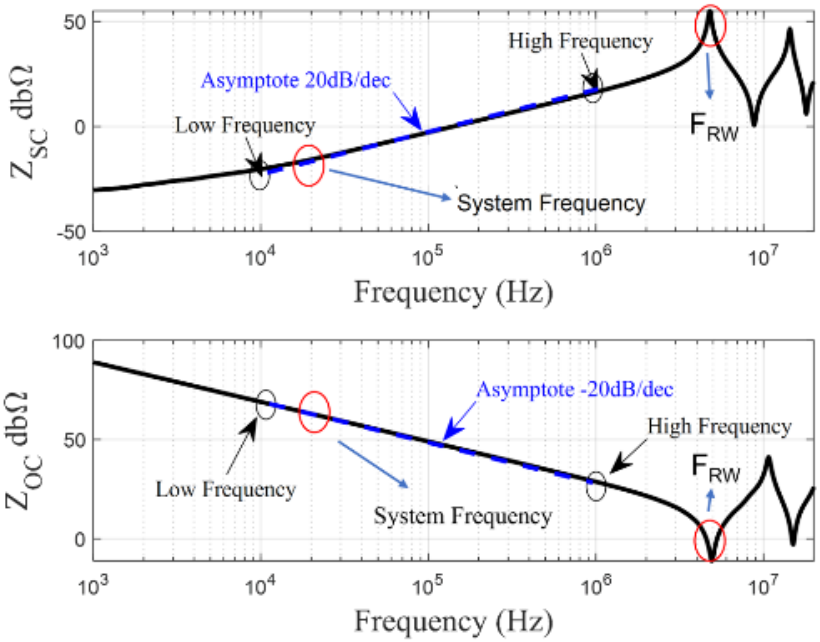


Fig. 3-1. *Line Parameter Extraction Based on Impedance Measurements of Short Circuit and Open Circuit and HF & LF Range Selection*

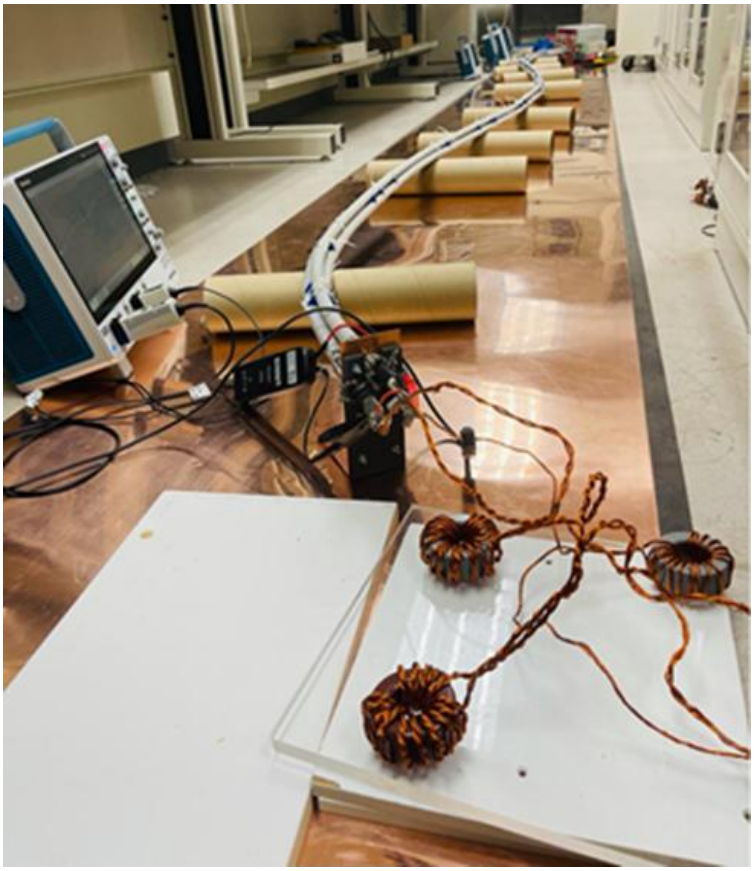


Fig. 3-2. *Transmission Line Effect Test Set Up at SBU*

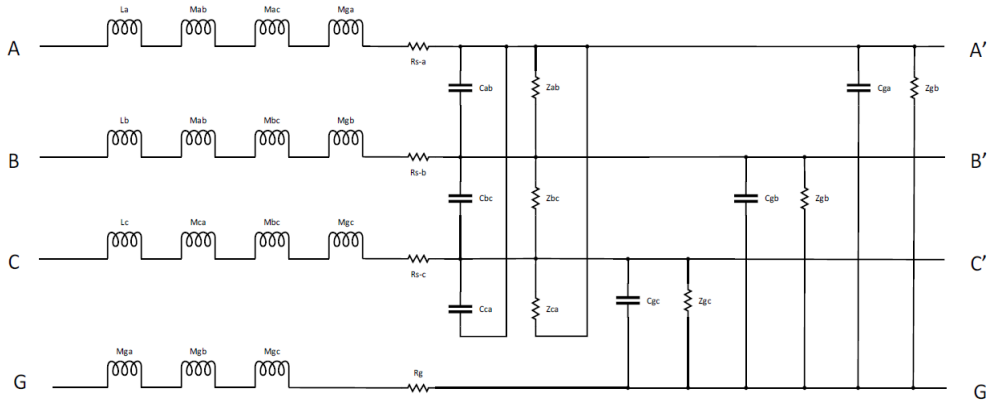


Fig. 3-3. *Equivalent 3-Phase Cable Mode*

Table 3-1. *Extracted Cable Parameters*

Parameter Extracted	Magnitude
R_a	36 mΩ
L_a	0.650 uH
C_g	5.632 nF
C_{ab}	0.06 nF
R_g	40 mΩ
L_g	0.35 uH
K for M_{ab}	0.25

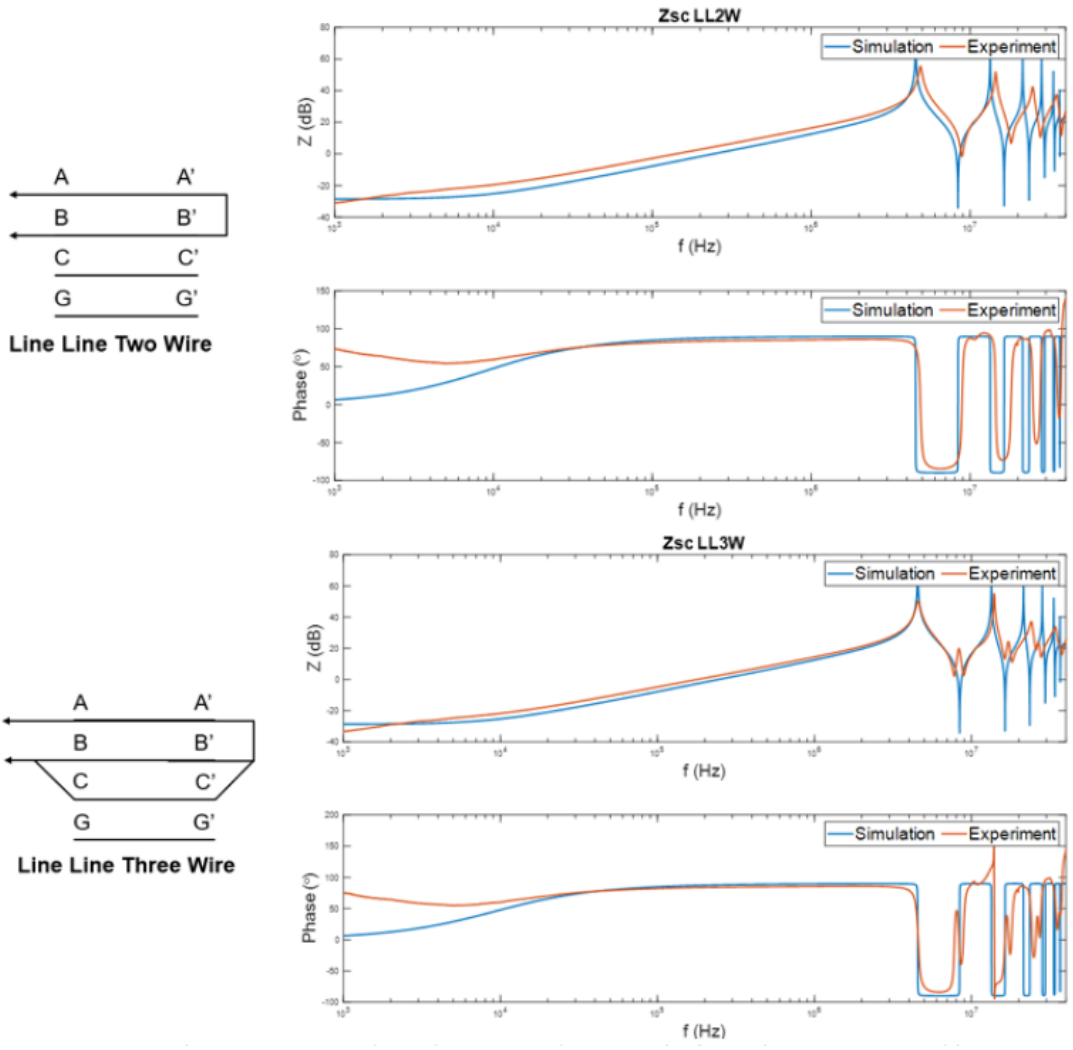


Fig. 3-4. *Comparing the Experiment and Simulation Impedance Results a) Line-Line Two Wire Short Circuit b) Line-Line Three Wire Short Circuit Test*

On the other hand, the RTRC team also explored the pure analytical modeling approach with the hope that it may save a lengthy cable measurement process. Although models based on transmission line theory and electromagnetic field analysis have been developed for various cables configuration with single or multiple conductors from the literature, it is found that analytical models are only accurate for the inductance calculation of the unshielded line-line cables or single coaxial cable (shield as return path). When considering the strongly shielded line-line cables (one forward and one return, each has its own shield), the analytical models for the inductance seem only accurate at relatively low frequency but degrade at higher frequency based on the team's experimental testing. Further, state-of-art models do not consider the impact of the shield of single-wire cable yet. From the team's observation, the negative coupling and induced eddy currents seems stronger at the high frequency range due to the presence of the shield layer. Consequently, more research might be needed in this area if a practical analytical approach is desired.

For the resistance modeling, a good match has been observed with measurements below hundreds of kHz for the shielded cables. However, above this frequency range, analytical results show significantly underestimated values based on the team's preliminary study. This highlights the impact of the accuracy in reflection voltage modeling, since the strong damping effect might be underestimated using the calculated

low ac resistance at MHz range. It is also noted that mixed accuracy performance has been reported in literature for the analytical model [1-2]. As with the inductance modeling, further research is needed here.

Power Converter Modeling: For a dv/dt filter design, the power converter is traditionally simplified as an ideal PWM step source or source with predefined dv/dt slope. This approach is simple but does not truly represent the actual excitation source of the PWM converters. It is also unable to capture the accumulated impact of adjacent pulses on the reflected overvoltage. More importantly, it fails to present the interaction between the source and the cable when reflection voltage is traveling back and forth due to the impedance mismatch in the interconnected driving system. An alternative approach can be developed using the measured open-loop terminal voltages of the PWM converter in the place of the idealized voltage source, but it fails as this also does not capture the impedance interaction – as seen later in Fig. 3-10.

Therefore, to provide a high-fidelity model that includes the characteristics of the reflected voltages, a detailed converter model including parasitic inductances and parasitic grounding capacitances is recommended. When the converter output dv/dt matches the actual operation, this method can predict the results with good accuracy. The interaction between the parasitic impedances of the converter and its switching speed affects the voltage overshoot significantly, while the ringing frequency on the cable is determined by the passive cable impedances. Further, when an interface cable of relatively short length is used to bridge the PWM converter and the AC cable, a degree of mismatch between the predicted and measured behavior is found if the impedance of this short interface cable is neglected in the model, as shown in Fig. 3-5. This could be improved as shown in Fig. 3-8.

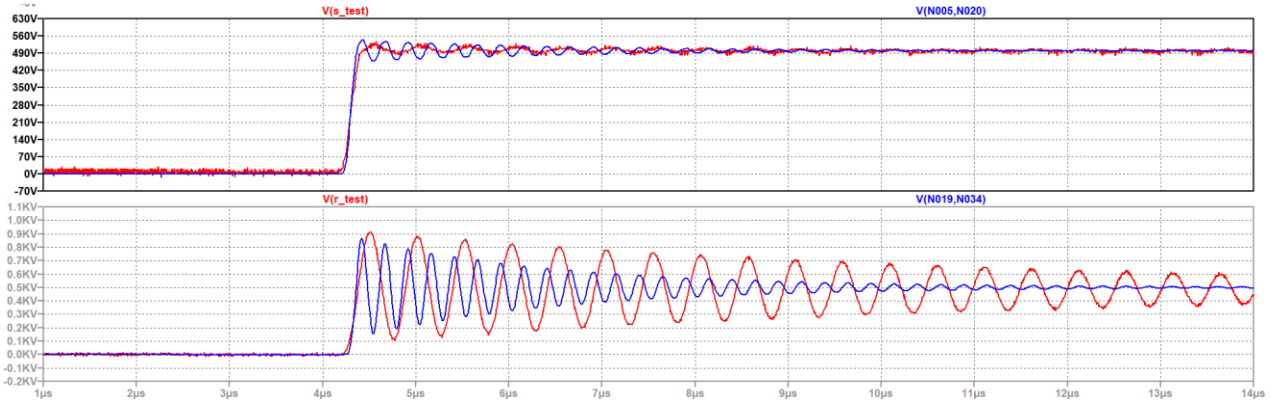


Fig. 3-5. *Reflection Voltage of Modeling (in Blue) and Testing (in Red) Results without Including the Interface Wire's Impedance in the Model. Top: Converter, Bottom: Cable Far-End Side.*

Overall System Modeling: a practical modeling approach and verification test rig is proposed for the reflection voltage estimation and dv/dt filter design. On the converter side, as shown in Fig. 2-6, the three-phase motor drive is used as the PWM excitation source to study how the pulse gaps or modulation index impact the reflection voltage. On the cable end, three-phase shielded cables are formed as a single loop whose two phases out of three are connected and paralleled to form the return path. On the load end, considering the generic usage of a motor drive and dv/dt filter for potentially different motors or loads, the 'no load condition' is adopted. Although the motor impedance may have certain impacts on the motor terminal stress, an open circuit creates the worst-case scenario with the highest voltage stress induced due to full voltage reflection, and further, the verification of cable model accuracy and attenuation performance of dv/dt filter also does not need the motor. Hence, an open circuit simulation/test with cables is sufficient. This also avoids the unnecessary complexity of modeling the motor as well. However, if the focus is on internal wiring voltage distribution and turn-turn insulation stress of the motor, a detailed motor model is certainly required.

To capture the effect of the inverter impedance on the transmission line effect, detailed SiC chip-level models with the device parasitic capacitances, as well as the parasitic impedances of the circuit are included in the model. The cable is segmented into 1-meter sections connected in series to simulate the 7-meter cable RTRC has in the experimental test rig.

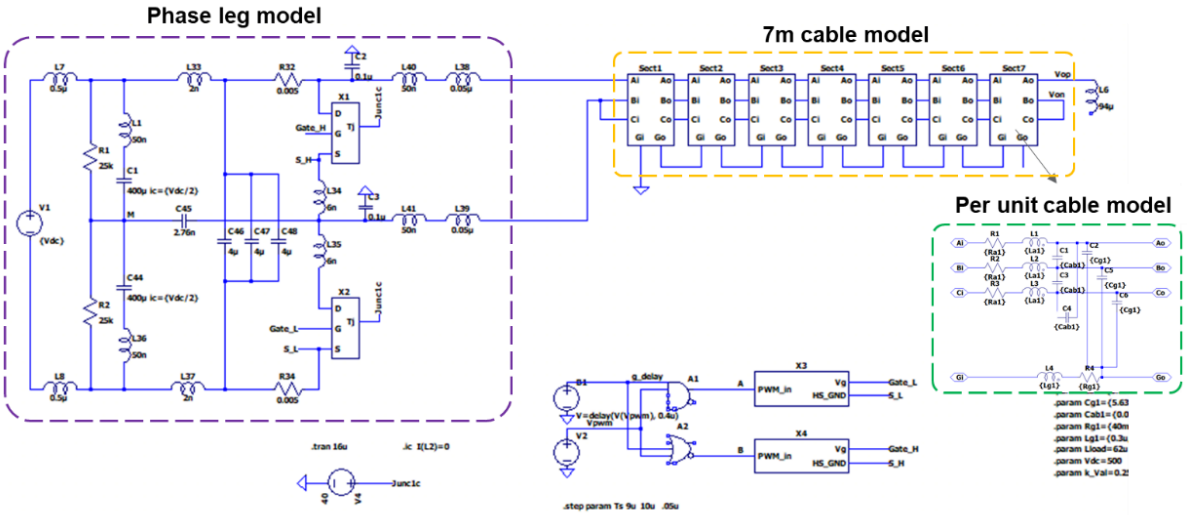


Fig. 3-6. *LTspice Based Single Phase DPT Based Simulation Model with a Phase Leg of PWM Converter and 7 Sections of 1-Meter Lumped ɔ Shape Cable Model*

The detailed cable impedance model of the three-phase is provided in Fig. 3-7 for one section, where the paralleled R-L represents the skin/proximity effect related ac resistance. The couplings among the line inductances are also included.

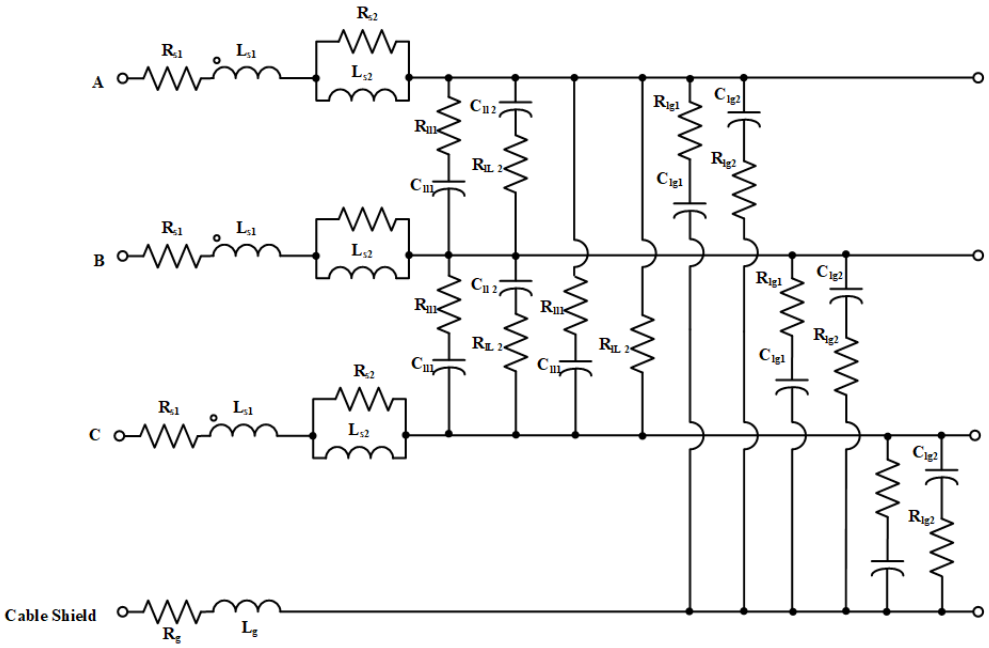


Fig. 3-7. *Cable Impedance Model per Section for the Three-Phase Shielded Cables*

As mentioned previously, any potential interface wire between cable and inverter should be considered in the simulation model. Due to the limitation of the experimental test rig, an interface wire of several feet is adopted between the converter terminals and bulky three-phase motor cables. Its inductance and resistance (L38-L40 in Fig. 3-6) are required to be included in the model – as shorter or wider the cable necessarily reduces the impact on the modeling of overvoltage stress. Thus, an effort has been made to minimize this set of wire as short as possible in the setup. Fig. 3-8 illustrate the significant difference when the 0.48 µH inductance of a short interface wire is considered, compared to poor modeling accuracy in Fig. 3-5.

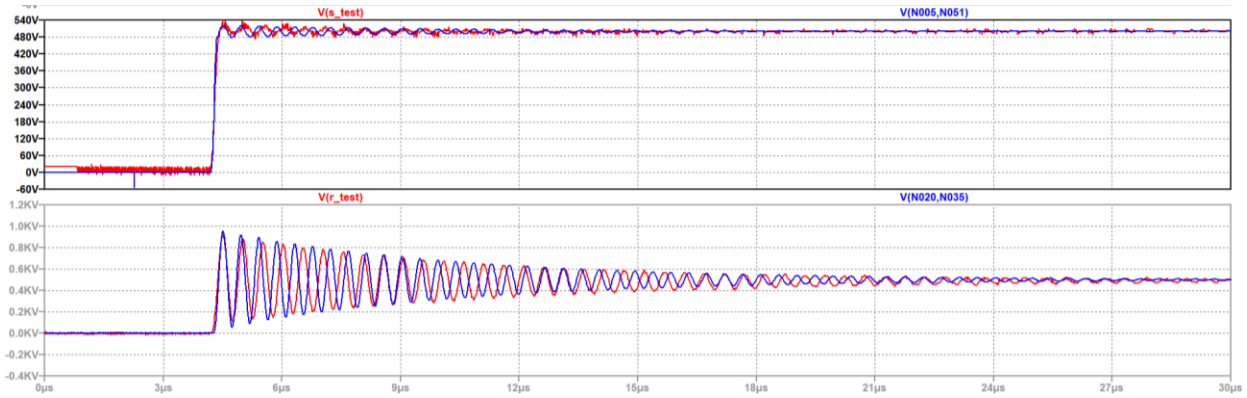


Fig. 3-8. *Reflection Voltage of Modeling (in Blue) and Testing (in Red) Results (Bottom) When Including the Impedance of the Interface Wire in the Model. Top: Converter Side, Bottom: Cable Far-End Side*

A comparison is also conducted between the presented modeling approach and a simplified method based on an ideal voltage source. As illustrated in Fig. 3-9, the simplified method incorporates the measured PWM voltage waveforms of the converter terminals as an ideal voltage excitation source to the cable impedance.

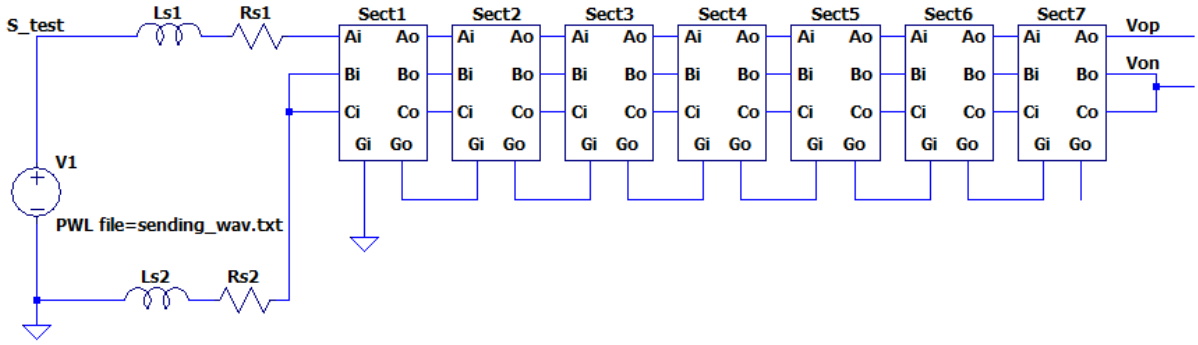


Fig. 3-9. *LTspice Based Simulation Model using Measured PWM Converter Waveform as Ideal Excitation Source*

As per Fig. 3-10, the simplified method illustrates significantly different peak voltage and oscillation damping time. The simplified method might be acceptable to predict the first peak of load side voltage but fails to correctly predict the whole behaviors after that. This is likely due to the break of the interaction of traveling wave reflection when the converter side is modeled by a controlled voltage source.

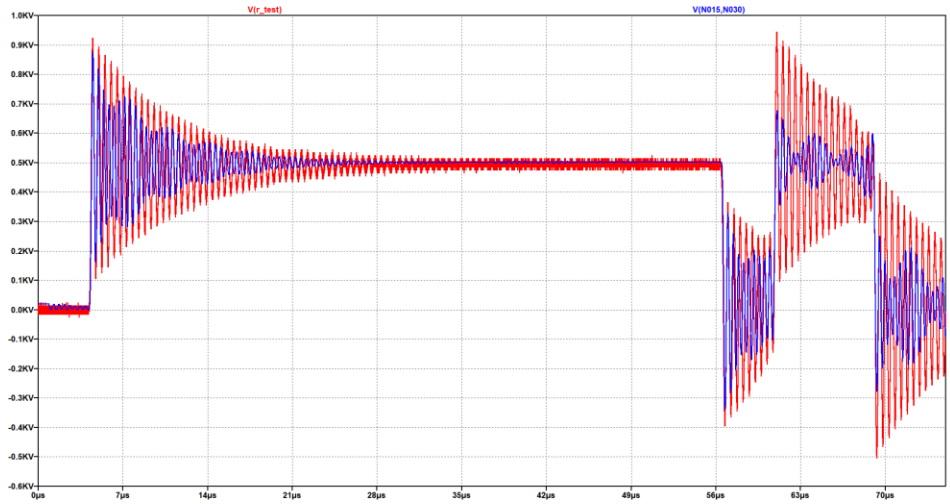


Fig. 3-10. *Reflection Voltage of Modeling (in Blue) and Testing (in Red) Results Based on the Simplified Modeling Approach with Measured PWM Output Voltage Waveforms as the Excitation Source to Eliminate Converter Modeling*

3.1.2. Validation of Modeled Reflection Voltage

A single-phase double pulse test (DPT) setup is implemented to validate the cable model. A set of three-phase cable is connected to the single-phase leg of the three-level inverter, with phase A of the three-phase cables connected to the positive DC bus (DC+); phase B and C are shorted at both ends and connected to the AC output of the phase leg. The load side of the cables are open to emulate the worst-case scenario for transmission line effect with maximum reflection. Further, the shield layer of all three phases is shorted at both ends and the inverter side of the shield is grounded.

The transmission line effect test setup is implemented at RTRC, as shown in Fig. 3-11. A set of 7m three phase 4/0 cable is connected to Phase A of the RTRC developed 1 MW motor drive system. The other ends of the cables are open to capture the worst-case scenario. A copper plate is used to terminate the EMC shielding, and the inverter side of the shielding is connected to the ground through the inverter chassis. Cable spacers are used to separate the cables to replicate the planned installation in the aircraft. To mitigate the interface wire issue mentioned in the previous section, the filter connection with the bulky cables and the motor controller terminals are improved to minimize the length of the interface wire as much as possible. This effort improves the agreement between the simulation model and test reflection voltage as seen from Fig. 3-13, compared to Fig 3-5 and Fig. 3-10. As illustrated, a 750 V peak voltage (25% overshoot) and significant oscillations are observed on the cable far end without adding the dv/dt filter.

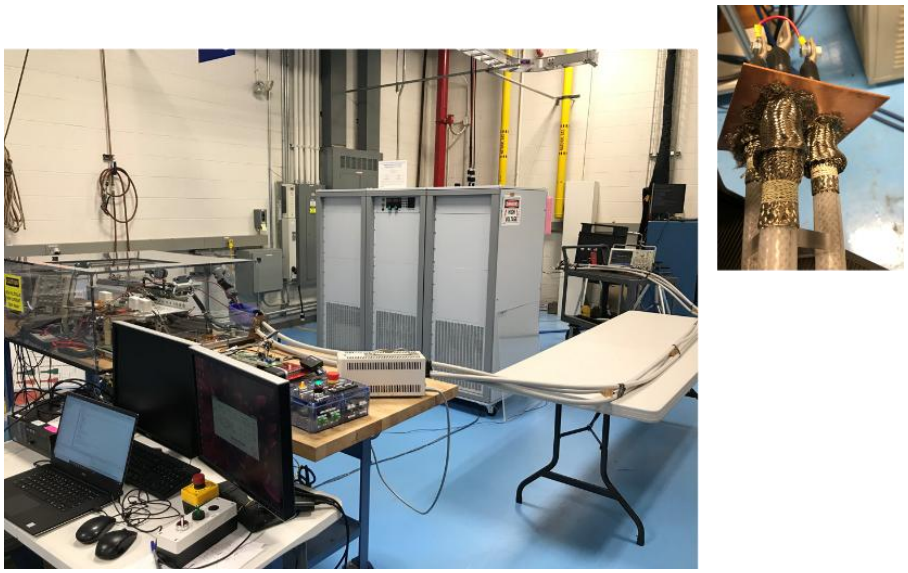


Fig. 3-11. *Transmission Line Effect Test Rig at RTRC*

The test results match well with the simulation waveform, as shown in Fig. 3-12. The red traces are test results, and the blue traces are simulation results.

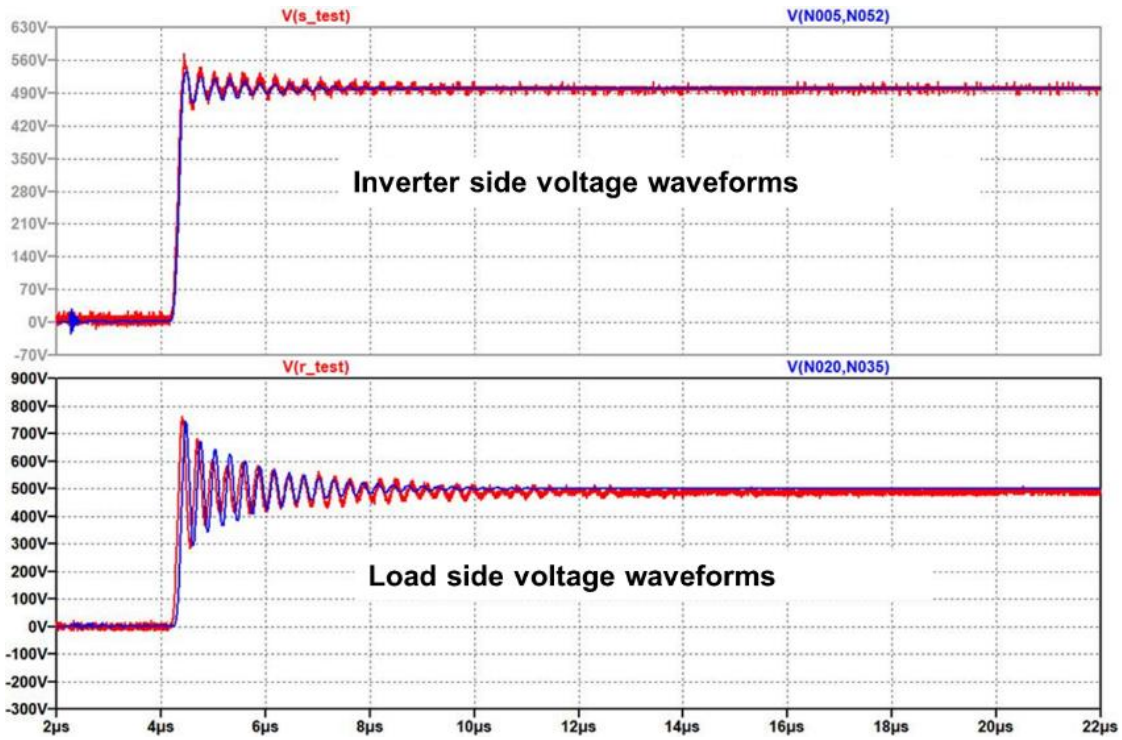


Fig. 3-12. *Reflection Voltage of Modeling (in Blue) and Testing (in Red) Results in the Improved Setup with Shorter Interface Wire, and dv/dt Filter is Not Applied. Top: Converter Side, Bottom: Cable Far-End Side*

3.1.3. Preliminary dv/dt Filter Design and Inductor Core Specification

A single-stage LCR dv/dt filter topology is selected due to its common application and inherent simplicity, as shown in Figure 3-13. An optimization-based approach is adopted to determine the filter parameters without over dimensioning the design. This approach accounts for the impedances of the inverter and allows the designer to decide between the level of voltage attenuation and filter losses.

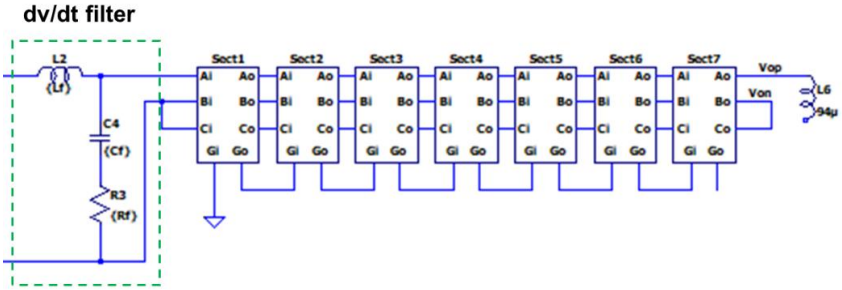


Figure 3-13. *LCR dv/dt Filter Schematic*

The first step is to determine the base values of the filter parameters. The voltage drop across the filter inductor should be minimal, i.e.,

$$L \leq \min\left(\frac{V_{ph}\beta}{2\pi f I_{ph}}\right) = \frac{V_{ph}\beta}{2\pi f_{max} I_{ph}} \quad (1)$$

where V_{ph} is the phase voltage of the inverter, f_{max} is the maximum fundamental frequency and I_{ph} is the phase current. If the percentage voltage drop across the inductor is limited to β=1% of $V_{ph,}$ then the maximum value of L can be calculated as follows:

$$L_{max}=637/\text{sqrt}(3)*0.01/(2*\text{pi}*1.2e3)/625 = 0.78\ \mu H \quad (2)$$

The reactive power stored in the filter capacitor should be limited to a minimum value as well, i.e.,

$$C \leq \min\left(\frac{Q*\gamma}{3*2\pi f {V_{ph}}^2}\right) = \frac{P*tan(\text{acos}(PF))*\gamma}{3*2\pi f_{max} {V_{ph}}^2} \quad (3)$$

where Q are P are the reactive and real power of the inverter, respectively; PF is the power factor. If the reactive power stored in the capacitor is limited to γ=1%, the maximum capactance value can be determined as C_{max} = 3.1 µF.

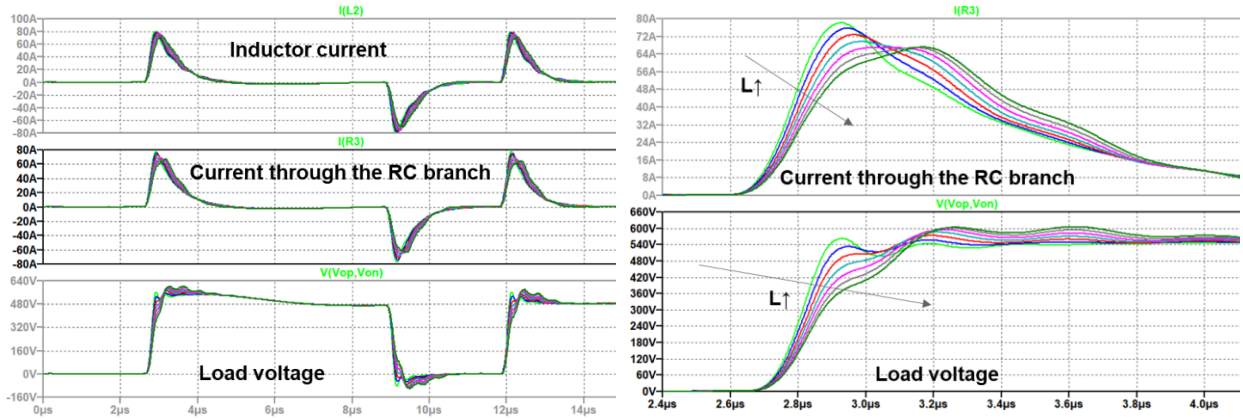
The corner frequency of the LCR filter must be smaller than the cable frequency, and hence, the intrinsic frequency of the 7m feeder cable is:

$$f_{cable} \approx \frac{1}{4l\sqrt{L_o C_o}} = 3.3\ \text{MHz} \quad (4)$$

The corner frequency of the dv/dt filter is:

$$f_{dvdt} = \frac{1}{\pi*\max(t_r,t_f)} = 2.1\ MHz \quad (5)$$

Further, the effect of varying filter inductance on the system waveforms are studied through simulation with the system LTspice model incorporating the filter and cable model. Fig. 3-14 shows the change in the switching waveforms as the inductance value varies from 0.1 to 0.7µH at a 0.1 µH interval. The filter resistance and capacitance are fixed at 5Ω and 100nF, respectively. An inductance of 0.5µH is chosen to achieve desired load voltage attenuation to satisfy cable and machine insulation requirements, without excessive losses in the RC branch.

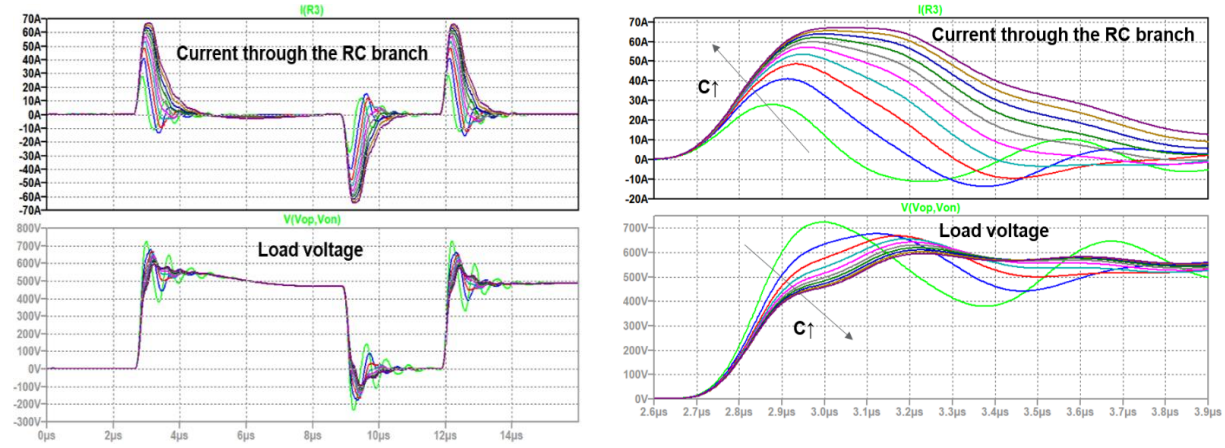


(a) Effect of L on waveforms

(b) Zoomed in RC branch current and load voltage waveforms with varying L

Fig. 3-14. *Effect of Varying L (0.1~0.7µH, at 0.1µH Interval), R=5ohm, C=100nF*

The effect of the capacitance values is also evaluated, with Fig. 3-15 illustrating the effects of varying values on the switching waveforms. It can be observed that with larger capacitance, the load voltage peak voltage is smaller. However, larger capacitance also means higher current through the RC branch, and hence higher power losses. Hence, a capacitance value between 40nF to 60nF provides a good compromise between load voltage attenuation and additional power losses. In this design, a capacitance value of 47nF is chosen based on commercial component availability.



(a) Effect of C on waveforms

(b) Zoomed in RC branch current and load voltage waveforms with varying C

Fig. 3-15. *Effect of Varying C (10~100nF, at 10nF interval), R=5Ω, L=0.5µH*

Varying the value of resistance has limited significant impact on the load peak voltage, but it impacts the power losses in the dv/dt filter significantly. In this design, the resistance is chosen as 10Ω. Finally, L-R-C parameters for the 7-meter system are selected as **L=0.5µH, R=5Ω, C=47 nF**, with the simulated performance with the dv/dt filter is shown in Fig. 3-16.

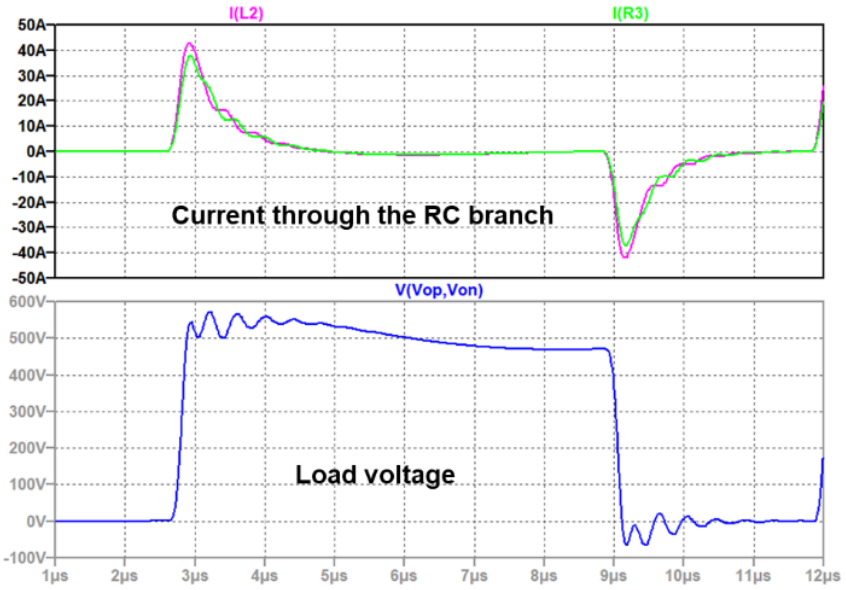


Fig. 3-16. *Simulation Results with dv/dt Filter*

Based on this preliminary design, the geometry of the inductor core is optimized for the best combination of weight and length through a series of conductor arrangement and outer/inner diameter trade-off. The length and mass of the inductor assembly are optimized to minimize the weight and volume of the dv/dt filter assembly, as shown in Fig. 3-17.

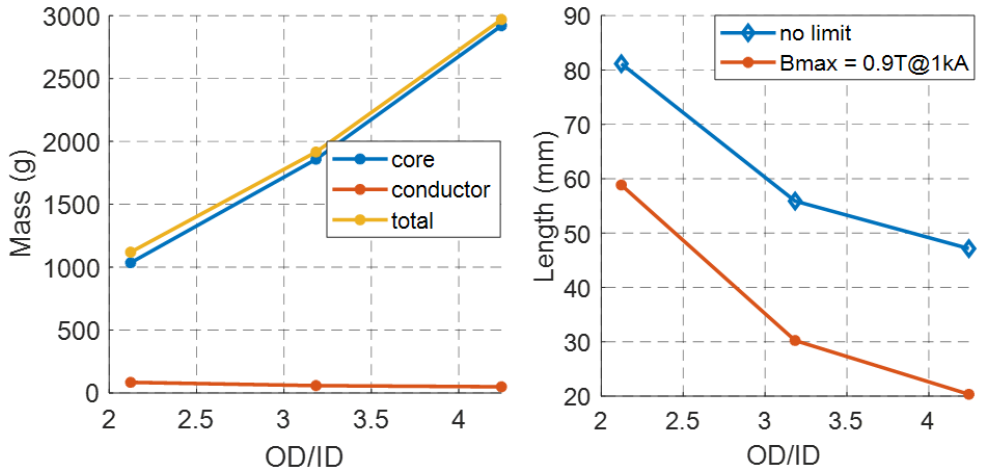


Fig. 3-17. *Core Geometry Optimization Results*

The height of the bus bar is slightly over twice the skin depth of a 1.2 kHz AC signal, and two parallel bus bar configuration is selected to better utilized the core window area. Relative to area, the NASA team developed a series of cores with different inductance to form several inductance options for rapid preliminary testing and verification, as shown in Fig. 3-18.

L (uH)	ID (mm)	OD (mm)	h (mm)	μ_i	μ_o	mass (g)
0.1	24.5	35.6	25	55	80	78
0.2	24.5	46.7	25	55	105	180
0.3	24.5	57.8	25	55	130	305
0.5	24.5	80.1	25	55	180	614
2 x 0.25	24.5	52.3	50	55	117	480

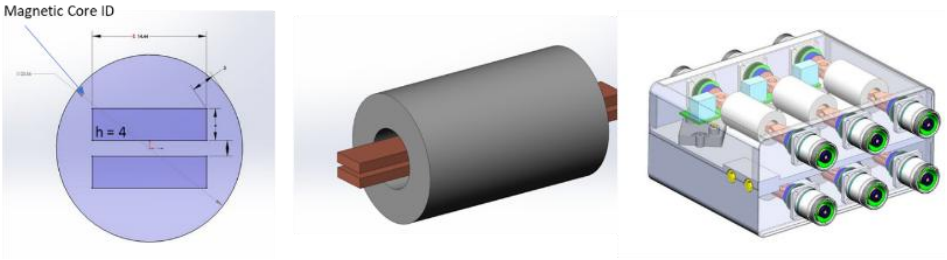


Fig. 3-18. *Inductor Specification for 7-Meter Cable System*

3.1.4. Preliminary Filter Testing for 7 Meter Cable System

Out of the five NASA GRC cores, the magnetic cores B and E (Fig. 3-19) provided the required inductance and were used to build the single phase dv/dt filter prototype, as shown in Fig. 3-20. The test results are provided in Fig. 3-21 and Fig. 3-22 with the insertion of the designed filter.

Fig. 3-19. *Soft Magnetic Cores from NASA (B_{max}=0.9T, 80% Stacking)*

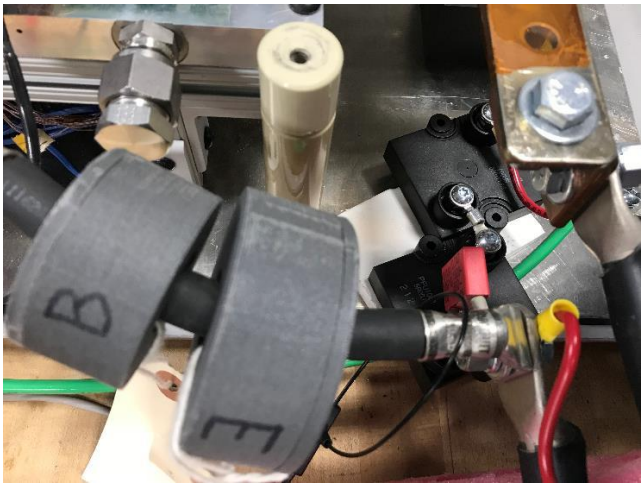


Fig. 3-20. *Single Phase dv/dt Filter Implmentation*

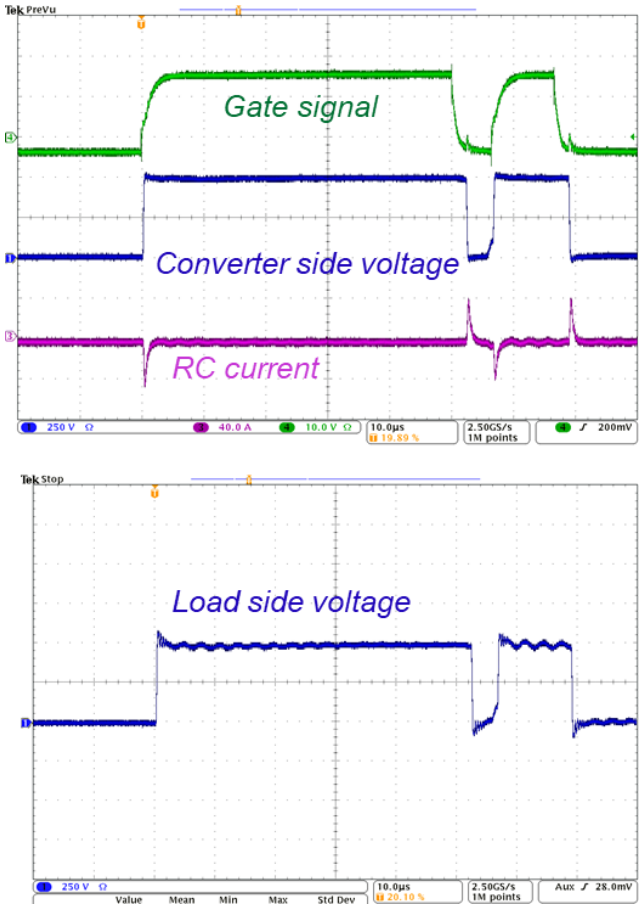


Fig. 3-21. *Results with dv/dt Filter Designed and Tested in 7 Meter Cable System*

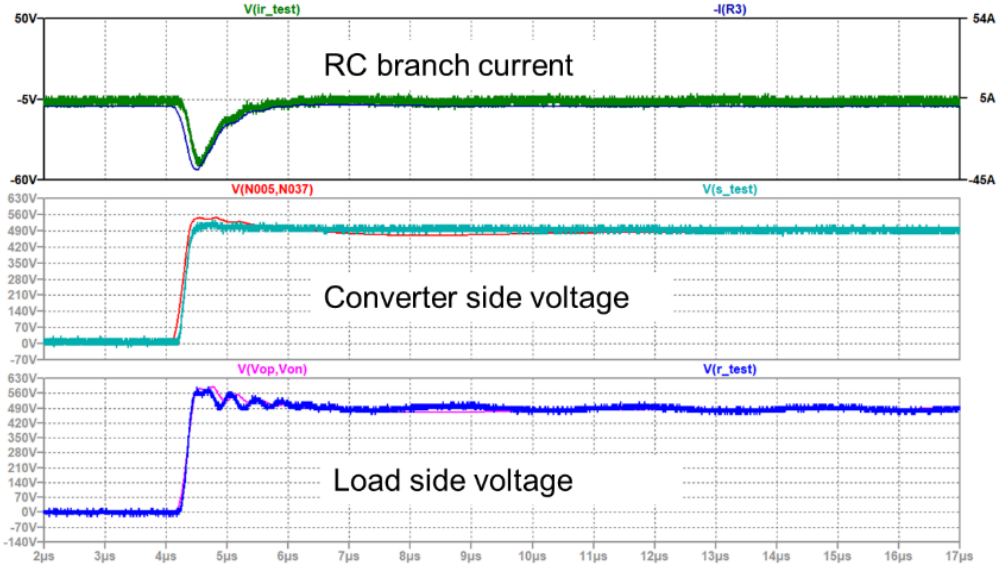


Fig. 3-22. *Simulation and Test Results Comparison with dv/dt Filter (Green, Teal and Blue Traces are Test Results)*

A 23% over voltage reduction is achieve through the dv/dt filter, as compared with the case without filter in Fig. 3-23.

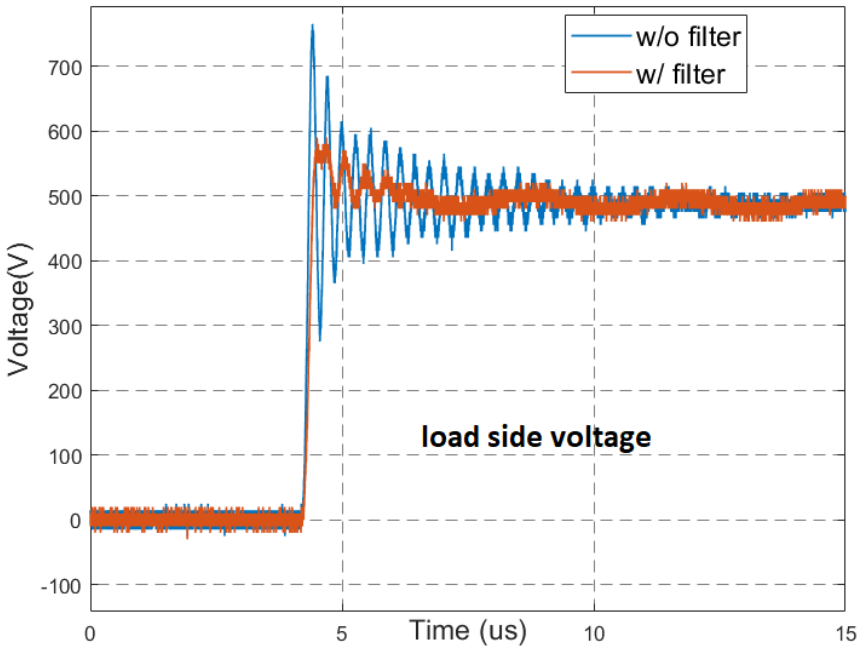


Fig. 3-23. *Tested Load Voltage with and without the dv/dt Filter in 7 Meter Cable System*

3.2. Three-Phase dv/dt Filter Design

The same method applied in the 7 m cable system is directly adopted for specifying the filter inductance, resistance and capacitance required to mitigate the voltage stress and high frequency ringing caused by reflected waves in the envisioned flight demonstration system with approximately 120 ft long AC feeder cables. The final parameters L=0.7 μH, C= 47nF, R = 10 Ω are selected which help reduce the voltage stress by 19% drop through the DPT system simulation. A sensitive study is also conducted to evaluate the impact of DC bus voltage and cable length on the overvoltage mitigation. As seen from Fig. 3-24, the voltage stress mitigation is slightly impacted by the DC link voltage, which are likely due to the voltage dependent behavior of power device switching speed and its junction capacitance. However, the designed filter is less sensitive to the cable length when 100ft, 120 ft, and 130 ft lengths are considered.

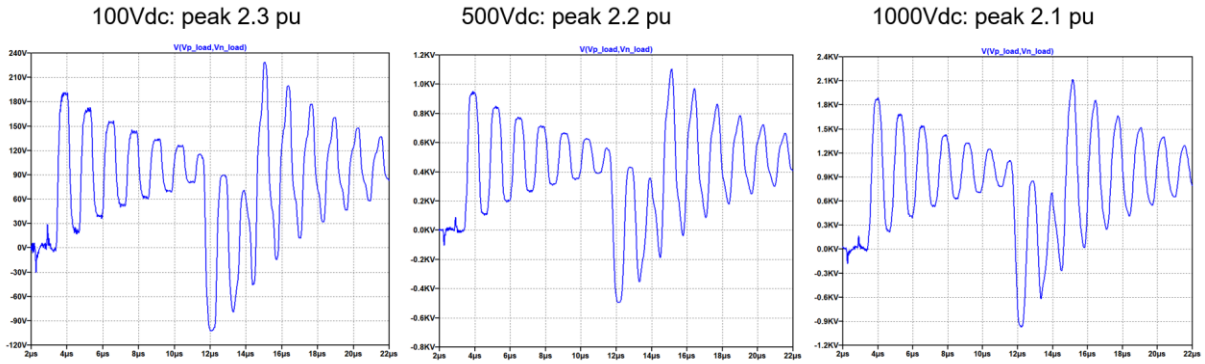


Fig. 3-24. *Voltage Stress Sensitivity over DC Link Voltage in the Filtered System*

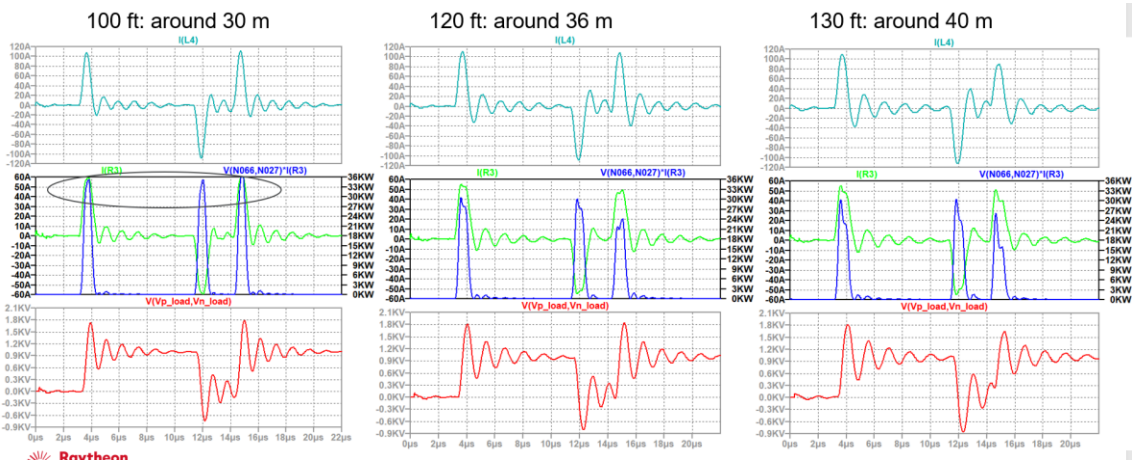


Fig. 2-25. *Voltage Stress Sensitivity over AC Cable Length in the Filtered System*

To evaluate the performance of the soft magnetic core developed by NASA GRC team, two sets of three-phase dv/dt filters with the same parameters are designed for comparative study. Fig. 3-26 provides the two dv/dt filter units built, the first with commercial inductor amorphous cores and the second with NASA GRC soft magnetic (nano-crystalline) cores.

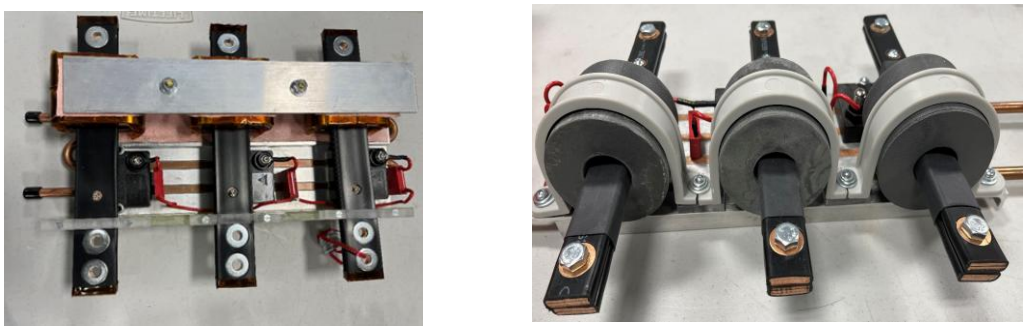


Fig. 3-26. *dv/dt Filter Units with Baseline COTS Cores (Left) and NASA GRC Cores (Right)*

3.3. EMI Filter Inductor Core Characterization

To determine the core losses, the area under the BH curve during excitation is the core loss per volume per cycle, which requires measuring magnetic field (H) and flux density (B). Since the core geometry and winding geometry are known, a sense winding is used to indirectly provide the flux density swing associated with the magnetic field, indirectly associated with the winding current. The schematic of this method is shown in Fig. 3-27, where the primary winding has the inductor current, and the sense winding is left open. In this approach, the reflected impedance from the open winding does not corrupt the primary winding current, and due to the open winding, there is no voltage drop associated with the secondary winding impedance – allowing for a direct reflection of induced voltage from the magnetizing flux. A one-watt external resistor Rext is used to limit the dc bias current. Note: a few tests were taken at room temperature to ensure that the external resistor does not affect the core loss measurement. The test platform is developed in RTRC lab for this measurement as shown in Fig. 3-28.

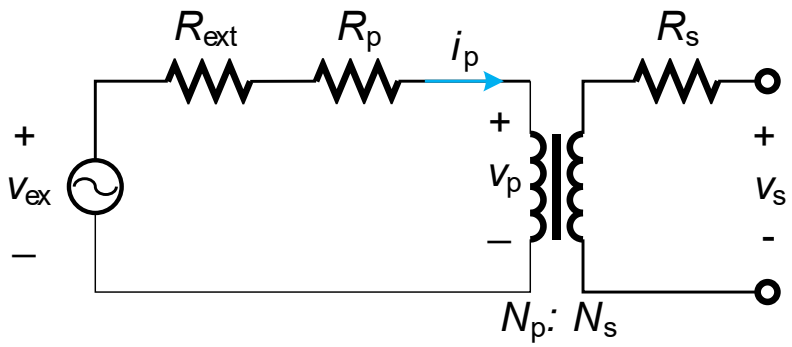


Fig. 3-27. *Core Loss Measurement Circuit Schematic*

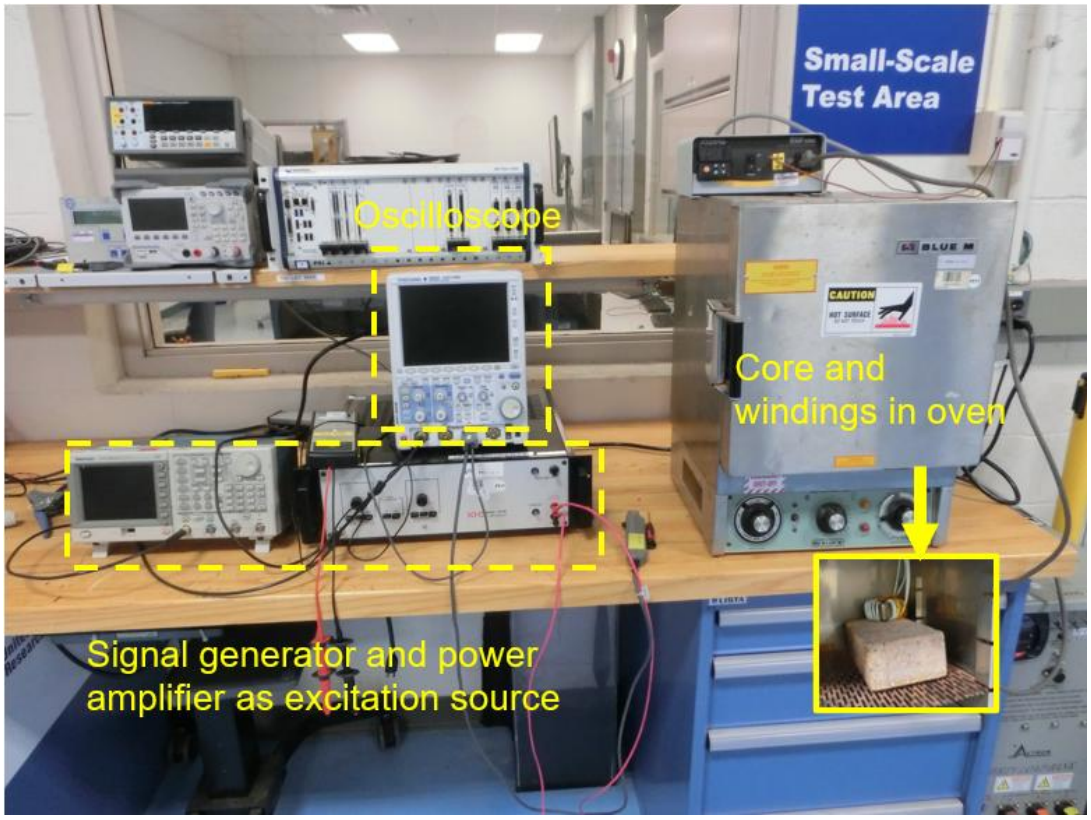


Fig. 3-28. *Core Loss Measurement Test Rig*

The NASA provided common mode inductor core is characterized at room temperature, and the measurement results (as shown in Fig. 2-29) are consistent with those from the NASA team. These cores are then characterized over a range of excitation frequencies from 1 kHz to 20 kHz and a varying temperature from 50 ˚C to 200 °C. Fig. 2-30 shows that core losses of the GRC cast and fabricated core are unaffected by operating temperature. This test procedure was repeated a week later at 100 ºC, with Fig. 2-31 showing the losses are slightly lower in the second set than the first set.

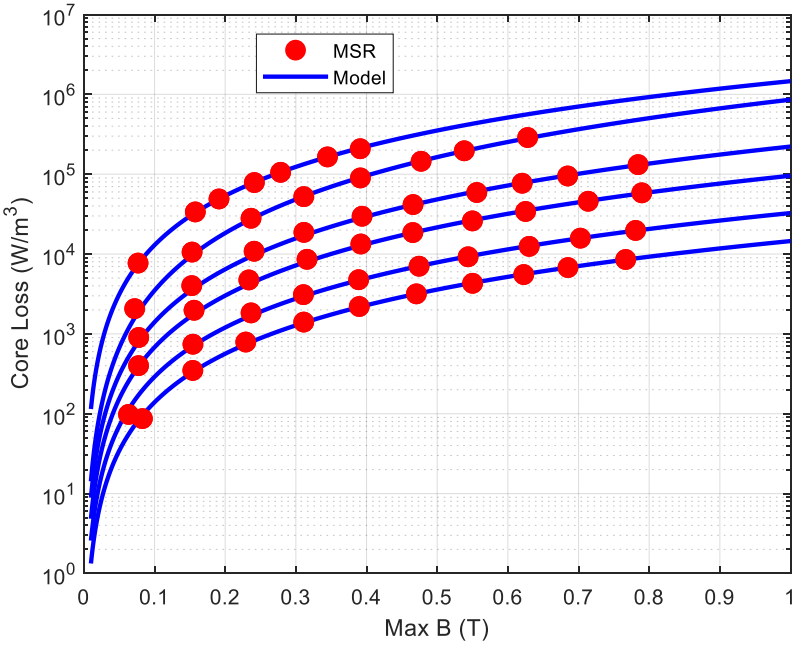


Fig. 3-29. *Common Mode Inductor Core Loss Measurement Results*

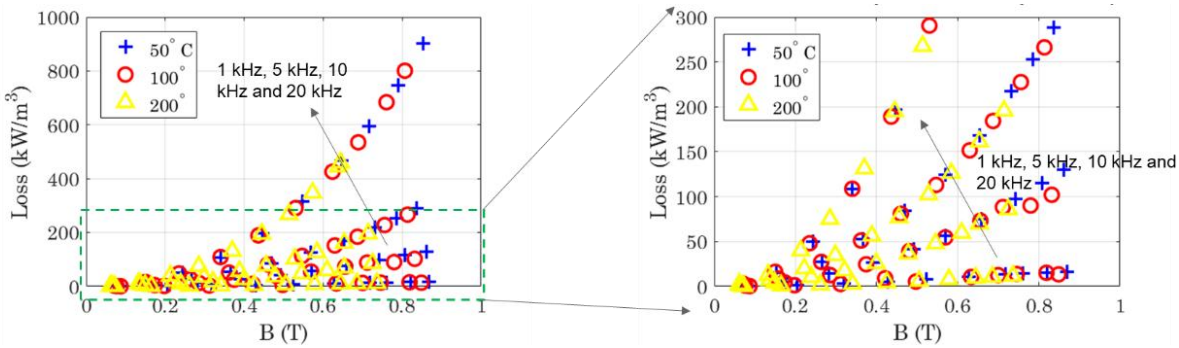


Fig. 3-30. *Core Loss Versus Field at a Range of Temperatures*

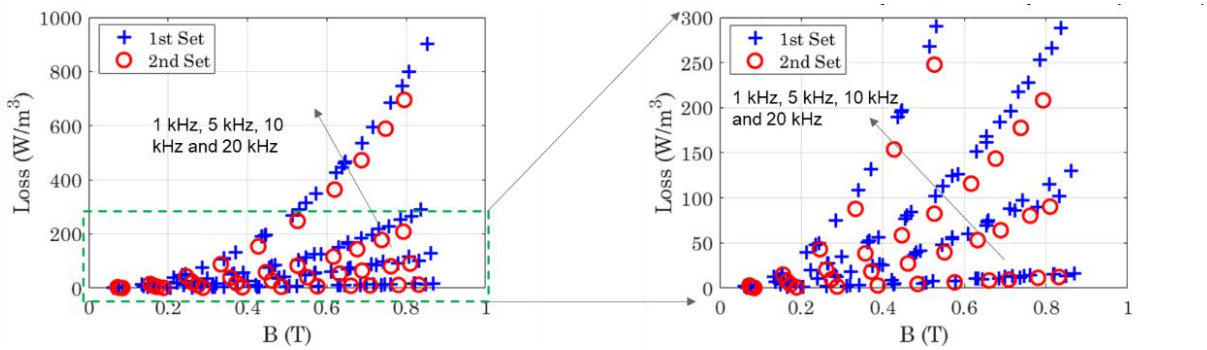


Fig. 3-31 *Core Loss in Two Test Sets*

3.4. EMI Noise Reduction and Resonance Mitigation

To provide the specifications for EMI filter inductor cores that NASA team would need for core casting and fabrication, EMI noise level must first be characterized. The procedure starts with the existing off-the-shelf DC side EMI filter together with the newly designed dv/dt filter on the AC side to evaluate the EMI noise and then narrows down the filter parameter selection by referring to the existing EMI filter parameters. In the best case, if the off-the-shelf core-based filter helps meet the EMI emission standard, the same parameters could be utilized for NASA GRC core design.

A dedicated EMI testing platform is therefore built in RTRC lab following DO-160 standard, as illustrated in Fig. 3-32, where 6-phase 7-meter cable is arranged in a zig-zag manner on the grounded earth plane and connects the 1 MW motor controller to a motor emulation load with 6-phase L and R load in series with neutral-to-ground capacitance.

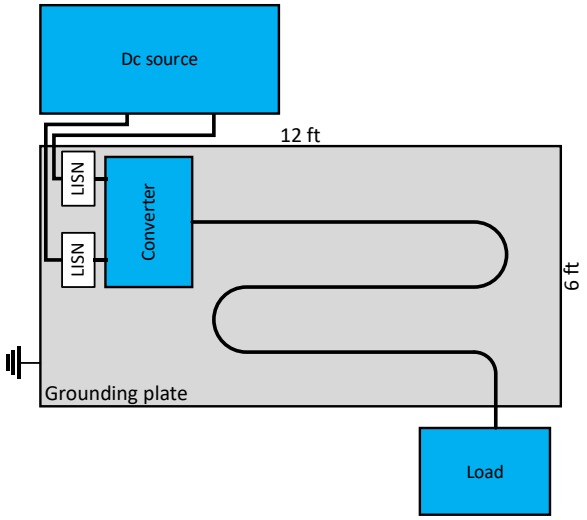


Fig. 3-32. *Draft Layout of EMI Setup per DO-160*

3.4.1. Noise Reduction Through Modulation

To reduce the EMI noise and minimize the size and weight of passive filter components, several active approaches through PWM modulation strategy are explored due to the dependency of the EMI spectrum on the modulation depth (M) and phase displacement (θ), as per Fig. 3-33, when driving a 6-phase motor drive. The first solution is to control the phase displacement of the dual sets of the three-phase voltages outputted from the inverter.

$$v(t) = \frac{V_{dc}}{2}\cos(\omega_0 t) + \frac{V_{dc}}{\pi}\sum_{m=1}^{\infty}\frac{1}{m}\sum_{n=-\infty}^{+\infty}J_n(m\pi M)\cos(n\pi)\sin\left(\frac{n}{2}\pi\right)\cos\left[m\omega_c t + n(\omega_0+\theta)t\right] \quad (6)$$

Sixty-degree phase displacement is found to provide the maximum harmonic reduction, as shown in the simulated current spectra in Fig. 3-34. As a result, the CM inductance required is reduced from 150 μH to 10 μH.

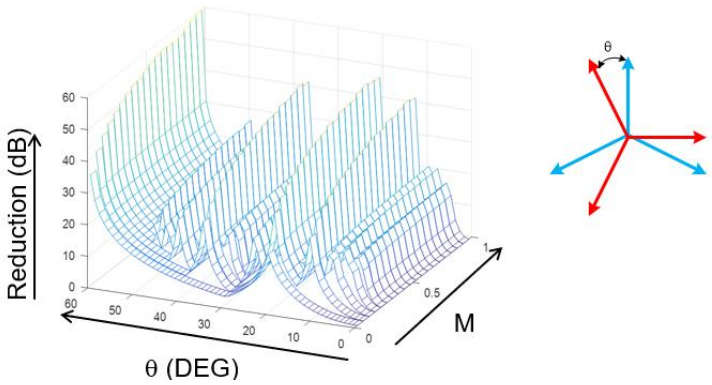


Fig. 3-33. *Maximum Harmonic Reduction due to Phase Displacement on (M, q) Plane*

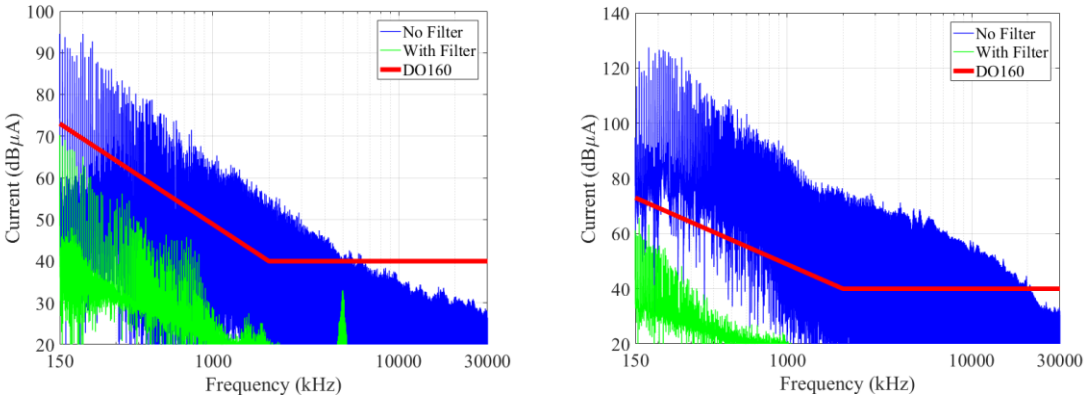


Fig. 2-34. *Simulated EMI Noise Reduction with 60 Degree (Left) and 0 Degree (Right) Phase Displacement*

The second solution is to further shift the PWM carriers of the dual three-phase sub-inverters by 180 degrees, which helps reduce the high frequency current ripples on the DC link side and lower the DC-link capacitor rms current and thermal stress. In addition, this technique reduces the DC side CM EMI noise if used with 60-degree phase shift control. Overall, about 30 dB reduction is achieved at low frequency due to the CM cancellation modulation, and this cancellation is effective up to 9 MHz on AC side and 3 MHz on DC side, as demonstrated in tested results in Fig. 3-35.

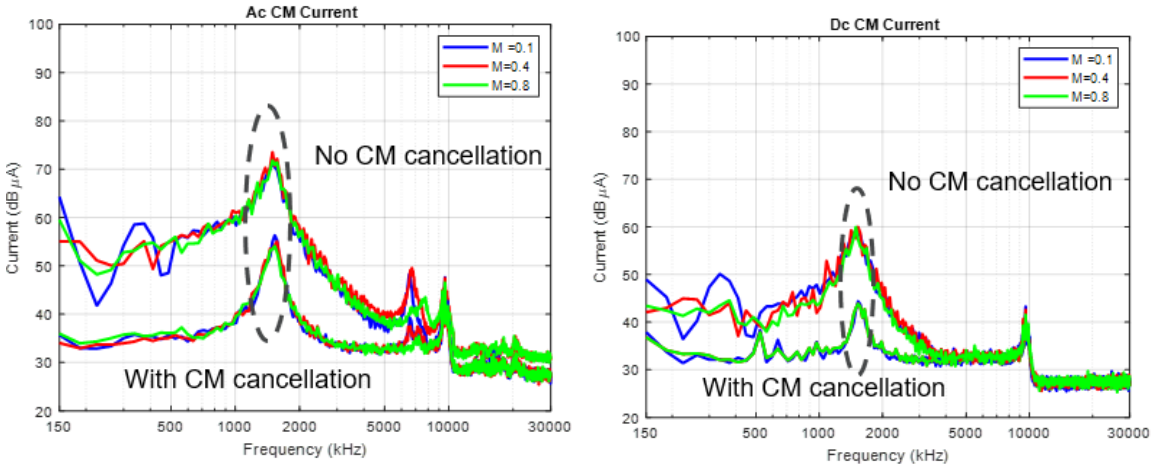


Fig. 3-35. *Tested AC (Left) and DC (Right) CM EMI Noise Reduction with 60-Degree Phase Displacement*

3.4.2. Resonance and Mitigation

Through the initial test, several types of resonance behaviors are observed in this system. The first behavior is that the DM (differential mode) noise on the DC side has a high peak of around 10 MHz @ 400V and has a strong voltage dependence. As clearly seen from Fig. 3-36, when DC voltage increases, the resonance peak shifts to higher frequency range. The same voltage dependence is not observed on the AC side and hence is likely related to the DC side circuit in the motor drive. This behavior is likely due to the switching commutation loop ringing between the loop inductance ESL and the junction capacitance Coss of the power modules on the DC side, which is voltage dependent as illustrated in the device datasheet Fig. 3-37 Under this assumption, adding a high-frequency DM capacitor with lower ESL impedance would reduce the ringing.

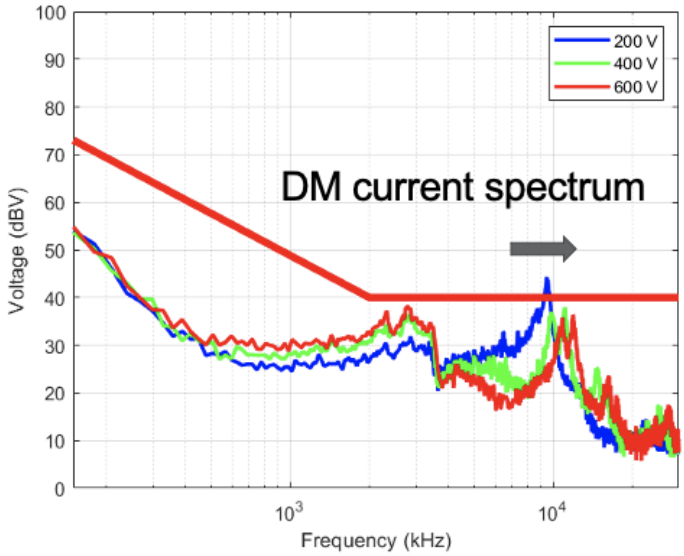


Fig. 3-36. *DC DM Noise Resonance Showing Voltage Dependence*

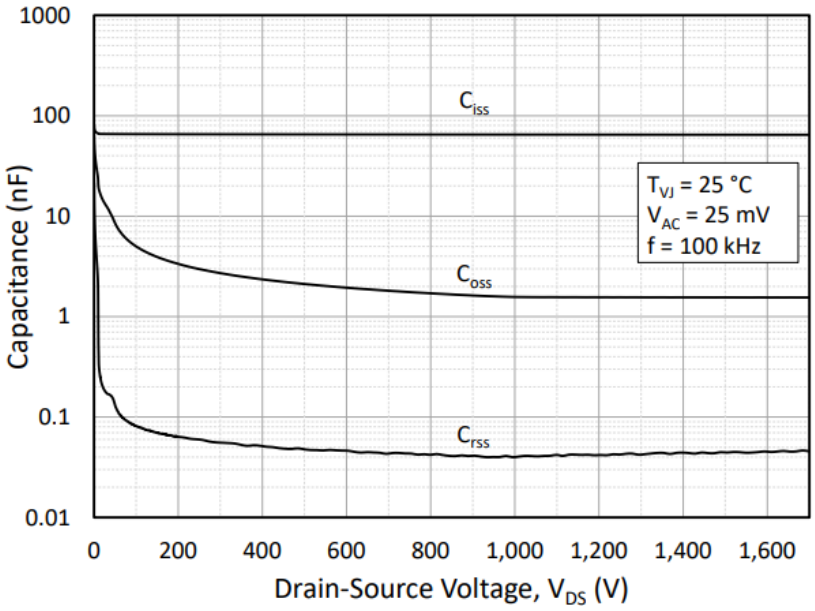
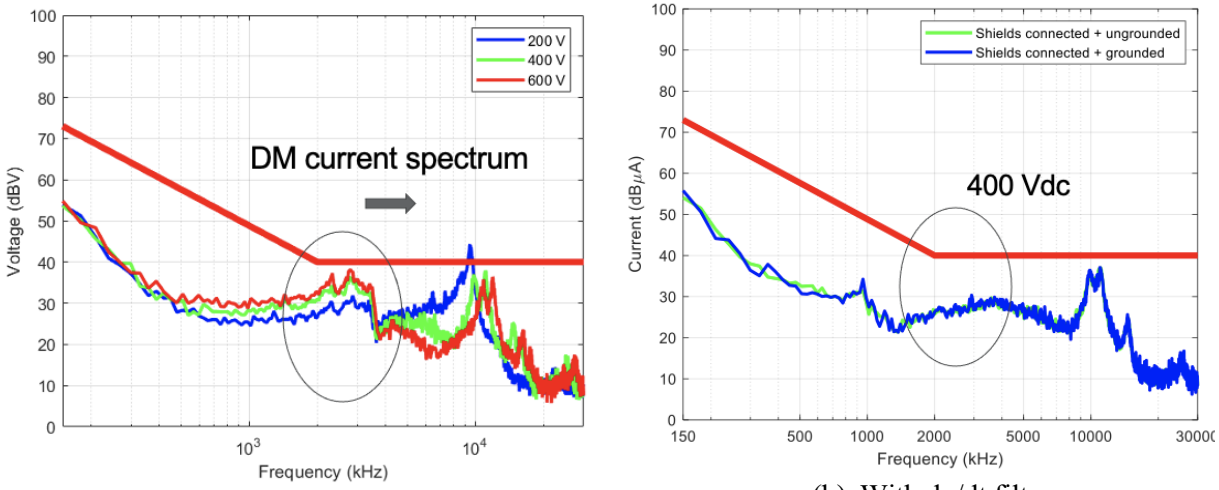


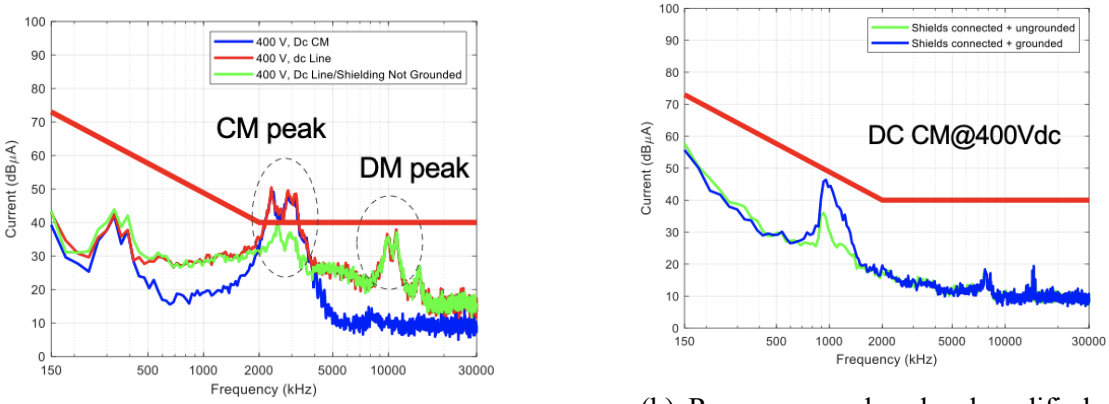
Fig. 3-37. *Voltage Dependence of Coss of the Power Devices*

The second behavior on the DM noises is in the 2-3 MHz range, at the reflection voltage ringing frequency due to the transmission line effect. The addition of the dv/dt filter helps as shown in Fig. 3-38. After dv/dt filter insertion, the DC DM noise at 2-3 MHz is fully damps with a small peak shifted to around 956 kHz. The grounding of shield has no impact on DM as expected since its impact is on the CM path, as shown in Fig. 3-39.



(a) No dv/dt filter (b) With dv/dt filter

Fig. 3-38. *Mitigation of the DM Resonance Spike by dv/dt Filter*



(a) Resonances seen without dV/dt filter

(b) Resonances reduced and modified with dV/dt filter

Fig. 3-39. *CM current Spectrum without (Left) and with (Right) dV/dt Filter*

A major challenge is the noise pattern in CM path. As shown in Fig. 3-40, a strong resonance spike exists in the common-mode (CM) noise around 1-3MHz range. This issue is evaluated with a variety of grounding and shielding arrangements (with details in the ninth quarter report), as listed in Table 3-2.

It is found that most of the CM currents that are primarily present in the lower frequency range are actively circulating in a dual 3-phase system due to the 60-degree phase displacement, and the 180-degree carrier shifted PWM modulation scheme. The resonance that results in a three-phase or six-phase system can cause this as well. Moreover, the asymmetry between the two sets of three-phase sources and the impedances to ground can also produce the undesired CM noise.

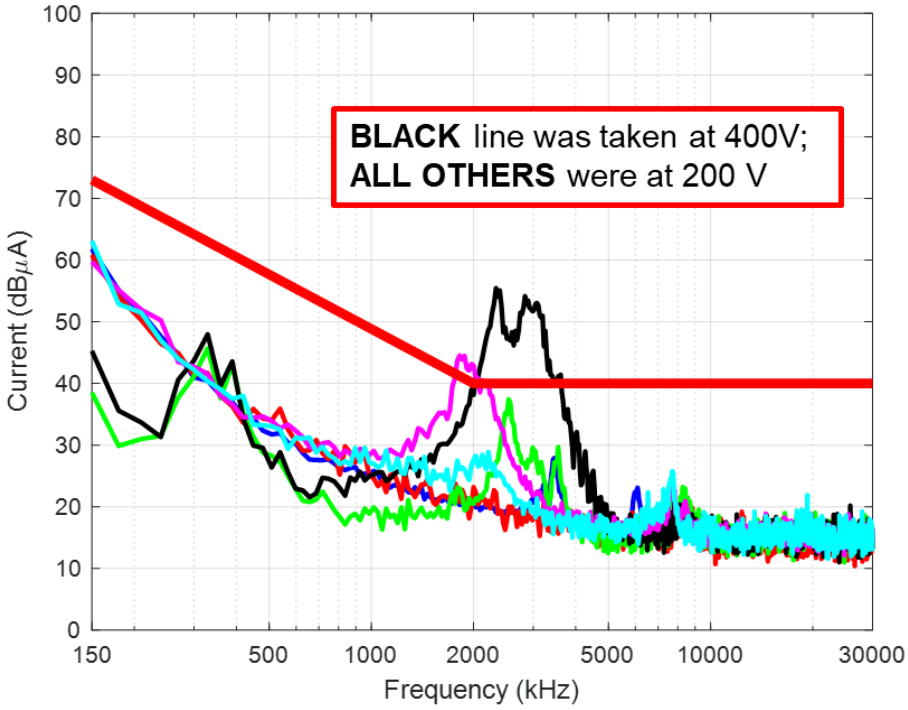


Fig. 3-40. *CM Current Results Taken under Various Laboratory Conditions*

Table 3-2. *Configuration of the System during the CM Noise Test*

	Blue	Red	Green	Black	Magenta	Cyan
Shielding shorted	N	N	Y	Y	Y	Y
Shielding grounded	N	N	N	Y	Y	Y
dv/dt filter	N	Y	N	N	Y	Y
dv/dt filter grounded	N	N	N	N	N	Y

The shielding scheme employed can also have a significant impact on the common-mode (CM) noise. Grounding the shielding of a cable creates an additional CM loop, which can lead to LC resonance within that loop. The use of a dv/dt filter helps attenuate the differential mode (DM) ringing and shifts the CM resonance towards the lower frequency range due to the insertion of an equivalent CM inductance. However, this ringing also contributes to CM noise current. By grounding the dv/dt filter, damping within the CM loop can be achieved due to the grounded RC branch. Nonetheless, this approach results in higher power loss in the filter resistors. Alternatively, incorporating a CM choke on the AC side between the cable and the load proves to be a better solution, since it takes the advantage of the strong resistive impedance at 100s kHz ~ MHz range of the CM choke to dampen the AC resonance, introduced by the cable and all components on the CM path, without generating high resistive power loss due to damping resistors.

Two options to implement the CM suppress CM noise for a six-phase system are explored, as shown in blue and red in Fig. 3-41: 1) the first is to place a choke around all six phases, which has a weak damping effect on the internal 3-phase current flow, as this only slightly impacts the 6-phase CM current depending on the ground path impedance ratio and does not prevent CM current between the two sets of phases; 2) another option is to place two 3-phase CM chokes to enable strong damping effect on each of the internal 3-phase CM current flows. The residual difference, the final 6-phase CM can be significantly reduced.

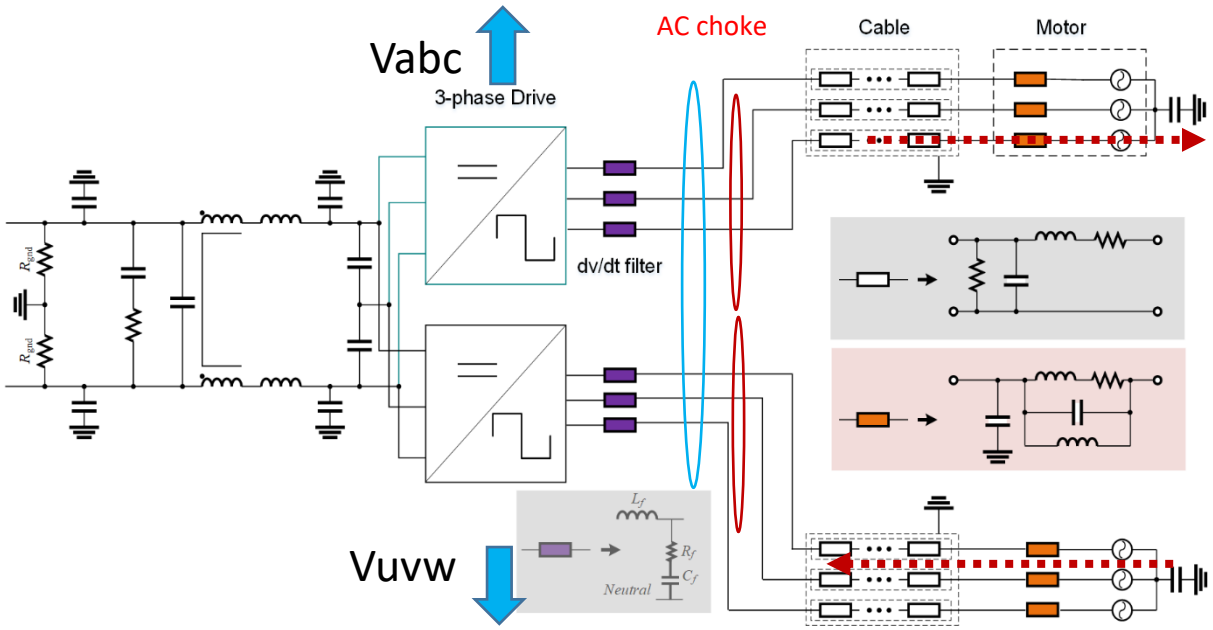
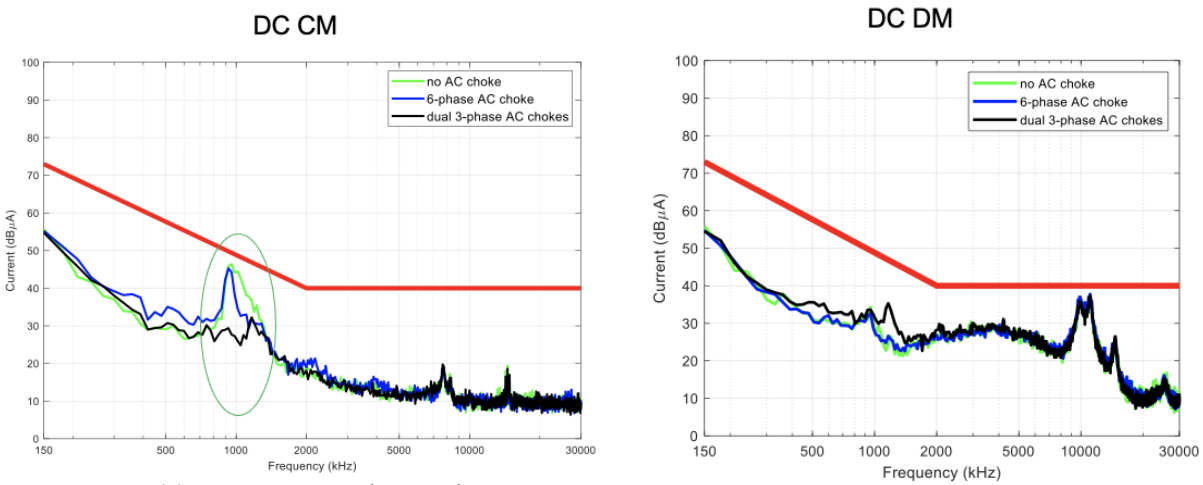


Fig. 3-41. *Two Options for Adding AC Chokes*

To verify the damping scheme, tests were performed with the commercial-off-the-shelf (COTS) AC side CM damping choke at 1 kV for the 7 m cable system. In comparison, for a single 6-phase CM choke, almost no damping effect is found for the total CM current. On the other hand, the dual 3-phase CM choke approach is much more effective for damping the resonance for both the AC side and DC side CM noises. There is only slightly higher DM noise at the 1.16 MHz with dual 3-phase CM AC choke due to an imbalance of dual 3-phase circulating current (see Fig. 3-42).



(a) Common Mode Results (b) Differential Mode Results

Fig. 3-42. *CM and DM Results Comparison between 6-Phase and 3-Phase AC Damping CM Chokes*

Two COTS core options were used as the initial testing (VAC W630 core and the VAC W468 core). Due to higher inductance and smaller size, W468 was chosen as the final core for testing. Concerning the potential impact of low saturation current rating on the core performance, DC saturation current is measured using the proposed method shown below (see Fig. 3-43, 3-44, and 3-45).

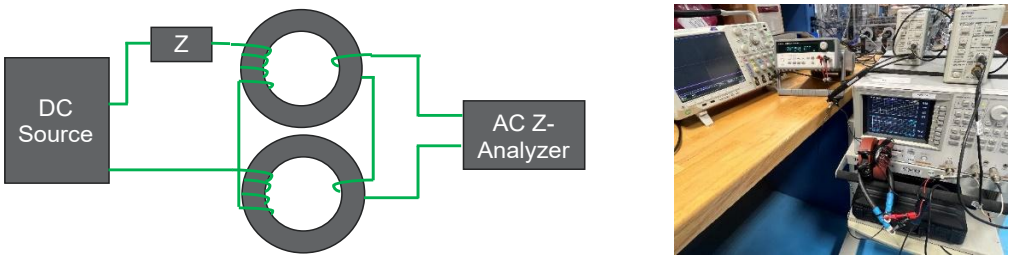


Fig. 3-43. *DC Injection Setup with Dual-Toroidal Cores and Reversed e-Connection to Cancel Induced Voltages on DC Coil Schematic (Left) and Photo (Right)*

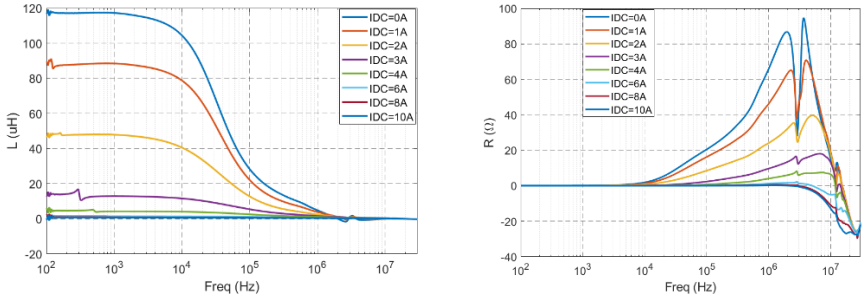


Fig. 3-44. *Measured Inductance and Resistance for the W468 Core*

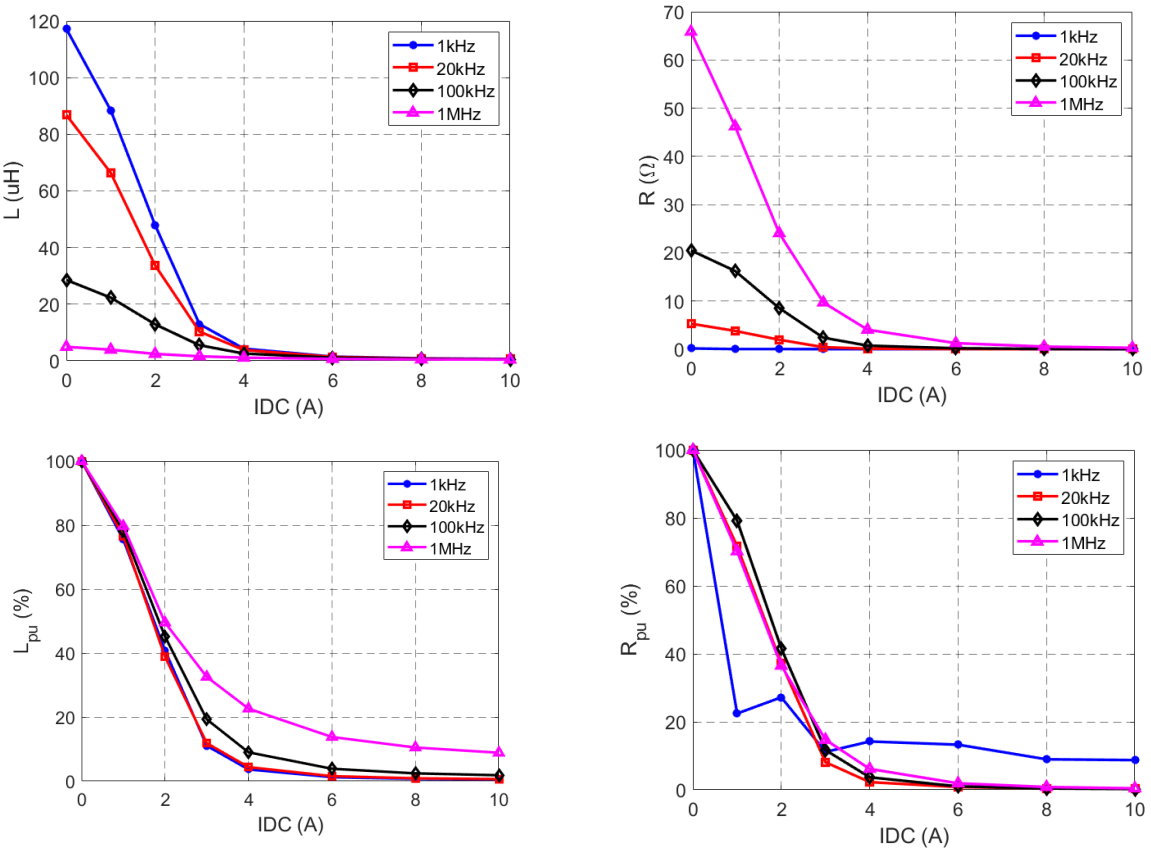


Fig. 3-45. *Measured Resistance and Inductance of the W468 Core at Multiple Frequencies*

With the W468 cores (choke 2), the original common mode peaks at 7.6MHz and 14.5MHz are diminished and the DM noise at 1.16 MHz is reduced. The overall performance of the system is further improved, as it addresses both the AC side common mode noise and the DC side common mode noise occurring within the MHz range, specifically at frequencies of 7.6 MHz and 14.5 MHz. These advancements contribute to a more reliable and efficient operation of the dual 3-phase drive system (see Fig. 3-46).

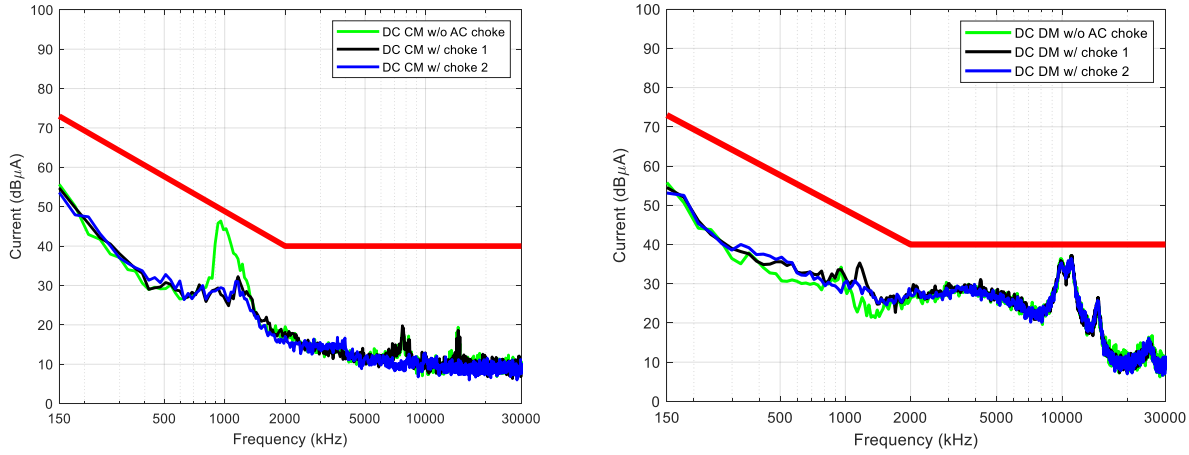
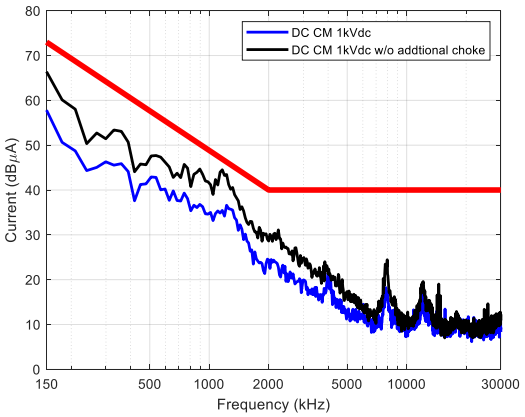
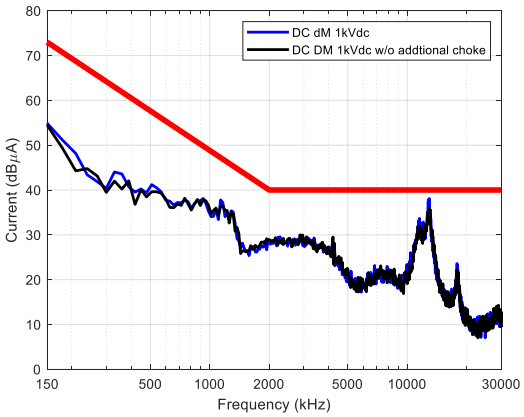


Fig. 3-46. *DC EMI Noise with Dual Three-Phase AC CM Chokes, Choke 1 = W630, Choke 2 = W468*

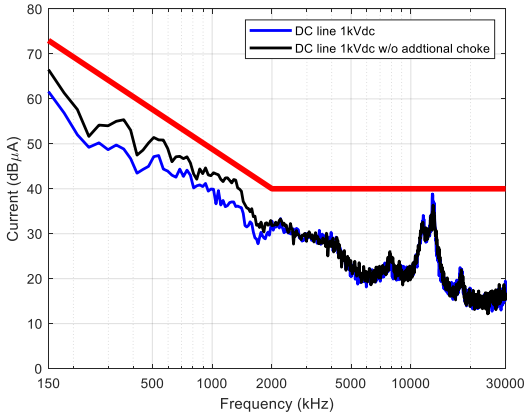
The experimental results at 1 kV (DC) nominal bus voltage, as in Fig. 3-47, further confirms the excellent performance of the damping AC CM choke. Note that all previous results included an extra DC CM choke, which was installed on the external busbar of the inverter for debugging purposes. This additional choke was removed to confirm that adding the AC chokes alone together with the DC side EMI filter on the drive system to ensure that the EMI standards are met. Without the additional choke, the DC CM noise is 5-7dB higher in the low-frequency to medium-frequency range but still within the standard limit. For the DC DM, the additional DC CM choke does not affect the results substantially, but the HF peaks are slightly lower. As a result, the DC line is slightly higher in the low-frequency range and the peaks are slightly lower in the high-frequency range.



(a) DC CM



(b) DC DM



(c) DC Line

Fig. 3-47. *Performance Results with the AC Chokes with a 1kVdc Nominal Tests for CM (a), DC (b), and (c) DC Line with and without the additional DC CM Choke*

Given the positive results of the tests using the COTS filter, the following chokes in Table 3-3 are considered based on the tested EMI noise pattern and resonance peak distributions. Option B is finally chosen for the design, considering the inner diameter constraint to accommodate the three-phase motors cables. Further, its lower mass makes this choke a better candidate. With this information, the cores were then fabricated by NASA (Fig. 3-48). As shown in Fig. 3-49 compares the COTS cores, similar peak currents of 3-phase CM circulating current are observed (3.1A @1kV, M=0.1, light load) with the NASA-

GRC cores showing lower inductance than the COTS core due to more DC saturation margin (see Fig. 3-50). Note, the time-based waveforms of the same operating condition for the GRC cores are shown in Fig. 3-51 for additional context the presented EMI figures in this section. These cores are designed for higher reliability and robustness, and higher damping resistance due to NASA-GRC's customization capability on core resistance control towards the frequency range of interest, i.e., 100 OHM at 1MHz for GRC core vs. 50 OHM at 1MHz for COTS core. With the combination of inductance and resistance impedance behaviors, similar EMI noise reductions are achieved for both cores, except the slightly higher DM noise at lower frequency end due to the lower inductance of GRC cores.

Table 3-3. *Core Specifications*

RTX CM v2	**A**	**B**	**C**	**D**
μ_r	24000	24000	22500	21000
R_i (m)	0.0345	0.032	0.03	0.028
R_o (m)	0.047	0.0435	0.0417	0.0398
h (m)	0.0508	0.0508	0.0508	0.0508
s	0.8	0.8	0.8	0.8
m (kg)	1.015	0.865	0.835	0.797
I_{peak} (A)	6	6	6	6
B_{inner} (T)	0.83	0.90	0.90	0.90
L_{CM} (H)	6.03E-05	5.99E-05	6.02E-05	6.00E-05

Fig. 3-48. *GRC Fabricated AC CM Damping Choke*

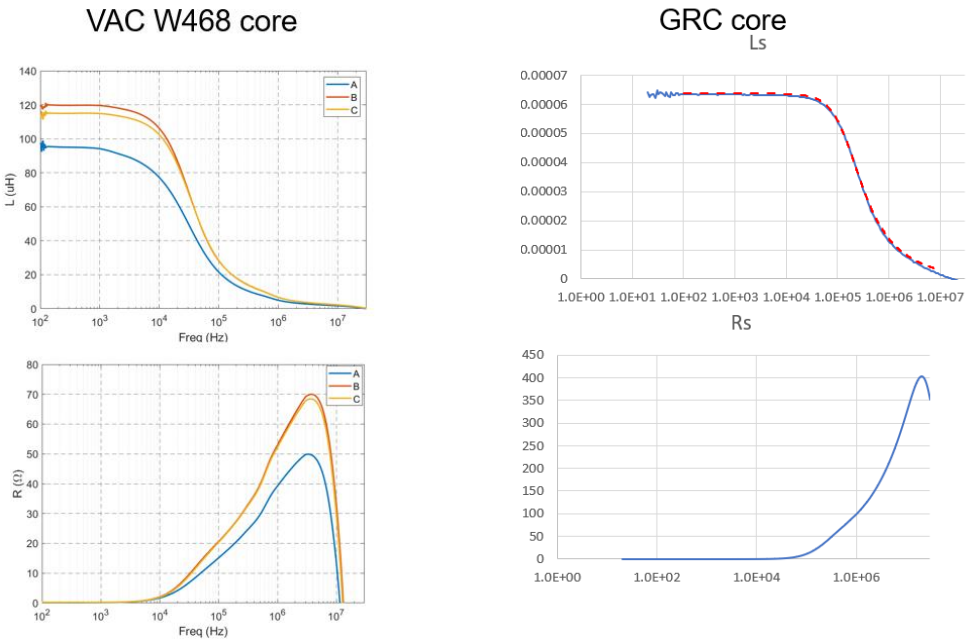
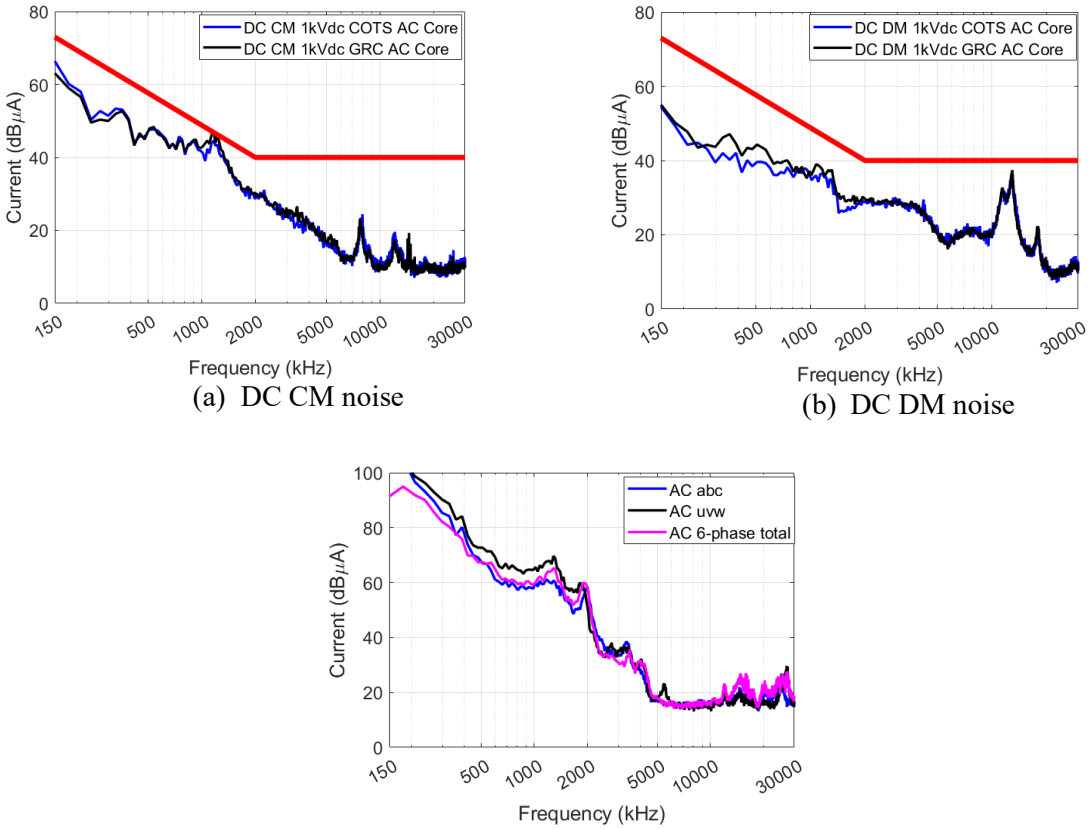


Fig. 3-49. *Impedance of COTS AC CM choke (Left) and GRC AC CM Choke (Right)*



(a) DC CM noise

(b) DC DM noise

(c) AC 6-phase CM noise

Fig. 3-50. *EMI Testing Results with GRC AC CM Choke*

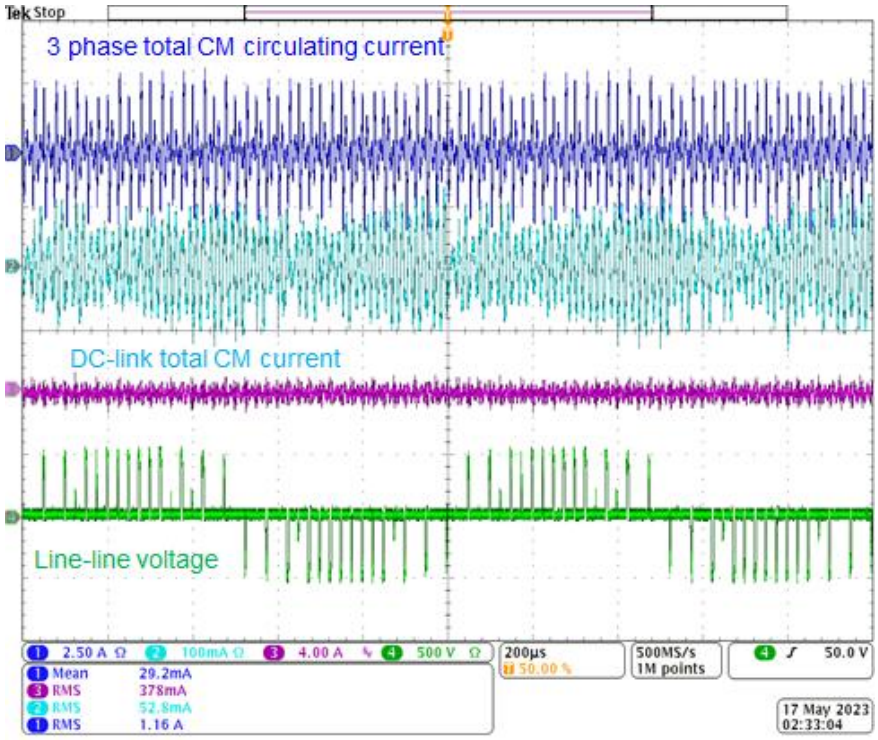


Fig. 3-51. *3-Phase Total CM Circulating Current, DC-Link CM Current, CM Inductor Current and the Line Voltage for the NASA-GRC Cores under 1 kV and M=0.1*

3.4.3. DC EMI Core Design

With the addition of AC CM choke that successfully dampens the EMI noise resonances and spikes, the existing DC EMI filter parameters of the motor drive used meets the target specification. Hence, these parameters were used for the NASA GRC core design. Note: although it is possible to design a smaller CM core for the similar inductance and power rating (and it was fabricated and delivered to RTRC), the inner window was constrained by the complicated DC busbar geometry. After several iterations across the two teams, the CM core was designed to follow the same inner diameter as the existing COTS core design with two split units for the sake of easier installation. Furthermore, the existing DM core is based on two C-cut cores, which is quite different from the gapless design process within GRC team. The geometry design of the gapless DM core would increase a lot of complexity considering its mounting onto the DC busbar of the MW motor drive. The two teams decide to go with the existing DM cores given the limited time and budget.

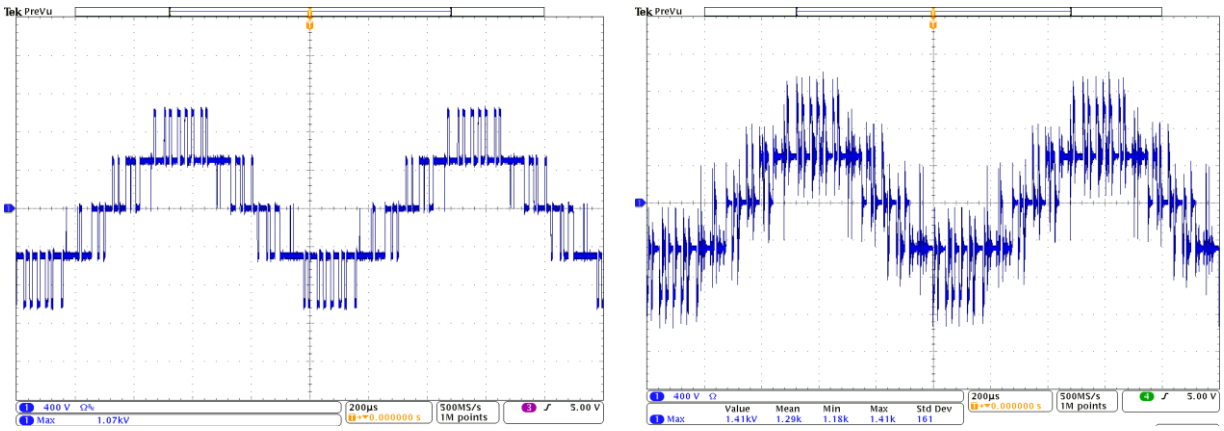
4. TESTING AND RESULTS

To verify the performance of the GRC core based dv/dt filter, the three-phase dv/dt filter is applied in a test rig with three-phase motor controller and 7 m cable system and compared with COTS core-based filter.

4.1. Overvoltage Mitigation and Damping in Motor Drive System

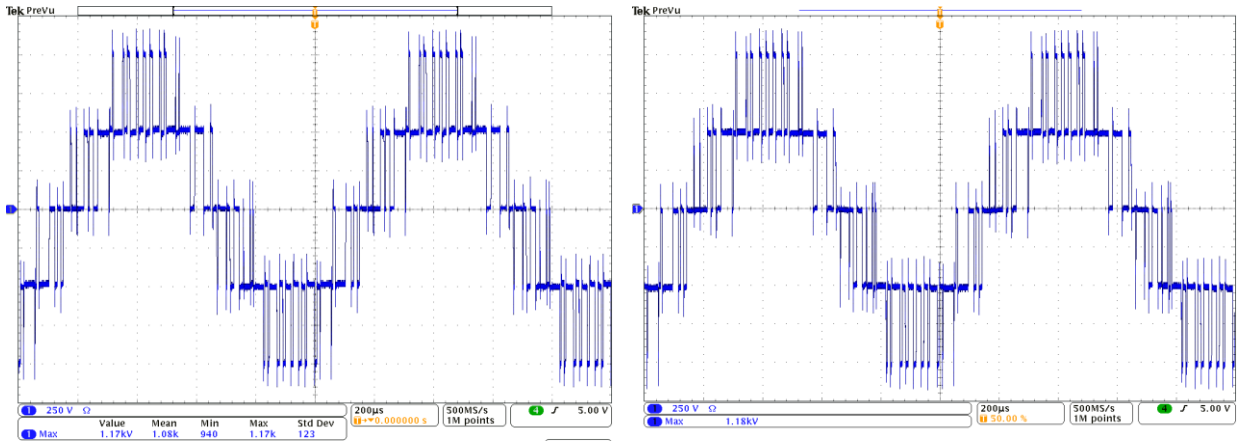
***Setup*:** The no load open circuit test, with the dv/dt filter conditioning the RTRC MW inverter PWM waveform output, measures the voltage at the far end of the power cables with the highest impedance mismatch between source and load, and hence, has the highest potential overvoltage due to the transmission line effect. A DC power supply is connected at the MW inverter DC link input where it is inverted to a PWM AC signal. The input terminal of the dv/dt filter is connected to the AC outputs of the inverter, where it conditions the dv/dt slope of PWM voltage output of MW motor controller. This output terminal is connected to a 7 m long three-phase power cable with the ends in open circuit.

Voltage attenuation results: *A* of comparison tests with and without the filter insertion were conducted under different DC bus voltages from 100 Vdc up to 1000 Vdc. Fig. 4-1 (a) and (b) illustrate the line-line voltage waveforms without the filter at the converter output and the cable far end at 1 kV dc. The maximum voltage at cable far end is 1.41 kV (0.41 kV overvoltage) with significant voltage ringing around 2 MHz. This will likely lead to high motor winding and cable power loss and voltage stresses, as well as high EMI noise. Fig. 4-2 (a) and (b) show the cable far end results with both the COTS core based and NASA SM core-based filters inserted. The filter effectiveness is clearly illustrated with both cores providing the same performance.



(a) Cable near end (converter side) (b) Cable far end

Fig. 4-1. *Cable Line-Line Voltage without the dv/dt Filter under No-Load Condition*



(a) with COTS core at far end (b) with NASA core at far end

Fig. 4-2. *Cable Far End Line-Line Voltage with the dv/dt Filter under No-Load Condition*

To enable a clear observation of filter voltage attenuation and dampening effect, the waveforms are plotted on the same graph. As observed in Fig 4-4, the designed filter effectively suppresses the voltage stress on the load side, and eliminates most of the high frequency ringing harmonics, which is very helpful for reduction of high frequency motor power loss and bearing currents, as well as being important for the mitigation of conducted and radiated EMI emission along the cable.

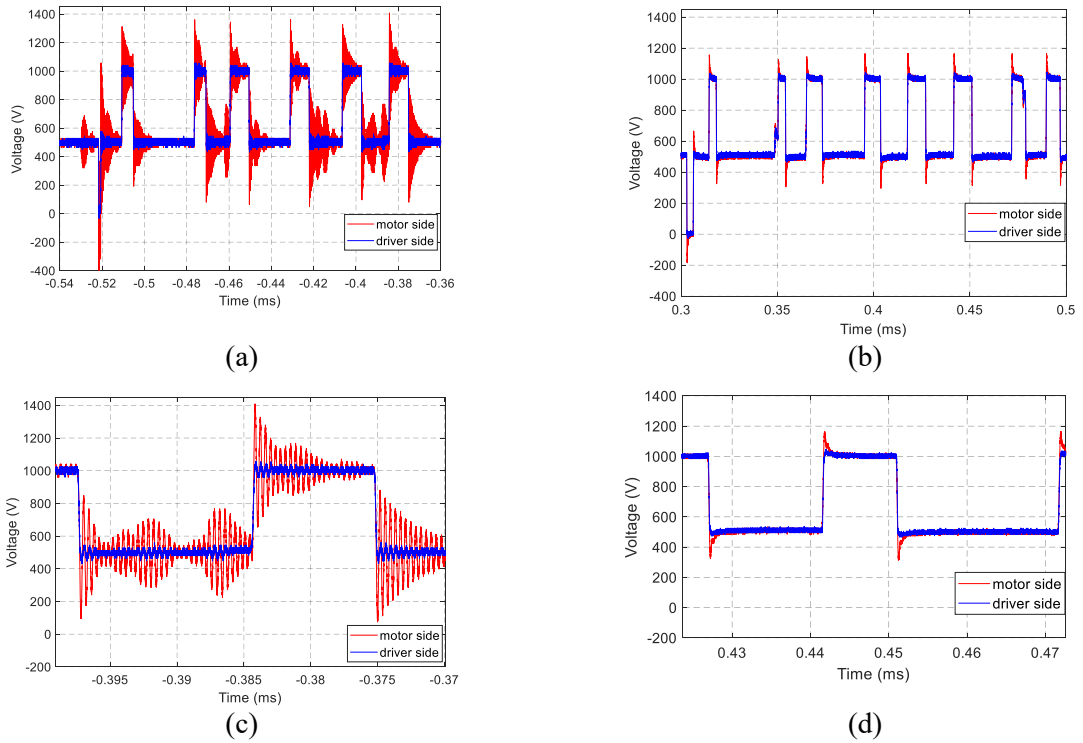


Fig. 4-3. *Comparison of Reflection Voltages on Cable Far End (Motor Side) and Converter Side before and after adding the dv/dt Filter. (a) Before adding Filter; (b) After adding Filter; (c) Zoomed-in of (a); (d) Zoomed-in Waveforms of (b).*

4.2. High Power High Current Recirculation Test and Core Loss Estimation

4.2.1. Necessity of High Current Testing

Power loss measurement challenge: even with the most state-of-the-art measurement instruments, the power losses measurement results contained large potential discrepancy from estimate due to the low power loss at partial rating. Note: the core power loss is calculated by averaging its instantaneous power over one line cycle. Based on loss modeling and feedback from the NASA team, a sensing coil (read coil) technique is implemented to measure the core voltage. A 10-turn read coil is implemented on one of the dv/dt inductor cores for voltage measurement, and current is measured with high bandwidth current probe. Both the voltage and current are captured with an oscilloscope. Fig. 4-4 shows a sample oscilloscope measurement result at 31 Arms AC current. However, with 20 MB points at sample rate 1.25 GS/s and the oscilloscope channel tuned to maximize the waveforms on screen, the losses for both COTS and GRC cores are measured with less than 1 W. However, under these oscilloscope settings, the accuracy is not guaranteed due to impact of the probe accuracy, ADC sampling error of the oscilloscope, and potential voltage/current misalignment. To be able to fully characterize the core losses and compare the performance of the different core options, high power tests are necessary since the base loss would be dominant over the inevitable errors at high current high-power conditions and RTRC achieves that through recirculating current tests.

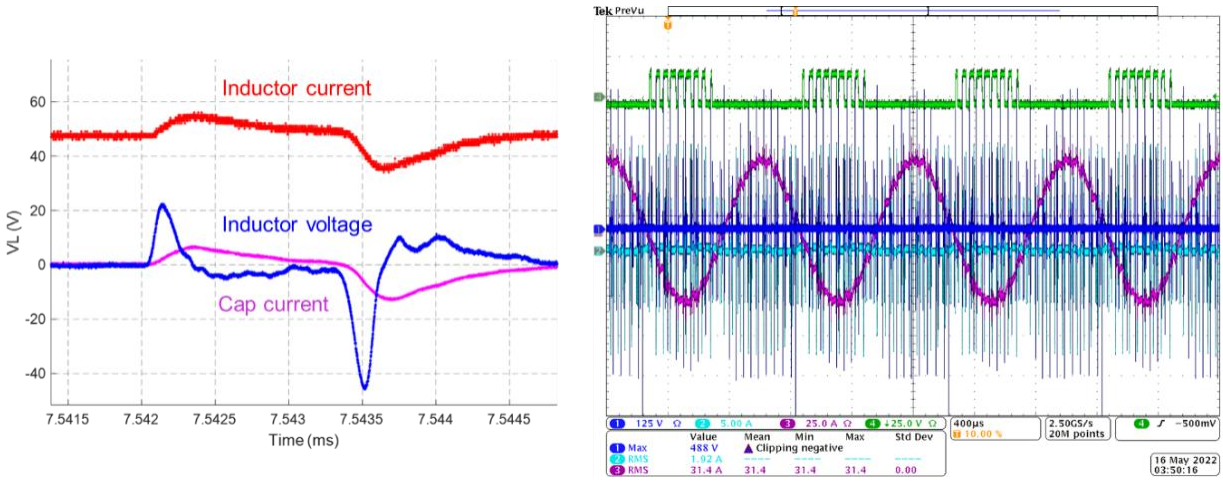


Fig. 4-4. *Sample Loss Measurement Output*

Observation of eddy current loss introduced by gap core: one of the major advantages of GRC dv/dt core is the gapless core structure, which avoids the air gap induced fringe effect and leakage flux around the gap area in the COTS gaped amorphous core. Through the analysis carried out by NASA team, the stray flux around the air gap will induce eddy currents and attract the conducted current towards the air gap region around the center of the busbar. The bus-bar utilization in the face of a fringing field depends on the frequency and bus bar properties, but one way to characterize this effective change in resistance is through temperature measurement on the busbar itself. However, with very low current level, the harmonics is not enough to drive this effect and evident temperature rise or difference (see Fig. 4-5).

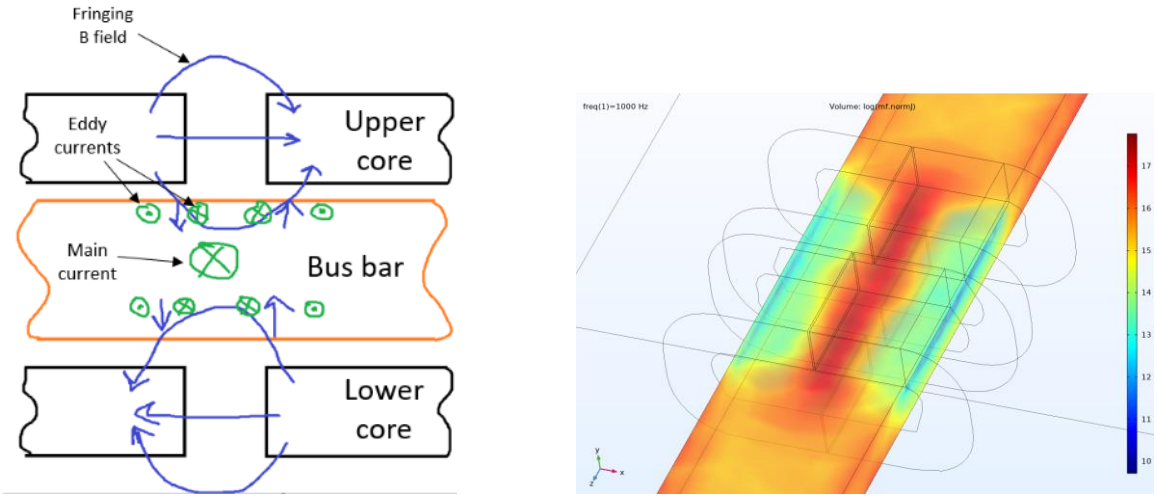


Fig. 4-5. *Cartoon Illustrating Fields and Currents (Left) and FEA Simulation Showing Current Concentration in Busbar (Right)*

4.2.2. High Current High Power Recirculation Testing

To enable high power high current test, the simplest method is to form a recirculation test rig where two motor drives are connected on the DC side sharing a common DC bus and interconnect on the AC side through interface inductors. In this way, the DC power supply only needs to provide high voltage bus level with power to cover the power losses of the converters, and the converters can generate the desired high AC voltage and current inside the loop (see Fig. 4-6). For this type of system, one simple control is to apply the phase shift control treating the two converters as two voltage sources, where their magnitudes and phasor difference create the current flow and active/reactive power transference (power angle based control method used for recirculation test, Fig. 4-7).

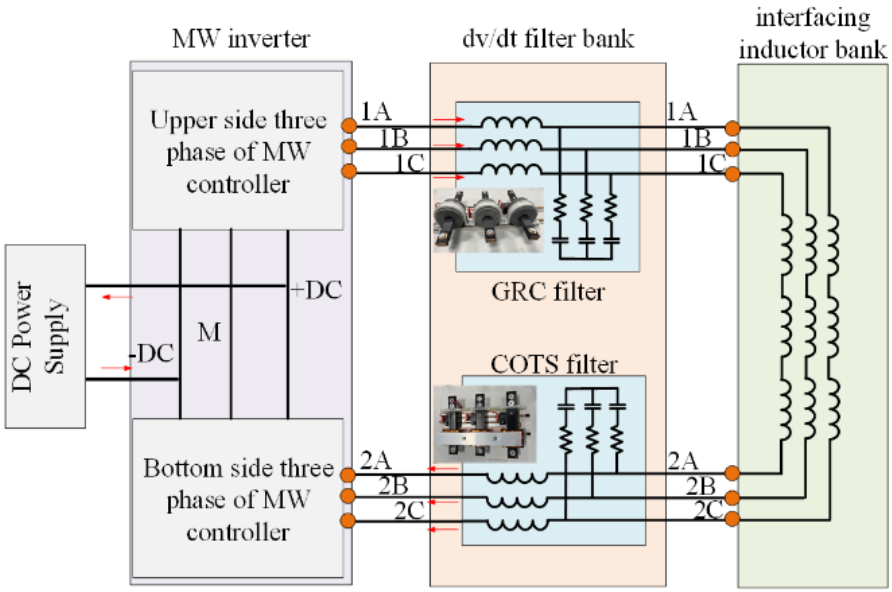


Fig. 4-6. *Schematic of Recirculation Test Setup*

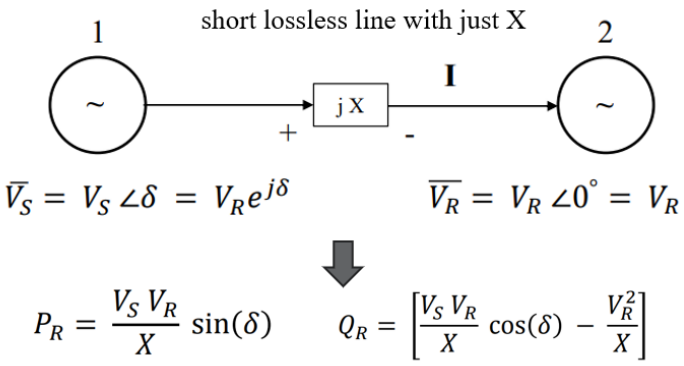


Fig. 4-7. *Power Angle Based Control Method*

A dedicated test rig is built for the above system, as shown in Fig 4-8, with a series of preparation tests conducted to ensure the sensing, protection, control firmware and software are correct and ready before the power test. To enable fair comparison between the COTS core and GRC cores, the two filters are also installed in the test rig and mounted in a cabinet, allowing to measure the same current flow simultaneously.

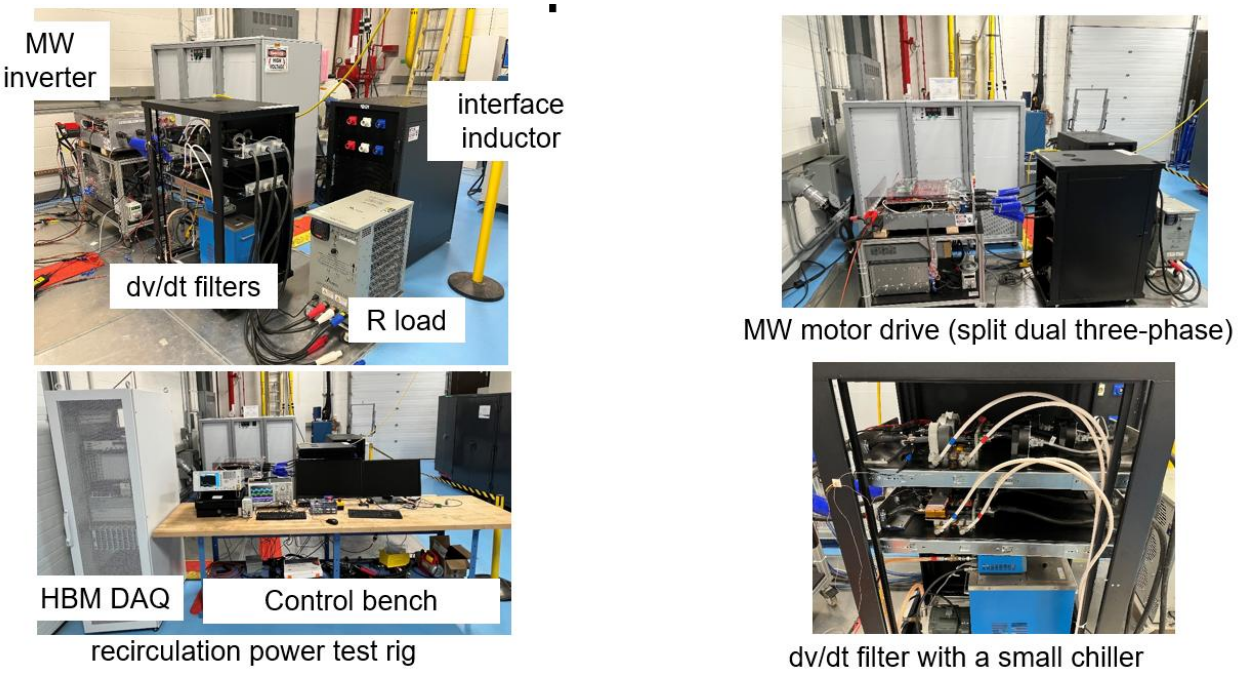


Fig. 4-8. *Photos of Recirculation Test Setup*

To ensure the proper control, a simulation model is also developed using the same modulation scheme and measured cable and filter impedances. As verified in Fig. 4-9 and 4-10, the simulated current rms value matches the calculated value based on the control principle (see Fig. 4-7).

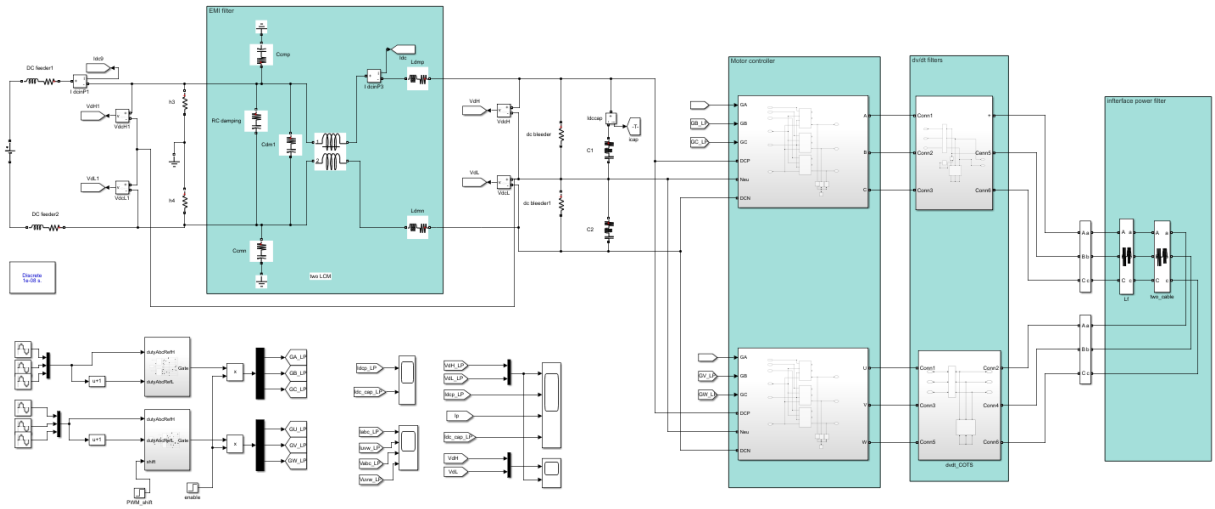


Fig. 4-9. *Simulation Model of the Recirculation Test Setup*

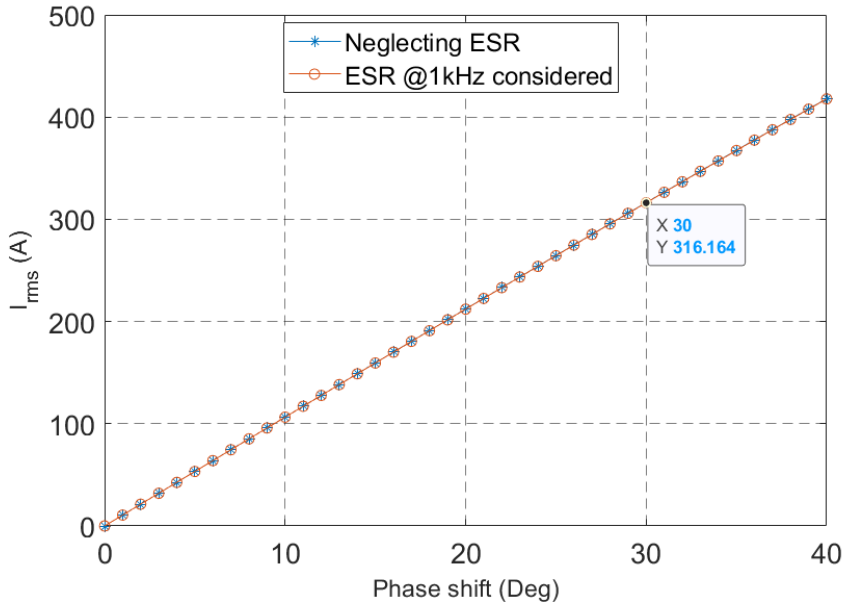


Fig. 4-10. *Calculated Current vs. Phase Shift Command*

In general, for the three-level T-type motor drive, low modulation index (M) leads to unbalanced thermal stress within power modules per phase leg of T-type converter. Hence, higher M is preferred for the test. In the test, Vdc voltage, M and phase shift are all adjusted accordingly based on the testing need. However, the AC current is only tested up to 313Arms~320Arms around due to two limits on existing hardware: 1) thermal stress on the front panel of power inductor cabinet (due to eddy current loss); 2) mis-triggering issue of desaturation protection on the gate driver board of motor controller above 320Arms current (a workaround solution is known but could not be implemented prior to the end of the project).

To capture the thermal stress and eddy current effects in the COTS dv/dt core, a comparative test study is conducted. Eight thermal couplers are installed on the two sets of dv/dt filters as shown in Fig. 4-11 and Fig. 4-12 below.

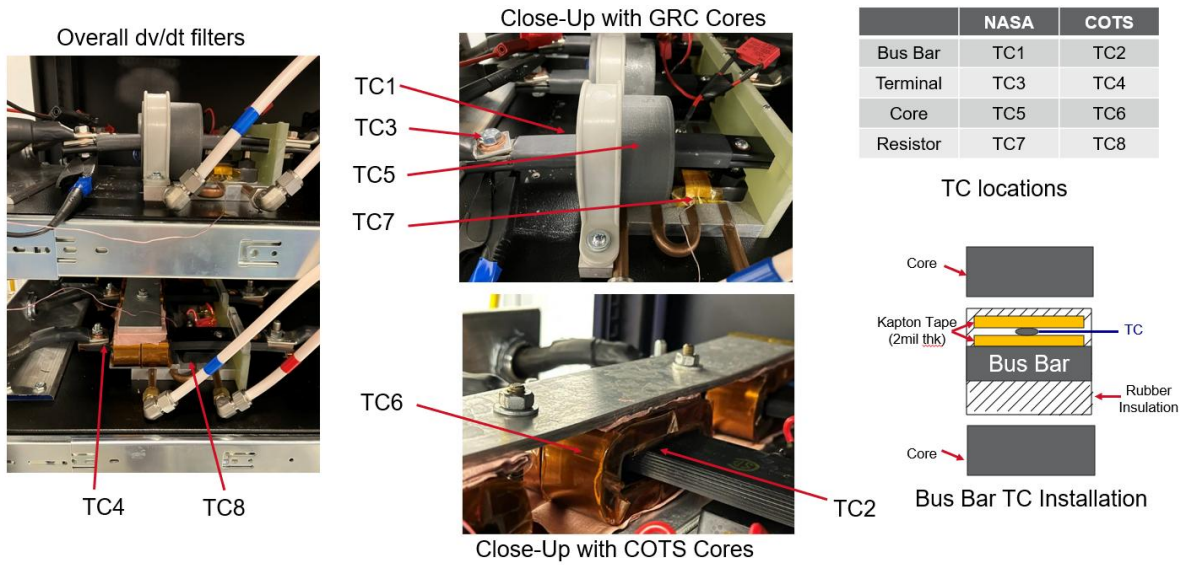


Fig. 4-11. *TC Mounting for Thermal Stress Comparison between GRC and COTS Cores*

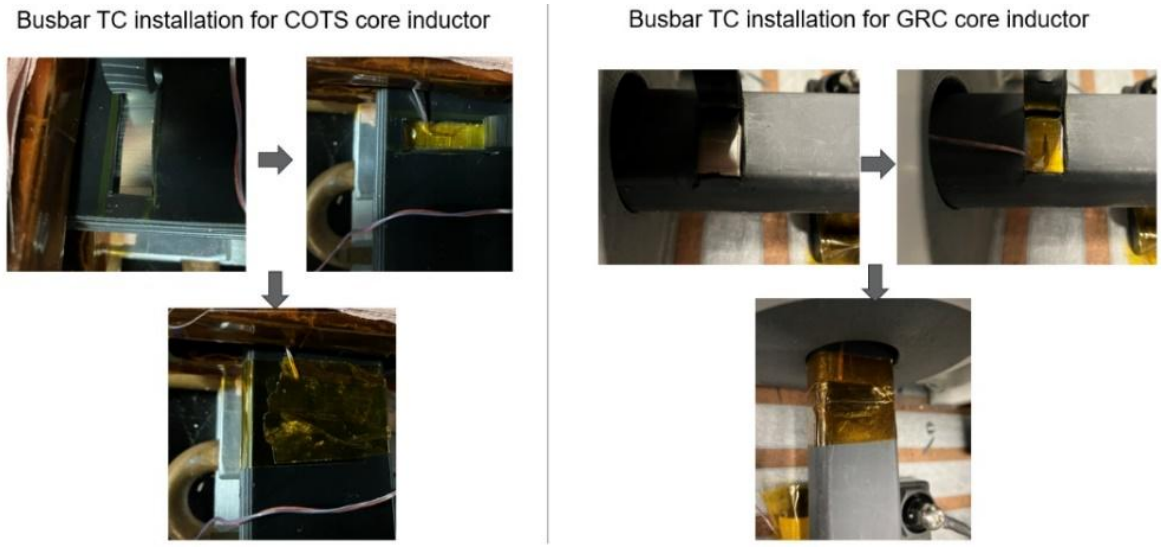


Fig. 4-12. *TC Mounting Procedure and Method for Busbar Temperature around Center of COTS Gap Core (GRC Core is used as Reference Point)*

Further, long duration tests of 30 minutes in length are conducted at two sampled conditions under 850Vdc to evaluate the thermal stress and behaviors under different current levels, as provided in Fig. 4-13 and Fig. 4-14.

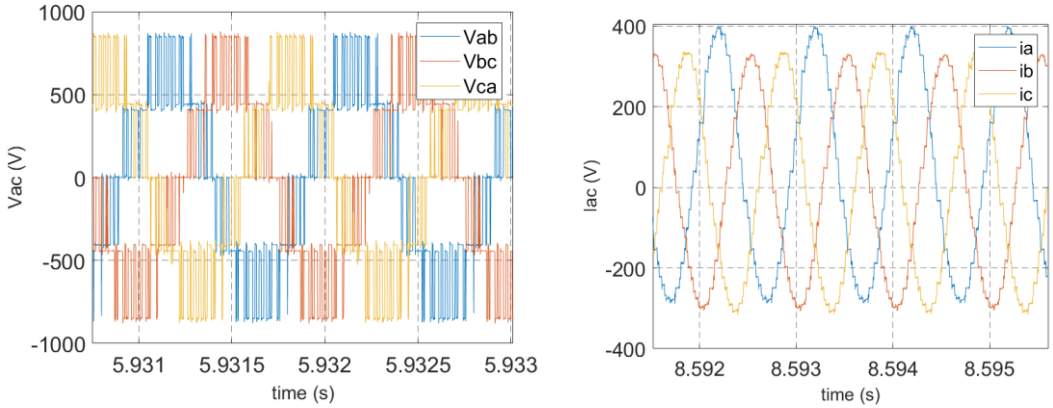


Fig. 4-13. *AC Output Voltage (Left) and Current (Right) at M=0.85, VDC=850V, Irms=223A, and Phase Shift 23 Degrees*

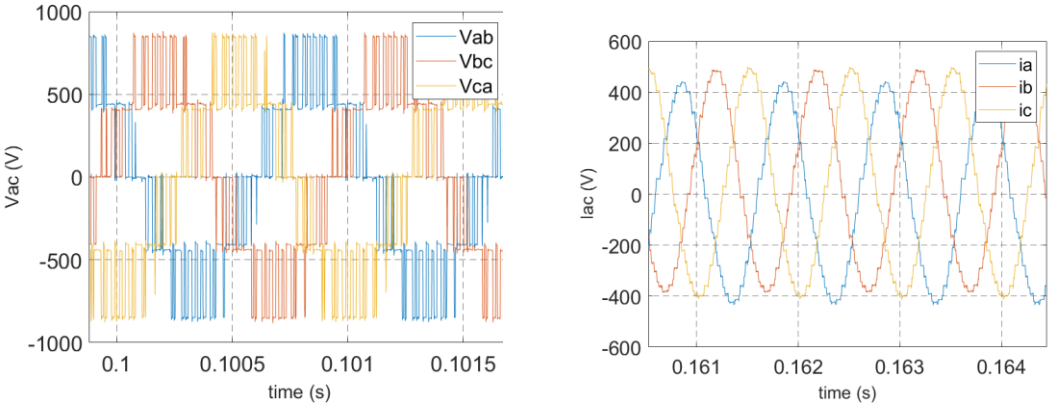


Fig. 4-14. *AC Output Voltage (Left) and Current (Right) at M=0.85, VDC=850V, Irms=313A, and Phase Shift 30 Degrees*

Temperature monitoring results: The thermal monitoring results for the above two tests are presented in Fig. 4-15 with IR images (see Fig. 4-16). One major observation is that the busbar center beneath the gap of the COTS core shows lower temperature than its terminal in Fig. 3-16 results. This may be because the thermocouple is off center, or the actual bus bar configuration is different from the model. Since the clamping bar on the three-phase COTS cores was removed after Fig. 3-15 test to obtain a better IR camera image, it may further introduce core position shift and this possible misalignment can lead to the TC being in an underutilized section of the conductor, and explain the phenomenon.

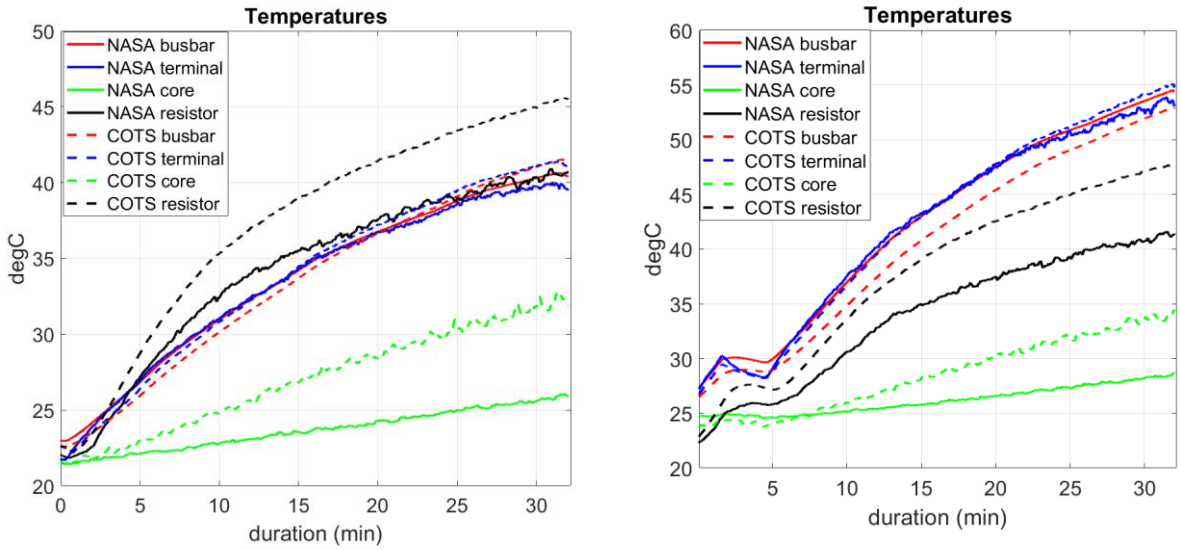


Fig. 4-15. *TC readings at M=0.85, VDC=850V, Irms = 223A, Phase Shift 23 Degree (Left), and M=0.85, VDC=850V, Irms = 313A, Phase Shift 30 Degree (Right)*

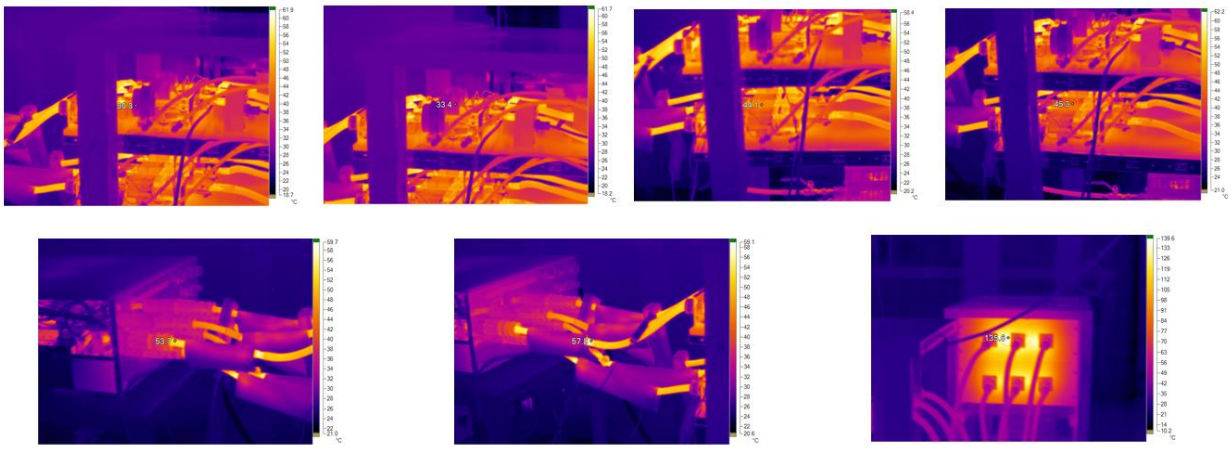


Fig. 4-16. *IR Camera Images at M=0.85, VDC=850V, Irms = 313A, Phase Shift 30 Degree*

On the other hand, as expected, the NASA-GRC cores have a busbar and terminal which show similar temperatures, since there is no gap core induced eddy loss effect. It is also noted that the GRC core temperature is lower and there a difference in the resistor temperatures (COTS vs GRC). This could be related to the stronger voltage ringing on the COTS core-based filter (more ringing current will flow to the RC branch), as seen from Fig. 4-17. Note that there is around 3ft interface cable each phase between converter and dv/dt filter busbar where voltage before filter is probed. With the impedance interaction, overall, GRC core inductor shows slightly stronger effects of overshoot voltage mitigation and ringing dampening at switching transitions.

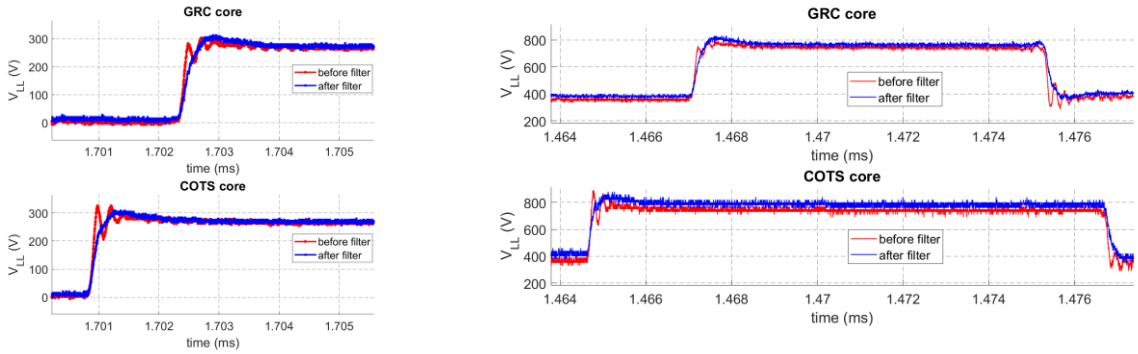


Fig. 4-17. *Line-Line Volage Before (Top) and After (Bottom) dv/dt Filters 500Vdc, Phase Shift =31deg, M=0.5, 102Arms (Left), and dv/dt filters 750Vdc, Phase Shift =30deg, M=0.85, 280Arms (Right)*

Furthermore, note that the rubber isolation layer of the connector in the main inductor cabinet is rated around 120 °C while the steel made front panel around the connectors rose to 136 °C within the duration of the test due to the eddy current effects around the main power cables and a further test at longer duration was not conducted.

Core loss measurement: Based on prior lessons learned, the core loss measurement and calculations are very sensitive to a lot of factors. Even at the high current testing conditions, the best practices are followed as below:

- A 10-turn read coil on one phase inductor is used to measure the voltage.
- A current probe is measuring current flow through the core.
- Core power loss is calculated by averaging the instantaneous power over one line cycle offline, using the saved waveforms from oscilloscope.
- In addition, several approaches that can help improve the method accuracy are explored and utilized:
    - Maximum bandwidth of voltage and current probes are used (Voltage probe: 300 MHz; Current probe: 2MHz for 500Arms max)
    - Maximize the vertical stretch on Oscilloscope for V/I waveforms.
    - Two types of 500 Arms current probes are tried and compared.
    - Hi-Res mode is finally adopted to realized higher sampling accuracy (11-bit ADC vs 8-bit)
    - V/I alignment is very critical and sensitive for results, which is adjusted based on transients' alignment between voltage and current waveforms.

Due to the limited bandwidth of current probe, current ripples are smoother than the voltage waveform and the voltage/current are required to be better aligned by approximately 80ns based on a combination of the simulation and observation. With that compensation value, the core losses are calculated in Figs. 4-18 under Vdc=850V, phase shift = 30 deg. From these results, the GRC core shows much lower loss compared to 2 cascaded AMCC-32 COTS cores. However, given the potential errors in the measurement, better understanding on the trend of the loss difference is still needed.

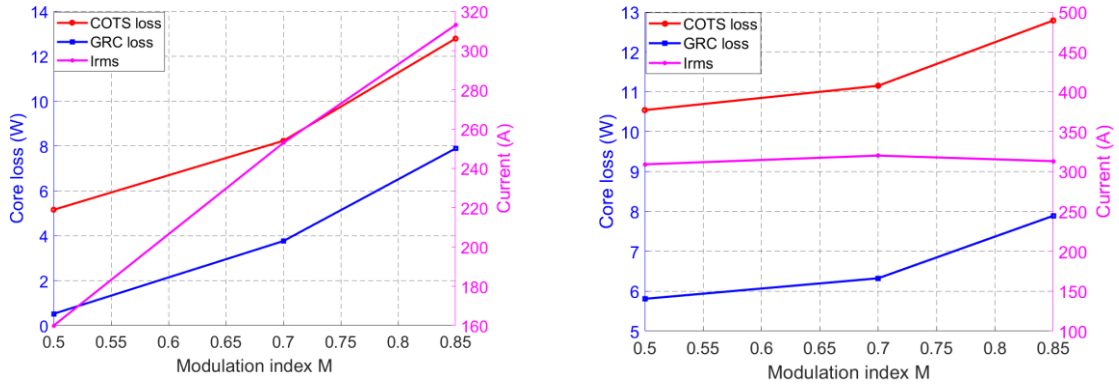


Fig. 4-18. *Core Loss Increases with Current (major factor) and M (Left), Phase Shift Adjusted for Similar Irms current level for Different M Cases (Right)*

To further verify the results, the above result for the COTS core is further compared with estimation method using GSE based on the measured line current, and the literature reported Steinmetz parameters [3-4]. Note that only 600 kHz below current contents are utilized for the loss calculation to avoid unrealistic errors at very high frequency since the Steinmetz parameters is only valid in a limited frequency range (see Fig. 4-19).

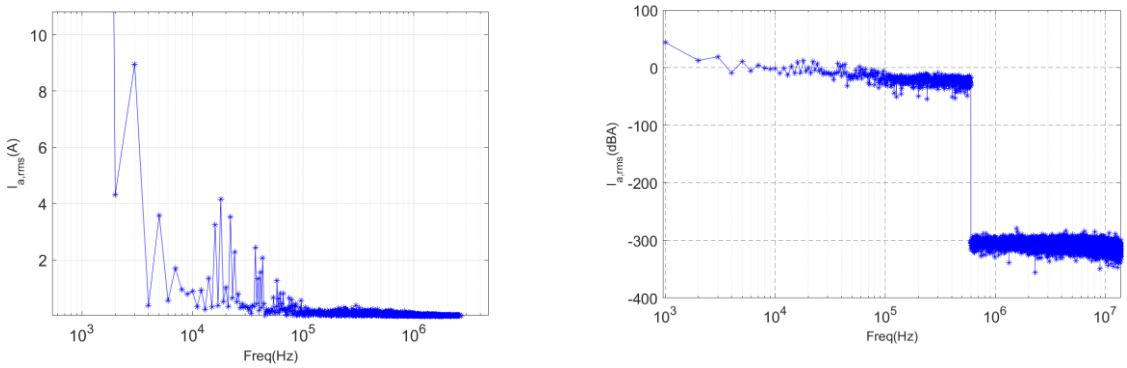


Fig. 4-19. *AC Current FFT (Left), and AC Current FET with 600 kHz (Right)*

From the results in Fig. 4-20, the approximate values of two different approaches are close, although there are still obvious errors. The key factors are: 1) measured method has V/I alignment errors, probe errors, and ADC sampling errors; 3) the GSE method itself being inaccurate – giving a rough estimation with the Steinmetz parameters valid only in the limited frequency range. At very high frequency range, high errors could be induced if the parameters are extracted from relatively lower frequency which is the current case for the parameters taken from literature.

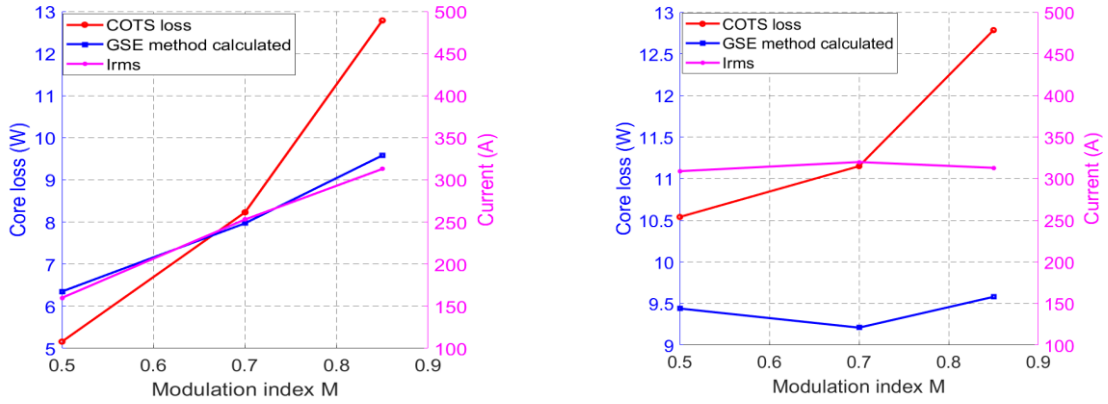
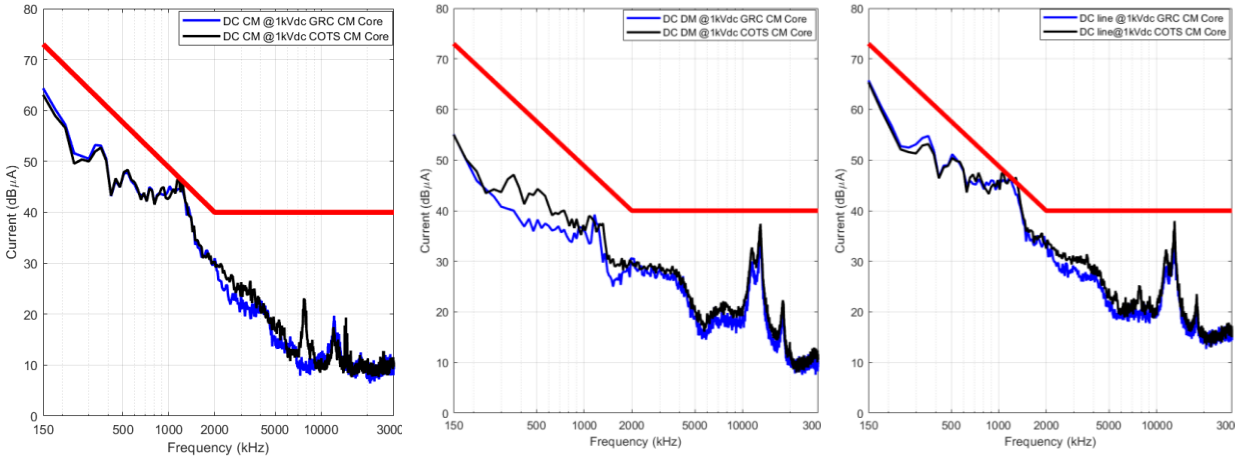


Fig. 4-20. *Core Losses between V/I Measurement and GSE Calculation with Increasing Current (Left), and as Current is Maintained (Right)*

From the results in Fig. 3-23 and Fig. 3-24, the approximate values of two different approaches are close, although there are still obvious errors. The key factors are: 1) measured method has V/I alignment errors, probe errors, and ADC sampling errors; 3) the GSE method itself being inaccurate – giving a rough estimation with the Steinmetz parameters valid only in the limited frequency range. At very high frequency range, high errors could be induced if the parameters are extracted from relatively lower frequency which is the current case for the parameters taken from literature.

4.3. EMI Performance Testing

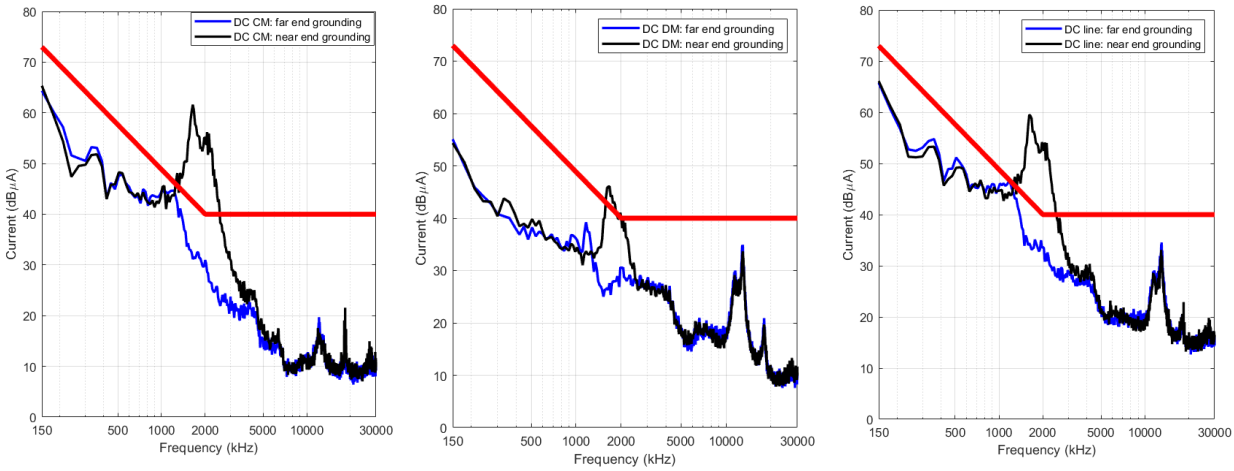
The newly designed GRC DC CM cores are installed in the MW motor controller and tested in the same test rig previously used for COTS core testing. As seen from Fig. 4-21, the GRC cores show overall better line EMI attenuation from 2 MHz to 10 MHz, where CM noise is dominant below 5 MHz and DM noise is dominant above 5MHz. Specifically, the GRC cores provide stronger CM noise attenuation from 2 MHz to 10 MHz. With the GRC cores, the DM noise also gets lower from 250 kHz to 10 MHz even the DM cores are still the same COTS cores. One of the possible reasons is that the GRC CM cores may provide a bit higher leakage inductance, which helps the DM noise reduction. One other possible cause is the slightly different inductance that may be introduced by the reassembly process of the DM core and busbar.



(a) DC CM noise comparison (b) DC DM noise comparison (c) DC line noise comparison

Fig. 4-21. *Comparison of DC Noise with GRC and COTS Core Based CM Inductor*

The impact of the cable shield grounding location on conducted EMI is also investigated in this motor drive system (see Fig. 4-22). The EMI noise of the system when 6-phase cable shields are shorted and grounded at near-end and rear-end of the cables, respectively, are tested. The far-end grounding, which is also the previous arrangement, is found inducing much lower noise current than the near-end grounding option. In the latter case, both CM and DM noise spectra show a high noise spike around 1.6MHz, due to the LC resonance in the phase current introduced by cable line-neutral (DM) capacitance and line-ground (CM) capacitance respectively.



(a) Comparison of DC CM noise with different grounding locations

(b) Comparison of DC DM noise with different grounding locations

(c) Comparison of DC line current noise with different grounding locations

Fig. 4-22. *Comparison of DC EMI Noise with Different Grounding Locations*

5. CONCLUSION

In this report, three types of soft magnetic cores based on the NASA GRC team's advanced nanocomposite magnetics have been designed and fabricated for a selected MW motor drive system in the electric propulsion power train. These cores were evaluated thoroughly and compared with COTS counterparts. Several key findings and lessons are as follows:

1) The DC EMI CM cores are characterized at room temperature and elevated temperature showing robust temperature invariance. Applying such type of cores for the CM inductors demonstrates better noise attenuation performance from 2 MHz to 10 MHz range than the COTS counterpart in a test rig build as per DO-160 standard specifications.

2) Owing to the undesired system resonances in the motor drive system with long cables and prominent parasitic capacitances, a dedicated AC CM choke is proposed and designed as resonance damper as a result of its inherited nonlinear frequency-dependent core resistance and flexible permeability customization capability from the NASA-GRC team. The results showed excellent damping performance and noise reduction at potentially much lower power loss compared to conventional resistor solutions.

3) A comprehensive transmission line effect modeling methodology and dv/dt filter design procedure was developed, and dedicated GRC cores were cast and fabricated for a three-phase dv/dt filter. These cores were tested and/or simulated in a down-scaled motor drive system with 7 m long cable as well as the envisioned 40-meter-long cable system. Comparable voltage overshoot and settling time performances were observed and due to the stronger and more flexible resistive impedance possible with the GRC cores, better dampening of the initial voltage spike is observed in the high current high-power test. To evaluate the thermal stress and core loss of the dv/dt cores as well as its advantage as a gapless core over traditional gaped amorphous cores, a high current high power recirculation test rig was built and tested to 320 Arms at 1 kHz fundamental frequency, 20 kHz switching frequency under 850 Vdc and various modulation indexes given the limitations of the system. The results show better performance by having lower loss over the COTS cores with further room to test at even higher current level to fully illustrate the benefits. The challenges on core loss estimation and measuring are also explored and summarized, for which higher current testing overall provides better and reasonably accurate results.

6. References

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