

NASA TECHNICAL NOTE



NASA TN D-4052

c.1

LOAN COPY: NBSM  
AVAL GALLER  
KIRTLAND AFB, N



TECH LIBRARY KAFB, NM

NASA TN D-4052

IMPROVED MICROPOWER  
LOGIC CIRCUITS

*by John C. Sturman*

*Lewis Research Center*

*Cleveland, Ohio*





## IMPROVED MICROPOWER LOGIC CIRCUITS

By John C. Sturman

Lewis Research Center  
Cleveland, Ohio

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

---

For sale by the Clearinghouse for Federal Scientific and Technical Information  
Springfield, Virginia 22151 - CFSTI price \$3.00

# IMPROVED MICROPOWER LOGIC CIRCUITS

by John C. Sturman

Lewis Research Center

## SUMMARY

Modifications to a previously reported micropower logic circuit improve its performance and make possible its fabrication in monolithic form. A further improvement in power consumption was made by designing the circuit to operate from power supply voltages that vary with temperature.

Logical gating circuits that use these techniques are discussed. These circuits were designed to operate at pulse rates of approximately 100 000 pulses per second at power levels of approximately 100 microwatts each. At reduced pulse rates, the same basic circuits can be designed to operate at power levels as low as a few microwatts per element.

## INTRODUCTION

A steadily increasing effort is being expended to develop low-power logic circuits and semiconductor devices suitable for them. This trend has been in effect for at least 6 years, although the motivations for micropower development have changed considerably during this period. Originally, low-power circuits were necessary to provide any reasonable life for experiments on the relatively small, weight-limited satellites then available. Today, it is possible to launch much larger payloads, but the experiments they carry have become so much larger and more sophisticated that they require a vast increase in the amount of electronics. The situation is further complicated by the wide acceptance of integrated circuits for improved reliability as well as small size. Thus, low power is no longer just a virtue; it has become an absolute necessity if the high packaging density possible is to be fully utilized without creating severe heat dissipation problems.

Until recently, most low-power logic has relied upon conventional circuits using bipolar transistors with passive loads, which dissipate considerable power. It has been shown (ref. 1) that this approach limits the power transfer efficiency of such circuits to

about 18 percent under normal operating conditions. Even when operated at minimum levels of current and voltage, which is usually done, the power levels of this type of circuitry are high for their performance. Considerable improvement in efficiency is attainable with the use of complementary circuits in which NPN and PNP transistors form non-linear loads for each other (refs. 2 and 3). This configuration, first reported by Baker (ref. 4), is quite efficient for multivibrators because complementary outputs are available to provide the proper regenerative drive to all transistors. The configuration is not nearly as good for gate circuits because of the requirement for driving two complementary transistors from a single input. This limitation has been overcome partly in a design made by Schmidt and Chace (ref. 5). They developed a regenerative gate that uses complementary transistors and retains the fast rise and fall times and efficiency of this type of circuit but requires two complementary inputs and as many components as a multivibrator.

Other means of building micropower logic include tunnel diodes (refs. 6 and 7) and complementary field effect transistors (refs. 8 to 11). The tunnel diodes are hampered by the low-power supply voltages required and the difficulty of interstage coupling. The field-effect transistors show considerable promise since field effect devices are readily fabricated in integrated form and since interstage coupling is simplified because of the high input and low output impedances of the devices used.

Currently available field effect transistors are suitable for low-speed logic where they can compete favorably with bipolar devices. The considerably higher operating voltage required by field effect transistors, combined with typical input capacitances of approximately 5 picofarads, leads to power losses that increase with frequency faster than the best micropower circuits built with bipolar devices. Field effect transistors show considerable promise; however, further development will be required to perfect them to a state comparable to the best conventional micropower transistors currently available. About the same can be said of metal-oxide semiconductors, except that the enhancement mode metal-oxide semiconductor transistor may be somewhat superior to the conventional field effect transistor.

It should be apparent from the foregoing that no single type of circuitry is universally applicable to all the requirements of a digital logic system. Early in 1964, a program was therefore undertaken at Lewis to assemble a complete set of compatible, micropower, digital logic modules utilizing the circuit types most adaptable to each function. A secondary requirement was that the circuits, if possible, be adaptable to integrated fabrication techniques. Since this study was oriented toward a general purpose set of logic circuits, only the most generally applicable circuit techniques were considered. Field effect transistors were not sufficiently perfected at the time, so all circuits were built with the best low-power bipolar transistors that could be found. The well-known complementary circuit was chosen for the multivibrators, while the gate circuits used

were based on a similar transistor configuration previously reported (refs. 3 and 12). This circuit utilizes two similar transistors to clamp the output to either the supply voltage or ground, much as is done in the complementary multivibrators. It is easier to drive, however, since the input is to only one of the two transistors, which permits use of all the conventional input gating schemes. This report concerns only the similar transistor gate circuits and their modifications.

Similar transistor gate circuits were designed to operate at a maximum of approximately 100 000 pulses per second over a temperature range of  $-20^{\circ}$  to  $80^{\circ}$  C; however, they were not optimized for such factors as fan-in, fan-out, or noise immunity. Discrete components were used to fabricate the actual modules, but the circuit design was slanted towards future construction in integrated form. A new technique tried was one in which the power supply voltage is made a function of temperature. With this technique, it is possible to use a more optimum design at any temperature and thereby save power.

## SIMILAR TRANSISTOR CIRCUIT DESIGN

### Basic Circuit Design

Most of the gate circuits discussed in this report are derived from the basic similar transistor inverter, originally described in reference 3, and shown in figure 1. Four improvements in the original design were investigated. These include the use of newer and considerably improved transistors, a critical determination of the optimum supply voltages for the original configuration, the replacement of the backward diode with a transistor, and the addition of a complementary transistor to supply a constant current drive. The resulting circuits have a lower power consumption per bit and in some cases are more suitable for construction in integrated form. These changes are described in detail after the basic circuit operation is presented.

The basic circuit, shown in figure 1, is a logical inverter. When the lower transistor  $Q_1$  is saturated by a positive input, its collector potential drops to near ground potential. This drop is coupled through diode  $D_1$  to the base of the upper transistor  $Q_2$ , which turns it off. Simultaneously, a conduction path is provided to ground through backward diode  $D_2$  and the lower transistor to clamp the output to ground. (Shorting of the voltage supply  $V_{CC}$  to ground during this transition due to storage in  $Q_2$  is negligible.) In this state the major power loss occurs, that is, the current-resistance loss  $I^2R$  in resistor  $R_1$ . When no input is present, the lower transistor turns off and current flows from voltage supply  $V_{BB}$  through resistor  $R_1$  into the upper transistor base. This current saturates the transistor, and it clamps the load to voltage supply  $V_{CC}$ . (For proper operation,  $V_{BB}$  must be slightly greater than  $V_{CC}$ .) In this state, the backward

diode in series with the conventional diode appears as an open circuit, so that all current passing through  $R_1$  must flow into the upper transistor and thence to the load. Also, the lower transistor draws no current, so that the only path to ground is through the load resistor. This feature of the circuit leads to its high efficiency.

## Transistor Selection

For use in this circuit, it was difficult to find a transistor that would have high gain at low collector currents, very low leakage, and low junction capacitance. It was necessary to make a fairly detailed survey of available devices and to measure the low-current parameters of a number of selected devices. The results of this study were published in 1965 (ref. 13). By this time, the "zero pf" micropower transistor (2N3493) had been introduced and was the first commercially available transistor designed for minimum power operation. It has the required high gain, low leakage, and most important, junction capacitances of less than 1 picofarad. This transistor was the ideal device for the similar transistor circuit, since it gave considerably improved performance over the best of the devices reported in the previous study.

## Determination of Supply Voltages

Transistor characteristics are the ultimate limiting factor that determines the minimum supply voltage which can be used for a particular circuit configuration. In the case of the similar transistor circuit, a determination of supply voltages is slightly more difficult than that for other circuits because two supply voltages must be optimized. The problem was approached by first determining the lowest practical collector supply voltage  $V_{CC}$  that would meet design requirements over the desired temperature range of  $-20^{\circ}$  to  $80^{\circ}$  C. The voltage drop for one diode used as a logical gate was included in the coupling circuit portion of the design. Only direct-current operating conditions were considered, since the results calculated on this basis allowed a sufficient voltage margin for proper operation. The result of these calculations showed that a collector supply voltage of 2.5 volts was sufficient when the 2N3493 was used in the circuit configuration of figure 1.

Determining the larger of the two supply voltages  $V_{BB}$  required different considerations. In the first attempt to optimize this voltage, the formula derived in reference 4 was used. The formula gives the optimum value of  $V_{BB}$  based on a minimum direct-current dissipation in the circuit elements for the specific case of a 50-percent-on, 50-percent-off duty cycle:

$$V_{BB} = V_{BE} + V_L + \sqrt{\frac{V_L}{2} (V_L + V_{BE})} \quad (1)$$

where  $V_{BE}$  is the base-emitter saturation voltage, and  $V_L$  is the output or load voltage.

The dissipation in the similar transistor circuit can be calculated from the formula used to derive equation (1):

$$(P_T)_{50\%} = \frac{I_{b,2}}{2} \left[ V_{BB} \left( \frac{V_{BB} - V_D - V_{CE}}{V_{BB} - V_L - V_{BE}} \right) + V_{BB} - V_L \right] \quad (2)$$

where  $(P_T)_{50\%}$  is the total power dissipation for a 50-percent duty cycle,  $I_{b,2}$  is the upper transistor base current,  $V_D$  is the coupling diode forward drop, and  $V_{CE}$  is the transistor saturation voltage. If this power is plotted against  $V_{BB}$ , the curve of figure 2 is obtained. (Collector dissipation in the upper transistor was neglected since it is a function of load and not of  $V_{BB}$ .) This curve exhibits a broad minimum at about 5 volts, which is the result obtained from equation (1). Since the minimum is indeed broad, it follows that a small shift from the optimum voltage for  $V_{BB}$  would be permissible if it improved circuit performance - rise time, propagation delay, etc.

To determine the desirability of making a shift from optimum voltage, the transient performance as a function of  $V_{BB}$  was investigated at the Lewis Research Center by Victor Richley of Youngstown University while in the Case-Lewis Summer Facility Program. The results indicated that the optimum value based on optimum rise and fall times for a given power level was very nearly 5 volts, although, as in the direct-current case, the minimum was rather broad.

On the basis of the aforementioned methods, the supply voltages for all the logic elements of the basic similar type were fixed at 2.5 volts for  $V_{CC}$  and at 5.0 volts for  $V_{BB}$ . These voltages are the minimum necessary to allow operation over the desired temperature range of  $-20^\circ$  to  $80^\circ$  C.

## Elimination of Backward Diode

Another desirable modification of the similar transistor circuit is the elimination of the silicon backward diode. This is necessary if the circuit is to be fabricated in integrated form, since it is currently impossible to fabricate tunneling devices with other circuitry in single-chip integrated form.

The unique property of the backward diode most important to the functioning of this circuit is its extremely low forward voltage drop, typically, less than 100 millivolts. This low voltage drop enables the similar transistor circuit to maintain an off voltage less than the turn-on voltage of the succeeding stage. This feature simplifies coupling circuits and eliminates the need for a reverse-biasing supply. If a conventional diode were substituted for the backward diode, the circuit would function, but the off voltage would increase sufficiently to negate this advantage.

To retain the advantages of the backward diode and yet have a completely integrable circuit, the similar transistor inverter shown in figure 3 was developed. The added transistor  $Q_3$ , in conjunction with diode  $D_1$ , isolates the base and the emitter of the upper transistor  $Q_2$  when it is conducting, yet it turns on when the lower transistor conducts to maintain the shunt path from output to ground. The 10-picafarad capacitor  $C_3$  acts as a speedup capacitor to provide extra base drive to transistor  $Q_3$  during the fall times of the output when  $Q_3$  must handle the capacitive discharge current (including strays) from the load. The power consumption of this circuit is slightly higher than the original (fig. 1) because of the dissipation in resistor  $R_4$ . If the fabrication method used allows high value resistors, this increase is negligible, and performance of the modified circuit is in every way comparable to that of the original. If a restriction is placed on maximum resistor size, a small increase in power dissipation may result.

## Current Drive Modification

The power dissipation can be minimized by the proper choice of supply voltages. Further improvement could be made if the larger supply voltage  $V_{BB}$  were reduced without increasing the power dissipation during the time the lower transistor is turned on. This is not possible directly because decreasing  $V_{BB}$  while maintaining a constant base drive for transistor  $Q_2$  requires a lower value of  $R_1$ , which in turn increases the power lost in the circuit, as shown in figure 2. One solution to this problem is the substitution of a constant current device for resistor  $R_1$  of figures 1 and 3. This substitution allows  $V_{BB}$  to be decreased to just slightly more than  $V_{CC}$  without any increase in the power loss. Various field effect and tunneling devices have constant current properties, but few are available presently. Those that are require voltages too high to be practical. A practical solution is the use of a PNP transistor  $Q_4$ , as shown in figure 4. The minimum value for the base drive supply voltage  $V_{BB}$  is now determined by the base voltage  $V_{BE}$  of the PNP transistor and its temperature dependence. The base drive supply voltage  $V_{BB}$  is, however, less than before.

If the same level of base drive is maintained, the circuit of figure 4 is slightly slower, but the lower transistor  $Q_1$  carries considerably less current from the  $V_{BB}$

supply through the drive circuit for the upper transistor, and the circuit dissipation is decreased. By increasing the upper base drive current to  $Q_2$ , circuit performance can be restored. For the circuit shown, the same rise and fall times were attained at a power level below that of the original circuit, as shown in figure 5. This figure compares the power consumption for the original and modified circuits as a function of the pulse repetition rate. Similarly, for the same power level, a faster rise time can be obtained. Another aspect of this modified circuit is the improvement in the shape of the pulse leading edge. Instead of having the characteristically rounded RC time constant shape, it has a linear rise with little rounding at the top, which suggests that this modified circuit could also be used to generate a ramp by the addition of a timing capacitor. As the circuit stands, the rise time is determined by the various capacitances connected and reflected to the base of the upper transistor  $Q_2$  and the charging current delivered by the PNP transistor  $Q_4$ .

### Relation of Supply Voltage to Temperature

The minimum operating voltage for a particular circuit configuration is strongly influenced by device parameters and, therefore, by temperature. It was therefore undertaken by Anthony V. Bertolino to determine the minimum operating voltages for the similar transistor circuit as a function of temperature, and using worst-case design conditions.

A computer program was written to calculate the minimum values of supply voltages using as input the transistor parameters and their variation with temperature. The results are presented in figure 6 for the circuit shown in figure 1. Circuits built and operated at the computed voltages performed reliably but showed considerable variation in propagation time over the temperature range given. To correct this variation, the computer-calculated supply voltage curve for  $V_{CC}$  was made linear with temperature and was increased somewhat to extend operation to  $150^{\circ}$  C. The resulting rise time at various temperatures was measured, and an easily attainable value was selected. The linearized values of  $V_{CC}$ , shown in figure 6, were used to determine experimentally the values of  $V_{BB}$  necessary to maintain a constant rise time of 0.5 microsecond for the circuit of figure 4. The resulting  $V_{BB}$  is also plotted as a function of temperature in figure 6. The power consumption for the circuit operated under these conditions compared with that for operation at constant supply voltages is presented in figure 7. At constant voltage, this circuit had a rise time that varied from 0.86 to 0.30 microsecond over the temperature range of  $-50^{\circ}$  to  $125^{\circ}$  C.

This modified transistor circuit evidently accomplished the basic goal of saving power and, in addition, eliminated rise-time change with temperature. The fact that power consumption decreases rapidly with temperature indicates that this is indeed a

partial solution to the thermal dissipation problem. The solution even tends to stabilize circuit temperature by decreasing power consumption as the circuit becomes hotter and by dissipating more power as the circuit cools. In actual practice, it would be necessary to have a temperature sensor monitor the temperature of the assembly of elements and control the power supply accordingly.

During the course of this work, the author did not come across any published mention of the techniques just discussed. However, while this report was in preparation, an article (ref. 14) that appeared showed some of the practical aspects of "Sliding-Scale" power supplies and illustrated several methods of achieving various compensating functions.

All the changes made to the basic similar transistor inverter do not in any way affect the external connection of the circuit. Only one input is required, which permits the use of most standard gating circuits with it. The output voltage in the low state is sufficiently small that no voltage shifting is necessary in coupling to succeeding stages. Thus, minimum power and maximum simplicity are achieved. Logic circuits based on the similar transistor concept are discussed in the following section.

## SIMILAR TRANSISTOR LOGIC CIRCUITS

The basic similar transistor circuit previously described is an inverter and may be used as such. Since its input drives only one transistor in a conventional fashion, all normal coupling and gating circuits can be used. In terms of minimum power consumption, the use of either diode gating or transistor gating is best when the circuits are constructed in discrete component form. The circuit can be operated with  $T^2$  L-type inputs, but too much capacitance is added to the input if a separate transistor must be used for each input. With multiple-emitter transistors, used as either discrete components or in integrated circuit form, considerably better performance could probably be obtained (ref. 15).

There is some choice to be made in the type of gating to be used with the similar transistor circuit. Transistor input gates give good performance because they allow direct coupling between stages so that both positive- and negative-going waveforms are coupled into the circuit. In comparison with transistor input gates, when diode gates are used, the diodes isolate the driven circuit for one polarity transition, and a sufficiently low resistance must be provided to return the input capacitance to the opposite polarity or nondriven state. The result is increased dissipation, since nearly all micropower circuits operate in a region where their transition times are determined by RC time constants and not by other device parameters. When used in the NOR configuration shown in figure 8, transistor gates do have the disadvantage of paralleled collector capacitance.

This disadvantage causes a noticeable degradation of circuit transition times and therefore has been used for gates of no more than two inputs. The use of transistor gating in the NAND configuration shown in figure 9 is also limited to two inputs. In this case, performance is not penalized by the use of two transistors because they are used in series; the limitation is due to the collector-emitter saturation drop across the transistors. If more than two were used, the total direct-current drop would be such that the following stages would be biased very close to conduction for no input. Insufficient safety margin would exist.

Although it is logically possible to build systems that use only two input gates, this design is quite impractical when the power required is a consideration. For more than two inputs, diode gates are quite effective and those shown in figures 10 and 11 have been used. In practice, there is little difference in performance between the various gate circuits, as is shown in figure 12. Thus, the validity of limiting the use of transistor gating to no more than two inputs is indicated.

Other functions can also be implemented with transistor gating. For instance, if it is practical to build special purpose circuits for a given application, a combination of elements such as those shown in figure 13 is possible. This combination provides the logical function  $D = A \cdot C + B \cdot C$  with a power drain equal to that of only one logic element. To use NAND and NOR elements in this combination would require four of them if the exact function were required and three if the inverted output were acceptable.

Another example of a special application circuit is the exclusive NOR circuit shown in figure 14 along with a truth table of its logical characteristics. It operates on the power for a single element, and as such represents a large power saving in implementing the exclusive NOR function. Although it has been used successfully in micropower logic systems, it has several characteristics that must be considered carefully to determine if it is applicable in any particular system. One limiting factor is that the circuit transfers the turn-off load from the output to the driving stages. This limits the fan-out in many practical cases and prevents cascading exclusive NOR circuits. A further limitation of the circuit is that it may provide an erroneous output under certain transient conditions, as exemplified in figure 15. When both inputs drop simultaneously, or very nearly so, a negative-going spike appears at the output. It lasts only about a microsecond, but this might be long enough to cause false triggering in some systems. The circuit, when circumstances permit its use, does implement the exclusive NOR function with a very minimum power requirement.

Although the circuits previously described are quite sufficient to provide all gating functions for a logic system, provisions for time delay and storage remain. If triggering is not considered, it is always possible to connect pairs of inverters to form bistable elements, in which case, an R-S flip flop can be constructed with a pair of two input NOR gates. In like manner, the similar transistor gates can be used to build monostable

multivibrators for the time delay function. Although these multivibrators work when built up in this fashion, they do not trigger as easily as might be desired for short pulses. This deficiency could probably be corrected by suitable modification to adapt the basic circuit to the specific design of a multivibrator element. This adaptation would be desirable for integrated circuits in particular, although it was not made in this program because all circuits were to be built with discrete components, and designs for complementary multivibrators were readily available. (Further information on complementary micropower logic circuits can be found in refs. 16 to 21.)

## RESULTS AND DISCUSSION

Several modifications of the basic similar transistor circuit were discussed, and specific designs and performance data presented for some. These circuits have been used in a number of logic elements that were built with discrete components and used an improved cordwood packaging technique (ref. 22). The logic elements in turn have been used successfully to construct breadboard flight-type digital systems capable of operating at clock rates exceeding 100 000 pulses per second. The average power drain for each of these elements is approximately 100 microwatts when operated with supply voltages of 2.5 and 5.0 volts. Also, as indicated in figures 6 and 7, the basic circuits can operate even more efficiently over wide temperature extremes at a minimum power drain if the power supply voltages are made a function of temperature.

Important features of these logic elements include (1) minimum power consumption, which is due partly to the low supply voltages used; (2) flexible logic design made possible by the use of several gate types, which facilitates minimizing the number of elements required per system, and concomitantly, the power drain; (3) operation over a wide temperature range; (4) good fan-out (a factor of 5 achieved easily and possibly much higher values); (5) the capability of easily scaling the circuits to optimize their operation for any pulse rate up to about a million pulses per second. This latter feature requires some elaboration. The ability to scale the operating rate of these circuits lies in the fact that at low power levels the maximum operating rate is determined by RC time constants and not transistor transient response. As long as operation is in this range, a proportional change in the value of all resistors will change the maximum operating rate. A small adjustment of the speed-up capacitors may be necessary also, since the turn-on change varies somewhat with the load current. Power consumption will, of course, change in direct proportion to the maximum operating rate.

The circuits described in this report, while applicable to any logic system, may not represent the optimum circuit configurations for any specific case. Permitted the freedom to design a special circuit for each logic element in a system, it is possible to im-

prove upon any small set of logic elements. An example of such an improvement would be a gate that has an extremely low duty cycle and drives a minimum load. The simplicity gained here by the use of a conventional circuit might outweigh the negligible power saving, if any, to be had with micropower circuits. (See ref. 23 for a discussion of other circuit types applied to micropower.)

At the present, the similar transistor concept has not been used to build a complete set of compatible logic elements. The real impetus for this would be a need for micropower integrated circuits, in which application the similar transistor concept should be of maximum value, particularly if it is used with controlled power supply voltages. Since power dissipation is still a major problem for high-density integrated circuits, the circuits described in this report should prove valuable.

Lewis Research Center,  
National Aeronautics and Space Administration,  
Cleveland, Ohio, March 1, 1967,  
125-25-02-01-22.

## REFERENCES

1. Sturman, John C.: Micropower Logic Circuits. NASA SP-5022, 1965. (Also: Sturman, J. C.; and Hall, J. H.: Micropower Logic Circuits. Instruments Control Syst., vol. 39, no. 8, Aug. 1966, pp. 101-105.)
2. Bothwell, T. P.; and Kolodin, L.: A Bistable Symmetrical Switching Circuit. Proceedings of the National Electronics Conference, Vol. 12, National Electronics Conference, Inc., 1957, pp. 655-667.
3. Sturman, John C.: Micropower Transistor Logic Circuits. NASA TN D-1462, 1963.
4. Baker, R. H.: Maximum Efficiency Transistor Switching Circuits. Tech. Rep. 110, Lincoln Lab., M.I.T., Mar. 22, 1956.
5. Schmidt, W. G.; and Chace, D. E.: Design Aspects of Minimal-Power Digital Circuitry. Group Rep. -1965-6(AFESD-TDR-65-45, AD-612769), Lincoln Lab., Mass. Inst. Tech., Feb. 9, 1965.
6. Englemann, R.: Research and Development of Solid State Tunnel Devices and Arrays Capable of Operation at Microwatt Power Levels. Final Dev. Rep., June 1, 1962-July 31, 1963, CBS Labs., Aug. 19, 1963. (Available from DDC as AD-417247.)

7. Gardner, P. ; Glicksman, R. ; and Bergman, R. H. : Application of Tunnel Diodes to Micropower Logic Circuits. Proceedings of the National Aerospace Electronics Conference, Dayton, May 11-13, 1964, IEEE, 1964, pp. 32-38.
8. Mitchell, M. M. ; and Ahrons, R. W. : MOS Micropower Complementary Transistor Logic. Computer Design, Feb. 1966, pp. 28-38.
9. Moore, G. E. ; Sah, C. T. ; and Wanlass, F. M. : Metal-Oxide-Semiconductor Field-Effect Devices for Micropower Logic Circuitry. Micropower Electronics. Edward Keonjian, ed., AGARDograph No. 77, Pergamon Press, 1964, pp. 41-55.
10. Ahrons, R. W. ; Mitchell, M. M. ; and Burns, J. R. : MOS Micropower Complementary Transistor Logic. - Proceedings of the 1965 International Solid-State Circuits Conference, Digest of Technical Papers, R. M. Foster, Jr., ed. Lewis Winner, 1965, vol. 8, pp. 80-81.
11. Gagnon, Roger A. : The Use of Metal-Oxide-Semiconductor Field Effect Transistors (MOST) in Complementary Configurations. Masters Thesis, Rep. No. GE/EE/65-9, AD-622424, Air Force Institute of Technology, Aug. 1965.
12. Sturman, John C. : Inverter Circuit, U. S. Patent 3,271,590, Sept. 6, 1966.
13. Sturman, John C. ; and Kovach, Donald G. : Evaluation of Transistors and Diodes For Micropower Circuit Applications. NASA TM X-1050, 1965.
14. Gams, Theodore C. : "Sliding-Scale" Power Supplies Can Improve Instrument-System Accuracy. Electronic Instrument Digest, Mar.-Apr. 1966, pp. 8-11.
15. Boulter, B. A. : The Multiple Emitter Transistor in Low Power Logic Circuits. Micropower Electronics. Edward Keonjian, ed., AGARDograph No. 77, Pergamon Press, 1964, pp. 105-120.
16. Eimbinder, Jerome: Multichip Circuits Get Off the Ground. Electronics, vol. 37, no. 25, Sept. 21, 1964, pp. 105-107.
17. Tietsch, Roger A. : Complementary Microwatt Logic Circuits. Electronic Equipment Eng., vol. 11, no. 8, Aug. 1963, pp. 50-52.
18. Chang, G. Y. : A Silicon Monolithic, Micropower Complementary Flip-Flop. Integrated Circuits. Pt. 2 of WESCON/65; Proceedings of the Western Electronic Show and Confention, San Francisco, Aug. 24-27, 1965, Western Periodicals Co., 1965.
19. Tietsch, R. A. : Integrated Micropower Circuits. Final Rep., Sperry Rand Corp. (NASA CR-53512), 1963.

20. Hung, R. Y.; and Lin, H. C.: Integrated High-Speed, Low-Power Complementary Bipolar Transistor Nand Gate. Integrated Circuits. Pt. 2 of WESCON/65; Proceedings of the Western Electronic Show and Convention, San Francisco, Aug. 24-27, 1965. Western Periodicals Co., 1965.
21. Sturman, John C.; and Bertolino, Anthony V.: Low-Power, Low-Level Analog-to-Digital Converter for Space Vehicle Applications. NASA TN D-2916, 1965.
22. Sturman, John C.: A Fast and Economical Technique for Welded Cordwood Electronic Module Fabrication. NASA TM X-1206, 1966.
23. Wagner, Lawrence F.; and Meindl, James D.: Static and Dynamic Performance of Micropower Transistor Logic Circuits. Integrated Circuits. Pt. 2 of WESCON/65; Proceedings of the Western Electronic Show and Convention, San Francisco, Aug. 24-27, 1965. Western Periodicals Co., 1965.

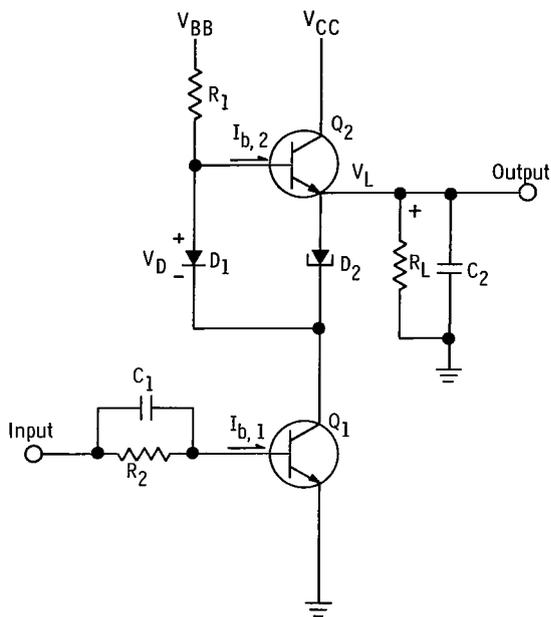


Figure 1. - Similar transistor inverter.

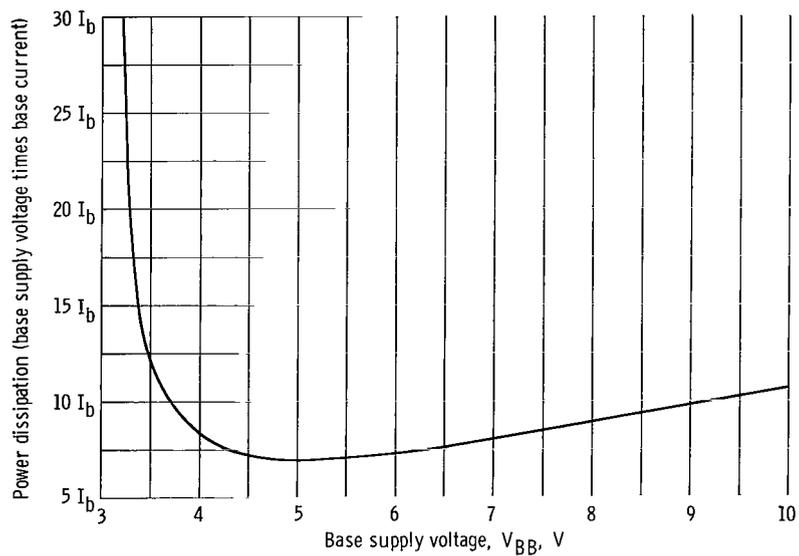


Figure 2. - Calculated power dissipation as function of base supply voltage in similar transistor circuit.

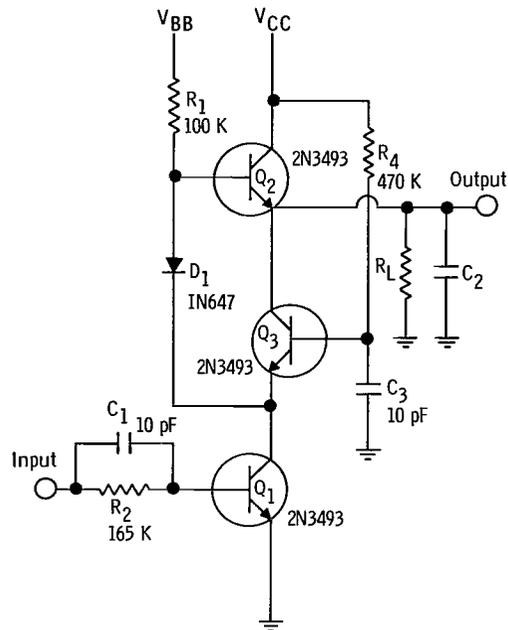


Figure 3. - Similar transistor inverter modified to eliminate backward diode.

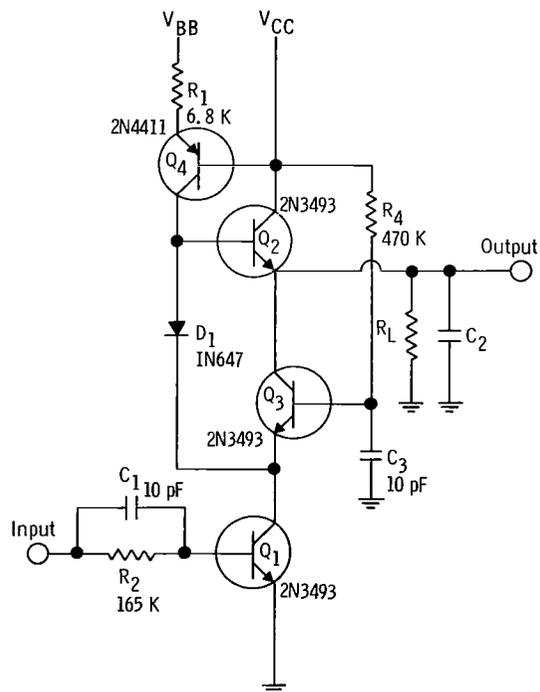


Figure 4. - Similar transistor inverter with constant current drive.

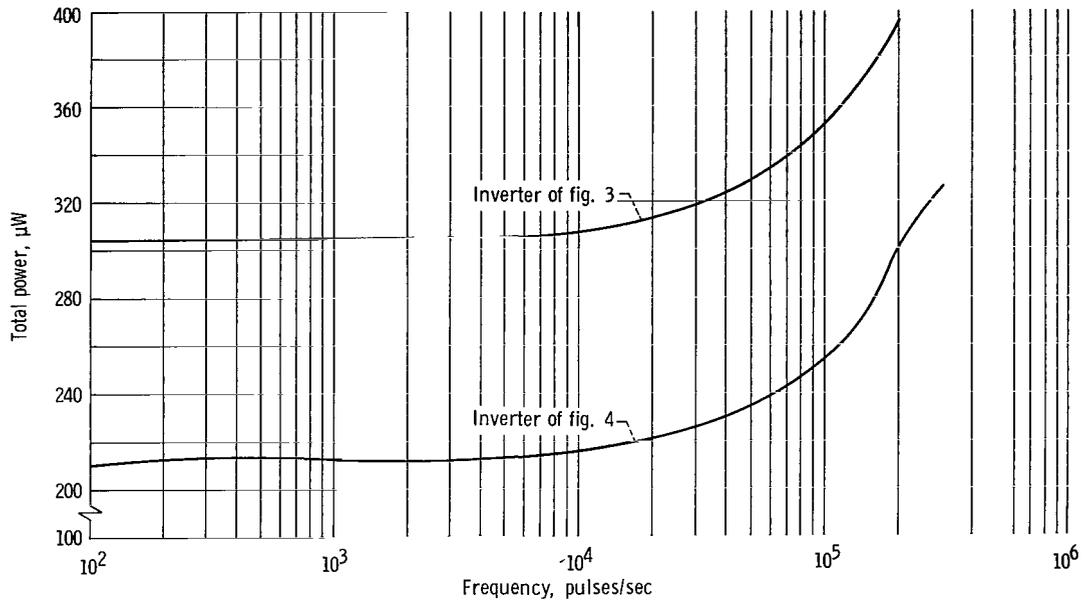


Figure 5. - Comparison of inverter power requirements as function of pulse repetition rate.

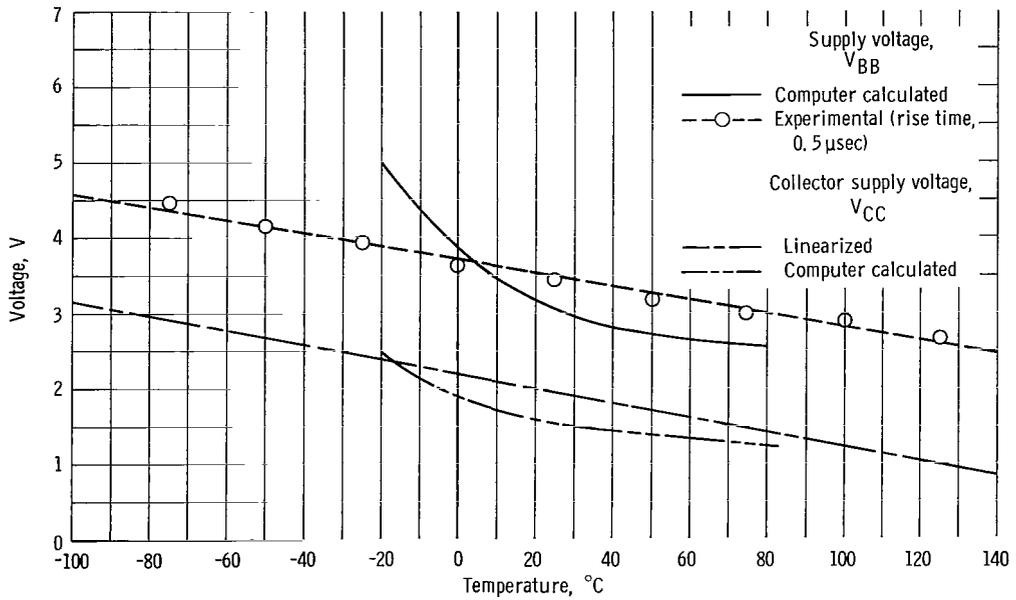


Figure 6. - Similar transistor supply voltages.

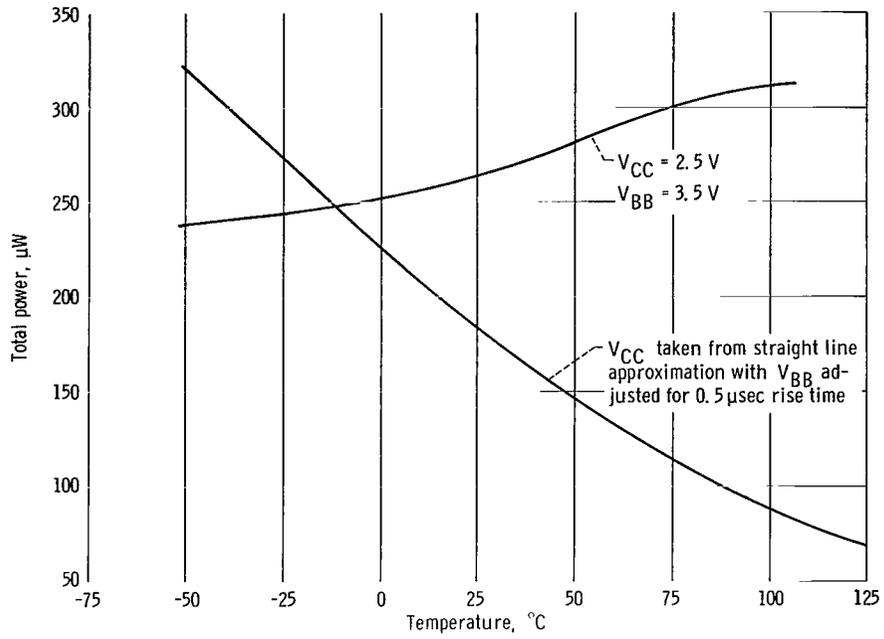


Figure 7. - Power as function of temperature for current drive similar transistor circuit.

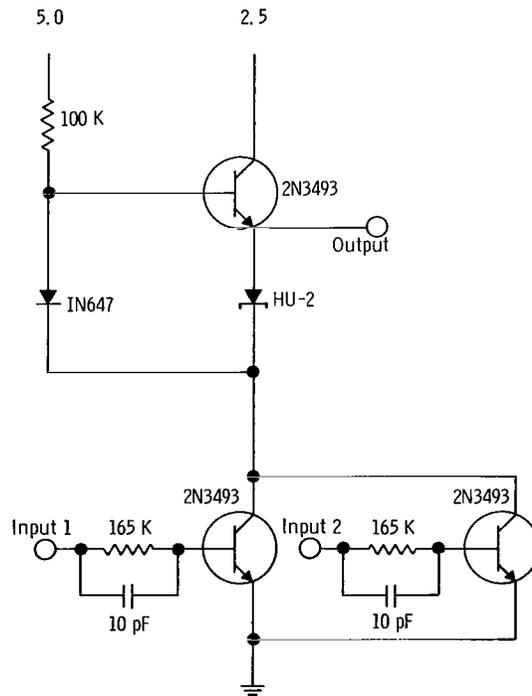


Figure 8. - Transistor input for similar transistor NOR gate.

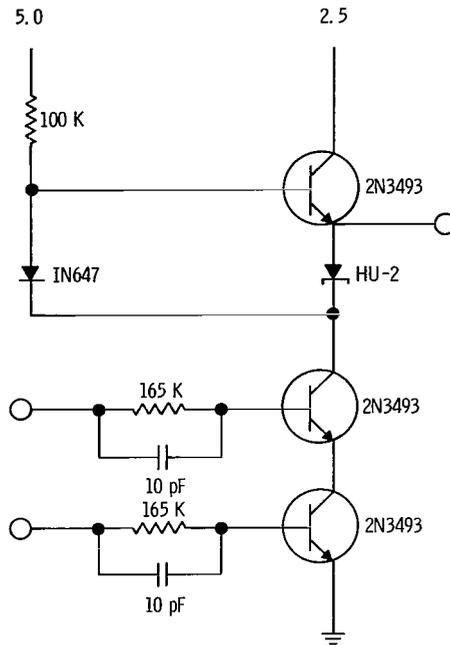


Figure 9. - Transistor input similar transistor NAND gate.

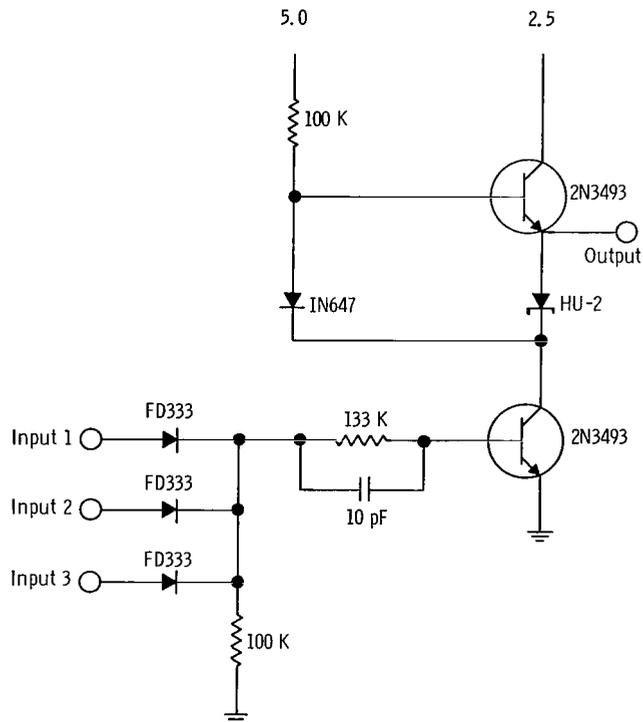


Figure 10. - Diode input similar transistor NOR gate.

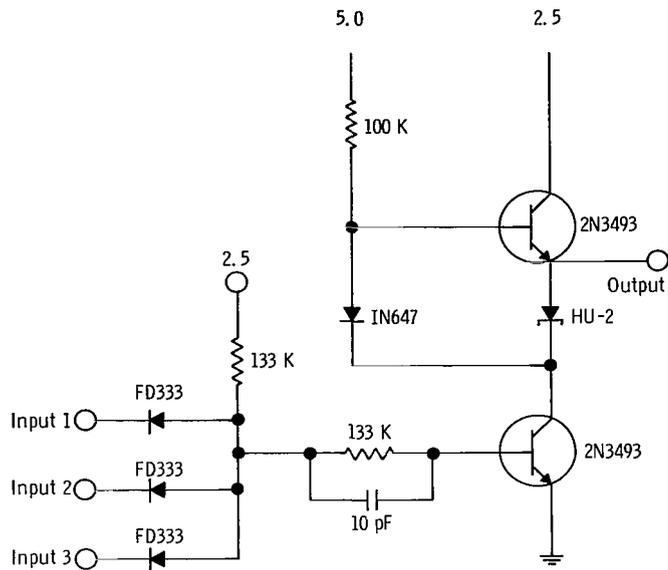


Figure 11. - Diode input similar transistor NAND gate.

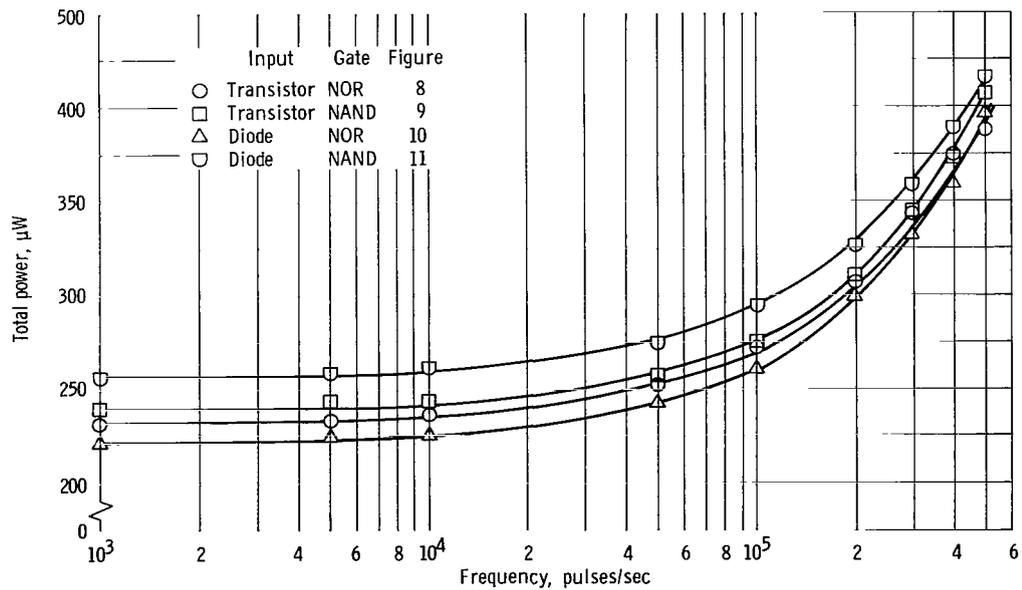


Figure 12. - Power consumption of similar transistor gates. All gates loaded with 33 000 ohms and 50 picofarads.

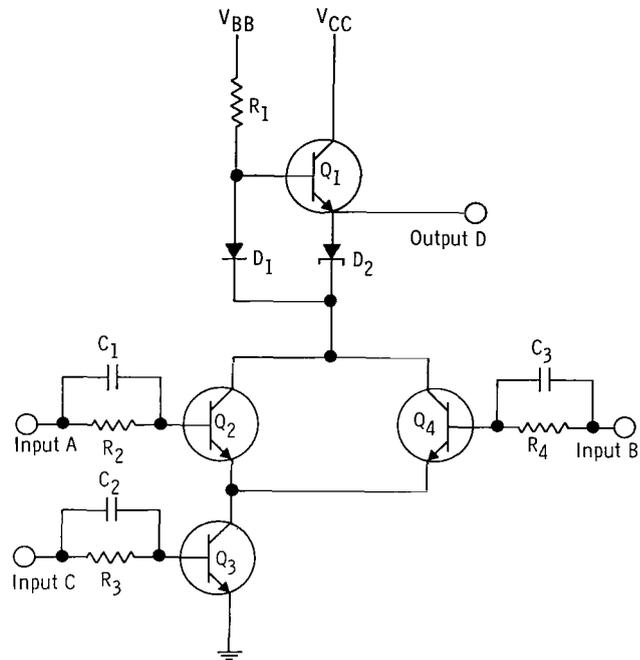


Figure 13. - Combined gate.  $D = \overline{A \cdot C} + \overline{B \cdot C}$ .

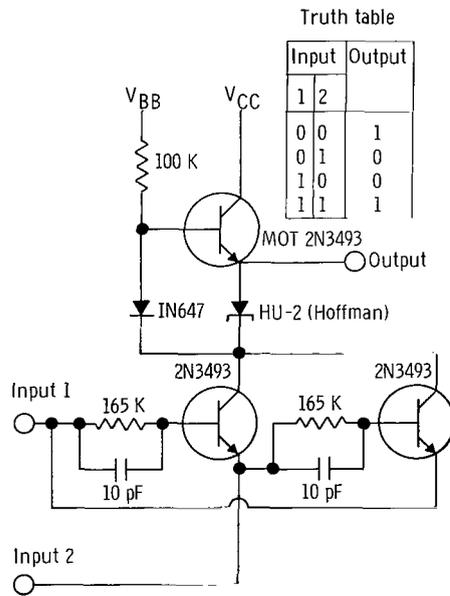


Figure 14. - Exclusive NOR gate.

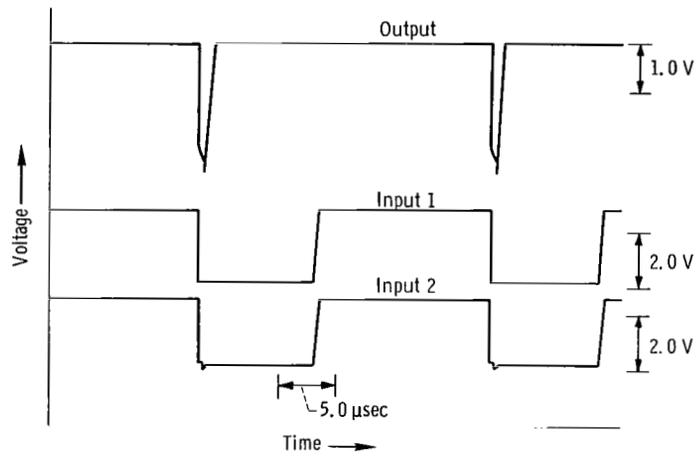


Figure 15. - Waveshapes of two-input similar transistor exclusive NOR gate.

*"The aeronautical and space activities of the United States shall be conducted so as to contribute . . . to the expansion of human knowledge of phenomena in the atmosphere and space. The Administration shall provide for the widest practicable and appropriate dissemination of information concerning its activities and the results thereof."*

—NATIONAL AERONAUTICS AND SPACE ACT OF 1958

## NASA SCIENTIFIC AND TECHNICAL PUBLICATIONS

**TECHNICAL REPORTS:** Scientific and technical information considered important, complete, and a lasting contribution to existing knowledge.

**TECHNICAL NOTES:** Information less broad in scope but nevertheless of importance as a contribution to existing knowledge.

**TECHNICAL MEMORANDUMS:** Information receiving limited distribution because of preliminary data, security classification, or other reasons.

**CONTRACTOR REPORTS:** Scientific and technical information generated under a NASA contract or grant and considered an important contribution to existing knowledge.

**TECHNICAL TRANSLATIONS:** Information published in a foreign language considered to merit NASA distribution in English.

**SPECIAL PUBLICATIONS:** Information derived from or of value to NASA activities. Publications include conference proceedings, monographs, data compilations, handbooks, sourcebooks, and special bibliographies.

**TECHNOLOGY UTILIZATION PUBLICATIONS:** Information on technology used by NASA that may be of particular interest in commercial and other non-aerospace applications. Publications include Tech Briefs, Technology Utilization Reports and Notes, and Technology Surveys.

*Details on the availability of these publications may be obtained from:*

SCIENTIFIC AND TECHNICAL INFORMATION DIVISION  
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Washington, D.C. 20546