

NASA TM X-55905

# A RESETTABLE MONOSTABLE PULSE GENERATOR

## NORMAN M. GARRAHAN

JULY 1967



**GODDARD SPACE FLIGHT CENTER**  
**GREENBELT, MARYLAND**

GPO PRICE \$ \_\_\_\_\_

CFSTI PRICE(S) \$ \_\_\_\_\_

Hard copy (HC) 3.00

Microfiche (MF) .65

**N67-36402**

(ACCESSION NUMBER)

(THRU)

11  
(PAGES)

1  
(CODE)

TMX-55905  
(NASA CR OR TMX OR AD NUMBER)

09  
(CATEGORY)

FACILITY FORM 802

A RESETTABLE MONOSTABLE  
PULSE GENERATOR

Norman M. Garrahan

July 1967

GODDARD SPACE FLIGHT CENTER  
Greenbelt, Maryland

PRECEDING PAGE BLANK NOT FILMED.

### ABSTRACT

Galactic x-ray investigation requires the selection for measurement of individual x-ray particles from a multitude of other cosmic particles constantly impinging on the detecting sensors. To isolate a lone genuine x-ray event, a section of the logic requires a 10-microsecond blocking resettable memory to indicate a preceding absence of pulse pileup and to permit the sensors to reach their quiescent state. Such a circuit is discussed herein.

A low-power solid-state memory circuit furnishes a blocking output state for a preset time duration upon receipt of a particle-pulse from the sensors. It is also capable upon receipt of an additional close-following particle-pulse (which could cause pulse pileup) of terminating the first preset time duration and commencing a new preset time duration without interruption to the existing blocking output state. Circuit operation is discussed in detail.

PRECEDING PAGE BLANK NOT FILMED.

PRECEDING PAGE BLANK NOT FILMED.

CONTENTS

	<u>Page</u>
ABSTRACT . . . . .	iii
INTRODUCTION . . . . .	1
RESETTING MONOSTABLE . . . . .	1
CONSTANT-AMPLITUDE PULSE GENERATOR . . . . .	7

ILLUSTRATIONS

Figure

1	Resettable Monostable Functional Block Diagram. . . . .	1
2	Constant-Amplitude Pulse Generator Schematic Diagram . .	3
3	Resettable Monostable Pulse Generator . . . . .	4
4	Resettable Monostable Waveforms . . . . .	5

~~PRECEDING PAGE BLANK NOT FILMED.~~

# Resettable Monostable

## A PULSE GENERATOR WITH OUTPUT RESETTING

By  
Norman M. Garrahan

### INTRODUCTION

As part of NASA's continuing scientific effort directed to galactic x-ray investigation, several rockets will be launched toward the Crab Nebula for x-ray particle measurement. The sampling and measurement equipment aboard one of these rocket experiments has a requirement for a low-power solid-state logic circuit to furnish a blocking output state for a preset time duration upon receipt of a particle-pulse. It must also be capable upon receipt of an additional close-following particle-pulse (which may cause pulse pileup) of terminating the first preset time duration and commencing a new preset time duration without interruption to the existing blocking output state. A circuit which can satisfy these requirements is herein described and is called a resettable monostable, although in the actual x-ray rocket equipment it is referred to as a resettable memory.

### RESETTABLE MONOSTABLE

This composite circuit may be conveniently broken down into three separate functions as shown in Figure 1. In the first function (a), the particle input pulse triggers a pulse generator which supplies a constant-amplitude fixed-width unipolar pulse to a timing circuit in (b) which generates a ramp rundown about a preset dc level. This dc level sets the threshold turn-on point for the output pulse generator of (c). When the ramp exceeds the preset dc level the pulse generator will switch output states and remain in the new output state for the duration of time the ramp remains above the preset dc level. A second or an additional particle pulse will generate another constant-amplitude pulse to reset the timing circuit and commence a new ramp rundown. The resetting consists of placing a new charge on the timing capacitor. The unique feature of this

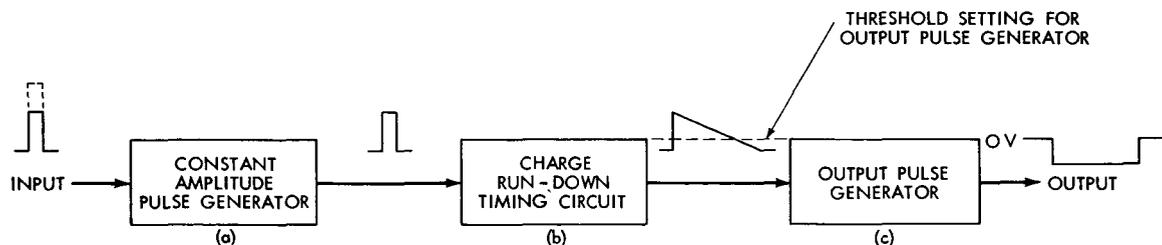


Figure 1. Resettable Monostable Functional Block Diagram

operation is the fact that the amount of total charge from which the ramp commences to rundown is the same for each received pulse regardless of the amount of charge remaining on the timing capacitor from the previous pulse. Thus, each received pulse reinitiates a new "C"-measured rundown-discharge time independent of any previously received pulse. Furthermore, as long as the ramp rundown remains above a preset dc level the output pulse generator will remain in its first-received pulse-triggered output state regardless of how many later input pulses act on the ramp rundown.

Where a constant-amplitude pulse is available it may be fed directly into the (b) circuits; otherwise the constant-amplitude pulse generator circuit should be used. This ensures that the timing capacitor used to generate the ramp rundown receives the same amount of charge for each input pulse received. A schematic diagram of this circuit is shown in Figure 2.

Figure 3 shows the resettable monostable of Figure 1(b) and the output pulse generator of Figure 1(c) as a unit. The monostable has two discrete output states; (1) rest state 'A' and (2) new triggered-on state 'B'. The 'B' on-time duration is determined by the run-down of an acquired charge on capacitor C9 in the R20C9 network. On receipt of a constant-amplitude input pulse this capacitor is charged to a fixed level in the RC network and immediately commences to discharge or run-down linearly towards a zero charge level. After passing through a cascaded emitter follower where it receives a -0.5 voltage offset, this point is picked off and coupled to a dc level-sensitive threshold-sensing circuit preset to be actuated when the acquired charge is raised above -0.3 volt towards ground. On receipt of a second or subsequent trigger pulse within the RC run-down-time duration the acquired charge is reset to the fixed peak level, the first or previous measured run-down is terminated, and a new run-down commences from the new level of acquired charge. It is significant to note that the old acquired charge does not fall to a zero level but immediately resets to the peak level of the newly acquired pulse-charge. This is shown in the waveforms of Figure 4(a and b). The coupled dc level-sensitive threshold-sensing circuit previously actuated when the first or original acquired charge was raised above the -0.3 volt trigger level will not see the acquired charge level variations that occur above this threshold sensing level, and therefore the threshold circuit output will remain unchanged from its first pulse-actuated 'on' state.

In Figure 3, transistors Q5 and Q6 form an emitter-coupled pair and function as a voltage comparator to the voltages applied across each base. The output is single ended and is taken from across R15 and used to drive charging transistor Q9, which charges timing capacitor C9 through fast-recovery diode

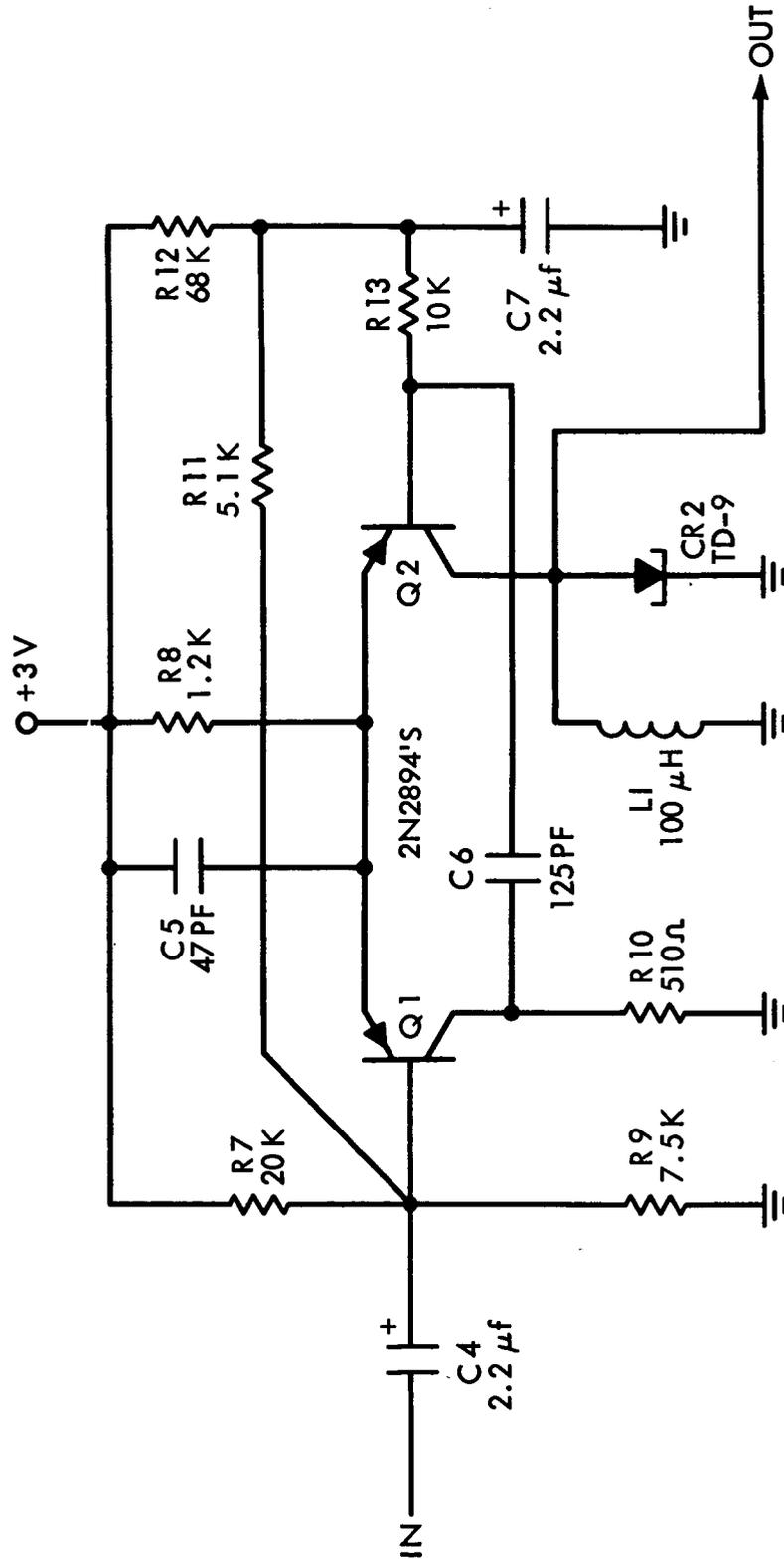


Figure 2. Constant-Amplitude Pulse Generator Schematic Diagram

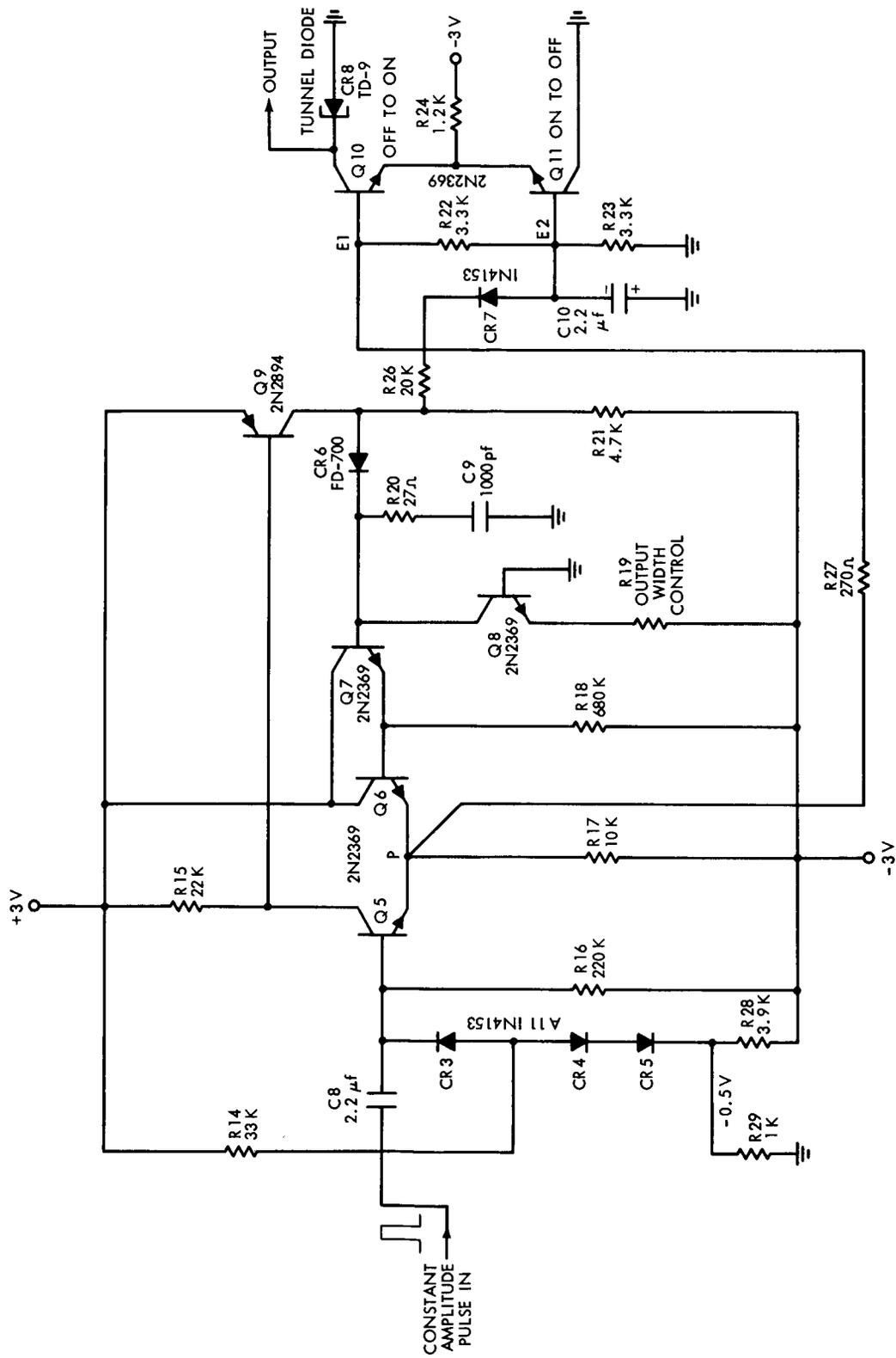


Figure 3. Resetable Monostable Pulse Generator

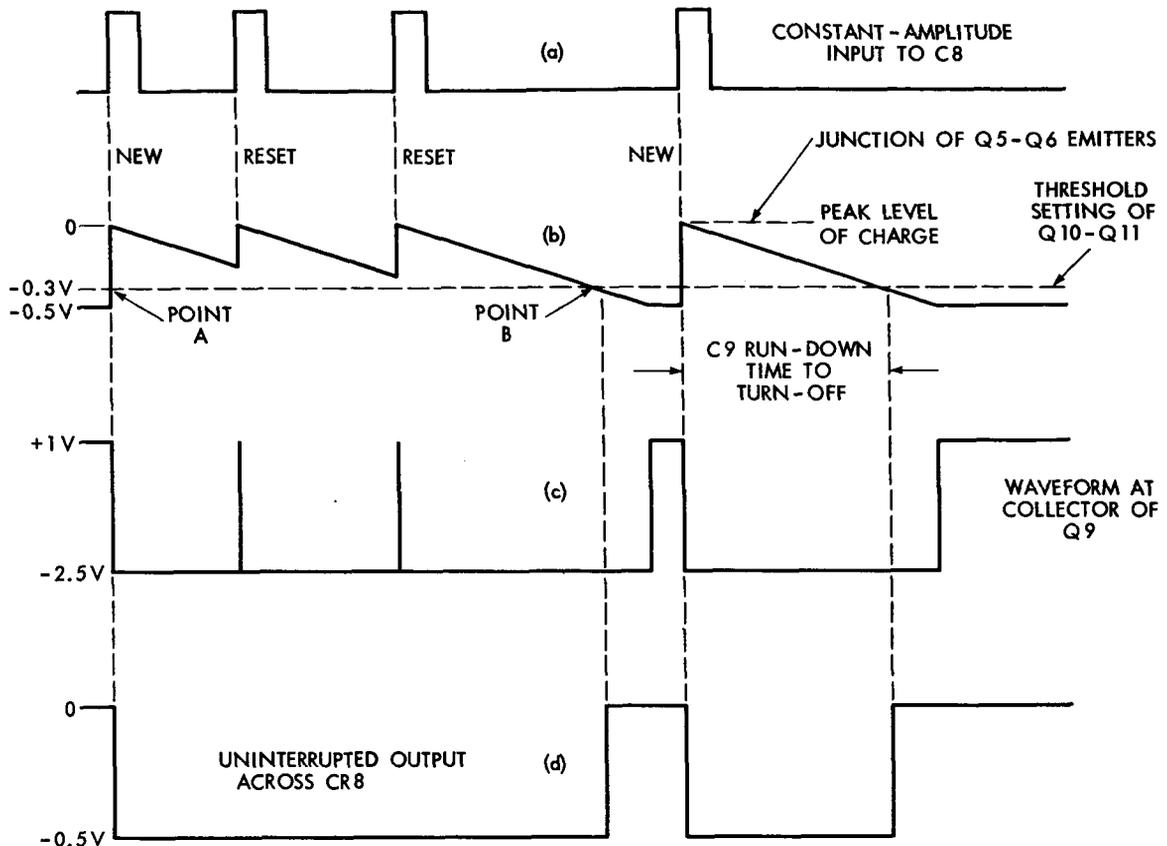


Figure 4. Resetable Monostable Waveforms

CR6. The three diodes at the input, CR3, CR4, and CR5, form a dc restorer (and temperature compensating) circuit which references all incoming pulses to a common level. Transistor Q8 and resistor R19 provide a constant-current discharge path for capacitor C9 to achieve a linear run-down. Transistor Q7 provides a high-impedance couple between the voltage comparator and the timing capacitor C9. Where stringent requirements on pulse width variations prevail, R19 may be connected to a zener diode-controlled reference voltage instead of directly to the usual power bus.

Disregarding circuit components R26 and CR7 for the moment, the operation of this resetable monostable is described next. On receipt of an input pulse, Q5 drives Q9 which rapidly forces a charge into C9 through CR6. The width of the input pulse is chosen to permit C9 to charge to the peak input amplitude while the input pulse is still present on the base of Q5, thus an input-image pulse appears on the base of Q6. Voltage comparator Q5-Q6 now cause the collector current of Q5 to seek a null thus removing the drive from across R15. By this time the input pulse has passed and C9 commences to discharge through Q8. The termination of the drive on Q9 results in its collector rising to the supply

voltage of -3 volts; therefore diode CR6 is back-biased, preventing any leak back of the charge on C9. The discharge path for C9 is mainly through Q8 but a negligible amount is taken by Q7 to maintain it and hence Q6 in conduction. The waveform at the collector of Q9 is shown in Figure 4(c).

Once the input pulse has passed, the emitter current of Q6 flowing through common emitter resistor R17 will hold Q5 in cutoff to a back-bias level equal to the voltage remaining on timing capacitor C9. As long as there is any charge remaining on C9, transistor Q6 will be maintained in conduction and its emitter current through R17 will generate a value of hold-off bias for Q5. This is significant because it implies that any additional new pulse(s) must first overcome this hold-off bias before Q5 will again conduct (a measure of noise immunity).

As far as timing capacitor C9 is concerned any additional new pulse(s) will reset the acquired charge level to the fixed peak charge level from the existing charge level, rather than from the zero charge level. This feature is shown in Figure 4(b) for various pulse recurrence times. The acquired charge (junction P) does not first fall to zero for pulses falling within the discharge run-down time of C9, but its charge is immediately reset to the peak charge level. Therefore, when triggered with a 'first' pulse, the output state remains uninterrupted for all subsequent pulses occurring within that portion of the RC run-down ramp time existing above the threshold-sensing-level turn-off point. Thus, as indicated in Figure 4(b), a dc-level-sensitive threshold detector connected at the junction of the Q5-Q6 emitters will be actuated at point 'A' and remain in the ON state through time duration 'B' without interruption. Transistors Q10-Q11, tunnel diode CR8 and the associated resistors and capacitors compose this threshold detector. The acquired charge level variations, referenced to -0.5 volt, are picked off junction 'P' of Q5-Q6 (Figure 3) and fed through low-value isolating resistor R27 to the voltage divider combination consisting of R22 and R23; decoupled voltage E2 essentially sets the reference switching point. These resistance values are so weighed that voltage levels E1 and E2 favor a stable non-conducting state for Q10 and a conducting state for Q11 for the quiescent condition when only the reference level of -0.5 volts is present at the top of R22-R23. On receipt of the acquired charge voltage variations (positive going from the -0.5 voltage reference level) Q10 will be switched ON and Q11 switched OFF. With this increase in the collector current of Q10, diode CR8 will be switched from a low impedance 'OFF' state to a high impedance 'ON' state and a fast-risetime pulse will appear across CR8. Transistor Q10 and CR8 will remain in this state for the duration of time the acquired charge at junction 'P' remains above the threshold setting level.

To achieve the same output pulse width for each input pulse regardless of variations in trigger repetition rate it is necessary to maintain a constant

voltage at E2 across R23. As shown in Figure 4(b) for high repetition rates the acquired charge level may not reach the -0.5 volt reference level for extended periods, and were it not for the presence of compensation provided to E2, this would cause the average charge build-up on C10 to fall—changing the trigger reference level. This compensation is provided by connecting the E2 point to the collector of Q9 through R26 and CR7. The pulse appearing at the collector of Q9 is negative, as shown in Figure 4(c), and follows the acquired charge run-down-time duration. Sufficient additional current is thus supplied to C10 by selecting R26 to compensate for the reduced charging effects of high input pulse repetition rates. Diode CR7 prevents any leak back from C10 at low repetition rates.

Temperature compensation for the base-emitter junction offset voltage variation of Q5 is provided by the diode network consisting of CR3, CR4, and CR5. This insures that the -0.5 volt reference level is temperature stable. Additional temperature stability of the output pulse width may be achieved by sharing the total resistance of R23 with a sensistor.

Choosing a value for timing capacitor C9 is interrelated with the required output pulse width, input pulse amplitude and width into C8, and ramp discharge current through Q8. The ramp discharge current through Q8 must be great enough to maintain Q8 in conduction at low temperatures and also be several orders of magnitude above other leakage currents from C9. The capacitance value of C9 coupled with the resistance in its charging path should make an RC product about 1/2 the time duration of the input pulse into C8 so that C9 can charge to the peak amplitude; lacking this, the constant amplitude input pulse into C8 would have to embody a constant width to insure that timing capacitor C9 receives a constant charge for each received pulse.

The resettable monostable of Figure 3 consumes approximately 20 milliwatts of power and has been fabricated in welded modular form on a production basis.

## CONSTANT-AMPLITUDE PULSE GENERATOR

The pulse generator of Figure 2 is one of a family of new low-power tunnel-diode pulse generators developed for use in equipment intended for deep-space particle measurement. This particular pulse generator will generate an output pulse of fixed duration on the leading edge of an input pulse whenever its amplitude exceeds a preset threshold level.

For additional information see NASA TN D-3558.