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STUDY OF COLD SUBSTRATE DEPOSITION OF THIN FILM PASSIVE ELEMENTS

By Donald R. Schoonover

January 1968

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Electronics Research Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Isaac Lagnado
Technical Monitor
NAS 12-561
Electronics Research Center
575 Technology Square
Cambridge, Massachusetts 02139

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ABSTRACT

Thin film resistors and capacitors having various material compositions were fabricated on glass substrates and on oxidized silicon substrates using the Librascope cold substrate deposition process. Capacitors of 10^5 picofarads per square inch deposited on glass substrates met all design goal requirements of tolerance, temperature coefficient, breakdown voltage and high temperature life. Capacitors fabricated on oxidized silicon wafers met all design goals with exception of the specified breakdown voltage, due to pinholes in the thermally oxidized wafer surface. Resistors of 10^3 ohms per square met all design goal requirements of tolerance, temperature coefficient, noise and high temperature life. Resistors having larger sheet resistances (10^4 and 10^5 ohms per square) were reproducibly deposited, but, when subjected to a post-deposition burn-in (to stabilize the films prior to life tests at 350°C), experienced changes in characteristics such that their final values could not be reproducibly achieved within design goal tolerances.

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STUDY OF COLD-SUBSTRATE DEPOSITION OF THIN FILM PASSIVE ELEMENTS

By Donald R. Schoonover

General Precision Systems, Inc.
Librascope Group
Glendale, California

INTRODUCTION AND SUMMARY

The purpose of this program was to investigate the feasibility of fabricating thin film resistors and capacitors with more stringent design goal requirements than those outlined in a previous contract: NAS 12-109, "Study of Cold-Substrate Deposition of Thin Film Passive Elements", October 1966. The primary differences between the two contracts were an increase in specific capacitance, more emphasis on the higher ohms per square resistance ranges, more severe temperature cycling, and an extension of fabrication techniques to formation of similar passive elements on passivated silicon substrates.

Materials investigated during the performance of this program were, primarily, standard materials employed in current thin film technology for the fabrication of passive components. Specifically, the materials chiefly used for the resistors were Tophet-C and germanium-chromium mixtures, and for capacitors were silicon monoxide and aluminum oxide dielectrics.

Resistors having a specific resistance of 10^3 ohms per square as well as capacitors having a specific capacitance of 10^5 picofarads per square inch fabricated on Corning No. 7059 glass substrates met all design goals. These same design goals, with the exception of the specified minimum breakdown voltage, were met for capacitors fabricated on oxidized silicon substrates. The reduced breakdown voltages were probably due to pinholes present in the thermally oxidized silicon.

Capacility of the deposition process to fabricate resistors in the range of 10^4 and 10^5 ohms per square was demonstrated by reproducible deposition of resistors on glass and on oxidized silicon substrates. However, large resistance changes occurred during the stabilization treatment after the deposition. These changes resulted from contamination of the resistive film by the substrate or overcoating material, or by the occlusion of residual gas

molecules during deposition, or a combination of these. The effect of the contaminants was amplified by the island structure of these extremely thin films.

PASSIVE ELEMENT FABRICATION

All resistors and capacitors were fabricated in a standard vacuum deposition system which employed Librascope's cold-substrate deposition process. These passive elements were fabricated on glass and oxidized silicon substrates and were to conform with the design goal requirements stipulated in Part A of the Appendix.

Resistor Fabrication

The geometrical pattern selected for the thin film resistors consisted of a set of four rectangularly-shaped elements arranged in a rectangular array. The detailed description of the processing sequence for preparing and testing the resistors, which follows, is shown schematically in Figure 1.

a. Substrate preparation

Two types of substrate were used for the depositions. The first type was Corning No. 7059 which is an alumino-boro-silicate glass. This substrate material was selected because, other than for a 1-2μ waviness developed in the surface during the high-temperature drawing of this glass, it has a relatively smooth surface. This characteristic is undoubtedly more critical in capacitor fabrication than in resistor fabrication. The other type of substrate was p-type (boron-doped) silicon wafer which had a 5000 A^{o} thermally oxidized surface, a 111-orientation, a resistivity of 0.93-1.08 ohm-cm, and were 6 - 8 mils thick.

Prior to deposition, all substrates were subjected to a thorough cleaning procedure. The first stage of cleaning consisted of degreasing of the substrate surfaces in both the liquid and condensing vapors of trichloroethylene. More specifically, a substrate was submerged and agitated in hot, almost boiling, trichloroethylene. The substrate was then suspended directly above the liquid surface of the boiling trichloroethylene. The vapor of the trichloroethylene condensed on the substrate and droplets of the trichloroethylene fell back into the boiling liquid. After approximately three minutes of vapor degreasing, the substrate was removed from the vapor and stored in a dust-free, dry enclosure.

The second stage of cleaning differed for the two types of substrates used in this program. The second stage of cleaning for the glass substrates was performed after the substrate had been placed in the deposition system and the chamber evacuated. By establishing a glow discharge in a residual argon atmosphere, the substrate was subjected to ion cleaning by ion bombardment for a minimum of thirty minutes. To avoid damaging the oxide layer of the passivated silicon wafers, cleaning by ion bombardment was

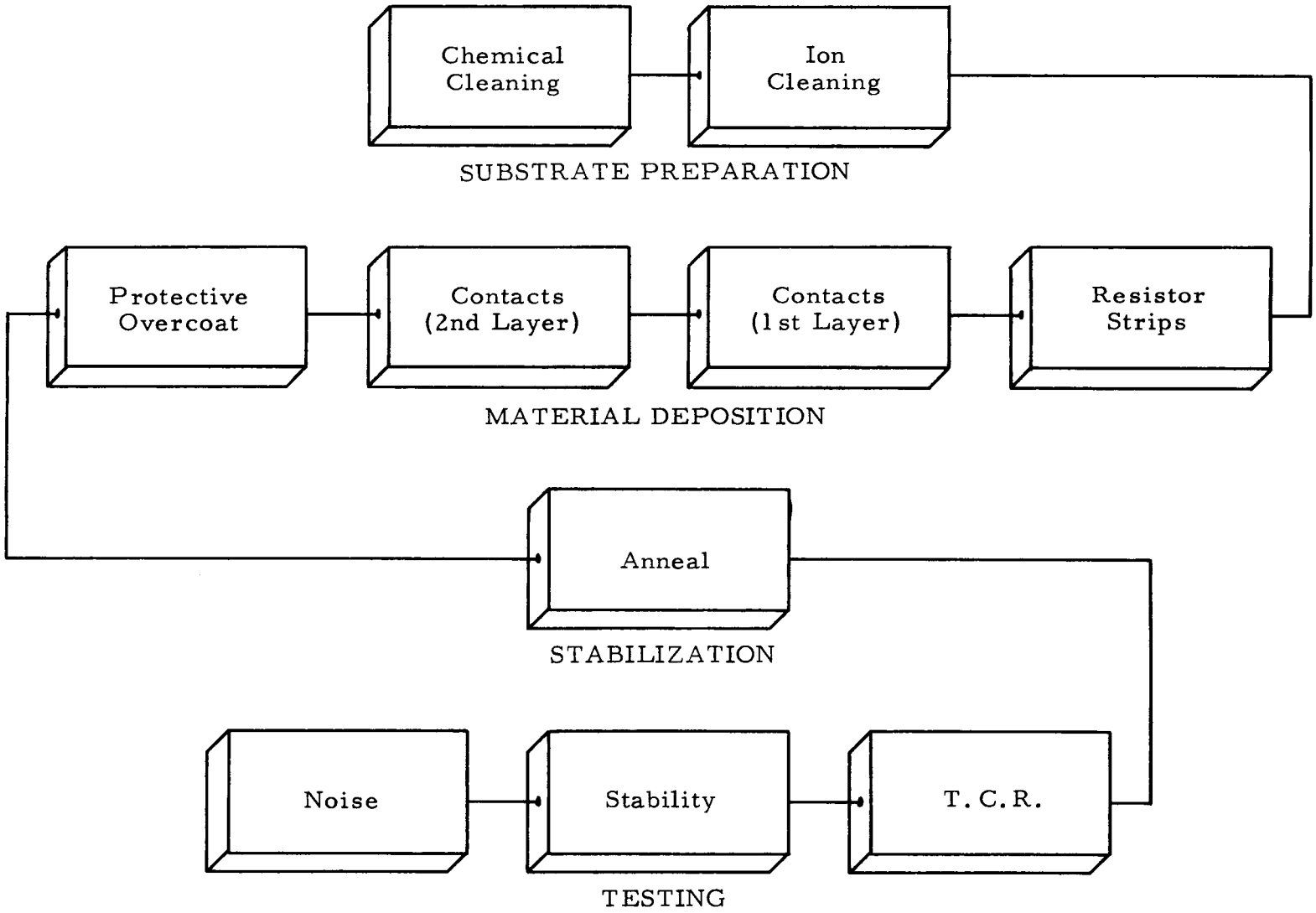

Figure 1. Sequence of Resistor Fabrication, Stabilization and Evaluation

eliminated. As a substitution for the ion cleaning of these substrates, the evacuated chamber containing an oxidized silicon substrate was purged with argon for five minutes prior to deposition to partially degas the substrate surface.

b. Material deposition

To minimize adsorption of residual gas molecules to the cleaned substrate surface, pump-down of the chamber and deposition of the resistors immediately followed the ion cleaning. This was necessary to insure good adherence of the film to the substrate and to minimize adverse effects caused by interaction of the adsorbed residual gas molecules with the resistor film during high temperature cycling of the resistors. To further minimize contamination by adsorption at intermediate stages of the fabrication, material depositions were conducted without breaking vacuum until all fabrication steps for a given set of elements had been completed. The fabrication to completion without breaking vacuum was facilitated by using a unique, specially designed metal mask and mask changer. A diagram of the metal mask used for these depositions is shown in Figure 2. The mask was constructed from a 0.020" sheet of No. 300 series stainless steel and consisted of three regions. The edges of the mask openings were "stepped" to a 0.004" lip (see inset in Figure 2) to minimize mask shadowing of the substrate. The mask changer was designed to permit longitudinal movement of the mask by external, mechanical controls so that any one of the three regions of the mask (see Figure 2) could be positioned for deposition of the desired pattern, or the mask could be completely removed during ion cleaning. The mask and mask changer were designed so that both resistors and capacitors could be fabricated without modification of the mask or of the mask changer.

For the fabrication of resistors, the metal mask was positioned initially so that Region A (see Figure 2) was directly beneath the substrate. The resistive material was then deposited on the substrate in the form of two long strips. After the desired amount of resistive material was deposited, the mask was repositioned so that Region B was directly below the substrate. In this position, the mask permitted deposition of the material for the electrical contacts. By the combination of the resistive film geometry and contact film geometry, resistors with approximately two-square configurations were obtained. A pictorial sketch of a set of fabricated resistors (before the deposition of the overcoating material) is shown in Figure 3. The contact material was actually much thicker relative to the thickness of the resistance material than that displayed in Figure 3. The deposition of contacts on the resistive strips rather than under the resistive strips avoids the formation of "elbows" in the thin resistive films at the junction of the contacts. The presence of these "elbows" contributes significantly to unreliable and unpredictable performances during the subsequent temperature cycling. The final material deposition was through Region C of the mask which permitted a protective overcoating film to be placed over the entire resistor pattern, leaving only the ends of the contacts exposed for testing purposes.

Resistive Films.--The resistive material was deposited in the form of two narrow strips through Region A (Figure 2) of the metal mask. The

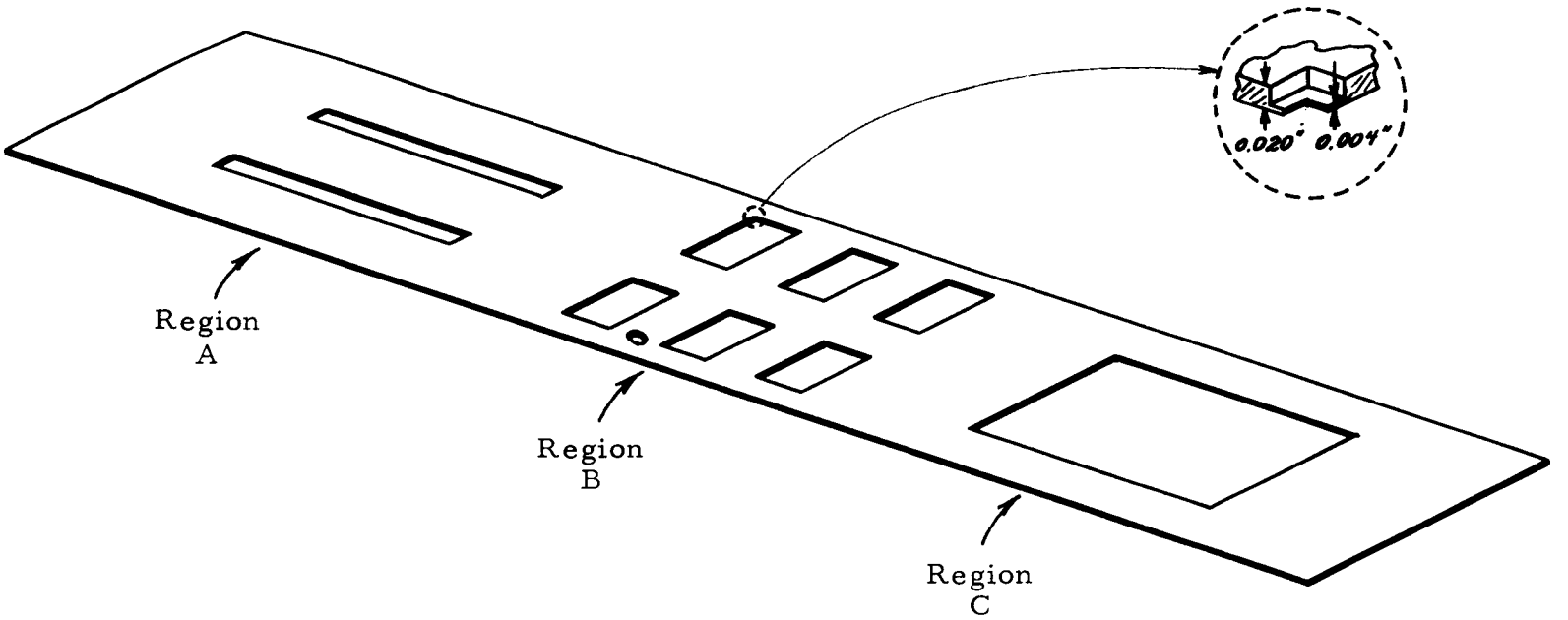

Figure 2. Metal Mask for Material Deposition

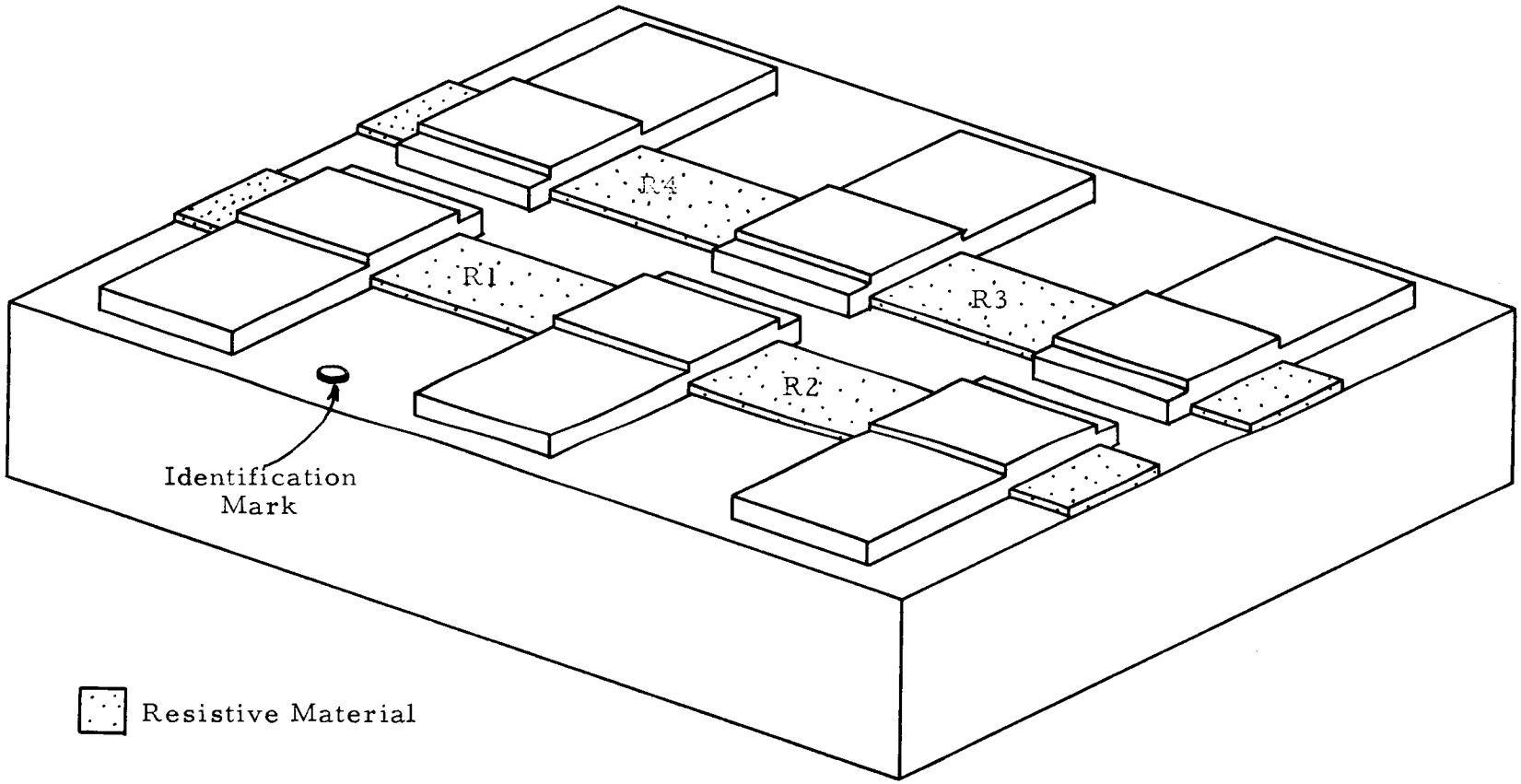

Figure 3. Set of Four Resistors on Substrate (without overcoating material)

duration of deposition was determined by monitoring the resistance value of another resistor which was being deposited simultaneously and which was positioned immediately adjacent to the mask changer at an equivalent distance from the material source. For all resistor depositions, including those on oxidized silicon, the monitor was a 1/2" x 3/4" Corning No. 7059 glass substrate with predeposited gold contact pads which were spaced so that one square of resistance area was exposed to the condensing vapor of the resistive material. A bridge network external to the deposition chamber was electrically connected to the monitor. The bridge network enabled the system operator to select the ohms-per-square value of the resistive strips by manipulating the external controls of a shutter assembly. This shutter was positioned between the material source and the substrate, permitting accurate control over the amount of material deposited on the substrate.

Electrical contacts. -- The electrical contacts were formed by depositing through Region B (Figure 2) of the metal mask. In most cases, in order to prevent or reduce the possibility of excessive stressing at the film-contact junction, which would have occurred if dissimilar materials were used, the material used for the electrical contacts was the same as that used for the resistive strips. The electrical contacts were of sufficient thickness so the resistance of these contacts were relatively negligible compared to the resistance of the two-square resistors. In order to provide a good, weldable structure, a layer of a selected material was sometimes deposited on the electrical contacts. Careful consideration was given to the selection of this material to avoid altering the resistor characteristics caused by diffusion of this second layer material into the resistive material at the elevated temperatures specified for this program. This problem was especially pronounced with gold, which was initially used for the sample fabrication. When the diffusion problem was recognized, aluminum and Tophet-C were substituted for gold. External electrical connections to the deposited contacts were realized with beryllium-copper pressure contacts or with parallel-gap welded leads.

Protective overcoat. -- A protective, overcoating material was deposited through Region C (Figure 2) of the metal mask. Deposition was continued until sufficient material was deposited to provide a continuous layer which completely covered the entire resistor pattern, with the exception of the tips of the electrical contacts. Except for the few sets which received aluminum oxide, silicon monoxide was selected as the overcoating material for the depositions.

c. Stabilization Procedure

In order to meet the life test design goal requirement of less than $\pm$ 2 percent drift after 100 hours at 350°C, the resistors were subjected to a post-deposition annealing treatment. This annealing was accomplished by placing the resistors in an oven at room temperature and, to avoid thermal shock, slowly increasing the oven temperature to the annealing temperature over a two-hour time interval. After maintaining the oven at the annealing temperature for several hours, the power to the oven was disconnected, allowing the resistors inside the oven to slowly return to room temperature.

Capacitor Fabrication

This section of the report presents the fabrication and stabilization procedures followed in the preparation of the capacitors. The chronological sequence followed in preparation, stabilization and testing of the capacitors is shown in Figure 4. Procedures followed for substrate preparation and for stabilization by a post-deposition annealing treatment are essentially the same as those used for fabricating resistors.

a. Material deposition

All processing steps required to fabricate a set of capacitors on a substrate were conducted without breaking vacuum. These capacitors were fabricated using the same metal mask as that used for fabricating the resistors (see Figure 2). The fabrication function of each region of the mask, however, was largely different from that when fabricating resistors. For the capacitors, the mask was first positioned so that Region A was beneath the substrate. Conductive material was then deposited on the substrate in the form of two long strips which served as the bottom electrodes. The mask was then repositioned so that approximately two-thirds of Region C was directly below the substrate. In this position, the capacitor dielectric was deposited on the substrate (see Figure 5). The mask was then positioned so that Region B was directly below the substrate and the counter electrodes were deposited as shown in Figure 5. Although used for only a few sets of capacitors, a protective overcoat was formed by placing Region C of the metal mask directly beneath the substrate and depositing an overcoat similar to that used for the resistor pattern.

Electrical contacts. -- The two narrow conductive strips which served as the bottom electrodes were made thick enough to form continuous, low-resistance current paths, but excessive thickness was avoided in order to minimize the possibility of developing a break in the dielectric material. If such a break occurred, then the counter electrode could make direct electrical contact with the bottom contact and thereby short out the associated capacitor. The thickness of the counter electrodes was not considered critical as long as a low-resistance current path was obtained. With the deposition configuration used for fabricating capacitors, the two capacitors on each of the two conductive strips shared a common terminal. Therefore, electrical connection to capacitor 1 was obtained through contacts C_1 and C_{12} (see Figure 5), to capacitor 2 through contacts C_2 and C_{12}, etc.

Dielectric films. -- The mask changer was designed in such a way that the position of the metal mask relative to the position of the substrate could be adjusted by means of an external mechanical control. This permitted placement of the mask so the dielectric material could be deposited on the substrate in such a manner that the subsequent counter electrode deposition furnished both the "plates" for the capacitors and pads to reinforce the contact areas of the thin bottom electrodes. The duration of the dielectric deposition was controlled by monitoring the thickness of the deposited dielectric material

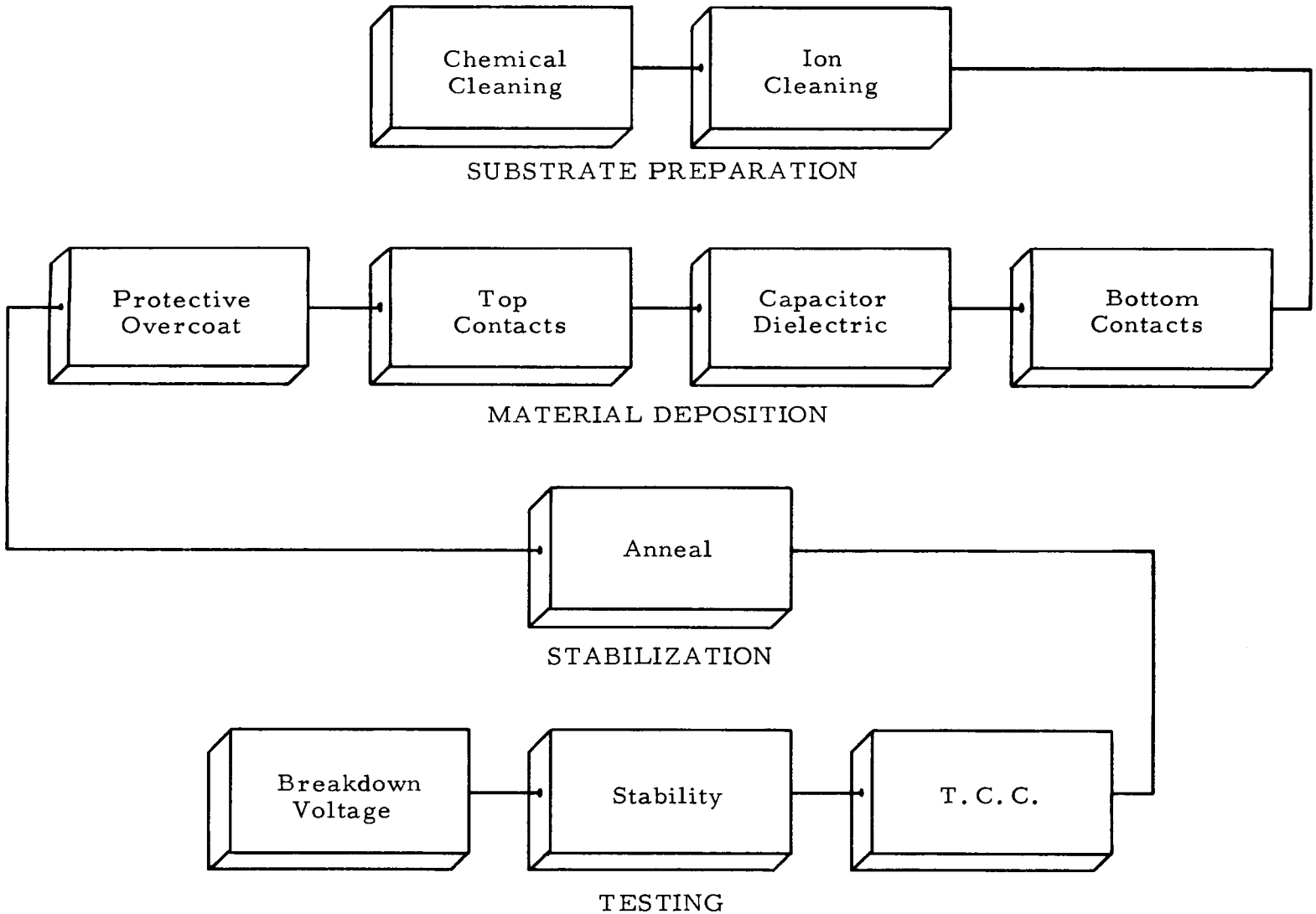

Figure 4. Sequence of Capacitor Fabrication, Stabilization, and Evaluation

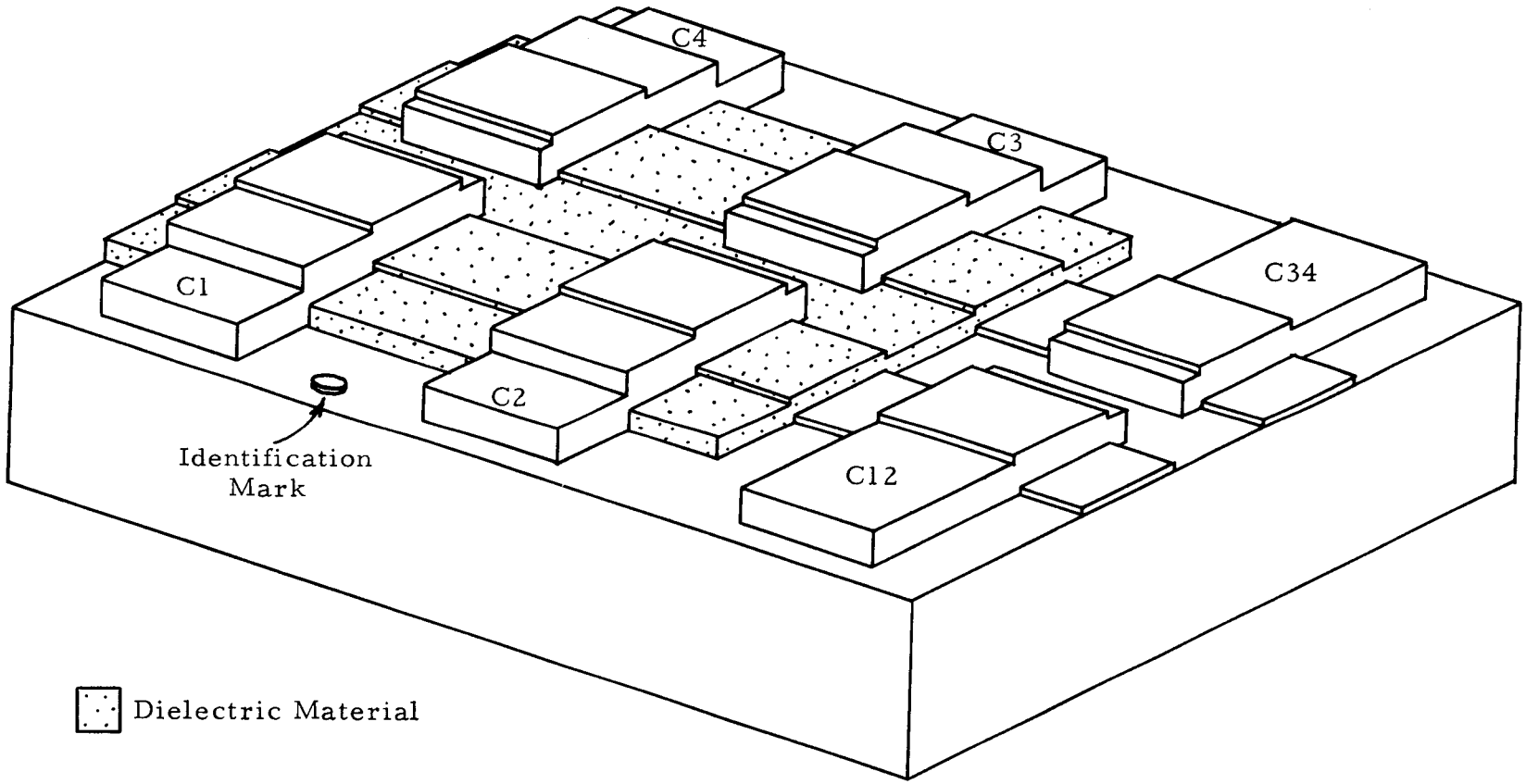

Figure 5. Set of Four Capacitors on Substrate (without overcoating material)

with a quartz crystal oscillator. The crystal for the oscillator was positioned immediately adjacent to the capacitor substrate during deposition. The supporting fixture for the crystal was arranged so that a linking mechanism between the support and the mask changer permitted only the dielectric material to be deposited on the crystal.

PASSIVE ELEMENT TEST DATA

Resistor Test Data

The data obtained for the individual resistors fabricated in conducting this project are given in Appendix B. In listing the resistors in this Appendix, identification is provided by listing the substrate possessing that resistor (e.g., R4) followed by the number of the resistor on that substrate as given in Figure 4 (e.g., R4-2). The specific resistance (ohms per square) for a given resistor was calculated by dividing the measured resistance for that resistor by the number of squares in that resistor. For a resistor with rectangular geometry, the number of squares in that resistor is the length of the resistor (distance between electrical contacts), ℓ, divided by the width, w, or

$$\text{number of squares} = \frac{\ell}{w}$$

Physical dimensions and the number of squares for each of the four resistors of a typical set fabricated on a substrate are given in Table I (see Figure 6)

TABLE I
PHYSICAL DIMENSIONS OF RESISTOR ELEMENTS

Resistor	Number of Squares
1	0.1286/0.0604 = 2.13
2	0.1292/0.0606 = 2.13
3	0.1304/0.0615 = 2.12
4	0.1297/0.0614 = 2.11

Various material combinations for the resistive, contact, and protective overcoating films were investigated. The combinations are listed in Table II.

The resistors in Groups I through IV and Group XIII had Tophet-C (Registered Trademark, W. B. Driver Co.) as the resistive material. Tophet-C is a nickel-chromium-iron alloy comprised of 61% Ni, 24% Fe, and 15% Cr. Bulk values of resistivity and temperature coefficient of resistance

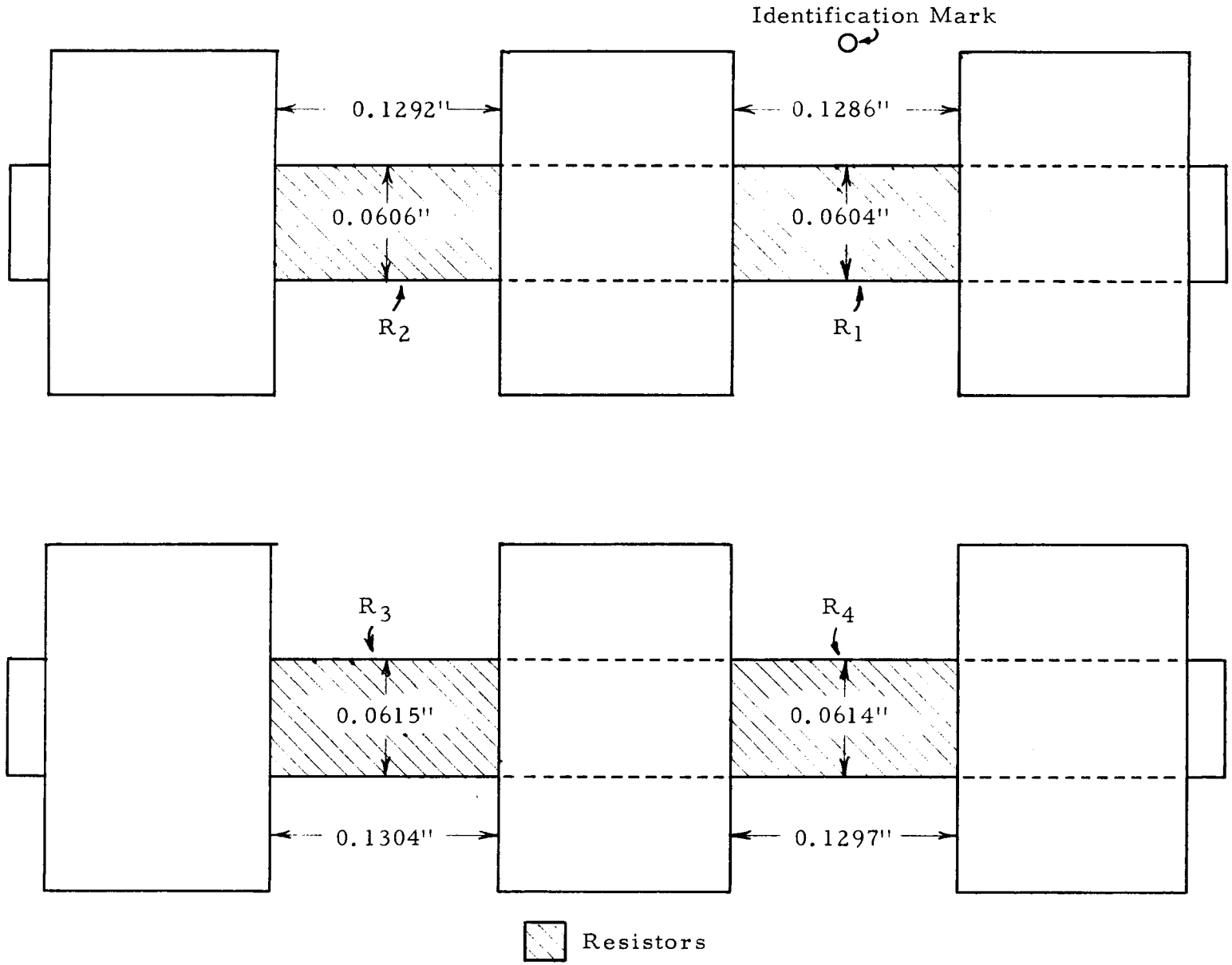

Figure 6. Physical Dimensions of a Typical Set of Fabricated Thin Film Resistors

(T.C.R) for this material are 112 micro-ohm-cm and +130 ppm/°C (over the temperature range 0-100°C), respectively.

TABLE II
MATERIAL COMBINATIONS OF FABRICATED RESISTORS

Group	Materials			
	Substrate	Resistive	Contact	Overcoat
I	Corning No. 7059	Tophet-C	(R)* + Au	SiO
II	"	"	(R)* + Al	"
III	"	"	Top-C	"
IV	"	"	"	Al_2O_3
V	"	L.T.C.	L.T.C.	"
VI	"	Constantan	(R)* + Al	SiO
VII	"	Hafnium	Al	"
VIII	"	1 Cr 2 Ge	(R)* + Al	"
IX	"	1 Cr 1 Ge	"	"
X	"	2 Cr 1 Ge	"	"
XI	"	4 Cr 1 Ge	"	"
XII	"	9 Cr 1 Ge	"	"
XIII	Oxidized Si	Tophet-C	(R)* + Al	"

*indicates that the contacts had a two-layered structure, the bottom layer of which was the same as the resistive material.

The resistors in Group V were fabricated with L.T.C. (Sigmund Cohn Corp. Trademark; U.S. Pat. 2,840,468) as the resistive material. L.T.C. is comprised of Au 65% -Ni -Cr which has a bulk resistivity of 98 micro-ohm-cm and a T.C.R. of approximately +10 ppm/°C (0-100°C).

The resistors in Group VI employed a copper-nickel alloy, Constantan (Cu 55% - Ni 45%), as the resistive material. Values of resistivity and T.C.R. for bulk Constantan are 49 micro-ohm-cm and +20 ppm/°C (0-100°C), respectively.

The resistors of the remaining material groupings shown in Table II were formed from mixtures of chromium and germanium. These two materials were selected for the resistive material, not only because they are continuously miscible with each other, but also because other investigators in the field have reported that a mixture of these two materials evaporates without fractionation, providing a depositant which has a composition consistent with that of the material source. Since chromium is basically metallic and germanium is semimetallic, several different mixtures by atomic percent of chromium to germanium were investigated in the event that a minimum T.C.R. value over the specified temperature range might be displayed by some optimum composition of these two elements.

Initially, silicon monoxide was used for the overcoating material. However, resistors in the 10^4 and 10^5 ohms per square category exhibited unacceptably large, irreversible changes in resistance during the post-deposition annealing treatment. In the event that the silicon monoxide was interacting with the resistive material, aluminum oxide was introduced as another possible candidate for the protective overcoat. When no significant difference in resistor characteristics due to the difference in overcoating material was observed, silicon monoxide was used for the overcoating material in all subsequent depositions.

a. Uniformity of deposition

The criterion used to evaluate the uniformity of resistor values on any given substrate was the magnitude of the relative range of the resistance values on that substrate, $\overline{R}$. where

$$\text{Relative Range} = \frac{\text{Range}}{\text{Average Resistance}} = \frac{R_L - R_S}{\overline{R}}$$

Here, R_L and R_S represent the respective largest and smallest resistor values on a substrate. This method of evaluating uniformity not only takes into account variations in deposited film thickness but also non-uniformities introduced by substrate defects, fractionation, and any other parameters which affect the uniformity of the operational characteristics of the passive elements. After determining the relative range before anneal for each set of resistors on glass substrates, a distribution of these relative ranges without regard to material composition or ohms per square was determined. This was accomplished by determining the normalized frequencies of relative ranges within class intervals having equal widths of 0.1. The resulting distribution is shown in Figure 7(a). The distribution characteristics obtained for resistors fabricated on oxidized silicon substrates are presented in Figure 7(b). Comparison of these two graphs reveal that resistors deposited on oxidized silicon substrates have smaller variation in specific resistance over a given substrate than those deposited on glass substrates.

In order to evaluate whether the relative range for a given substrate was related to the magnitude of the specific resistance of elements on that substrate, another distribution was determined in the following manner:

i) Sets of resistors were grouped on the basis of the magnitude of the average resistance of the set;

ii) Average relative range for all sets within each group was then plotted as a function of average resistances of these groups.

Figures 8(a) and 8(b) show the resulting distributions obtained for resistors on glass and on oxidized silicon substrates, respectively. The midpoints of

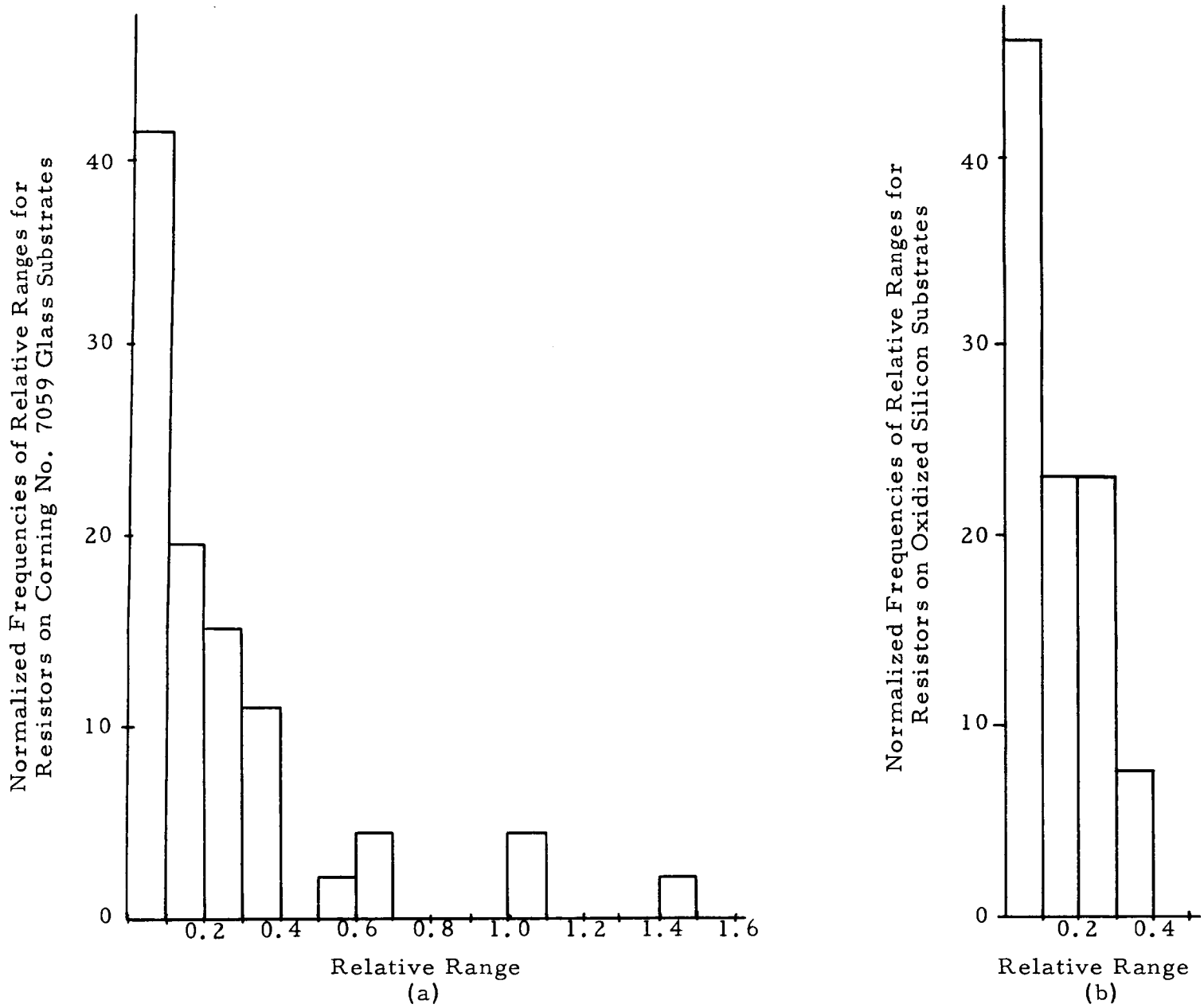

Figure 7. Distribution of Uniformities for Substrates Having Resistors on (a) Corning No. 7059 Glass and on (b) Oxidized Silicon Substrates

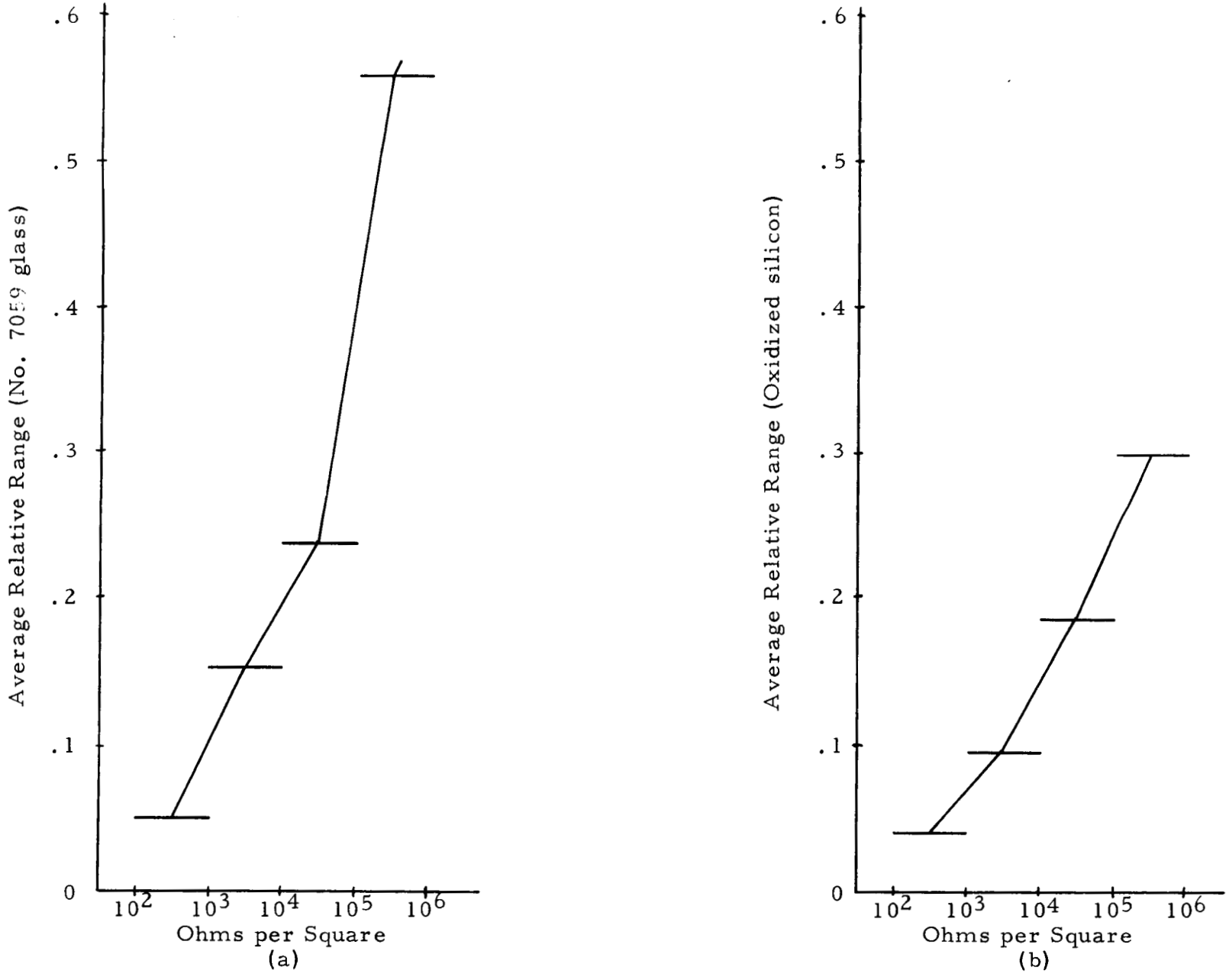

Figure 8. Distribution of Average Uniformity as a Function of Ohms Per Square for Resistors on (a) Corning No. 7059 Glass and on (b) Oxidized Silicon Substrates

the groups were connected to indicate the trend revealed by these distributions. The graphs in Figure 8 show a definite dependency of uniformity, as determined by the relative range, on ohms per square. Also, resistor uniformity is better on oxidized silicon than on No. 7059 glass substrates over the entire range from 10^2 to 10^6 ohms per square.

In order to meet the design goal requirements for high temperature stability, the resistors required a post-deposition annealing treatment. During this anneal, the resistors underwent an irreversible change in specific resistance. Plots of the ohms per square after anneal as a function of ohms per square before anneal are given in Figures 9 and 10 for the resistors in Groups I and XIII, respectively. Figure 9 reveals that non-stabilized resistors having specific resistances less than approximately 7×10^3 ohms per square decreased in magnitude during the anneal. If there had been no change in resistance during the anneal, all points would have fallen on the dotted line in Figure 9. The magnitude of change in resistance during anneal was larger for increasing resistance above 7×10^3 ohms per square. In fact, the 10^4 and 10^5 ohms-per-square resistors underwent a positive change of many orders of magnitude during annealing, with the magnitude of specific resistance after anneal being largely unpredictable. T.C.R.'s (temperature coefficient of resistance) measured for the resistors which underwent large changes during the anneal were negative, indicating conduction characteristics of an insulator. This suggests that the resistive films were partially, or totally, oxidized during the post-deposition annealing treatment.

Figure 10 reveals that the large positive change in specific resistance which occurred for resistors on glass did not occur for resistors on oxidized silicon substrates. Most of the resistors exhibited negative changes in resistance during the anneal, with an increasing scatter in the resistance change with increasing ohms-per-square resistances.

As an insufficient amount of data were available for the other material groupings, no graphical presentation of their characteristics was attempted. However, the available data suggests that curves similar to that in Figure 9 rather than that in Figure 10 would be obtained. Also, because of the large variation in resistance changes during the anneal, no attempt was made to determine the uniformity after the post-deposition annealing treatment.

b. Temperature coefficient of resistance

The temperature coefficient of resistance was determined by measuring the resistance of a resistor on a given substrate when the substrate had

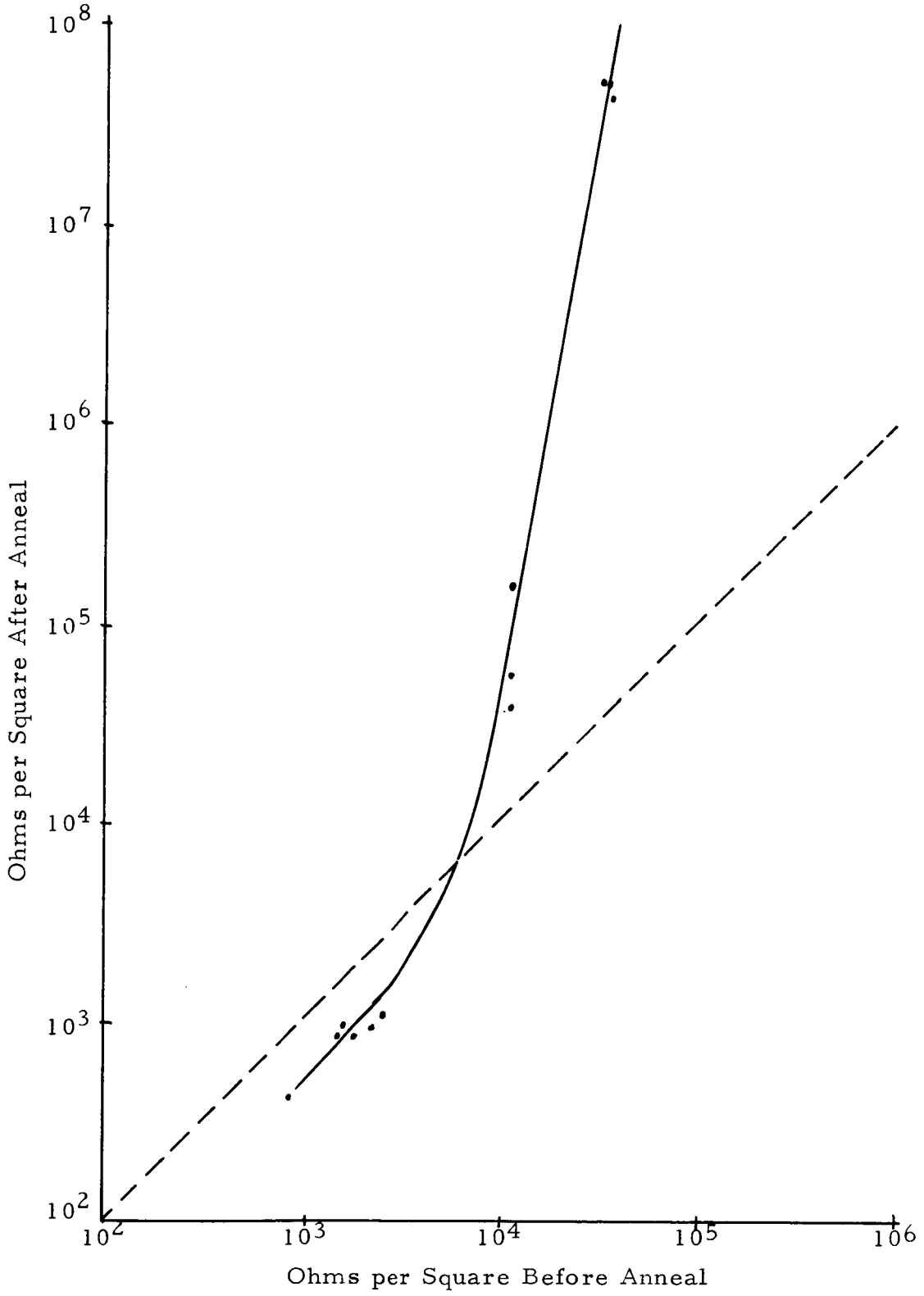

Figure 9. Specific Resistance After Anneal vs. Specific Resistance Before Anneal for Resistors in Group I

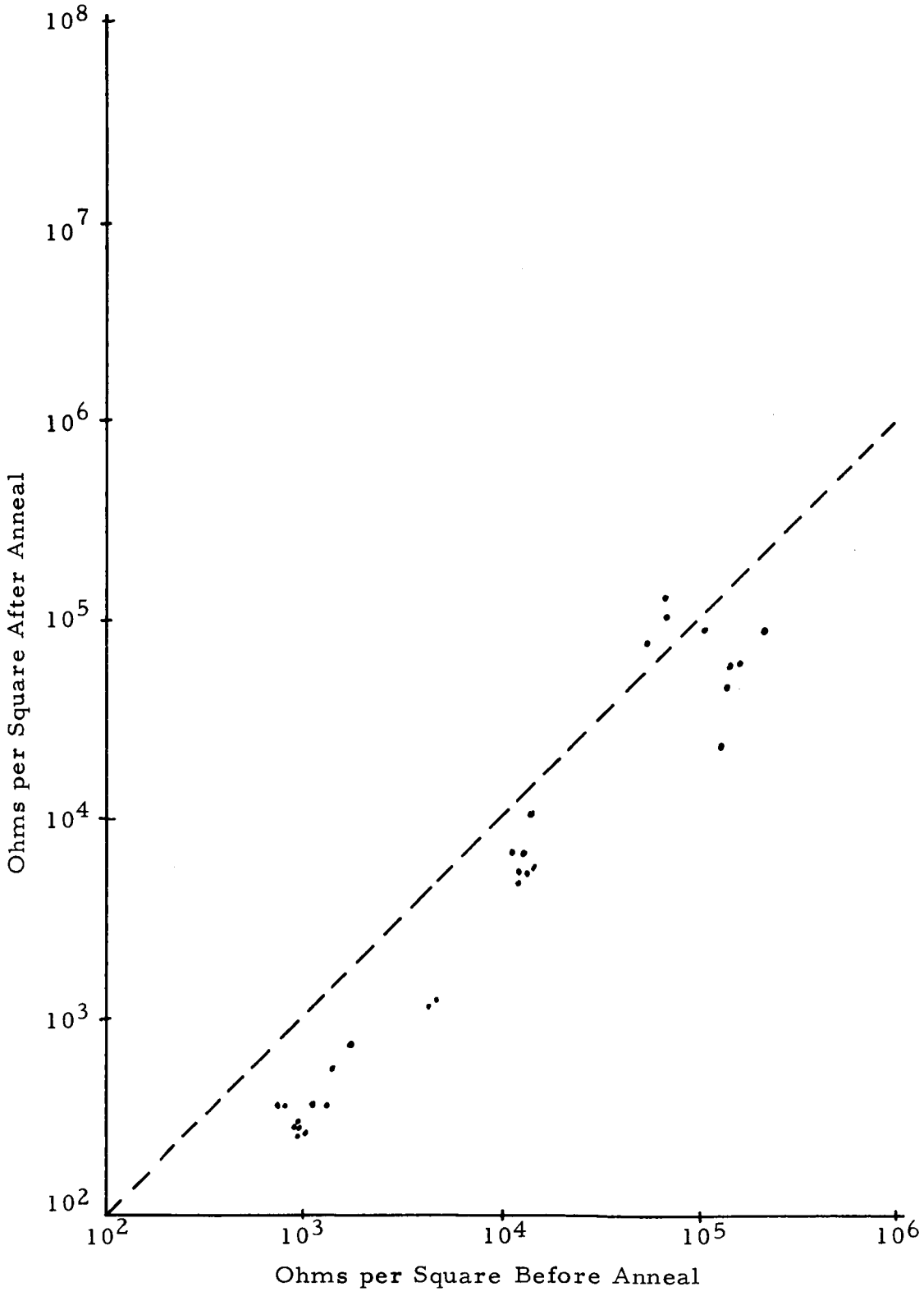

Figure 10. Specific Resistance After Anneal vs. Specific Resistance Before Anneal for Resistors in Group XIII

reached an equilibrium temperature in an environmental chamber. The resistance of the same resistor was then measured at some other temperature under similar equilibrium conditions. Then, the average temperature coefficient of resistance (T.C.R.) over the range between these two temperatures is

$$\text{T.C.R.} = \frac{\Delta R}{R_o} \frac{10^6}{\Delta T} \text{ ppm/}^{o}\text{C}$$

where ΔR is the difference between the two measured resistances, ΔT is the difference between the two equilibrium temperatures measured in degrees Centigrade, and R_o is the resistance of the resistor at room temperature (+23°C). The factor of 10^6 converts the T.C.R. to units of parts per million per degree Centigrade (ppm/°C). The T.C.R.'s which were determined are listed with their corresponding resistor in Appendix B. Although the lowest temperature specified in the design goal requirements was -30°C, corresponding to the temperature of liquid CO_2, a liquid CO_2 chamber was not currently available. Therefore, dry ice (solid CO_2) was used and -70°C was taken as the low temperature value rather than -30°C, as originally specified. The sublimation temperature of dry ice is actually -78.5°C. However, for the fixturing of the T.C.R. test setup, the lowest temperature at which the substrate could be stably maintained was at -70°C. The magnitudes of the resistances were measured with a Shallcross No. 6350 Wheatstone bridge and auxiliary equipment.

The general trend in the measured values of temperature coefficient of resistance was that resistors which displayed positive changes in resistance during the post-deposition annealing treatment almost without exception had negative T.C.R.'s. This was explained in the preceding section as the results which would be expected if oxides permeated the resistive films during stabilization, causing the resistors to display conduction characteristics of an insulator. Both negative and positive T.C.R.'s were measured for resistors undergoing small negative changes in resistance during the anneal, while only positive T.C.R.'s were observed for resistors with large negative changes. These positive T.C.R.'s suggest a predominance of metallic conduction. The magnitude of the T.C.R. values measured for resistors having mixtures of chromium and germanium for the resistive material increased for increasing concentration of germanium relative to chromium.

c. Stability

To determine the high temperature stability of a thin film resistor, the resistance values measured at room temperature before and after the resistors had been subjected to a temperature of 350°C for 100 hours were compared. The drift expressed as a percent was

$$\text{Percent Drift} = \frac{\Delta R}{R_B} (100)$$

where ΔR was the change in resistance during the heat treatment and R_B was the resistance before the treatment.

The magnitude of the measured drift depended on the length of the post-deposition annealing treatment. Results of stability tests performed on a set of resistors which had undergone a 5-hour anneal at 400°C and on another set which had undergone a 20-hour anneal at 400°C are given in Table III. The values indicate that a 5-hour anneal does not provide sufficient stabilization. The 20-hour anneal placed the drift for resistors on substrate No. R5 within the design goal requirements.

TABLE III
STABILITY vs. ANNEAL TIME

Resistor	Anneal Time	Percent Drift
R6-1	5 hours	+9.0
R6-2	5 hours	+9.0
R6-3	5 hours	+10.0
R6-4	5 hours	+8.9
R5-1	20 hours	+0.3
R5-3	20 hours	+1.0
R5-4	20 hours	+0.7

Comparing the drifts by material groupings (see Table II) without regard to the magnitude of specific resistance, the stability values obtainable from the available data are given in Table IV.

TABLE IV
PERCENT DRIFT DURING RESISTOR STABILITY TEST

Group	Number of Resistors	Percent Drift
I	15	+0.3 ± 0.4
IV	4	-0.8 ± 8.0
VI	4	-0.5 ± 1.3
VIII	4	+1.9 ± 0.9
IX	7	+2.4 ± 3.7
X	11	-1.1 ± 2.6
XI	10	+1.5 ± 0.8
XII	8	-0.3 ± 2.2
XIII	42	+2.0 ± 3.9

The numbers in the second column of Table IV designate the amount of data used to determine the values given in the third column. The values given in

the third column are the average percent drift, followed by the standard deviation as an indication of the scatter of values for the percent drift. The results shown are far from conclusive due to the small amount of data available for these calculations.

d. Noise

The resistor noise in a decade, N_R, was determined by means of the equation

$$N_R = K \frac{R_x + R_L}{R_L} \sqrt{N_T^2 - N_S^2}$$

where R_x is the resistance of the test specimen, R_L is the load resistance, N_s is the system noise, N_T is the total noise, and K is a multiplier which converts open circuit resistor noise voltage to noise per decade. The result obtained was then converted to db to the index of 1 microvolt per volt. The results of the noise tests which were conducted are presented in Table V.

TABLE V RESISTOR NOISE DATA				
Resistor	Ohms/Square	System Noise (μ V)	Total Noise (μ V)	Resistor Noise db (μV/V)
R9-1	873	.19	.195	-31
R9-2	881	.17	.19	-25
R9-3	853	.15	.155	-32
R9-4	953	.26	1.35	-1.2
R11-1	1095	.15	.20	-21
R11-2	1117	.165	.195	-23
R11-3	1094	.20	.27	-18
R11-4	1076	.15	.29	-16
R12-1	914	.22	.25	-22
R12-2	904	.225	.235	-27
R12-3	902	.175	.195	-25
R12-4	907	.23	.24	-27
R13-1	865	.25	.28	-22
R13-2	864	.20	.23	-23
R13-3	851	.23	.25	-24
R13-4	869	.21	.25	-21
R15-1	$.39 \times 10^5$	.225	.25	-5
R15-2	1.57×10^5	.195	.23	+7
R15-3	1.55×10^5	.25	.28	+7
R15-4	$.54 \times 10^5$	.235	.25	-5
R27-1	913	.20	.38	-14
R27-2	681	.21	.62	-9
R27-3	703	.30	1.0	-4
R27-4	905	.235	.255	-24
R33-1	8817	.235	.245	-19
R33-2	9089	.24	.45	-4
R33-3	8868	.175	.195	-17
R33-4	8692	.175	.185	-20

Capacitor Test Data

The grouping and data obtained for the capacitors fabricated in conducting this program are given in Appendix C. Only the values for those capacitors which survived the post-deposition annealing treatment are listed in this Appendix. Typical physical dimensions and the area of each of the four capacitors on a given substrate are given in Table VI (see Figure 11). The areas given in Table VI represent only that area where the counter electrode perpendicularly opposes the strip electrode. Any small contributions due to oblique, capacitive interaction are not included.

TABLE VI
PHYSICAL DIMENSIONS OF CAPACITOR ELEMENTS

Capacitor	Area (in^2)
C_1	$0.0604 \times 0.1226 = 7.405 \times 10^{-3}$
C_2	$0.0605 \times 0.1199 = 7.254 \times 10^{-3}$
C_3	$0.0615 \times 0.1201 = 7.386 \times 10^{-3}$
C_4	$0.0614 \times 0.1212 = 7.442 \times 10^{-3}$

The capacitance per unit area for a given capacitor on a substrate was obtained by dividing the measured capacitance by the corresponding area given in Table VI for that capacitor. The dielectric materials employed for fabricating capacitors were aluminum oxide (Al_2O_3), silicon monoxide (SiO), and combinations of these two materials in alternating layers. The analysis of the experimental test data was performed by classifying the capacitors into groups. The groups were selected according to the particular substrate-dielectric-conductor materials used for fabricating the capacitors on any given substrate (see Table VII). The reasons for

TABLE VII
CAPACITOR GROUPING FOR DATA ANALYSIS

Group	Materials		
	Substrate	Dielectric	Conductor
A	Corning No. 7059	Al_2O_3	Tophet-C
B	Corning No. 7059	Al_2O_3	Aluminum
C	Corning No. 7059	SiO	Aluminum
D	Corning No. 7059	Al_2O_3 + SiO	Aluminum
E	Oxidized Silicon	Al_2O_3	Tophet-C
F	Oxidized Silicon	Al_2O_3	Aluminum

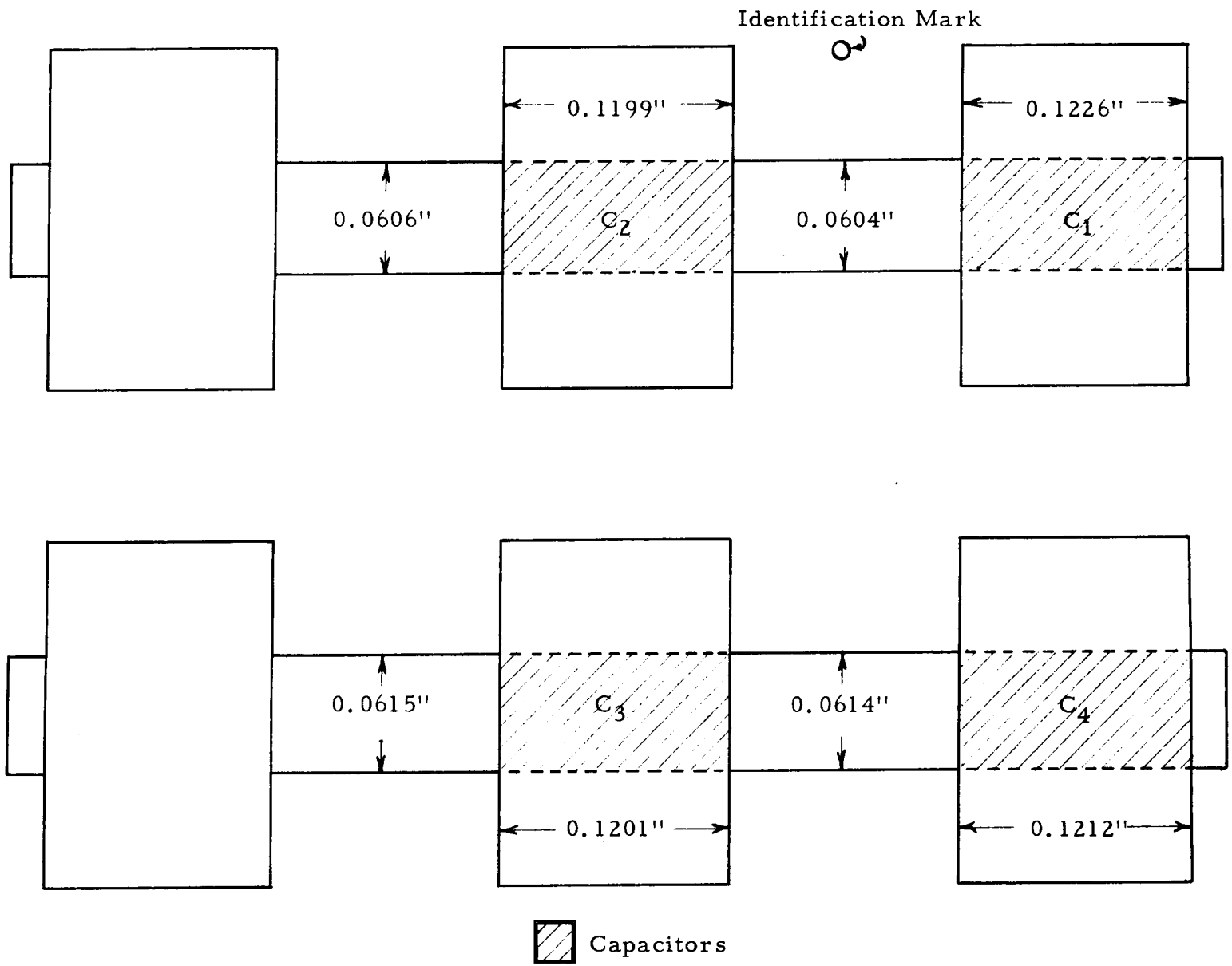

Figure 11. Physical Dimensions of a Typical Set of Capacitors

choosing these groupings were to establish the effects of a particular variable on the capacitor characteristics by maintaining other variables of the substrate-dielectric-conductor system unchanged. Specifically, significant differences in characteristics between capacitors of Group A and of Group B (Table VII) revealed dependence of characteristics on different conductor materials, differences between Groups B and C revealed effects of using different dielectric materials, and differences between Groups A and E revealed effects of using different substrate materials.

a. Uniformity of deposition

The relative range of capacitor values on any given substrate was taken as the criterion for evaluating the uniformity of capacitors on that substrate, where

$$\text{Relative Range} = \frac{\text{Range}}{\text{Average Capacitance}} = \frac{C_L - C_S}{\overline{C}}$$

Here, C_L and C_S refer to the respective largest and smallest capacitor value on the substrate. After calculating the relative range for each set of capacitors, the uniformity within each of the material groupings (see Table VII) was then determined. The resulting uniformities before the post-deposition annealing treatment are given in Table VIII. The values quoted in the Number of Substrates column indicate the amount of data used to obtain the values given in the Uniformity column. The first value given in the Uniformity column represents the average of all of the relative ranges for the sets of capacitors in that group. This is followed by the standard deviation of the relative ranges within that group, expressed as a plus-or-minus value, to give a measure of the scatter of the uniformities.

TABLE VIII
SUBSTRATE UNIFORMITY BEFORE ANNEAL

Group	Materials			No. of Substrates	Uniformity
	Substrate	Dielectric	Conductor		
A	Corning No. 7059	Al_2O_3	Tophet-C	5	.022±.012
B	Corning No. 7059	Al_2O_3	Aluminum	19	.021±.026
C	Corning No. 7059	SiO	Aluminum	5	.015±.005
D	Corning No. 7059	Al_2O_3 + SiO	Aluminum	6	.032±.028
E	Oxidized Si	Al_2O_3	Tophet-C	3	.204±.167
F	Oxidized Si	Al_2O_3	Aluminum	5	.30±. 60

In making the following comparisons, it was noted that in most cases the amount of data used for these calculations differed. Therefore, it should be emphasized that these observations may or may not be entirely accurate due to the small amount of data available for these calculations. Comparing Groups A and B in Table VIII, substrates with capacitors having aluminum

oxide dielectrics and Tophet C conductors have approximately the same uniformity as substrates having similar capacitors with aluminum conductors, but have a smaller spread in uniformities than the latter. Comparing Groups B and C in Table VIII, substrates with capacitors having silicon monoxide as the dielectric material appeared to have better uniformity and smaller spread in uniformities than substrates with capacitors having aluminum oxide as the dielectric material. The larger nonuniformity and larger spread in uniformity values shown for substrates with capacitors having layered dielectrics of aluminum oxide and silicon monoxide (Group D, Table VIII) could be due to a number of reasons but the difference is not really large enough to be considered significant. Comparing the values shown for Groups E and F with those of Groups A and B, respectively, the differences in average magnitude and in spread of uniformities for capacitors fabricated on oxidized silicon substrates as opposed to those fabricated on glass substrates are probably sufficiently large to be significant. An experiment was performed to determine whether the oxidized silicon substrates might be conducting a leakage current parallel to the desired current through a given capacitor. The six electrode pads obtained by depositing through Region C of the metal mask were deposited directly on an oxidized silicon substrate for this purpose. The measured capacitances between each pair of adjacent pads, which were common to one of the conductor strips in the capacitor array, were 382.0 and 390.4 picofarads. This magnitude of capacitance, which was too large for capacitance due to the close proximity of two adjacent pads, was due to conduction through the "capacitor" effectively formed by the oxide layer between the silicon substrate and the deposited pad, along the low resistance path formed by the bulk silicon, and back through the "oxide-layer-capacitor" formed beneath the adjacent pad. Therefore, since the oxidized silicon wafers displayed conduction through the substrate, any variation in the characteristics of the parallel leakage paths would contribute to the non-uniformity and spread of uniformity values. Also, a difference in quality of surface finish between the two types of substrates could affect the uniformity of capacitor values. The best uniformity before the post-deposition annealing treatment as measured by the relative range was displayed by Substrate No. C50 which had a relative range of 0.006; the worst uniformities before annealing were displayed by oxidized silicon substrates with capacitors having aluminum oxide dielectrics (Substrate No. C29 and No. C46, which had relative ranges of 0.36 and 1.37, respectively).

The uniformities of sets of capacitors after the post-deposition annealing treatment are given in Table IX. Comparing Tables VIII and IX, the uniformity relationships between the material groupings which existed after the post-deposition annealing treatment were essentially the same as those which existed before the anneal. The sets of capacitors appeared to be more uniform after the annealing treatment than they were before the anneal. The largest change in uniformity during the anneal appeared to be in Group E with capacitors on oxidized silicon substrates having aluminum oxide dielectrics and Tophet-C conductors.

TABLE IX SUBSTRATE UNIFORMITY AFTER ANNEAL					
Group	Materials			No. of Substrates	Uniformity
	Substrate	Dielectric	Conductor		
A	Corning No. 7059	Al_2O_3	Tophet-C	5	.016±.011
B	Corning No. 7059	Al_2O_3	Aluminum	14	.023±.017
C	Corning No. 7059	SiO	Aluminum	3	.017±.011
D	Corning No. 7059	Al_2O_3 + SiO	Aluminum	6	.024±.016
E	Oxidized Si.	Al_2O_3	Tophet-C	3	.098±.105
F	Oxidized Si	Al_2O_3	Aluminum	4	.39± .62

To determine the actual change in capacitance during the annealing treatment, the capacitance values measured after the anneal, C_A, were compared with corresponding values measured before the anneal, C_B. Thus, the capacitance change expressed as a percent was

$$\text{Percent Change During Anneal} = \frac{C_A - C_B}{C_B} (100)$$

The resulting values for each of the material groupings, given in Table X, reveal that the capacitors fabricated on glass and having aluminum oxide dielectrics changed least in specific capacitance during the post-deposition annealing treatment. Of these capacitors, those having Tophet-C conductors changed less than those having aluminum conductors. Capacitors on Corning No. 7059 glass substrates having silicon monoxide dielectrics displayed substantially larger capacitance changes during anneal, with still larger changes exhibited by capacitors on oxidized silicon substrates having aluminum oxide dielectrics. From the standpoint of reproducibility after anneal (least spread in values) capacitors on Corning No. 7059 glass substrates with

TABLE X PERCENT CHANGE IN SPECIFIC CAPACITANCE DURING ANNEAL					
Group	Materials			No. of Capacitors	Uniformity
	Substrate	Dielectric	Conductor		
A	Corning No. 7059	Al_2O_3	Tophet-C	18	-2.5± 1.8
B	Corning No. 7059	Al_2O_3	Aluminum	44	-3.4± 4.5
C	Corning No. 7059	SiO	Aluminum	11	-12.6± 3.3
D	Corning No. 7059	Al_2O_3 + SiO	Aluminum	21	-12.3± 4.4
E	Oxidized Si	Al_2O_3	Tophet-C	12	-29.0±25.4
F	Oxidized Si	Al_2O_3	Aluminum	15	-35.3±29.1

aluminum oxide dielectrics and Tophet-C conductors appeared to be the best of the material combinations tested. None of the sets of capacitors with aluminum oxide dielectrics and nickel conductors (four sets - No. C31 through No. C34) survived the post-deposition annealing treatment. Also, the two sets of capacitors on oxidized silicon substrates with silicon monoxide dielectrics and aluminum conductors (No. C48 and Co. C49) failed to survive the anneal.

A ninety-six hour shelf-aging test was conducted with two sets of capacitors. This test consisted of measuring the capacitance values immediately after fabrication by deposition, and remeasuring these same capacitors after ninety-six hours of shelf life. The two sets of capacitors fabricated for this test were designed to have one set of capacitance values within the design goals (No. C18) and one set with much larger values (No. C19). Both sets of capacitors were of material Group B. The measured capacitances and the resultant changes after 96 hours (Table XI) indicated that there was a relatively uniform, negative change in capacitance during the 96 hours following the deposition. This shift is of the same order of magnitude but is smaller than that normally observed during the post-deposition annealing treatment for Group B capacitors. After completion of the shelf-aging test, both sets of capacitors were subjected to the usual stabilization procedure (post-deposition anneal). During the anneal, the capacitors on substrate No. C18 showed a larger than usual capacitance change. Similarly to most other sets of capacitors fabricated with very high capacitance values, all of the capacitors on No. C19 failed by shorting during the annealing treatment.

TABLE XI
96-HOUR SHELF-AGEING TEST

Capacitor	Capacitance at Beginning of Test	Capacitance at Conclusion of Test	Percent Change
C18-1	732.0 pf	719.4 pf	-1.7
C18-2	712.0	700.2	-1.7
C18-3	716.2	706.6	-1.3
C18-4	730.9	717.1	-1.9
C19-1	3253 pf	3182 pf	-2.2
C19-2	3187	3114	-2.3
C19-3	3221	3150	-2.2
C19-4	3254	3187	-2.1

b. Temperature coefficient of capacitance

The temperature coefficient of capacitance (TCC) was determined by measuring the capacitance at the two end temperatures of a given temperature interval, and calculating the average change in capacitance per unit capacitance over that interval, or

$$TCC = \frac{\Delta C}{C_o} \frac{10^6}{\Delta T} \text{ ppm/}^oC.$$

where ΔC is the difference in capacitance measured at the two temperatures which differed by ΔT, and C_o is the capacitance at room temperature. The result is expressed in parts per million per degree Centigrade. The two temperature intervals employed in this project for evaluating the T. C. C. for capacitors were $+23^o \rightarrow +150^oC$ and $+150^o \rightarrow +250^oC$. The calculated values of T. C. C. for individual capacitors are given in Appendix C and, for the selected material groupings, are given in Tables XII and XIII. From these two tables, capacitors having silicon monoxide dielectrics appear to have the smallest temperature coefficient of capacitance and also have the smallest spread in T. C. C. Values.

TABLE XII
TEMPERATURE COEFFICIENT OF CAPACITANCE ($+23^o \rightarrow +150^oC$)

Group	Materials			No. of Capacitors	TCC ($+23^o \rightarrow +150^oC$)
	Substrate	Dielectric	Conductor		
A	Corning No. 7059	Al_2O_3	Tophet-C	4	+351 ± 26
B	Corning No. 7059	Al_2O_3	Aluminum	35	+272 ± 67
C	Corning No. 7059	SiO	Aluminum	3	+ 42 ± 12
D	Corning No. 7059	Al_2O_3 + SiO	Aluminum	4	+116 ± 5
E	Oxidized Si	Al_2O_3	Tophet-C	12	+303 ±154
F	Oxidized Si	Al_2O_3	Aluminum	8	+119 ± 54

TABLE XIII
TEMPERATURE COEFFICIENT OF CAPACITANCE ($+150^o \rightarrow +250^oC$)

Group	Materials			No. of Capacitors	TCC ($+150^o \rightarrow +250^oC$)
	Substrate	Dielectric	Conductor		
A	Corning No. 7059	Al_2O_3	Tophet-C	4	+358 ± 39
B	Corning No. 7059	Al_2O_3	Aluminum	34	+337 ± 79
C	Corning No. 7059	SiO	Aluminum	3	+ 89 ± 13
D	Corning No. 7059	Al_2O_3 + SiO	Aluminum	4	+188 ± 2
E	Oxidized Si	Al_2O_3	Tophet-C	12	+614 ±226
F	Oxidized Si	Al_2O_3	Aluminum	8	+151 ±103

For capacitors having aluminum oxide dielectrics and Tophet-C conductors and similar capacitors having aluminum conductors, the former appear to have more uniform TCC's on Corning No. 7059 glass substrates

over the entire temperature range from +23° → +250°C, whereas the latter appear to have smaller and more uniform TCC's on oxidized silicon substrates over the same temperature range. The lowest temperature coefficient of capacitance observed over the range +23° → +150°C was +31 ppm/°C for a capacitor (No. C53-1) on a Corning No. 7059 glass substrate having a silicon monoxide dielectric and aluminum conductors. The lowest TCC observed for the range +150° → +250°C was +53 ppm/°C for a capacitor (No. C54-4) on an oxidized silicon substrate having an aluminum oxide dielectric and aluminum conductors.

c. Stability

To determine the high temperature stability of the thin film capacitors, the capacitance values measured at room temperature were compared with the corresponding capacitance values measured after the capacitors had been subjected to an environmental temperature of 350°C for 100 hours. The results of the stability tests for individual capacitors, expressed as the percent change in capacitance during the high temperature cycling, are given in Appendix C. Group data for the selected material combinations are given in Table XIV. The results given in Table XIV indicate that the stability characteristics of capacitors on Corning No. 7059 glass substrates with aluminum oxide dielectrics and aluminum conductors when subjected to 350°C for 100 hours are the most predictable of the material combinations explored. However, capacitors with aluminum oxide dielectrics demonstrated lower average drifts than those with silicon monoxide dielectrics.

TABLE XIV
PERCENT DRIFT DURING CAPACITOR STABILITY TESTS

Group	Materials			No. of Capacitors	Percent Drift
	Substrate	Dielectric	Conductor		
A	Corning No. 7059	Al_2O_3	Tophet-C	18	-0.6 ± 4.3
B	Corning No. 7059	Al_2O_3	Aluminum	31	-0.7 ± 0.6
C	Corning No. 7059	SiO	Aluminum	10	-3.2 ± 5.7
D	Corning No. 7059	Al_2O_3 + SiO	Aluminum	21	-3.5 ± 5.7
E	Oxidized Si	Al_2O_3	Tophet-C	11	+0.3 ± 7.1
F	Oxidized Si	Al_2O_3	Aluminum	13	-0.4 ± 5.4

d. Breakdown voltage

Breakdown voltages were determined by applying a ramp voltage input to a series circuit consisting of a 100-megohm resistor and the capacitor being tested. The current through this series circuit was plotted on an x-y recorder as a function of the ramp voltage input. The voltage at the onset of nonlinear conduction (greater than ohmic) was taken as the breakdown

voltage. This method of determining the breakdown voltage was used because of its non-destructive nature. The breakdown voltages measured for individual capacitors are given in Appendix C. The results for the selected material groupings without regard to specific capacitance are given in Table XV. Of the material combinations investigated, Table XV indicates that capacitors having aluminum oxide dielectrics and aluminum conductors on glass substrates and on oxidized silicon substrates exhibited the highest breakdown voltages. The highest breakdown voltage was obtained with a Group B capacitor (No. C11-2) which displayed a breakdown voltage of 125 volts. Six capacitors in Group F which displayed anomalous I-V characteristics in the voltage breakdown test and which showed no conduction nonlinearity up to the 150 volts maximum available with the ramp voltage input were not included in the results shown in Table XV.

TABLE XV
BREAKDOWN VOLTAGE

Group	Materials			No. of Capacitors	Breakdown Voltage
	Substrate	Dielectric	Conductor		
A	Corning No. 7059	Al_2O_3	Tophet-C	18	12 ± 5
B	Corning No. 7059	Al_2O_3	Aluminum	42	37 ± 19
C	Corning No. 7059	SiO	Aluminum	10	19 ± 14
D	Corning No. 7059	Al_2O_3 + SiO	Aluminum	21	30 ± 11
E	Oxidized Si	Al_2O_3	Tophet-C	12	16 ± 17
F	Oxidized Si	Al_2O_3	Aluminum	5*	26 ± 10

*Six other capacitors in this group which had B.V. >150 volts were not used in the calculations.

In order to establish whether the observed breakdown voltages were controlled by small "peaks" or other localized non-uniformities in the deposited conductor strips, an experiment was performed where the strip electrodes were ion bombarded via an argon glow discharge just prior to deposition of the dielectric material (No. C39 and No. C42). Although the capacitors fabricated during this experiment appeared to have more uniform breakdown voltages, the difference was not significant enough to be conclusive for the small amount of data available for the comparison.

CONCLUSIONS AND RECOMMENDATIONS

Within certain limitations, thin film resistors and capacitors with large specific component values and with acceptable temperature coefficients can be fabricated for high temperature applications using Librascope's proprietary Cold Substrate Deposition Process. Specifically, resistors having sheet resistances on the order of 10^3 ohms per square can be fabricated within the design goal requirements in every respect on Corning No. 7059 glass substrates (see Appendix for data sheets of passive elements submitted to NASA-ERC). As a conclusion from the experimental results obtained in performing this program, it is felt that the techniques required to fabricate resistors having sheet resistances of 10^3 ohms per square are largely under control. However, resistors having sheet resistances of 10^4 ohms per square or greater displayed extremely large resistance changes during a post-deposition annealing treatment. The purpose of the annealing treatment was to provide a stabilizing "burn-in" prior to the 350°C life tests. The annealing changes were not as large for resistors fabricated on oxidized silicon substrates as on 7059 glass; but were, nevertheless, present, particularly for the specimens with larger sheet resistance. Thus, further experimentation is required to produce resistors having sheet resistances of 10^4 ohms per square or larger. The limited success experienced with these higher sheet resistances was undoubtedly complicated by island structuring which is an inherent property of extremely thin films. The solution to developing these resistors lies primarily with finding a suitable material combination which can be deposited with thicknesses commensurate with those of continuous thin films and yet provide the higher ohms per square. These materials must also be relatively chemically inert over the entire specified temperature range. A material structure which has promising possibility of meeting the stringent requirements is a mixture of a material, such as a carbide, imbedded in an insulating material, such as aluminum oxide. The insulating material would provide the bulk required to deposit thicker films yet still retain the higher specific resistances. Assuming a structure such as this could provide sheet resistances of the proper magnitude, the fractional concentrations of the two constituents could be adjusted in such a manner that the positive temperature coefficient of resistance of one would largely cancel out the negative coefficient of the other over the temperature range of interest. In addition, a material composition such as this might be self-protective so that no overcoating film would be required to prevent environmental degradation. As for obtaining resistors on oxidized silicon substrates which have characteristics consistent with those on glass substrates, a simple, straightforward application of a properly selected, undercoating material may be sufficient.

Capacitors have been fabricated on Corning No. 7059 glass substrates which satisfactorily met all of the design goal requirements. Similar capacitors fabricated on oxidized silicon substrates met all requirements with the exception of specified minimum breakdown voltage. Breakdown voltages within the specified range were achieved only sporadically and the wide spread in the breakdown voltage values suggests that these variations are caused by the presence of pinholes in the capacitor substrate (the thermally grown

silicon dioxide on the silicon wafer). Another complication introduced when fabricating capacitors on oxidized silicon substrates was the presence of parasitic capacitances. These capacitances were formed along a circuitous route through the effective "capacitor" formed by the oxide layer between one of the electrodes and the silicon substrate, along the low resistance path of the silicon, and back through the oxide layer to the other electrode. A logical remedy for minimizing these parasitic capacitances is isolation of the capacitors from the oxidized silicon with a deposited layer of insulating material.

Further efforts to develop capacitors which have even larger specific capacitances should be centered on successful deposition of continuous thin films with materials having larger dielectric constants. Continuation of efforts with the presently used dielectric materials by reduction in film thickness would undoubtedly lead to lower breakdown voltages and lower device yield (due to increase in probability of pinhole formation).

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APPENDICES

Appendix A. Design Goal Requirements

The design goals for the thin film passive elements fabricated in the performance of this program are as follows:

Resistors

a. Films deposited on glass or ceramic substrates.
   (1) Sheet resistances of 10^3, 10^4, and 10^5 ohms per square.
   (2) Temperature coefficient of resistance (TCR) in the range -30°C to +150°C within ± 100 ppm/°C.
   (3) Temperature coefficient of resistance in the range +150°C to +300°C within
       100 ppm/°C for the 10^3 ohms per square
       150 ppm/°C for the 10^4 ohms per square
       200 ppm/°C for the 10^5 ohms per square
   (4) Current noise (db): -25 μ V/V in a decade.
   (5) Nominal value of resistance without adjusting within ± 10% of the design goal.
   (6) Stability after 100 hrs. at 350°C within ± 2%.

b. Same requirements as above but for resistor films deposited on thermally oxidized silicon wafers (4000-5000 Å thickness of SiO_2).

Capacitors

a. Films deposited on glass or ceramic substrates.
   (1) Capacitance of 100,000 pf/in^2.
   (2) Temperature coefficient of capacitance within ± 300 ppm/°C.
   (3) Breakdown voltage of 30 VDC.
   (4) Nominal value without adjustment within ± 10%.

b. Same requirements as above but for films deposited on thermally oxidized silicon wafers (4000-6000 Å thickness of SiO_2).

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Appendix B. Resistor Data

Resistor	Group	Resistane $\Omega/\square$ after	Percent change During anneal	Percent Drift	TCR (-70→ +150)	TCR (+150→ +300)
R1-1	I	$.99 \times 10^3$	-11.5	-1.6	+117(+62)*	-42
R1-2	I	1.10×10^3	-10.5	-3.7	+206(+153)	+11
R1-3	I	1.02×10^3	-12.9	0	-330(-230)	+15
R1-4	I	$.97 \times 10^3$	-11.8	+2.5	-198(-126)	-32
R4-1	I	1.37×10^3	-7.9	+73.4	+624(+646)	+770
R4-2	I	25.80×10^3	+1281	+8550.	-100(-267)	-327
R4-3	I	2.88×10^3	+78.0	+68.5	+620(+642)	+805
R4-4	I	1.10×10^3	-19.6	+23.5	+615(+653)	+820
R5-1	I	4.16×10^2	-48.4	+0.3	+54(+50)	+44
R5-3	I	4.24×10^2	-48.8	+1.0	-105(-10)	+111
R5-4	I	4.20×10^2	-48.6	+0.7	+53(+47)	+31
R6-1	I	$.57 \times 10^3$	-42.7	+9.0	+52(+58)	+74
R6-2	I	$.59 \times 10^3$	-43.4	+9.0	+54(+75)	+65
R6-3	I	$.59 \times 10^3$	-41.7	+10.0	+15(+63)	+95
R6-4	I	$.58 \times 10^3$	-40.0	+8.9	+98(+77)	+74
R9-1	I	$.87 \times 10^3$	-41.0		+51(+52)	+59
R9-2	I	$.88 \times 10^3$	-40.9		+51(+54)	+63
R9-3	I	$.85 \times 10^3$	-41.0		+57(+59)	+60
R9-4	I	$.95 \times 10^3$	-39.6		+51(+57)	+81
R11-1	I	1.09×10^3	-56.4	-0.4	-2(0)	+54
R11-2	I	1.12×10^3	-56.7	0	-2(+10)	+25
R11-3	I	1.09×10^3	-56.5	0	0(0)	+23
R11-4	I	1.08×10^3	-56.0	0	-10(-4)	+35
R12-1	I	$.91 \times 10^3$	-59.5	+0.5	+23(+32)	+34
R12-2	I	$.90 \times 10^3$	-59.8	+0.3	+24(+29)	+45
R12-3	I	$.90 \times 10^3$	-59.5	+0.1	+21(+29)	+10
R12-4	I	$.91 \times 10^3$	-59.5	+1.1	+69(+107)	+45
R13-1	I	$.86 \times 10^3$	-54.5	-0.1	+12(+17)	+43
R13-2	I	$.86 \times 10^3$	-55.2	0	+17(+22)	+29
R13-3	I	$.85 \times 10^3$	-55.2	+0.1	+15(+22)	+22
R13-4	I	$.87 \times 10^3$	-54.6	+0.1	+12(+26)	+40
R15-1	I	3.90×10^4	+269		-285(-228)	-307
R15-2	I	15.71×10^4	+1310		-559(-510)	-768
R15-3	I	15.51×10^4	+1350		-990(-852)	-1052
R15-4	I	5.38×10^4	+388		-440(-368)	-505
R17-1	I	4.20×10^7	$+1.21 \times 10^5$		-11,520(-3,740)	
R17-2	I	5.39×10^7	$+1.53 \times 10^5$		-11,480(-3,590)	
R17-3	I	5.50×10^7	$+1.78 \times 10^5$		-11,100(-3,610)	
R17-4	I	5.69×10^7	$+1.80 \times 10^5$		-10,830(-3,650)	

* values in parentheses are for values of TCR(+23 → + 150)

Resistor	Group	Resistance Ω/□ after	Percent change During anneal	Percent Drift	TCR (-70→ +150)	TCR (+150→ +300)
R18-1	I	1.71×10^{8}	$+3.72 \times 10^{5}$			
R18-2	I	3.06×10^{8}	$+6.50 \times 10^{5}$			
R18-3	I	3.80×10^{8}	$+8.11 \times 10^{5}$			
R18-4	I	3.71×10^{8}	$+7.55 \times 10^{5}$			
R20-1	I	5.77×10^{8}	$+2.69 \times 10^{5}$			
R20-2	I	5.84×10^{8}	$+2.55 \times 10^{5}$			
R20-3	I	5.29×10^{8}	$+2.68 \times 10^{5}$			
R20-4	I	5.24×10^{8}	$+2.66 \times 10^{5}$			
R21-1	I	1.97×10^{10}	$+1.37 \times 10^{7}$		-21,100(-6,960)*	-985
R21-2	I	2.58×10^{10}	$+2.20 \times 10^{7}$		-17,100(-7,200)	-717
R21-3	I	2.69×10^{10}	$+2.34 \times 10^{7}$		-39,500(-7,200)	-715
R21-4	I	2.75×10^{10}	$+1.85 \times 10^{7}$		-23,100(-7,160)	-761
R24-1	II	5.85×10^{2}	-21.9		+11 (+63)	+58
R24-2	II	6.03×10^{2}	-17.7		0 (+61)	+106
R24-3	II	5.60×10^{2}	-23.6		-50 (+53)	+123
R24-4	II	5.93×10^{2}	-22.7		-62 (+50)	+131
R25-1	II	2.42×10^{7}	$+1.60 \times 10^{5}$		-6010 (-5,210)	
R25-2	II	1.68×10^{7}	$+1.17 \times 10^{5}$		-7020 (-2,390)	
R25-3	II	$.50 \times 10^{7}$	$+ .36 \times 10^{5}$		-4970 (-3,570)	
R25-4	II	1.41×10^{7}	$+1.00 \times 10^{5}$		-5350 (-3,520)	
R26-1	II	2.94×10^{8}	$+3.00 \times 10^{5}$			
R26-2	II	4.04×10^{8}	$+5.00 \times 10^{5}$			
R26-3	II	2.26×10^{8}	$+2.81 \times 10^{5}$			
R26-4	II	2.75×10^{8}	$+3.07 \times 10^{5}$			
R27-1	VI	9.13×10^{2}	-72.0	+0.3	+131(+110)	+178
R27-2	VI	6.81×10^{2}	-69.3	+0.8	+125(+163)	+220
R27-3	VI	7.03×10^{2}	-59.5	-2.0	+128(+106)	+244
R27-4	VI	9.05×10^{2}	-70.4	-1.0	+148(+153)	+14
R28-1	VI	$.35 \times 10^{5}$	-25.5			
R28-2	VI	11.30×10^{5}	+567			
R28-3	VI	6.58×10^{5}	+234			
R28-4	VI	$.21 \times 10^{5}$	-42			
R31-1	VIII	$\sim 10^{10}$	-			
R31-2	VIII	$\sim 10^{10}$	-			
R31-3	VIII	$\sim 10^{10}$	-			
R31-4	VIII	$\sim 10^{10}$	-			
R32-1	VIII	$\sim 10^{7}$	-			
R32-2	VIII	$\sim 10^{7}$	-			
R32-3	VIII	$\sim 10^{7}$	-			
R32-4	VIII	$\sim 10^{7}$	-			

* values in parentheses are for values of TCR(+23→+ 150)

Resistor	Group	Resistance Ω/□ after	Percent Change During anneal	Percent Drift	TCR (-70→ +150)	TCR (+150→ +300)
R33-1	VIII	8.97×10^3	+707	+1.7	-3420(-2490)*	-1280
R33-2	VIII	9.20×10^3	+716	+1.2	-3320(-2530)	-1390
R33-3	VIII	9.15×10^3	+712	+3.2	-3430(-2480)	-1370
R33-4	VIII	8.82×10^3	+707	+1.4	-3120(-2480)	-1240
R35-1	IV	6.44×10^2	-59.2	+1.5		
R35-2	IV	6.34×10^2	-58.9	+6.1		
R35-3	IV	6.80×10^2	-55.2	-12.3		
R35-4	IV	6.69×10^2	-57.1	+1.7		
R36-1	IV	$\sim 10^8$	-			
R36-2	IV	$\sim 10^8$	-			
R36-3	IV	$\sim 10^8$	-			
R36-4	IV	$\sim 10^8$	-			
R37-1	V	1.61×10^4	+339	+2.2		
R37-2	V	5.11×10^4	+905	+5.9		
R37-3	V	$\sim 10^8$	-	-		
R37-4	V	$\sim 10^8$	-	-		
R38-1	V	$\sim 10^8$	-			
R38-2	V	$\sim 10^8$	-			
R38-3	V	$\sim 10^8$	-			
R38-4	V	$\sim 10^8$	-			
R40-1	IX	$\sim 10^8$	-			
R40-2	IX	$\sim 10^8$	-			
R40-3	IX	$\sim 10^8$	-			
R40-4	IX	$\sim 10^8$	-			
R41-1	IX	$\sim 10^8$	-			
R41-2	IX	$\sim 10^8$	-			
R41-3	IX	2.44×10^5	+950			
R41-4	IX	$.34 \times 10^5$	+98			
R42-1	IX	7.62×10^3	-43.7	+2.2	unstable	unstable
R42-2	IX	∞(scratch)	-	-	-	-
R42-3	IX	5.07×10^3	-54.5	+1.7	+15 (-35)	-157
R42-4	IX	5.12×10^3	-53.6	+2.5	+15 (-32)	-100
R43-1	IX	$\sim 10^8$	-			
R43-2	IX	$\sim 10^8$	-			
R43-3	IX	$\sim 10^8$	-			
R43-4	IX	$\sim 10^8$	-			
R44-1	IX	3.66×10^3	+220	+6.1		
R44-2	IX	5.88×10^3	+375	+6.6		
R44-3	IX	19.50×10^3	+1390	-4.7		
R44-4	IX	14.90×10^3	+1200	+2.2		

* values in parentheses are for values of TCR(+23→+ 150)

Resistor	Group	Resistance Ω/□ after	Percent Change During anneal	Percent Drift	TCR (-70 → +150)	TCR (+150 → +300)
R45-1	X	447	-26.0	-1.6		
R45-2	X	465	-27.2	-0.9		
R45-3	X	459	-23.8	-2.0		
R45-4	X	442	-25.4	-1.4		
R46-1	X	4.86×10^3	-37.7	-1.2	+8 (-125)*	-149
R46-2	X	4.46×10^3	-40.0	-2.9	-126 (-132)	-135
R46-3	X	4.70×10^3	-36.8	-1.9	-236 (-238)	-245
R46-4	X	5.75×10^3	-25.5	-3.3	-261 (-210)	-131
R47-1	X	5.05×10^4	+54.0	-2.8		
R47-2	X	10.30×10^4	+232.0	-0.6		
R47-3	X	$\sim 10^8$	-	-		
R47-4	X	3.44×10^4	+10.5	+6.4		
R48-1	XI	1.09×10^3	-13.0	+1.0		
R48-2	XI	1.16×10^3	-15.0	+0.3		
R48-3	XI	$.99 \times 10^3$	-23.4	+2.0		
R48-4	XI	$.89 \times 10^3$	-28.0	+2.1		
R49-1	XI	1.31×10^4	+51.9	+2.5	-824 (-870)	-918
R49-2	XI	1.67×10^4	+88.9	+2.5	-738 (-1170)	-1403
R49-3	XI	1.44×10^4	+65.3	+1.4	-814 (-872)	-1000
R49-4	XI	1.54×10^4	+88.9	+0.9	-808 (-875)	-1094
R50-1	XI	2.54×10^4	+72.7	+1.1		
R50-2	XI	2.49×10^4	+31.8	+0.8		
R50-3	XI	∞	-	-		
R50-4	XI	∞	-	-		
R51-1	XII	1.61×10^3	-10.2	-1.1		
R51-2	XII	1.57×10^3	-19.7	-1.2		
R51-3	XII	1.63×10^3	-16.3	-3.5		
R51-4	XII	1.75×10^3	-4.9	-0.5		
R52-1	XII	4.00×10^3	-32.1	-1.4	-675 (-615)	-564
R52-2	XII	3.74×10^3	-30.7	-0.3	-531 (-572)	-676
R52-3	XII	3.58×10^3	-31.2	+2.1	-672 (-743)	-755
R52-4	XII	4.12×10^3	-26.3	+3.6	-778 (-770)	-705
R53-1	II	8.42×10^3	+31.6			
R53-2	II	3.62×10^3	-42.0			
R53-3	II	4.14×10^3	-35.5			
R53-4	II	2.91×10^3	-53.5			
R54-1	II	$\sim 10^8$	-			
R54-2	II	$\sim 10^8$	-			
R54-3	II	$\sim 10^8$	-			
R54-4	II	$\sim 10^8$	-			

* values in parentheses are for values of TCR(+23 → + 150)

Resistor	Group	Resistance Ω /□ after	Percent Change During anneal	Percent Drift	TCR (-70→ +150)	TCR (+150→ +300)
R55-1	Sp	$\sim 10^8$	-			
R55-2	Sp	$\sim 10^8$	-			
R55-3	Sp	$\sim 10^8$	-			
R55-4	Sp	$\sim 10^8$	-			
R56-1	Sp	2.66×10^5	-0.5	+8.1	-1390 (-1450)*	-1530
R56-2	Sp	1.88×10^5	+0.2	+7.8	-1260 (-1310)	-1290
R56-3	Sp	1.29×10^5	+20.9	+11.2	-2000 (-1840)	-1040
R56-4	Sp	3.48×10^5	-2.1	+3.6	-1810 (-1650)	-1430
R58-1	VII	$\sim 10^8$	-			
R58-2	VII	$\sim 10^8$	-			
R58-3	VII	$\sim 10^8$	-			
R58-4	VII	$\sim 10^8$	-			
R59-1	VII	1.41×10^3	-63.5			
R59-2	VII	1.56×10^3	-66.3			
R59-3	VII	1.57×10^3	-64.1			
R59-4	VII	1.42×10^3	-62.1			
R60-1	VII	$\sim 10^8$	-			
R60-2	VII	$\sim 10^8$	-			
R60-3	VII	$\sim 10^8$	-			
R60-4	VII	$\sim 10^8$	-			
R62-1	XIII	352	-59.5	-2.0	+218 (+222)	+71
R62-2	XIII	355	-59.4	-0.4	+193 (+231)	+88
R62-3	XIII	359	-58.8	+2.1	+186 (+145)	+61
R62-4	XIII	355	-59.0	-2.1	+127 (+126)	+115
R63-1	XIII	293	-68.0	-0.5	+22 (+13)	+117
R63-2	XIII	300	-68.4	-0.6	+50 (0)	+73
R63-3	XIII	287	-69.0	+2.1	-90 (+233)	+44
R63-4	XIII	282	-68.4	+0.8	-160 (+119)	+79
R64-1	XIII	282	-69.0	+1.3	+68 (+66)	-100
R64-2	XIII	288	-69.3	+2.1	+37 (+90)	-142
R64-3	XIII	288	-68.6	+2.3	+97 (+116)	-66
R64-4	XIII	284	-68.4	+3.5	+76 (+92)	-45
R65-1	XIII	728	-58.5	+4.7	+466 (+544)	+692
R65-2	XIII	758	-58.0	+4.4	+485 (+582)	+692
R65-3	XIII	739	-55.0	+4.1	+465 (+517)	+272
R65-4	XIII	568	-62.5	+8.7	+464 (+526)	+424
R66-1	XIII	242	-75.3	+1.0	+460 (+505)	+596
R66-2	XIII	250	-75.1	+0.4	+425 (+547)	+490
R66-3	XIII	254	-74.9	-3.7	+547 (+408)	+470
R66-4	XIII	(cracked)	-	-	-	-

* values in parentheses are for values of TCR(+23→+ 150)

Resistor	Group	Resistance Ω/□ after	Percent Change During anneal	Percent Drift	TCR (-70→ +150	TCR (+150→ +300)
R67-1	XIII	349	-71.6	+1.9	+177 (-21)*	-885
R67-2	XIII	361	-73.5	+2.6	+136(+164)	+208
R67-3	XIII	355	-72.5	+1.5	+127(+147)	+115
R67-4	XIII	349	-72.0	+1.9	+99(+150)	+154
R68-1	XIII	362	-75.5	+2.0	+265(+194)	+139
R68-2	XIII	364	-76.0	+1.9	+187(+152)	+258
R68-3	XIII	377	-75.2	-1.6	+23(+118)	+368
R68-4	XIII	371	-74.5	-3.3	+76(+171)	+444
R69-1	XIII	5590	-61.0	-8.1	-172 (-219)	+634
R69-2	XIII	5960	-61.1	-18.1	-221 (-222)	+455
R69-3	XIII	5050	-63.3	+10.5	-207 (-103)	-50
R69-4	XIII	4790	-61.5	+31.7	-152(-117)	-53
R70-1	XIII	1116	-74.8	+3.1	+38 (+63)	+14
R70-2	XIII	1230	-74.6	+1.3	+54 (-3)	+23
R70-3	XIII	1182	-73.0	+2.1	+78 (+60)	+12
R70-4	XIII	1131	-74.4	+3.3	+72 (+99)	+15
R71-1	XIII	10.50×10^3	-27.0	+4.3	-570 (-450)	-606
R71-2	XIII	6.45×10^3	-43.0	+7.8	-473 (-369)	-430
R71-3	XIII	6.49×10^3	-56.0	+2.5	-416 (-309)	-310
R71-4	XIII	6.93×10^3	-51.0	+3.3	-414 (-334)	-319
R72-1	XIII	(on edge)	-	-	-	-
R72-2	XIII	(on edge)	-	-	-	-
R72-3	XIII	8.91×10^4	-14.8	-41.6	-1580(-1420)	-1010
R72-4	XIII	2.18×10^4	-83.0	+264.0	-2560(-2550)	-3580
R73-1	XIII	5.93×10^5	+45.2	+10.9	-3890 (-2000)	-1800
R73-2	XIII	4.77×10^5	+35.6	+4.4	-3440 (-2380)	-1610
R73-3	XIII	8.42×10^5	+48.4	-41.6	-926 (-2840)	-1960
R73-4	XIII	8.54×10^5	+49.1	-26.4	unstable	unstable
R74-1	XIII	1.00×10^5	+31.7	+0.8	-2210 (-1720)	-1270
R74-2	XIII	1.26×10^5	+46.6	+1.2	-2360 (-1820)	-1320
R74-3	XIII	$.76 \times 10^5$	+28.5	+0.9	-1990 (-1560)	-1180
R74-4	XIII	$.72 \times 10^5$	+26.3	+1.4	unstable	unstable

* values in parentheses are for values of TCR(+23→+ 150)

Appendix C. Capacitor Data

Capacitor	Group	Capacitance 10^5pf /in^2	Percent Change During anneal	Percent Drift	TCC 23→150	TCC 150→250	Breakdown Voltage
C1-2	B	0.92	*	-0.7			30
C2-1	B	1.26	-2.1	*	+269	+339	*
C2-2	B	1.26	-2.1	-2.3	+266	+334	25
C2-3	B	1.26	-1.5	-0.6	+279	+331	25
C2-4	B	1.24	-2.5	-0.5	+281	+299	17
C3-1	B	1.44	-2.8	-0.4	+351	+530	35
C3-3	B	1.43	-2.6	-0.4	+357	+505	38
C3-4	B	1.43	-3.3	-0.5	+349	+551	30
C5-1	B	1.11	-2.9	-0.4	+246	+280	33
C5-2	B	1.09	-3.0	-0.3	+136	+310	45
C5-3	B	1.07	-3.0	-0.5	+213	+289	55
C5-4	B	1.11	-3.2	-0.5	+239	+255	40
C6-1	B	1.47	*	*	*	*	*
C10-1	B	2.65	-3.5	-1.4	+279	+298	8
C10-2	B	2.67	-3.2	-1.5	+277	+268	15
C10-3	B	2.64	-3.7	-0.8	+259	+293	8
C10-4	B	2.61	-3.9	-0.9	+264	+274	15
C11-1	B	.70	-0.2		+283	+295	40
C11-2	B	.70	+0.1		+283	+291	125
C11-3	B	.70	-0.4		+274	+290	75
C11-4	B	.69	-0.5		+267	+290	75
C12-2	B	1.59	+7.4	*	+456	unstable	*
C12-4	B	1.58	+7.3	*	+469	+510	*
C13-1	B	7.21	+35.3	*	*	*	*
C13-2	B	6.99	+35.6	*	*	*	*
C15-1	B	1.42	-5.0	+0.3	+296	+306	13
C15-2	B	1.40	-4.8	+0.5	+288	+308	10
C15-3	B	1.39	-4.5	+0.2	+262	+350	15
C15-4	B	1.41	-5.5	+0.2	+242	+405	20
C18-1	B	.89	-10.0	-0.4	+225	+374	40
C18-2	B	.92	-6.3	-0.9	+233	+341	40
C18-3	B	.92	-4.9	-0.7	+245	+324	50
C18-4	B	.91	-7.1	-1.3	+281	+257	35
C21-2	B	1.04	-3.9	-0.5	+319	+366	55
C21-3	B	1.04	-3.2	-0.4	+270	+357	35
C22-1	A	1.37	-1.4	-2.1			5
C22-2	A	1.37	-2.2	-4.3			12
C22-3	A	1.35	-1.8	-1.5			10
C22-4	A	1.36	-0.1	+8.0			4
C23-1	A	1.16	-5.8	-0.8			4
C23-2	A	1.16	-5.2	-0.7			8
C23-3	A	1.15	-4.8	-0.8			13
C23-4	A	1.17	-3.6	-0.8			15

Capacitor	Group	Capacitance 10^5pf /in^2	Percent Change During anneal	Percent Drift	TCC 23→150	TCC 150→250	Breakdown Voltage
C25-1	A	.87	-2.9	-3.8			20
C25-2	A	.88	-3.1	-10.9			13
C25-3	A	.87	-2.7	-0.8			25
C25-4	A	.88	-2.8	+8.3			15
C26-1	A	1.00	-3.4	+1.3	+349	+398	15
C26-2	A	.99	-3.3	+3.5	+347	+381	9
C26-3	A	.99	-1.5	+1.0	+322	+336	14
C26-4	A	1.02	+0.1	-2.0	+384	+315	12
C27-2	A	.49	-1.3	-1.5			13
C27-3	A	.49	+0.5	-3.2			10
C28-1	E	1.24	-5.1	+6.3	+211	+509	12
C28-2	E	1.25	-5.7	+6.6	+156	+527	15
C28-3	E	1.22	-4.9	+6.5	+144	+500	15
C28-4	E	1.23	-5.2	+6.9	+166	+480	8
C29-1	E	1.16	-37.1	+1.1	+297	+396	2.5
C29-2	E	1.13	-13.9	+2.6	+320	+561	2.5
C29-3	E	1.11	-16.7	+6.2	+239	+491	2.5
C29-4	E	1.17	-16.7	+6.7	+349	+1028	5.0
C30-1	E	.50	-49.4	-11.5	+610	+876	50
C30-2	E	.50	-58.1	-9.3	+596	+1030	15
C30-3	E	.40	-67.3	-5.6	+269	+490	20
C30-4	E	.41	-67.5	-6.0	+278	+478	50
C35-1	B	1.14	-7.9				13
C35-3	B	1.16	+3.3				55
C35-4	B	1.20	+9.4				45
C36-1	B	.62	-12.4	-13.7			30
C36-2	B	.63	-11.3	*			30
C36-3	B	.66	-9.4	-17.8			30
C36-4	B	.64	-9.3	-16.7			45
C37-1	D	.87	-6.1	-0.2			35
C37-3	D	.88	-7.1	-0.2			35
C38-1	D	.78	-18.2	-3.0			30
C38-2	D	.77	-18.5	-3.3			50
C38-3	D	.76	-19.2	-3.6			35
C39-2	B	1.42	-3.9	*			35
C39-3	B	1.42	-3.9	-1.5			50
C39-4	B	1.42	-4.3	-1.2			35
C40-1	D	1.47	-8.0	-13.6			15
C40-2	D	1.54	-7.5	-7.4			17
C40-3	D	1.54	-7.3	-9.9			20
C41-1	D	1.04	-9.8	-0.5	+120	+186	23
C41-2	D	1.03	-10.4	-1.0	+115	+189	40
C41-3	D	1.03	-10.7	-0.4	+120	+189	12
C41-4	D	1.03	-11.2	-0.3	+110	+187	45
C42-1	D	1.23	-12.8	-0.3			35
C42-2	D	1.23	-12.3	-0.5			30
C42-3	D	1.22	-12.6	-0.3			35
C42-4	D	1.23	-12.8	-0.4			25

Capacitor	Group	Capacitance 10^5pf /in^2	Percent Change During anneal	Percent Drift	TCC 23→150	TCC 150→250	Breakdown Voltage
C44-1	B	.91	-4.9	-1.3	+173	+356	60
C44-2	B	.89	-4.3	-1.7	+166	+347	80
C44-3	B	.88	-5.0	-1.2	+219	+290	50
C44-4	B	.89	-4.2	-1.3	+220	+237	65
C45-2	F	1.66	-8.1	*			15
C45-3	F	1.57	-8.1	-5.8			40
C45-4	F	1.57	-8.8	-2.7			32
C46-1	F	.34	+1.7	-0.1			>150
C46-2	F	.34	+2.5	-0.6			>150
C46-3	F	1.62	-9.1	+8.8			23
C46-4	F	1.63	-8.5	+8.3			20
C47-1	F	.43	-62.9	-3.3	+180	+196	>150
C47-2	F	.43	-62.6	-4.5	+180	+381	>150
C47-3	F	.44	-62.2	-2.3	+45	+101	>150
C47-4	F	.41	-63.4	-3.0	+134	+169	>150
C50-1	C	.86	-10.3	-8.8			5
C50-2	C	.86	-10.3	-8.0			10
C50-3	C	.86	-10.5	-10.3			5
C50-4	C	.86	-10.7	-10.9			8
C51-1	C	.82	-16.7	+3.3			45
C51-2	C	.82	-16.3	+4.3			35
C51-3	C	.81	-16.9	*			*
C51-4	C	.82	-16.8	-0.3			25
C53-1	C	1.04	-9.9	-0.4	+31	+78	22
C53-2	C	1.05	-9.9	-0.4	+42	+85	24
C53-3	C	1.02	-9.9	-0.2	+54	+103	10
C54-1	D**	.26	-60.1	-0.1	+118	+112	>150
C54-2	D**	.27	-58.2	-4.2	+163	+93	>150
C54-3	D**	.27	-58.8	-6.7	+65	+104	>150
C54-4	D**	.24	-62.3	+8.3	+67	+53	>150
C55-1	D	.38	-19.1	-1.5			35
C55-2	D	.39	-18.3	-2.0			35
C55-3	D	.40	-14.8	-1.1			40
C55-4	D	.39	-15.5	-2.1			25

**(Si Sub)

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Appendix D. Passive Element Data Sheets

The data sheets included in this appendix specify the characteristics of selected passive elements as measured in the laboratories of Librascope's Physical Research Department. These elements were submitted to NASA-ERC as a portion of the contractual agreement. The sheets are arranged in the following order:

Resistors:		Page
10^3 Ω/□	on glass (No. R12)	51
10^4 Ω/□	on glass (No. R33)	52
10^5 Ω/□	on glass (No. R56)	53
10^3 Ω/□	on oxidized silicon (No. R70)	54
10^4 Ω/□	on oxidized silicon (No. R71)	55
10^5 Ω/□	on oxidized silicon (No. R74)	56
Capacitors:		
10^6 pf/in.^{2}	on glass (No. C5)	57
10^6 pf/in.^{2}	on oxidized silicon (No. C29)	58

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DATA SHEET FOR RESISTOR SUBSTRATE NO. R12

Substrate:	Corning glass No. 7059
Resistive Material:	Tophet-C
Contact Material:	Tophet-C/Au
Overcoating Material:	Silicon monoxide
Nominal Value:	10^3 ohms per square

Resistor	Resistance Ohms/Square	Dev. from Nom. Value %	TCR (-70→+150) ppm/°C	TCR (+150→+300) ppm/°C	Drift %
R12-1	918	-8.2	+23	+34	+0.5
R12-2	906	-9.4	+24	+45	+0.3
R12-3	904	-9.6	+21	+10	+0.1
R12-4	917	-8.3	+69	+45	+1.1
Average	911		+34	+33.5	+0.5
Range	14		48	35	1.0
Rel. Range	.015		1.41	1.05	2.0
Std. Deviation	7.3		23	28.6	.43
Rel. Std. Dev.	.008		.68	.85	.86

DATA SHEET FOR RESISTOR SUBSTRATE No. R33

Substrate:	Corning glass No. 7059
Resistive Material:	1 part (At. %) Cr to 2 parts (At. %) Ge
Contact Material:	Cr-Ge/Al
Overcoating Material:	Silicon Monoxide
Nominal Value:	10^4 ohms per square

Resistor	Resistance 10^4 Ohms /Square	Dev. from Nom. Value %	TCR (-70→+150) ppm/°C	TCR (+150→+300) ppm/°C	Drift %
R33-1	8.97	-10.3	-3420	-1280	+1.7
R33-2	9.20	-8.0	-3320	-1390	+1.2
R33-3	9.15	-8.5	-3430	-1370	+3.2
R33-4	8.82	-11.8	-3120	-1240	+1.4
Average	9.03		-3322	-1320	+1.9
Range	38		310	150	2.0
Rel. Range	.042		.093	.11	1.05
Std. Deviation	17		144	72	.9
Rel. Std. Dev.	.020		.043	.05	.47

DATA SHEET FOR RESISTOR SUBSTRATE No. R56

Substrate:	Corning glass No. 7059
Resistive Material:	Tophet-C
Contact Material:	Tophet-C
Overcoating Material:	Silicon monoxide
Nominal Value:	10^5 ohms per square

Resistor	Resistance 10^5 Ohms /Square	Dev. from Nom. Value %	TCR (-70→+150) ppm/°C	TCR (+150→+300) ppm/°C	Drift %
R56-1	2.66	+166	-1390	-1530	+8.1
R56-2	1.88	+88	-1260	-1290	+7.8
R56-3	1.30	+30	-2000	-1040	+11.2
R56-4	3.48	+248	-1810	-1430	+3.6
Average	2.33		-1615	-1322	+7.8
Range	2.18		740	490	7.6
Rel. Range	.94		.46	.37	.98
Std. Deviation	.95		348	213	3.1
Rel. Std. Dev.	.41		.22	.16	.40

DATA SHEET FOR RESISTOR SUBSTRATE No. R70

Substrate:	Oxidized silicon
Resistive Material:	Tophet-C
Contact Material:	Tophet-C/Al
Overcoating Material:	Silicon monoxide
Nominal Value:	10^3 ohms per square

Resistor	Resistance Ohms /Square	Dev. from Nom. Value %	TCR (-70→+150) ppm/°C	TCR (+150→+300) ppm/°C	Drift %
R70-1	1116	+11.6	+38	+14	+3.1
R70-2	1230	+23.0	+54	+23	+1.3
R70-3	1182	+18.2	+78	+12	+2.1
R70-4	1131	+13.1	+72	+15	+3.3
Average	1165		+61	+16	+2.5
Range	114		40	11	2.0
Rel. Range	.098		.66	.69	.80
Std. Deviation	52		18	5	.9
Rel. Std. Dev.	.045		.30	.31	.36

DATA SHEET FOR RESISTOR SUBSTRATE No. R71

Substrate:	Oxidized silicon
Resistive Material:	Tophet-C
Contact Material:	Tophet-C/Al
Overcoating Material:	Silicon monoxide
Nominal Value:	10^4 ohms per square

Resistor	Resistance 10^4 Ohms /Square	Dev. from Nom. Value %	TCR (-70→+150) ppm/°C	TCR (+150→+300) ppm/°C	Drift %
R71-1	1.098	+9.8	-570	-606	+4.3
R71-2	.692	-30.8	-473	-430	+7.8
R71-3	.665	-33.5	-416	-310	+2.5
R71-4	.714	-28.6	-414	-319	+3.3
Average	.792		-468	-416	+4.5
Range	.433		156	296	5.3
Rel. Range	.55		.33	.71	1.18
Std. Deviation	.205		73	138	2.3
Rel. Std. Dev.	.26		.16	.33	.51

DATA SHEET FOR RESISTOR SUBSTRATE No. R74

Substrate:	Oxidized silicon
Resistive Material:	Tophet-C
Contact Material:	Tophet-C/Al
Overcoating Material:	Silicon monoxide
Nominal Value:	10^5 ohms per square

Resistor	Resistance 10^5 Ohms Square	Dev. from Nom. Value %	TCR (-70→+150) ppm/°C	TCR (+150→+300) ppm/°C	Drift %
R74-1	1.01	+1	-2210	-1270	+0.8
R74-2	1.28	+28	-2360	-1320	+1.2
R74-3	.76	-24	-1990	-1180	+0.9
R74-4	.73	-27	-6200 unstable	+2150	+1.4
Average	.95				+1.1
Range	.55				.6
Rel. Range	.58				.55
Std. Deviation	.26				.3
Rel. Std. Dev.	.27				.27

DATA SHEET FOR CAPACITOR SUBSTRATE No. C5

Substrate: Corning glass No. 7059
Dielectric Material: Aluminum oxide
Contact Material: Aluminum
Nominal Value: 10^5 picofarads per in^2

Capacitor	Capacitance 10^5 pf/in^2	Dev. from Nom. Val. %	TCC (+23→+150) ppm/°C	TCC (+150→+250) ppm/°C	Breakdown Voltage	Drift %
C5-1	1.11	+11.0	+246	+280	33	-0.4
C5-2	1.09	+9.0	+136	+310	45	-0.3
C5-3	1.07	+7.0	+213	+289	55	-0.5
C5-4	1.11	+11.0	+239	+255	40	-0.5
Average	1.10		+209	+284	43	-0.4
Range	.04		110	55	22	0.2
Rel. Range	.036		.53	.19	.51	.50
Std. Deviation	.02		50	23	10	0.1
Rel. Std. Dev.	.018		.24	.08	.23	.25

DATA SHEET FOR CAPACITOR SUBSTRATE No. C29

Substrate	Oxidized silicon
Dielectric Material:	Aluminum oxide
Contact Material:	Tophet-C
Nominal Value:	10^5 picofarads per in^2

Capacitor	Capacitance 10^5 pf/in^2	Dev. from Nom. Val. %	TCC (+23→+150) ppm/°C	TCC (+150→+250) ppm/°C	Breakdown Voltage	Drift %
C29-1	1.16	+16.0	+297	+396	2.5	+1.1
C29-2	1.13	+13.0	+320	+561	2.5	+2.6
C29-3	1.11	+11.0	+239	+491	2.5	+6.2
C29-4	1.17	+17.0	+349	+1028	5.0	+6.7
Average	1.14		+301	+619	3.1	+4.1
Range	.06		110	632	2.5	5.6
Rel. Range	.053		.37	1.02	.81	1.37
Std. Deviation	.03		47	281	1.3	2.8
Rel. Std. Dev.	.026		.16	.46	.41	.68

NEW TECHNOLOGY APPENDIX

After a diligent review of the work performed under this contract, no new innovation, discovery, improvement or invention was made during the entire performance of any works under this contract.