Low-Power Integrated-Circuit Driver for Ferrite-Memory Word Lines

The problem:
Standard bidirectional current drivers utilize npn bipolar transistors and transformers. These circuits possess negligible quiescent power dissipation. Also, the transformers complicate integrated-circuit (IC) fabrication of these schemes. Circuits using only npn bipolar transistors consume excessive power. Although complementary bipolar circuits can provide bidirectional word-drive current pulses, fabricating high-quality npn and pnp devices on a common substrate also presents problems.

The solution:
A newly developed word-line drive circuit, realizable in IC form, generates bidirectional current pulses and consumes little power. Also, current-pulse amplitudes and rise times are independent of active-device parameters. This composite circuit uses both npn bipolar and p-channel MOS transistors (BIMOS).

How it's done:
The figure shows the new BIMOS word-driver circuit. Each driver uses three bipolar npn transistors (Q1, Q2, and Q3), one MOS p-channel device (Q4), and three internal resistors (R1, R2, and R3). Inputs consist of a positive supply line (V_S), a write line (V_W), a read line (V_R), and a write current line (V_IN). The emitter of Q3 and the collector of Q2 provide an output (V_O) which drives a single laminated-ferrite word line. Two external precision resistors, R_R and R_W, set the amplitude and rise time, respectively, of the read and write current pulses.

The BIMOS driver provides (1) ease of IC construction; (2) low standby power consumption; (3) bidirectional current pulses; and (4) current-pulse amplitudes and rise times independent of active-device parameters, e.g., transistor beta.

Note:
Requests for further information may be directed to:
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Reference: TSP70-10374

Patent status:
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