DESIGN AND PERFORMANCE ANALYSIS OF A MEDIUM-POWER DC-DC CONVERTER

by Arthur G. Birchenough and Francis Gourash

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Cleveland, Ohio
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16. Abstract
The design and performance of an experimental dc-dc converter are described. The converter was rated for a power output of 1 kW, with a 150-percent overload rating, and it produced a 200-V, ±1-percent, dc output from an input of 56 V, ±10 and ±20 percent. Voltage regulation is accomplished by varying the duty cycle of the internal 7-kHz quasi-square-wave carrier. Integrated circuits in the control section, a proportional current drive system, and powdered metal cores (Ni-17Fe-2Mo) for the power transformer were some of the design features. The measured efficiency peaked at 92 percent and was 88 percent at 1 kW. The total component weight was 6 lb (2.7 kg).
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SUMMARY

The design and performance of an experimental quasi-square-wave dc-dc converter compatible with a high-input-voltage pulse-width-modulation inverter is reported. A breadboard model, which has a 56-volt (+10- and -20-percent) dc input with a 200-volt (±1-percent) dc output, was built and tested. Power output was 1 kilowatt with a continuous overload capability of 150 percent.

The output stage used transistors in a full-bridge arrangement. These transistors offered speed, gain, and saturation characteristics which resulted in high efficiencies. Toroidal powdered-metal cores (Ni-17F3-2Mo) instead of laminated cores were used in a low-loss power transformer operating at the 7 kilohertz carrier frequency. An integrated-circuit control section and a proportional current drive system also helped produce high efficiencies over a broad range of output power, with a peak efficiency of 92 percent. Efficiency was greater than 87 percent for 150 watts to 1.2 kilowatts of output, and it was almost independent of the input voltage.

This converter was designed for high reliability by minimization of component parts, component derating, inclusion of an overload protection circuit, and by the use of circuits which produced no potentially damaging voltage or current spikes. The total parts count is less than 100, and the weight of these components is approximately 6 pounds (2.7 kg).

INTRODUCTION

The conditioned electrical power required for future space missions will increase considerably into the multikilowatt range as the missions become more complex and of longer duration. The need for more efficient, lighter weight, and more reliable power conditioning will increase.
This report describes a dc-dc converter designed for high reliability, high efficiency, and reduced size and weight. To accomplish these ends, the design features include high-frequency operation with as few parts as possible, elimination of critical components, a minimum of adjustments, component derating for greater safety margins, and the use of low-power integrated circuits. Also, a proportional current drive system and a high-efficiency transformer were used in an experimental breadboard model which was fabricated and tested to evaluate the converter design. The experimental model was rated for a power output of 1 kilowatt and produced a regulated dc output of 200 volts (±1 percent) from an unregulated dc input of 56 volts (+10 and -20 percent).

The overall converter design and the operation of the individual circuits are described, and the performance test results are analyzed and evaluated. (A complete schematic circuit diagram with its parts list is included in fig. 11 at the back of the report.)

PRINCIPLES OF OPERATION

Design Philosophy

The converter discussed in this report was designed to be used with a lightweight, high-efficiency, pulse-width-modulated inverter rated at approximately 1 kilowatt per phase. The inverter was designed for operation without an output transformer, and it therefore requires a regulated high-voltage dc input. Existing converters that can be used are generally bulky, inefficient, or unreliable (ref. 1).

In the converter, design, size, weight, efficiency, and reliability were considered equally important; therefore, the design was not optimized for any single quality. The circuit configuration is a full-bridge inverter followed by a transformer and rectifier. Proportional current drive was used in the output stage which operated at 7 kilohertz.

The primary advantage of high-frequency power conversion is the reduction in size and weight which is possible because of the smaller magnetic components. However, high-frequency operation results in increased switching and core losses, so a compromise must be made which results in acceptable weight and efficiency.

Integrated circuits were used in the control section to reduce power consumption and to increase the reliability. And, throughout the circuit, only a minimum number of parts were used, and these were derated.
Quasi-Square-Wave Converter Operation

Voltage regulation in a quasi-square-wave converter is accomplished by a technique similar to phase control in ac regulators. The power output stage, which consists of a full-bridge circuit with power transistors, generates a quasi-square-wave ac voltage at 7 kilohertz by controlling the switching of the power transistors. The duty cycle of the quasi-square-wave is varied to regulate the output voltage as the input voltage and load vary.

The half-cycle average value of a quasi-square-waveform is defined by

\[
E_{\text{ave}} = \frac{1}{T/2} \int_0^{T/2} e(t) \, dt
\]

where \( e(t) \) is the instantaneous voltage and \( T/2 \) the half-cycle period. If \( e(t) \) is a constant equal to \( E \) for part of the period and then equal to zero for the rest of the half cycle,

\[
E_{\text{ave}} = \frac{1}{T/2} \left[ Et \right]_{t_1}^{t_2} = \frac{E \Delta t}{T}
\]

where \( \Delta t = t_2 - t_1 \) is the time interval that \( e(t) = E \).

This expression indicates that the average value of the periodic voltage is proportional to the duty cycle \( \Delta t/T \).

In the converter, the frequency of the quasi-square-wave voltage is fixed, and the magnitude of the dc supply voltage varies independently, so that the average value of the voltage is controlled by varying \( \Delta t \). During normal operation, \( t_2 \) is equal to \( T/2 \) and \( t_1 \) is the variable. Because \( t_1 \) is variable, the bridge output is not a pure square wave but is a quasi-square-wave as illustrated in figure 1, curve c. The base drive voltages, for the power transistors of the bridge circuit, required to produce the quasi-square-wave ac voltages are shown in figure 1, curves a and b.
The quasi-square-wave voltage is rectified as illustrated in figure 1 (curve d) and is then filtered to remove the ripple. The dc output voltage is proportional to the average of the quasi-square-wave voltage; that is,

\[ V_{\text{out dc}} \approx kE_s \Delta t \]

where \( E_s \) is the value of the dc supply voltage and \( k \) is a proportionality constant.

**Block Diagram Description**

A block diagram of the dc-dc converter employing quasi-square-wave regulation of the output voltage is shown in figure 2. Typical waveforms for the functional circuits are illustrated in the diagram, and the operation of the circuits is now discussed.

**Generation of quasi-square-wave.** - A timing generator produces a narrow pulse at approximately 75-microsecond intervals which set the basic carrier frequency at 7 kilohertz (one-half the timing generator repetition rate). The regulator is then synchronized to produce a series of rectangular pulses at the timing generator frequency whose widths vary from 0 to nearly 75 microseconds depending on input voltage and load. The width of the pulses determines the duty cycle.

**Separation of quasi-square-wave into two-phase drive signal.** - A flip-flop is also synchronized to the timing generator and produces two square-wave outputs at one-half
the timing generator frequency. These two signals are complements of each other; that is, when one output is positive, the other is zero. Therefore, the two outputs appear as square waves with a $180^\circ$ phase shift between them. These two square waves are then combined with the quasi-square-wave in a pair of AND gates. These gates have a positive output if both the flip-flop signal and the quasi-square-wave are positive. Thus, because the square waves are complements, only one gate at a time can have a positive output. Signals of the same width as the quasi-square-wave appear alternately at the outputs of the gates as drive signals. The signals are identical but phase shifted $180^\circ$. These two drive waveforms are as shown in figure 1, curves a and b.

**Amplification of drive signal.** - The voltage and current drive sections (fig. 2) amplify the gate output voltages and produce currents sufficient to drive the four power stage transistors. More specifically, voltage drive amplifier A operates into a pair of current drive amplifier stages which provide the control for the associated pair of power output transistor switches. Voltage drive amplifier B, with the same wave shape but phase shifted $180^\circ$, similarly operates into a second pair of current drive amplifier stages which control a second pair of output transistor switches.
Formation and amplification of quasi-square-wave signal. - In the power output stage, the quasi-square-wave signal is formed by controlling a pair of transistor switches with each phase of the drive signal. These transistor switches function as a double-pole double-throw switch, alternating the polarity of the voltage applied to the transformer. To generate the dwell time when there is no output, there is a time when none of the transistors are on. A typical quasi-square-output-wave is shown in figure 1 as the bridge voltage, curve c. The peak voltage is nearly equal to the input voltage, and the pulse width is proportional to the duty cycle.

Step-up of voltage. - The output voltage of the power stage can be increased, or decreased, to any convenient level by a transformer located within the power output stage, which operates at the carrier frequency. This also provides isolation between the input and output voltages.

Rectification of high voltage quasi-square-wave. - The output of the transformer is rectified so that the result is a pulsating dc voltage. The peak voltage is proportional to the converter input voltage, and the pulse width is equal to the width of the original quasi-square-wave signal.

Filtering. - Filtering the rectified transformer output produces a dc output voltage proportional to the product of the converter input voltage and the duty cycle. If the duty cycle is changed as the input voltage changes, such that the product is nearly constant, the output voltage will be regulated, and, except for the effect of the output impedance, it will be independent of load.

CIRCUIT DESCRIPTION

Control Circuit

The operations of carrier frequency generation, voltage regulation, current limit, and drive signal steering are performed by this section of the circuit. The circuit is shown in figure 3 and key waveforms from this circuit are sketched in figure 4. Reference 2 describes the operation of the integrated circuits.

The timing pulse, which synchronizes all operations in the converter and determines the carrier frequency, is generated by a relaxation oscillator consisting of integrated circuit NAND gates IC\textsubscript{1A}, IC\textsubscript{1B}, and IC\textsubscript{1C} and components C\textsubscript{1} and D\textsubscript{1}. A NAND gate is an element whose output is in the high state if any of its inputs are low, or in the low state if all its inputs are high. To start the cycle, assume the outputs of gates IC\textsubscript{1A} and IC\textsubscript{1C} are high and IC\textsubscript{1B} is low. The voltage at point A rises as the input current of gate IC\textsubscript{1A} discharges C\textsubscript{1}. When the voltage of point A reaches the thresh-
Figure 3. - Converter control circuit.
old voltage of gate IC\textsubscript{1A}, its output goes down. This causes gates IC\textsubscript{1B} and IC\textsubscript{1C} to switch, clamping the input of IC\textsubscript{1A} to ground through D\textsubscript{1} and IC\textsubscript{1C}. Since the input of IC\textsubscript{1A} is now low, its output rises, charging C\textsubscript{1} as it rises. Gates IC\textsubscript{1B} and IC\textsubscript{1C} then switch and the cycle repeats. Because the charging current from the output of IC\textsubscript{1A} is much larger than the discharge current, the pulse (as shown in fig. 4) is very narrow, approximately 6 microseconds wide.

The frequency of oscillation is determined by an RC network, which consists of C\textsubscript{1} and two resistors inside the logic gate IC\textsubscript{1A}, and the threshold voltage of IC\textsubscript{1A}. The frequency varies several percent because of the temperature and supply voltage variations, but it does not affect the converter operation noticeably.

The timing pulse is used in the regulation loop and for drive signal steering. In the last application, the pulse, inverted because it is taken from the output of IC\textsubscript{1B}, is coupled to a flip-flop (IC\textsubscript{3A}). The flip-flop changes state with each pulse, and its two outputs Q and Q (see fig. 4) are connected to two NAND gates which steer drive signals alternately to voltage drives A and B.

The output voltage of the converter is determined by the width of the drive signal. A drive signal is generated during each cycle of the timing generator. Since the action of IC\textsubscript{3A} directs these drive signals alternately to opposite sides of the power bridge, the drive signal width is identical for both sides and the operation will be balanced.
The width of the drive signal is determined by the current $i$ fed back from the regulation loop. This current charges $C_2$, and the capacitor voltage $V_{C_2}$ rises linearly to a voltage determined by the zener diode $D_3$. When $V_{C_2}$ reaches this voltage, $D_3$ conducts, clamping $V_{C_2}$ and turning on $Q_1$. Transistor $Q_1$ stays on, generating a drive signal, until $C_2$ is discharged through $D_2$ by the timing pulse generator. The cycle then repeats. After $C_2$ is discharged, the delay before $Q_1$ again conducts; therefore, the drive signal width is determined by the magnitude of $i$, which is controlled by the regulator.

The regulation loop allows isolation between the control signal and the converter. For dc output-voltage regulation, the converter output is connected to the output sense points in figure 3. When the output voltage exceeds the level determined by $D_7$, $D_8$, $D_9$, $R_4$, and $R_5$, a current flows through the loop and $Q_2$ begins conducting. This places a load on $T_1$, since this secondary voltage is rectified by $D_6$ and applied to $Q_2$. The primary voltage of $T_1$ is a square wave obtained from flip-flop IC3B through series resistances $R_2$ and $R_3$. As the loading caused by $Q_2$ increases, the primary voltage decreases because of the increasing voltage drop of the resistors. As the transformer voltage is reduced, the voltage driving $Q_3$ is reduced. Transistor $Q_3$ operates as a current source, and reducing its drive reduces $i$ and the drive signal width, lowering the converter output voltage. Additional regulation loops may be added by adding secondary windings to $T_1$. If this converter is used to drive an inverter, it would be necessary to regulate from the inverter output. Figure 5 shows a method of accomplishing this without adding more windings to $T_1$. In this case, the dc regulation loop would then function as an overvoltage loop to protect the inverter. Also, because the dc regulation loop would be faster, it would limit the peak ac output during startup or load transients.

![Figure 5. - Modified regulation circuit.](image-url)
The overcurrent protection is designed to remove the drive signal whenever the instantaneous collector current of the output transistors exceeds a preset value. If the collector current exceeds this value, the voltage, generated by current transformer $T_6$ and rectifier $D_{25}$ (fig. 7) across $R_1$, will exceed the threshold of IC$_{4B}$ (fig. 3). A flip-flop formed by IC$_{4A}$ and IC$_{4B}$ then changes state removing the drive signal through $D_4$. The drive remains off until the timing pulse resets the flip-flop at the end of the cycle. As was stated in the expansion of quasi-square-wave regulation, the voltage regulation loop functions by controlling the leading edge of the wave $t_1$, whereas the current limit operates on the trailing edge of the drive wave $t_2$.

**Drive Circuit**

The function of the drive circuit is to amplify the drive signals from the control circuit and to couple them to the power stage transistors. The drive circuit consists of two voltage drive sections - one for each drive signal and four current drive sections (fig. 2), and one for each power stage transistor. The drive circuit for one phase of the bridge, consisting of one voltage and two current drive stages, is shown in figure 6.

The voltage drive uses a Darlington transistor ($Q_4$) driven from the NAND gate IC$_{2C}$ (fig. 2). A fast turnoff of the current-drive transistor is accomplished by using a
powdered metal core, which has low permeability, for \( T_2 \). The energy stored in the core increases as \( Q_4 \) conducts and this energy is released to provide a turnoff pulse for the current drive stages \( Q_6 \) and \( Q_8 \) when \( Q_4 \) turns off.

The current drive stage utilizes proportional current feedback from a pair of current transformers (\( T_4 \) and \( T_5 \)). The primary windings of these transformers are connected in series with the power transformer as shown in figure 7, and the secondary windings drive the base junctions of transistors \( Q_{10} \) and \( Q_{12} \) as illustrated in figure 6. Transistor \( Q_6 \) is driven by the voltage drive stage to initiate the current feedback.
When $Q_4$ turns on, $Q_6$ is turned on and a small amount of current is fed to the power stage transistor base junction by the voltage drive to start conduction in that stage. A current proportional to the collector current then increases the base current of $Q_{10}$ to hold it saturated. When $Q_4$ turns off, $Q_6$ is forced off and the current feedback from $T_4$ flows through $D_{14}$ instead of through $Q_6$ to $Q_{10}$. The turnoff pulse from $T_2$ also supplies a negative bias to $Q_{10}$. This negative bias speeds up the turnoff.

Each voltage drive controls two current drives, in phase, and each current drive controls one power transistor. Only two current transformers are used, in push-pull operation, which resets their cores automatically.

**Output Stage**

The power output bridge with the input filter $L_1$ and $C_8$, output filter $L_2$ and $C_{10}$, and output rectifiers $D_{26}$ to $D_{29}$ is shown in figure 7. The output transistors form a conventional four element full bridge (ref. 3) with the main current path shown in heavy lines. The four diodes $D_{21}$ to $D_{24}$ return reactive currents from the power transformer to the power supply. In conjunction with capacitors $C_6$ and $C_7$ they also eliminate voltage spikes at the power transistors.

The power transformer $T_7$ uses a toroidal core wound to minimize stray capacitance and leakage inductance. The leakage inductance of $T_7$ combined with the switching characteristics of the bridge rectifiers $D_{26}$ to $D_{29}$ produces voltage spikes at the rectifier output that are damped by the resistive-capacitive network $R_{21}$ and $C_9$. Fast recovery rectifiers are also required to minimize these spikes.

**TEST RESULTS**

A breadboard model of the converter was built and tested using bench power supplies and a load bank. Also, separate power supplies were used to power the control and voltage drive circuits. Input and output voltage and current measurements were made with 1/4-percent accuracy or better meters; therefore, the overall efficiency measurements are accurate within 1 percent.

**Efficiency**

The overall efficiency of the converter as a function of input voltage and output power is plotted in figure 8. The peak measured efficiency was greater than 92 percent.
at a 600-watt output with a 56-volt input, and it was almost independent of the input voltage. For any input within the +10 to -20 percent input voltage range, the efficiency varied less than 2 percent except at very low power outputs. The efficiency shown included all the drive, control, and regulator losses, but it did not include low level (15-V) power supply losses. It is estimated that these losses would not exceed 2 watts and, therefore, would have a negligible effect on the overall efficiency, except at very low output powers. This converter was better than 70-percent efficiency at 1-percent rated output, and it consumed approximately 1 watt with no load on the output. The approximate losses of the major components and subsystems are given in table I for the converter operating with a 56-volt input and 1-kilowatt load.

![Figure 8. Overall converter efficiency against output power. Output voltage, 200 volts.](image)

**TABLE I. MAJOR COMPONENT AND SUBSYSTEM LOSSES**

<table>
<thead>
<tr>
<th>Component or subsystem</th>
<th>Loss, W</th>
<th>Percent of total loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power stage transistors</td>
<td>35</td>
<td>32</td>
</tr>
<tr>
<td>Output transformer</td>
<td>30</td>
<td>27.5</td>
</tr>
<tr>
<td>Current drive system</td>
<td>20</td>
<td>18</td>
</tr>
<tr>
<td>Output filter inductor</td>
<td>5</td>
<td>4.5</td>
</tr>
<tr>
<td>Output rectifiers</td>
<td>5</td>
<td>4.5</td>
</tr>
<tr>
<td>Output filter resistor-capacitor (R_{21-C_9})</td>
<td>5</td>
<td>4.5</td>
</tr>
<tr>
<td>Control and voltage drive</td>
<td>5</td>
<td>4.5</td>
</tr>
<tr>
<td>Wire losses and miscellaneous</td>
<td>5</td>
<td>4.5</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>110</strong></td>
<td><strong>100.0</strong></td>
</tr>
</tbody>
</table>
Weight

The total component weight of this converter is only 6 pounds (2.7 kg), and more than 60 percent of this weight is due to magnetic items. Consequently, further weight gains could be expected, with a decrease in efficiency, if the frequency were increased. Table II contains the weights of the major components used in the breadboard converter. No size or weight estimates were made for a packaged system.

<table>
<thead>
<tr>
<th>Component or subsystem</th>
<th>Weight</th>
<th>Percent of total weight</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output transformer</td>
<td>28 oz</td>
<td>0.80 kg 29</td>
</tr>
<tr>
<td>Output filter inductor</td>
<td>17 oz</td>
<td>0.48 kg 18</td>
</tr>
<tr>
<td>Current drive system</td>
<td>13 oz</td>
<td>0.37 kg 14</td>
</tr>
<tr>
<td>Power stage transistors</td>
<td>12 oz</td>
<td>0.34 kg 13</td>
</tr>
<tr>
<td>Input filter inductor</td>
<td>10 oz</td>
<td>0.28 kg 10</td>
</tr>
<tr>
<td>Input filter capacitor</td>
<td>5 oz</td>
<td>0.14 kg 5</td>
</tr>
<tr>
<td>Voltage drive system</td>
<td>5 oz</td>
<td>0.14 kg 5</td>
</tr>
<tr>
<td>Reactive diodes and rectifiers</td>
<td>4 oz</td>
<td>0.11 kg 4</td>
</tr>
<tr>
<td>Control circuit</td>
<td>2 oz</td>
<td>0.06 kg 2</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>96 oz</td>
<td>2.72 kg 100</td>
</tr>
</tbody>
</table>

Voltage Regulation

Figure 9 illustrates the change in duty cycle as a function of load and input voltage. The slope of the straight sections of the curves at high output powers is determined by the open loop output impedance of the converter, which is approximately 6 ohms. At low power levels the output filter becomes less effective and the output capacitor tends to charge to peak voltage. The duty cycle then decreases further to compensate.

Voltage regulation was approximately ±1 percent. Transient response, which was approximately 5 milliseconds for a step increase in load, increased to approximately 50 milliseconds for a decrease from full load to 1-percent load. This was caused by a slight overshoot and the long response time of the resistor-capacitor (R-C) combination formed by the load and output capacitor. Response time from full load to half load was only 1 millisecond. The regulator was stable for all loads, but there was some ringing caused by the step changes in load.
Off-Limit Operation

The converter would operate and regulate with input voltages up to 150 percent of the rated input. But above that, peak ratings of several semiconductors in the circuit would be exceeded. Too low an input does not cause any damage as long as the drive circuit has full voltage, but the output voltage will be reduced.

An overcurrent circuit was incorporated to limit the collector current in the output transistors to a 75-ampere peak. This circuit is sufficient to protect the converter during startup, overload, and short-circuited output. And, output transistor failure is prevented even in the event of some types of internal failures.

Filtering

Output current ripple waveform into the filter capacitor and load was triangular (fig. 1, curve e) with an amplitude of 2 amperes peak-to-peak at 14 kilohertz superimposed on the direct current output. The input ripple wave was of a similar shape but was not measured.

DISCUSSION

Reliability is of prime importance in all aerospace equipment. One approach to
reliability is the incorporation of protective devices throughout the system. But such
designs result in increased complexity and the need for more critical parts. This con-
verter, using fewer than 100 parts, requires no selected, matched, or precision com-
ponents and only three variable resistors, if \( R_4 \) is used to set the output voltage pre-
cisely.

The control circuit already utilizes several integrated circuits, and hybrid thin-
or thick-film circuits could replace most of the discrete components. Power dissipa-
tion and peak stress in the control and voltage drive sections are very low, contributing
to long-life expectancy. Total power dissipation in these sections is approximately
1 watt. Voltages, current, and powers in the current drive and output stages are much
higher, but the ratings are at least 150 percent of the peak stresses.

Current drive tends to keep the power output transistors saturated because the
base current is proportional to the collector current. This protects the power transis-
tors from the high dissipation that would result if they came out of saturation at a high
current level. Because of the high switching speed of the output transistors, sweepout
currents (ref. 4) are not required, thereby preventing possible base junction degrada-
tion.

Because it is effectively a series connection of transistors, bridge output circuits in-
herently reduce the voltage across the transistors by a factor of 2, but they can, however,
suffer high peak currents due to transistor switching characteristics (ref. 3). If one
pair of transistors is turned on at the same time as, or before, the other pair is turned
off, a short-circuit path will exist across the power supply, through these transistors,
during the switching interval due to the finite turnoff time of all transistors. In this
circuit, the peak current \( i \) charging \( C_2 \) is limited, and thus a minimum delay
is produced before \( Q_1 \) turns on and begins the drive pulse. If this delay is made greater
than the turnoff time of the slowest transistor, these short-circuit currents are elim-
inated. In practice, this minimum delay is not critical and the adjustment made by
varying \( R_8 \) could be eliminated. The only effect is a change in the minimum input
voltage required for full output voltage.

The penalty paid for the reliability of the full-bridge output circuit is the large num-
ber of power transistors required, each with its collector-emitter drop and base drive
losses. The two transistor circuit illustrated in figure 10 would seem to reduce the
drive and collector-emitter losses considerably. But the higher voltage transistors re-
quired for this circuit do not exhibit gain or saturation characteristics comparable to
those of available low-voltage transistors, thereby cancelling most of the possible ad-
vantages. Also, the power transformer for the two transistor circuit would have to be
larger to be equally efficient; thus, the voltage spike problems would be more severe,
and the reliability would therefore be reduced.

The bridge circuit used requires only a very simple transformer with no split or
tapped windings. This is an advantage as the winding configuration is very important. Stray capacitance and inductance must be minimized for efficient and reliable operation. The transformer used, which had a relatively low permeability core ($\mu = 205$) and operated at a high flux density of 5 kilogauss (0.5 tesla), attained a high efficiency with low weight because of the low core loss and toroidal winding. Also, because of the non-square loop core characteristics, accurate balancing was not required to prevent saturation.

The proportional current drive system was also necessary to achieve the high efficiencies, especially at low output levels, because the drive power is nearly proportional to the collector current. In a nonproportional drive system, the drive power is nearly constant, but does increase at low levels of output power because of decreased base to emitter voltage drop. And the transistor switching speed is reduced at low collector currents because of the constant drive current building up an excessive amount of stored charge in the base region. This reduced switching speed also generally increases switching losses. In the system used in the converter, the control and voltage drive circuits account for much of the loss at very low-power levels, and collector-emitter dissipation accounts for most of the power loss at high-power levels. Larger output transformers and filters alone could extend the high power range slightly with good efficiency, but for good gain and saturation characteristics and increased reliability, the power transistors should be operated at less than one-half of their peak current ratings. Therefore, paralleled transistors would be required for greatly increased power output.

Figure 10. - Two transistor power stage.
CONCLUDING REMARKS

It was shown that high-performance medium power dc-dc converters could be built utilizing readily available components and relatively simple circuitry.

The efficiency was high and nearly constant over a broad operating range. It held above 87 percent from 150 watts to 1.2 kilowatts output with the input varying from 44.8 to 61.6 volts. Peak measured efficiency was greater than 92 percent at 600 watts and only dropped to 70 percent at 1 percent of rated output. Standby or no load power consumption was approximately 1 watt.

Electrical component weight was 6 pounds (2.7 kg). Nearly 60 percent of the weight is concentrated in the magnetic components. It is believed that these parts could be optimized for a specific mission. This optimization would reduce the efficiency slightly for a weight reduction of up to 25 percent.

The quasi-square-wave regulation and control circuit was simplified by the extensive use of integrated circuits, which also reduced the power consumption. Voltage regulation was ±1 percent from no load to full load for rated input voltage. Overload protection was included, and the input voltage could increase to 150 percent of rated input with complete regulation and no damage.

Most of the magnetic components used powdered-metal cores (Ni-17Fe-2Mo). The efficient performance of this converter was largely attributable to these cores. Core loss was very low, and their nonsquare-loop characteristics eliminated the need for balancing the circuit.

Lewis Research Center,
National Aeronautics and Space Administration,
Cleveland, Ohio, October 28, 1969,
120-27.

REFERENCES


Reference designation | Part number | Description |
--- | --- | --- |
C1, C2, C6, C7, C8, C9, C10 | 1N549 | 0.005 μF, 600 V, ceramic |
D1, B2, D4, D9 | IN755 | 40 mA, 175 V |
D5, D6, D25, D26, D27, D28, D29, D30 | IN3581 | 10 A, 50 V |
R1, R2, R4, R9, R11, R12 | IN29708 | 10 W, 6.2 V |
B3 | 2N640 | 12 A, 400 V, fast recovery |
B4 | 2A10 | 12 A, 600 V, fast recovery |
R3 | MC672 | Quad input gate |
R7 | MC683 | Dual J-K flip-flop |
Q1, Q2 | 2N722 | 0.5 A, 50 V |

Figure 11. - Converter
<table>
<thead>
<tr>
<th>Reference designation</th>
<th>Part number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q_3</td>
<td>2N4036</td>
<td>1A, 90V</td>
</tr>
<tr>
<td>Q_4, Q_5</td>
<td>2N3230</td>
<td>7A, 80V, Darlington</td>
</tr>
<tr>
<td>Q_6, Q_7, Q_8, Q_9</td>
<td>2N3264</td>
<td>25A, 100V</td>
</tr>
<tr>
<td>Q_{10}, Q_{11}, Q_{12}, Q_{13}</td>
<td>MHT8923</td>
<td>90A, 140V</td>
</tr>
<tr>
<td>R_1</td>
<td></td>
<td>500Ω, 0.5W, variable</td>
</tr>
<tr>
<td>R_2, R_3</td>
<td></td>
<td>1800Ω, 0.5W</td>
</tr>
<tr>
<td>R_4</td>
<td></td>
<td>22000Ω, 0.5W</td>
</tr>
<tr>
<td>R_5</td>
<td></td>
<td>10000Ω, 0.5W</td>
</tr>
<tr>
<td>R_6</td>
<td></td>
<td>33000Ω, 0.5W</td>
</tr>
<tr>
<td>R_7</td>
<td></td>
<td>100000Ω, 0.5W</td>
</tr>
<tr>
<td>R_8</td>
<td></td>
<td>10000Ω, 0.5W, variable</td>
</tr>
<tr>
<td>R_9, R_{10}</td>
<td></td>
<td>1500Ω, 0.5W</td>
</tr>
<tr>
<td>R_{11}, R_{12}</td>
<td></td>
<td>47Ω, 0.5W</td>
</tr>
<tr>
<td>R_{13}, R_{15}, R_{17}, R_{19}</td>
<td></td>
<td>100Ω, 0.5W</td>
</tr>
<tr>
<td>R_{14}, R_{16}, R_{18}, R_{20}</td>
<td></td>
<td>15Ω, 10W, tapped at 7.5Ω</td>
</tr>
<tr>
<td>R_{21}</td>
<td></td>
<td>130Ω, 3W</td>
</tr>
<tr>
<td>T_1</td>
<td></td>
<td>Control transformer, 1:1:1</td>
</tr>
<tr>
<td>T_2, T_3</td>
<td></td>
<td>Drive transformer, 3:1:1</td>
</tr>
<tr>
<td>T_4, T_5</td>
<td></td>
<td>Drive transformer, 1:8.5:8.5</td>
</tr>
<tr>
<td>T_6</td>
<td></td>
<td>Current transformer, 5000:1</td>
</tr>
<tr>
<td>T_7</td>
<td></td>
<td>Output transformer, 5:5:1</td>
</tr>
</tbody>
</table>

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