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STUDY OF FAILURE MODES OF MULTILEVEL LARGE SCALE INTEGRATED CIRCUITS

by Earl S. Schlegel

Prepared by
PHILCO-FORD CORPORATION
Blue Bell, Pa.
for Electronics Research Center

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By Earl S. Schlegel

1. Integrated Circuits

Prepared under Contract No. NAS 12-544 by
PHILCO-FORD CORPORATION
Blue Bell, Pa.

for Electronics Research Center

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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SUMMARY

Empirical and theoretical investigations of the factors that affect the fundamental electrical properties of the $Si-SiO_2$ interface have resulted in techniques for improving the reliability and performance of large scale multilevel microcircuit arrays.

A new set of test structures has been prepared to evaluate the fundamental electrical properties of oxide-silicon interfaces of the types likely to be found in large scale multilevel microcircuit arrays. This set was designed for use on wafers with production MOS microcircuits. The set includes a sufficient number of test structures to represent each type of region in a microcircuit. The set includes both new test structures and previously existing structures redesigned to have improved sensitivity. A discussion is given of the considerations involved in the design of each test structure in the set and of problems that arise in their use.

An additional effect of the introduction of a second layer dielectric has been postulated. Tests have been proposed that might be applied to simple leakage current measurements taken on complex circuits to identify the cause of degradation or failure. MOS transistors, with and without a second layer dielectric, have been subjected to an accelerated aging test and parameter shifts were measured. Samples containing aluminum oxide and silicon nitride were evaluated.

Techniques are given for measuring field inversion voltages in regions not covered by metal. Experimental data are given that compare the field inversion voltage under metal to that in regions not under metal, and the importance of the difference between these voltages is discussed. Experimental data are given on fast state annealing and it has been shown that the process that anneals fast states from beneath metal does not anneal them from under narrow metal lines. The effects of processing variables on surface recombination velocity have been measured, and compared with the effects of these variables on leakage current. Direct measurements of the surface conductivity of insulator layers used in microcircuits have shown vapor plated phosphosilicate to have a surprisingly low surface conductivity. Data have been taken that further support a postulate that mobile ion densities in an oxide are influenced by the presence of a p-n junction.

INTRODUCTION

Background

This is the fourth Scientific Report on a program of both theoretical and experimental studies designed to improve the understanding of the means by which large scale integrated (LSI) circuitry can be made to yield the predicted improvements in microcircuit reliability.

In previous Scientific Reports on this program, we reviewed in detail each of the known surface-related factors that might be expected to influence the reliability of LSI circuitry. We also discussed the increased complexity of the fabrication processes required to build LSI circuitry and indicated possible ways in which the new materials, new processes or the new level of complexity might be expected to contribute to the problem of maintaining the desired reliability of the circuitry.

Our investigations have been designed to provide information that is applicable both to bipolar and MOS microcircuit structures. We have continued to maintain cognizance of an extensive body of published literature so that our efforts can be effectively directed to pursue the most important and most useful results with a minimum of repetition of previously reported work, and a minimum amount of work that would be difficult to relate to the LSI technology in general use today. We have studied the implications of discernible

trends in microcircuit technology insofar as future microcircuit reliability is concerned.

Objectives

The objectives of this program are to:

1. Develop fundamental information to improve the understanding of possible failure modes of LSI circuitry.
2. Develop basic models to facilitate the discussion and understanding of the variations in the performance and reliability of LSI circuitry.
3. Develop test structures for measuring the fundamental parameters of the oxide-silicon interface.
4. Correlate data taken from test structures with that taken from actual devices so as to determine which individual effects have degraded the yield or reliability.
5. Establish practical techniques for eliminating or circumventing effects referred to in 4.

The scope of this program has been limited to yield and reliability problems related to the electrical properties of the insulator-silicon interface in microcircuits. Although the limited scope of this program does not include reliability problems due to

pinholes in the dielectric layer, contact resistance, or metal continuity over oxide steps, Philco-Ford has other programs in which these other factors of microcircuit performance and reliability are being studied. Some of the results of these other efforts have been reported in a paper by Schnable and Keen[1].

Summary of Accomplishments Reported in Previous Scientific Reports

The most significant accomplishments covered by the previous three Scientific Reports include the following:

1. The preparation of an extensive bibliography of pertinent literature.
2. The development of a useful comprehensive model that embodies each of the known possible factors that influence the performance and reliability of large scale multilevel integrated circuits.
3. The design and fabrication of monolithic integrated circuit test structures for the evaluation of LSI production processes, and the evaluation of these test structures on conventional microcircuit wafers.
4. The use of these test structures to study the effects of variations in the materials and processes used in the fabrication of LSI circuits.

5. The development, based on 1 through 4 above, of a next generation of test structures to provide more complete information on the fundamental properties of the oxide-silicon interface.

6. The development of a broad general understanding of the various ways in which test structures can be effectively used for process development, in-process control and for reliability studies.

7. The development of a broad range of techniques for obtaining the most useful information from test structures. Examples of such possibilities include:

   a. The comparison of data taken on different test structures on the same chip to yield information not available on the individual test structures.

   b. The comparison of data taken under different ambient conditions.

   c. The creation of test structures from standard production microcircuit structures by means of a simple change in the metal pattern.

8. The proposal and development of techniques both for measuring and preventing the degrading effects of surface ions on microcircuit structures.

9. The demonstration, both experimentally and theoretically, of the importance of studying every one of the types of regions in a microcircuit.

10. The evaluation of a number of types of insulator layers made of various materials and by various processes for their possible use as second-layer materials for multi-level microcircuits.

11. The discovery of what appear to be two types of gettering of mobile ions from oxides.

12. The collection of data that show how the electrical properties of an oxide change as the oxide is subjected to each step in a complex bipolar microcircuit production process.

13. The taking of experimental data to determine the effects of a deposition of a vapor-plated second-layer oxide on the parameters of transistors, of both the MOS and bipolar type, in production microcircuits.

14. The study of the effects of a deposited second-layer insulator on the stability of transistors in production bipolar microcircuit chips.

The contract, as amended, also provides that the program shall include consultation, and the preparation and delivery of samples as specifically requested by the program monitor in support of this and other program efforts. A significant amount of effort has been directed toward these areas, including a number of meetings and telephone conversations, a visit at NASA/ERC by G. L. Schnable of Philco-Ford and one at Philco-Ford, Blue Bell, Pa. by R. Yatsko and R. Beatty of NASA/ERC. A part of the consultation activities consisted of the submission of letters that reviewed the current state-of-the-art in aluminum metallization and electromigration, and provided detailed bibliographies on these topics. We suggested a microcircuit for investigators at NASA/ERC to use to create a proven process capability for making p-channel enhancement mode MOS microcircuits and supplied a set of masks for this purpose.

NEW GENERATION OF TEST STRUCTURES

In the first Scientific Report on this program we describe (pages 41-49) a set of basic test structures that were designed to provide a means for measuring the fundamental electrical properties of the insulator-silicon interface. The demonstration of the effectiveness of these test structures in a wide range of applications for the study and control of the electrical properties of the insulator-silicon interface has been a primary subject of each of the Scientific Reports on this program.

Because of our satisfaction with the results from that set of test structures, we have designed and built, with Philco-Ford funds, a new set of test structures that is intended for use as a universal set that can be included on any mask set used for making production MOS microcircuits. The availability of this set of test structures significantly improves our capability for controlling the process used for making production quantities of MOS circuits and for finding the exact cause and nature of yield or reliability problems.

The improvements of the new set of test structures over the previous set include the following:

1. It has been designed to be fabricated with exactly the same process used to make the production microcircuits.

2. It includes test structures for the evaluation of each type of area in the microcircuit -- thin or gate oxide under metal, thick or field oxide under metal, and thick or field oxide not under metal. The importance of this capability is demonstrated and discussed in subsequent sections of this report.

3. New types of test structures have been created and improvements have been made in the sensitivity of some of the previously existing test structures.

In this section of this report, we present in detail the considerations involved in the design of each of the individual test structures in this new set and discuss the results of our evaluation of them. Figure 1 is a photograph of a chip having this new set of test structures with identifying numbers to facilitate the following discussion.

Structure No. 1 is an MOS capacitor with thick oxide. Two main considerations were taken into account in the design of this structure. First, the oxide in this structure must be prepared in the same way as that in the field regions of the microcircuit so that it properly represents the field regions of the microcircuit. Second, the area must be sufficiently large so that the capacitance is significantly larger than the unavoidable capacitance of the package or of the probing apparatus used to

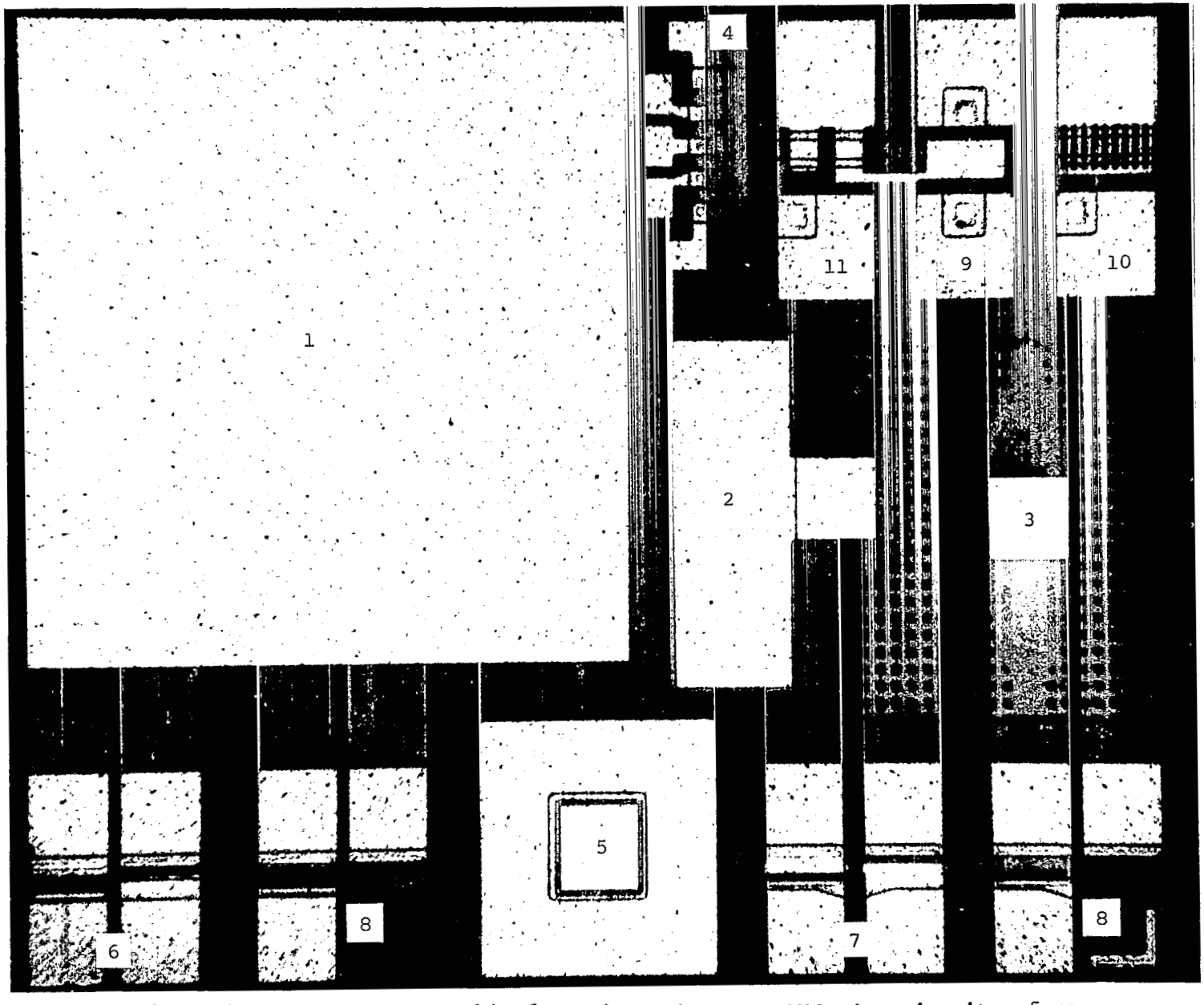


Figure 1. Test structure chip for universal use on MOS microcircuit wafers.

take measurements. This capacitor has an area of 30 x 30 mil^2. It can be used to measure:

1. Effective charge density contained in the oxide and at the insulator-silicon interface. The effective charge density can be calculated from the flat band voltage and the thickness and dielectric constant of the oxide. The type of charge (mobile or immobile charge and charge in slow states or fast states) can be at least partially determined by studying the effect of an applied bias, a temperature change or a combination of the two.
2. Oxide thickness.
3. Average resistivity of the silicon in the depletion layer.

Structure No. 2 is an MOS capacitor on thin oxide. A contact land was located on thick oxide so that the wire bonds would not have to be made over the thin oxide. The oxide in this case is made in the same way as the oxide in the gate regions of the MOST's. The area of this capacitor can be smaller by the ratio of the thickness of the thin oxide to that of the thick oxide to have the same capacitance as that of the capacitor having the field oxide. The applications of this capacitor are the same as those for structure No. 1.

Structure No. 3 is a diffused p-n junction that has been designed to have a high periphery-to-area ratio to increase its sensitivity to effects at the periphery. This device can be used to measure device characteristics such as diode reverse current and diode breakdown voltage. These parameters provide a measure of more fundamental properties such as surface recombination velocities, fast state densities and effective charge densities in the oxide.

Structure No. 4, shown enlarged in Figure 2, is a new experimental test structure that is intended to provide a measure of the amount of lateral diffusion beyond the edge of a diffusion cut. This information is necessary if one is to have a good measure of the metallurgical length of the channel region of an MOS transistor. The knowledge of the metallurgical channel length is necessary for the calculation of the carrier mobility from the transconductance of an MOS transistor. The use of Hall measurements, as discussed on pages 43-45 of the first Scientific Report, for measuring carrier mobility is fairly impractical for purposes other than research.

This structure has diffused p-type regions that were formed with the diffusion of the p-type regions in the microcircuit. Referring to Figure 2, the spacings of p-type regions A, B, C, D and E from p-type region F are 0.30, 0.25, 0.20, 0.15 and 0.10 mils,

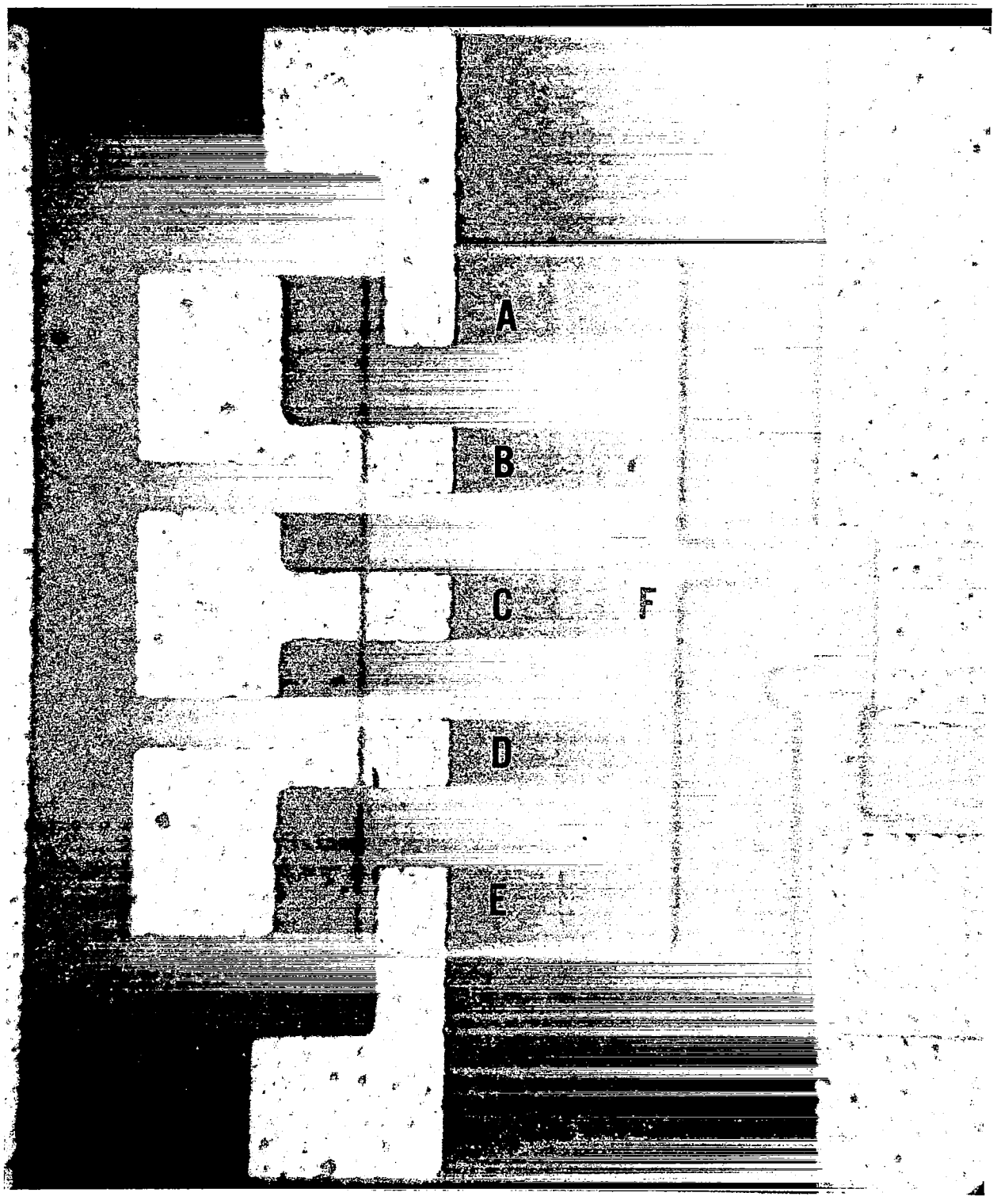


Figure 2. Test structure for measuring lateral diffusion.

respectively. By measuring the current-voltage relationship between these p-regions one can determine which of the regions are shorted and which are not. From this information one can obtain a good measure of the amount of lateral diffusion under the mask. A good measure of the channel length is important if one is to have a good understanding of the relative influence of the various known factors (channel length, oxide thickness and carrier mobility) on device performance.

An alternative technique for measuring lateral diffusion is angle lapping and staining. Angle lapping and staining has a number of undesirable aspects. First, it is fairly difficult to perform, time consuming and requires special equipment. Second, it destroys the chip -- which could be a problem if only a few test structure chips are included on each production wafer. Most importantly, the accuracy of the edge of a stained region as a measure of the location of the electrical or metallurgical junction has never been established.

Structure No. 5 is a gate controlled diode (a p-n junction with an overlapping gate electrode). This structure is similar to one in the previous set of test structures except that, because this set is intended only for use with circuits having p-type diffusion into n-type silicon, the second gate electrode is not included. This second gate is not needed because the

charge in oxides is always found to be positive and therefore there is no need for a gate to limit the area of the inversion layer. As described in the earlier reports, this structure is useful for measuring the surface recombination velocity as described by Fitzgerald and Grove.[2] It is also useful for measuring fast state densities. The technique for measuring fast state densities has been discussed by Deal et al.[3] In this technique, the capacitance-voltage relationship of the gate electrode is measured with the p-type region shorted to the substrate. Under these conditions the observed capacitance-voltage relationship has the shape of the low frequency curve described by Grove et al.,[4] i.e., in the region in which the inversion layer exists the capacitance approaches that of the oxide because the p-type region can supply carriers to the inversion layer in time periods that are short relative to the period of the measuring signal. If there are no fast states, the voltage range over which the capacitance is low is relatively narrow. On the other hand, if a significant number of fast states are present they must be filled before an inversion layer forms, and therefore the range of low capacitance in the capacitance-voltage curve is relatively wide. The width, then, of this "valley" in the C-V curve is a measure of the fast state density. This technique has also been demonstrated by Kooi.[5] This technique provides a measure only

of the number of fast states that were filled or emptied to form the inversion layer. Since the statistics for occupancy of the fast states is not only a function of the applied voltage but also of the temperature, one might expect to find further information concerning the fast state density if one were to study the capacitance voltage relationship at several temperatures. Deal et al.[3] have shown that the width of the valley in the capacitance-voltage relationship is significantly increased if the temperature is reduced to 77°K, and this increase provides another measure of the fast state density.

We find that the fast state density of devices having aluminum metallization is reduced to a negligible level during the wire and header bonding operations. It might be desirable at times if one could measure the fast state density on a wafer or a chip without subjecting it to the annealing temperatures involved in header and wire bonding but it is impractical to probe a structure of this size and to maintain the proper probe positions through this large a temperature excursion. The impracticality of this measurement is not a serious problem since fast state densities that do not survive the packaging operations present no problem in the finished device. On the other hand this technique is valuable for the evaluation of materials such as silicon nitride[3]

that impede the motion of the species that are involved in the annealing operation.

Structure No. 6 consists of two MOS transistors having a common source and field oxide under their gates. One of these transistors has its gate connected to a p-type region while the gate metal of the other transistor is not connected to silicon. It should be noted that the gate of every MOS transistor in a circuit is connected to silicon somewhere in the circuit. On the other hand, test structure discrete transistors on chips or wafers usually do not have their gate metal connected to silicon so that they can be used to measure the breakdown voltage of the oxide. Having these two structures on the same chip, one is able to determine the importance of having the gate metal tied to silicon and to establish whether future discrete MOS transistors designed to serve as test structures should have the gate connected to silicon.

Structure No. 7 is very similar to structure No. 6 except that the oxide under the gate is thin instead of thick as in structure No. 6. The difference in the shape of the p-type regions was chosen to minimize the sensitivity of the channel geometry to the alignment of the masking operations.

Structures No. 8 are similar to structures No. 6 and 7 but they do not have gate metal. These structures make it possible

to study breakdown and punchthrough voltages without the complicating influence of the gate metal. These structures are new and represent another attempt to obtain an electrical measure of variations in channel length. The presence of the metal in structures No. 6 and 7 influences the state density because of its influence on the annealing of the fast states. Further, and more importantly, it influences the density of the charge on the oxide surface during a measurement of breakdown or punchthrough voltage because the presence of the metal provides, in effect, a large number of allowed states for electrical charge and a path by which charge can easily flow to these states. These structures can also be used as bipolar transistors, the current gain of which provides another measure of the fast state density. (The dependence of lateral bipolar transistor current gain on surface potential -- which can be varied by applying voltage to the gate metal -- can be measured on either structures No. 6 or 7).

Structures No. 8 can also be used to measure the inversion voltage in regions not covered by metal by depositing conductive paste over the channel region.

Structure No. 9 is an MOS transistor having a channel length of 2 mils instead of 0.4 mil as in structure No. 6. The oxide thickness under the gate is that of the field oxide. This structure is intended for studies of phenomena that are dependent

on the length of the channel. One such effect was described on pages 84 and 85 of Scientific Report No. 3.

Structure No. 10 is for the study of surface ions. It is similar to the surface-ion test structure in the first set of test structures. The utility of the first surface-ion test structure was described in references 6 and 7. We have increased the number of gate digits in this device in order to increase its sensitivity. An unexpected finding (discussed on pages 55-57) with this test structure made us aware that this structure is also useful for studying phenomena associated with narrow metal line widths.

Structure No. 11 is also intended for studying surface-ion effects. The difference between structures No. 10 and 11 is that No. 10 is intended for use in structures having no insulator layer over the metal, while No. 11 is for use when there is an insulator layer over the metal. The wider digits of No. 11 provide room for openings in the layer of insulator over the metal so that surface ions can flow from the metal to the top layer of insulator -- to increase the sensitivity of the device to surface-ion effects.

In addition to the eleven test structures described above, the geometry of the p-type regions in the area between structures No. 4 and 11 makes it possible to use conductive paste to measure field inversion voltage in a region not covered by metal.

The new set of test structures was designed into a chip 52 x 62 mil^2, a size that permits its inclusion on the large majority of our production microcircuit wafers.

This set of masks can be used with each of our processes that are used for producing MOS circuits in large volume.

We have established that each of these test structures fulfills its intended purpose. Experimental data from structures like those in the new set other than structures No. 3 and 4 have been described in previous Scientific Reports. Structure No. 3 is a rather complex p-n junction, and it could be expected to exhibit poorly shaped current-voltage curves. Figure 3 shows a photograph of a typical I-V curve obtained from this structure. An enlarged view of structure No. 4 is shown in Figure 2 (page 12). Referring to Figure 2, Figure 4 shows I-V curves measured across the terminals indicated. Also shown is a plot of the punchthrough voltage as a function of the measured spacing between the edges of the diffusion cuts. In Figure 5 we show a photograph of similar I-V curves taken on a chip near the middle of a wafer and on another chip near the edge of the wafer. These photographs demonstrate the simplicity of the use of this test structure for measuring the uniformity of the diffusion and masking over the wafer.

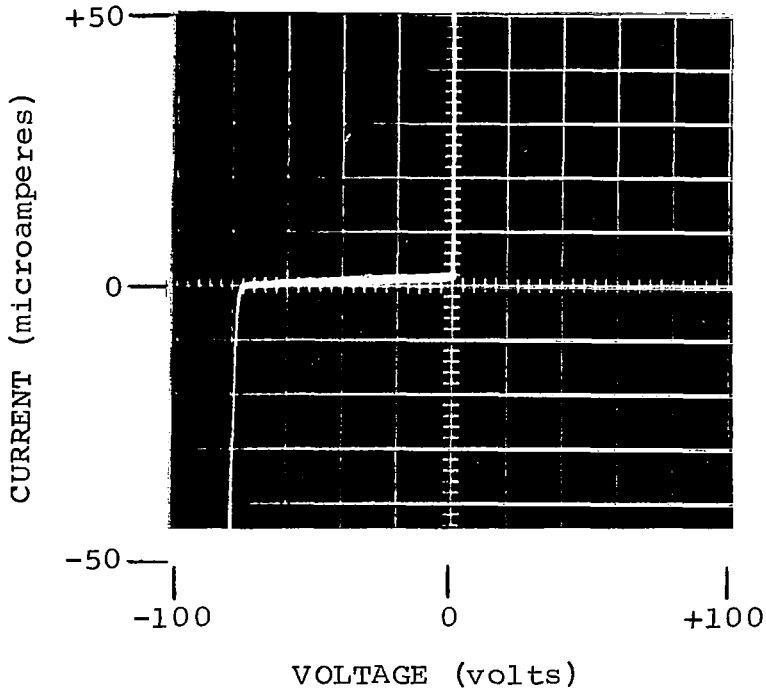


Figure 3. Current-voltage characteristics of test structure No. 3.

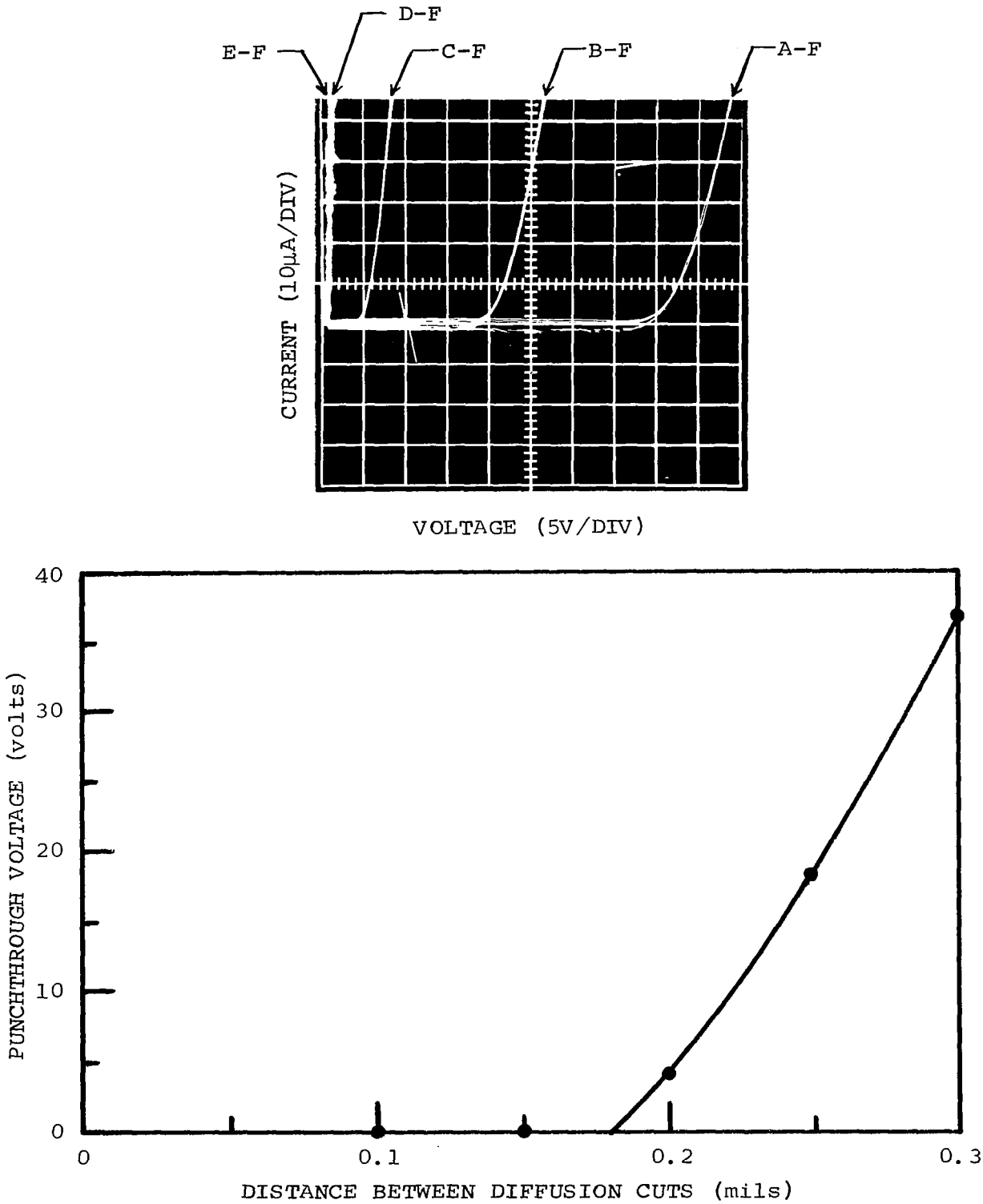
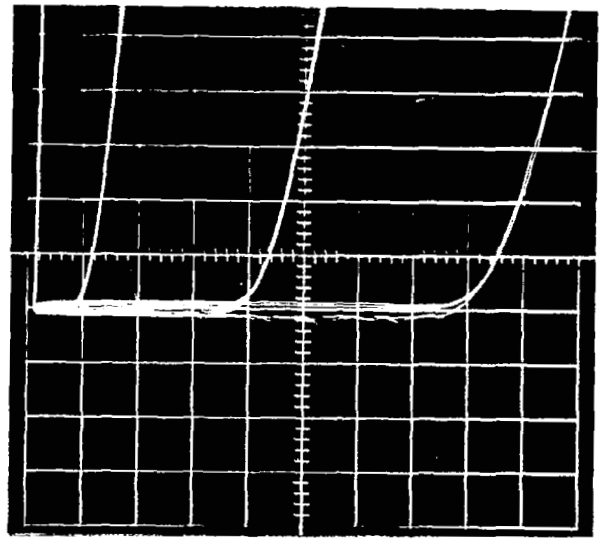
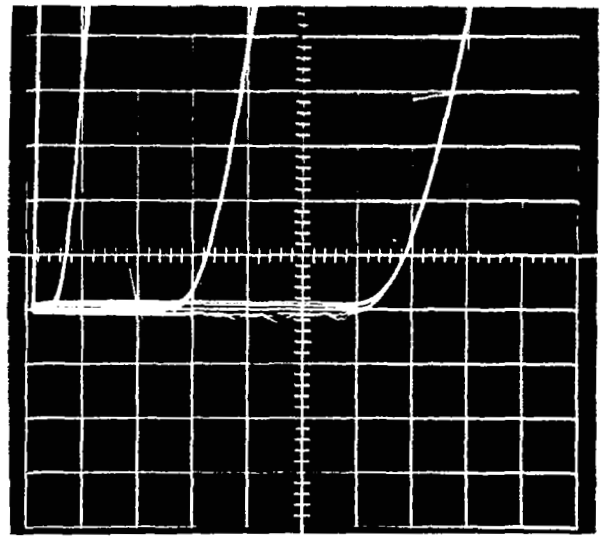


Figure 4. Data from test structure for measuring lateral diffusion



a. Middle of wafer.



b. Edge of wafer.

Figure 5. I-V curves taken on test structure for measuring lateral diffusion -- variation on a wafer.

THEORETICAL STUDIES

Our theoretical studies during this reporting period in the program were concentrated in three areas:

1. The question of whether a punchthrough voltage or a field-enhanced avalanche-breakdown voltage is being measured between two adjacent, p-type diffused regions separated by a homogeneous n-type region. These voltages occur between source and drain regions in MOS microcircuits or between base and resistor regions in bipolar microcircuits.
2. The development of techniques for determining the reason for degradation or failure in an individual microcircuit.
3. A qualitative analysis of the effects of a second layer oxide on the electric field strength near the oxide-silicon interface.

Punchthrough or Breakdown Voltage

Microcircuits with high resistivity regions have significant yield and reliability problems because the inversion voltage in the regions of the microcircuit structure having thick oxide is too low. If the inversion voltage is too low, a voltage on

a metal that bridges two p-type regions can form an inversion layer or channel which degrades the isolation between the two p-type regions and thereby degrades or causes failure of the circuit. For this reason it is important to have test structures for measuring the field inversion voltage. Suitable test structures for this purpose are MOS transistors having an oxide under the gate similar (in thickness and in preparation) to that in the field of the microcircuit.

MOS transistors are frequently tested as two-terminal devices (with the gate and drain common and the source and substrate common) because two-terminal measurements can be performed more easily on an automatic tester than can three-terminal measurements. The two-terminal measurement is good for transistors that have either a long channel region or a thin oxide over the channel. On the other hand, a transistor having thick oxide such as that in the field of a microcircuit, and a channel length of the usual 10-16 microns, will often have a punchthrough voltage that is lower than its two-terminal inversion voltage. In this case, one must be careful not to mistake the punchthrough voltage for the inversion voltage. When there is any doubt, the measured two-terminal inversion voltage measurement should be compared with a three-terminal inversion voltage measurement taken with a relatively low voltage (roughly 5 volts) on the drain.

The punchthrough voltage is lower than one might expect because when the gate is tied to the drain the voltage on the gate induces a charge on the gate metal that decreases the punchthrough voltage. It is worth noting also that charge in the oxide (Q_{ss}) significantly increases the punchthrough voltage. The magnitude of this effect can be qualitatively estimated from the fact that a typical Q_{ss} of 2×10^{11} cm^{-2} establishes as much charge per square centimeter as that in a depletion layer 2 microns thick in silicon having 10^{15} impurity atoms per cm^3.

We have found differences between two-terminal and three-terminal measurements of "inversion voltage" as shown in Table I. These measurements were taken at a drain current of 10 μA. The drain voltage on the three-terminal measurements was 5 volts. The resistivity of the n-type substrate was 5 ohm-cm and the channel length (between the edges of the diffusion cuts) was 14 microns.

TABLE I

Difference Between 2- and 3-Terminal V_{GST}

Device Number	2-Terminal V_{GST}	3-Terminal V_{GST}	Difference
44	18.5 V	39.0 V	20.5 V
76	21.0	38.7	17.7
38	23.6	40.0	16.4
48	24.3	34.5	10.2
75	27.4	41.6	14.2
46	29.7	41.3	11.6
50	32.0	50.5	18.5

Techniques for Determining the Cause of Degradation or Failure in an Individual Microcircuit

The utility of test structures has been discussed and demonstrated throughout each of the reports in this program. Each study and diagnosis of a degraded or failed complex microcircuit structure gives an increased appreciation of the value of test structures. Unfortunately, there are situations in which one either has no test structures to represent a group of microcircuits or in which one desires to study a particular microcircuit. For these reasons, it is important to develop useful techniques for studying and measuring individual microcircuits to establish the cause of degradation or failure.

In failure analyses of microcircuits, metal interconnections are frequently opened by scribing to isolate local portions of a circuit so that an individual device or part of a circuit can be tested by probing. This technique is destructive and fairly difficult to implement.

In a large number of cases, MOS microcircuit degradation is due to excessive leakage current. We have studied the theoretical possibilities for determining the nature of the leakage current in a given individual microcircuit without the technical difficulties or destruction involved in scribing metal interconnections to open them.

Considering the complexity of LSI circuitry, techniques are desired by which simple measurements can be taken to determine whether a defect exists anywhere within a complex structure.

It has been found that useful data can be obtained by measuring the leakage current between a variety of combinations of the terminals of the microcircuit. An automatic tester can rapidly measure the leakage current for each of a large number of combinations of the terminals. From such data, one can often establish a correlation between the circuit failure and one or more of the leakage current levels. Assuming such a correlation, we have considered a number of possibilities by which different types of leakage current might be identified.

Specifically, for each type of leakage current, we have considered each of the known possible ways in which its level might be altered and have then considered the direction of change in the current level that each of these influences would be expected to make.

The possible types of excessive leakage currents are the following:

1. Reverse current of a p-n junction
2. Through pinholes in the oxide
3. Channeling under a metal
4. Channeling not under a metal
5. Punchthrough between p-type regions

6. Parasitic bipolar transistor action between p-type regions

7. Avalanche of a p-n junction.

These leakage currents can be expected to be influenced by the following variables in the conditions of measurement.

1. Temperature

2. Ambient light level

3. History of exposure to ionizing radiation

4. Test voltage

   a. D-C voltage level or pulse height

   b. Pulse width

   c. Pulse shape

   d. Repetition rate

In the following, we discuss, in turn, the expected effects of these variables on each of the types of leakage current.

An increase in temperature is expected to:

1. Exponentially increase the current through a reverse biased p-n junction. The activation energy is 0.55 eV, i.e., the current would increase by roughly two orders of magnitude for a temperature change from 25°C to 125°C.

2. Decrease the current through a pinhole between a negatively biased metal and a p-type region due to the decrease in the carrier mobility, or increase the

current through a pinhole between negatively biased metal and the n-type substrate at the same rate as that expected at a reverse biased p-n junction because in this case the current is limited by the number of available minority carriers.

3. Decrease the channel current under a metal due to the decreasing mobility if the fast state density is negligible. On the other hand, the current will increase if fast states are present because they would be emptied as the temperature is increased.
4. Decrease the channel current in regions not covered by metal, in the same way as in regions under metal except that it is much more likely that fast states are present in regions not covered by metal and therefore one should expect an increase in current with increasing temperature.
5. Increase current due to parasitic bipolar transistor action with a current-temperature dependence similar to that for the reverse current of a diode.
6. Have either of two effects on punchthrough voltage. In the absence of fast states there might be little effect. On the other hand if fast states are present, an increase in temperature would decrease the positive

charge in the fast states over an n-type region and thereby reduce the punchthrough voltage and increase the leakage current between p-type regions.

An increase in the light level is expected to increase the reverse current of a p-n junction, and that involved in parasitic bipolar transistor action. It would not be expected to alter any of the other currents.

Ionizing radiation can be used to increase the effective positive charge density in the oxide:

1. This would increase the inversion voltage in n-type silicon and therefore decrease channel currents.
2. This would increase the punchthrough voltage and provide a means for determining whether a failure is due to punchthrough.

An increase in the test voltage level would:

1. Increase leakage current through channels or "forward biased" pinholes, roughly according to Ohm's law.
2. Increase the reverse current of a p-n junction or a pinhole. This increase could be quite small if the current saturates.
3. Increase punchthrough-induced currents.
4. Increase parasitic transistor currents because of the increase in beta with increasing collector voltage.

Variations in the pulse width, pulse shape or repetition rate have not been used to obtain useful information for separating leakage currents. We include them here because their consideration might lead to measurement techniques by which leakage currents might be characterized.

Physical Effect of a Second-Layer Insulator on the Oxide-Silicon Interface Properties

In each of our Scientific Reports, we have mentioned that the deposition of a second-layer insulator might alter the electrical properties of the oxide-silicon interface because of the temperature involved, because of contamination or because of electrochemical or work function effects. The determination of the significance of the effect of specific processes and materials on these electrical properties has been a major subject of each of our reports. During this reporting interval, we have considered an additional possible effect of a second-layer insulator.

Consider the structural geometry shown in Figure 6. The capacitance between the metal electrode and the silicon substrate is increased if the material between planes AB and BC is changed from air or nitrogen to a material with a higher dielectric constant, such as vapor plated SiO_2 or phosphosilicate. For a

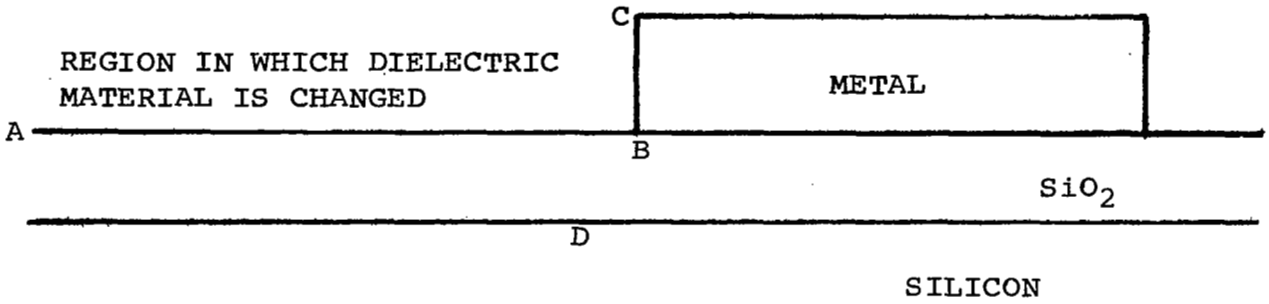


Figure 6. Diagram for model for effect of change in second-layer dielectric.

given voltage on the metal, such an increase in capacitance would increase the surface potential and the charge density per unit area, in the silicon near the region labeled D. These changes in surface potential and area charge density can alter the electrical characteristics of a microcircuit.

EXPERIMENTAL STUDIES OF THE FUNDAMENTAL PROPERTIES OF THE MIS SYSTEM

An Evaluation of Samples of Vapor Plated Aluminum Oxide and Silicon Nitride

In Scientific Report No. 3, we reported results of the evaluation of a wide variety of types of materials that have been considered for use as insulator layers over the metal layer in microcircuits. We have also discussed in previous reports the compatibility requirements of this type of a layer with the materials and processes in present use in microcircuits.

These findings have indicated that the most promising material for a second layer insulator over aluminum is vapor plated phosphosilicate. Aluminum oxide and silicon nitride are frequently mentioned as promising materials for this purpose. In Scientific Report No. 3 we reported that aluminum oxide vapor plated at 400°C is very unstable electrically. Aluminum oxide and silicon nitride can be deposited with stable properties at temperatures of 800°C or higher but there is no process for depositing good quality films of these materials at temperatures that would not melt the aluminum metal or cause the aluminum-silicon eutectic (577°C) to form if either of these materials is used over the aluminum metal in the microcircuit structure.

On the other hand, there is an increasing trend in the industry to use aluminum oxide or silicon nitride over a thin layer of thermally grown SiO_2 and under the metal either to decrease the threshold voltage or to provide an insulator layer having a higher breakdown voltage. Aluminum oxide apparently yields a low inversion voltage because of an "insulator-insulator contact potential;"[9,10] while silicon nitride yields a low inversion voltage because of its high dielectric constant[11] and its ability to be produced in quite thin layers that are relatively resistant to shorting through the insulator layer.[11,12] With either material it is necessary to have a thin layer (approximately 200 Å) of thermally grown SiO_2 on the silicon so as to have low fast state density at the insulator-silicon interface.

Both silicon nitride and aluminum oxide have been used in MOS arrays. Silicon nitride has been used in bipolar arrays. In each of these cases these insulators are under the metal. Both are reported to be alkali barriers.[13,14]

We have prepared samples of these materials for evaluation for use under the metal layer. The conditions of deposition for these samples were the following which are representative of the processes used by the industry.

Silicon Nitride Deposition Conditions:

Substrate temperature: 1000°C

H_2: 40 liters/minute

SiH_4: 0.003 liter/minute

NH_3: 0.1 liter/minute

Aluminum Oxide Deposition Conditions:

Substrate temperature: 1000°C

H_2: 20 liters/minute

CO_2: 3 liters/minute

$AlCl_3$ (anhydrous): sublimated in a flow of 2 liters/minute of H_2 at 150°C.

The measured charge densities in MOS capacitors containing these materials are summarized in Table II. The data in Table II indicate the following.

1. The effective immobile charge density is lower in samples having aluminum oxide than it is in the samples having silicon nitride. Nigh et al.[9,10] report that the insulator-insulator contact potential for aluminum oxide and silicon dioxide is between 1.2 and 2.0 volts. Assuming this contact potential to be 1.5 volts, we calculate Q_{ss} levels of 2.1×10^{11} on the samples containing aluminum oxide instead of the $1.3\text{-}1.7 \times 10^{11}$ given in Table II. On the other hand, the effective

TABLE II

CHARGE DENSITIES IN Al_2O_3 AND Si_3N_4

	10^{11} CHARGES/cm^2			
	IMMOBILE	MOBILE (300°C)	MOBILE (27°C)	FAST STATE DENSITY
2000 Å TG SiO_2, 2000 Å VP Al_2O_3, 6000 Å VP SiO_2	1.7	>8.8	---	<0.1
2000 Å TG SiO_2, 2000 Å VP Al_2O_3	1.3	2.8	0.1	<0.1
2000 Å TG SiO_2, 2000 Å VP Si_3N_4, 6000 Å VP SiO_2	9.2	>8.5	---	1.3
2000 Å TG SiO_2, 2000 Å VP Si_3N_4 DEPOSITED AT 1000°C	6.8	0.1	<0.1	1.3
200 Å TG SiO_2, 1050 Å VP Si_3N_4 DEPOSITED AT 900°C	7.0	3.5 (T)	0.5	7.0
2000 Å TG SiO_2 (CONTROLS FOR Al)	1.4	<0.1	<0.1	<0.1

ABBREVIATIONS

TG Thermally Grown
VP Vapor Plated
(T) Trapping

immmobile charge in our samples containing aluminum oxide is no lower than that in the sample having only thermally grown SiO_2. It may be that our samples have no significant insulator-insulator contact potential.

2. The deposition of silicon nitride has increased the effective immobile charge density from 1.4×10^{11} to $6.8\text{-}9.2 \times 10^{11}$ cm^{-2}. This is similar to the results reported very recently by Hillery.[15]

3. Both aluminum oxide and silicon nitride, deposited under the conditions described above, are electrically much more stable than are any other kind of insulator layers that we have studied other than thermally grown SiO_2. Unfortunately, the 1000°C deposition temperature prevents the use of these materials over metallic layers.

4. Vapor plated SiO_2 over stable insulator layers induces a high level of instability because of the high mobile ion content in vapor plated SiO_2.

5. Silicon nitride is a barrier to the species that are involved in the annihilation of fast states. This was previously reported by Deal et al.[3] The densities of fast states shown in Table II were measured by the technique of Brown and Gray.[16]

Accelerated Aging Test Data on MOS Transistors

In an earlier part of this program, we took bipolar microcircuit wafers from a production line and delineated the metal into a special pattern to make it possible to test discrete transistors in the chip. We divided these wafers into halves and half of each wafer was given a deposition of chemically vapor plated SiO_2. The transistors from both halves of the wafers were then tested before and after a 5-day bake at 175°C during which a reverse bias of 6 volts was applied. The results were presented in the first Scientific Report.

A similar test of the effect of deposited dielectric has been conducted with MOS structures as follows. Two wafers were taken from a lot of production MOS microcircuit wafers. The chips from these wafers contain discrete p-channel enhancement mode MOS transistors. The substrate is 5 ohm-cm, <111> oriented silicon. They were fabricated by an alkali free process with no phosphorus diffusion or phosphosilicate deposition. The wafers were divided into halves and half of each wafer was given a deposition of one micron of vapor plated phosphosilicate. The deposition and control techniques for this phosphosilicate were described on pages 7-12 of Scientific Report No. 2.
The ability of phosphosilicate to getter sodium is reported in

Reference 6. Each chip has two discrete MOS transistors. One of these transistors has under its gate an oxide of the type (preparation and thickness) that is under the gate of the transistors in the circuit. The other transistor has under its gate an oxide of the type found in the field of the circuit. Contact cuts were made through the vapor plated layer and the transistors were then scribed and header and wire bonded into TO-5 packages.

These transistors were electrically tested before and after 548 hours of accelerated aging. The accelerated aging was done at 125°C with -20 volts applied to the gate on half of the devices, and to the drain on the other half. In each case the other three terminals were tied together. The results discussed below, were similar for the two conditions of applied aging bias.

The following parameters were measured on each transistor:

I_1 The leakage current, at -20 V, of the drain relative to the source, gate and substrate.

I_2 The leakage current, at -20 V, of the source relative to the drain, gate and substrate.

V_1 The breakdown voltage, at 10 μA, of the drain relative to the source, gate and substrate.

V_2 The breakdown voltage, at 10 μA, of the source relative to the drain, gate and substrate.

V_3 The breakdown voltage, at 10 μA, of the source, gate and drain relative to the substrate.

V_{T1}, V_{T2} The threshold voltage, measured with the gate tied to the drain and the source tied to the substrate, at both 10 μA (V_{T1}) and 100 μA (V_{T2}).

As expected, because of the symmetry of MOS transistors, the measured values of I_1 and I_2, and of V_1 and V_2, were very similar. Also, the results from each of the two wafers were similar. Further, the threshold voltage data at 100 μA lead one to the same conclusions as those at 10 μA. Therefore, data from only one of the wafers are shown in Figures 7 to 14. Measurements I_2, V_2 and V_{T2} are not shown because of their similarity to I_1, V_1 and V_{T1}, respectively.

The data in Figures 7 to 14 can be summarized as follows:

1. The phosphosilicate and its deposition process (400°C for less than four minutes) does not degrade the leakage current of the devices at any point in the test.
2. The leakage current did not increase significantly during the accelerated life test.
3. The devices having the phosphosilicate exhibited breakdown voltages (of all types) that were more tightly grouped, that had higher levels on the average and

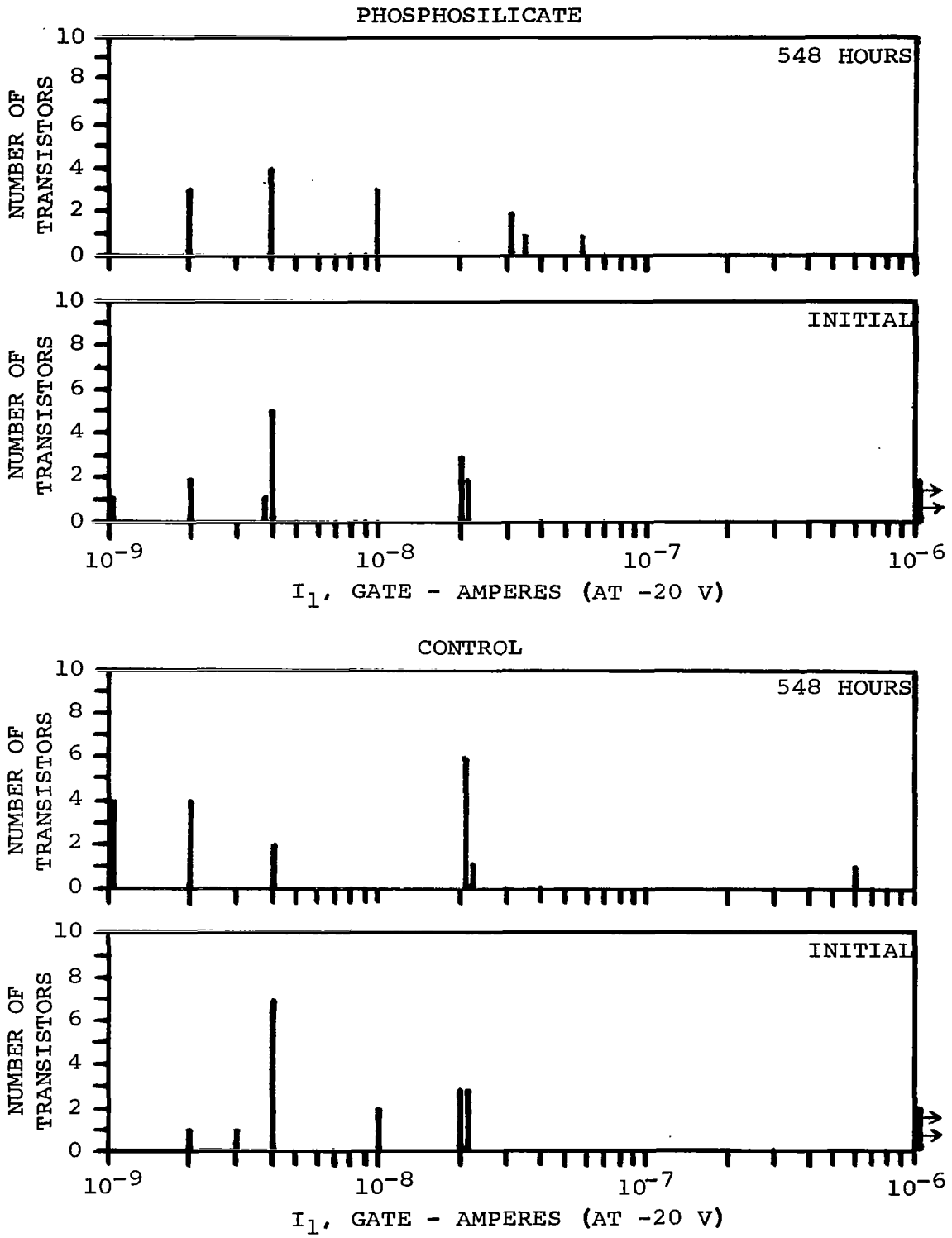


Figure 7. Results of life test of MOS transistors -- I_1, gate.

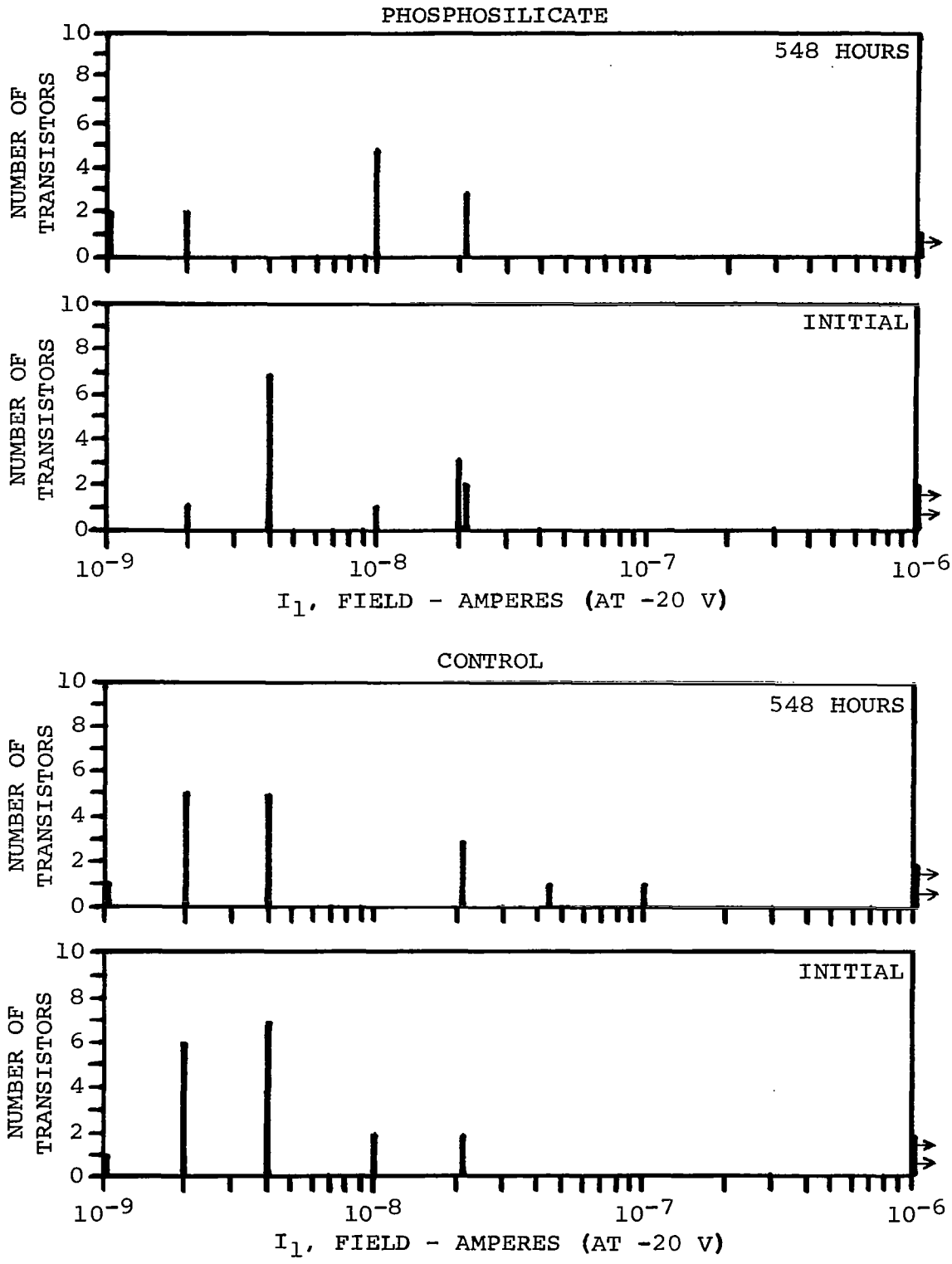


Figure 8. Results of life test of MOS transistors -- I_1, field.

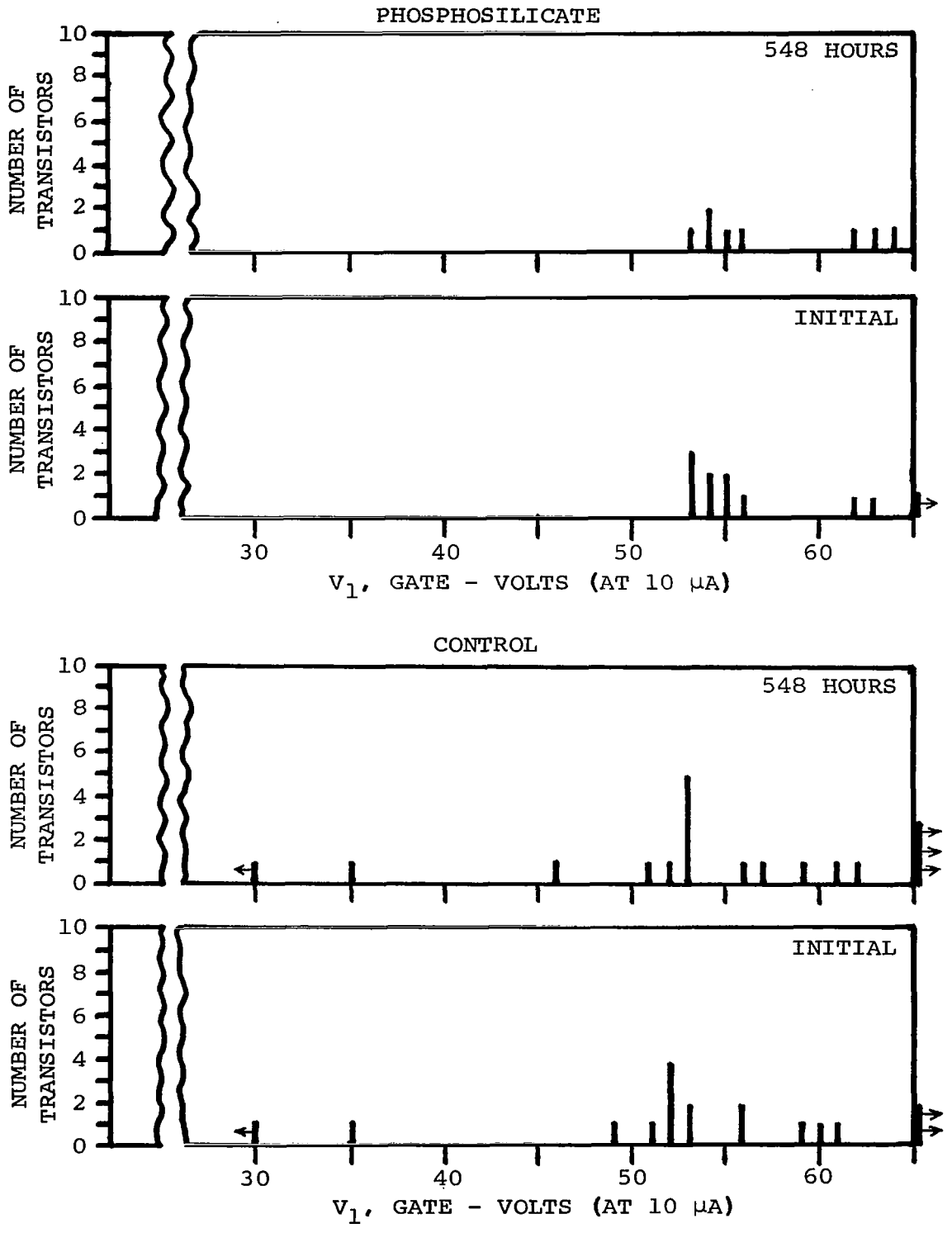


Figure 9. Results of life test of MOS transistors -- V_1, gate.

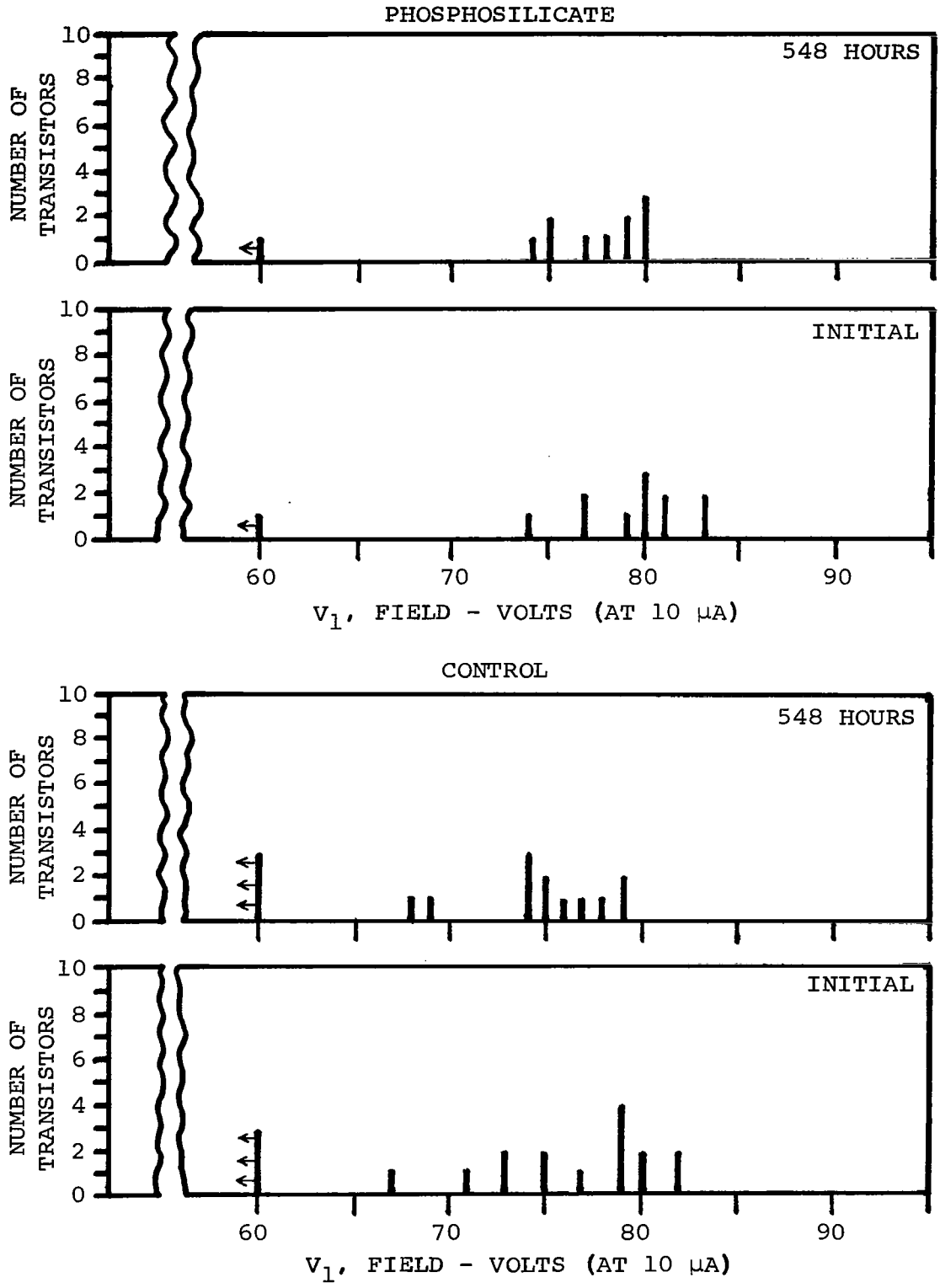


Figure 10. Results of life test of MOS transistors -- V_1, field.

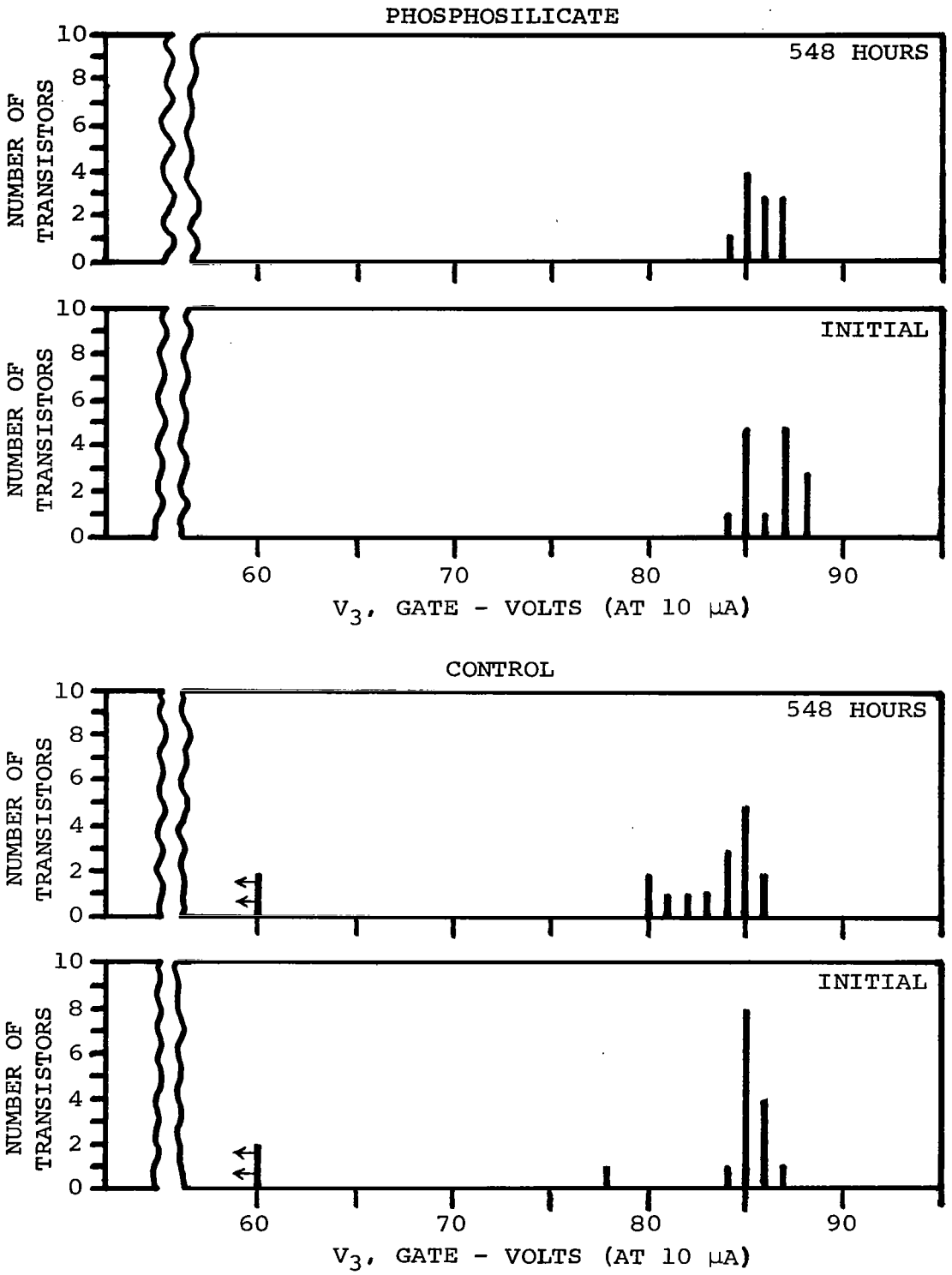


Figure 11. Results of life test of MOS transistors -- V_3, gate.

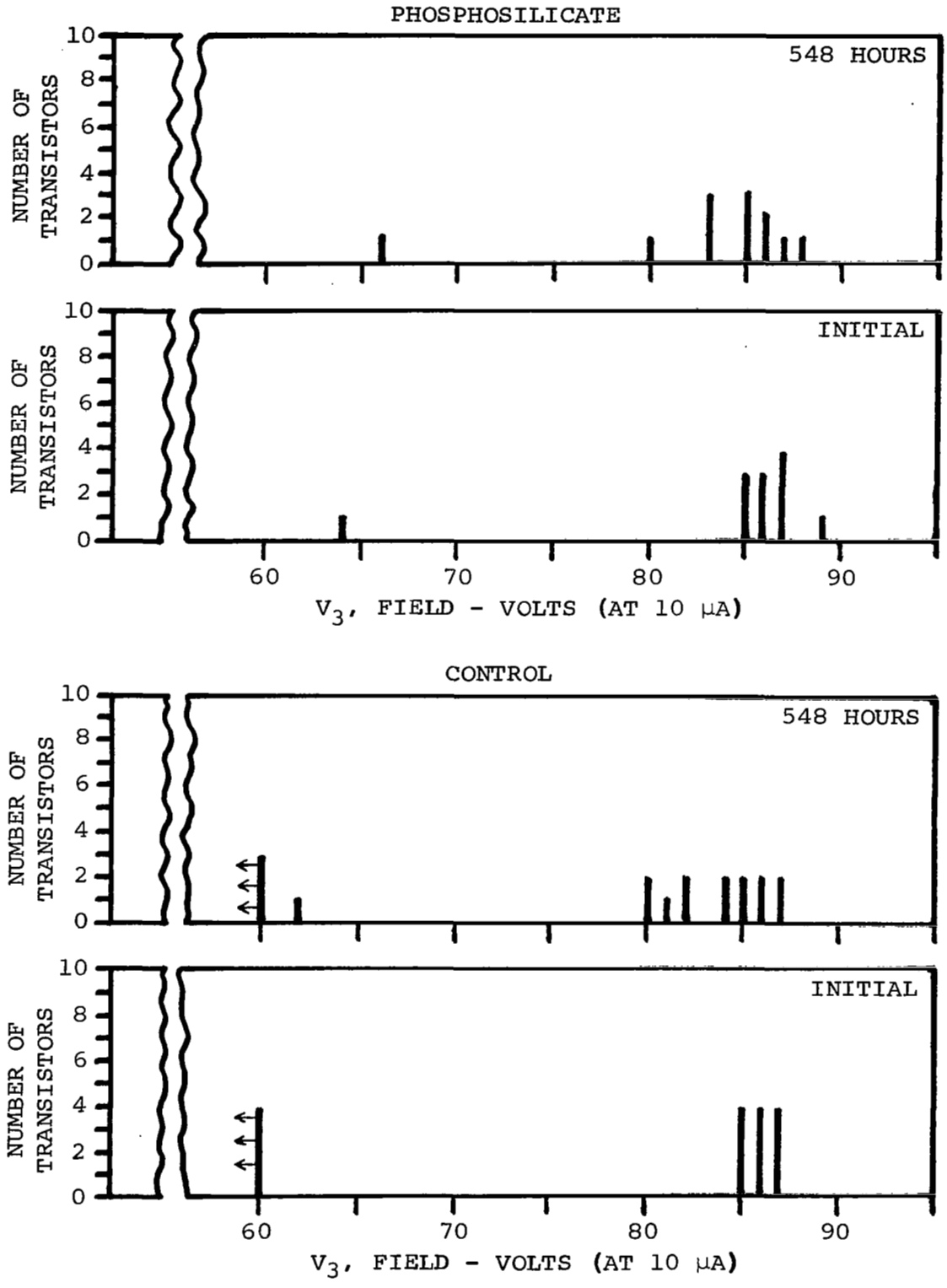


Figure 12. Results of life test of MOS transistors -- V_3, field.

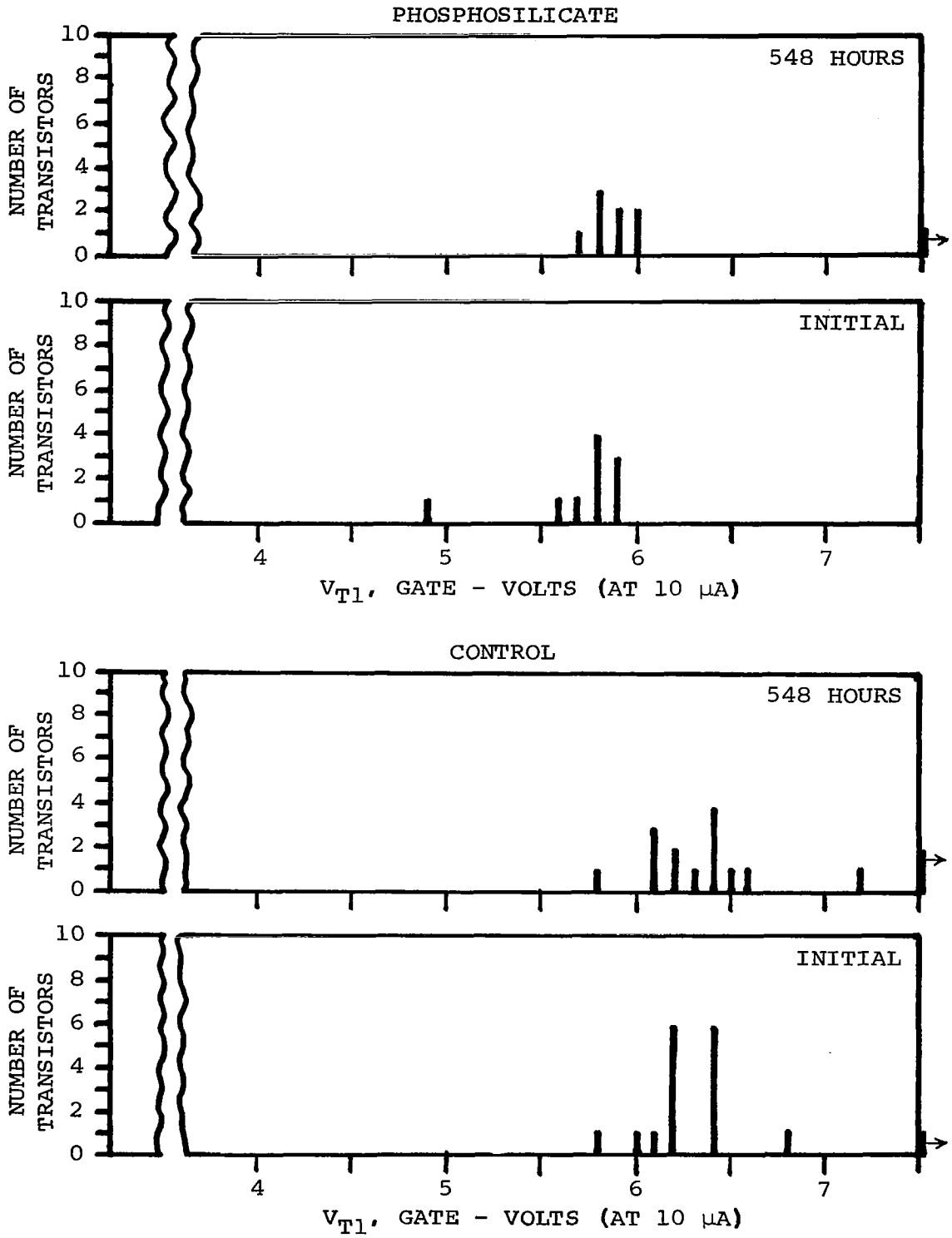


Figure 13. Results of life test of MOS transistors -- V_{T1}, gate.

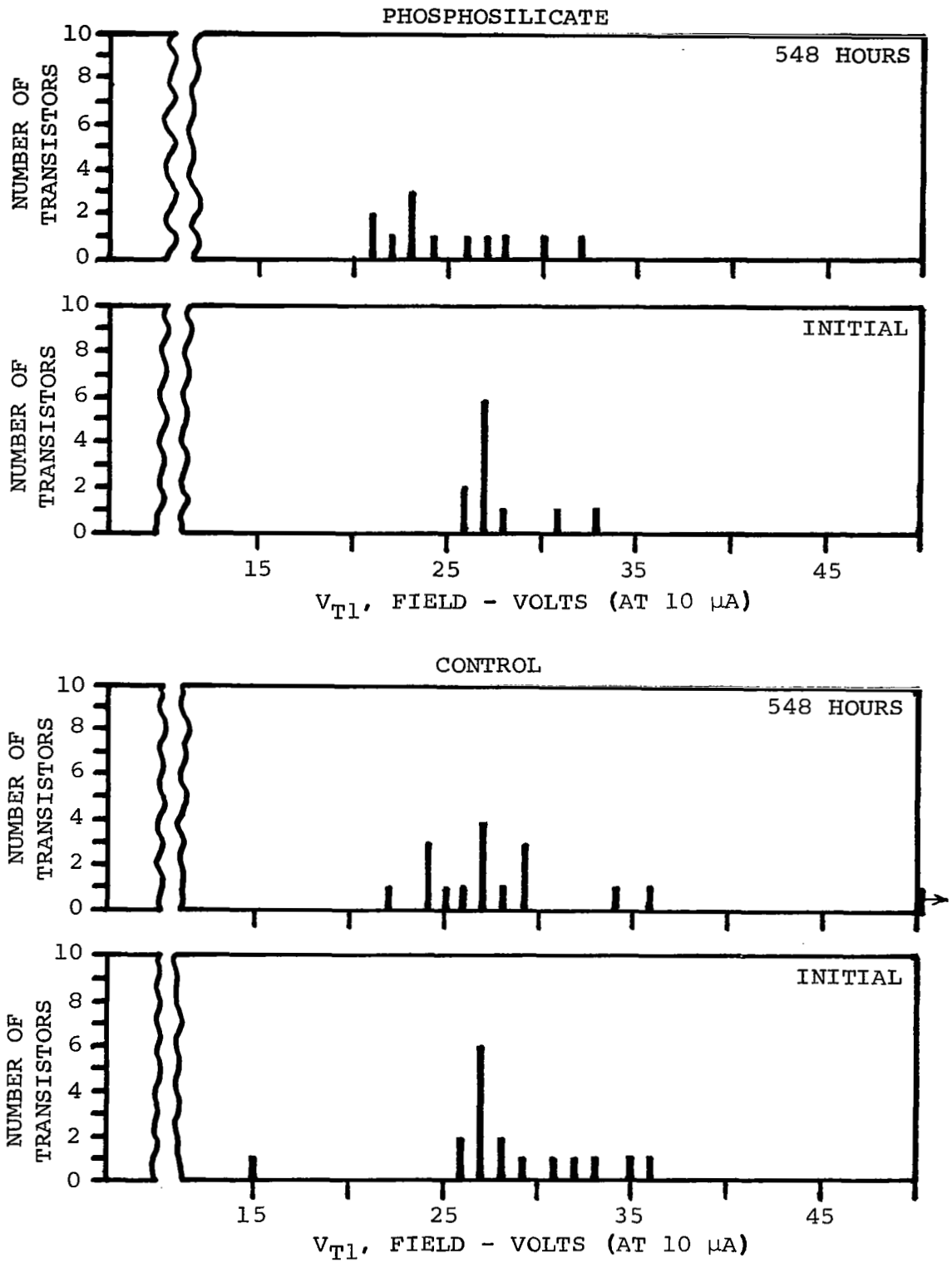


Figure 14. Results of life test of MOS transistors -- V_{T1}, field.

that held up better on life than those of the control devices.

4. Gate oxide transistors with phosphosilicate have lower threshold voltages (by about 0.5 V) than those without phosphosilicate.

5. The threshold voltage on all of the transistors with gate oxide was stable through the accelerated life test.

6. The threshold voltage on the transistors with the field oxide was decreased (by up to 5 V) during the life test.

7. There was no significant difference in the threshold voltage of transistors with field oxide between devices with and those without phosphosilicate.

These data show that sensitive devices under accelerated stress conditions show no detrimental effects due to the presence of a layer of vapor plated phosphosilicate or the process used to apply it. We conclude that the deposition of vapor plated phosphosilicate at 400°C is therefore suitable for use with LSI circuits.

Annealing of Fast States

Importance of Fast States. - Fast states are an important influence on microcircuit performance and reliability because they strongly

influence the surface potential of the silicon and its dependence on applied voltage and temperature. For this reason we have reported in previous reports (e.g., Table I of Scientific Report No. 3) on the influence of various processing variables on the measured fast state density.

The importance of the fast state density can be appreciated from the results of the following experiment involving transistor devices having the geometry described in the first Scientific Report (pages 46-47). The oxide thickness under the gate is 1700 Å. The devices were measured by probing on the metallized wafer before they were alloyed. They were then subjected to a heat treatment similar to that involved in the header bonding operation and then they were again measured on the wafer under probes. The data in Figure 15 demonstrate the large change in both the threshold voltage and the transconductance due to the annealing out of fast states during the header bonding operation. We also measured the fast state density in capacitors on the same wafer by the technique described by Deal et al[3] and found that roughly 18×10^{11} fast states/cm^2 were annealed out during the heat treatment.

Anneal of Fast States in Large Area Capacitors. - In Scientific Report No. 3, we showed that the fast state density as measured by Brown and Gray[16] was not reduced to negligible

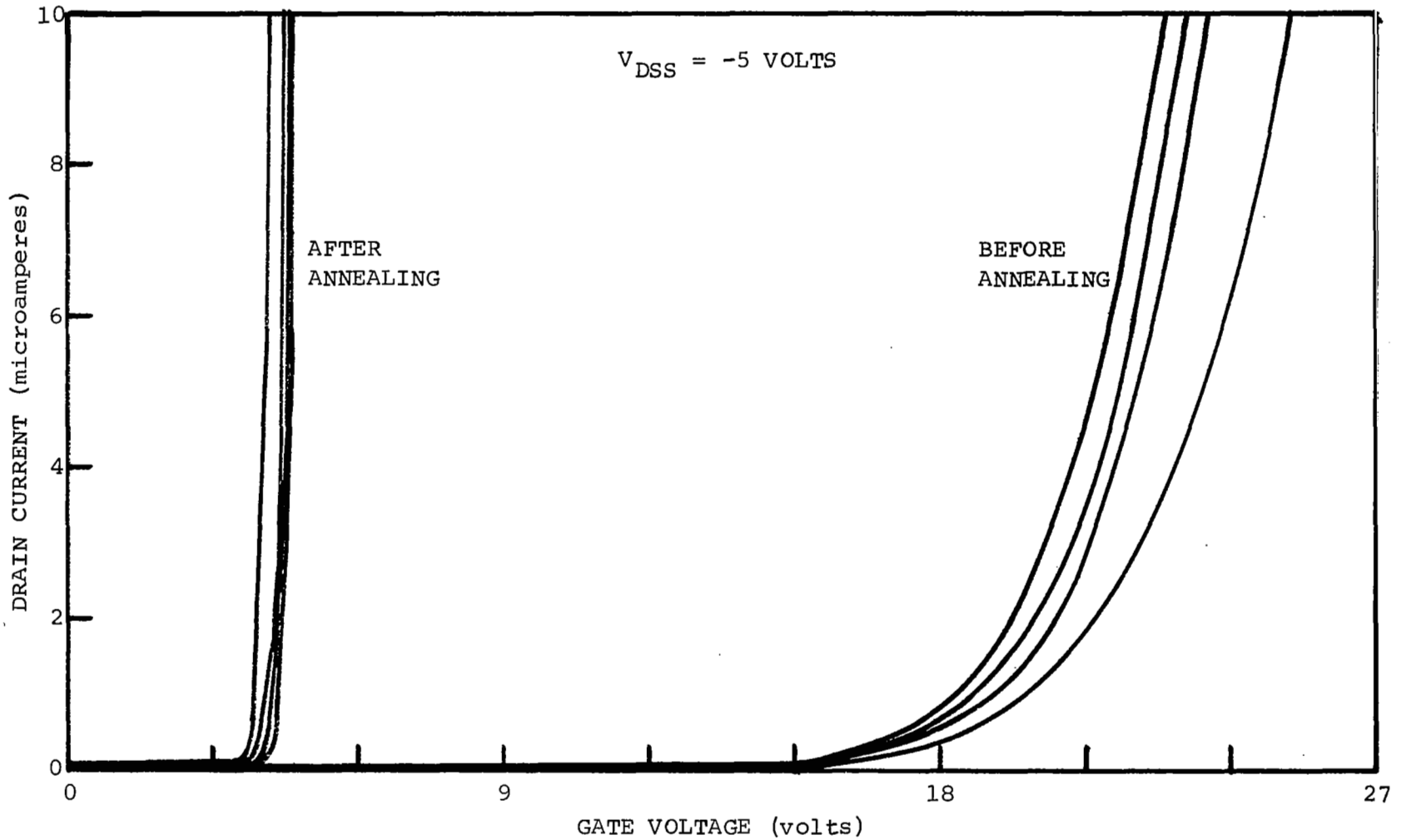


Figure 15. Effect of fast state annealing on the characteristics of MOS transistors.

levels by a hydrogen anneal at 350°C; that is, 7×10^{11} fast states/cm^2 remain after an anneal at 350°C for 120 minutes. In subsequent work, we found that a hydrogen anneal at 500°C for 30 minutes does anneal this fast state density to less than 1×10^{11} cm^{-2}. This would indicate that the lowest temperature for the complete annealing of fast states in hydrogen is between 350 and 500°C. Our results are consistent with the findings of other investigators as given below:

1. Balk[17] discussed experimental results involving annealing at 320°C in hydrogen. He found that the annealing effect saturated in 2-1/2 hours. His data show that 3.5×10^{11} fast states/cm^2 were still present after the anneal.
2. Kooi[5] annealed in hydrogen for 30 minutes at 450°C. His data appears to show the disappearance of fast states to an undetectable number.
3. Brown and Gray[16] show that an anneal at 800°C for one hour in hydrogen decreases the fast state density to less than 10^{10} cm^{-2}.
4. Gray and Brown[18] report that a one-hour anneal in hydrogen at 400°C reduced the fast state density to about 2×10^{10} cm^{-2}.

We have prepared silicon nitride layers by vapor deposition at 900°C. The nitride was 1050 Å thick over a 200 Å layer of thermally

grown SiO_2. We found that our usual alloying treatment, that would have annealed the fast state density (with aluminum electrodes) to a negligible level (less than 1×10^{11} cm^{-2}), left from 4.7 to 6.9×10^{11} fast states per cm^2 (measured by the technique of Brown and Gray[16]). Similar results have been previously reported by Deal et al.[3]

Also, we have made MOS capacitors with nickel instead of aluminum and the same alloying cycle that essentially anneals all of the fast states when the metal is aluminum leaves roughly 40×10^{11} fast states per cm^2 as measured by the Brown and Gray[16] technique. This also has been reported previously by Deal et al.[3]

All of these data demonstrate the importance of the evaluation of fast state densities in any investigation of the possible effects of second-layer insulator materials or processes on the performance and reliability of microcircuits.

Table III is an updated summary of our most important results in experiments in the annealing of fast states from oxides in large area capacitors.

TABLE III

FAST STATE DENSITIES (GRAY AND BROWN), MEASURED WITH GOLD BALL PROBE

	10^{11} FAST STATES/cm^2
OXIDE GROWN THERMALLY IN DRY AMBIENT	24-40
H_2 BAKE, 350°C, 30 MIN.	7
H_2 BAKE, 350°C, 120 MIN.	7
H_2 BAKE, 500°C, 30 MIN.	<1
H_2O BOIL, 5 MIN.	30
H_2O BOIL, 60 MIN.	10
METALLIZED (Al)	13
METALLIZED (Al), BAKED (500°C, 12 MIN.)	<1
METALLIZED (Ni), BAKED (500°C, 12 MIN.)	40
METALLIZED (Al), NOT BAKED, HEADER AND WIRE BONDED ON TO-5	<1
METALLIZED (Al), METAL REMOVED, BAKED (500°C, 12 MIN.)	6-25
BAKE AT 300°C, 45 MIN., 10^{-6} TORR, SUBSEQUENTLY METALLIZED AND BAKED (500°C, 12 MIN.)	3
1000 Å OF SILICON NITRIDE DEPOSITED, METALLIZED (Al), BAKED (500°C, 12 MIN.)	5-7

Annealing of Fast States Near the Edge of a Metallized Region.- One of the important findings made to date with the new set of test structures has been the observation that fast states do not anneal out under narrow metal lines as they do under wide metal lines.

The specific test structure involved in this discovery is shown in Figure 16. It shows four separate p-regions, with their contact lands, and two lands connected to gate metal. The structural arrangement permits measurements to be made on different parts of this structure as four discrete transistors. The structure shown in Figure 16 includes a transistor with gate digits 0.2 mil wide, and three other possibilities for measuring transistors with wider gate metal. The oxide under each of the gates is field oxide.

Inversion voltages were measured on these structures yielding the results shown in Table IV. From these data one can calculate that after the alloying operation approximately 10^{12} fast states/cm^2 were present beneath 0.2 mil wide aluminum lines.

We also found that the hydrogen anneal decreased the inversion voltage from 35 to 30 volts under devices with wider gates. This indicates but does not prove (the possibility that this decrease was due to the temperature and time alone cannot be ruled out) that the hydrogen permeates the aluminum.

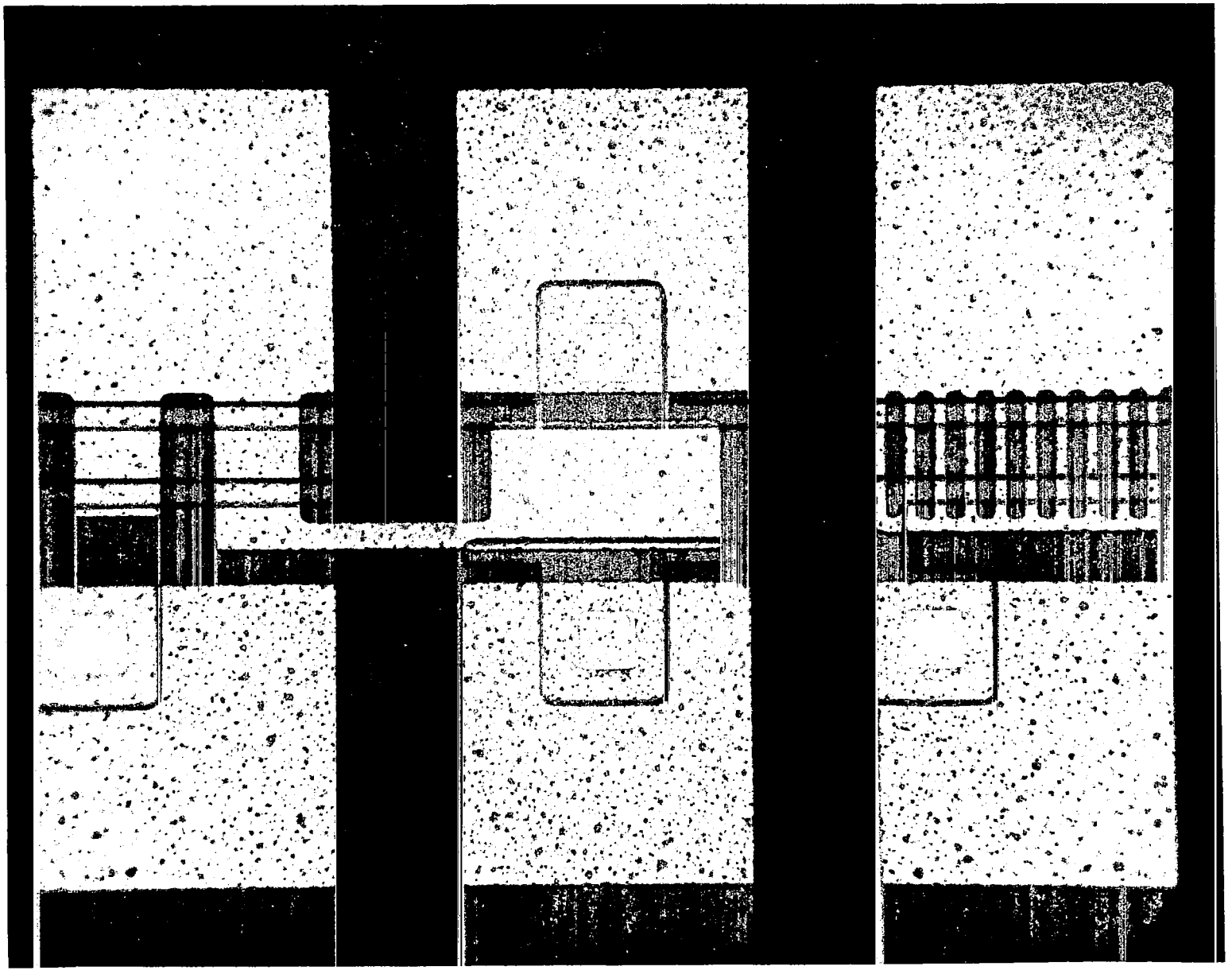


Figure 16. Surface ion and channel length test structures.

TABLE IV

INVERSION VOLTAGE UNDER TWO ALUMINUM LINE WIDTHS AND DIFFERENT TREATMENTS

LINE WIDTH (MILS)	TREATMENT	INVERSION VOLTAGE (VOLTS)
0.2	AFTER ALLOYING AT 500°C, 12 MIN.	70 to 100
	AFTER BOILING IN DI WATER FOR 1 HOUR AND REALLOYING AT 500°C, 12 MIN.	70 to 100
	AFTER ALLOYING AT 500°C, 1 HOUR	70 to 100
	AFTER H_2 ANNEAL AT 345°C, 30 MIN.	35
1.5	AFTER ALLOYING AT 500°C, 12 MIN.	35

Influence of P-N Junctions on the Mobile Charge Density in MOS Transistors

In Scientific Report No. 3 (pages 84, 85 and 91) we showed that the presence of a p-n junction influences the density of mobile charge in the oxide near the junction. We interpreted this as being due to the fringing field in the oxide due to the p-n junction. That is, the same field that keeps holes in the p-region and electrons in the n-region drifts positive sodium ions to the regions over the p-type source and drain and away from the n-type channel. This interpretation provides an explanation for why the mobile charge density found in p-channel MOS transistors with channels 1.0 mil long is higher than in those having a channel 0.4 mil long. The data in Scientific Report No. 3 taken on samples with boron diffusion into phosphorus doped substrates are shown in Table V. Also shown are data for MOS capacitors that we interpreted as evidence that oxide surfaces getter sodium ions from regions covered by metal to regions not covered by metal.

To test our interpretation, we conducted a similar experiment on samples that contain a phosphorus diffusion in a substrate of boron-doped silicon. The results of this experiment are also shown in Table V. The transistor and capacitor structures of these

TABLE V

MOBILE (300°C, ±12 V, 12 MIN.)
CHARGE DENSITY IN DIFFERENT STRUCTURES

	P-ON-*N*	*N*-ON-*P*
MOS CAPACITOR, 30 x 30 MILS^2	7×10^{11}	0.4×10^{11}
MOS CAPACITOR, HIGH PERIMETER-TO-AREA RATIO	2.9	3.0
MOS TRANSISTOR, 1 MIL CHANNEL LENGTH	1.8	0.7
MOS TRANSISTOR, 0.4 MIL CHANNEL LENGTH	0.4	2.1

samples are essentially the same as those involved in the earlier work. In addition to the differences in diffusant and substrate dopants there were other processing differences. The phosphorus was deposited as vapor plated phosphosilicate at 400°C over the thermally grown oxide diffusion mask and then diffused at 1150°C for 15 minutes. All of the oxide was then removed, so that the phosphosilicate would not immobilize the sodium ions. An oxide layer (2200 Å) was then grown so that the final oxide would contain very little phosphorus. (Phosphorus would immobilize the mobile charge).

All of the transistor data shown in Table V support the model that the sodium drifts from the oxide over n-regions to that over the p-regions.

On the other hand, the charge densities in the capacitors do not support another model (discussed in Scientific Report No. 3) that the surface of the oxide getters the sodium ions from regions covered by metal to regions not covered by metal. It may be that the relative amount of mobile charge in the 30 x 30 mil^2 capacitor and in the capacitors with the narrow metal lines (high P/A) is more dependent on the relative amount of mobile charge beneath the metal and on the top surface of the insulator after the metal has been delineated than on a possible gettering phenomenon.

Surface Recombination Velocity

Surface recombination velocity is an important determinant of the leakage current in either MOS or bipolar circuits and of the current gain of transistors in bipolar circuits. For this reason, it is important to establish whether the processes used in the fabrication of complex LSI circuits degrade the surface recombination velocity.

We have used the technique of Fitzgerald and Grove[2] to measure the surface recombination velocity in samples made of various materials and by various processes used to build LSI circuits. We measured the surface recombination velocity of samples with second-layer oxides under the aluminum metal. The results of these measurements are shown in Figure 17. These data show that the surface recombination velocity is greatly increased by the deposition of vapor plated SiO_2 or phosphosilicate. We also measured the fast state densities in MOS capacitors on these same chips by the technique of Brown and Gray[16] and obtained the results given in the first column of Table VI. These results are consistent with the data in Figure 17.

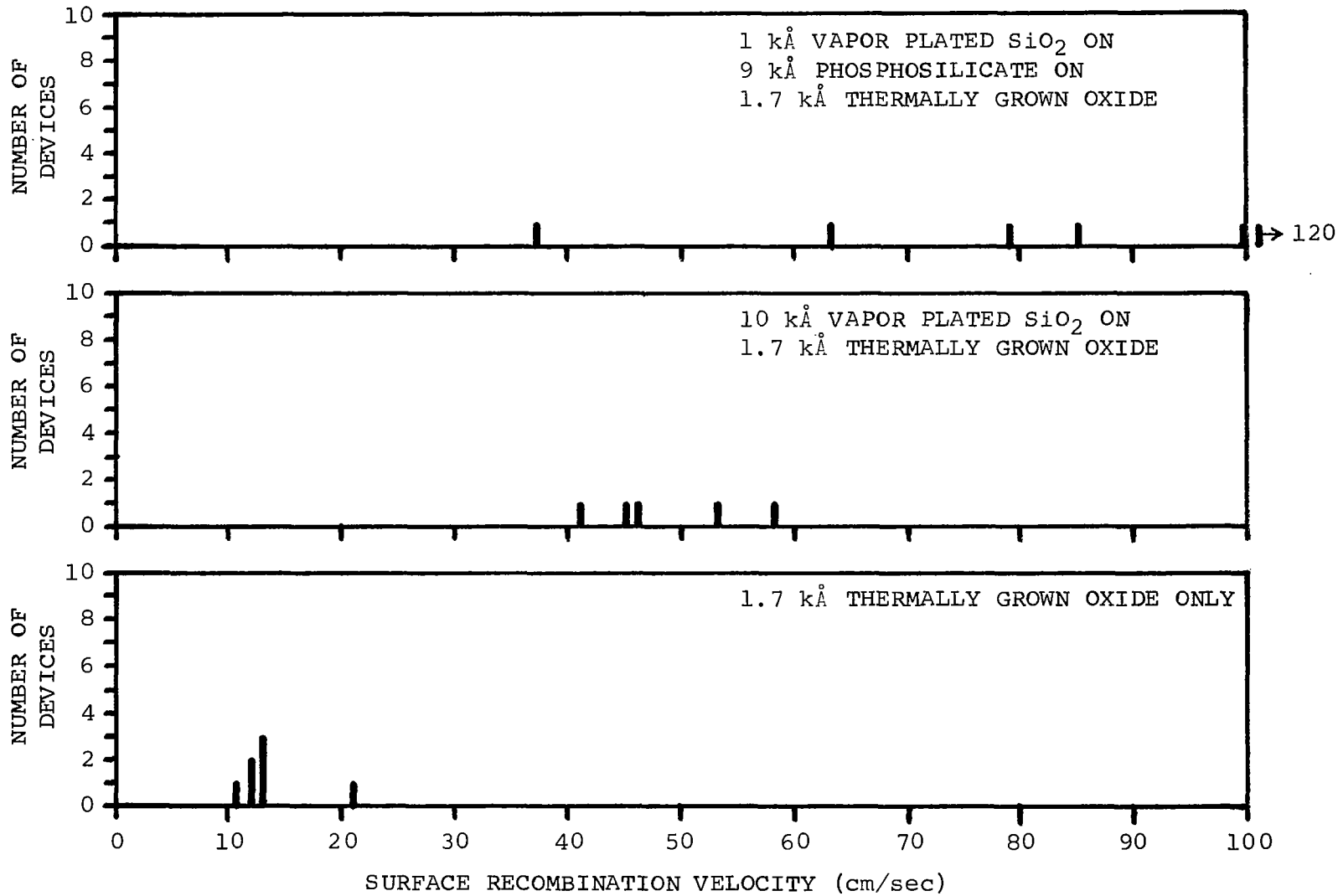


Figure 17. Effect of vapor plated oxides, under the metal, on the surface recombination velocity.

TABLE VI

FAST STATES AND Q_{ss} IN MULTILEVEL INSULATORS

	Fast States	Q_{ss}
Thermally grown SiO_2 only	0.3×10^{11} cm^{-2}	3.9×10^{11} cm^{-2}
Vapor plated SiO_2 over thermally grown SiO_2	1.0	7.9
Vapor plated phosphosilicate over thermally grown SiO_2	2.7	9.6

On pages 73 and 74 of Scientific Report No. 3, we presented data that show that other samples having a layer of vapor plated phosphosilicate have lower leakage currents than samples without the vapor plated layer. The lower leakage current level would appear to be inconsistent with the higher surface recombination velocity. There is not necessarily an inconsistency. Since the surface recombination velocity is a function of the surface potential, as shown in Reference 19, a sample having a high maximum surface recombination velocity could have a low leakage current because of a surface potential that is far from intrinsic. (The surface recombination velocity as measured by Fitzgerald and Grove[2], is the maximum level - that at an intrinsic surface potential. The samples with the lower leakage current were found to have higher values of Q_{ss}, as shown in the second column in Table VI.

We conclude that while the deposition of phosphosilicate increases the maximum surface recombination velocity, it decreases the effective surface recombination velocity and the leakage current because of an increase in the surface potential.

Experiments in which a layer of phosphosilicate was vapor plated over the metal show (Figure 18) that the degradation in the measured surface recombination velocity is much smaller.

Goetzberger et al.[20] have postulated that fast states may be due to charges in the oxide. If their model is valid one might expect that the fast state density, and therefore the surface recombination velocity, could be altered in a given sample by drifting the mobile charge toward or away from the silicon. To test this hypothesis, we compared the measured surface recombination velocity before and after mobile charge was drifted by an applied field at an elevated temperature in several samples known to contain mobile cnarge in the oxide. The mobile charge in these samples was as high as 25×10^{11} cm^{-2}. The data in Figure 19 show a small increase in the surface recombination velocity due to the drift of mobile charges toward the silicon. Previous efforts to influence the density of Brown and Gray states caused by drifting mobile charge yielded negative results.

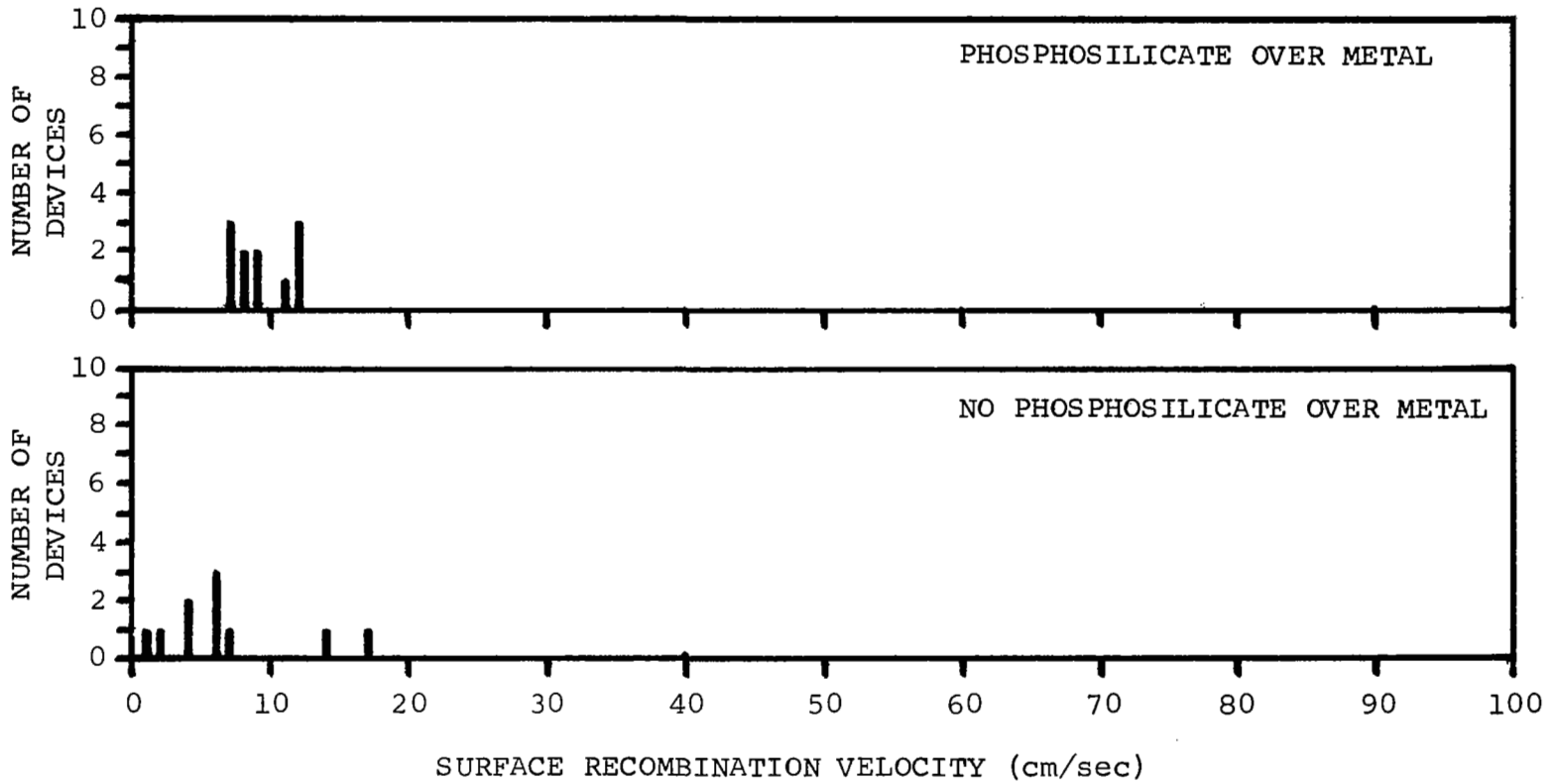


Figure 18. Effect of vapor plated oxides, over the metal, on the surface recombination velocity.

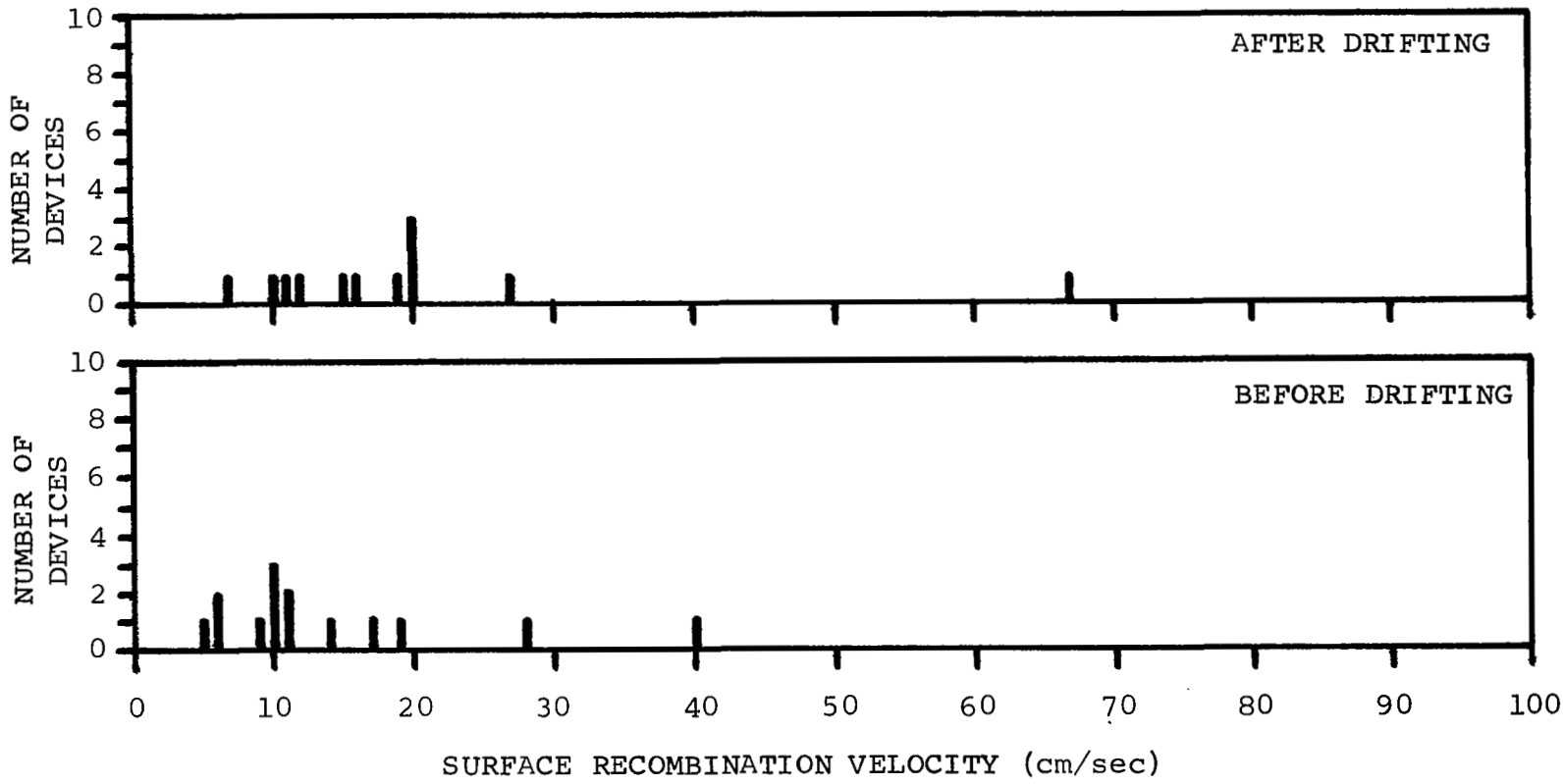


Figure 19. Effect of drifting mobile charge toward the silicon on the surface recombination velocity.

Comparison of Inversion Voltage in Regions Covered by Metal and in Regions not Covered by Metal

An important determinant of microcircuit performance and reliability is the relative inversion voltage in various parts of the microcircuit structure -- under the transistor gates, under the metal interconnections and in regions not covered by metal.

The inversion voltage under the transistor gates establishes the turn-on voltage of the transistors - an important determinant of the performance of the circuit. If the inversion voltage under metal interconnections is lower than the operating voltage thereon, inversion will occur and the necessary isolation between adjacent p-type regions will be degraded, and the performance and reliability of the circuit will be impaired. If the inversion voltage is too low in regions not covered by metal, surface ions might build up a sufficient charge on the surface to invert these regions and similarly degrade the circuit performance or reliability.

If the inversion voltage in regions not covered by metal is much higher than in regions covered by metal, there is neither a performance nor a reliability problem.

If the inversion voltage is lower in regions not covered by metal than in regions covered by metal there is a very definite reliability problem. In this case, the circuit might work well

initially but when the applied voltage has been on the circuit for a period of time, surface ion migration on the insulator surface could create channels in the region not covered by metal and cause the circuit to fail. It is unlikely that the inversion voltage would be lower in regions not covered by metal than in regions covered by metal when that metal (e.g., aluminum) enhances the annealing of surface states. On the other hand, if the metal is aluminum and it is alloyed before the delineation, or if metals are being used that do not anneal fast states, the inversion voltage in regions not covered by metal can be equal to those in regions covered by metal. If the inversion voltage in these two types of regions are equal, a slight reduction in the inversion voltage in regions not covered by metal, perhaps due to a difference in the moisture in the oxide in the two types of regions, could create yield or reliability problems.

In the section concerning the annealing of fast states (pages 50 - 54), we give data showing that fast states are not annealed out in regions not covered by aluminum as they are in regions covered by aluminum. These data raise the following questions:

1. How does one measure the inversion voltage in regions not covered by metal?
2. Quantitatively, how does the inversion voltage under regions not covered by metal compare with the inversion voltage in those regions that are covered by metal?

Concerning question 1, there are two ways in which we have measured the inversion voltage in regions not covered by metal. If an appropriate structure exists, one can apply a conductive paste on the oxide, between two p-regions, that serves as a gate electrode for measuring the inversion voltage. (Paste applied at room temperature is unlikely to alter either the charge or the fast state density in the oxide. Also, if there is a work function difference between the paste and the silicon, the effect of this difference is negligible when the oxide is thick.)

For thin oxides, the use of conductive paste does not always yield a reliable measurement of the threshold voltages. We believe this to be due to a less than adequate intimacy of the contact between the conductive paste and the oxide (contact intimacy is more important on thin oxides.) An inadequate intimacy of contact may be due to the size and shape of the conducting particles in the paste being such that the surfaces of the conducting spheres could not contact the oxide at every point of its area. In the case of thin oxides, one can obtain a measure of the inversion voltage by observing the effects of oxide surface ions. That is, the techniques described in Reference 7 can be used to measure the minimum voltage on the metal that will induce channeling beyond the metal. The difficulties involved with making measurements of inversion voltages on thin oxides are relatively

unimportant because MOS microcircuits should be designed so that there are no regions with thin oxides not covered by metal.

Concerning question 2, we have measured differences between the inversion voltage in regions not covered by metal and those that are covered by metal of approximately 60 volts on an oxide thickness of 13,000 Å. This is what one would expect if there were 10^{12} fast states per cm^2 in the regions not covered by metal -- a not unexpected density in view of our data given in Table I of Scientific Report No. 3 where we report finding 6×10^{11} to 25×10^{11} fast states per cm^2 for the situation in which the metal is removed before alloying.

If the alloying is performed after the delineation of the aluminum, the inversion voltage in regions not covered by aluminum is not likely to present a problem.

Surface Conductivity

In Scientific Report No. 3 we described (pages 46 and 47) a test structure having interdigitated electrodes that was designed to measure directly the surface conductivity of the top surface of an insulator. This structure, designed for LSI reliability studies on a related program, has also been described in Reference 1. This structure, shown in Figure 20, has a surface conducting channel geometry with a width-to-length ratio of 5000.

The difficulties involved in measuring the surface conductivity directly were discussed on pages 46 and 48 of Scientific Report No. 3. On pages 48 and 49 of that report, and in a published paper[6], we discussed the relative advantages of the surface-ion test structure.

In spite of the difficulties involved in making a direct measurement of the surface conductivity and in relating surface conductivity measurements to the behavior expected of microcircuit structures, direct measurements of surface conductivity provide information not otherwise obtainable and therefore we have done further work with the test structure shown in Figure 20. We find we can measure the surface conductivity with this structure at a 90% relative humidity, and that we can compare the surface conductivity for various dielectric materials. The humid ambient increases the surface current to conveniently measurable levels and makes the current through the insulator relatively negligible. The data in Figure 21 show the results taken on thermally grown SiO_2, vapor-plated SiO_2, and vapor-plated SiO_2 containing 3% (by weight) phosphorus. The aluminum was evaporated from a tungsten coil as is typical for bipolar microcircuits. Measurements taken on MOS capacitors show that such an evaporation deposits more than 10^{12} sodium ions/cm^2 on the oxide surface. Data are shown for three values of voltage on the silicon substrate relative

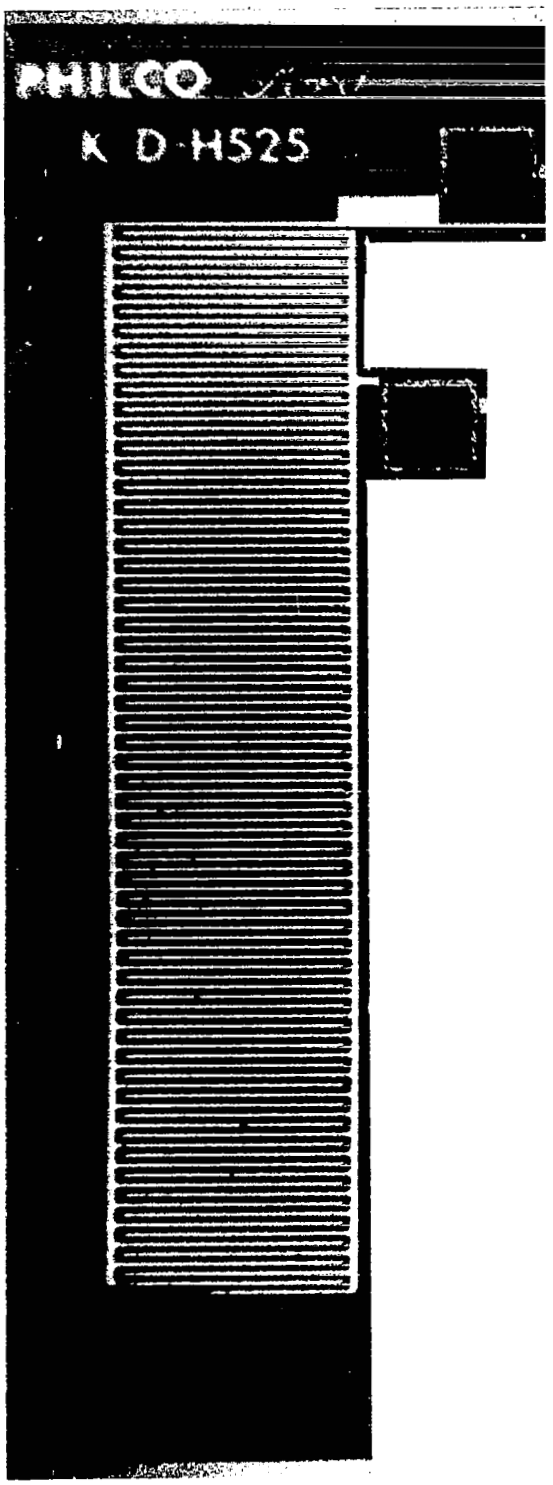


Figure 20. Test structure for the direct measurement of surface conductivity.

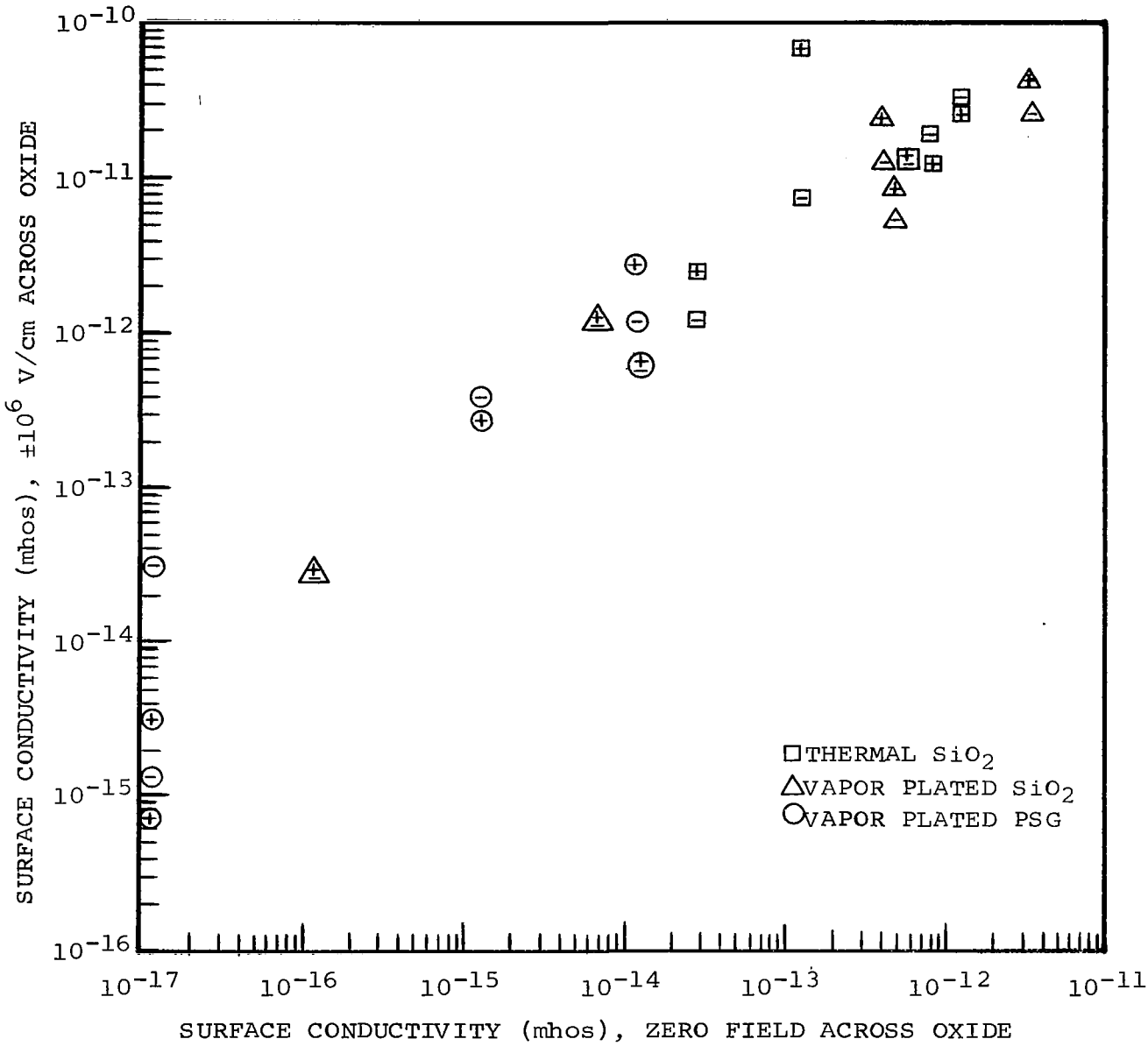


Figure 21. Surface conductivities of several oxides for several transverse electric fields.

to the metal. The voltage between the interdigitated electrodes was 1.5 volts.

Concerning these data, the following points must be stressed. We find that the surface conductivity is time dependent during its measurement. We have observed an increase in surface conductivity with time and then subsequently a decrease over a period of roughly two hours. We believe the increase is due to a slow build-up of the surface charge density due to the application of the substrate potential, while the decrease is due to a polarization of the surface charge density or a development of an insulating area on the surface due to an electrolytic evolution of gas. The data shown in Figure 21 were taken immediately after the voltage was applied.

While much further study could be proposed in this area,we do not consider the cost of such a study to be justifiable in this program in view of the stated objectives of the program. Such study would be more appropriate for a research effort with the objective to study the detailed nature of surface conductivity.

The data in Figure 21 show:

1. The utility of our test structure for measuring surface conductivity directly. It provides an additional means for comparing insulator surfaces.

2. Vapor plated oxides have lower surface conductivities than thermally grown SiO_2. This seems to be most pronounced in the case of the phosphosilicate. A phosphosilicate layer might be expected to be hygroscopic and therefore expected to have a high surface conductivity. In contrast, Snow and Deal[21] report that the bulk resistivity of phosphosilicate is at least a factor of 25 lower than that for SiO_2. One might postulate that the surface conductivity is due to sodium ions and that phosphosilicate immobilizes these ions.
3. Surface conductivity increases when there is a voltage applied to the substrate. This confirms our model described in Reference 7.
4. There is good correlation between the surface conductivity measured at different values of substrate bias.
5. Surface conductivity is fairly insensitive to the polarity of the voltage applied to the substrate.

Effect of an Applied Gate Voltage at an Elevated Temperature on the Threshold Voltage of MOS Transistors

Deal et al.[22] and Goetzberger[23] have reported that the application of a voltage to an MOS capacitor at an elevated

temperature alters the immobile charge density (Q_{ss}) in the oxide. We have demonstrated that this phenomenon also occurs on MOS transistors, as shown in Figure 22. This phenomenon can be important during the alloying operation as indicated by the data shown in Figure 23. These data were taken on two groups of alloyed MOS transistors from the same wafer. The only difference between the two groups was that in one of the groups the charge was removed from the gate of each transistor by contacting with a zero biased probe before the alloying step. The data in Figure 22 show that the devices that had the charge removed exhibited a more uniform inversion voltage after the alloying operation. We believe that this demonstrates that charge on the metal of an MOS structure can influence the MOS system during the alloying operation to alter the effective charge in the oxide. We believe that the charge on the capacitors was due to wafers sliding over each other in a petri dish. This would not occur in normal processing because wafers containing microcircuits would not be allowed to slide over each other because the metal pattern can be scratched.

Because of the effect of gate voltage during alloying on the transistor characteristics, our set of test structures includes MOS transistors in which the gate is tied to a p-type region in the silicon. This is described on page 16 of this report.

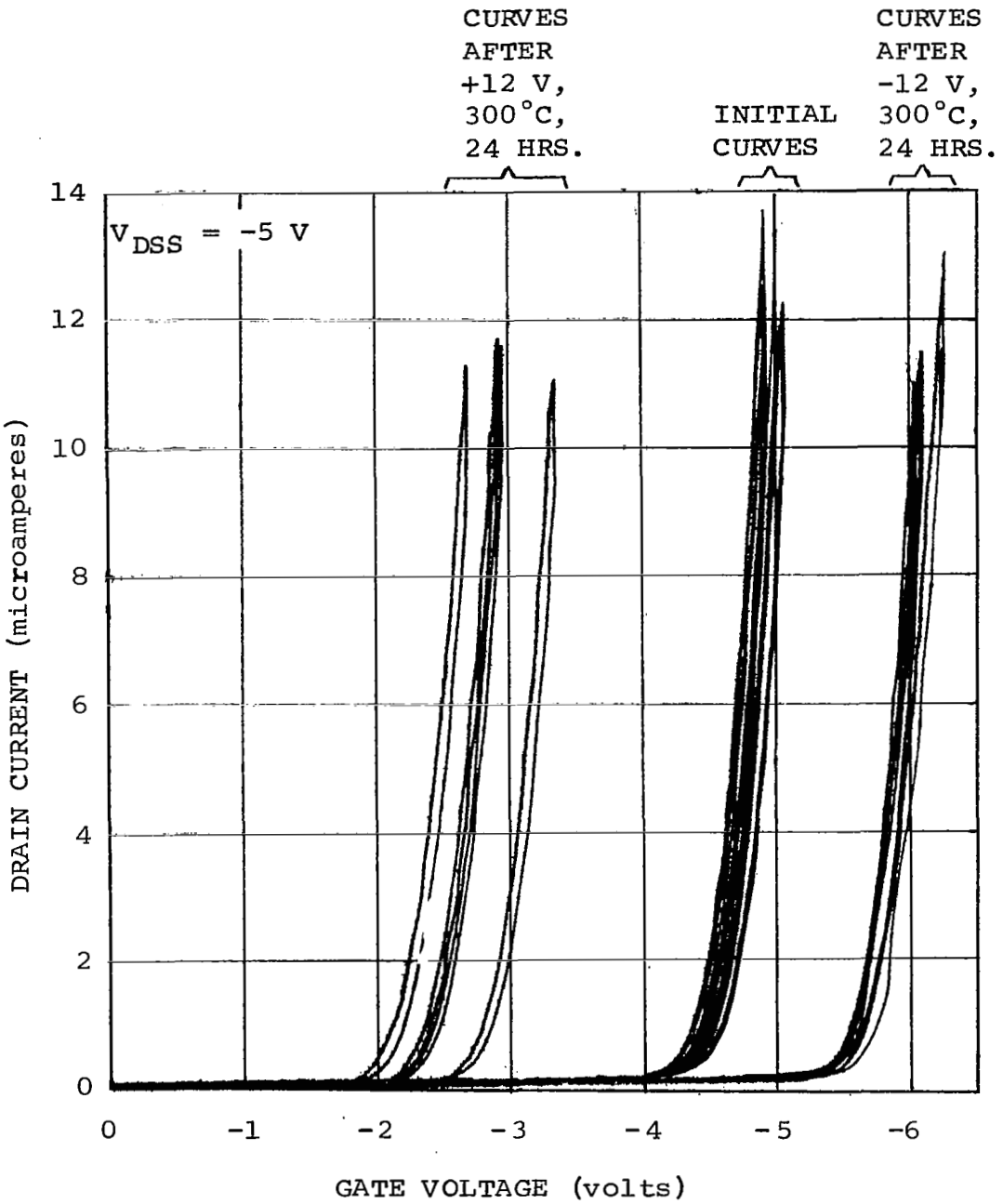


Figure 22. Effect of applied bias at an elevated temperature on the threshold voltage of MOS transistors.

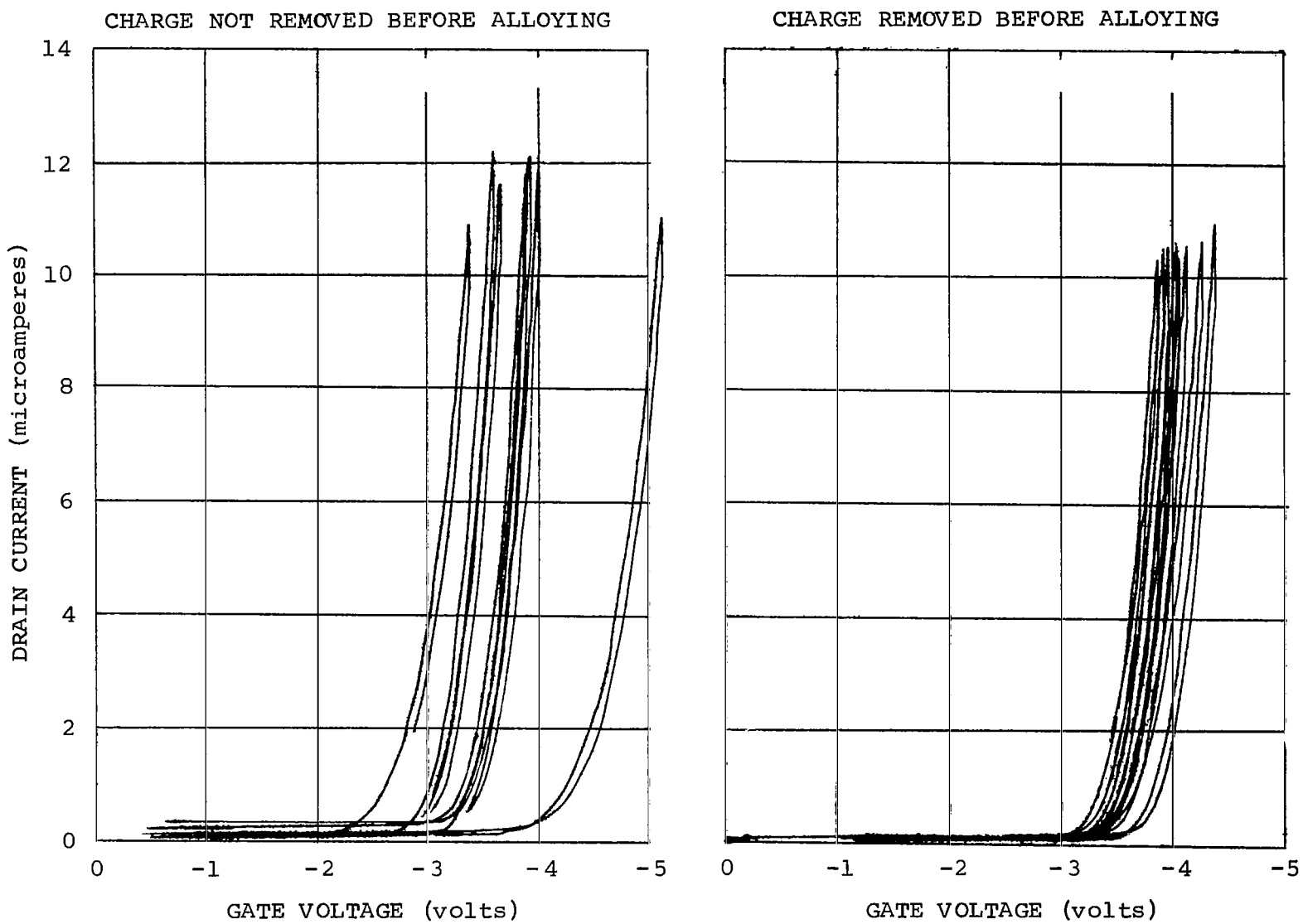


Figure 23. Effect of charge on the metal during alloying on threshold voltage of MOS transistors.

At the alloying temperature it would be impossible, during alloying, for such a device to have a non-zero voltage on the gate. Test transistors with floating gates might have different threshold voltages than the circuit transistors that they are to represent. A circuit transistor always has the gate metal connected to the silicon at a drain of another transistor or at a protective diode.

Instability in Protective Diodes

Because of the susceptibility of MOS transistors to the development of shorted gates due to breakdown of the gate oxide, manufacturers design the input terminals of microcircuits to have protective p-n junction diodes in parallel with the input to limit the voltage applied across the oxide. To increase the protection, gate controlled diodes are used because they have lower breakdown voltages. A gate controlled diode is a junction diode having a metal electrode overlying and electrically tied to the high resistivity side of the junction. A negative voltage applied to the p-type diffused region will induce positive charge on the metal. This positive charge increases the field in the depletion layer and therefore decreases the breakdown voltage. Note the similarity between the protective diode

structure and an MOS transistor, making it easy to include in MOS microcircuit chips.

For process control and product reliability, we monitor the breakdown voltage of the drain of an MOS transistor with the gate and source tied to the substrate. We find that this breakdown voltage is significantly increased by the measurement itself. Our measurements show that this increase is quite small (<4%) if a voltage just below breakdown is applied for a period of 16 hours. On the other hand, if avalanche current is drawn, the breakdown voltage can increase by more than 30% in less than a minute. We believe that the increase is due to avalanche generated energetic electrons being injected into the oxide in a manner somewhat related to that reported by Nicollian and Goetzberger.[24]

We have measured this increase on p-channel MOS transistors made by a variety of processes including wafers having <100> and <111> orientations, and have found no significant differences. We found similar instability in devices made by several other manufacturers. Similar results have been reported by investigators at Texas Instruments[25] and Motorola.[26]

We find that this instability in breakdown voltage is not observed on n-channel transistors. We believe that this is due to the difference in barrier height for electrons from the silicon

to the oxide (3.15 eV) and that for holes (3.75 eV). Also, with p-channel devices the polarity of the operating voltage drifts electrons from the silicon to the oxide while in n-channel devices the electrons would be drifted away from the oxide.

CONCLUSION

1. The effectiveness of a new set of test structures has been proven. This set has advantages over our previous sets of test structures in that:
   a. The processes used for its fabrication are the same as those used for building production MOS microcircuits.
   b. The single set includes a sufficient number of test structures for the evaluation of each type of region in the microcircuit.
   c. New test structure types have been included, and previously existing types have been redesigned to be more sensitive.
2. The considerations involved in the design of each of the test structures have been presented in detail, along with a discussion of the uses of each.
3. A discussion is given of various means for handling problems that arise in the use of these test patterns.
4. Theoretical considerations have been used to set up criteria by which simple leakage current measurements taken on complex circuits might be used to identify the cause of degradation of failure in individual microcircuits.
5. An additional model has been proposed concerning an effect which a deposition of a dielectric may have on the characteristics of a microcircuit.

6. An accelerated aging test has been conducted with MOS transistors on production wafers of commercially available types of microcircuits. Samples were tested both with and without a vapor-plated phosphosilicate second-layer dielectric. The data show that the transistors are not degraded by the deposition and presence of the vapor plated phosphosilicate.

7. It has been demonstrated that a barrier (to mobile ions) layer in the insulator does not insure device stability if there are mobile ions in the layer of insulator overlying the barrier layer.

8. The work of other investigators has been corroborated that silicon nitride over a thermally grown SiO_2 layer increases the flat band voltage and impedes the annihilation of fast states.

9. The importance of measuring inversion voltages both in regions covered by metal and in regions not covered by metal has been discussed. Two techniques for measuring inversion voltages in regions not covered by metal have been discussed. Experimental data that show the relationship between these inversion voltages have been presented.

10. Experimental data have been taken that show a lower limit for the temperature for the complete annealing of fast states with hydrogen. Data are presented on the effects of silicon nitride and of electroless nickel on the annealing of fast states.

11. Experimental data have been taken showing that the fast states are not annealed out under narrow aluminum lines by processes that anneal out essentially all the fast states under wider metal lines.

12. Experimental data have been taken showing that surface recombination velocities of thermally oxidized silicon are increased by the addition of a vapor-deposited layer of SiO_2 or phosphosilicate. A small increase occurs if the second layer is deposited over a metallized (aluminum) sample of thermally grown SiO_2. Further, it has been shown that a process that increases the surface recombination velocity can at the same time change the surface potential so that the overall effect is a lower leakage current.

13. The possibility of making direct measurements of surface conductivity of an insulator of the type found in microcircuits has been established. Vapor-plated phosphosilicate has been shown to have a surprisingly low surface conductivity in comparison with that of thermally-grown SiO_2.

14. Additional data have been taken that support a hypothesis given in Scientific Report No. 3 that a p-n junction influences the mobile ion content in an MOS transistor. This has several important implications. One can infer that p-channel MOS microcircuits should be more stable than either

n-channel or complementary MOS microcircuits. Also, this phenomenon should be taken into account in the establishment of design rules, i.e., design rules might be different for these three types of MOS microcircuit.

15. Another hypothesis given in Scientific Report No. 3, that an insulator surface getters mobile ions, was not supported by additional data possibly because of other influences of greater significance.

16. It has been demonstrated that an applied gate voltage at an elevated temperature alters the threshold voltage of MOS transistors due to a phenomenon reported earlier for MOS capacitors.

17. A phenomenon believed to be due to avalanche injection of electrons into oxide layers has been subjected to experimental study and its implications for microcircuit reliability have been discussed.

RECOMMENDATIONS

We recommend that work be continued to:

1. Conduct theoretical and experimental studies of the factors which affect the fundamental electrical properties of the $Si-SiO_2$ interface of structures having two dielectric layers.
2. Further develop the models and the understanding of each of the surface-related causes of instability ir multilevel microcircuits.
3. Conduct correlation studies to establish the value of test vehicles for the determination of the reliability of actual microcircuit structures of both the bipolar and MOS type.
4. Correlate the effects on life test data of deposited second-layer insulators on structures used in LSI arrays with measurements taken on test structures.
5. Conduct investigations to evaluate specific process changes for the improvement of microcircuit reliability.
6. Establish whether mobile ions exist at an interface between two insulator layers.
7. Study the effects of depositing insulator layers over the metal on samples having Al_2O_3 or Si_3N_4 under the metal.

8. Study the effects of heat treatments used to improve the contact resistance in vias between two layers of metal on the properties of the oxide-silicon interface.

9. Utilize the results of this program to improve the reliability of microcircuits by the establishment of appropriate design rules.

10. Prepare a discussion of the effects on reliability of a conversion from <111> to <100> oriented silicon.

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APPENDIX A

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APPENDIX B

NEW TECHNOLOGY

To conform to the requirements of the New Technology clause of the contract, a review meeting was held to determine the reportable items. Personnel participating in the review included G. L. Schnable, the Program Manager, and E. S. Schlegel, the principal investigator on the program.

A list of reportable items is given below. These items are inventions, discoveries, improvements, or innovations.

1. New test structure set for general use with MOS microcircuits (Pages 7-19.)

A new set of test structures has been built and demonstrated for general use with production MOS microcircuits. Compared with the previous set of test structures, this set has the advantages that it is prepared by the exact process that is used in the production of MOS microcircuits, it contains test structures for evaluating each type of region in the microcircuit, and it contains new, and improved, test structures.

2. Improved MOS transistor test structures. (Pages 16-18.)

The new set of test structures includes MOS transistors for testing:

a. Effects of channel length

b. Similar devices with and without gate metal.

3. Discovery that fast states are not annealed from regions under narrow metal lines. (Pages 55-57.)

The discovery was made that the effectiveness of aluminum in the annealing of fast states is practically eliminated if the metal line width is small (~0.2 mil).

4. Demonstration of capability to measure surface conductivity directly. (Pages 70-75.)

It has been demonstrated that direct measurements can be made of the surface conductivity of dielectric layers of the types used in microcircuits.

5. Demonstration of effects of substrate bias on the surface conductivity. (Pages 70-75.)

Data have been taken that support a model proposed in earlier work in this program in which it was postulated that the substrate bias influences the surface conductivity of a dielectric layer of the type used in microcircuits.

The discovery was made that the surface conductivity is affected equally by applied substrate voltages of either polarity. The discovery was made that the surface conductivity with an applied substrate voltage is proportional to that with zero applied substrate voltage.

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