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PHASE INTERPOLATION CIRCUITS FOR SCANNING PHASED ARRAYS

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SUMMARY

The classes of circuits described in this report can be used with a phased array antenna in order to allow a given array feed system to provide phase control for a phased array with many more elements. Alternatively, certain variations of these circuits can be used alone to provide phase control for small arrays while using only a single phase shifter for each direction of scan.

INTRODUCTION-

PHASE INTERPOLATION CIRCUITS FOR SCANNING PHASED ARRAYS

Recent developments (refs. 1-4) in the area of intermediate frequency phasing devices for scanning phased array antennas have led to systems which when properly calibrated can very precisely control the phases applied to array elements. Each of these systems offers particular advantages and disadvantages, but a feature common to most of them is the somewhat reduced phasing accuracy or greatly increased expense as the array is made progressively larger. The rapid scan capability and the relatively high phase accuracy of these analog systems as compared with arrays steered by conventional phase shifters, makes them attractive for many applications, especially those involving time shared multiple beams. This report describes two types of circuits to increase the number of elements which can be phased by an intermediate frequency phasing device such as those described in the references. An advantage of the circuits described herein is that they are duplicated many times in an array and so if implemented in stripline they can be constructed relatively inexpensively. In addition, it is expected that a system using these circuits would incorporate amplification at each antenna element after the signals from this device are up-converted to the appropriate transmit or receive frequencies.

In order to understand the function of such circuits, consider a linear array which is phased using an intermediate frequency phasing device. Since these devices are quite expensive to construct, it is desirable to extend their utility by providing some circuitry so that the same device can scan more antennas. An ideal system would be one which produced an extra set of phased outputs whose phases lie mid-way between those of the output of the original phasing device. Each phase line could then be said to be interpolated between the original adjacent phases. If this procedure is repeated several times, then the number of antennas phased by a given device is increased many-fold. Alternatively, one might conceive of a single device which produces not merely a single signal with phase half way between two other phases, but one which splits the interval into, say N intervals.

INTERPOLATION USING LINEAR CIRCUITS

The most obvious circuit for interpolating between two given signals is a simple sum hybrid as shown in Figure 1. Two adjacent signals are combined vectorially to pick off their vector summation. If the signals are $S_1 = \cos \omega t$ and $S_2 = \cos (\omega t + \theta)$; then the resulting signal is $\frac{1}{\sqrt{2}} \frac{\sin \theta}{\sin \theta/2} \cos (\omega t + \theta/2)$. The signal is at the phase angle $\theta/2$ for θ less than 180^o and has an amplitude modulation dependent upon θ such as that shown in Figure 1. This figure only shows the result up to $\theta = 90^o$, because the amplitude becomes severely modulated for larger angles, and is zero at $\theta = 180^o$. Consequently, this simple circuit is useful mainly in the range $-90^o \leq \theta \leq 90^o$, where the amplitude

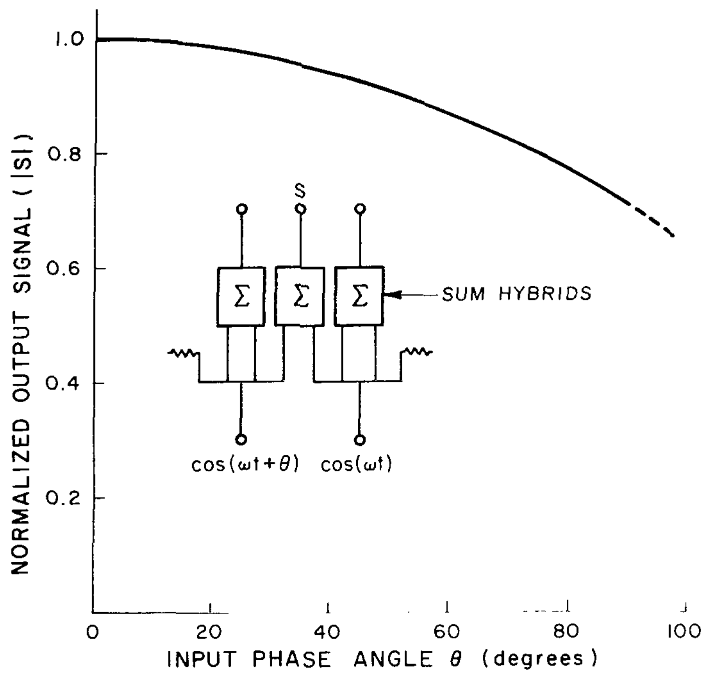


Figure 1.- Amplitude modulation of linear phase interpolating circuit

modulation is such that it can easily be removed by a phase insensitive limiter. Although not shown in the figure, it is possible to derive a linear circuit using switched 180° and 90° phase shifts in conjunction with this device which will perform the phase division without ambiguity for arbitrary input phase angles.

The circuit may of course be used a second time to further subdivide the given phase angles and increase the number of antennas phased by this system, although when this is done the amplitude modulation resulting from the first subdivision will result in phase error in the second group of interpolated signals. Figure 2 shows this second stage of phase interpolation with one input signal given by the output of the circuit of Figure 1

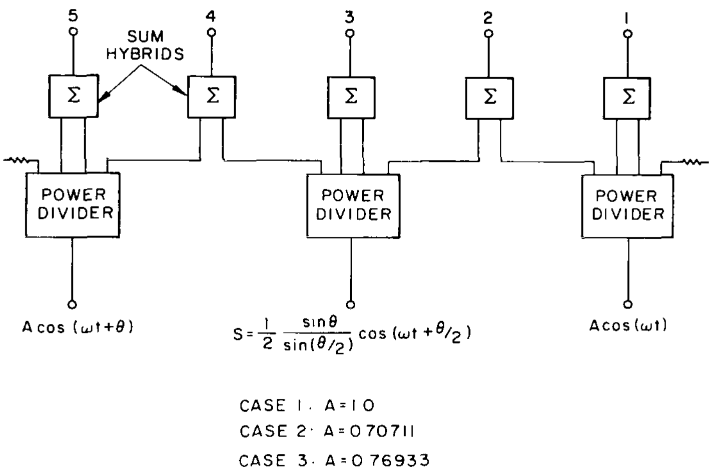


Figure 2.- A second stage of phase interpolation

$S = \frac{1}{2} \frac{\sin \theta}{\sin (\theta/2)} \cos (\omega t + \theta/2)$ and the other input signals are $A \cos\omega t$ and $A \cos(\omega t + \theta)$. For the case when $A = 1$, this circuit can be driven directly from the output of the circuit shown in Figure 1. In that case the maximum phase error occurs at $\theta = 90^\circ$ and is 4.07° (at terminals 2 and 4). Alternatively, the circuit can be designed to give zero phase error at 90° by setting $A = 0.707$ (Case 2). When this is done the maximum phase error is about 1.6° and occurs at about $\theta = 65^\circ$. Figure 3 shows a comparison of experimental and theoretical results using these two types of circuits. The ideally interpolated phase angles are the straight solid lines on this figure. The interpolated error can be reduced to a minimum over the $-90 \leq \theta \leq +90$ degree range by making $A = 0.76933$ (Case 3). When this is done the maximum error is about one degree and this error occurs at two places, θ equal to about 10 degrees and 90 degrees.

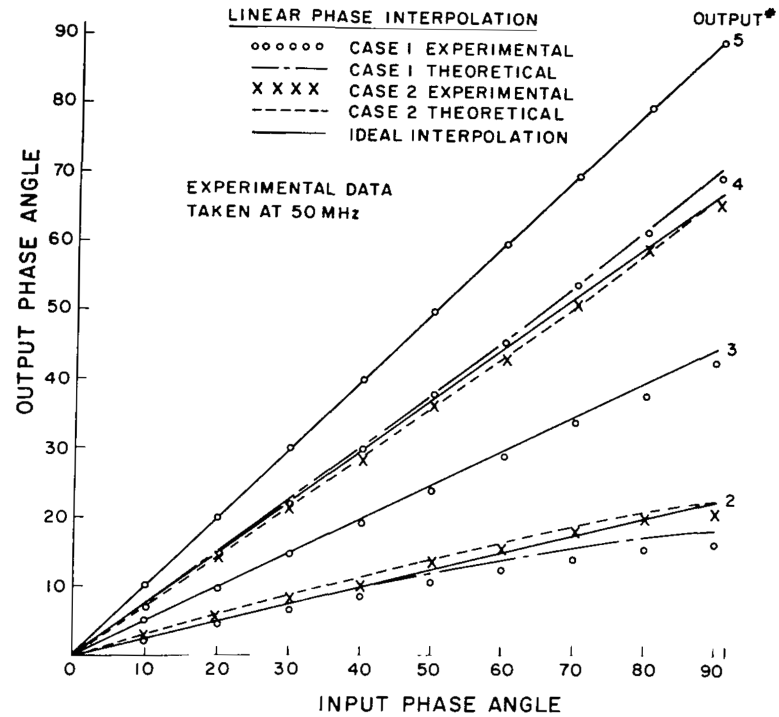


Figure 3.- Output phase vs input phase for linear phase interpolation (2 stages)

A further comparison of these alternatives reveals that if switches are to be used to extend the range of the first interpolation, and if no amplitude correction is provided for the switched signals, then the basic linear interpolation circuit (Case 1; A = 1) offers the least error over large interpolation angles. However, if these circuits are to be used in conjunction with frequency multipliers, then the modifications (Case 2 and Case 3) become the more appropriate solutions. In such cases one might expect to be able to use interpolation three or at most four times, therefore increasing the number of phased output terminals to 9 or 17 for every two input terminals. The maximum phase increment between these outputs (assuming 90° input phase variation and no switching) becomes 11.25° or 5.625°, and so to derive normal phase differences of the several hundred degrees needed for conventional phased array systems requires relatively large frequency multiples. Since the phase error is also multiplied, there is a very definite upper bound on the number of phase interpolations one should perform without switching. In those cases where switching can be practically used and if one is willing to switch in attenuation as well as the 90° and 180° phase shifts, then relatively longer chains of linear phase interpolation circuits can be implemented with good phase accuracy, although at the cost of greater complexity and control requirements.

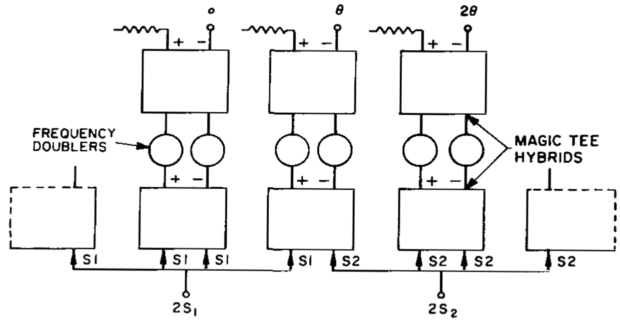
In general, if there are M input terminals, and one uses N stages of interpolation, then the total number of output terminals is:

$$(M-1)\left[2+\sum_{n=0}^{N-1}(2)^{N-1}\right]$$

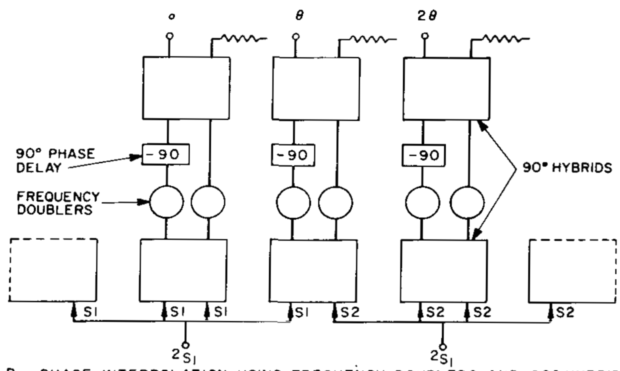
The necessity of performing switching operations arises because of the need to resolve the ambiguities resulting from dividing arbitrary large angles. It is for this reason that truly linear circuits cannot function over wide phase difference ranges. A class of nonlinear phase interpolation circuits is described in the remainder of this note.

PHASE INTERPOLATION USING DOUBLERS

The phase interpolation circuit using doublers is not only the most convenient one with which to introduce the concept, it also possesses characteristics which, under certain conditions, make it preferable to any other of the class of interpolating circuits. Two variations of this basic circuit are shown in Figure 4. To trace the interpolated signal of Figure 1A, consider the two adjacent signals $S_1 = \cos \omega t$ and $S_2 = \cos (\omega t + \theta)$ (hereafter the notation $S_1 = \underline{\omega/0}$ and $S_2 = \underline{\omega/\theta}$ will be used interchangeably with the above). At the sum and difference ports, respectively, of the center 180° hybrid shown in 1A, the signals are $\frac{1}{\sqrt{2}}(S_1 + S_2)$ and $\frac{1}{\sqrt{2}}(S_1 - S_2)$. If the doublers are ideal square law devices then the respective doubler outputs are proportional to $\frac{1}{2}(S_1 + S_2)^2$ and $\frac{1}{2}(S_1 - S_2)^2$. The difference term at the output magic tee is $\sqrt{2}\, S_1 S_2$. The corresponding signal at frequency 2ω is $\frac{1}{\sqrt{2}} \cos (2\omega t + \theta)$. The same processes can be used to derive the outputs at the left and right of this one. These signals are: $\frac{1}{\sqrt{2}} \cos (2\omega t)$ and $\frac{1}{\sqrt{2}} \cos (2\omega t + 2\theta)$. Thus it can be seen that the circuit of Figure 4A does provide three output signals of which one has a phase angle mid-way between those of the other two. The signals are at twice the frequency of the original control signals. If this process is repeated for each of the M output signals of a phasing device, the new device will phase (2M-1) elements. It should also be clear that the procedure may be performed a second time in principle and so phase an array of 4M-3 elements, etc. The circuit of Figure 4B performs the same function but uses 90° hybrids instead of the 180° hybrids of Figure 4A. It should be noted that in Figure 4 the signals at 0 and 2θ are derived using interpolation circuits. This procedure has



A PHASE INTERPOLATION USING FREQUENCY DOUBLERS AND MAGIC TEE HYBRIDS



B PHASE INTERPOLATION USING FREQUENCY DOUBLERS AND 90° HYBRIDS

Figure 4.- Several configurations for phase interpolation using doublers

advantages because of its symmetry, but it is obviously not necessary and probably cannot be justified economically except for the doubler circuit. In the circuits shown later, which use a higher order of multiplication, it will be assumed that the 0 and $N\theta$ terms are derived using multipliers and the appropriate phase shift and attenuation.

A unique feature of the phase interpolation circuit using doublers, is that it may even be used when the frequency doubler conversion loss differs considerably from square law. Many commercially available doublers have conversion loss characteristics similar to those shown in Figure 5. Since the power at each doubler is a function of phase angle one is led to suspect that there would be phase error and amplitude modulation of the output signal as the scan angle is changed. The advantage of this circuit can be seen by the following analysis. Assuming that the doublers are identical and have phase shift characteristics independent of power, the output signal of any frequency doubler in the system whose input signal is S is now given by: $S^2A(|S|)$ where $S = |S| \cos(\omega t + \theta_S)$ and $A(|S|)$ is a transmission factor for the doubler circuit. This transmission factor for square law devices is therefore defined to be $\frac{2C(|S|)}{|S|}$, where $-20 \log C(|S|)$ is the conversion loss.

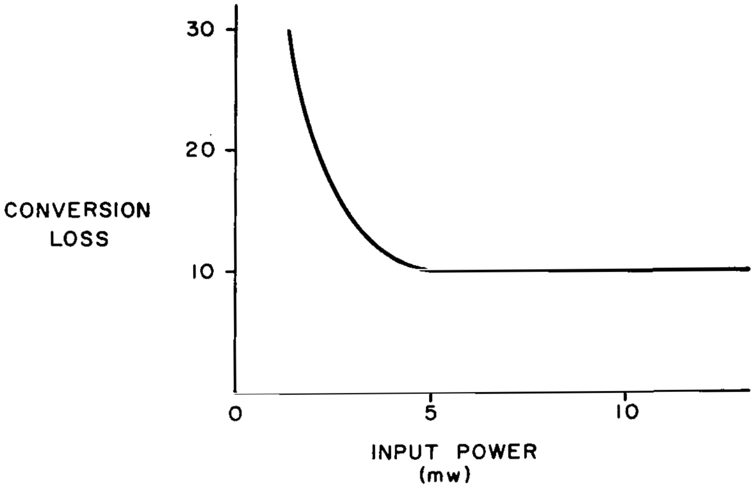


Figure 5.- Conversion loss vs. input power for typical frequency doubler

Referring to Figure 4A, the output of the doubler at the right is therefore $\frac{1}{2}(S_1 + S_2)^2 A(|\frac{S_1 + S_2}{\sqrt{2}}|)$ and of the doubler at the left, $\frac{1}{2}(S_1 - S_2)^2 A(|\frac{S_1 - S_2}{\sqrt{2}}|)$. The signal at the difference port of the output magic tee is therefore $\frac{1}{\sqrt{2}}$ times the first of these minus the second. Combining these terms and writing the frequency components at 2ω, one obtains the output signal:

$$\frac{1}{4\sqrt{2}} \Big\{ [A(|\frac{S_1 + S_2}{\sqrt{2}}|) - A(|\frac{S_1 - S_2}{\sqrt{2}}|)] \cos 2\omega t$$

$$+ [A(|\frac{S_1 + S_2}{\sqrt{2}}|) - A(|\frac{S_1 - S_2}{\sqrt{2}}|)] \cos (2\omega t + 2\theta)$$

$$+ 2[A(|\frac{S_1 + S_2}{\sqrt{2}}|) + A(|\frac{S_1 - S_2}{\sqrt{2}}|)] \cos (2\omega t + \theta) \Big\}$$

The third term of this expression is the desired interpolated term with phase angle θ. This term is severely amplitude modulated as a function of θ because of the bracketed term which multiplies it. The first two terms of the above expression represent signals with phase angles zero and 2θ. Since they are multiplied by identical coefficients, their resultant phase angle is also θ. Moreover, it can be shown that the amplitude modulation imposed upon this signal is such as to decrease the net amplitude modulation of the total resultant signal. The output signal indicated above can therefore be written as $\frac{1}{\sqrt{2}} A(|r|) \cos(2\omega t + \theta)$ where r varies between a maximum of 1.414 and a minimum of 1.0 (the input signal S_1 and S_2 being normalized to one as before). Thus, even if the signals S_1 and S_2 are in the range of saturation of Figure 5, the doubler interpolation system will operate with no phase error and only 3 dB of modulation even though the double conversion loss differs considerably from that for square law response. The 90° hybrid circuit of Figure 4B can be shown to possess the same characteristic. Figure 6 shows a comparison of experimental and theoretical results for the doubler phase interpolation circuit for various input signal levels using HP 10515A doublers. The experimental data confirms the expected phase accuracy and modulation characteristics.

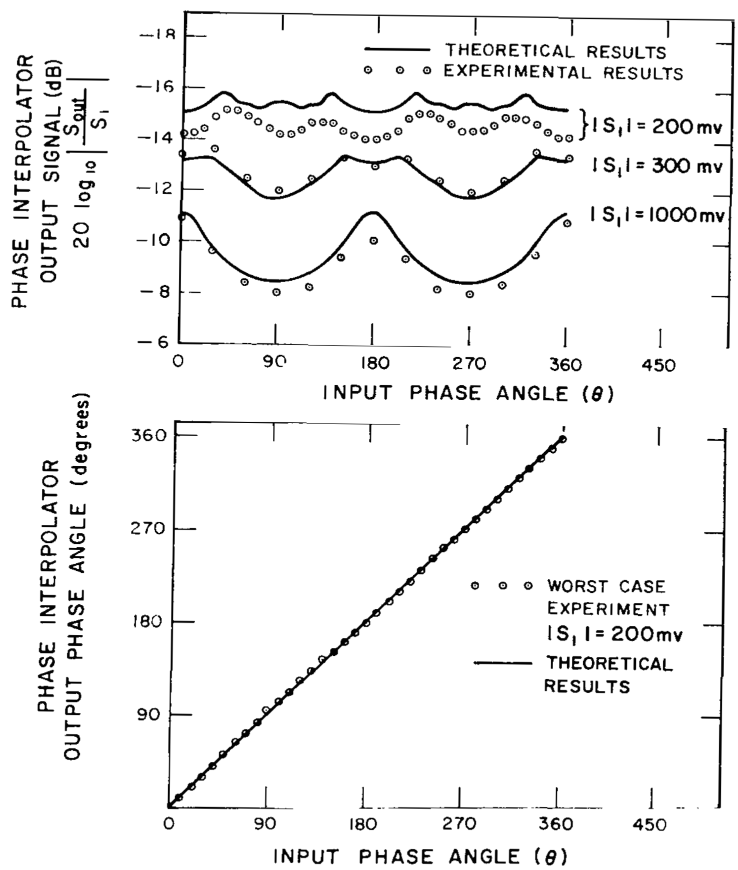


Figure 6.- Theoretical and experimental results for phase interpolation using doublers

This feature is unique to the doubler interpolating scheme and is not present for circuits which perform phase interpolation using multiplication of order N. Therefore, except for this specific case, the general class of circuits discussed in the next section requires the use of ideal power law multipliers.

GENERALIZED PHASE INTERPOLATING CIRCUITS USING MULTIPLICATION OF ORDER N

The doubling circuit described earlier accomplishes its function of separating out the signal which is related to the S_1S_2 term of the squared signal combination. This angle is at θ, and so it is the only integral number of the input phase shifts (θ) between 0 and the highest phase shift in the system, 2θ. If a higher order of multiplication, say the order N were used, there would be (N-1) integral multiples of θ possible between the phase shift extremes 0 and $N\theta$. If the signals possessing these phase angles could be separated, it would be possible to implement a system which selects a number of interpolated phase points between two given input signals. This circuit would then represent the ultimate generalization of the phase interpolation with multiplication principle.

In order to devise an interpolation scheme of order N, one divides the power of each of the two phased input signals into N parts. The signals at the first N terminals are all $S_1 = \cos \omega t$ and at the second N terminals $S_2 = \cos (\omega t + \theta)$. Using appropriate phase shifters and magic tee hybrids, one constructs the set of N-signals:

$$S^0 = (S_1 + S_2)$$

$$S^1 = (S_1 + S_2\underline{/\Delta})$$

$$S^2 = (S_1 + S_2\underline{/2\Delta})$$

$$S^{N-1} = (S_1 + S_2\underline{/(N-1)\Delta})$$

where the notation $S_2\underline{/p\Delta} = \cos (\omega t + \theta + p\Delta)$ is used throughout, and where $\Delta = \frac{2\pi}{N}$. These signals are used as the inputs to a set of power law frequency multipliers of order N. These components raise S^p to the power N and filter the signal at $N\omega$. From the binomial expansion one can show that the term in each $(S^p)^N$ which has its phase angle equal to some general integral number M times θ is written:

$$\frac{N(N-1)(N-2)\ldots(N-M+1)}{(M)!} \quad (S_1)^{(N-M)} \quad \cos\,(\omega t + \theta + p\Delta)^M$$

Apart from the amplitude factor which is common to each S^p, the component of this expression at the frequency $N\omega$ is given by

$$\cos\,(N\omega t + M\theta + Mp\Delta).$$

In view of the mathematical relationship

$$\sum_{p=0}^{N-1} \cos\,[N\omega t + M\theta + p\Delta(M-K)] = \begin{cases} 0 & K \neq M \\ N \cos\,(N\omega t + M\theta) & \text{for } K = M \end{cases}$$

it is clear that in order to separate out the term with phase angle $M\theta$ from all others one must build a circuit so that each signal $(S^p)^N$ is delayed by the phase angle $Mp\Delta$ before combining all the signals. The notation $(S^p)^N \underline{/-Mp\Delta}$ is used to indicate this operation. Therefore, each signal $(S^p)^N$ is divided into N-1 parts (using a power divider) and the appropriate phase delays are inserted before combining the signals to form the summations.

$$\Sigma(M\theta) = \frac{1}{\sqrt{(N-1)}} \sum_{p=0}^{N-1} (S^p)^N \underline{/-Mp\Delta} \qquad M = 1,2\ldots N-1$$

Using the previous relationship, this sum is seen to be free of all terms at phase angles other than $M\theta$. This construction has therefore yielded the set of signals with interpolated phase angles θ, $2\theta'$,...(N-1) θ which lie equally spaced between the extreme phases 0 and $N\theta$. The circuit which performs this interpolation is shown in Figure 7.

It is important to point out several additional facts about the general circuit. The first is that it does not exhibit the same invariance to multiplier power sensitivity that is displayed by the doubler circuit. Indeed, it can be shown that if the multiplier parameters do vary from power laws, then both amplitude modulation and phase error are evident at the interpolated signal output terminals. It should be emphasized that this is not a trivial requirement, and requires the use of quite special multipliers. Most conventional frequency multipliers have output power

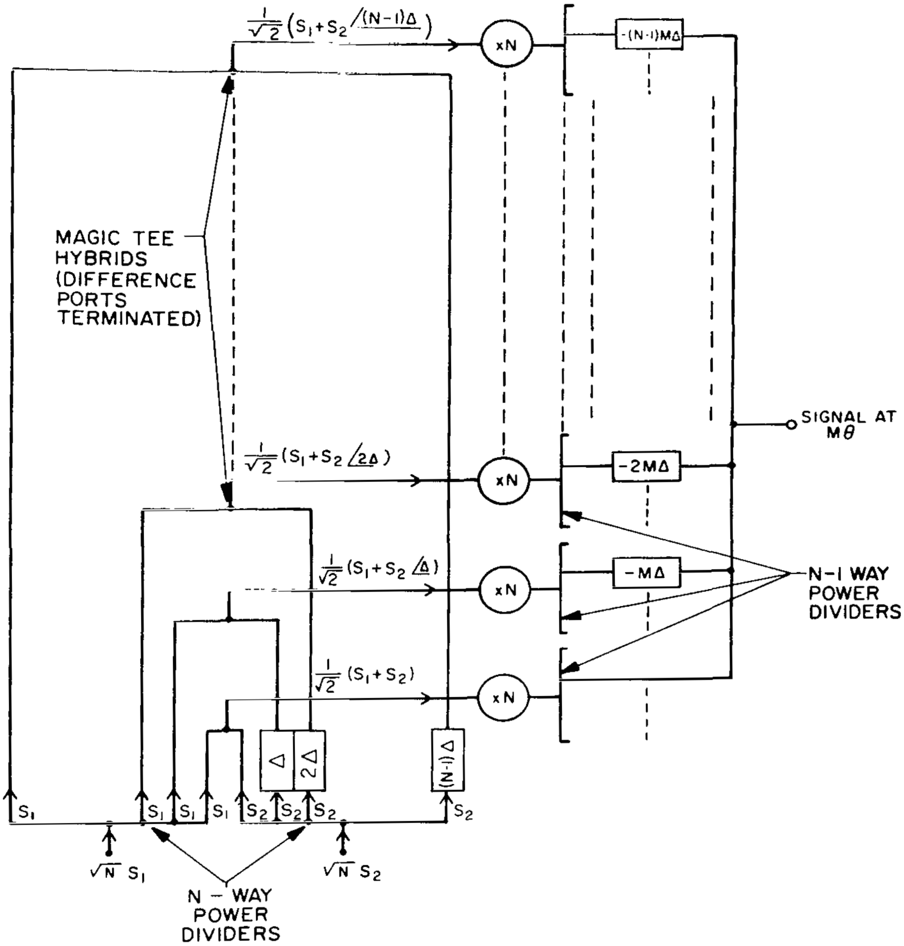


Figure 7.- General circuit for phase interpolation using multiplication of order N

which varies linearly with input power. The second feature of importance is that the various interpolated terms are of different amplitude for N > 3. This arises because of the binomial coefficient amplitude factor multiplying the various terms in the power expansion $(S^p)^N$. This factor limits the practical upper bound of the order of multiplication. Beyond the order 5, the amplitude ratio of the center element signal ($\frac{N\theta}{2}$ for N even, or $\frac{(N-1)\theta}{2}$ for N odd) to those at the interpolated angles θ and (N-1) θ exceeds 2.0. Beyond the order of 10 this ratio exceeds 25.0. Directional couplers, attenuators or limiters may be used to equalize these signals, but when the difference in signal amplitude becomes too great this too becomes impractical.

Subject to these two limitations, the phase interpolation scheme for general order N multiplication should provide a convenient and practical means of increasing the number of antennas which can be phased by a given system. In addition, the special case N=2 is seen to be nearly independent of the above limitations and so can be used for a less restrictive set of conditions.

REFERENCES

1. Huggins, W. H.: Generalized Radar Concepts with the Use of Array Antennas. Rand Report No. 1854, ASTIA No. AD 123544.

2. Spong, R. N.: Stability Analysis of a Phase Correction Scheme in the Monitor and Control Equipment of a Phased Array Radar. Supplement to IEEE Trans. Aerospace and Electronic Systems, Vol. AES-3, pp. 236-248, Nov. 1967.

3. Johnson, M. A.: Phased-Array Beam Steering by Multiplex Sampling. Proc. IEEE. Vol. 56, No. 11, pp. 1801-1811, Nov. 1968.

4. Mailloux, R. J.; Caron, P. R.; and LaRussa, F. J.: An Array Phasing Device Which Uses Only One Phase Shifter for Each Direction of Scan. IEEE Trans. Antennas and Propagation, Vol. AP-16, No. 2, pp. 258-260, March 1968.

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