

1J86-TOPS-555  
1 August 1970

FACILITY FORM 602

1 N70-39509 (THRU)  
2 235 (PAGES)  
3 CR-13603 (NASA CR OR TMX OR AD NUMBER) (CODE)  
4 03 (CATEGORY)

POWER CONDITIONING  
EQUIPMENT  
FOR A THERMOELECTRIC  
OUTER PLANET SPACECRAFT



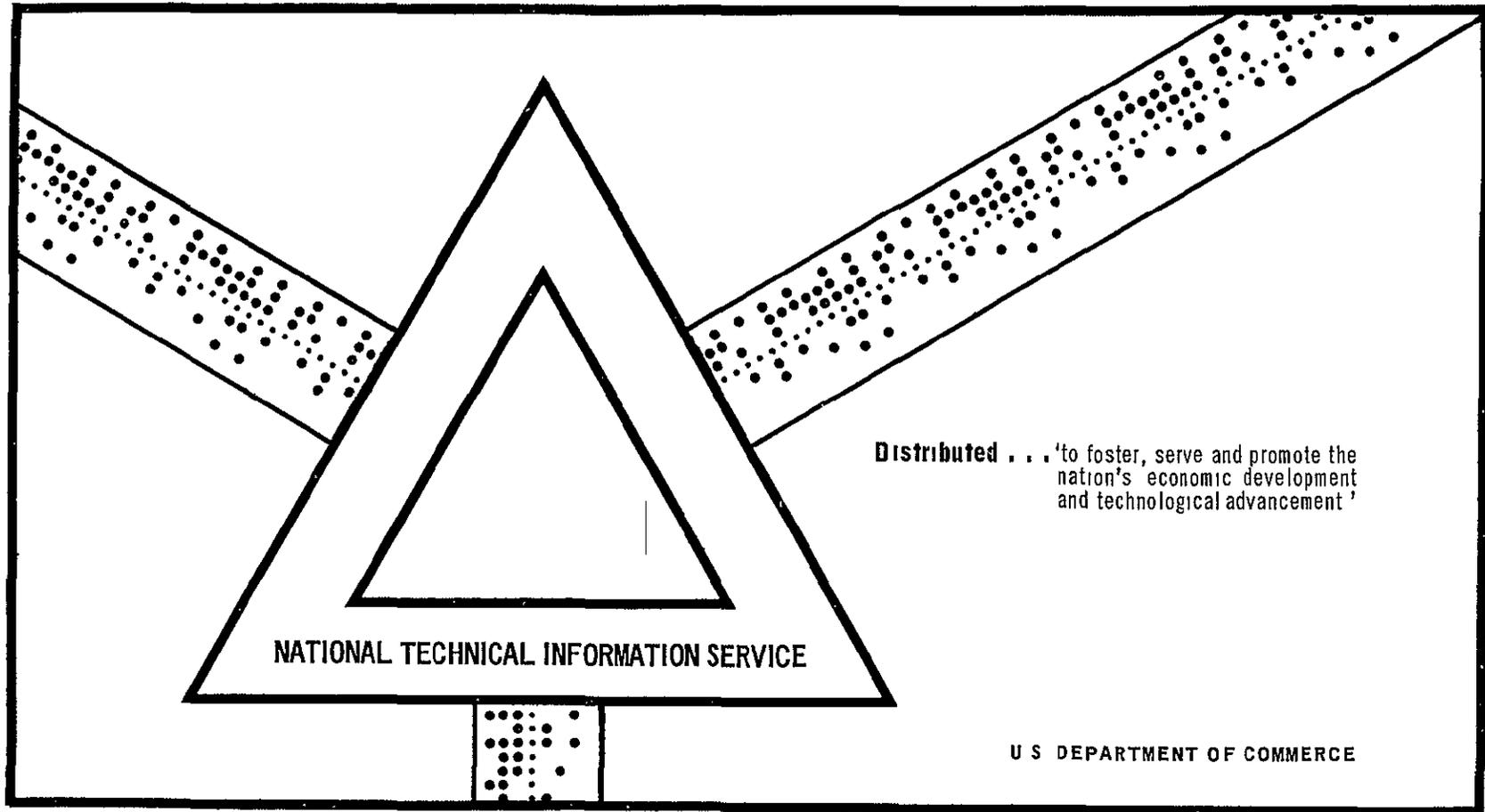
TECHNICAL REPORT  
FOR FIRST & SECOND QUARTERS, 1970  
JPL CONTRACT NO. 952536

Reproduced by  
NATIONAL TECHNICAL  
INFORMATION SERVICE  
Springfield, Va 22151

POWER CONDITIONING EQUIPMENT FOR A THERMOELECTRIC  
OUTER PLANET SPACECRAFT

General Electric

1 August 1970



1J86-TOPS-555  
1 August 1970

POWER CONDITIONING EQUIPMENT  
FOR A  
THERMOELECTRIC OUTER PLANET SPACECRAFT

TECHNICAL REPORT  
FOR FIRST & SECOND QUARTERS, 1970

JPL CONTRACT NO 952536

GENERAL ELECTRIC COMPANY  
VALLEY FORGE SPACE CENTER  
P O BOX 8555  
PHILADELPHIA, PENNSYLVANIA 19101

1J86-TOPS-555  
1 August 1970

POWER CONDITIONING EQUIPMENT  
FOR A  
THERMOELECTRIC OUTER PLANET SPACECRAFT  
TECHNICAL REPORT  
FOR FIRST & SECOND QUARTERS, 1970

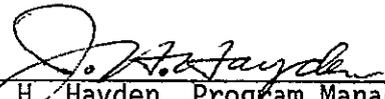
JPL CONTRACT NO 952536

"THIS WORK WAS PERFORMED FOR THE JET PROPULSION  
LABORATORY, CALIFORNIA INSTITUTE OF TECHNOLOGY, AS  
SPONSORED BY THE NATIONAL AERONAUTICS AND SPACE  
ADMINISTRATION UNDER CONTRACT NAS 7-100 "

Prepared by

R Andrews  
R Andryczyk  
S Capodici  
T Ebersole  
A Kirpich  
R Pellmann

Approved by

  
J. H. Hayden, Program Manager  
TOPS Power Conditioning Equipment

  
W. R. Becraft, Manager  
Electrical Subsystem Engineering

GENERAL ELECTRIC COMPANY  
VALLEY FORGE SPACE CENTER  
P O BOX 8555  
PHILADELPHIA, PENNSYLVANIA 19101

THIS REPORT CONTAINS INFORMATION PREPARED BY THE GENERAL  
ELECTRIC COMPANY UNDER JPL SUBCONTRACT ITS CONTENT IS NOT  
NECESSARILY ENDORSED BY THE JET PROPULSION LABORATORY,  
CALIFORNIA INSTITUTE OF TECHNOLOGY, OR THE NATIONAL  
AERONAUTICS AND SPACE ADMINISTRATION

ABSTRACT

This report covers activities performed from January through June, 1970 under JPL Contract No 952536. This contract pertains to the design and development of the electrical system and the Power Conditioning Equipment (PCE) for the Thermoelectric Outer Planet Spacecraft (TOPS) program.

During this reporting period, the system design was further developed taking the following into account:

- 1 Potential on-pad Radioisotope Thermoelectric Generator (RTG) limitations
- 2 Shunt dissipation alternatives
- 3 The configuration of the distribution and switching of power
- 4 The impact of test and checkout on the system design

Breadboard designs of various conditioning and switching elements are proceeding on schedule. As described in the body of this report, satisfactory test demonstrations have been completed on a number of these units.

CONTENTS

1 0 INTRODUCTION AND SUMMARY

2 0 STUDY APPROACH

3 0 PROGRAM STATUS

3 1 Power System Requirements

3 2 Subsystem Design

3 2 1 Electrical Configuration

3 2 2 Physical Configuration

3 2 3 Performance

3 2 4 Interfaces

3 2 5 Component Characteristics

3 2 6 Test and Operational Procedures

3 2 7 Reliability

3 3 Trade Studies

3 3 1 Power Source Studies

3 3 2 Power Regulation Studies

3 3 3 Distribution Studies

3 3 4 Switching Studies

3 4 Technology Development

3 4 1 Power Distribution Assembly

3 4 2 Shunt Regulator Assembly

3 4 3 Traveling Wave Tube Converter Assembly

3 4 4 Two-phase Inverter Assemblies

3 4 5 AC Power Conditioners

3 4 6 DC Power Conditioner Assemblies

3 4 7 Power Source and Logic Assembly

3 4 8 Subsystem Tests

3 4 9 Bench Test Equipment

4 0 CONCLUSIONS

5 0 NEW TECHNOLOGIES

6 0 REFERENCES AND BIBLIOGRAPHY

APPENDICES

- A TURN-ON TRANSIENT ANALYSIS
- B RADIATION EFFECTS
- C POWER SUBSYSTEM DESCRIPTION
- D POWER DISTRIBUTION ASSEMBLY
- E ENERGY STORAGE STUDY
- F TRANSFORMER OPTIMIZATION STUDY
- G OPERATIONAL PROCEDURES

LIST OF FIGURES

<u>Figure</u>		<u>Page</u>
2-1	Work Flow Diagram	2-2
3-1	Load Requirements Summary	3-5
3-2	Simplified Block Diagram	3-8
3-3	TOPS Power Subsystem Block Diagram	3-12
3-4	Component Designations	3-14
3-5	Power Margin Status	3-16
3-6	Signal Interface Diagram	3-21
3-7	Preliminary Component Characteristics	3-24
3-8	Subsystem Test Equipment Configuration	3-31
3-9	System Test Equipment Configuration	3-33
3-10	Pad Test/Launch Equipment Configuration	3-34
3-11	Reliability Summary	3-35
3-12	Block Diagram with Launch Battery	3-44
3-13	DC Distribution Concept	3-65
3-14	AC Distribution Concept	3-66
3-15	DC Distribution Variations	3-67
3-16	AC Distribution Variations	3-68
A-1	Allowable Power Loading	A-2
A-2	Allowable Power Unloading	A-2
A-3	Impedance Chart	A-3
A-4	Dynamic Impedance	A-4
A-5	Optimum Cable Resistance Per Foot	A-8
A-6	Fault Clearing Characteristics	A-8
A-7	Turn-On Current Transient	A-10
A-8	Inductor Response to a Voltage	A-12
A-9	Apparent Inductance	A-13
A-10	High Frequency Inductor Characteristics	A-15
A-11	Inductor Transformer Test Circuit	A-17
A-12	Turn-On Transient Current	A-17
A-13	Characteristic Weight of Tantalum Capacitors	A-19
A-14	Typical Inductor Characteristics	A-21
A-15	Optimized System Weight	A-22
A-16	TWT Converter Inrush Current	A-25
A-17	TWT Converter Delayed Current, Free Run	A-25
A-18	TWT Converter Delayed Current, clocked	A-25
A-19	TWT Converter Turn-On Relationships	A-26
B-1	Electrical Test Schematic	B-8
B-2	Typical Pretest Data, Sample #2	B-12
B-3	Typical Post Test Data, Sample #2	B-12
B-4	Radiation Effects on Leakage, Sample #1	B-14
B-5	Radiation Effects on Leakage, Sample #2	B-15
B-6	Radiation Effects on Leakage, Sample #3	B-16
B-7	Radiation Effects on Leakage, Sample #4	B-17

LIST OF FIGURES (CONTINUED)

<u>Figure</u>		<u>Page</u>
C-1	Redundancy Configurations From TOPS-3-250	C-4
C-2	Single Output Redundancy	C-5
C-3	Multiple Output Redundancy	C-5
C-4	Inverter or Converter Characteristics	C-7
C-5	Current Limited Redundancy Characteristics	C-8
C-6	Redundancy Configurations of TOPS-3-250	C-13
D-1	Solid State Switch Schematic	D-2
D-2	Electromechanical Relay Switch Schematic	D-3
D-3	Solid State Switch Turn-On Characteristics	D-4
D-4	Solid State Switch Turn-Off Characteristics	D-5
D-5	Relay Switch On/Off Characteristics	D-6
E-1	Typical Load Sequence at Planetary Encounter	E-3
E-2	Cell Failures Due to Separate Causes	E-12
E-3	Cumulative Cell Failure Rates	E-13
E-4	Reliability for 12 Year Mission	E-14
E-5	Reliability for 9 Year Mission	E-15
E-6	Reliability for 6 Year Mission	E-16
E-7	Reliability of Multiple Cell System	E-18
F-1	Transformer Physical Characteristics	F-2
F-2	Optimized Minimum Dissipation Supermalloy Transformers	F-3
F-3	Characteristics of Orthonal Toroidal Transformers	F-17
F-4	Characteristics of Supermalloy Toroidal Transformers	F-18
F-5	Characteristics of Silectron Cut Core Transformers	F-19
F-6	Characteristics of Supermalloy Cut Core Transformers	F-20
F-7	Locus of Orthonal Toroidal Transformers	F-21
F-8	Locus of Supermalloy Toroidal Transformers	F-22
F-9	Locus of Silectron Cut Core Transformers	F-23
F-10	Locus of Supermalloy Cut Core Transformers	F-24
F-11	Composite of Optimized 18 Watt Transformers	F-26
G-1	PCE Test Module Interface	G-4
G-2	PCE Flight Plug Interface	G-5
G-3	Subsystem Test Equipment Configuration	G-8
G-4	Shunt/Auxiliary Load Controller Test	G-11
G-5	Current Throttle Test	G-13
G-6	Series Regulator Test	G-15
G-7	Low Voltage Cut-Off Test	G-17

LIST OF TABLES

<u>Table</u>		<u>Page</u>
2-1	Task Descriptions	2-3
3-1	RTG Power Requirements	3-6
3-2	Baseline Selections	3-7
3-3	Physical Characteristics	3-15
3-4	RTG Power Margin	3-17
3-5	Performance Characteristics	3-19
3-6	Telemetry Data Points	3-22
3-7	Command Interface Definition	3-23
3-8	PCE Connector Identification	3-27
3-9	Comparison of Switching Devices	3-74
3-10	AC Power Conditioning Requirements	3-83
A-1	Hook-Up Wire Data	A-7
A-2	Minimum Weight Cable	A-10
A-3	Capacitor Characteristics	A-18
B-1	1763-1820 Electrical Characteristics	B-11
B-2	Sample #2 Annealing Study	B-19
C-1	Load Redundancy	C-2
C-2	Failure Criteria	C-10
F-1	Formulae	F-4
F-2	Transformer Analysis Printout	F-6
F-3	Transformer Analysis Program	F-9

GLOSSARY

		<u>Page</u>
Amperes Per Square Inch	ASI	F-1
Central Computer Subsystem	CCS	3-2
Flight Command Subsystem	FCS	3-9
Ground Power Unit	GPU	G-4
Low Voltage Cut Off	LVCO	3-9
Multi-Hundred Watt	MHW	3-13
Operational Support Equipment	OSE	3-25
Power Conditioning Equipment	PCE	111
Radioisotope Thermoelectric Generator	RTG	111
Shunt Resistor Panel	SRP	3-11
Thermoelectric Outer Planet Spacecraft	TOPS	111
Traveling Wave Tube	TWT	3-18

SECTION 1 INTRODUCTION AND SUMMARY

This report covers activities performed under JPL Contract No 952536 for the period 1 January 1970 through 30 June 1970

The effort of this contract is directed at designing and developing the PCE for the TOPS concept. The function of this equipment is to receive power from RTG power sources and to condition, distribute and control this power for the spacecraft loads. The TOPS mission, aimed at a tour of the outer planets, will operate for an estimated 12 year period. Unique design characteristics required for the power conditioning equipment result from the long mission time and the need for autonomous on-board operations due to large communications distances and the associated time delays of ground initiated actions.

The TOPS program was specifically initiated as a means for evaluating the status of various subsystem technologies for extended outer planet missions. This particular power conditioning equipment contract is being conducted within this context. Near term objectives are to develop subsystem concepts, conduct trade studies, and identify and proceed with necessary technology developments. Specific trade studies are concerned with the use of AC or DC distributed power, the need for batteries, and the selection of bus configurations which yield a high probability of mission success. Technology developments pertain principally to techniques for increasing the life of power equipment and devices. These include examinations of such items as circuit redundancy and the possible replacement of life limited mechanical relays by solid state switching circuits.

Long-term goals will be aimed at designing, building and testing power conditioning equipment against detailed design requirements resulting from the near-term studies and integration with the overall TOPS concept

The principal accomplishments during this period are as follows

- A distribution concept has been developed which assures that power will be available to the Central Computer System in the event of a load or source fault
- Evaluation of alternative shunt regulation schemes has resulted in the selection of a two-step sequenced shunt for each RTG. Each shunt regulator operates independently, avoiding interface complexity
- Launch batteries to augment limited on-pad RTG capability were evaluated. As a result of the complexity introduced, their use is discouraged
- Emphasis has been placed on AC distribution as a result of a JPL project decision
- Present weight estimates for the power conditioning equipment are as follows
  - PCE within power system - 40 lbs
  - PCE in other subsystems - 81.5 lbs
- A converter for the TWT was completed and successfully tested

- Three DC to DC converters used for representative spacecraft loads (Tracking Receiver, DC Magnetometer, and Science Data Subsystem) were built and tested to demonstrate synchronous operation from a central clock signal with backup free-run capability
- Gyro and wheel two-phase inverters were redesigned and tested
- A current monitor and low voltage cutoff circuits were developed
- A breadboard subsystem consisting of the following was successfully tested and delivered
  - 1 - 270 watt shunt regulator
  - 1 - 400 Hz momentum wheel inverter
  - 1 - 1600 Hz gyro inverter
  - 1 - Quad redundant solid state switch
  - 1 - Quad redundant relay switch
  - 3 - DC to DC converters
  - 1 - TWT converter
  - 1 - Low voltage cut-off circuit
  - 1 - Current monitor

A separate report will be issued covering the breadboard subsystem tests

SECTION 3 PROGRAM STATUS

This section reports on each of the task items listed in Table 2-1

3.1 Power System Requirements (Task 1.0)

Design guidelines for the TOPS Power Conditioning Equipment have been developing in conjunction with overall system design guidelines for the TOPS mission. The guidelines noted below are general in nature and are identical to those presented in the previous quarterly report.

- Power source - 4 RTG's, each rated at 156 watts at beginning of mission and 118 watts at end of mission
- Life - 12 years
- No batteries to be used unless higher reliability and/or mission advantages can be demonstrated
- Reliability shall be a strong factor in the PCE design, and shall be achieved through judicious part selection, use of redundancy, etc. No single component failure shall cause catastrophic failure of the PCE. No failure in the power source shall impair operation of the PCE. Additionally, redundant power supplies shall be used for all mission critical subsystems.
- On/off switching shall be provided for all non-mission critical subsystems.

- All power on/off switches and all primary/standby unit switches shall be commandable by both a primary source in the Central Computer Subsystem (CCS) and a backup source by ground command through the flight command subsystem
- Telemetry points shall be incorporated in the PCE to provide the CCS with information on the performance of the PCE, so that in the event of PCE failures the CCS can take corrective action (switch to a standby unit, remove a faulted load from the bus, etc )
- Some capability will exist in the PCE to detect faulted loads or PCE failures, and to remove faulted loads or switch to standby PCE units in the event that the CCS is unable to perform these functions
- Short circuit protection in the form of circuit breakers that may be reset by CCS or ground command shall be provided for bus protection at the front end of PCE power supplies
  - a As a series element for all subsystems which are not mission critical,
  - b Where necessary to insure that a secondary mode of operation is obtainable by either on-board logic or ground command in the event of a failure in an element of the primary mode
- Circuitry shall be provided to minimize power switching transients and to limit current in the event of a load or power supply fault

- Non-toggle switching shall be used so that knowledge of switch status is not required and so that multiple commands can be sent
- Main inverters and DC to DC converters shall be capable of free-running should the sync signal be lost
- Weight and volume of the PCE shall be minimized
- Power efficiency of the PCE, including inverters, converters, switches, etc , shall be maximized
- Power consumption by the power switching control circuitry shall be minimized
- Immunity to spurious switch operation shall be provided
- The type approval temperature range shall be  $-20^{\circ}\text{C}$  to  $+80^{\circ}\text{C}$  as measured at the shear plate of the power bay
- The regulation of the shunt regulator shall be traded off against the required regulation of the power supplies, and an optimization in terms of efficiency shall be reached
- The nominal frequency of the two phase gyro inverter shall be between 1584 Hz and 1616 Hz The frequency tolerance of this inverter shall be  $\pm 0.01\%$  The frequency of the two phase momentum wheel inverter shall be  $400 \pm 5\%$  Hz

- If an AC distribution system is used, the frequency tolerance shall be +5%
- Load requirements as a function of mission phase are summarized on Figure 3-1. This is based on the detailed load information shown on Table 3-1 which was supplied by JPL.

### 3 2 Subsystem Design (Task 2 0)

A decision has been reached by JPL that the principal form of distributed power will be AC. Accordingly the power system concept has been modified to incorporate this requirement. Baseline selections for the system are summarized in Table 3-2. Overall electrical, physical, and interface characteristics of the present concept are described below. The justification for particular system selections is provided under paragraph 3 3, Trade Studies.

#### 3 2 1 Electrical Configuration

A simplified block diagram of the system is shown on Figure 3-2. Four RTG's are used, estimated to provide an initial output of 624 watts (156 watts each) and a conservative end of life power (after about 12 years) of 472 watts (118 watts each). The RTG outputs are combined through isolation diodes to provide a regulated 30 VDC bus. Regulation is accomplished by separate shunt regulators at each RTG. Each shunt regulator dissipates excess power by a two-stage sequence operation of transistor-resistor sections. As described in paragraph 3 3 2 this type of shunt regulator was selected because of low dissipation of the transistor elements and minimum interface complexity.

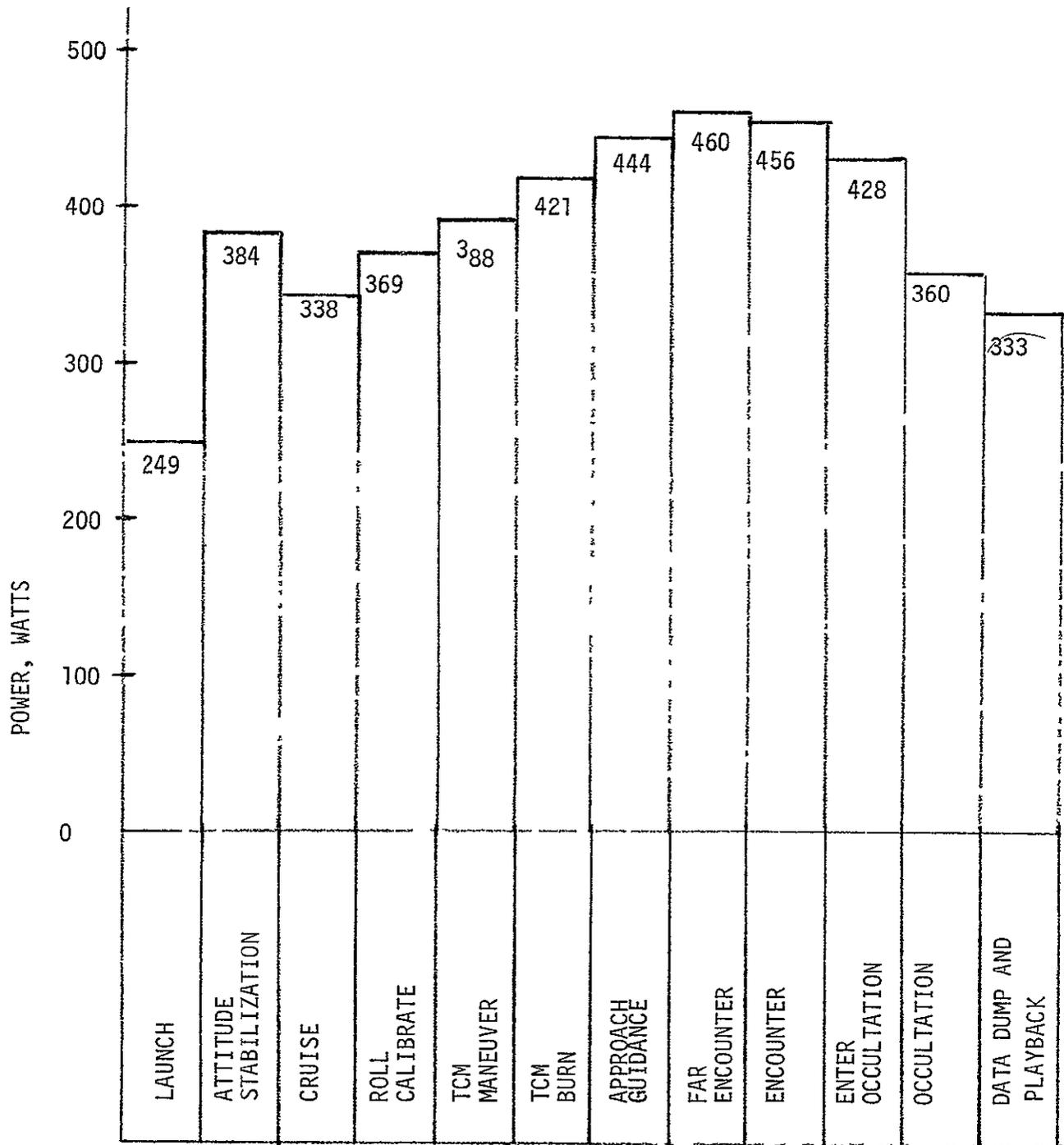


FIGURE 3-1

LOAD REQUIREMENTS SUMMARY

TABLE 3-1 RTG POWER REQUIREMENTS BY MISSION PHASE  
(each load includes T/R and Main Inverter losses)

Load	Launch	Attitude Stabilization	Cruise	Roll Calibrate	TCM Maneuver	TCM Burn	Approach Guidance	Far Encounter	Encounter	Enter Occultation	Occultation	Data Dump and Playback
Command Receiver	7 7	7 7	15 4	7 7	7 7	7 7	7 7	7 7	7 7	7 7	7 7	7 7
Tracking Receiver	---	---	---	---	---	---	---	12 2	12 2	12 2	---	12 2
RFS Preamp	2 5	2 5	5 0	2 5	2 5	2 5	2 5	2 5	2 5	2 5	2 5	2 5
RFS Control Unit	3 1	3 1	3 1	3 1	3 1	3 1	3 1	3 1	3 1	3 1	3 1	3 1
S-Band Exciter	2 8	2 8	2 8	---	---	---	2 8	---	---	2 8	2 8	---
X-Band Exciter	---	---	---	6 8	6 8	6 8	---	6 8	6 8	6 8	---	6 8
S-Band Power Amplifier	51 1	51 1	51 1	---	---	---	51 1	---	---	51 1	51 1	---
X-Band Power Amplifier	---	---	---	62 2	62 2	62 2	---	62 2	62 2	62 2	---	62 2
RFS Telemetry	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0
Control Computer	50 0	50 0	50 0	50 0	50 0	50 0	50 0	50 0	50 0	50 0	50 0	50 0
Measurement Processor	12 0	12 0	12 0	12 0	12 0	12 0	24 3	24 3	24 3	12 0	12 0	12 0
Data Storage	44 9	44 9	44 9	44 9	44 9	44 9	44 9	44 9	44 9	44 9	44 9	44 9
Timing Synchronizer	0 5	0 5	0 5	0 5	0 5	0 5	0 5	0 5	0 5	0 5	0 5	0 5
Flight Command	6 4	6 4	6 4	6 4	6 4	6 4	6 4	6 4	6 4	6 4	6 4	6 4
Attitude Control Electronics	---	11 2	11 2	11 2	11 2	11 2	11 2	11 2	11 2	11 2	11 2	11 2
Attitude Propulsion Thrusters	---	38 4	19 2	---	---	---	19 2	19 2	---	19 2	19 2	---
Gyro Heaters	7 2	7 2	---	7 2	7 2	7 2	7 2	7 2	7 2	7 2	7 2	---
Gyro Electronics	9 8	9 8	---	9 8	9 8	9 8	9 8	9 8	9 8	9 8	9 8	---
Gyro Spin Motor	12 3	12 3	---	24 0	24 0	12 3	24 0	12 3	12 3	12 3	12 3	---
Reaction Wheels	---	12 9	12 9	12 9	25 8	---	12 9	12 9	12 9	12 9	12 9	12 9
Accelerometer	---	---	---	---	---	2 0	---	---	---	---	---	---
Cruise Sun Sensors	---	3 0	3 0	3 0	3 0	3 0	3 0	3 0	3 0	3 0	3 0	3 0
Acquisition Sun Sensors/Sun Gate	---	0 5	0 5	0 5	0 5	0 5	0 5	0 5	0 5	0 5	0 5	0 5
Canopus Sensor	---	5 5	5 5	5 5	5 5	5 5	5 5	5 5	5 5	5 5	5 5	5 5
Sun Shutter	---	7 2	7 2	7 2	7 2	7 2	7 2	7 2	7 2	7 2	7 2	7 2
Autopilot Electronics	2 6	---	---	---	---	2 6	---	---	---	---	---	---
Motor Gimbal Actuators	20 1	---	---	---	---	55 8	---	---	---	---	---	---
Science Scan Electronics	---	---	---	2 5	---	---	2 5	2 5	2 5	2 5	2 5	---
Science Scan Actuators	---	---	---	2 4	---	---	2 4	2 4	2 4	2 4	2 4	---
AGSS Platform Electronics	---	---	---	---	---	---	2 5	2 5	---	---	---	---
AGSS Platform Actuators	---	---	---	---	---	---	2 4	2 4	---	---	---	---
M G A Pointing Electronics	---	---	1 3	1 3	1 3	---	---	---	---	---	---	---
M G A Pointing Actuators	---	---	1 2	1 2	1 2	---	---	---	---	---	---	---
Pyrotechnic Control Unit	---	10 0	---	---	10 0	---	---	---	---	---	---	---
Engine Solenoids	---	---	---	---	---	21 4	---	---	---	---	---	---
Temperature Control	---	25 5	25 5	25 5	25 5	25 5	25 5	25 5	11 3	25 5	25 5	25 5
Approach Guidance Sensor	---	---	---	---	---	17 5	17 5	---	---	---	---	---
Vector Helium Magnetometer	---	4 6	4 6	4 6	4 6	4 6	4 6	4 6	4 6	4 6	4 6	4 6
Plasma Wave Detector	---	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2
Trapped Radiation Detector	---	1 3	1 3	1 3	1 3	1 3	1 3	1 3	1 3	1 3	1 3	1 3
Trapped Radiation Instrument	---	5 6	5 6	5 6	5 6	5 6	5 6	5 6	5 6	5 6	5 6	5 6
Micrometeoroid Detector	---	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1	1 1
Meteoroid-Asteroid Detector	---	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2
Plasma Probe	---	14 0	14 0	14 0	14 0	14 0	14 0	14 0	14 0	14 0	14 0	14 0
Charged Particle Telescope	---	4 5	4 5	4 5	4 5	4 5	4 5	4 5	4 5	4 5	4 5	4 5
Radio Emission Detector	---	3 3	3 3	3 3	3 3	3 3	3 3	3 3	3 3	3 3	3 3	3 3
Ultraviolet Photometer	---	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2
Infrared Multiple Radiometer	---	---	---	---	---	---	---	8 9	---	---	---	---
IMR Cooler	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2	2 2
Television A (Wide Angle)	---	---	---	---	---	---	---	28 4	---	---	---	---
Television B (Narrow Angle)	---	---	---	---	---	---	36 0	36 0	---	---	---	---
Power Telemetry	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0	1 0
Power Switching & Logic	4 8	4 8	4 8	4 8	4 8	4 8	4 8	4 8	4 8	4 8	4 8	4 8
TOTAL	242 0	373 0	328 7	360 3	378 3	410 1	432 8	448 4	443 9	416 9	350 2	324 1
DIODE LOSS (0 8V)	6 5	10 0	8 8	9 1	10 1	11 0	11 5	12 0	11 8	11 1	9 8	8 7
RTG TOTAL	248 5	383 6	337 5	369 4	388 4	421 1	444 3	460 4	455 7	428 0	360 0	332 8

Table 3-2

B A S E L I N E   S E L E C T I O N S

<u>FUNCTION</u>	<u>SELECTION</u>	<u>REASON</u>
Power Source	RTG's	Sun distance
Regulation	Shunt regulators	Maintain load on RTG's to limit temperatures
Distribution	a) 30 VDC to inverters, TWT converter & heater loads	a) Voltage established by RTG
	b) 50 VAC, 4096 Hz, square wave for distribution to load T/R's	b) Frequency is within minimum weight range
Protection	a) Redundant busses to CCS and power control circuitry	a) Assure fault removal capability
	b) Low voltage cutoff circuit	b) Backup to CCS corrective procedures

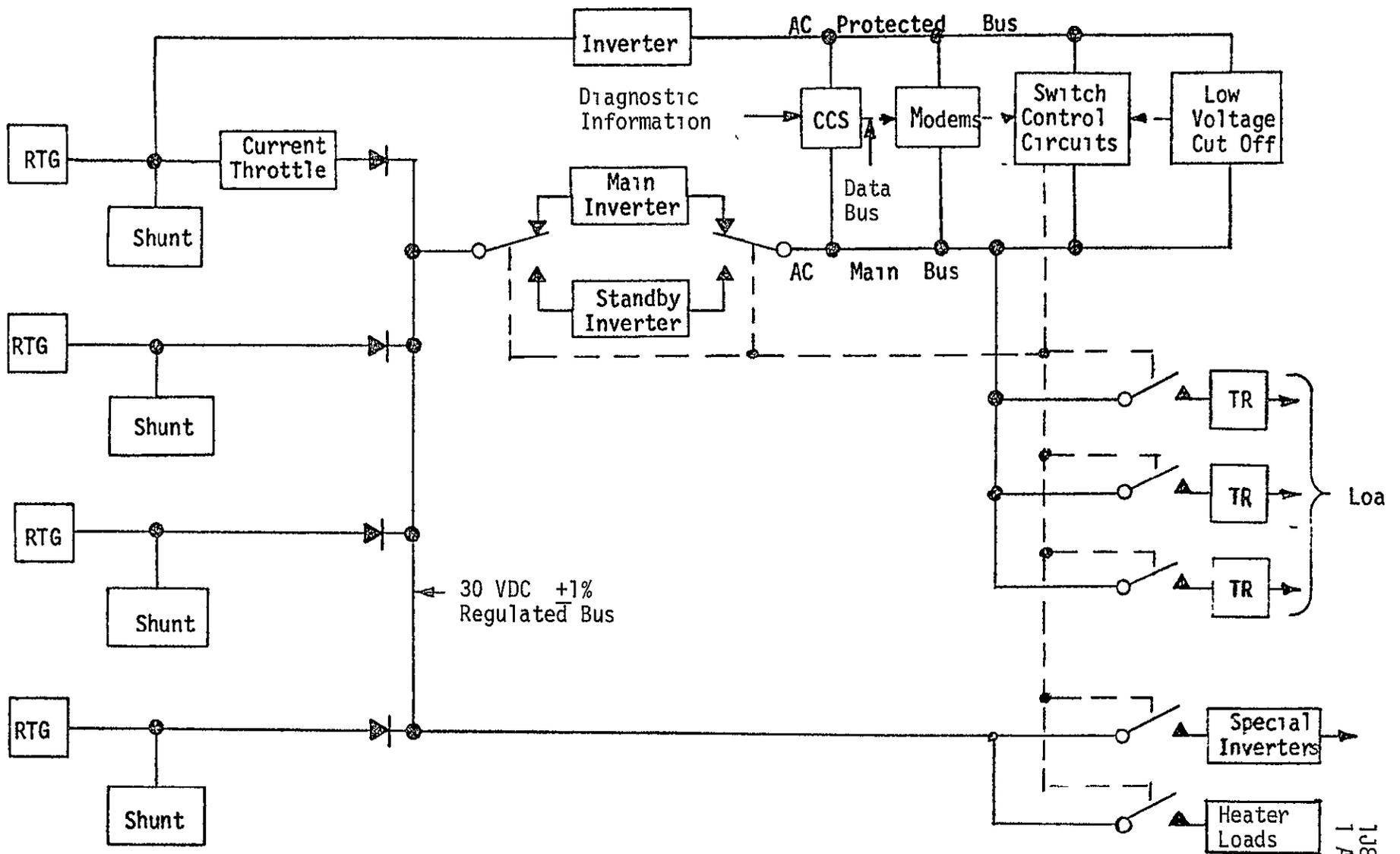


FIGURE 3-2

SIMPLIFIED BLOCK DIAGRAM

The 30 VDC power is supplied to a main inverter with standby redundancy for generating AC power. This is the power used for general distribution. The 30 VDC power is also supplied directly to the attitude control two-phase inverters, TWT converters, and heater loads.

An additional AC bus distributes power from RTG No. 1. This protected bus serves as a redundant source of power to the CCS and associated power control functions. Should power on the main AC bus fail due to load or power system equipment faults, the AC protected bus would provide the power required for diagnosis and corrective action by the CCS. The Current Throttle shown in the output line of RTG No. 1 has the function of maintaining required voltage levels on the AC protected bus. If a fault occurs on the main bus with a consequent drop in voltage, the Current Throttle would respond by increasing its series impedance such that its input voltage would be held constant. In this way the protected bus voltage would be maintained.

Control of power switches is accomplished through circuits which receive actuation signals from the CCS, the Flight Command Subsystem (FCS) or the Low Voltage Cutoff (LVCO). The CCS and FCS relay their signals in digital form through data bus channels and the modulation-demodulation (modem) units shown.

Two independent methods are used to rectify fault conditions:

1. CCS Fault Correction - the state of the power system is determined by CCS in response to diagnostic information (currents, voltages, switch states, etc.). Through interpretive subroutines CCS determines

the existence and location of faults, overload conditions or other abnormalities and determines where and how corrective measures should be applied. Such corrective actions will generally involve switch actuations for load removal or the transfer from main to standby units as shown in the case of the main DC/AC inversion chain. It is estimated that 30 milliseconds maximum would elapse from the onset of a fault condition until total corrective action took place.

- 2 LVCO Fault Correction - This method serves as a backup to the CCS method by initiating preprogrammed corrective actions. The existence of a voltage less than 27 VDC at the output of the RTG diodes for 100 milliseconds or greater is used as the criterion for initiating the corrective actions. Tentatively these actions would be
  - a Interrupt power to all non-essential loads.
  - b Transfer power from main to standby elements within critical load categories.
  - c Transfer from main to standby power conditioning elements.

The above actions may be carried out concurrently or sequentially, a factor which may be more appropriately resolved during system development tests.

Figure 3-4 shows the physical breakdown of assemblies comprising the power system. Size, weight and heat burden estimates for the PCE, SRP and other conditioning elements are shown in Table 3-3.

### 3.2.3 Performance

Power margin status is summarized on Figure 3-5. The load profile shown contains allowances for conditioning and diode losses and therefore represents the power demand at the RTG terminals. The RTG characteristic curve is based on data supplied by GE's Isotope Power System Operation in connection with the Multi-Hundred Watt (MHW) RTG program. The resulting RTG margins for different planetary encounters are expressed in absolute power and percent.

Analysis of steady state ripple in Appendix A indicates that filter designs which provide minimum system weight result in currents which may be 4 percent higher than that indicated by steady state loads.

Thus the RTG power should be at least 4 percent higher than the indicated demand. As shown on Figure 3-5 the presently defined loads and RTG performance estimates indicate less than 4 percent margin for the last encounter. Since the RTG performance is of a preliminary nature this margin deficiency cannot be fully evaluated at this time other than to bring attention to this potential problem. Solutions may lie in increasing the RTG capability or possibly in accepting degraded mission performance by removing certain less essential loads.

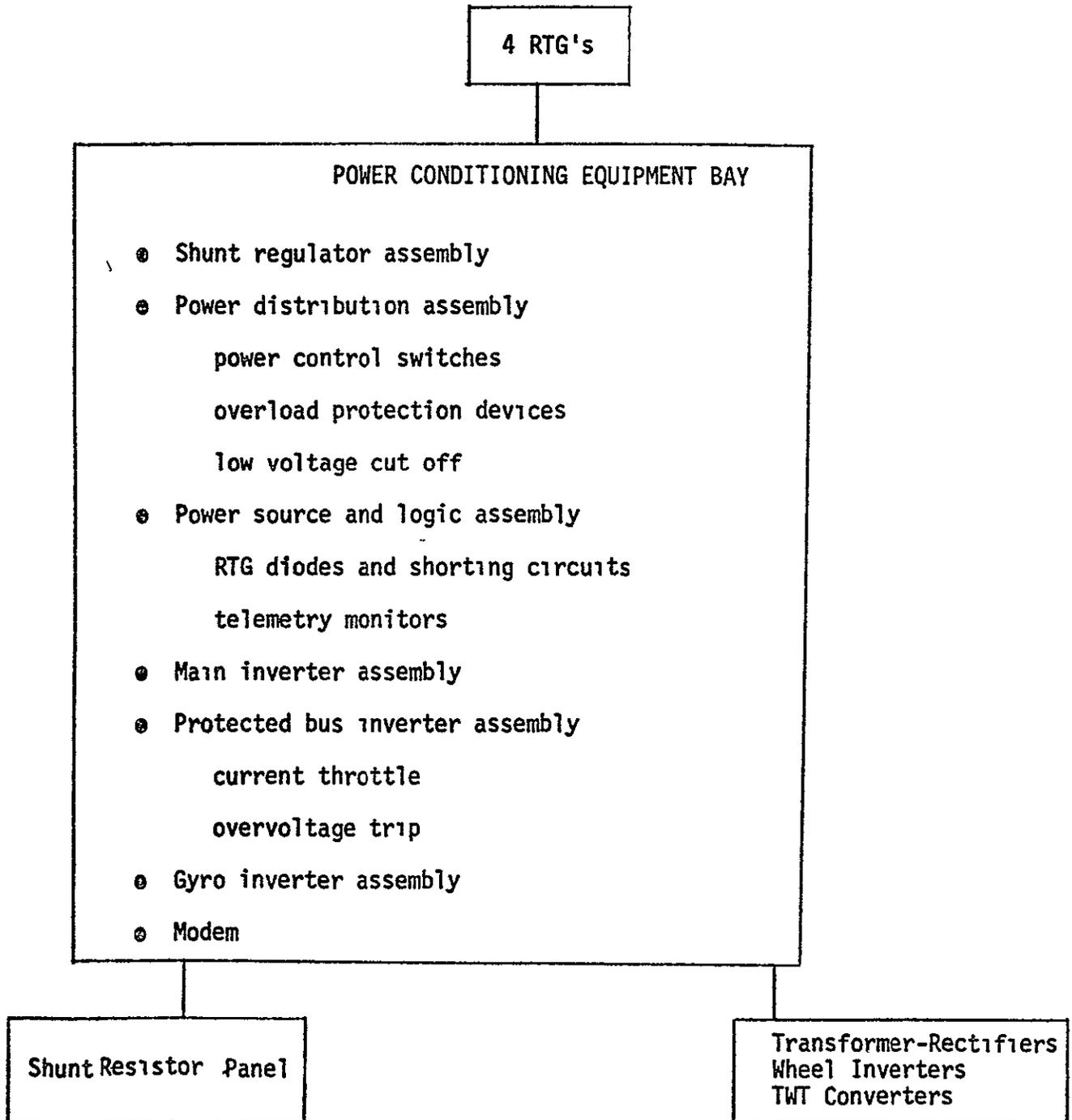


FIGURE 3-4

COMPONENT DESIGNATIONS

Table 3-3

P H Y S I C A L   C H A R A C T E R I S T I C S

ASSEMBLY	SIZE, CUBIC INCHES	WEIGHT, POUNDS	HEAT BURDEN, WATTS
SHUNT REGULATOR ASSEMBLY	220	3 5	50 0
POWER DISTRIBUTION ASSEMBLY			
SOLID STATE (80)	320	12 0	30 0
RELAY (80)	(320)	(12 0)	(00 0)
POWER SOURCE AND LOGIC ASSEMBLY	170	3 5	17 0
MAIN INVERTER ASSEMBLY (2)	220	10.0	40 0
PROTECTED BUS INVERTER ASSEMBLY	40	2 0	10 0
GYRO INVERTER ASSEMBLY (2)	140	3 5	1 0
MODEM	---	---	---
CHASSIS, WIRING	220	5.5—	---
PCE SUBTOTAL	1310 (1310)	40 0 (40 0)	148 (118)
SHUNT RESISTOR PANEL	650	4 5	310 0
WHEEL INVERTERS (6)	360	9 0	0 5
TWT CONVERTERS (5)	500	18 0	26 0
TRANSFORMER-RECTIFIERS (40)	2000	50 0	80 0
EXTERNAL SUBTOTAL	3510	81 5	416 5

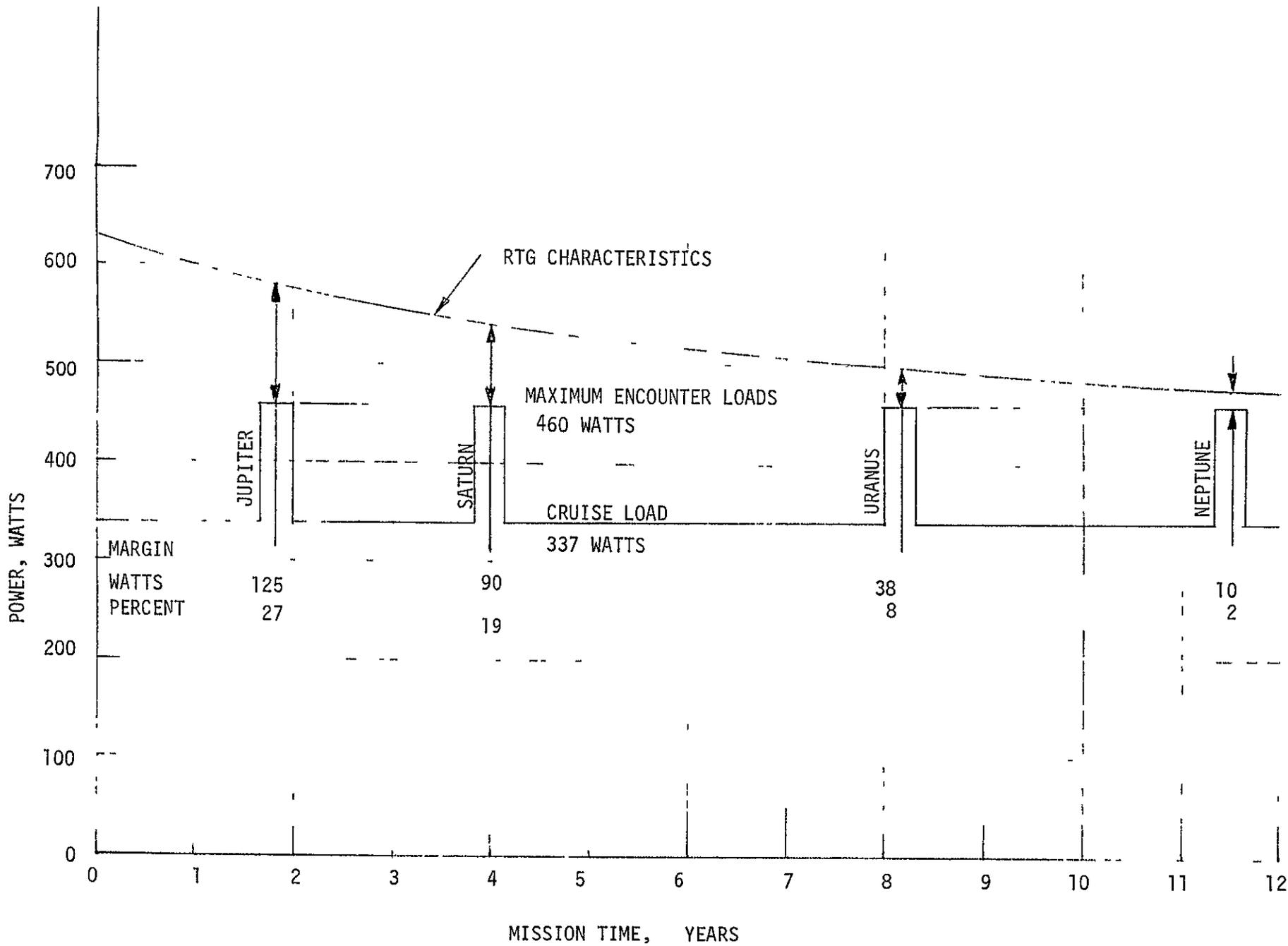


FIGURE 3-5

POWER MARGIN STATUS

In general the notion of degraded mission modes must be considered for the case where one or more RTG's fail to produce power. The RTG's are arranged to permit such failures without endangering the remaining RTG's through the use of isolation diodes and modularized shunt regulators. The mission worth under such degraded power conditions has not been evaluated as part of this study since such an evaluation can be more suitably performed as an aspect of overall system performance. As an aid in considering degraded power operations, Table 3-4 indicates power margin at various encounter phases considering the loss of up to two of the four RTG's.

TABLE 3-4 RTG POWER MARGIN, WATTS

Number of Operable RTG's	Encounter Phase			
	Jupiter	Saturn	Uranus	Neptune
4 out of 4	125	90	38	10
3 out of 4	-20	-48	-86	-108
2 out of 4	-168	-185	-211	-225

A cursory review of the loads shown in Table 3-1 provides a measure of the practicality of degraded power operation. With the failure of one RTG at the Jupiter encounter, for example, the 20 watt deficiency indicated on Table 3-4 could possibly be compensated by reducing heater power or removing several of the less significant science loads for the "Far Encounter" phase. Time sharing of certain loads may provide alternative solutions. For later encounters or larger RTG losses, severe changes in operation would appear necessary.

Another factor affected by power margin concerns the system response to step load changes. A section of Appendix E considers response to the turn-on of the traveling wave tube (TWT) which probably represents the largest load increment in the spacecraft system. As presently designed the TWT could incur significant voltage transients (to 50% of nominal regulation) for periods lasting 20 to 30 milliseconds. Avoidance of this transient by increased margin does not appear practical since the inrush current is on the order of 4 to 5 times larger than steady state values. It is believed that this transient could adversely affect the overall system, possibly to the extent of causing false indication of failure which could initiate certain corrective sequences within the CCS or Low Voltage Cutoff (LVCO). Further study of this problem is necessary which may involve changes in the TWT circuitry, revisions in the general approach for sensing faults and initiating corrective action, or combinations of such changes.

Electrical performance of the system is summarized on Table 3-5.

### 3 2 4 Interfaces

Preliminary interface definition is defined below.

#### A Telemetry

The general concept for handling measurement data for telemetry purposes will be to condition all signals to a 0 to 5 volt analog signal corresponding to the measurement range. Signal source impedance will be 5000 ohms or less. Depending on the number of measurements, it is possible that they will be multiplexed and

TABLE 3-5

PERFORMANCE CHARACTERISTICS

AC MAIN BUS

- 50 VAC, RMS,  $\pm 3\%$ , Square wave, single phase
- Rise Time 1 microsecond nominal
- Frequency 4096 Hz  $\pm 1\%$ , (Synchronized)  
4096 Hz +0, -10% (Free run)

AC PROTECTED BUS

- 50 VAC, RMS,  $\pm 8\%$ , Square wave, single phase
- Rise Time 1 microsecond nominal
- Frequency 4096 Hz  $\pm 01\%$ , (Synchronized),  
4096 Hz +0, -10% (Free Run)
- Rated Power 100 watts

DC MAIN BUS

- 30 VDC  $\pm 1\%$
- Ripple 300 MV Peak to Peak
- Transient Response to 100 watt step load  
30 MV excursion,  
100  $\mu$ sec duration

- Dynamic impedance less than 100 milliohms

DC PROTECTED BUS

- 30 to 32.8 VDC
- Ripple 300 MV peak to peak
- Power 110 watts end of life
- Dynamic impedance less than 500 milliohms

SWITCHING CHARACTERISTICS

	<u>Solid State</u>	<u>Relay</u>
1 ON/OFF TIME, MILLISECONDS	2 to 10	2 to 10
2 BOUNCE TIME, MILLISECONDS	0	2 to 10
3 FORWARD DROP	1.8 V	0.50V
4 LEAKAGE CURRENT	100 MICROAMPERES	0
5 RAMP TIME	20 $\mu$ S to 100 $\mu$ S	NOT AVAILABLE
6 OVERLOAD TRIP	120%	120%
7 TRIP TIME, MILLISECONDS	0.3 to 2.5	0.3 to 2.5

transmitted from the subsystem through a single coax cable as shown in Figure 3-6. This approach would also be used to route signals to and from the CCS and FCS. If this concept is adopted, the required multiplexing and modulation/demodulation equipment would be supplied for inclusion in the PCE equipment bay. Table 3-6 is a preliminary breakdown of telemetry measurements.

B Command

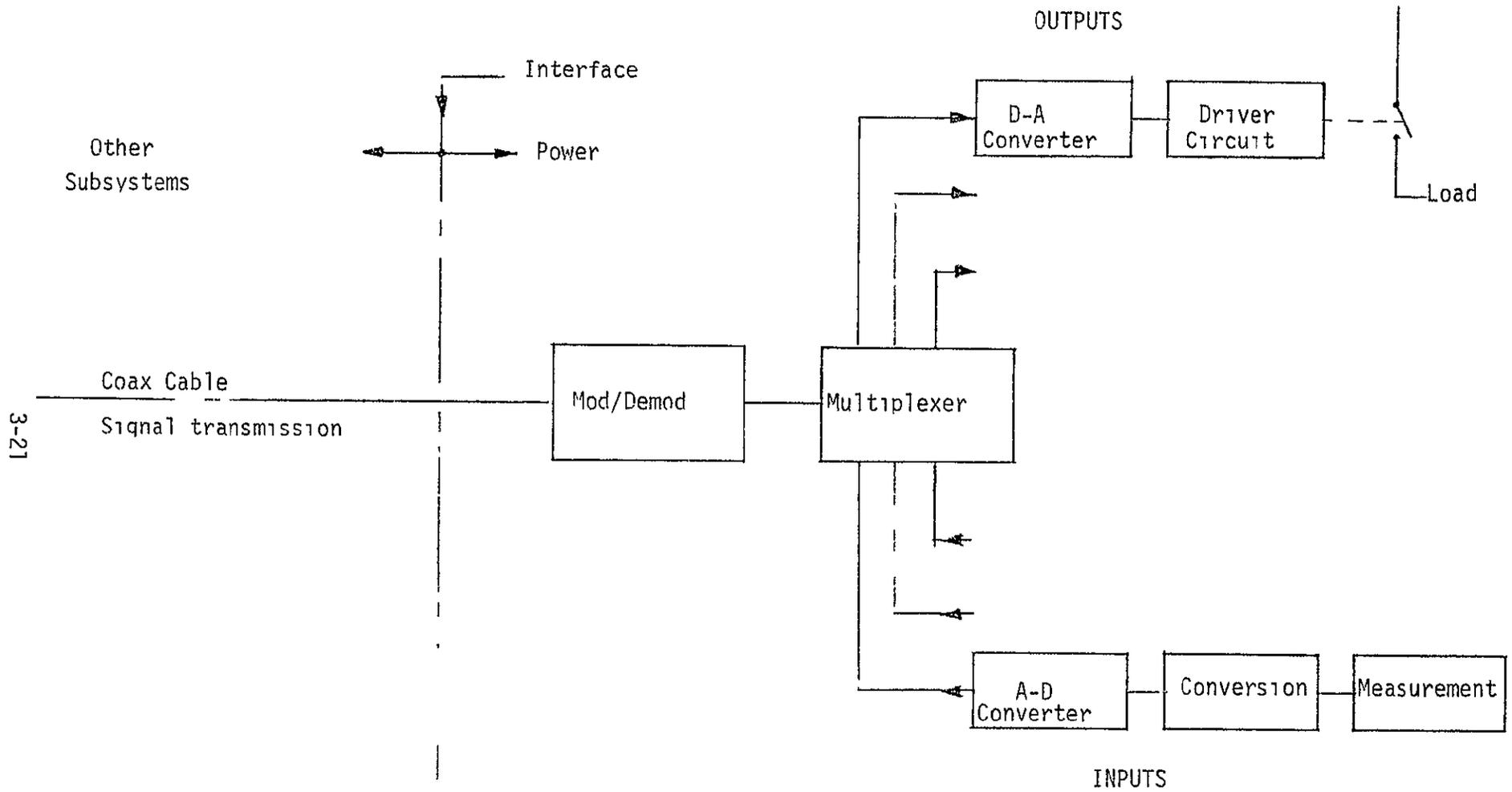
A preliminary breakdown of command requirements is shown on Table 3-7.

C CCS

Generally the CCS interaction with the power system will be to control the power applied to the various loads. This control will depend on the particular mission sequence and the power margin status. As long as sufficient margin is available, operations can proceed according to planned sequences. If margins are insufficient, the CCS, through stored instructions, withholds power according to some priority criterion. As presently visualized, status information for margin determination will be multiplexed and distributed in a manner similar to the telemetry information.

3.2.5 Component Characteristics

Preliminary characteristics for the components designated in Figure 3-4 are described in Figure 3-7.



3-21

FIGURE 3-6 SIGNAL INTERFACE DIAGRAM

TABLE 3-6

TELEMETRY DATA POINTS

<u>MEASUREMENT</u>	<u>RANGE</u>	<u>QUANTITY</u>
PCE INPUT VOLTAGE	0-60 VDC	4
PCE INPUT CURRENT	0-10 AMP	4
SHUNT REGULATOR CURRENT	0-5 AMP	4
DC MAIN BUS VOLTAGE	25-35 VDC	1
DC MAIN BUS CURRENT	0-40 AMP	1
AC MAIN BUS VOLTAGE	40-60 VAC	1
AC MAIN BUS CURRENT	0-24 AMP	1
DC PROTECTED BUS VOLTAGE	25-35 VDC	1
DC PROTECTED BUS CURRENT	0-5 AMP	1
AC PROTECTED BUS VOLTAGE	40-60 VAC	1
AC PROTECTED BUS CURRENT	0-3 AMP	1
RTG TEMPERATURE	~ - - -	<u>4</u>
	TOTAL	24

### 3 2 6 Test and Operations Procedures

The TOPS Power Conditioning Equipment must be designed such that it can be tested at all levels of spacecraft assembly. The prime object of this effort is to identify design requirements peculiar to testing which effect the PCE design.

#### 3 2 6 1 PCE Interfaces

In order to formulate test procedures, it was helpful to first identify all the interface functions of the PCE, and to assign these functions to specific connectors. In so doing, it was possible to configure cabling diagrams and identify functions which must be simulated by Operational Support Equipment (OSE) at the different test levels. The assumptions used in defining the PCE connectors were:

- A Miniature, lightweight, high density, rectangular connectors would be used.
- B AWG #28 gauge wire would be used except for the connections from the RTG's to the PCE.
- C The operating current in the #28 wire would be 112 milliamperes in order to maximize the power subsystem from a weight standpoint.

A total of twelve (12) connectors are required to handle all the PCE functions. They are as follows:

- J1 - RTG #1 & #2 input power
- J2 - RTG #3 & #4 input power
- J3 - Flight/Test plug
- J4 - Test/Umbilical
- J5 - RTG temperature sensors
- J6 - FCS coaxial cable
- J7 - CCS coaxial cable
- J8 - User subsystem loads
- J9 - User subsystem loads
- J10 - User subsystem loads
- J11 - User subsystem loads
- J12 - User subsystem loads

The detailed description of each connector is shown in Table 3-8

### 3 2 6 2 Test Configurations

Three levels of testing were studied to determine test ability

The first is the PCE subsystem test where all the major circuits of the PCE are assembled and interconnected for the first time

The next level is the spacecraft system integration and test. This is the first time the PCE is interfaced to the TOPS flight hardware

Last, the pad test/launch support phase was analyzed

TABLE 3-8

P C E. CONNECTOR IDENTIFICATION

J1 INPUT POWER CONNECTOR (AWG #20)

			<u>Number of Wires</u>
RTG #1	SUPPLY	(5 amps)	7
RTG #1	RETURN		7
RTG #2	SUPPLY	(5 amps)	7
RTG #2	RETURN		<u>7</u>
TOTAL			28

J2 INPUT POWER CONNECTOR (AWG #20)

			<u>Number of Wires</u>
RTG #3	SUPPLY	(5 amps)	7
RTG #3	RETURN		7
RTG #4	SUPPLY	(5 amps)	7
RTG #4	RETURN		<u>7</u>
TOTAL			28

J3 FLIGHT PLUG INTERFACE (AWG #28)

		<u>Number of Wires</u>
Main Bus Out		8
Power to X-Band Exciter (227 ma)		2
Power to S-Band Exciter (93 ma)		1
Power to Sun Sensor (100 ma)		1
Power to A/C Electronics (374 ma)		4
TOTAL		<u>16</u>

TABLE 3-8 (Continued)

J4 TEST CONNECTOR (AWG #28)

	<u>Number of Wires</u>
External Ground Loads (6 amp)	4
External Power for Sensors	2
RTG #1 V, I, T	3
RTG #2 V, I, T	3
RTG #3 V, I, T	3
RTG #4 V, I, T	3
Shunt Reg #1 I	1
Shunt Reg #2 I	1
Shunt Reg #3 I	1
Shunt Reg #4 I	1
DC Main Bus V, I	2
AC Main Bus V, I	2
DC Protected Bus V, I,	2
AC Protected Bus V, I,	2
Monitor Return	1
RTG Shunting Switch Command	4
Manual Initialize	1
Common Return	1
	<hr/>
TOTAL	37

TABLE 3-8 (Continued)

J5 RTG TEMPERATURE SENSORS (AWG #28)

		<u>Number of Wires</u>
RTG #1	Sensor Power and Return	2
RTG #1	Temperature Sensor Signal	1
RTG #2	Sensor Power and Return	2
RTG #2	Temperature Sensor Signal	1
RTG #3	Sensor Power and Return	2
RTG #3	Temperature Sensor Signal	1
RTG #4	Sensor Power and Return	2
RTG #4	Temperature Sensor Signal	<u>1</u>
TOTAL		12

J6 FCS INTERFACE CONNECTOR (COAX)

J7 CCS INTERFACE CONNECTOR (COAX)

<u>J8</u>	Output Power Connector	(AWG #28)	}	466 WIRES TOTAL
<u>J9</u>	Output Power Connector	(AWG #28)		
<u>J10</u>	Output Power Connector	(AWG #28)		
<u>J11</u>	Output Power Connector	(AWG #28)		
<u>J12</u>	Output Power Connector	(AWG #28)		

### 3 2 6.2 1 Subsystem Test

At this point, the PCE must be tested to verify operability of each shunt regulator, the current throttle, overvoltage trip, each inverter, the power distribution switches, and the low voltage cut off circuits. Figure 3-8 defines the equipment configuration required for this test.

A ground power unit consisting of four separately controlled RTG simulators will enable individual testing of each shunt regulator.

A test module provides the capability to switch "hard wired" loads during all test phases prior to final fairing installation.

The load simulator has programmable loads controlled by the OSE test set. Also this unit has sensors to detect the presence/absence of output power from each PCE distribution switch. Inverter frequency will be measured and transmitted to the OSE test set by the load simulator.

An interface simulator will provide command information to the CCS and FCS modems internal to the PCE. Verification of telemetry output thru the modems will be accomplished in this simulator.

The OSE test set will control the operations of all OSE equipment. The PCE internal sensors will be monitored thru connector J4. This data will be displayed and recorded at the test set.

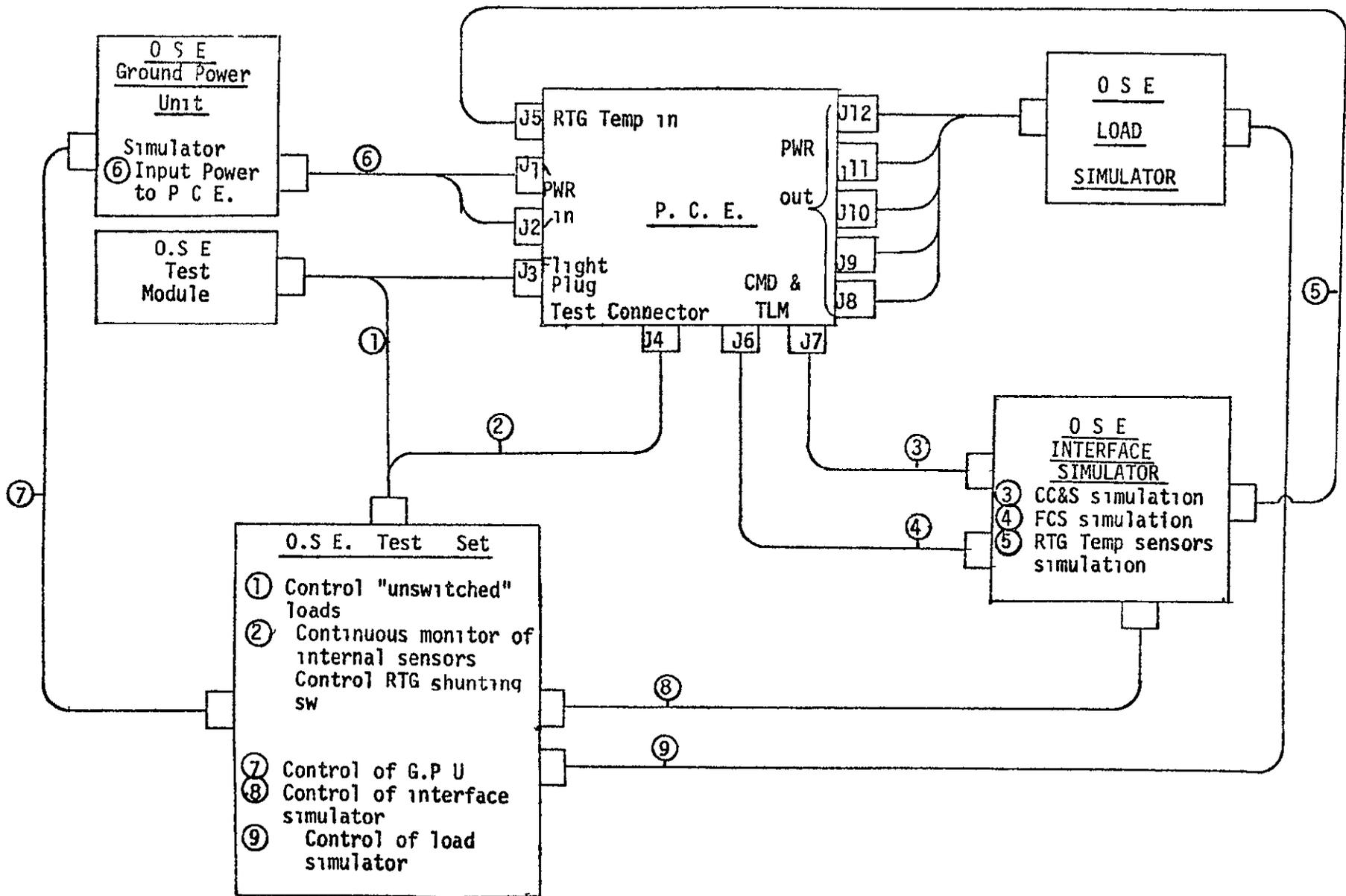


FIGURE 3-8

SUBSYSTEM TEST EQUIPMENT CONFIGURATION

### 3 2.6 2 2 System Integration and Test

All flight hardware will be electrically interconnected for the first time at this test. Figure 3-9 shows that the only simulated interface is the RTG's.

Before applying power to the system, the PCE must once more be checked to verify proper operation.

Each shunt regulator, the current throttle, and the inverters will be checked first, then the CCS will be powered to operate the PCE distribution switches. Final testing of the Low Voltage Cut Off will be done at this point.

### 3 2 6 2 3 Pad Test/Launch Support

Figure 3-10 defines the PCE configuration for this phase. All OSE interfacing is thru the vehicle umbilical.

At this point, the primary PCE functions (shunt regulators, current throttle and the inverters) will be checked prior to application of power to the loads. Proper power switching will be determined as each load is operated thru a mission profile sequence. Secondary PCE functions such as the overvoltage trip and the low voltage cut off circuits would not be operated during a normal pad sequence.

### 3 2 7 Reliability

Figure 3-11 shows a summary of calculated reliabilities for the system based on a ten year mission. The values shown in the table pertain to the reliability

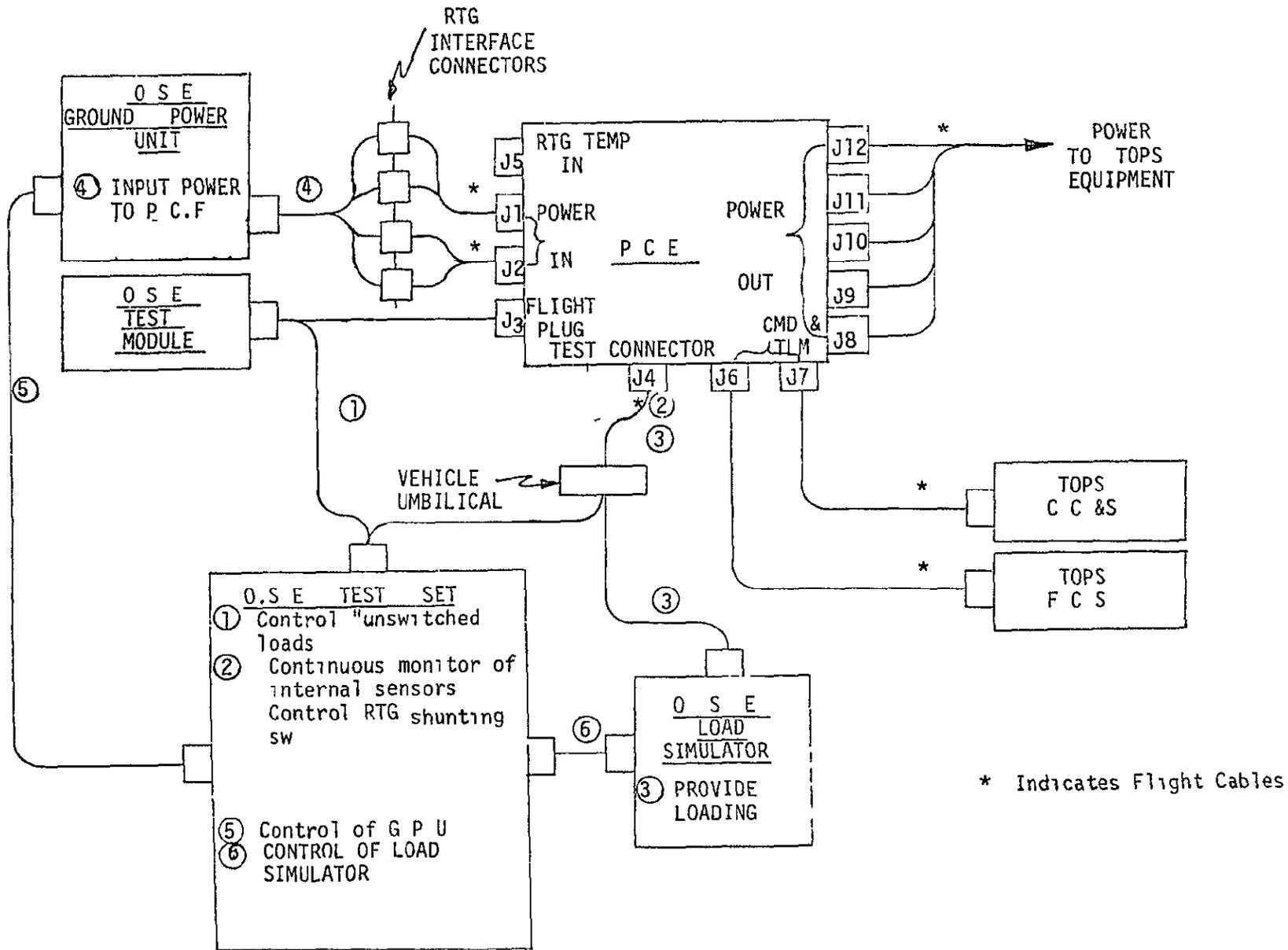
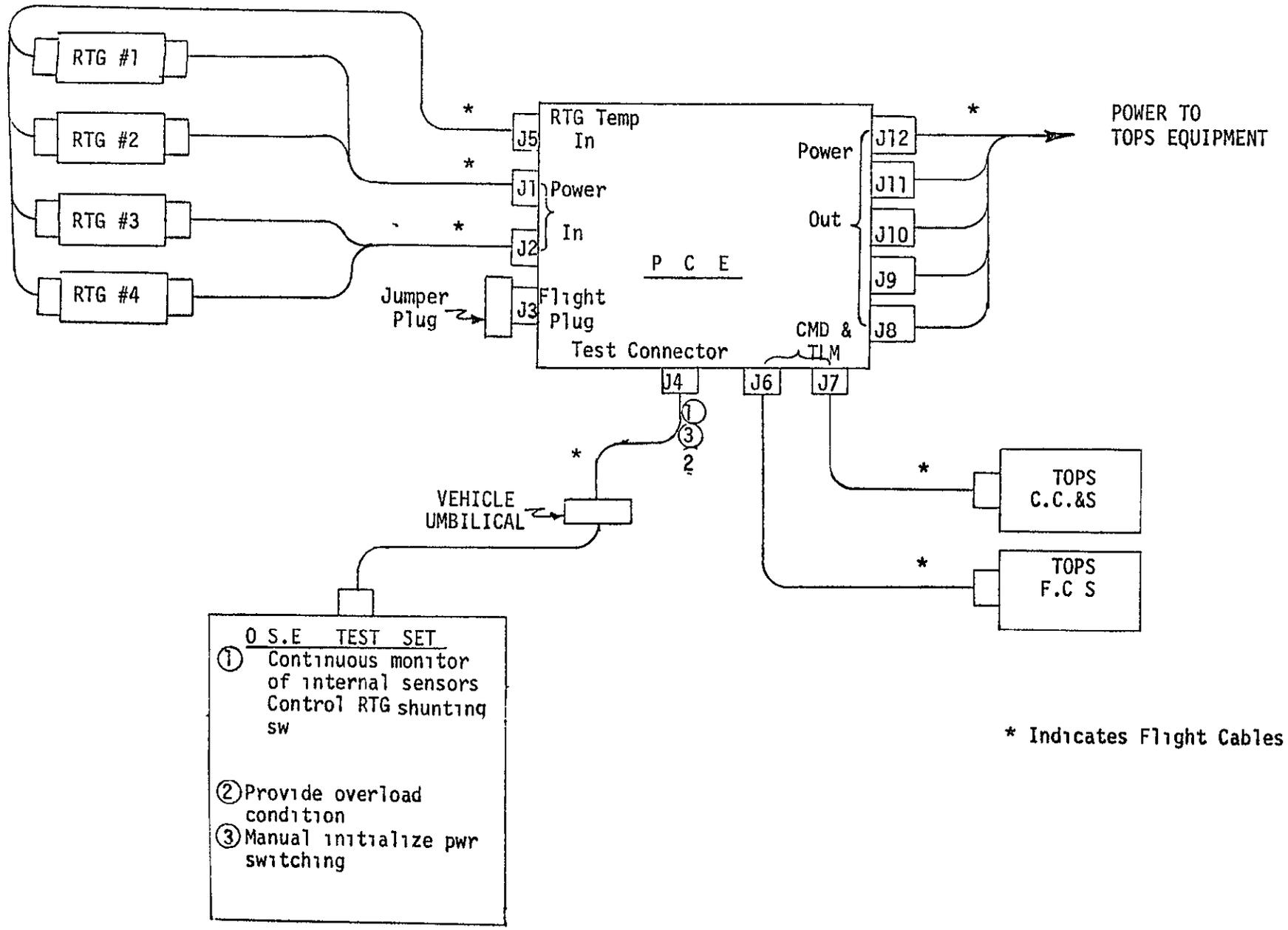


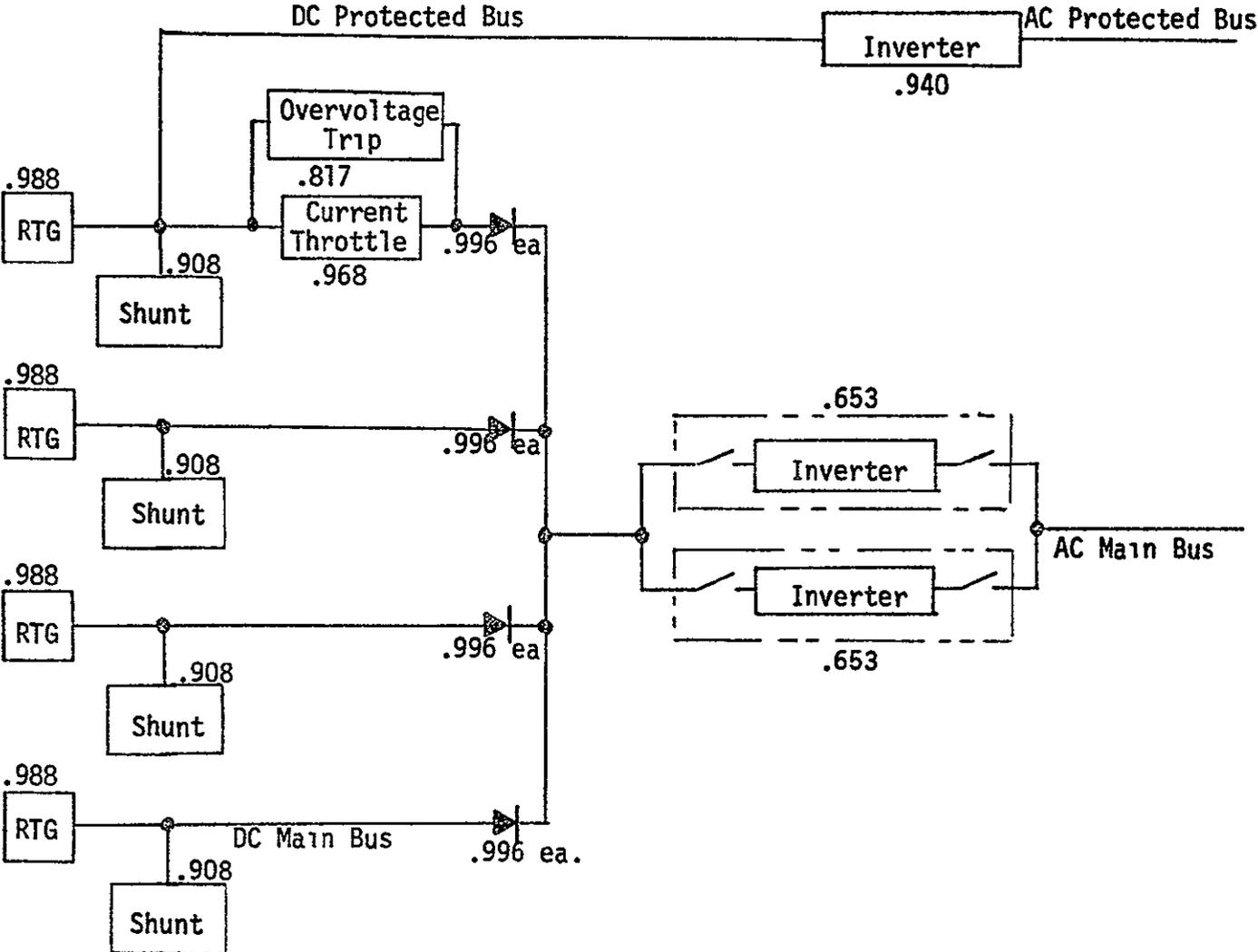
FIGURE 3-9 SYSTEM TEST EQUIPMENT CONFIGURATION



\* Indicates Flight Cables

FIGURE 3-10 PAD TEST/LAUNCH EQUIPMENT CONFIGURATION

Based on 10 year mission



	Main Bus Reliability		Protected Bus
	100% Power	75% Power	
AC System	.7296	.8193	.8708
DC System	.8292	.9311	.8740

FIGURE 3-11 RELIABILITY SUMMARY

of providing power on the main and protected busses. The values for the DC system are simply those calculated ignoring the presence of the main and protected bus inverters

Total power system reliability would have to take account of power control and power conditioning elements in order to make a valid reliability comparison of AC and DC systems. With DC to DC converters used for the DC system and less complicated transformer rectifiers used for the AC system the reliability difference in the two systems shown in the figure will tend to be reduced

The reliability values for 100 and 75 percent power cases refer to the availability of power from four and three RTG's respectively

The reliability numbers indicated at each of the blocks is based on the number and type of parts considered for the particular block

### 3 3 OPTIONS AND TRADE STUDIES

The features of the system described in Section 3.2 were selected through continuous evaluation of alternatives during the course of the study. This section summarizes the principal trade study and evaluation efforts and, where appropriate, describes design options which appear practical and might be employed where warranted by particular conditions.

The trade studies are grouped according to their relationship with the following power system functional areas:

- 1 Power Source
- 2 Regulation
- 3 Distribution
- 4 Power Switching

#### 3 3 1 Power Source Studies

Studies of the RTG power source for TOPS are being conducted under a separate contract and have been considered in this TOPS-PCE program only insofar as proposed RTG concepts influence the power system configuration. The principal factors considered thus far are:

- (a) The need for long term flight batteries, and
- (b) the use of launch batteries to augment limited on-pad RTG capability.

##### 3 3 1 1 Long-Term Flight Batteries

The purpose in considering a long-term flight battery revolves around the high degree of operational flexibility provided by batteries. Principally

they permit the application of loads greatly in excess of those capable of being satisfied by the prime power source. Additionally, through power averaging, they potentially permit a reduction in the capacity of the prime power source. In the case of RTG's this can represent large cost savings because of the high costs of isotopic fuels. Evaluation of these and other factors is provided below.

#### EVALUATION FACTORS

##### A Power Averaging

The load profile chart, Figure 3-1, indicates a maximum power requirement of 460 watts during the Far Encounter phase of any particular planetary pass. This phase may last as long as twenty hours. For each watt supplied by nickel cadmium batteries (the only reasonable contender for the life requirements involved) the weight penalty is 2 pounds considering an energy density of 10 watt-hours/per pound and operation for 20 hours. For the contemplated RTG's, the weight penalty is about 0.5 pounds per watt. Thus the weight penalty of battery averaging is at least four times as great as increasing the RTG size to provide direct power. With depths of discharge less than 100 percent (decreasing the effective energy density) and taking the losses of discharge conditioning into account the weight penalty difference is even more pronounced. For these reasons the use of batteries for power averaging does not appear to be justified for the TOPS mission.

B High Current Pulse Loads

Particular pyro loads will incur power demands significantly over and above those listed on the power profile, Figure 3-1. Suitable methods for supplying such loads are through the use of (1) capacitor - bank systems of the type used on previous Mariner - Class spacecraft, (2) thermal batteries which have been used for many high current short pulse duration applications. These systems are reliable and would be suitable for the 12 year TOPS mission.

C Turn-On Transients

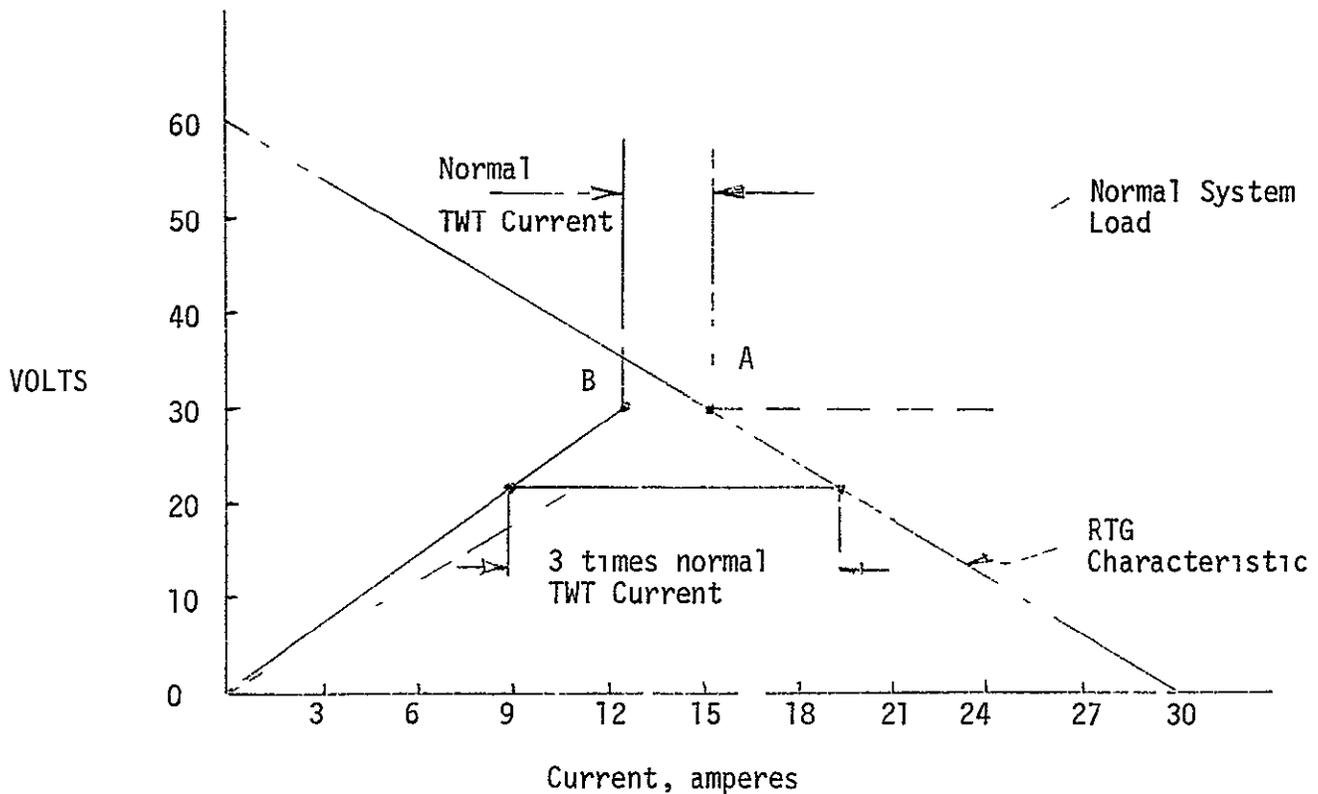
Many continuous loads whose steady-state demands would be satisfied by the RTG have high starting current characteristics. The TWT mentioned earlier provides a case in point. Batteries would seem to minimize the turn-on transient disturbances. However, a variety of suppression techniques can also be employed to minimize transients and these should be thoroughly investigated before a battery is used for transient suppression purposes.

D Fault Clearing Capability

The high current possible with batteries make them ideal for fault clearing purposes. The RTG's may also have sufficient fault clearing capability. An estimate of this capability is provided below to determine if the battery is necessary for this purpose.

In this estimate it is assumed that all loads are fused and that any fault may be cleared with a current at 3 times the normally rated load value by blowing the fuse. The figure below shows the relationship of the RTG voltage-

current characteristic to the load characteristics. This relationship as shown assumes a nominal load of 460 watts with the RTG just capable of supplying this power. This represents a situation which might exist at the Far Encounter phase of the last planetary encounter.



Point A represents the normal operating point with the system drawing 15.3 amps at 30 volts from the RTG. The TWT is the largest load and is rated at about 60 watts. Point B indicates the current drawn by all loads except the TWT. The load line through the origin and point B represents the impedance of these loads assuming they are purely resistive in nature. Assuming a complete short in the TWT, the system voltage would be depressed increasing

the RTG current output. At 20 volts or lower the current through the TWT fuse would be larger than 3 times the normal rating and the fault would be cleared.

In the above example the largest load of the system was used. The clearing capability for smaller loads would be that much better. The conclusion is that sufficient fault clearing capability exists with the RTG's and the use of batteries for that purpose is unnecessary.

E Reliability

Any present commitment on the use of a long-life battery for TOPS would be made without the benefit of a demonstrated 12 year life capability. This is probably the most important single fact against the use of a long-life battery. Aside from this, the possible leakage of electrolyte may endanger other spacecraft equipment and possibly interfere with certain science measurements. Reliability is also compromised as a result of the additional integration complexity involving such functions as charge regulation, discharge regulation, battery temperature control, etc.

CONCLUSIONS

The use of long-term flight batteries for TOPS appears neither necessary nor desirable. The principal benefit of batteries would be to reduce turn-on voltage transients. It is considered that other less complex techniques can be used to relieve such transients. These would include a variety of suppression circuit techniques and the judicious application of filters to the more sensitive loads.

### 3 3 1 2 Launch Batteries

Launch batteries may be required if the RTG's are not capable of generating power because of environmental restrictions during the launch phase. The proposed RTG's are designed for vacuum operation and may be damaged if certain interior elements are exposed to air. Since the RTG's cannot be vacuum sealed reliably, it may be necessary to cool the fuel capsule before launch or pressurize the RTG interior with an inert gas which would be released after space flight is achieved. With fuel capsule cooling no power is generated, requiring the use of a launch battery (full RTG power would be developed several hours after launch), while with inert gas protection, partial power is generated.

The study reported here was to determine the complexity involved in using a launch battery and thereby indicate, from a power system standpoint, which of the proposed RTG schemes, fuel capsule cooling or inert gas pressurization, was preferred. No attempt was made to justify the preference from an RTG point of view considering comparative RTG weight penalties, manufacturing complexity or cost.

A subsystem configuration was developed which used batteries specifically for the case where pre-launch cooling of the RTG's is used, i.e., no power is generated prior to launch. In accordance with the load profile a launch and ascent load of 250 watts is used. A rough calculation indicated that full RTG power would be developed after 2 hours. This was the value assumed in determining battery size.

Evaluation of this system is provided below

- A Weight - The launch phase requires 500 watt-hours of energy (250 watts for 2 hours) With allowances for prelaunch and contingencies, a 750 watt-hour capability seems reasonable Using silver-zinc batteries rated at 50 watt-hours per pound, the battery weight is 15 pounds It is estimated that 5 to 10 pounds of other equipment would be required (series regulators, protective circuits, etc) for a total of 20 to 25 pounds This would be the difference in a battery versus no-battery system discounting any difference in RTG weight In sizing the battery, no allowance was made for partial RTG power generation during the 2-hour buildup period If the possibility of a battery failure is hypothesized during this 2 hour period the gradual buildup of RTG power to the loads could be injurious In the implementation described in the following paragraph the RTG's are actually shorted out to prevent the gradual buildup possibility Thus the disallowance for partial RTG power is justified
- B Battery Electrical Integration - Figure 3- 12 shows a particular arrangement for integrating launch batteries into the power source end of the subsystem Various other schemes were considered - the one shown appeared to be least complex and survives a variety of failure mode conditions Comparing this schematic with one not using a battery (Figure 3-3) the following differences are noted
- 1 Two series regulators are required for feeding battery power to the protected and main busses

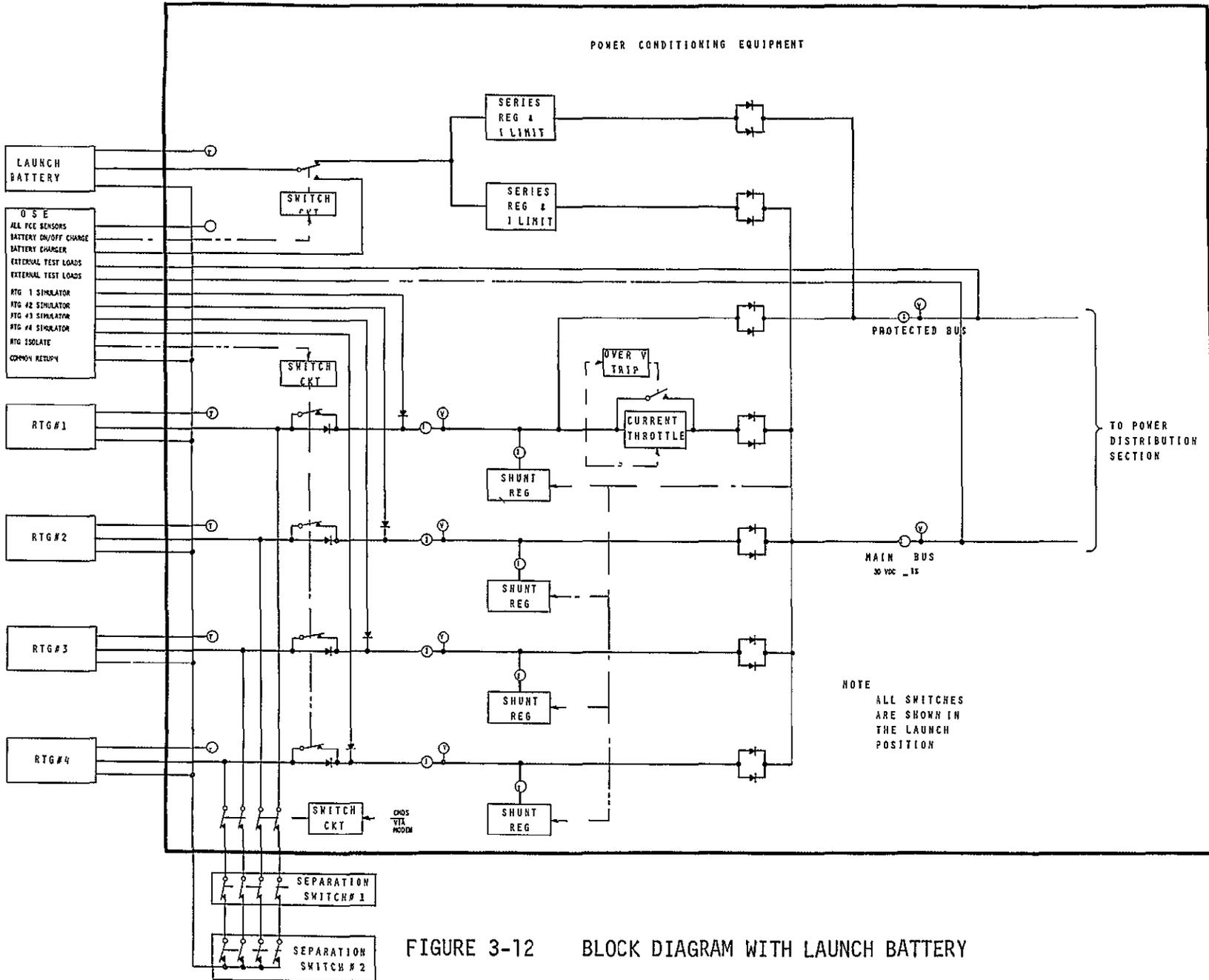


FIGURE 3-12 BLOCK DIAGRAM WITH LAUNCH BATTERY

- 2 Isolation diodes are introduced on the protected bus to prevent the battery from discharging through the shunt regulator of RTG No 1
- 3 A switch circuit is introduced to permit battery charging through OSE
- 4 RTG output diodes are used to permit on-pad testing of the subsystem. Since the RTG's are cold the diodes prevent them from loading down RTG test simulators. Once space flight is achieved and the RTG's produce full power these blocking diodes are bypassed through a switching circuit.
- 5 Separation switches are used to short the RTG's. This is a backup feature used in the event of a failure of the launch battery. As long as the spacecraft is attached to the kickstage the switches are closed, shorting the RTG's and thus preventing partial power from being applied to the loads. If a battery failure is detected it would be necessary to delay separation until proper RTG temperatures are established. Since separation occurs after interplanetary injection the delay may be acceptable. No power would be available but the mission could proceed normally after separation. An additional switch circuit is shown which can override the RTG shorting once it is established that RTG temperatures are at a level permitting sufficient power generation.

In general it is seen that the batteries introduce a variety of electrical complexities. Not all of these have been covered in detail. For example each new switching element will require command & CCS circuitry not to mention the additional test procedures that would be required.

C Battery Physical Integration - The principal problem regarding physical integration concerns potential leakage of the battery. Opinions regarding this question were solicited from several battery experts. They all felt that the active silver-zinc system would in time exhibit electrolyte leakage. Ways of getting around this problem might be as follows:

- 1 Jettison the battery
- 2 Mount the battery on the kick stage
- 3 Develop an hermetic case and/or improved seal

The first two options introduce significant interface complexity. The third method would require additional weight and would be difficult to prove for the life times involved.

#### CONCLUSION

The above evaluations indicate a preference for on-pad RTG capability. However, this must be weighed against the complexities in RTG design that might be involved.

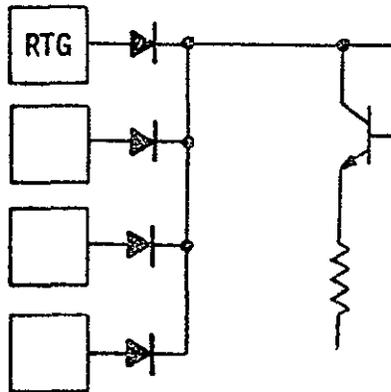
### 3 3 2 Regulation Studies

Shunt regulation was selected early in the study as the appropriate method for regulating the RTG voltage. The principal reasons for this selection are (1) maximum possible efficiency - in-line loss elements are avoided, (2) shunt regulation presents constant load conditions for the PTG's which both limit RTG internal temperatures and avoid abrupt temperature-time conditions.

A variety of shunt regulation methods are possible. As described below several types were considered and a particular approach adopted as being most suitable.

#### SHUNT ALTERNATIVES

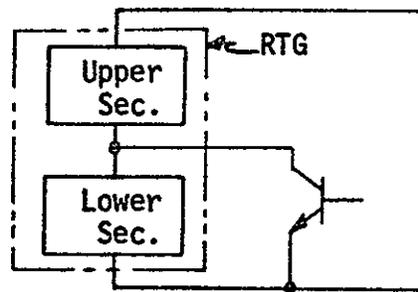
##### 1 Full, linear dissipative



Operation All excess RTG power is dissipated within the shunt regulator. To limit environmental temperature variations the transistor elements would be located in the PCE bay. The less critical resistor elements may be located externally. Maximum dissipation occurs when the transistors are saturated with almost full bus voltage applied to the resistive elements. The maximum transistor dissipation is about 1/4 this value when the transistor and resistor drops are equal.

Evaluation For a shunt designed to dissipate the full RTG output (600 watts at beginning of life) the transistors must be designed to dissipate 150 watts. It is estimated that the PCE bay could handle about 100 watts of total dissipation with an allocation of 40 to 50 watts for the shunt transistor elements. Thus the full dissipative shunt approach exceeds this constraint.

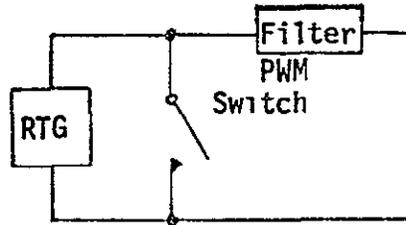
## 2 Partial Shunt



Operation The RTG's are electrically divided into upper and lower sections. Shunt regulation is applied to one of the sections which results in a total dissipation 1/4 that of a full shunt. The need for resistive shunt elements is eliminated, however the transistor dissipation is identical to that for a full shunt.

Evaluation No decrease in transistor dissipation is provided by this approach. Therefore no relief is provided for the PCE dissipation problem. Resistive elements are eliminated but at the expense of requiring a more complicated RTG design whose upper and lower sections must be physically integrated to average out the different temperature operating points of both sections.

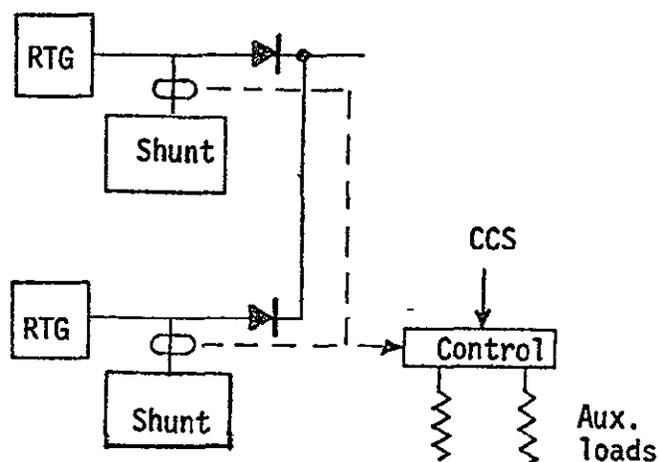
3 Switching Shunt



Operation The shunt switch ( a transistor switch would be used) operates in a rapid pulse width modulated mode permitting the transfer of only that amount of energy required to sustain the load. The filter smooths the chopped nature of this energy flow. Except for switching, control and filter losses, there is no large component of dissipated power.

Evaluation The filter incurs a direct loss of 3 percent of the transferred power. With the switch in a closed position the RTG current is twice that at rated power. This could result in excessive EMI generation. Other analysis shown in previous reports indicates significant rises ( $\Delta T \approx 60^\circ\text{C}$ ) in hot junction temperatures at no-load conditions.

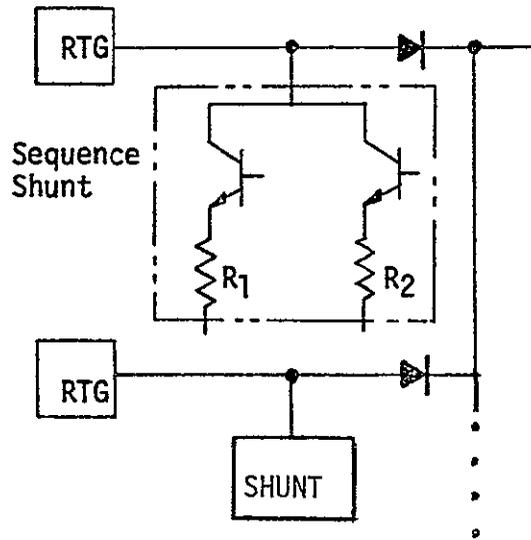
4 Full, linear dissipative, auxiliary loads



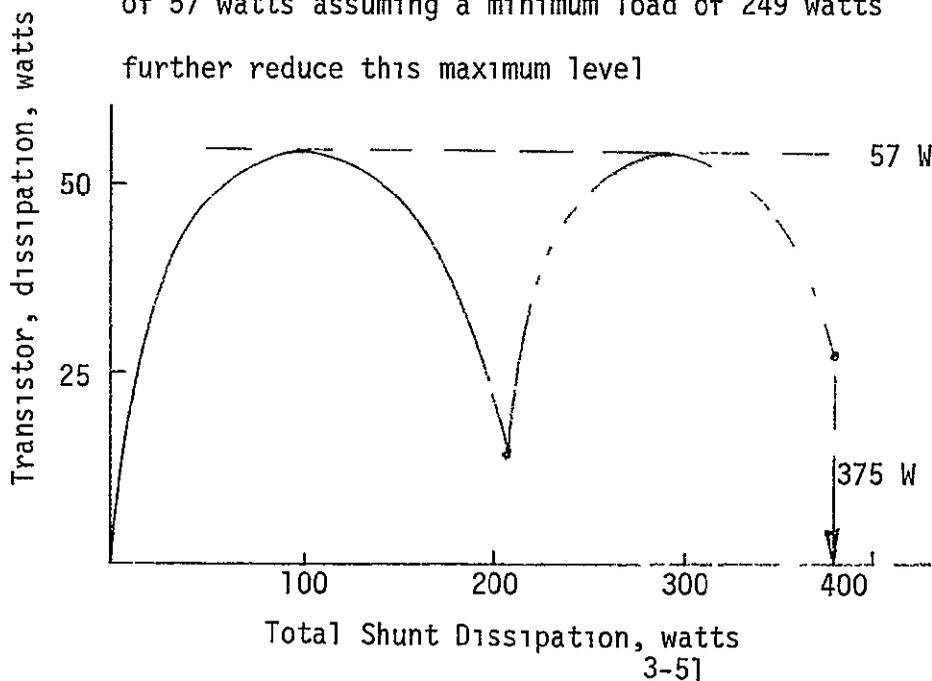
Operation This approach uses a full dissipative shunt with its range reduced through the use of auxiliary loads. To limit the transistor dissipation to around 40 watts (the limit of the PCE-bay dissipation) the shunt resistive elements are sized to dissipate 160 watts. Sufficient auxiliary loads are then required to absorb the full RTG capability (440 watts for a 600 watt RTG output). The auxiliary loads are in discrete increments permitting load adjustments such that the active shunt regulator is always at midrange (around 80 watts of dissipation). The switching in or out of any load (none of which is greater than 80 watts) then occurs within the dynamic range of the shunt regulator. Subsequently the auxiliary loads must be adjusted to again bring the active shunt to midrange in preparation for the next application of loads. In this way, all switching (including the switching of the auxiliary loads themselves) occurs within the dynamic range of the active shunt, resulting in fast system response. To maintain the midrange adjustment it is necessary to sense the active shunt current and through appropriate logic circuitry add or remove the necessary auxiliary loads until the proper shunt current value is reached.

Evaluation: This approach satisfies the PCE bay dissipation constraint but at the expense of added complexity - current sensing in an active control loop, logic circuitry, auxiliary loads, switching elements

5 Full, sequence  
dissipative



Operation This method uses two or more transistor/resistor legs per shunt which operate sequentially. As the transistor in the first leg is varied from full-off to full-on, the transistor passes through a region of maximum dissipation as shown in the sketch below. When the first transistor is saturated the second leg operates from full-off to full-on. For the resistance values indicated the sketch shows the range of transistor dissipation as a function of total shunt dissipation. With a 2-step sequence it is possible to limit transistor dissipation to a maximum value of 57 watts assuming a minimum load of 249 watts. Additional steps could further reduce this maximum level.



BOL RTG Power	624 W
Minimum Load	249 W
Shunt Req't	375 W

Dissipation profile for  
 $R_1 = 3.95$  ohms  
 $R_2 = 5.25$  ohms

The resistor values are applicable if a single shunt is used for all 4 RTG's. Since 4 separate shunts would be used the appropriate resistance values are quadrupled  $4 \times 395 = 158$  ohms for the first leg of each shunt and  $4 \times 5.25 = 21$  ohms for the second leg.

Evaluation The sequence shunt appears attractive from a thermal standpoint. Preliminary circuit concepts are not complex and interface requirements are minimized. It appears feasible that each RTG could use a separate sequence shunt without any requirements for using common control circuitry.

Conclusion Based on the above evaluations the sequence shunt appears to offer the most suitable characteristics. Detailed circuit and reliability analyses are required to further substantiate this choice.

### 3.3.3 Distribution Studies

These studies have concerned bussing arrangements, RTG diode isolation, fault protection concepts, and comparisons of AC and DC power distribution. The results of these studies are presented below.

#### 3.3.3.1 Bussing Arrangements

The purpose of this study was to identify several practical bussing alternatives and through an elimination process select a baseline bussing arrangement.

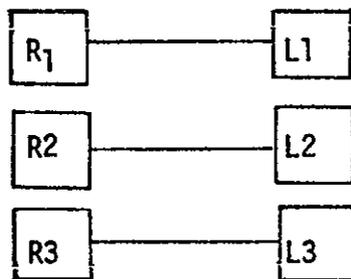
Certain basic criteria were used in considering bussing alternatives:

1. Power is to be provided from 3 to 4 separate RTG's.

- 2 The output from any single RTG or group of RTG's will be regulated at 30 VDC. This constraint results from the basic selection of shunt regulation described earlier and the voltage defined for the RTG's under study.
- 3 Consideration is to be given to establishing power priority to loads in accordance with their mission criticality.
- 4 Means are to be incorporated for limiting the effect of source or load faults.

The principal bussing concepts considered and their evaluation are described below.

1 Separate bus concept

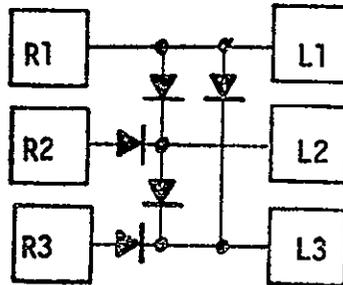


Description The loads are divided into separate groups and supplied by separate RTG's.

Evaluation This method provides the best isolation against load or source faults but is severely limited in its flexibility. Critical loads contained in any of the load groups ( $L_1$ ,  $L_2$  or  $L_3$ ) are dependent on power from a single source. Failure of any single source could thereby constitute

a total loss of the mission. Another severe flexibility restriction concerns the power demand limitation imposed by any single source - no load is permitted to exceed the single source capability.

2 Priority bus concept

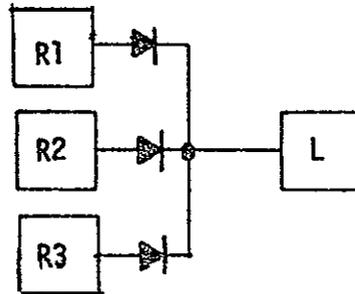


Description This concept is representative of a class of arrangements in which certain priority load groups can receive power from multiple sources while less critical groups are restricted to power from fewer sources. In the particular concept shown, L3 receives power from R1, R2 and R3, L2 receives power from R1 & R2, and L1 receives power only from R1.

Evaluation It would appear that this method passively accomplishes power priority to critical loads. However this capability is conditional on the critical loads also being those demanding the greatest power. From the arrangement shown, L3 would be the critical load group since power is available from all three sources. If components of L3 demand peak power in excess of the output of one RTG the arrangement is fine. If, however, peak demands are associated with non-critical loads, more generally the case, the advantages of this system are somewhat compromised. If non-mixing of critical and non-critical loads is to be rigidly adhered to the system is probably no more flexible than the "Separate Bus Concept" described earlier. Since the

TOPS requirements are of a preliminary nature, the adoption of such priority bussing arrangements is not considered to be appropriate at this time

### 3 Single Bus Concept



Description All sources supply power to a common bus, all loads draw power from this common bus

Evaluation This method provides the greatest source/load flexibility. Source fault protection is easily provided with the use of the isolation diodes shown. Active means for isolating load faults or limiting their effects is required.

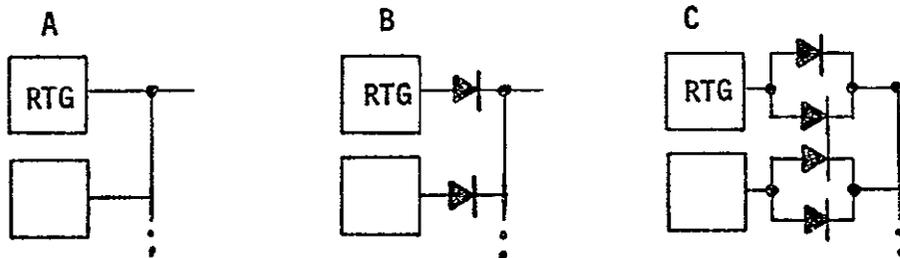
Conclusion The single bus concept provides the flexibility required for the sources and loads as presently defined. The greatest deficiency of this concept pertains to the need for active means for load fault detection and corrective action. Although the alternative bussing concepts may provide some relief in this regard for certain loads it is not clear that all load combinations could avoid the need for active load fault detection methods. This further substantiates the single bus concept as the preferred choice.

3 3 3 2 RTG Diode Isolation

The previous section indicates that source fault protection is easily achieved by RTG diode isolation. This section shows the evaluation of such isolation.

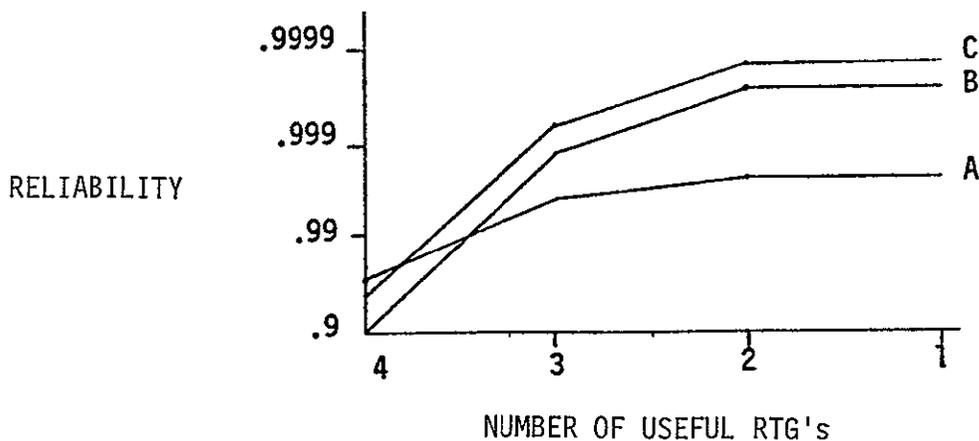
The figure below shows three arrangements for the RTG's which were considered, with associated diode power loss and weight penalties.

METHOD



POWER LOSS, %	0	2.5	2.5
WEIGHT PENALTY, lbs	0	0.5	0.8

For a system which uses four RTG's, the 10 year reliability of providing partial or full power (1, 2, 3 or 4 RTG's) is shown on the sketch below for the three arrangements considered. This calculation takes the possibility of RTG and diode failures into account in both short and open circuit failure modes.



The reliability of having power from all RTG's is highest for Case A in which no isolation diodes are used. This is consistent since the diodes are entirely unnecessary when power from all RTG's is required. The diodes introduce failure modes accounting for the lower reliability of Cases B & C. Where fewer RTG's are acceptable the diodes play a significant role as indicated.

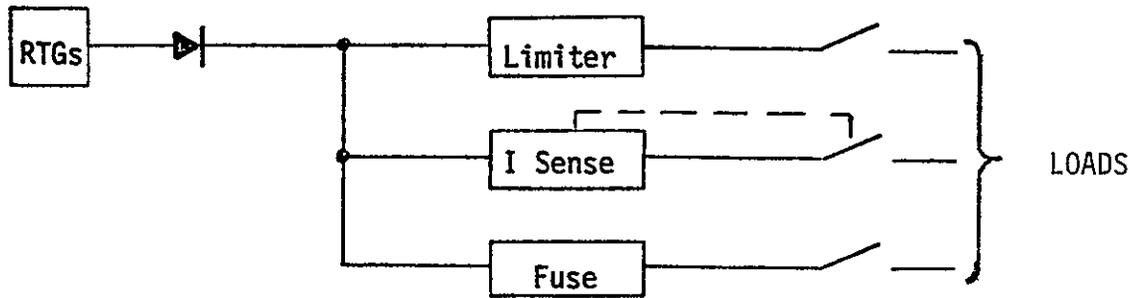
As indicated in Section 3.2.3, a significant mission capability can still be provided with the loss of one or more RTG's. For this reason, the diode protection option is preferred. A nominal weight increase of 0.3 pounds also indicates the desirability of using 2 parallel diodes at the output of each RTG.

### 3.3.3.3 Fault Protection Study

The study of bussing arrangements (paragraph 3.3.3.1) indicated a preference for having the RTG outputs fed to a common bus. The principal benefit is in load operational flexibility because of higher peaking capability. Since all loads would operate from this bus some means for removing faulty loads is necessary in order to maintain power service to the remaining loads.

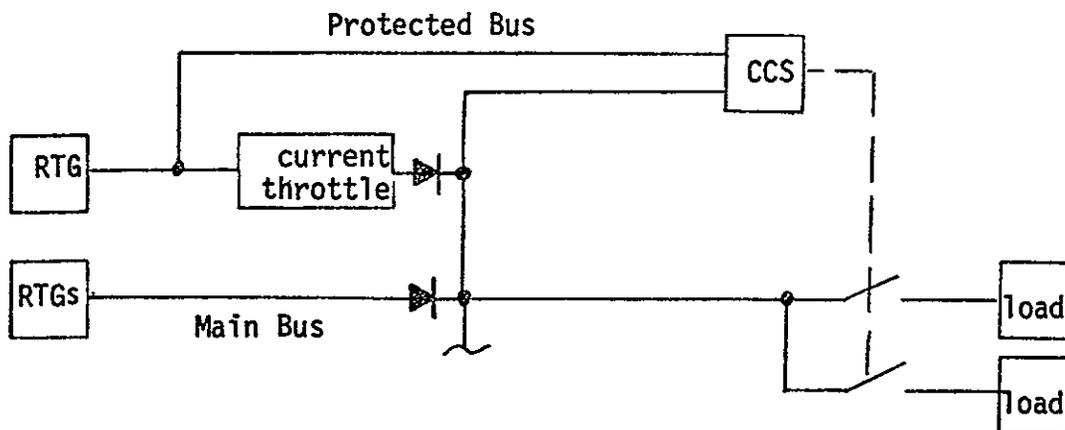
Several preliminary fault removal concepts were evaluated as a start in evolving a protection system design.

CONCEPT NO. 1 - This concept depends on using separate fault protection devices for each load as indicated in the sketch below.



The limiter and fuse devices can detect and at best limit or isolate the faulty loads. The sensor/relay device has the added ability of providing corrective action which, besides removing the faulty load through a switching action, might involve transferring power to a substitute load. It is estimated that the TOPS system could involve eighty separate loads. Hence eighty devices of the above type might be required.

CONCEPT NO 2 - This concept depends on a centralized source (CCS) for detecting and isolating the fault and transferring to standby loads. The sketch below indicates the approach.



Fault information is fed to the CCS. Such fault information may be derived from general system sensors or load dedicated sensors. Through the diagnostic capability of the CCS the faulty load is detected and removed upon actuation of its power control switch. In order for CCS to perform the detection and isolation functions it requires a source of power. Since a particular load fault could conceivably short out the main bus with a resultant loss of power to the CCS, a redundant source of power is used to preclude this possibility. This so called "protected bus" takes power from one of the RTG's ahead of an in-line "current throttle" impedance device. This device responds to a main bus voltage depression (due to a fault) by increasing its series impedance such as to maintain its input voltage at a minimum value. In this way the power of the associated RTG is available for CCS operation. The current throttle is in essence a series dissipative voltage regulator which responds to voltage sensing at its input rather than its output.

Both of the above concepts were considered to incorporate a backup means for initiating corrective action in response to a fault. The level of the main bus voltage was used as the criterion for initiating this action through a Low Voltage Cut Off (LVCO) circuit.

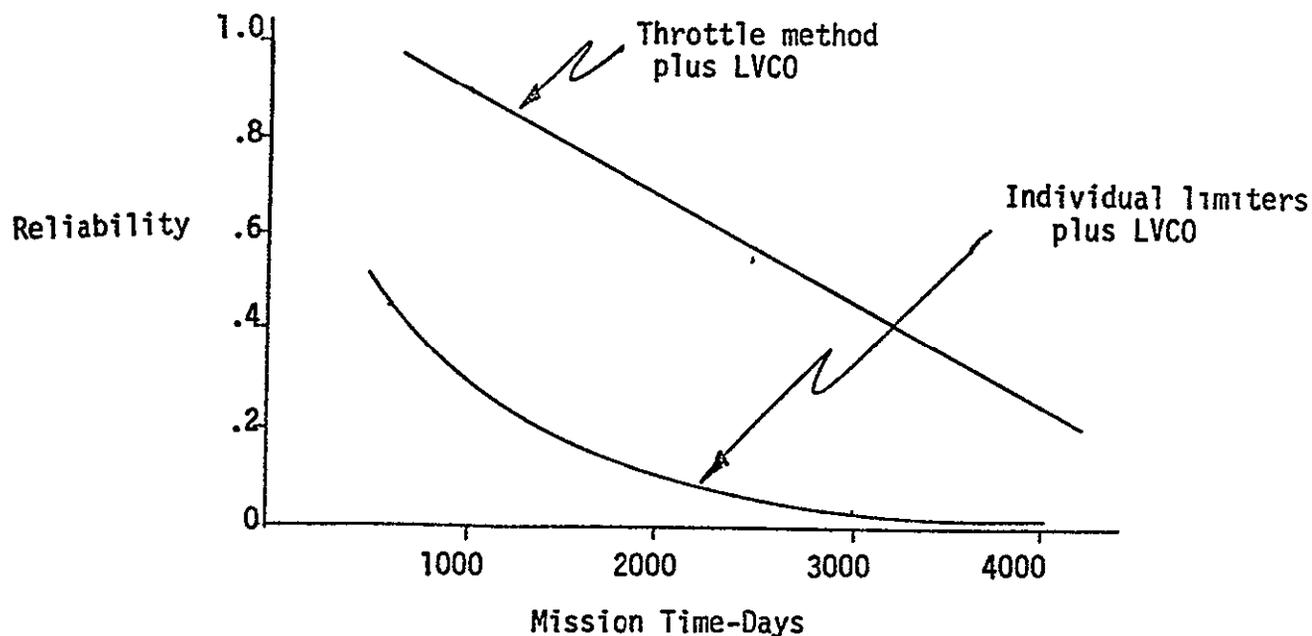
To keep the LVCO as simple and reliable as possible it would be designed to initiate certain predetermined actions. Nominally these actions might be the removal of power from all non-critical loads and the transfer from main to standby elements of critical loads. These actions may be carried out

sequentially with the idea that fewer switching actuations might be necessary. If the fault is removed early in such a sequence, further actuations would be unnecessary.

EVALUATION The principal evaluation of the concept described above concerned reliability. For this purpose nominal circuit complexities were assumed for the principal functions identified.

The switch designs described in Appendix D provided a basis for estimating the failure rate of the various power control elements considered. Reliability estimates of the current throttle and LVCO were based on considering circuits of similar complexity.

The principal results of this reliability estimate are shown below.



The results broadly indicate a preference for the second concept. The higher reliability is the direct result of reducing the complexity of the in-line switching elements. It may be recalled that Concept No. 1 depended on individual sensors for actuating switches at each load while Concept No. 2 depended on CCS as a central sensing element. It may be argued that CCS would have to depend on local sensors for its information and there would therefore be no real reduction in complexity. This may be true to some extent but in general CCS will respond to power margin conditions (indicated by the shunt regulator current) and load priorities established by the particular mission phase. A reduction in localized sensing therefore seems feasible. The complexity of the CCS would not be effected since its control of power margin and load priorities would be required for either of the concepts. Concept No. 2 therefore is the preferred concept. Its selection does not eliminate the possible use of individual sensor/relay devices. They may still be used as particular conditions dictate. In this sense Concept No. 2 is more encompassing as a basis for evolving a final fault protection system.

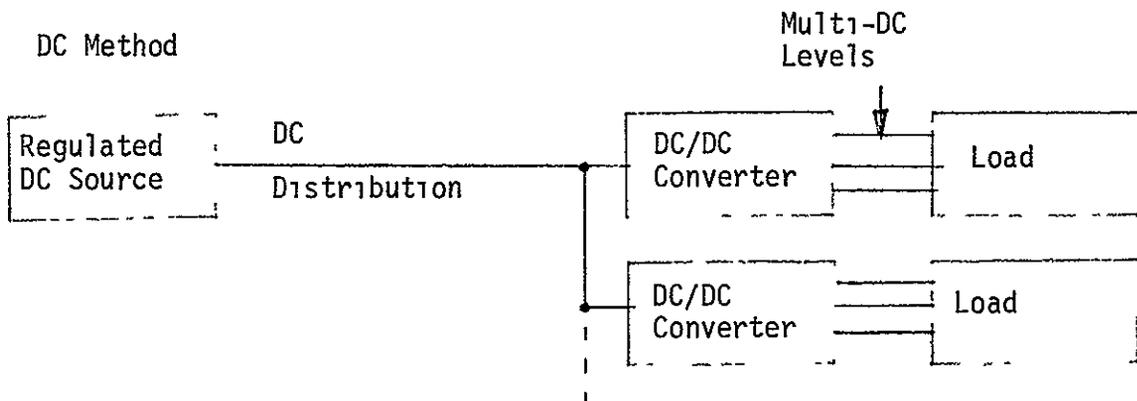
### 3.3.3 4 Distributed Form of Power

This trade study concerned the question of whether AC or DC is the preferred form of distributed power. This question pertains only to that class of loads which require power conditioned to multi-DC levels within a range of about  $\pm 100$  volts.

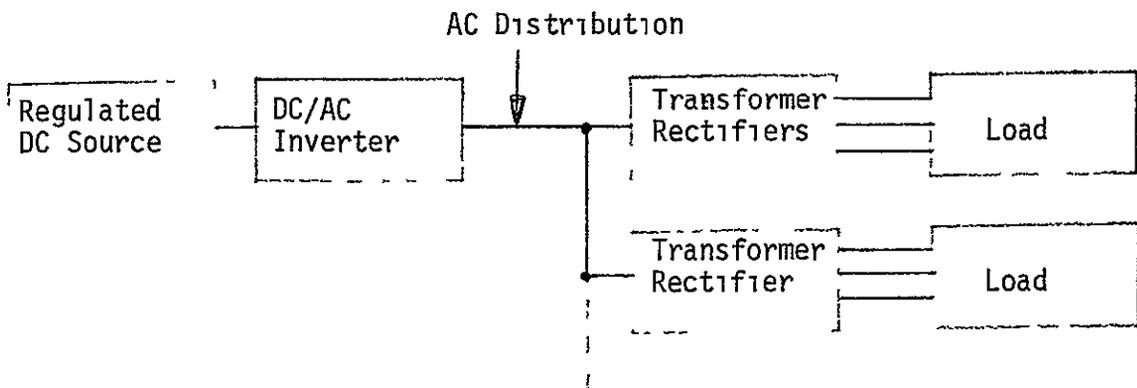
Certain loads requiring specific AC conditioning (e.g., 400 Hz motor loads) or very high voltage DC conditioning (e.g., TWT loads) would utilize special conversion units operating directly from the 30 VDC regulated RTG output. The consideration of AC vs DC specifically excludes these special loads.

The DC and AC methods for conditioning to multi-DC levels are illustrated below.

#### 1 DC Method



#### 2 AC Method



The DC method distributes the regulated RTG power at 30 VDC to separate DC to DC converters at the loads. The converters are specifically designed to provide the multi-DC levels required. Within each converter the power is chopped, transformed and rectified to the required levels.

The AC method inverts the RTG regulated power at some selected frequency and it is this AC power which is distributed to the various loads. Transformer-rectifiers at each load condition the AC power to the required DC levels.

Study results to date have not clearly favored one method over the other. As a general summary the DC method appears to have a slight edge regarding weight and efficiency. This is due to the fact that the AC method requires double transformation (one transformer in the inverter and one in each transformer rectifier) while the DC method requires only one transformer in each converter. Compensating somewhat for these differences is the greater user flexibility of the AC system. It is generally an easier task to modify a transformer-rectifier to adjust output voltages than it would be to modify a DC to DC converter, simply because fewer parts are involved and the complexity is proportionately reduced. All in all, the comparative studies of AC and DC have not resulted in a clearcut preference.

Although no specific recommendations were developed concerning the form of distribution, there is at least no contradiction with the JPL decision to consider AC as the preferred method at this time.

In order to provide further insight into this general question the implementation of both AC and DC distribution was considered with power control functions taken into account. Figures 3-13 and 3-14 show simplified diagrams of the functions required for both the DC and AC distribution methods. In either case the use of a data bus is assumed. The data bus transmits control signals from the CCS or the flight command subsystem. These signals are demodulated by the modem and routed to the appropriate switch control circuit. This circuit, which operates on DC from the main or protected busses, then provides the power to its associated switching element for controlling either the DC or AC power supplied to the loads.

The above simplified implementation can take many forms depending on the relative locations of the various elements. Figures 3-15 and 3-16 indicate some basic variations that were considered. They are described in greater detail below.

#### 1 DC Distribution Variations (Figure 3-15)

Four power control configurations are shown relating to critical and non-critical loads and whether power control is exercised within the PCE or at the load. A fifth configuration pertains to power for the CCS.

##### Configuration A: Critical redundant load, power switching at PCE

The power switching functions utilize the protected bus concept described earlier in paragraph 3.3.3.3. Besides the CCS, it is necessary to supply power from both busses to the CCS modems and the switch control

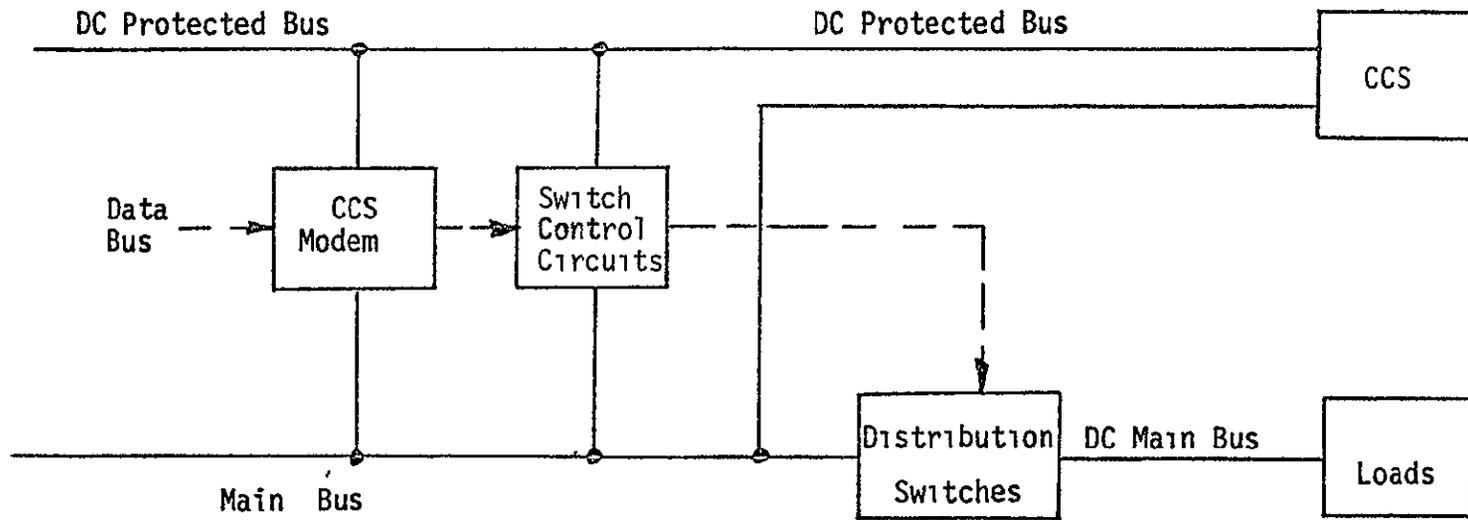


FIGURE 3-13

DC DISTRIBUTION CONCEPT

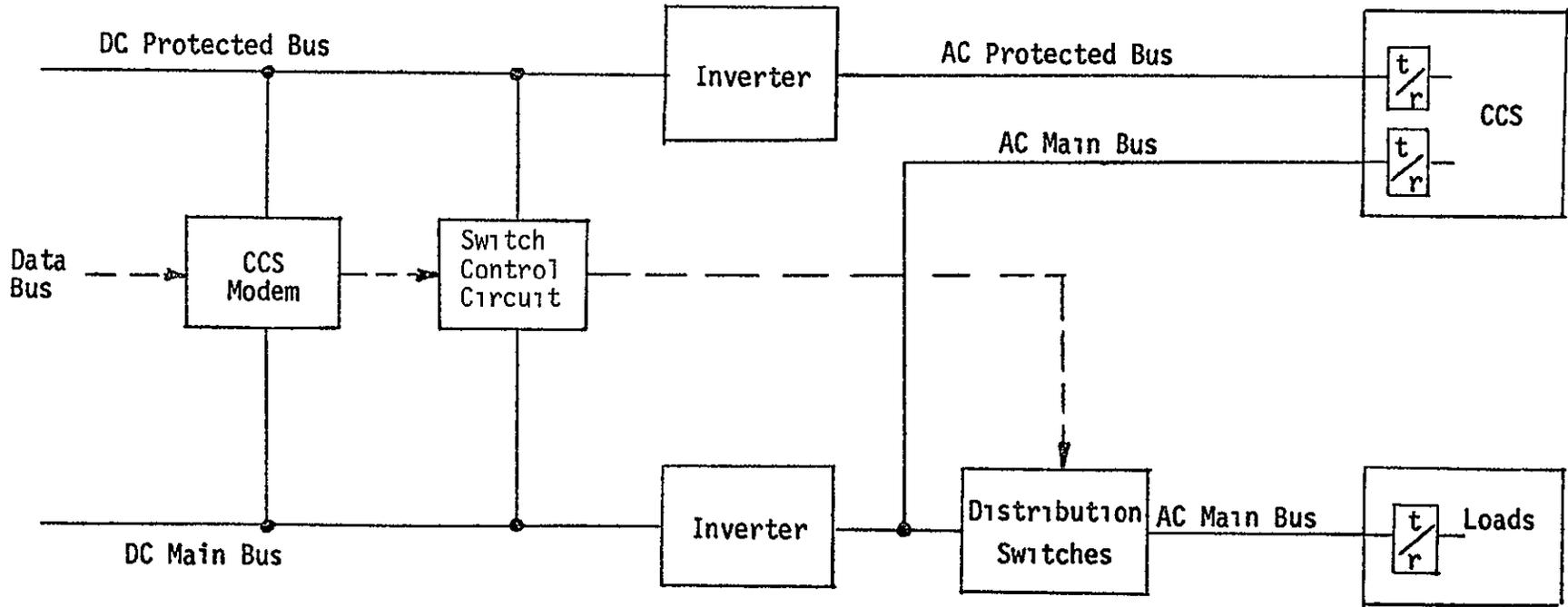


FIGURE 3-14

AC DISTRIBUTION CONCEPT

circuits, both of which can be considered as remote extensions of CCS (Note It would be pointless to guarantee power to CCS with the use of the protected bus concept unless CCS could perform meaningful actions Switch actuations represent these meaningful actions and therefore protected bus power must be made available for the switch elements as well as all other intermediate processing functions ) As shown in the figure the switches themselves are contained in the PCE They control main bus power to the main and standby loads The fault detection function for transferring from the main to the standby load are not shown These would presumably involve status monitors which measure the performance of the particular load in question and relay their information to CCS CCS then acts on this information and produces switching signals as required The extent to which protected bus power might be required by such status monitors has not been determined This is considered to be an aspect of overall system integration requiring a detailed knowledge of the various spacecraft loads, their failure modes, and the particular techniques used for fault detection

Configuration B Critical redundant load, power switching at load

Functionally this system is identical to that described above with the modems, switch control circuits, and switches located at each load (or subsystem grouping of loads) Protected bus power must now generally be distributed to the various loads The routing of this bus through

the spacecraft harness decreases its reliability. In addition, separate modems would be required for each load. These could also serve to relay the outputs of status monitors that might be located at the loads.

Configuration C Non-Critical load, switching at PCE

This implementation is the same as Configuration A except that no redundant element is used.

Configuration D Non-Critical load, switching at load

Same as Configuration B without a standby load.

Configuration E This arrangement pertains specifically to the CCS and suggests a possible distribution of main and protected bus power to the redundant elements within CCS. It is contemplated that no switching elements would be used since CCS must be utilized at all times.

Fuse protection is indicated for some of the configurations. These are not intended to represent firm recommendations and are only shown as being potential applications for this relatively uncomplicated form of fault protection. The fuses are principally intended for protection against harness faults and are used only where the location of switches prevent their use for clearing harness faults. Thus, in general, fuses are not applied where power control occurs within the PCE. A further restriction on fuses was to consider their use with only those critical

loads having standby replacement capability. The same general rules might also apply to non-critical loads with switch control at the PCE; no fuses would be used, whereas they might with loads not having control switches or where the switches are remotely located from the PCE bay.

## 2 AC Distribution Variations (Figure 3-16)

As shown in the figure, inverters are required for the main and protected busses. Standby redundancy is applied for the main bus inverter since a single failure could result in a total mission loss. No redundancy is used on the protected bus inverter since the bus itself is a redundant source of power for the CCS and its associated functions (modems and switch control circuits). The modem and switch control circuits contained within the PCE are similar to that described for the DC case. They operate from the regulated DC bus. Besides controlling load switching functions they also transfer the main inverter to its standby unit in the event of a failure. This would occur through the normal diagnostic capability of the CCS rather than through an inverter dedicated fault sensor. The power control configurations are similar to those described for the DC case.

### Configuration A Critical redundant load, power switching at PCE

Same as for DC case except transformer-rectifiers are substituted for DC to DC converters.

Configuration B Critical redundant load, power switching at load

Besides the substitution of transformer-rectifiers for DC to DC converters, additional transformer-rectifiers are required to operate the CCS modem and switch control circuits. This implementation thus appears to result in additional complexity.

Configuration C Non-critical load power switching at load

Same as DC case

Configuration D Non-critical load power switching at load

Same as configuration B above without redundancy

CONCLUSIONS

Either AC or DC distribution appears suitable for TOPS. From the standpoint of weight and efficiency DC distribution has a slight edge since fewer transformation stages are required. The AC method on the other hand provides flexibility which permits changes in loads and voltage levels with relative ease. All in all no dominant factor was identified which would indicate a strong preference of one method over the other.

An examination of power control implementation for the two methods indicated a preference for locating switching elements within the PCE bay which results in the following advantages:

- Fewer modem units are required since a single modem in the PCE can accommodate all of the power control switches.

- Fuses for harness protection can be eliminated since the switch elements in the PCE can provide the necessary protection
- General distribution of the protected bus is minimized

The disadvantage of centrally located switches results from additional harnessing (separate lines are required from each switch to its associated load) and the possibility of increased interface complexity. The switching logic of certain loads, for example, may be so intimately associated with the internal circuitry of the load that central location of power control switches is impractical.

Comparing AC and DC with respect to the power control implementation, complexity is about equivalent for the two cases if the switching elements are centrally located. If the switches are distributed throughout the system, the AC system appears to be more complex since additional transformer-rectifiers are required to operate the switching elements besides those required for the loads.

#### 3 3 4 Power Switching Studies

The development of switching devices is discussed under Technology Development, paragraph 3 4. Table 3-9 summarizes the principal comparison factors for (1) saturable reactor switches, (2) transistor switches, (3) mechanical relay switches.

#### CONCLUSIONS

No particular recommendations are forthcoming from this switching study. The results are mainly a "catalog" of switching circuit configurations from which appropriate selections may be made.

TABLE 3-9

COMPARISON OF SWITCHING DEVICES

FACTOR	EVALUATION				
	SATURABLE REACTOR	TRANSISTOR SWITCH		RELAY SWITCH	
	SINGLE	SINGLE	QUAD	SINGLE	QUAD
POWER EFFICIENCY, %	95*	97	94 4	99 9	99 9
WEIGHT, POUNDS	4*	09	25	125	25
RELIABILITY (10 YEARS)	9917*	9762	.9992	8259	9268
POWER TYPE	AC	DC	DC	AC/DC	AC/DC
COMMAND RETURN ISOLATION	YES	NO	NO	YES	YES
MAGNETIC EFFECTS	SLIGHT	NO	NO	YES	YES
R AMP CAPABILITY	POSSIBLE	YES	YES	POSSIBLE	POSSIBLE

\* DOES NOT INCLUDE COMMAND CIRCUITRY

### 3 4 Technology Development

The following sections report on the status of technology developments undertaken thus far in the program. For the most part these developments concern circuit designs for the various power conditioning elements, and tests of functional performance both singly and in a subsystem configuration. These designs have been perfected to a breadboard demonstration stage and were delivered. Together with the system definition activity, these results of the technology development effort will serve to define realistic PCE hardware requirements and capabilities in a later phase of the TOPS program.

To provide some perspective, the technology developments are discussed as they relate to each functional block of the PCE. Thus, switch developments are discussed as part of the Power Distribution Assembly since the majority of these switches will be contained in that assembly. A summary of the presently defined function and design approach for each functional block precedes the technology status discussion.

#### 3 4 1 Power Distribution Assembly

##### Function

- Houses power control switching devices
- Number of switching circuits 80
- Type power  
(typical) 30 VDC  
50 VAC, 4096 Hz
- Switch ratings up to 5 amperes

- Control signal 5 VDC, Transistor-Transistor Logic (TTL)  
30 Millisecond pulse
- Protective features Current trip  
Redundant make and break
- Transient suppression Ramp-on and  
Ramp-off features  
Noise immunity

#### Approach

- Analyze AC and DC switching circuitry features
  - Redundancy
  - Ramp turn-on
  - Ramp turn-off
  - Overcurrent limit
  - Overcurrent trip

#### Activity

- A quad relay switch, applicable to AC and DC distribution, with an overcurrent trip was built, tested and delivered
- A quad semiconductor switch, applicable to DC only, with an overcurrent trip was built, tested and delivered
- An AC static switch foldback current limited, with a saturable reactor control was built and tested, and a silicon controlled rectifier circuit was designed. These circuits did not demonstrate desirable characteristics and were abandoned

#### Status

- Requirements for toggle command have been deleted.

- Requirement for overcurrent limit has been deleted
- Quad relay and semiconductor switches with overcurrent trip protection for use with AC and DC power were built, successfully tested and delivered. Results are discussed in Appendix D
- A saturable reactor AC static switch with current limiting was breadboarded and tested

### 3 4 2 Shunt Regulator Assembly

#### Function

- Maintains constant RTG operating conditions by regulating voltage and absorbing excess power
- Regulation 30 VDC  $\pm 1\%$
- Excess power 270 watt capability has been built, tested, and delivered  
Most recent requirement is 310 watts—
- Losses (with no shunting) 0.5 watts
- Dynamic impedance 0.1 ohms (0 to 1 MHz)
- Transient response Recover to within regulation in one millisecond for a step load change of 270 watts

#### Approach

- Develop and test a breadboard shunt regulator with emphasis on quad redundancy features i.e., a design that can accept either a short or open of any single part

- The quad shunt regulator built and tested in the previous quarter was delivered. The results of recent interaction testing with the TWT converter is discussed in Appendix E.

### 3.4.3 TWT Converter Assembly

#### Function

- Provides DC to DC conversion of electrical power to satisfy traveling wave tube requirements
- Input voltage 30 VDC  $\pm 1\%$
- Output voltage
  - Helix 3400 to 3500 VDC, settable within  $\pm 2\%$ , regulation  $\pm 0.5\%$ , ripple 1.0 volt peak to peak
  - Collector 1425 to 1525 VDC, settable within  $\pm 5\%$ , regulation  $\pm 1.0\%$ , ripple 2.0 volts peak to peak
  - Anode 100 to 400 VDC, settable within 5.0 volts, regulation  $\pm 1.0\%$ , ripple 1.0 volt peak to peak
  - Filament, 5.0 to 5.5 volts rms, settable within 0.1 volts, regulation  $\pm 3.0\%$
- Current
  - Helix 2 to 5 milliamperes
  - Collector 43 to 48 milliamperes
  - Anode 0.2 milliamperes
  - Filament 220 milliamperes with a 400 milliampere limit

- Operation required through decrease from atmospheric pressure to deep space vacuum

#### Approach

- Develop and test a breadboard unit with emphasis on transformer design and fabrication techniques, and the high voltage series regulators
- Demonstrate ability of critical electronic piece parts to survive the expected radiation environment

#### Status

- Circuit designs were developed for the TWT converter and reported previously
- Eight transformer configurations have been built and tested with varying degrees of success. Latest version shows satisfactory operation and high efficiency. Overall supply efficiency of near 90% was obtained through use of a supermalloy material cut core for the output transformer in place of the originally used silicon material
- Three series regulator circuits have been built and tested. Improvements in converter filter characteristics were implemented to attenuate the input ripple to the series regulators

- Complete functional performance has been demonstrated
- The breadboard circuitry was tested with the breadboard shunt regulator
- Circuits have been delivered
- The series pass transistor of the high voltage regulator has been exposed to a radiation dose greater than expected for the TOPS mission, and degradation was within acceptable limits. Test results and discussion is included in Appendix B

#### 3 4 4 Two-Phase Inverter Assemblies

##### Function

• Provides conversion from DC to two Phase AC for gyros and momentum wheels		
• Requirements	<u>GYROS</u>	<u>WHEELS</u>
Power rating, continuous	12 watts	12 watts
Power rating, peak	20 watts	12 watts
Frequency	1600 Hz	400 Hz
Electrical configuration	3 wire	4 wire
Command logic	5 v TTL	5 v TTL
Phase reversal	No	Yes
Inhibit override	None	200 ms pulses
Free run	Yes	Yes
Output isolation	Yes	Not required

	<u>GYROS</u>	<u>WHEELS</u>
Output voltage	25 VAC <u>+5%</u>	26 VAC <u>+5%</u>
Free run frequency	1590 Hz+0, -4%	396 Hz +0 -4%
Frequency stability	$\pm 0$ 5%	Not required

### Approach

- Develop, test and deliver breadboard inverters (1 each for gyros and momentum wheels)

### Status

- A breadboard unit was built and tested to the requirements defined early in the program. No unique technology problems were identified. Two designs have been developed, built, and tested to the requirements described above, and were delivered.

## 3 4 5 AC Power Conditioners

### Function

- Two steps are involved
  - (1) Invert power from regulated DC to AC for general distribution to the loads
  - (2) At each load, transform and rectify to multiple voltage levels
- Inverter input voltage 30 VDC +1%
- Inverter output voltage tentatively at 50 volts rms, square wave, 4096 Hz
- Inverter to free run with loss of timing signal

Approach

- Build and test one inverter and three transformer-rectifiers for purposes of comparing weight, efficiency, and electrical performance with the DC to DC converters. The inverter and the transformer-rectifiers are to be built at JPL and are to furnish the loads listed in Table 3-10.

Status

- No activity to report.

TABLE 3-10  
AC POWER CONDITIONING REQUIREMENTS

INVERTER	TRANSFORMER-RECTIFIER	OUTPUT VOLTAGE	PERCENT REGULATION	POWER WATTS
Input Voltage 30 VDC $\pm 1\%$	No 1 Science Data Subsystem	+5	+10	15 75
		+15	$\pm 5$	1 5
		-15	$\pm 5$	1 5
Output Voltage 50 VAC RMS $\pm 2\%$ square wave	No 2 DC Magnetometer Experiment	+25	+0 5	1 2
		+5	$\pm 5$	625
		+5	$\pm 0 1$	025
		-5	$\pm 0 1$	025
		+12	$\pm 5$	600
		-12	$\pm 5$	600
Output Power 6 watts minimum 60 watts maximum	No 3 Tracking Receiver	+6	+2	2 0
		-6	$\pm 2$	2 0
		+15	$\pm 2$	2 0
		-15	$\pm 2$	2 0
Output Frequency 4096 Hertz $\pm 5\%$				

### 3 4 6 DC Power Conditioner Assemblies

#### Function

- Convert from regulated 30 VDC to user voltage levels
- Separate converters to be used at each load or functional load group
- All switching frequencies to be synchronized by single clock signal
- Converters to free run with loss of timing signal

#### Approach

- Build and test three converters for comparison of weight, efficiency, and electrical performance with inverters and transformer-rectifiers  
Loads are to be as shown for Task 3 4 5

#### Status

- The electronic portion of the converter has been packaged using thick film microcircuitry techniques. Three such "flat pack" units have been built and functional tests were performed demonstrating feasibility. No further effort will be expended on the flat-pack technology.
- The three converters for comparison with inverters and transformer-rectifiers were built and tested using discrete piece part packaging methods. These breadboards were delivered at the conclusion of subsystem testing.

1 August 1970

### 3 4 7 Power Source and Logic Assembly

#### Function

- Houses RTG isolation diodes, telemetry conditioning circuitry, and fault detection circuitry

#### Approach

- Design and build breadboards of unique circuit elements, such as current monitors and fault detection circuits

#### Status

- Low Voltage Cut Off and current sensor circuits have been built, tested, and delivered

### 3 4 8 Subsystem Tests

These tests were conducted to demonstrate the power system design concept and interaction between equipments using the breadboard assemblies of specific components. Electrical testing is complete and the breadboards have been delivered.

### 3 4 9 Bench Test Equipment

The requirement for design, fabrication, and delivery of bench test equipment has been deleted.

#### SECTION 4 CONCLUSIONS

The early phases of this program have been concerned mostly with analysis of system requirements, configuration studies to determine the optimum arrangement of equipment, and the development of circuits and devices to meet the extended life requirement of the TOPS mission. Concerning this aspect of the program, the principal conclusions are that no severe technological problems associated with extended life capability have been encountered, and circuit redundancy techniques are practical and have been applied successfully to solid-state and relay switching devices, and to the shunt regulator.

Emphasis has been placed on AC distribution as a result of a JPL project decision. A main and protected bus concept has been developed which assures that power will be available to the Central Computer Subsystem in the event of any load or source fault.

Alternative shunt regulator concepts were examined in consideration of the dissipation that can be accepted by the PCE bay, and based on this thermal burden limitation a sequence shunt appears to offer the most suitable characteristics.

Long-term flight batteries for TOPS appear neither necessary nor desirable. The principal benefit of batteries would be to reduce turn-on voltage transients. It is considered that other less complex techniques can be used to relieve such transients. Additionally, the weight penalty of battery averaging is at least four times as great as increasing the RTG size to provide direct power, thus the use of batteries for power averaging does not appear to be justified.

Launch batteries to augment limited on-pad RTG capability were evaluated. As a result of the complexity introduced, their use is discouraged, and a preference for on-pad RTG capability has been indicated. A converter for the TWT was completed and successfully tested, demonstrating capability to meet the functional requirements.

The most radiation sensitive transistor in the circuits under consideration is the High Voltage Series regulator pass transistor in the traveling wave tube converter. This selection was made on the premise that the results of increased leakage current could not be compensated for easily by device selection or device change. The results of radiation testing, however, demonstrated that the open emitter leakage current did not increase significantly and that gain degradation actually caused a decrease in the open base leakage current. The conclusion is that radiation sensitivity of all electrical piece parts must be considered carefully, but that adequate designs can survive the expected radiation.

SECTION 5      NEW TECHNOLOGY

No items of new technology have been identified during the period covered by this report

SECTION 6 REFERENCES AND BIBLIOGRAPHY

- 1 Statement of Work, Contract No 952536, Modification No 1, dated 27 June 1969
- 2 Statement of Work, Modification No 4, revised 20 November 1969
- 3 Statement of Work, Modification No 4, revised 5 December 1969
- 4 Design Requirements and Constraints for Thermoelectric Outer Planet Spacecraft (TOPS), Power Subsystem dated 24 April 1969
- 5 TOPS Mission Objectives and Design Criteria No TOPS-2-100 dated 17 February 1969
- 6 TOPS-1-100 Functional Requirements, Thermoelectric Outer Planet Spacecraft, 12 December 1969
- 7 TOPS-3-100 TOPS Spacecraft Characteristics and Restraints, June 25, 1969
- 8 TOPS-3-110 Functional Req , TOPS Functional Block Diagram, June 5, 1969
- 9 TOPS-3-180 Functional Req , TOPS Spacecraft Configuration, June 5, 1969
- 10 TOPS-3-190 Functional Req , TOPS Structural Design Criteria, June 12, 1969
- 11 TOPS-3-190 Functional Req , TOPS Structural Design Criteria, October 14, 1969
- 12 TOPS-3-210 Functional Req , TOPS Design Criteria for Spacecraft Temperature Control, June 10, 1969
- 13 TOPS-3-210 Functional Req , TOPS Design Criteria for Spacecraft Temperature Control, October 14, 1969
- 14 TOPS-3-220 Functional Req , TOPS Electronic Packaging, June 1, 1969
- 15 TOPS-3-230 Functional Req , TOPS Equipment and Weight List, June 4, 1969
- 16 TOPS-3-250 Functional Req , TOPS Power Profile and Allocation, June 16, 1969

- 17 TOPS-3-250 Functional Req , TOPS Power Profile and Allocation,  
24 November 1969
- 18 TOPS-3-270 Functional Req , TOPS Spacecraft Data Handling, May 29, 1969
- 19 TOPS-3-290 Functional Req , TOPS Spacecraft Ground Command and CC&S  
Command Structure, June 4, 1969
- 20 TOPS-4-2001 Functional Req , TOPS Flight Equipment Structure Subsystem,  
10 September 1969
- 21 TOPS-4-2004 Functional Req , TOPS Power Subsystem, June 10, 1969
- 22 TOPS-4-2007 Functional Req , TOPS Flight Equipment Attitude Control  
Subsystem
- 23 TOPS-4-2010 Functional Req , TOPS Flight Equipment Propulsion Equipment,  
23 September 1969
- 24 TOPS-4-2011 Functional Req , TOPS Temperature Control Subsystem,  
14 October 1969
- 25 TOPS-4-2015 Functional Req , TOPS Flight Equipment Attitude Propulsion  
Subsystem, 10 December 1969
- 26 TOPS-4-2017 Functional Req , TOPS Flight Equipment S/X Band Antenna  
System, 14 October 1969
- 27 TOPS-4-2018 Functional Req , TOPS Meteoroid Protection Subsystem,  
15 October 1969
- 28 TOPS Functional Block Diagram, Interoffice Memo 292-69-592 dated  
31 October 1969
- 29 System Guidelines for Design of TOPS Power Conditioning Equipment,  
Interoffice Memo 292-70-603 dated 14 January 1970

- 30 TOPS Power Profile dated 21 March 1968
- 31 TOPS Power Subsystem Requirements dated 10 April 1969
- 32 Power Profile dated 27 June 1969
- 33 TOPS Power Subsystem Requirements dated 8 July 1969
- 34 Power Profile and Allocation dated 4 August 1969
- 35 Voltage Distribution of Loads, Preliminary, Prepared August 1969
- 36 RTG Power Requirements by Mission Phase dated 20 October 1969
- 37 The Effect of TOPS Power Distribution Methods on Magnetic Field Experiments, Interoffice Memo dated 21 August 1969
- 38 Load Criticality List (TOPS) dated 1 August 1969
- 39 Power Switching and Diagnostic/Corrective Action Computation Priorities, Interoffice Memo 292-69-579 dated 18 September 1969
- 40 TOPS Flight Sequence 20 March 1969
- 41 TOPS Flight Sequence 31 March 1969
- 42 TOPS Electronic Packaging Preliminary Layout dated 1 October 1969
- 43 Guidelines for Magnetic Control of TOPS Hardware, by J G Bastow, 23 May 1969
- 44 Performance Characteristics of a Silicon-Germanium RTG in Long-Term Operation dated 29 April 1969
- 45 Traveling-Wave Tube Amplifier Power Supply, Detail Specification for, dated 11 December 1969
- 46 TOPS Power Switching, by Dean Anderson, dated 22 September 1969
- 47 Computational Requirements of the Power Subsystem, Interoffice Memo 342-69-A-464, dated 12 August 1969
- 48 Computational Requirements of the Power Subsystem, Preliminary, dated 17 December 1969

- 49 Solid State Relay, Interoffice Memo 342-69-A-468 dated 13 August 1969
- 50 A Redundant Shunt Regulator Concept, dated 18 December 1969
- 51 Baseline Attitude-Control Subsystem for the Thermoelectric Outer Planet Spacecraft, by W E Dorroh, JPL Space Programs Summary 37-58, Vol III, pages 117-121
- 52 TOPS Recommended Parts Failure Rate Data dated 10 April 1969
- 53 Preferred Parts List JPL Spec ZPP-2061-PPL-K dated 1 July 1969
- 54 Candidates for the TOPS Recommended Parts List dated 31 December 1968
55. Screening Requirements for Electronic Parts, General Specification dated 25 April 1966
- 56 Quality Control Requirements, Preliminary, received 16 July 1969
- 57 Failure Rate for Mariner Mars Power System Study
- 58 Mariner Mars 1969 Electrical Interface and Electrical Grounding dated 25 September 1968
- 59 Mariner Mars 1969 Electrical Interface and Electrical Grounding, 29 February 1968
- 60 Major System Design Problems for Deep Space Probes by William J Dixon AIAA Paper No 66-887 December 1967
- 61 To the Outer Planets by James E Long, Astronautics and Aeronautics - June 1969
- 62 Design of an Unmanned, Automated Spacecraft for the Grand Tour by L E Hove, IAF Paper No AS45 October 1968
- 63 Earth-Based Navigational Capabilities for Planetary Missions by T W Hamilton, AIAA Paper No 68-852 - August 1968

- 64 Trajectory Analysis of a Grand Tour Mission to the Outer Planets  
by Louis Kingsland, Jr , AIAA Paper No 68-1055 - October 1968
- 65 Automatic Maintenance of Aerospace Computers and Spacecraft  
Information and Control Systems, by Avizienis, Mathur, Rennels and  
Rohr
- 66 TOPS Power Subsystem Development Program dated 20 November 1969
- 67 An Unorthodox Transformer for Free-Running Inverters, by Francis C  
Schwartz, 4 August 1969
- 68 AC Current Limiters, Wilorco, Inc , dated 27 June 1969
- 69 Bi-Weekly Progress Review Meeting Minutes - 8 May 1969
- 70 Minutes of an Informal Meeting at ERC - 14 May 1969
- 71 Bi-Weekly Progress Review Meeting Minutes - 26 May 1969
- 72 Bi-Weekly Progress Review Meeting Minutes - 12 June 1969
- 73 Bi-Weekly Progress Review Meeting Minutes - 1 July 1969
- 74 Bi-Weekly Progress Review Meeting Minutes - 14 July 1969
- 75 Bi-Weekly Progress Review Meeting Minutes - 4 August 1969
- 76 Bi-Weekly Progress Review Meeting Minutes - 19 August 1969
- 77 Bi-Weekly Progress Review Meeting Minutes - 16 September 1969
- 78 Bi-Weekly Progress Review Meeting Minutes - 6 October 1969
- 79 Bi-Weekly Progress Review Meeting Minutes - 22 October 1969
- 80 Bi-Weekly Progress Review Meeting Minutes - 5 November 1969
- 81 Bi-Weekly Progress Review Meeting Minutes - 11 December 1969
- 82 Bi-Weekly Progress Review Meeting Minutes - 19 February 1970
- 83 Document 1030-26, Specification for Research and Advanced Development  
Technical Reports prepared by JPL Contractors, dated 1 June 1969

- 84 Specification for R&D Technical Reports Document 1000-8 dated  
1 January 1967
- 85 ERC/JPL Agreement for Power Processing Support of the TOPS Project  
dated 17 April 1969

APPENDIX A TURN-ON TRANSIENT ANALYSIS

Tests on the shunt regulator demonstrated that the rate of load change that could be furnished within the allowable bus deviation of plus or minus 300 millivolts was in the order of 60,000 amperes per second as shown in Figures A-1 and A-2. To control the load to this rate of change of current, passive filters consisting of single LC sections are adequate by inspection of nominal values, but must be closely investigated in the application.

The value of inductance required to control the rate of rise of current to the load under a suddenly applied voltage step can be determined from the expression

$$L \geq \frac{dv}{di/dt}$$

where

$dv$  = the step voltage applied to the load, 30 volts

$L$  = value of inductance in henries

$di/dt$  = maximum allowable rate of change of current, 60,000 amperes per second

With these limiting values, the minimum value of inductance required is

$$L \geq \frac{30}{60,000} = 0.0005 \text{ Henry}$$

Figure A-3 shows the relative impedance of LC combinations, and allows selection of filter parameters to

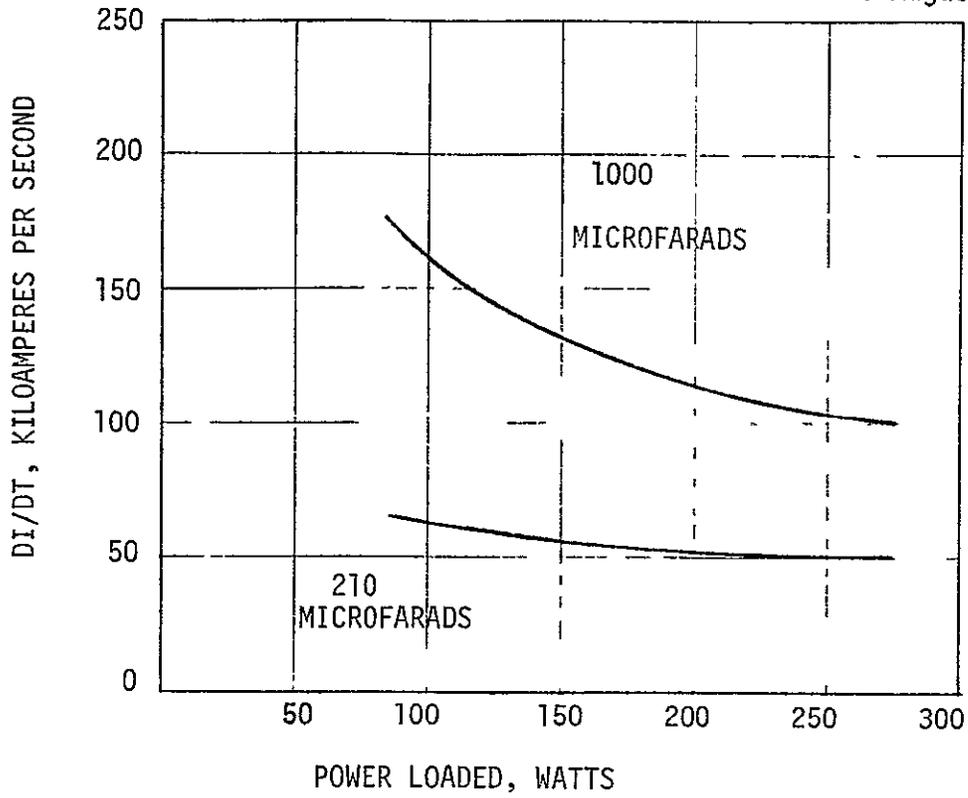


FIGURE A-1 ALLOWABLE POWER LOADING

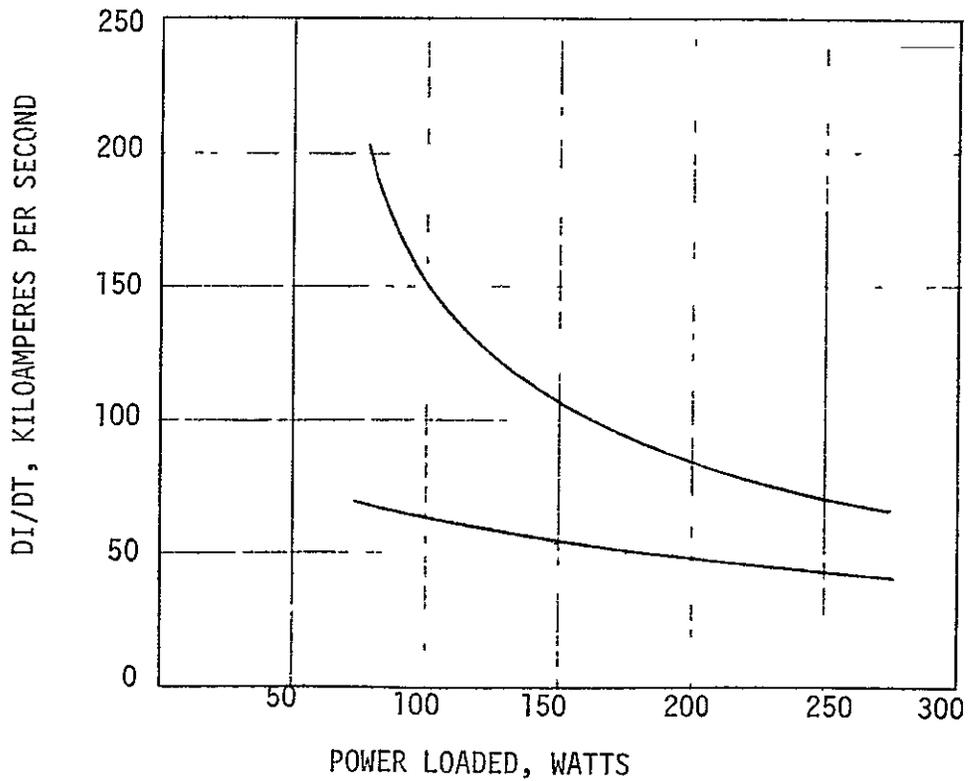


FIGURE A-2 ALLOWABLE POWER UNLOADING

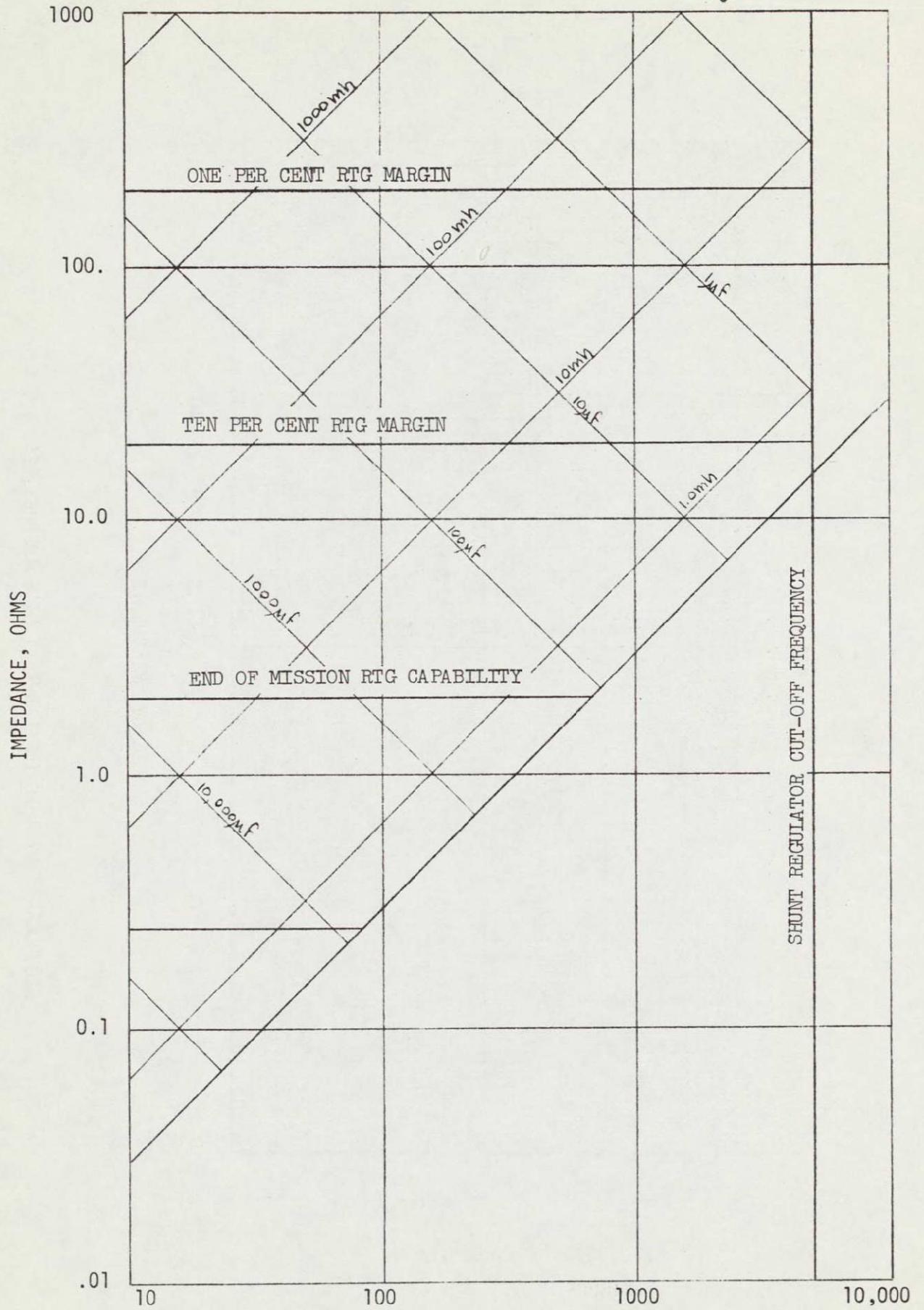


FIGURE A-3 IMPEDANCE CHART

A-4

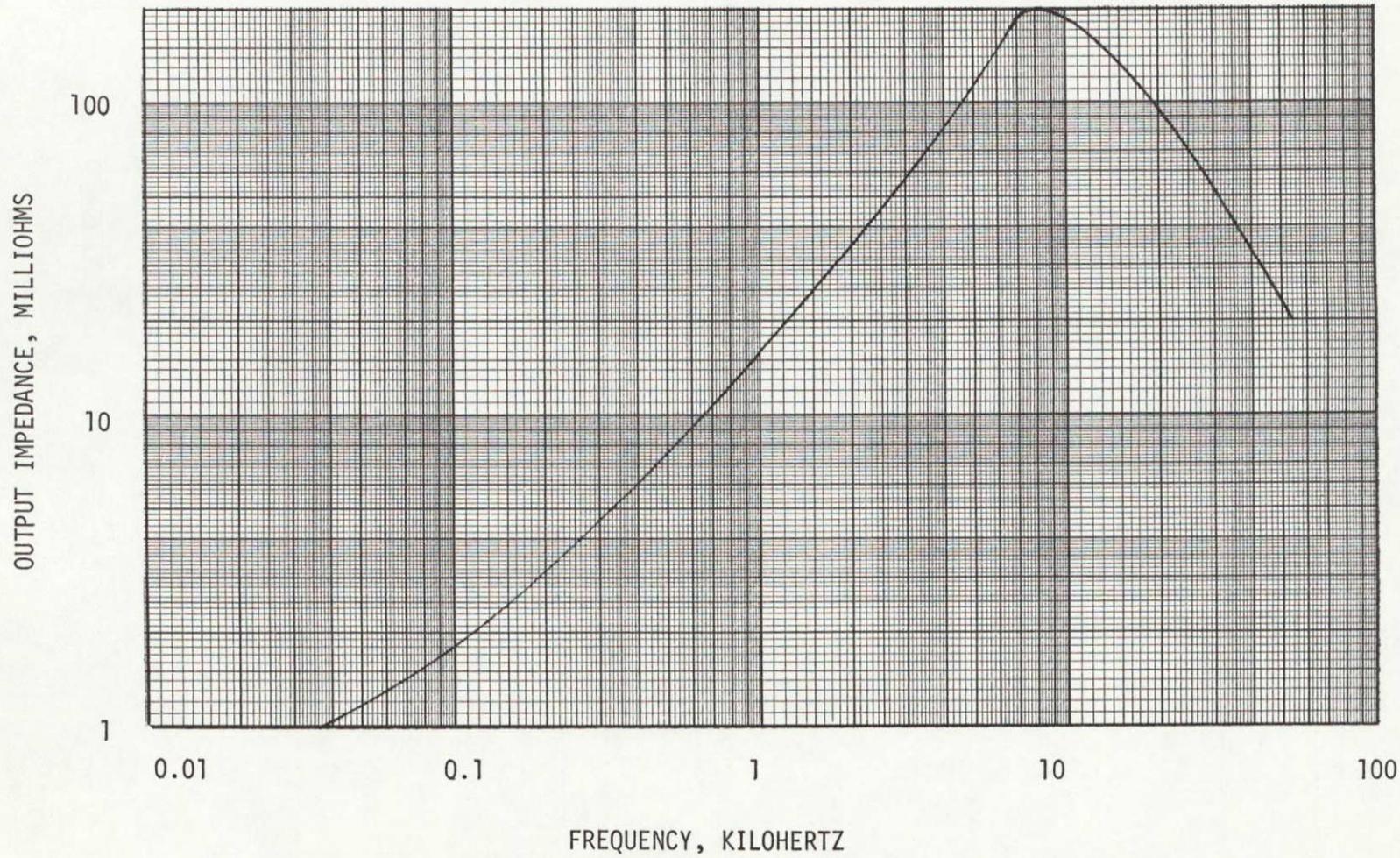


FIGURE A-4 DYNAMIC IMPEDANCE AT NINE AMPERES, 210  $\mu$ F

1J86-TOPS-555  
1 August 1970

- 1 Control the rate of rise of current
- 2 Provide low source impedance of DC current
- 3 Provide low shunt impedance of AC current
- 4 Minimize transient overshoot

A lower limit on inductance has been established as shown on Figure A-3 at 0.5 millihenries to control the rate of rise of current under a step load change. The shaded area above 5000 hertz is to preclude filter resonance in the region of high impedance of the shunt regulator shown on Figure A-4.

The impedance at DC is the sum of the effects of the shunt regulator static regulation, distribution harness losses, and series resistance of the inductor. The shunt regulator impedance at low frequency is less than one milliohm, as shown on Figure A-4.

The optimum current density in the distribution harness on a minimum weight spacecraft can be determined by a trade-off of wire weight to reduce losses against RTG weight to make up the watts that would be lost in a lighter weight distribution system.

The resistance of a conductor can be expressed as

$$R = \sigma l / A \quad \text{where}$$

R = resistance in ohms  
 $\sigma$  = resistivity of the material, ohm-inches<sup>2</sup>/inch  
l = length of the conductor  
A = cross-sectional area, inches<sup>2</sup>

The electrical losses in a length of conductor at a current level I are then

$$\text{Watts} = I^2 R = \sigma l I^2 / A$$

and the weight of this same piece of conductor can be expressed as

$$\text{Weight} = \rho l A \quad \text{where}$$

$$\begin{aligned} \rho &= \text{specific weight, pounds per cubic inch} \\ l &= \text{length, inches} \\ A &= \text{cross-sectional area, inches}^2 \end{aligned}$$

Obviously the loss in watts can be reduced by adding cross-sectional area, and consequently weight. The optimum current density for the minimum weight spacecraft can be determined when the watts saved by adding one pound of conductor are equal to the watts per pound trade-off figure for the vehicle

$$\text{New watts} = \sigma l I^2 / (A + dA)$$

$$\text{delta watts} = \frac{\sigma l I^2 (A + dA - A)}{A(A + dA)} = \frac{\sigma l I^2 dA}{A(A + dA)}$$

$$\text{new weight} = \rho l (A + dA)$$

$$\text{delta weight} = \rho l (A + dA - A) = \rho l dA$$

$$\frac{\text{delta watts}}{\text{delta weight}} = \frac{\sigma l I^2 dA}{\rho l A dA (A + dA)} = \frac{\sigma I^2}{\rho A (A + dA)} \quad \text{and rearranging,}$$

$$\frac{\sigma I^2}{\rho (A^2 + AdA)} = \frac{\text{delta watts}}{\text{delta weight}} \quad \text{and in the limit as } dA \text{ approaches zero,}$$

$$\frac{I}{A} = \sqrt{\frac{\rho}{\sigma} \frac{\text{delta watts}}{\text{delta weight}}} = \text{optimum operating current density,}$$

in amperes per square inch of cross sectional area of conductor, where delta watts/delta weight is the available watts per pound of RTG for the TOPS vehicle, presently 1.7 watts per pound, the resistivity of copper is approximately  $0.68 \times 10^{-6}$  ohm-inches<sup>2</sup>/inch, and the specific weight of copper is 0.32 pounds per cubic inch

$$\text{Operating current density} = \sqrt{\frac{0.32 \times 1.7}{0.68 \times 10^{-6}}} = 894 \text{ amps/inch}^2$$

The AWG wire contemplated for TOPS with a cross-sectional area of  $125 \times 10^{-6}$  square inches should be operated at 894 amps/inch<sup>2</sup> multiplied by  $125 \times 10^{-6}$  inches<sup>2</sup>, or approximately 112 milliamperes. In those exceptional cases where AWG 24 wire is allowed, the optimum current density of 894 amperes per square inch provides an operating current of 284 milliamperes.

The result of the distribution design analysis is a safe, reliable, minimum weight, minimum power loss distribution system within the principal design constraint of minimum weight or minimum voltage drop.

The distribution harness resistance per foot of round trip wire length can be obtained from Figure A-5. This was calculated based on wire data per MIL-W-81044/3, reproduced in Table A-1.

TABLE A-1

HOOK-UP WIRE DATA				
AMERICAN WIRE GAUGE	AREA, SQUARE MILS	OHMS PER THOUSAND FOOT RESISTANCE	POUNDS PER THOUSAND FOOT WEIGHT	ALLOWABLE CURRENT MILLIAMPERES
24	317	23.2	2.1	284
28	125	62.9	0.95	112

The distribution cable is composed of the minimum weight, single size number of strands that can carry the load current without exceeding the optimum current density. A somewhat lighter weight cable could be constructed at some intermediate load current levels by mixing both wire sizes in the same cable, but this refinement was not considered in detail.

The upper limit of operating current is the current that would cause the wire to melt and go to open circuit. These current-time relationships are shown on Figure A-6 which neglects radiation, but using copper resistivity of 1.589 micro-ohms per centimeter cube and a temperature coefficient of resistance of 1/234, determines when the copper will melt at 1083°C in a 40°C ambient.

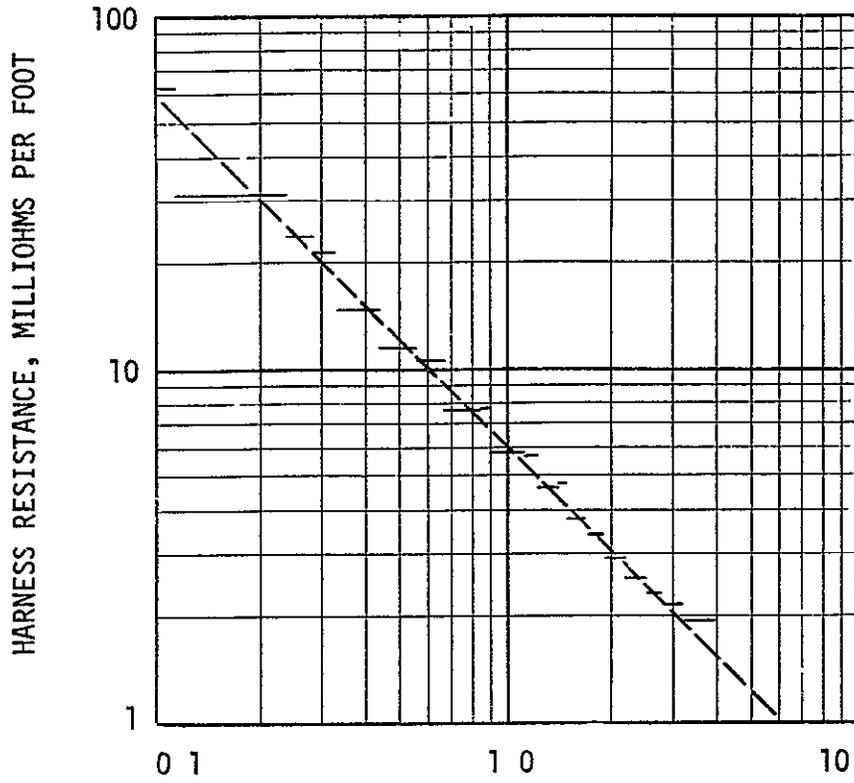


FIGURE A-5 OPTIMUM CABLE RESISTANCE PER FOOT

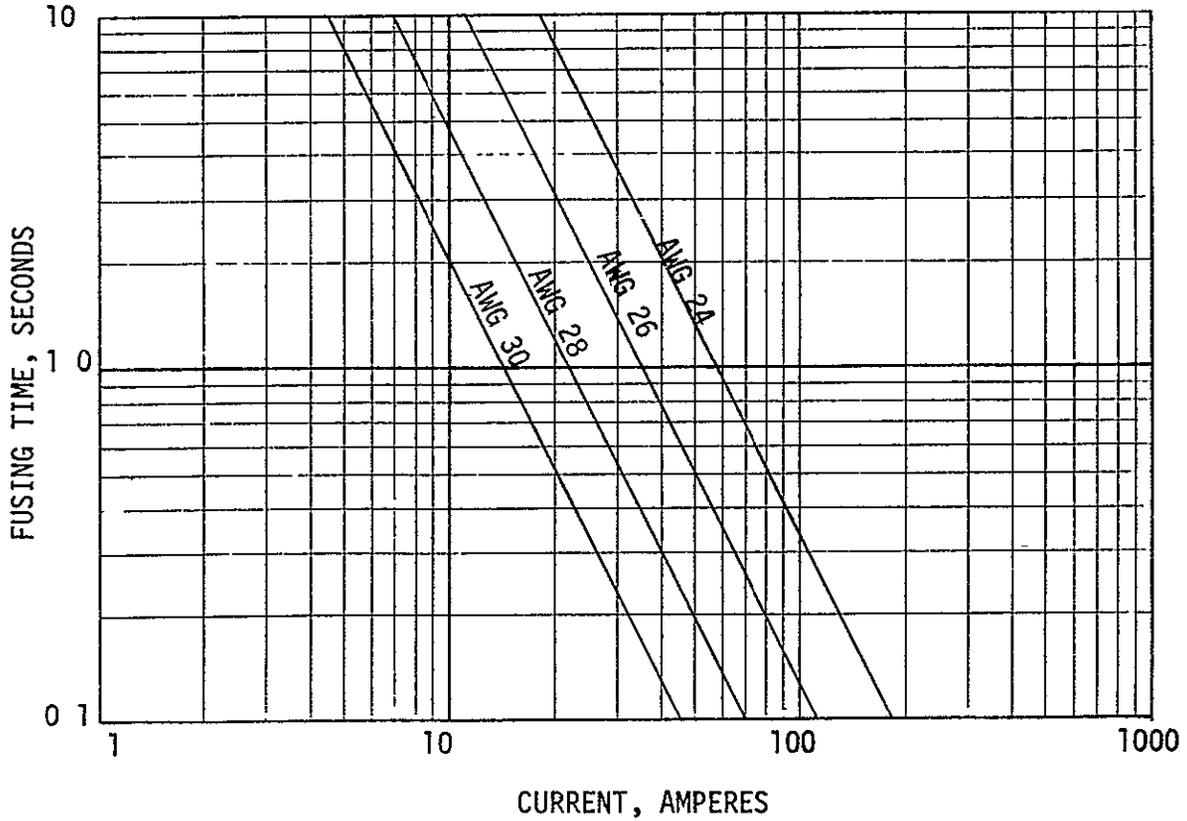


FIGURE A-6 FAULT CLEARING CHARACTERISTICS

The nominal percent harness loss from Table A-2 is 0.024 per foot of round trip length. For power distribution within the electronics bay, runs will average about ten feet, and the total wire resistance will range from twenty to one hundred and twenty milliohms, neglecting connector drops.

The resistance of the inductor will cause a 150 millivolt drop at rated current. This represents a 0.5 percent loss, equivalent to the nominal distribution penalty, and compatible with the regulation of plus or minus one percent.

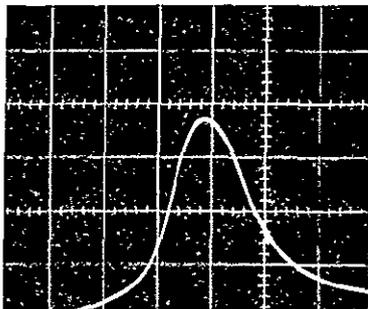
Under actual use conditions during turn-on transients, it was observed that typical inductors did not perform as expected from their AC characteristics. In fact, after a very short interval (approximately 200 microseconds) the inductor saturated from DC magnetization, and the current increased exponentially.

Figure A-7 is an oscilloscope reproduction of the current through the filter inductor at turn-on, with a time base of 200 microseconds per centimeter. It can be seen that the inductor is holding the current to a linear ramp during only the first few hundred microseconds.

The magnetic core of the inductor is made from a pulverized 2% molybdenum, 81% nickel, 17% iron alloy that is annealed, insulated, and pressed into a rigid toroid. The core used for this application has a nominal permeability of 125. The toroid is wound with approximately 14 feet of AWG 20 magnet wire to 108 turns to give a nominal inductance of

TABLE A-2

MINIMUM WEIGHT CABLE				
NUMBER OF WIRES		PER THOUSAND FEET		ALLOWABLE AMPERES
AWG 28	AWG 24	Pounds	Ohms	
1		0 95	62 9	0 112
2	1	1 90	31 45	0.224
3		2.10	23.2	0 283
4		2 85	20 97	0 336
6	2	3 80	15 72	0 448
8		4 20	11 6	0 566
11		5 70	10 5	0.672
13	3	6 30	7.73	0 849
		7 60	7 86	0.896
		8 40	5 8	1 132
11	4	10 45	5 72	1 232
		10 50	4 64	1 415
		12 35	4.84	1 456
8	5	12 60	3 87	1 698
		14 70	3 31	1 981
		16 80	2 9	2 264
6	6	18 90	2.58	2.547
		21 00	2 32	2.83
		23 10	2 11	3 113
4	7	25 20	1 93	3 396



VERTICAL SCALE = 4 amperes per centimeter

HORIZONTAL SCALE = 150 microseconds per centimeter

FIGURE A-7 TURN ON CURRENT TRANSIENT

1.83 millihenries, with minimum and maximum limits of 1.680 and 1.983 millihenries at very low flux densities. Nominal copper resistance of the winding of 0.0103 ohms per foot at 25°C and 0.0133 ohms per foot at 100°C results in a total resistance of 0.1442 to 0.1862 ohms.

The temperature coefficient of inductance is controlled by the addition of small percentages of special alloys, and the maximum expected variation of inductance over the temperature range of 25°C to 100°C is plus or minus 0.1%. The behavior of the temperature characteristic of stabilized cores at high flux density is somewhat different from at low flux density, but any difference is not considered to be significant in this analysis.

At initial turn-on, the bus voltage of 30 VDC is applied as a step function to the input of the filter, and the current will increase from zero with a rate controlled by the applied voltage and the physical and electromagnetic properties of the inductor.

$$E \approx -L \frac{di}{dt} = - \frac{d\phi}{di} \frac{di}{dt} = - \frac{d\phi}{dt}$$

The applied step voltage to the input of the filter results in an opposing time rate of change of flux. In this case, the rate of change of flux with current is non-linear, and the current is time variant. Furthermore, the time rate of change of current is non-linearly dependent on the instantaneous inductance and the rate of change of flux.

A piecewise linear approximation can be made by simplifying to

$$E \approx - \frac{d}{dt} (LI) = - L \frac{dI}{dt} - I \frac{dL}{dI} \frac{dI}{dt}$$

$$E \approx - \left[ L + \frac{dL}{dI} \right] \frac{dI}{dt}$$

In most analyses, the rate change of inductance with current is negligible, but in the case of the turn-on transient, the instantaneous current can go to ten times rated. A nominally one millihenry choke at two amperes has a rate of change of inductance of 0.4 millihenries per ampere, and both terms are significant.

Since the inductance decreases with increasing current, the slope will be approximately that shown on Figure A-8, which was determined by shorting an inductor across the terminals of a constant voltage power supply, and measuring the rate of current rise with a current probe and an oscilloscope.

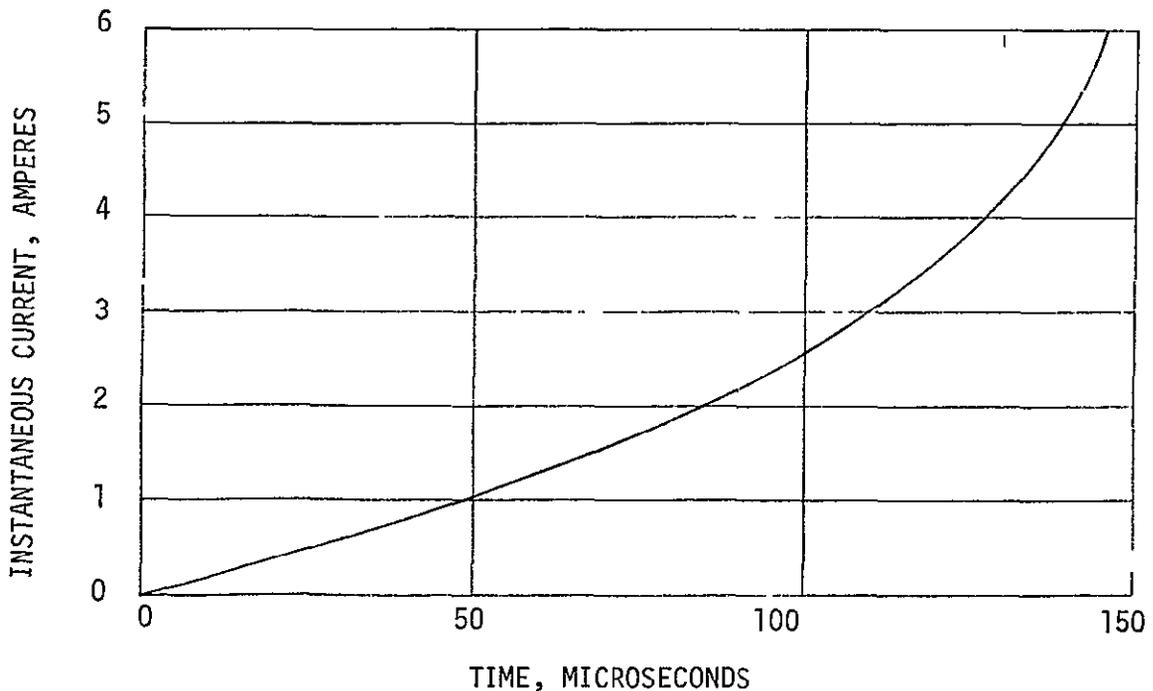
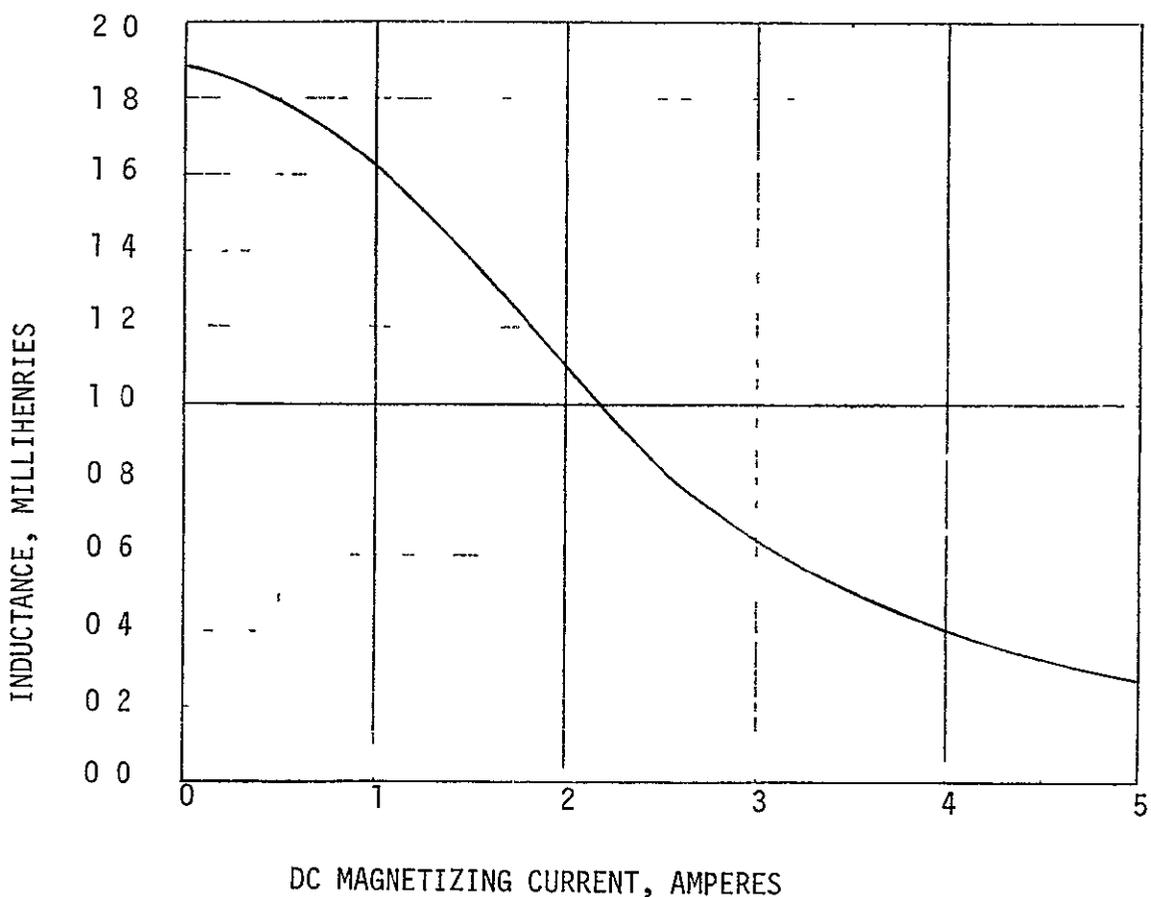


FIGURE A-8 INDUCTOR RESPONSE TO A VOLTAGE

It can be seen that after about 150 microseconds the current exceeds five amperes and the rate of current rise is beyond the control of the inductor if it started from zero. The initial rate of current rise is about fifteen thousand amperes per second.

To determine the inductive reactance, a resistive load was controlled by an AC current modulated transistor. The resulting alternating current voltage across the inductor under test was divided by the peak-to-peak current swing at the same frequency, allowing a determination of the dynamic impedance of the inductor. The DC current level was varied during the test to determine the effects of DC magnetization, and the results are shown on Figure A-9. This same information is available from Figure A-8 by computing the inductance from the time rate of change of current at each value of current.



DC MAGNETIZING CURRENT, AMPERES

FIGURE A-9 APPARENT INDUCTANCE

The maximum unsaturated inductance is nominally 1.83 millihenries, but may fall to a minimum value of  $1.83/125 = 14.64$  microhenries, where the relative permeability of the core material was allowed to degrade to 1, and the device operates effectively as an air core solenoid.

On any electrically excited electromagnetic device there is a voltage induced in each turn. These turns are conductors insulated with a dielectric film, and a turn-to-turn capacity exists. There is a build-up of total voltage from one end of a winding to the other. A maximum voltage exists between these end turns, and if these turns can be kept far apart, the intrawinding capacitance can be reduced.

Low capacitance is obtained by winding in one direction around a fraction of the available core, allowing a uniform build-up of turns but with minimum voltage between adjacent turns. This progressive or bank winding in sectors results in a group of windings in which adjacent turns represent parts of the coil that are close together in voltage, and end turns that are far apart.

The comparative results of a random layer wound inductor and a sector wound inductor are shown on Figure A-10. The total effect of the distributed intrawinding capacity can be considered as a single capacitor shunted across the coil terminals. This parallel circuit will exhibit a maximum impedance at some high frequency defined as the self-resonant frequency. However, the distributed capacitance does not appear to affect over-all circuit performance.

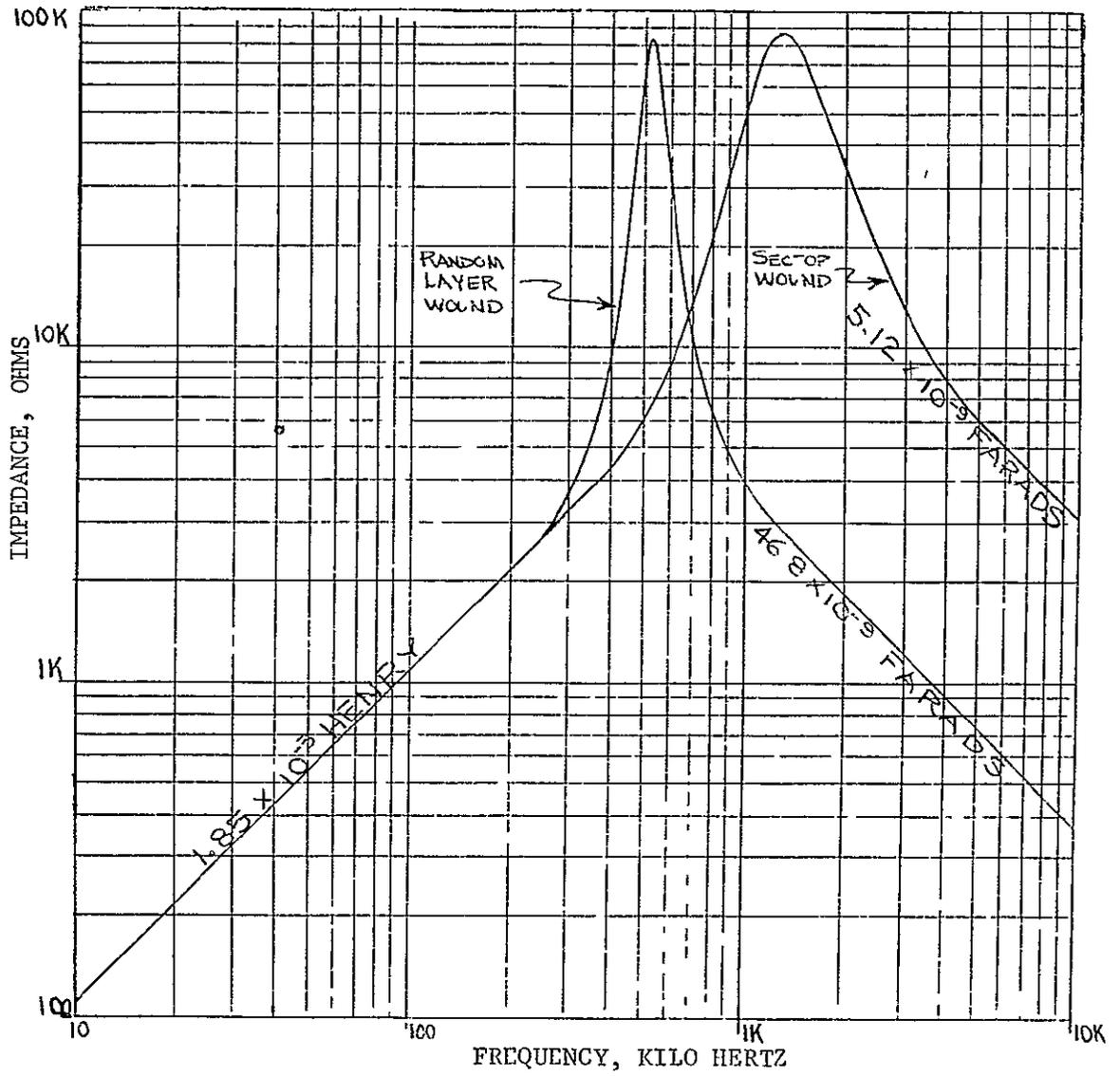


FIGURE A-10 HIGH FREQUENCY INDUCTOR CHARACTERISTICS

A novel approach to reducing the effects of DC magnetization was developed. This consisted of placing a second winding on the magnetic core, and terminating this winding across a resistor as shown in the schematic of Figure A-11. The value of this resistance was selected to minimize the peak current at turn-on. The induced voltage from the primary winding causes a current flow in the current limited secondary that effectively links the core in a direction to attempt to cancel the ampere-turns that caused it. This results in lower net ampere-turns of DC magnetization, and a higher apparent inductance.

Some typical data on resistor selection is plotted on Figure A-12, and it can be shown that the surge impedance of the series inductor-capacitor combination can be made to approach the theoretical impedance at resonance. The let-through current waveform from an applied step-function of voltage has a pseudo-sinusoidal shape at the filter resonant frequency. To a first order approximation then, the minimum size and weight filter can be determined by entering the graph of Figure A-3 at the left at the impedance required to hold the peak transient current to a desired value, and proceeding horizontally to the intersection with the shaded area.

The loads of interest to be protected by these filters range from ten ohms (three amperes) to one thousand ohms (thirty milliamperes). If these loads have any AC components, then the AC component must be supplied from the capacitor in shunt with the load. Furthermore, the capacitor must be sufficiently large to allow successful operation of the load.

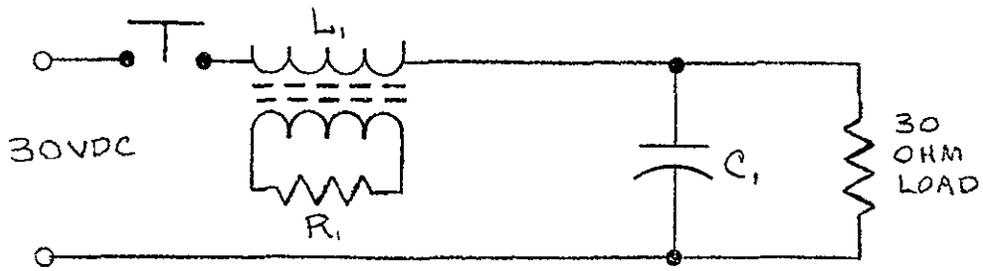
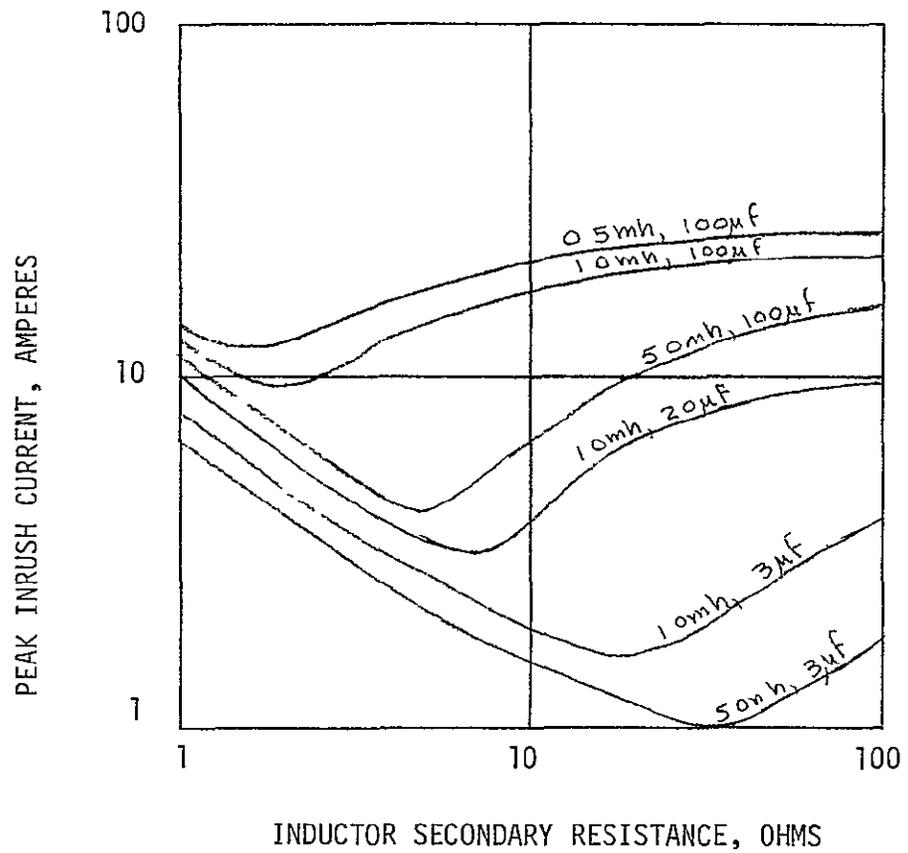


FIGURE A-11 INDUCTOR TRANSFORMER TEST CIRCUIT



INDUCTOR SECONDARY RESISTANCE, OHMS  
FIGURE A-12 TURN-ON TRANSIENT CURRENT

Foil tantalum capacitors are usually selected for low pass filter applications on DC systems. For the nominally 60 VDC rating required on the 30 VDC bus, the capacitance-equivalent series resistance product is a constant at approximately 180 microfarad-ohms. A value of nominal equivalent series resistance of the filter capacitor can thus be established in terms of capacitance in farads as

$$R_c = \frac{1}{C} (180 \times 10^{-6}) \text{ ohms}$$

Some typical foil tantalum characteristics in the values of interest are listed for information in Table A-3.

TABLE A-3

CAPACITOR CHARACTERISTICS				
VOLTAGE	MICROFARADS	CASE SIZE	RESISTANCE, OHMS	WEIGHT, GRAMS
50	12	C	15.6	2.5
50	30	D1	5.18	7.3
50	70	D2	2.46	11.2
50	100	D3	1.78	14.5
60	8	C	23.3	2.5
60	25	D1	7.77	7.3
60	50	D2	3.69	11.2
60	70	D3	2.59	14.5
60	4	C	60.0	2.5
100	2	C	119.0	2.5
100	1	C	168.0	2.5

The characteristic weight of tantalum foil capacitors of type CL-55 and CL-65 of MIL-C-3965, covering the capacitance range from 10 microfarads to 1000 microfarads, is fairly uniform. Typical weights per microfarad are shown on Figure A-13.

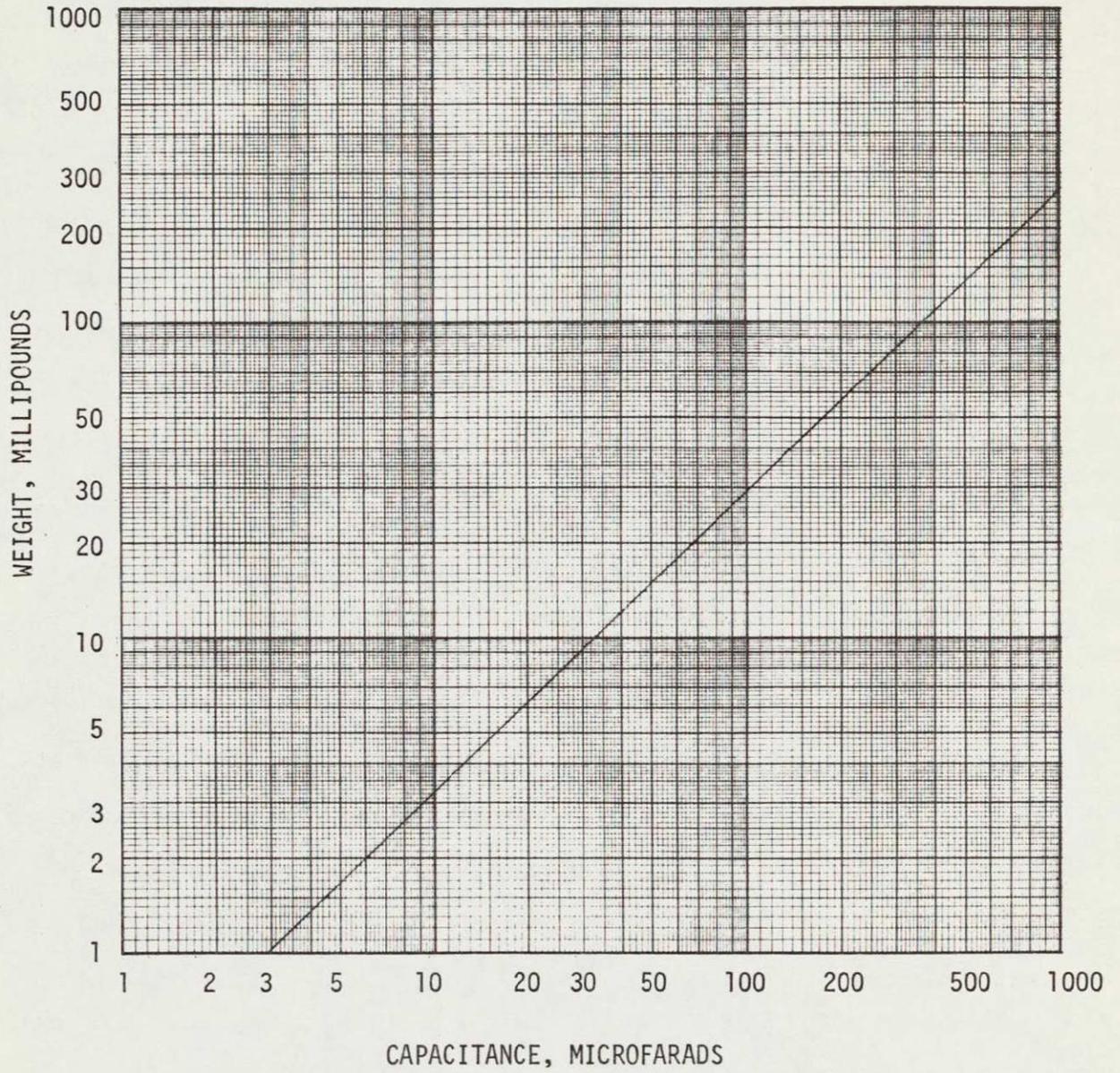


FIGURE A-13

CHARACTERISTIC WEIGHT OF TANTALUM CAPACITORS

1 August 1970

Inductor weights vary more nearly as the product of inductance and the square of the rated current, and per unit weights vary almost ten to one as a function of core material, losses, and the style of packaging. A typical range of weight values is shown between the two nominal limits of Figure A-14. A meaningful tradeoff exists then between the amount of filtering provided to limit ripple current, and the extra weight of RTG capacity to provide the peak over average current that is permitted on the bus. If the output capacitance of the shunt regulator is neglected, each component should limit its peak current with a filter whose weight is optimized to minimize the combined weight of the filter and the RTG. The results of this trade-off is shown on Figure A-15, where the two nominal limits on inductor weight were used, data is presented for sixty typical loads rated at 0.5 amperes each, and the results show that permissible ripple current should be in the range of two to four percent.

The only additional requirement on the filter piece part values is the surge impedance. The series combination of the inductor and the capacitor at initial application of voltage should not present such a low impedance to the vehicle bus that it is pulled out of regulation. The composite DC load on the bus occurs in the far encounter mode, and results in 440 watts of power, or nominally 2 ohms.

A-21

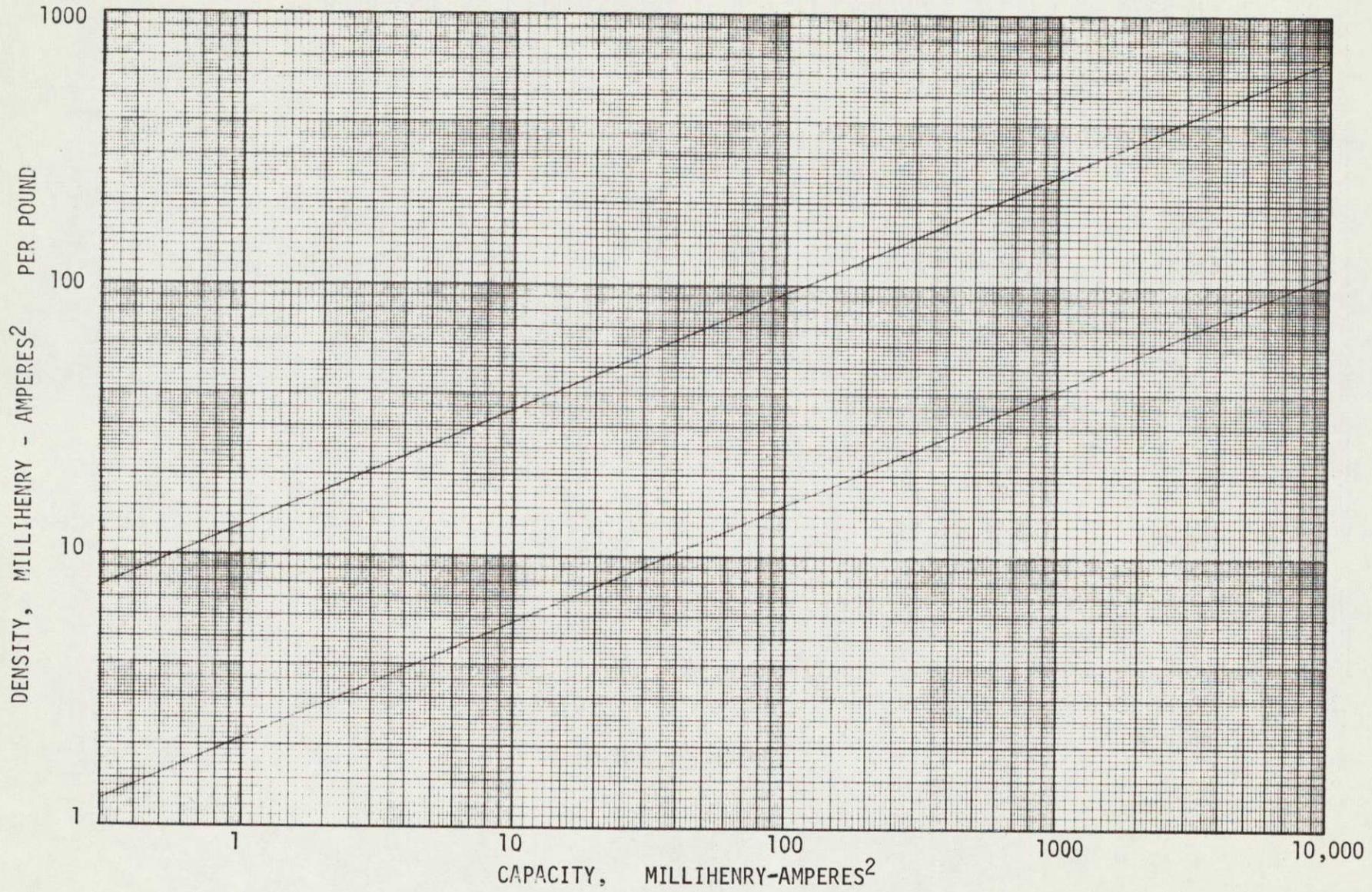


FIGURE A-14

TYPICAL INDUCTOR CHARACTERISTICS

1086-TOPS-555  
1 August 1970

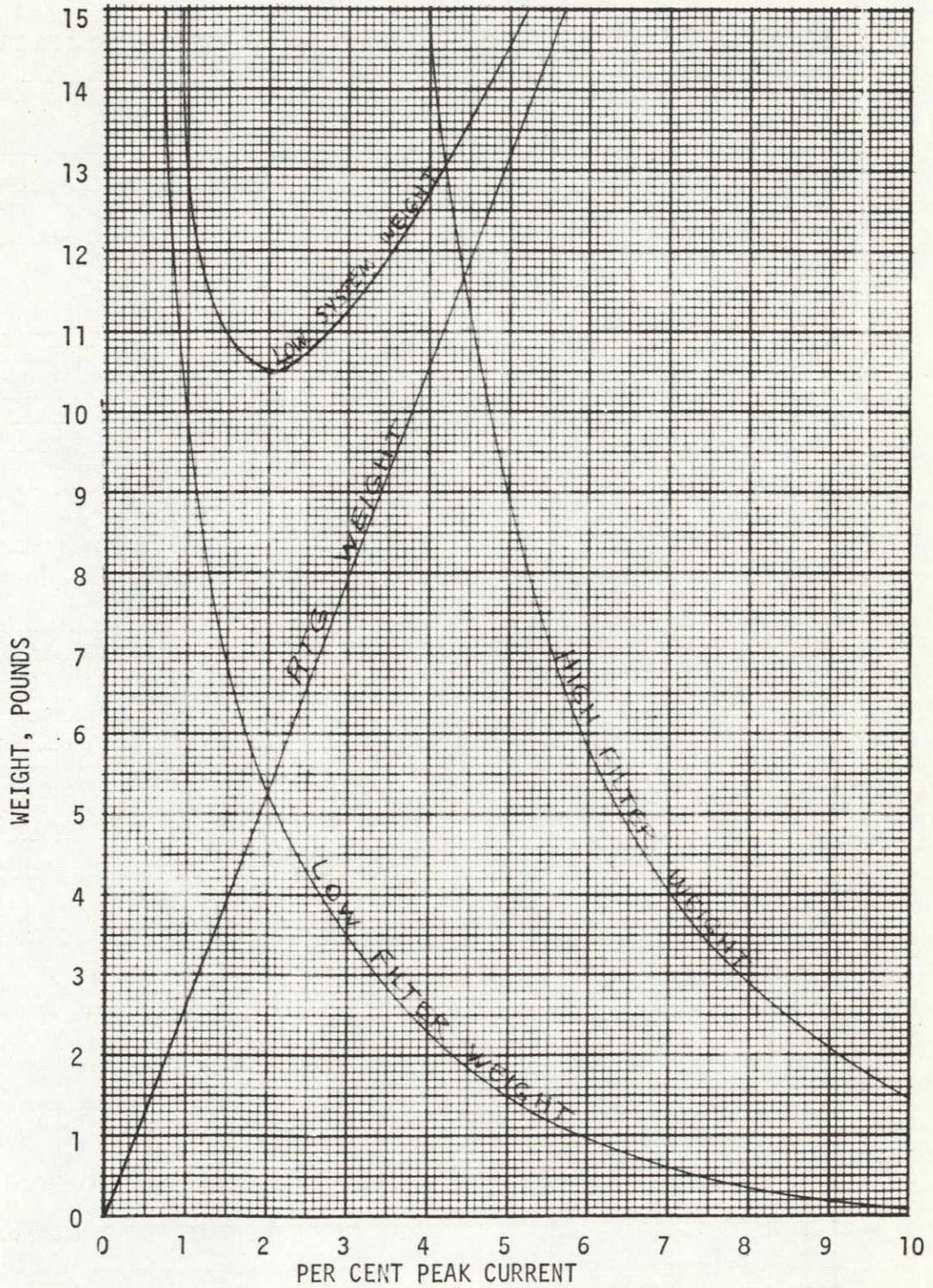


FIGURE A-15 OPTIMIZED SYSTEM WEIGHT

This equivalent impedance is shown on Figure A-3 as a low impedance boundary, and represents the total capability of the RTG system at end of mission. Obviously the transient load must be limited to some small percentage of this value for a balanced spacecraft design.

Usual practice for all expendables in a launch vehicle configuration is to allocate a ten percent margin. If this guideline is imposed, then the design margin of the power source could be utilized to furnish transient energy. The requirement on the filter now is that the surge impedance be at least twenty ohms to limit the peak current to ten percent of the end of mission RTG capability. This is also shown as a low impedance limit on Figure A-3, and now the filter inductance and capacitance values are realistically limited to a few decades of values for each piece part. The ideal and minimum size and weight would be a one millihenry, two microfarad "L" section, with a self-resonant frequency of 3500 Hertz, and a surge impedance of 22 ohms.

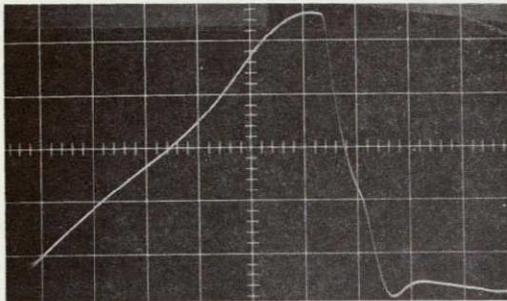
However, this value of capacitance may be inadequate to supply a low impedance path for switching loads such as converters and inverters. A more realistic value here is nominally twenty microfarads, lowering the surge impedance to 6.5 ohms at a resonant frequency of one kilohertz. Charging such a filter

from a current limited source results in an out-of-regulation condition for less than one millisecond, and is tolerable if the fault detection circuits are suitably delayed to prevent nuisance trips during turn-on transients.

Filters with these nominal characteristics have been included in the three DC to DC converters to demonstrate the performance parameters when operating from the shunt regulator.

The TWT Converter provides a more stringent requirement on the bus. The initial turn-on transient peaks at about ten amperes after about one millisecond as shown on Figure A- 16 . At this time, the heater supply is loaded, but the main high voltage converter is delayed until the tube has had time to warm up. After the delay, the main converter has to start up and charge the output filter capacitors. During this transient interval, an auxiliary oscillator drives the switching transistors with a higher than normal base drive. The current transient during this interval is as shown on Figure A-17 with the converter free running, and on Figure A-18 with vehicle clock. This overcurrent transient peaks at about twelve amperes and persists for about forty milliseconds.

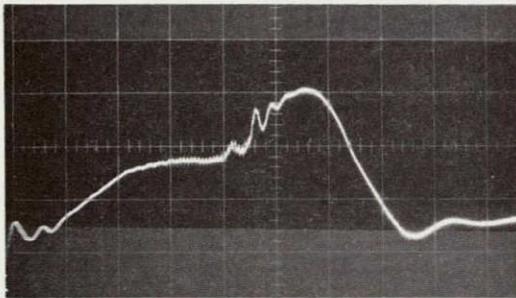
Figure A-19 graphically portrays the conditions on the main bus if this condition is allowed to occur when the RTG has sufficient power for the steady state load only. Bus voltage will remain constant until the RTG capacity at 30 volts is exceeded. This occurs at about thirteen milliseconds.



HORIZONTAL = 200 MICROSECONDS  
PER CENTIMETER

VERTICAL = 2 AMPERES PER  
CENTIMETER

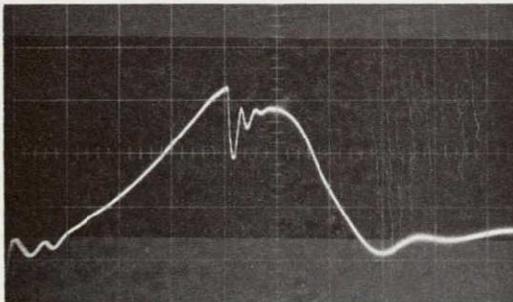
FIGURE A-16 TWT CONVERTER INRUSH CURRENT



HORIZONTAL = 10 MILLISECONDS  
PER CENTIMETER

VERTICAL = 4 AMPERES  
PER CENTIMETER

FIGURE A-17 TWT CONVERTER DELAYED CURRENT, FREE-RUN



HORIZONTAL = 10 MILLISECONDS  
PER CENTIMETER

VERTICAL = 4 AMPERES PER  
CENTIMETER

FIGURE A-18 TWT CONVERTER DELAYED CURRENT, CLOCKED

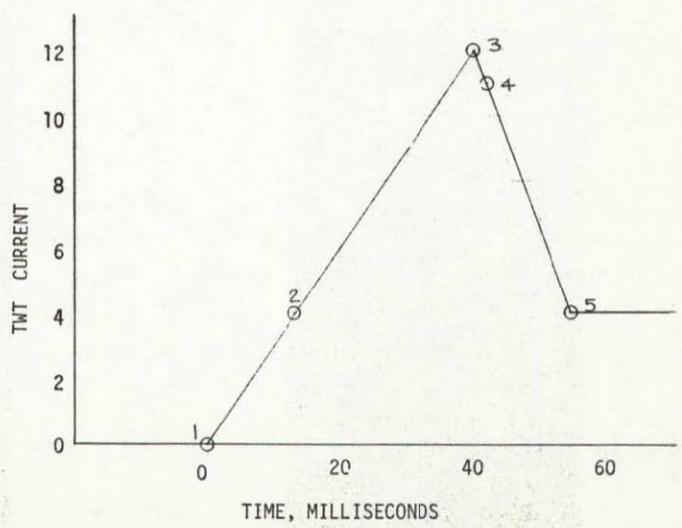
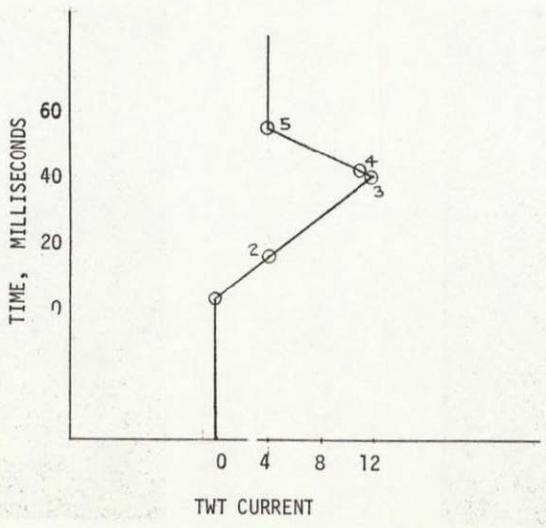
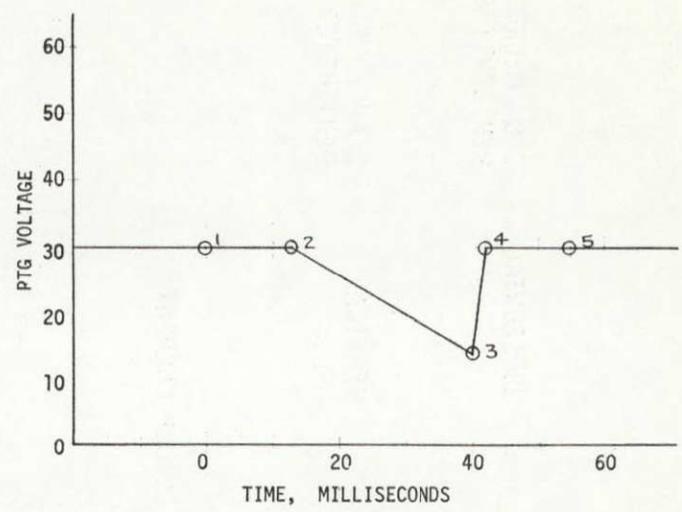
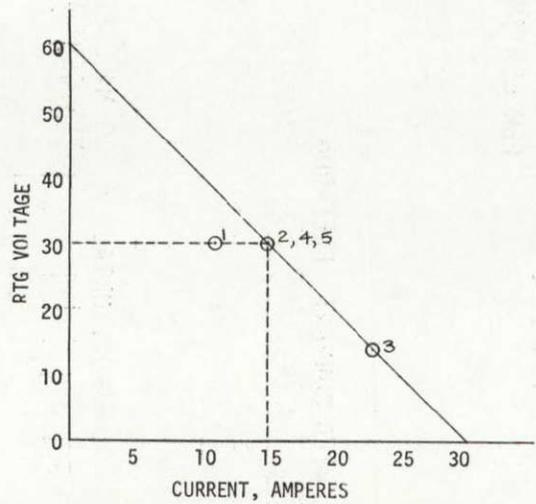


FIGURE A-18 TWT CONVERTER TURN-ON RELATIONSHIPS

A-26

1J86-TOPS-555  
1 August 1970

At this time the current starts to decay, and the bus recovers in an additional two milliseconds. It should be noted that an out-of-specification condition existed for 26 milliseconds, and failure detectors must be delayed to permit this expected transient condition.

APPENDIX B    SELECTED RADIATION EFFECTS

Introduction    Considerable thought has been applied to select piece parts, materials, and components that will adequately withstand the expected radiation environment. Existing hardware that has been qualified for the space radiation environment will be used in many cases, and the choice of passivated semiconductor piece parts for general use significantly increases the reliability of the system in the radiation environment. In addition, the circuit design in many applications can be made to tolerate the predicted irradiation without affecting functional performance. In general, judicious piece part derating for gain and leakage will contribute significantly to the stability of the system. Furthermore, the detrimental effects of radiation on electronics can be reduced to tolerable limits through component packaging to utilize to the fullest extent possible the shielding afforded sensitive components by less sensitive devices. Shielding obviously gives protection in the case of electron and proton radiation, but is ineffective in preventing neutron and gamma damage.

Radiation Sources Neutron and gamma irradiation from a radioisotope thermoelectric generator utilizing plutonium 238 as a fuel are potential problems for the power conditioning equipment semiconductor devices. The gamma and neutron environments of concern have been specified as an absorbed dose equivalent to 300 rads in silicon, and  $3 \times 10^{11}$  neutrons incident upon a square centimeter of surface area (NVT).

The geomagnetically trapped radiation environment that the spacecraft will encounter during the earth parking orbit, early transition, and planetary encounters will consist of electrons and protons. For the most part, the electrons will constitute the primary penetrating component of the trapped particles since the magnetic field at low altitudes is not capable of trapping protons of energy greater than about five million electron volts (Mev). However, large quantities of low energy protons, less than about 5 Mev, can be expected. These low energy protons are readily absorbed in the external spacecraft surface and are of concern only to exterior surface mounted equipment, such as the shunt resistor panel. This high flux, although not very penetrating, delivers a significant surface dose.

Additional dose rates will accrue from outer planet Van Allen belt particle fluxes as functions of energy, trajectory, and flyby times. Jupiter's Van Allen belts are formidable, having calculated peak fluxes equal to or greater than  $10^{11}$  electrons per centimeter squared second and approximately  $10^9$  particles per centimeter squared second, yielding equivalent dose rates in silicon of greater than  $10^5$  rads per hour at altitudes of 1.5 Jovian radii.

Saturn's belts are at least two orders of magnitude less intense, and their existence is highly problematical. The intensity and existence probabilities of belts around Uranus and Neptune are even less.

Sporadic, intense solar flare activity occurs which may result in the spacecraft receiving a significant radiation dose due to solar flare protons. In addition to the energetic particles of periodic solar flares, the sun releases a continual flux of very low energy particles into the solar system. This flux is referred to as the "solar wind", consists primarily of low energy protons and electrons, and has a mean velocity near earth of 500 kilometers per second. In the vicinity of the earth, the protons have energies of several thousand electron volts, and a density of approximately five protons per cubic centimeter. Similarly, the electron density is approximately one thousand electrons per cubic centimeter with energies of the order of several electron volts. The near earth proton flux is approximately  $2 \times 10^8$  particles per centimeter squared second, and although not very penetrating, will constitute a significant ionization dose on the spacecraft surface. It is of interest to note that for shield thicknesses greater than about one gram per square centimeter, the solar flare proton environment is the major contributor to the internal dose. The internal dose due to the Bremsstrahlung created by the impinging electrons will be less than 100 rads. This Bremsstrahlung dose, while being very penetrating, will not contribute significantly to the ionization expected from the other components of the radiation environment.

Primary galactic cosmic rays consist primarily of various atoms stripped of their electrons, with high energy electrons amounting to a few percent of the primary flux. The majority, however, are hydrogen atoms. The average energy of these particles is four billion electron volts, with the energy varying from less than  $10^2$  Mev to  $10^{13}$  Mev. The average free space isotropic flux is two particles per centimeter squared second. This intensity is modulated somewhat by the eleven year solar cycle, being about a factor of two more at solar minimum than at solar maximum. This is apparently due to the injection of large magnetic clouds into the entire solar system by the sun during maximum sunspot years, which in turn deflect away some of the galactic particles. This component of the radiation environment, although very penetrating, will not constitute a significant radiation dose to the spacecraft systems. As a worst case, the flux will be approximately four particles per centimeter squared second throughout almost the entire mission, yielding a typical total of approximately  $10^9$  per centimeter squared.

Based on these calculations, almost all the entire mission dose will be due to the Jupiter flyby. To obtain the requisite velocity increment to continue the Grand Tour Mission, the spacecraft must approach to within approximately ten Jovian radii, yielding doses of equal to or greater than an absorbed dose equivalent to 1000 rads in silicon for 0.1 grams per centimeter squared shielding.

Effects on Semiconductor Electronics The main effects of ionizing radiation on semiconductor electronics, particularly transistors, are the bulk damage effects and the so-called radiation-induced surface effects. The bulk damage effect is the disruption of the crystal lattice of the semiconductor material. In transistors, this causes a decrease in carrier lifetime in the base region of the device. This effect takes place whether the device is electrically active or not. The surface effects phenomenon, on the other hand, is more predominant when the devices are simultaneously under electrical stress and exposed to ionizing radiation. This effect is due mainly to the interaction of the ionized gas (in the hermetically sealed transistor) and ionized surface impurities with the semiconductor surface.

Both of these effects (bulk and surface) can affect the transistor gains quite drastically. In addition, the surface effects can also alter junction leakage currents considerably. The extent to which device parameters are altered for a given radiation dose can depend to a large degree on device construction and initial electrical characteristics.

The change in the leakage current for gas filled mesa and planar devices is caused essentially by the total accumulated ionization dose. The effect is apparently strongly dependent upon surface contamination, thickness of the passivation layer and other process variables, resulting in a rather random behavior. Two of the transistor parameters most sensitive to surface effects in both passivated and non-passivated devices are the collector-base leakage current ( $I_{CB0}$ ) and the current gain.

In general, passivated devices are much less sensitive to  $I_{CBO}$  variations than non-passivated devices. It is difficult to make generalizations about  $I_{CBO}$  increases on passivated devices. Some devices have thresholds equivalent to an absorbed dose of  $10^4$  to  $10^5$  rads in air. On the otherhand, the Space Systems Organization of the General Electric Company has tested hundreds of passivated 2N708, 2N914, 2N930, and 2N2453 devices which showed no significant  $I_{CBO}$  increases up to doses of approximately  $10^6$  rads in air. Also, large variations from one device manufacturer to another have been seen. Thus, it appears that the quality of the passivation on the collector-base junction is a controlling factor.

Considering the previous environment estimates, it is seen that the internal ionization doses to the electronic components for the twelve year mission depend on parameters totally beyond the control of the circuit designer. Generator fuel and shielding, parking orbit inclination and duration, Jupiter fly-by distance, and solar activity all contribute to the expected environment.

The expected irradiation range for the mission is a minimum absorbed dose equivalent to 300 rads in silicon as specified in "Design Requirements and Constraints for Thermoelectric Outer Planet Spacecraft (TOPS) Power Subsystem" dated 24 April 1969, or a maximum of perhaps two decades greater than this for a close Jupiter fly-by. A 300 to 3000 rad gamma dose is far below the ionizing radiation damage threshold of passivated minority carrier devices. A neutron exposure of  $3 \times 10^{11}$  NVT, however, is about the damage threshold for certain types of transistors.

The most sensitive transistor in the circuits under consideration is the high voltage series regulator pass transistor in the Traveling Wave Tube Converter, which operates at very high collector to emitter voltage and at very low current. Any increase in leakage current above the minimum current required by the load would result in loss of regulation and an increase in output voltage. Additionally, there is no source of negative voltage to back bias the emitter to base junction. This would permit the collector to base leakage current to be removed before it is amplified by transistor gain.

The same type transistor is used in other applications at lower voltage and higher current, but the low current application is most sensitive to increased leakage current if surface effect damage is severe at the radiation doses of interest. Furthermore, this phenomenon is influenced by the test conditions of temperature, time, and bias. The investigation of the transistor design indicates that very little degradation in leakage current and current gain should be expected below  $10^5$  rads exposure dose.

Test Procedure An experiment was performed on a sample of four Westinghouse silicon power transistors, type 1763-1820, to determine the effect of a high dose of radiation. The test schematic of Figure B-1 was used. The test method involved simultaneous exposure of the four devices. One hundred volts of collector to emitter bias was continuously applied, except for one dose increment. This was to determine if healing might occur with radiation and no bias. The device cases were grounded, and leads were shielded to facilitate handling, reduce spurious radiation induced signals, and allow

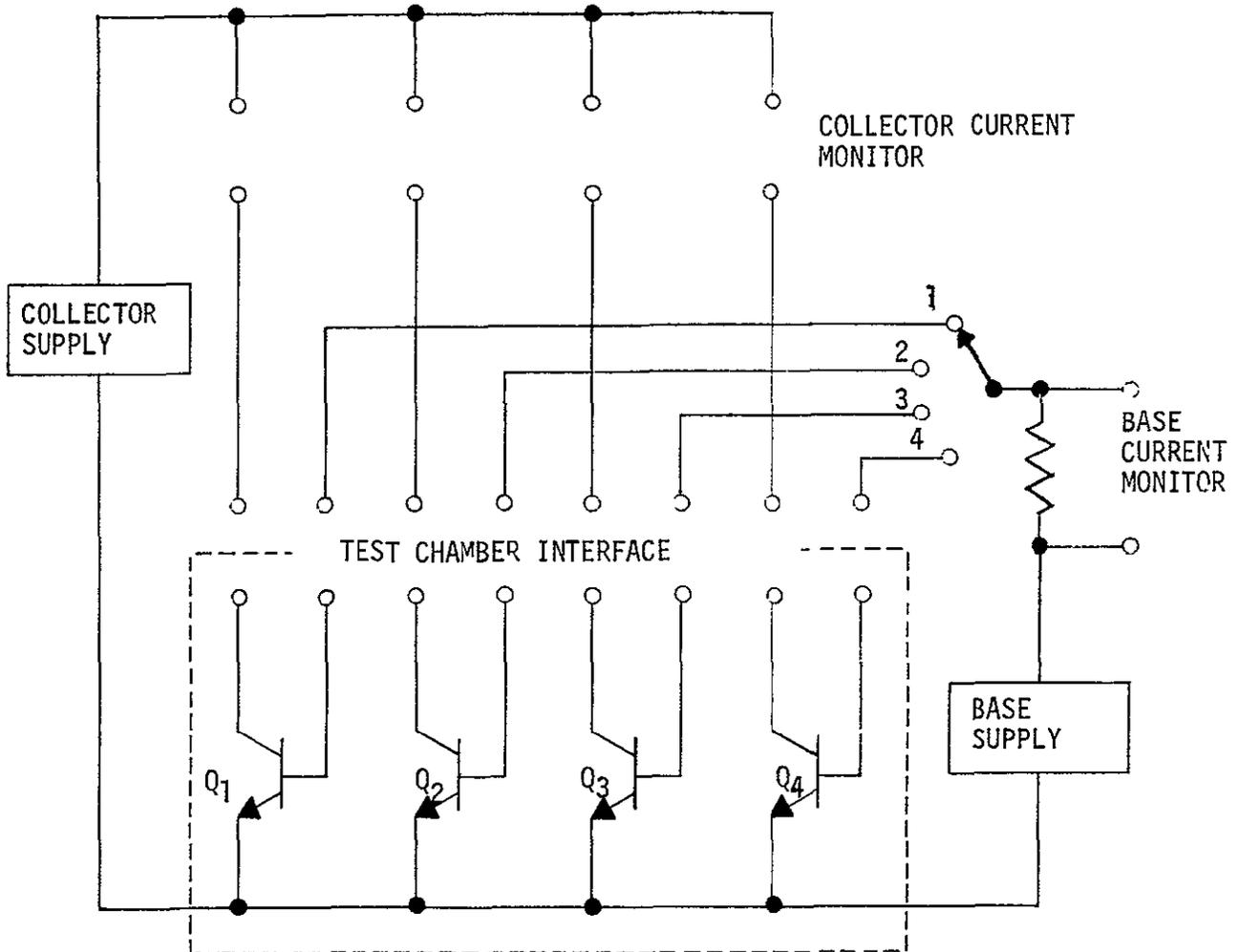


FIGURE B-1 ELECTRICAL TEST SCHEMATIC

monitoring of case temperature on one device. A Keithley 602 electrometer was used to measure collector current, and base current was monitored by a Keithley 155 microvoltmeter across a precision one kilohm resistor. Power supplies were used to bias the collector to emitter junction and the base to emitter junction, and a one hundred kilohm series base resistor was used during the test.

Radiation was supplied from a Cobalt 60 source at the Franklin Institute, Philadelphia, Pennsylvania, with a total dose obtained of  $5 \times 10^5$  rads  $\pm 10\%$ .

The specific measurements made were

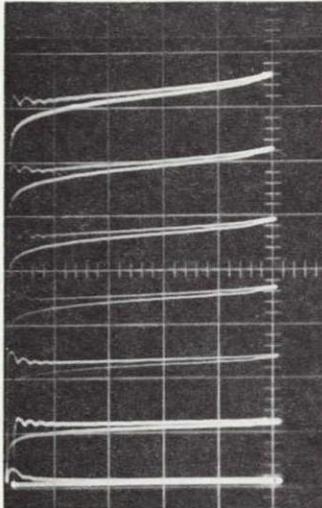
- a Pre- and post-test curve tracer measurements of gain over a range of collector currents from 0.5 to 35 milliamperes for collector to emitter voltages up to one hundred volts.
- b Pre- and post-test measurements of open emitter, collector to base leakage current with a one hundred volt bias.
- c Pre-, during, and post-test measurements of collector to emitter leakage current with open base, and required base current at 0.5 milliamperes of collector current to establish current gain.
- d Radiation exposure dose during the test phase.
- e The degree of post-test recovery of leakage current and gain for one device at an elevated annealing temperature of 200°C.

The electrical characteristics specified by Westinghouse Electric Corporation Semiconductor Division, Youngwood, Pennsylvania, are as tabulated in Table B-1. The 1763-1820 is an NPN double epitaxial silicon power transistor designed expressly for high reliability operation in military, space, and industrial applications.

A reproduction of curve tracer measurements on sample #2 are shown in Figures B-2 and B-3 as typical of the four devices tested. Operation is shown from zero to one hundred volts collector to emitter bias, and from zero to forty milliamperes collector current. The post irradiation measurements are also post annealing, and portray the gain recovery to seventy percent of initial value.

TABLE B-1. 1763-1820 Electrical Characteristics

Collector to Emitter Voltage	180 Volts
Collector to Base Voltage	180 Volts
Emitter to Base Voltage	7 Volts
Peak Collector Current	40 Amperes
Peak Base Current	10 Amperes
Open Base Collector Current at 135 Volts Bias	0.5 Milliamperes
Minimum Current Gain at 20 Amperes	20
Minimum Gain-Bandwidth Product at 10 Megahertz	30 Megahertz
Minimum Operating Junction Temperature	0°C
Maximum Operating Junction Temperature	200°C

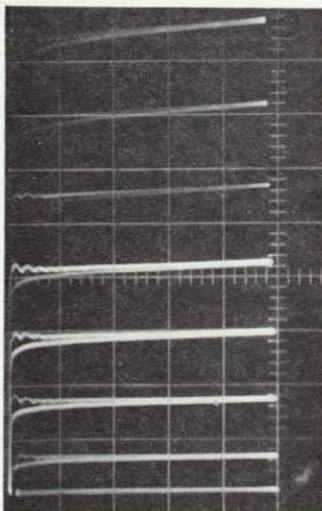


Vertical: 5 Milliamperes Per Division

Horizontal: 20 Volts Per Division

Base Current Steps: 0.2 Milliamperes

FIGURE B-2. TYPICAL PRETEST DATA, SAMPLE #2



Vertical: 5 Milliamperes Per Division

Horizontal: 20 Volts Per Division

Base Current Steps: 0.3 Milliamperes

FIGURE B-3. TYPICAL POSTTEST DATA, SAMPLE #2

The change in open base collector to emitter leakage current as a result of radiation can be determined from Figures B-4 thru B-7. Data taken both under radiation and at ambient conditions is presented. The results on Sample #1 show a reduction in leakage current with irradiation under both conditions. This indicates the lack of any mechanism to increase true collector to base leakage current, shows the effect of gain degradation reducing total collector to emitter leakage current, and shows higher leakage under radiation exposure which is attributed to energetic particle activity. Data on Sample #2 shown on Figure B-5 is similar to that of Sample #1, with the added post annealing test point for reference. Figures B-6 and B-7 show fairly constant leakage current with radiation dose at ambient, although Sample #3 demonstrated at least one decade higher leakage in the radiation environment. The apparent good performance of leakage current variation is more probably due to low gain, and consequently low amplification of energetic particles.

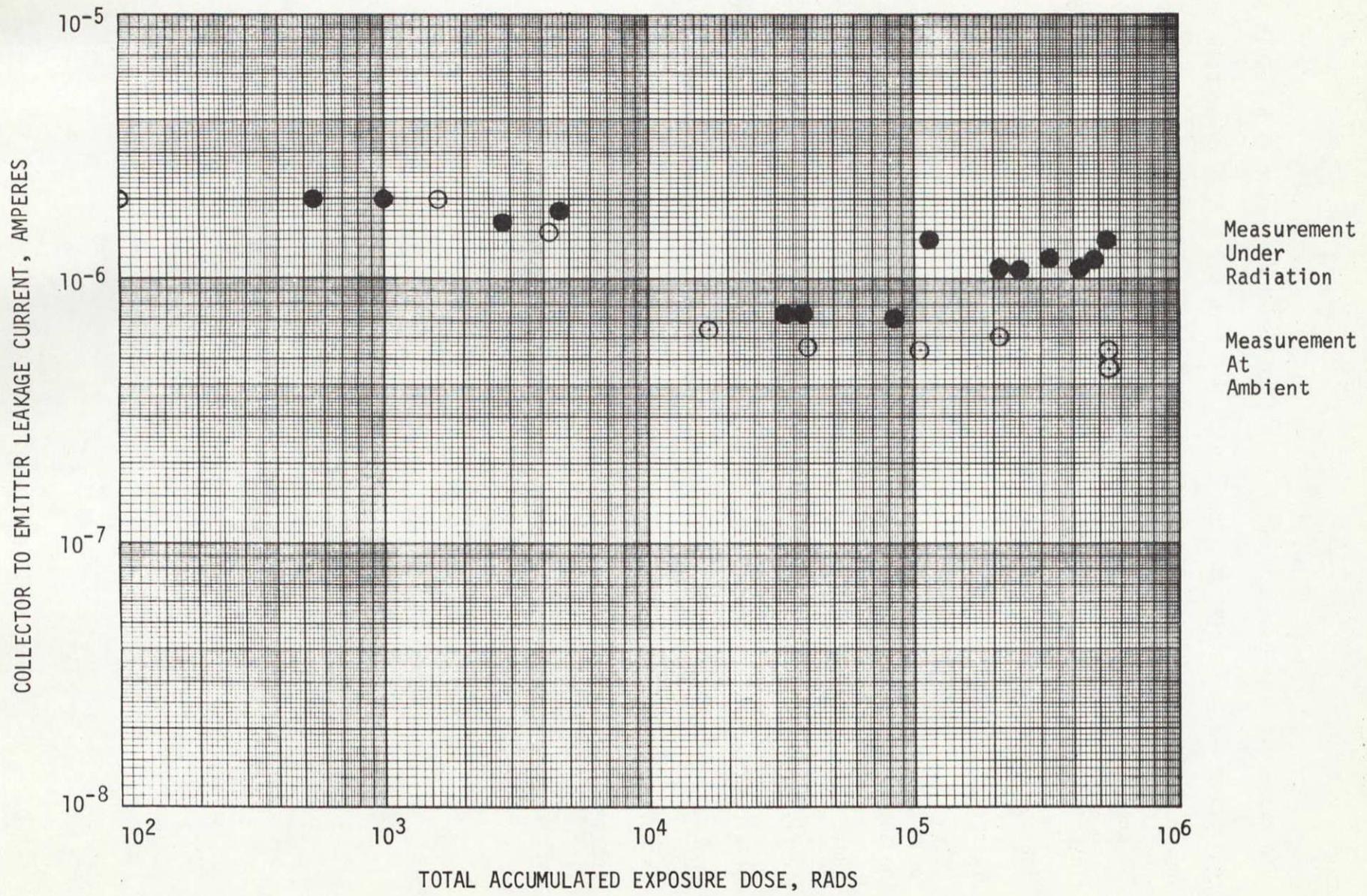


FIGURE B-4. RADIATION EFFECTS ON LEAKAGE, SAMPLE #1

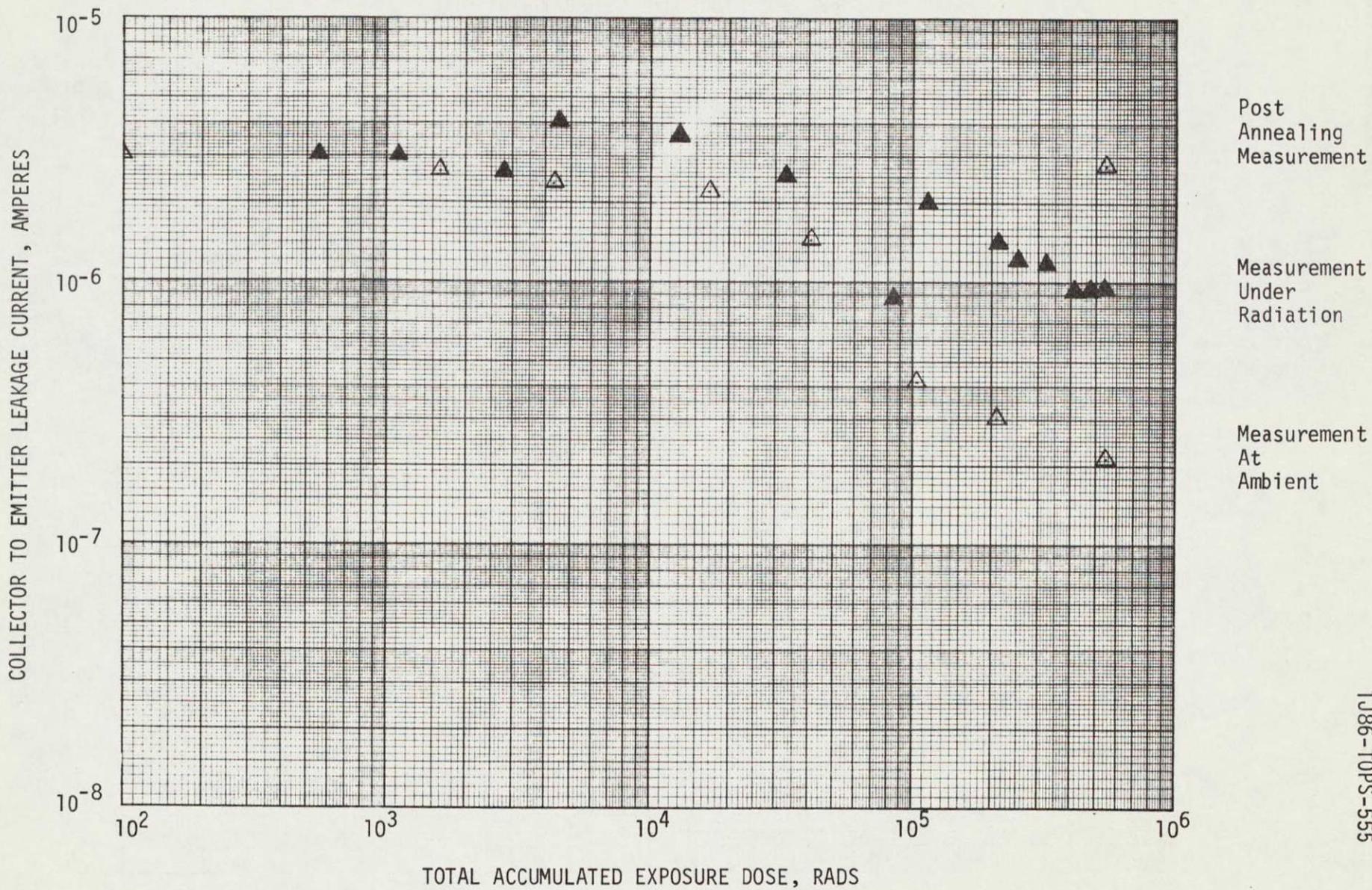


FIGURE B-5. RADIATION EFFECTS ON LEAKAGE, SAMPLE #2

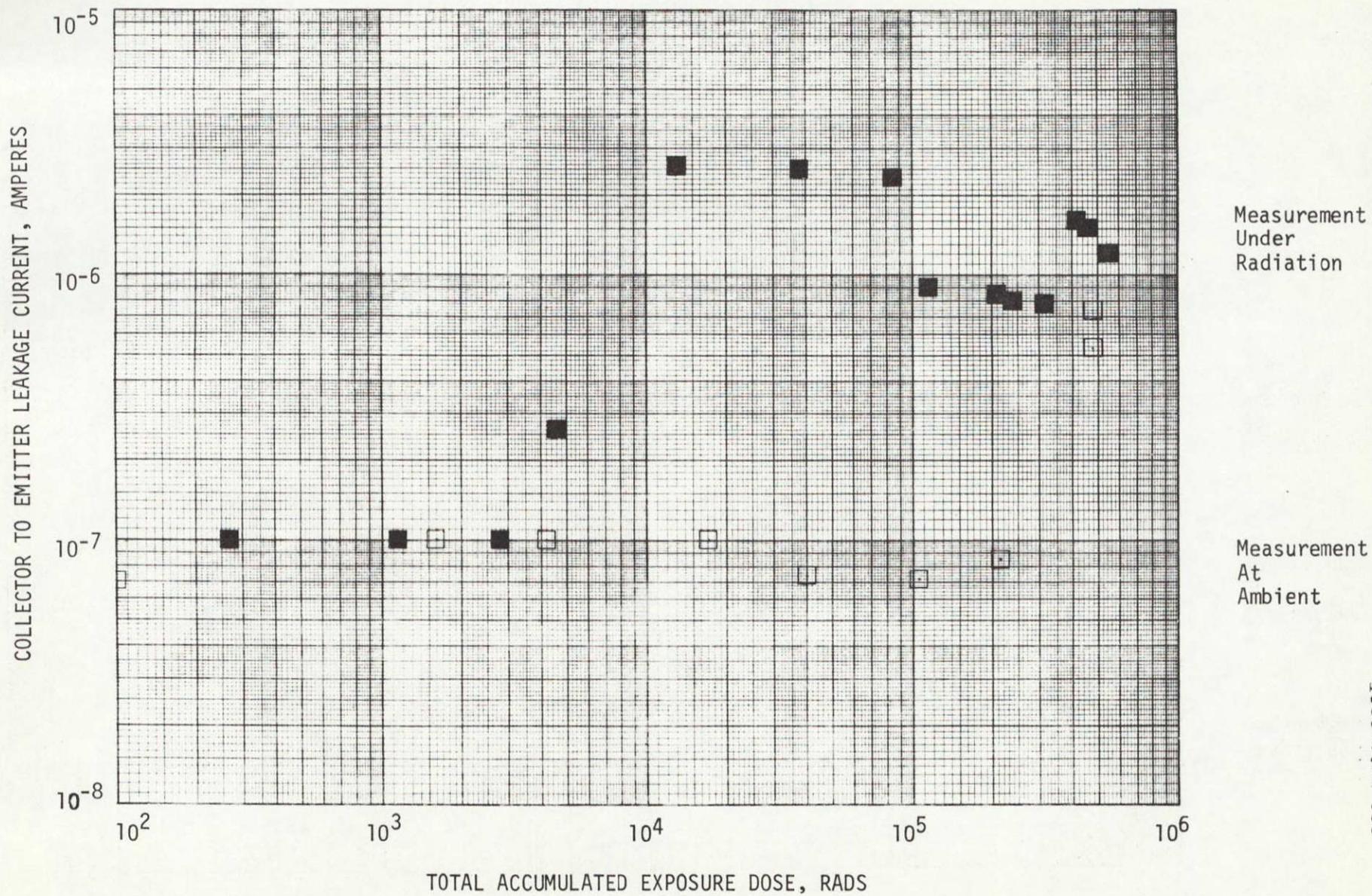


FIGURE B-6. RADIATION EFFECTS ON LEAKAGE, SAMPLE #3

B-17

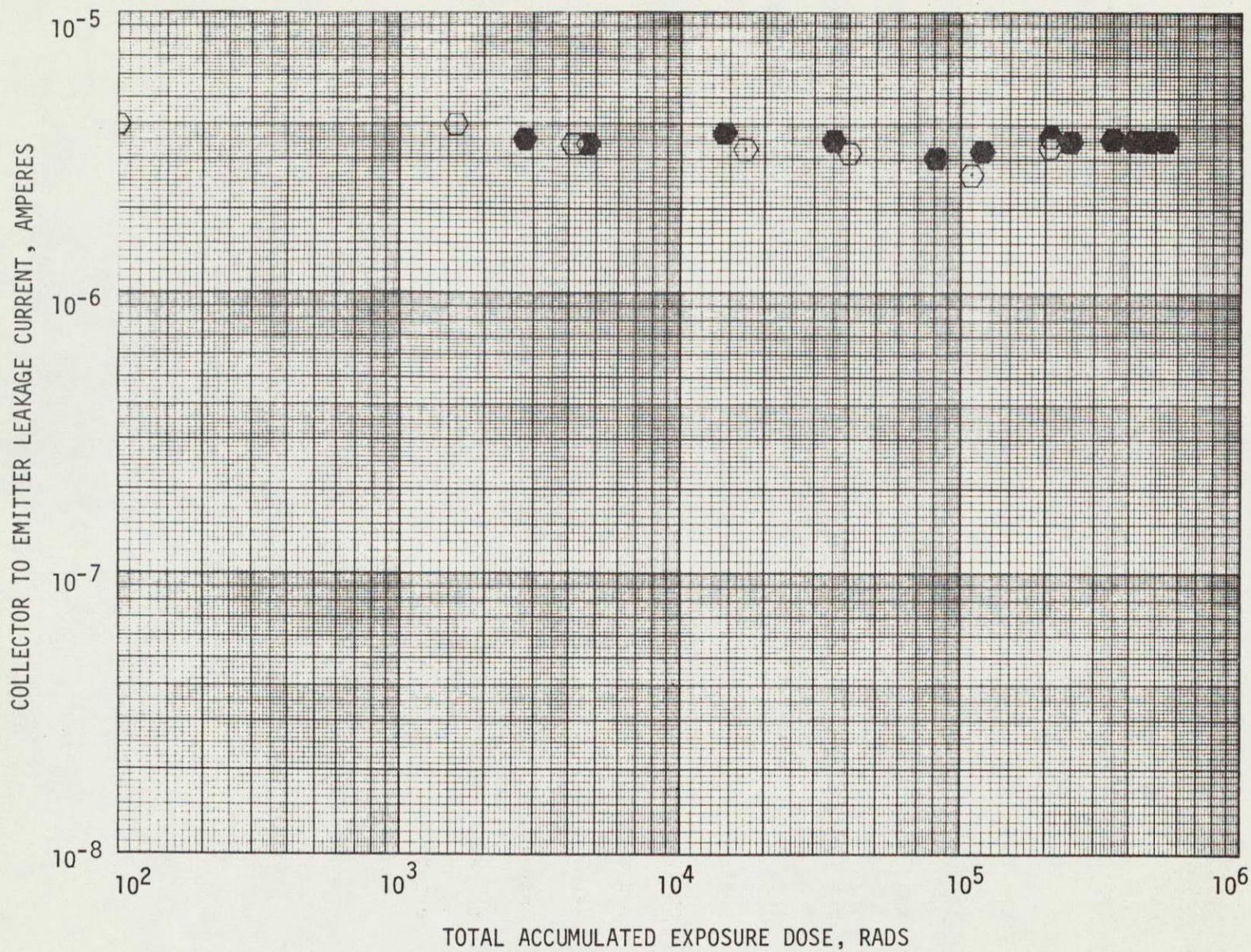


FIGURE B-7. RADIATION EFFECTS ON LEAKAGE, SAMPLE #4

1J86-TOPS-555

Table B-2 shows the increase in Post-irradiation current gain as a result of an exposure to a temperature of 200° Centigrade. Measurements were made at room temperature immediately after the exposure, and the exposure time was in increments of 1 hour, 1 hour, and 14 hours. Healing by annealing indicates that the degradation in current gain during irradiation was due to surface effects phenomena. The gain was reduced to 20 percent of its pre-test value as a result of the radiation dose administered, but recovered to approximately seventy percent of its initial value as a result of annealing.

The results of collector to base leakage current measurements indicate that this characteristic is exceptionally stable, demonstrating a high quality surface passivation and an extremely low level of surface impurities. The collector to emitter leakage current shows a decrease from initial to post radiation, but this is an apparent decrease only, and is actually the result of gain degradation operating on the relatively stable collector to base leakage current. There is no absolute correlation between gain at collector to base leakage current and measured gain at 0.5 milliamperes, but the trends are in the same direction.

TABLE B-2. SAMPLE #2 ANNEALING STUDY

	Initial Reading	Post Radiation	ANNEALING TIME AT 200°C		
			1 Hour	2 Hours	16 Hours
Collector to Emitter Voltage, Volts	100	100	100	100	100
Collector Current, Milliamperes	0.5	0.5	0.5	0.5	0.5
Base Drive, Microamperes	18.0	90.0	31.0	24.0	26.5
DC Current Gain	27.8	5.55	16.1	20.8	18.9
Collector to Base Leakage, Microamperes	0.27	0.23	0.28	0.42	0.26
Collector to Emitter Leakage, Microamperes	2.8	0.22	1.2	2.6	1.4

B-19

1J86-TOPS-555

Conclusions Based on the expected total accumulated radiation dose and the performance of the transistor selected as the worst device from a radiation environment and application standpoint, it is assumed that selection of devices and design of circuits can overcome the degradation expected from radiation from all causes

The high voltage regulator was identified as being especially susceptible to damage that would cause poor performance. This selection was made on the premise that the results of increased leakage current could not be compensated for easily by device selection or design change. Gain degradation is more easily corrected, for example

The results of the radiation testing, however, demonstrated that the open emitter leakage current did not increase significantly, and that gain degradation actually caused a decrease in the open base leakage current. This indicates that, in the application, performance as to leakage current will be enhanced by the radiation environment

APPENDIX C      POWER CONTROL OF REDUNDANT LOADS

One aspect of power distribution is power conditioning redundancy and its implementation. Generally, each load requires multiple voltages that are developed at the load by either a transformer-rectifier or a DC to DC converter. Some of these loads are classified as critical, and according to TOPS-3-250 "Power Profile and Allocation" they require redundant power conditioning equipment. Parallel and standby redundancy configurations are suggested in TOPS-3-250. This analysis reviews these redundancy methods in terms of circuit implementation, failure criteria, and failure detector requirements.

A review of loads to identify redundancy was performed. The type of redundancy if not defined in TOPS-3-250 was selected based on power level and system function. Generally, where power level was low or where the load function could not be interrupted, parallel redundancy was selected. Where power level was high or where functional redundancy is used, standby redundancy is selected. An example is the CCS. Table C-1 is a summary of the redundant loads and type of redundancy. Briefly, four loads have parallel redundancy, three loads (possibly six) have standby redundancy, and ten loads (possibly seven) have standby power conditioning and load redundancy.

TABLE C-1 LOAD REDUNDANCY

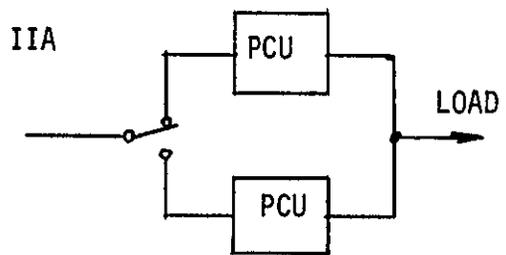
SUBSYSTEM	REDUNDANCY	REASON
1 Central Timing	Parallel	Power level 0.5 watts, system critical
2 Central Computer	Standby	Load redundancy 50/63.3 watts, (multiple channels)
3 Central Processor	Standby	Load redundancy 12/24.3 watts, (multiple channels)
4 Data Storage	Standby	Power level 44.9 watts, (multiple functions)
5 Flight Command Subsystem	Parallel	Power level 6.4 watts, time critical
6 Pyrotechnic Control Unit	Parallel	Power level 1.2 watts, time critical
7 S-Band Power Amp	Standby	Both PCE & Load (PCE & Load matching)
8 X-Band Power Amp	Standby	Both PCE & Load (PCE & Load matching)
9 S-Band Exciter	Standby	Both PCE & Load per TOPS-3-250
10 X-Band Exciter	Standby	Both PCE & Load per TOPS-3-250
11 Command Receiver	Standby	Both PCE & Load Requires Parallel Operation
12 RFS Pre Amp	Standby	Both PCE & Load Requires Parallel Operation
13 Tracking Receiver	Standby	Both PCE & Load per TOPS-3-250
14 Attitude Control Electronics	Standby	Power Level 11.2 watts, (not time critical)
15 Canopus Sensor	Parallel	Power Level 5.5 watts (time critical)
16 Gyros	Standby	Both PCE & Load 12.3 watts (minimize failure detector switching)
17 Gyro Electronics	Standby	Power Level 9.8 watts (not time critical)

KEY STANDBY LOAD CONFIGURATION TYPE II B, EXCEPT  
 ● TYPE II A  
 ○ POSSIBLY II A

Parallel and standby configurations referenced in TOPS-3-250 are shown in Figure C-1. Possible circuit connections to implement the redundancy configurations are shown in Figure C-2 and C-3.

The power conditioning referenced in Figure C-2 and C-3 have the characteristics shown in Figure C-4 and failures result in deviations from these characteristics. For example, Curve A shows the relationship between input and output voltage. The ratio of output to input voltage is a constant and a power conditioning failure is a change in this ratio. For the defined source the input voltage will not increase, but due to load faults may decrease resulting in an output voltage decrease as shown in Curves A and C. A failure criteria therefore is a decrease in output voltage if the input voltage is constant. From Curve B the ratio of output current to input current is constant and a power conditioning failure is a change in this ratio. Increases in input current without corresponding output current change is a power conditioning failure. For the loads considered, the normal load is generally a maximum load and corresponds to a maximum input current. Loads above the normal (load faults) result in higher input current. Therefore, a second failure criteria is  $I_1 > I_{max}$  if  $I_0 < I_{max}$ . A further observation is that the load current will only increase to a fault level as a result of load degradation. Since the power conditioning provides power to a single load, differentiating between load and power conditioning faults is not essential. Therefore, the second failure criteria reduces to  $I_1 > I_{max}$ .

STANDBY



PARALLEL

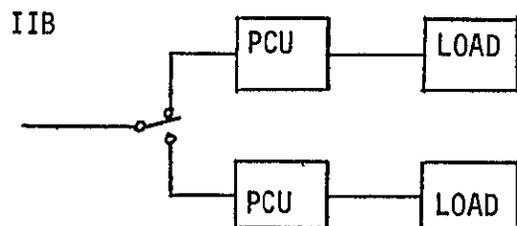
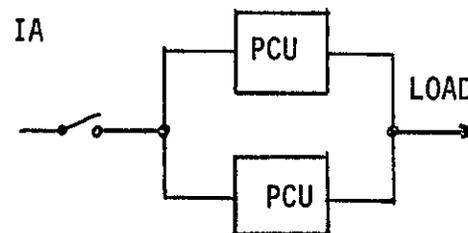


FIGURE C-1

REDUNDANCY CONFIGURATIONS FROM TOPS-3-250

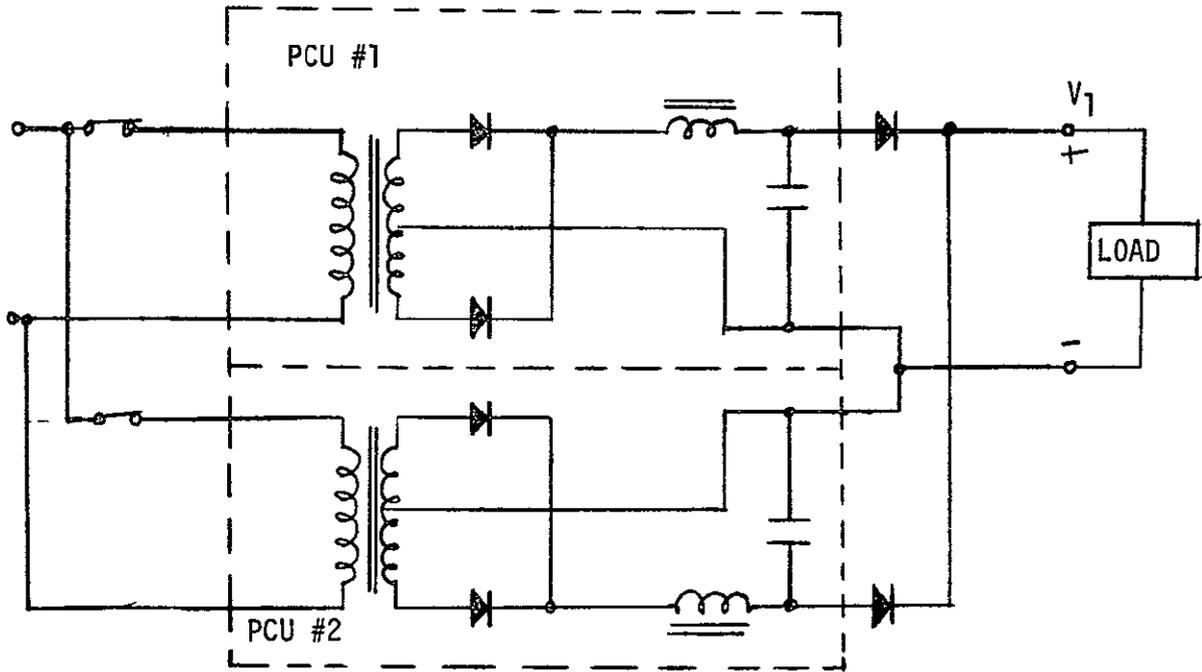


FIGURE C-2 SINGLE OUTPUT REDUNDANCY

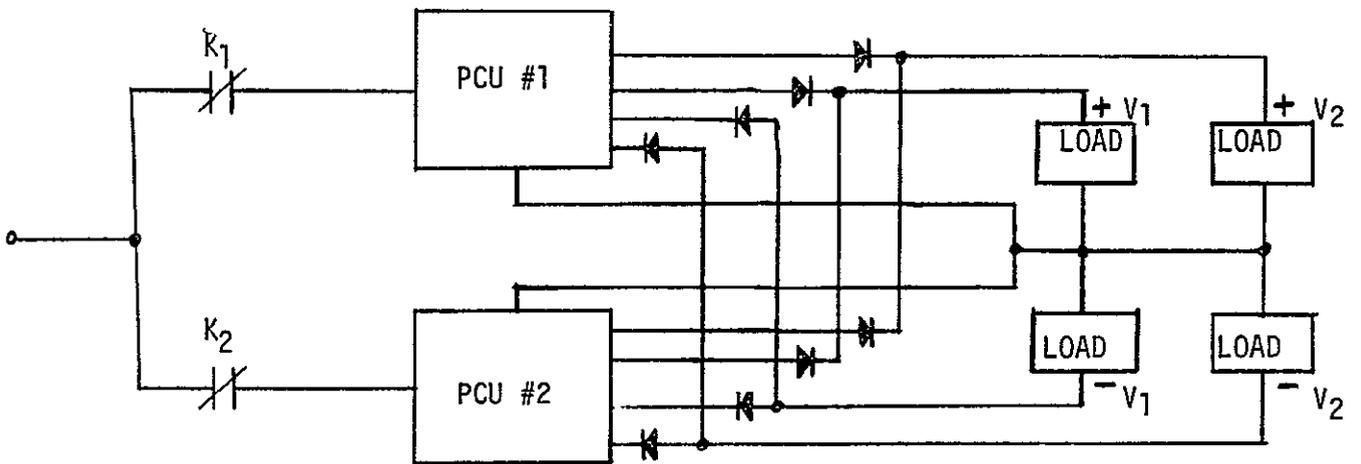


FIGURE C-3 MULTIPLE OUTPUT REDUNDANCY

The characteristics of Figure C-4 are for a power conditioning unit without current limiting. Effects of current limiting on the failure criteria are now discussed. Figure C-5 shows the possible current limiting concepts. Case I is the reference without current limiting (also shown in Figure C-4). Case II places a current limiter between the source and the redundant power conditioning units. In Case III each power conditioning unit has its own current limiter. Below each configuration is a voltage-current characteristic to show the effects of faults on the source or load current. Basic differences are the amounts of source current required to satisfy all possible faults. Source current for Case I is limited only by the source. The current limit for Case II is slightly above the current allocation. Case III, however, requires twice the normal current for the parallel redundancy and only one times the normal current for standby redundancy.

Since parallel redundancy is selected only for subsystems requiring continuous operation, Case II does not apply because in the current limit mode the input voltage to both power conditioning units decreases, thereby reducing output voltage. Case II does not apply for standby redundancy because the current limit failure would result in disabling both power conditioning units.

The failure criteria defined is for a power conditioning unit without current limiting. This criteria results in failure detector requirements to disconnect or transfer the failed power conditioner in the event of  $V_o < V_{min}$  if  $V_1 = K$  or  $I_1 > I_{max}$ . As observed from the current limiting characteristics

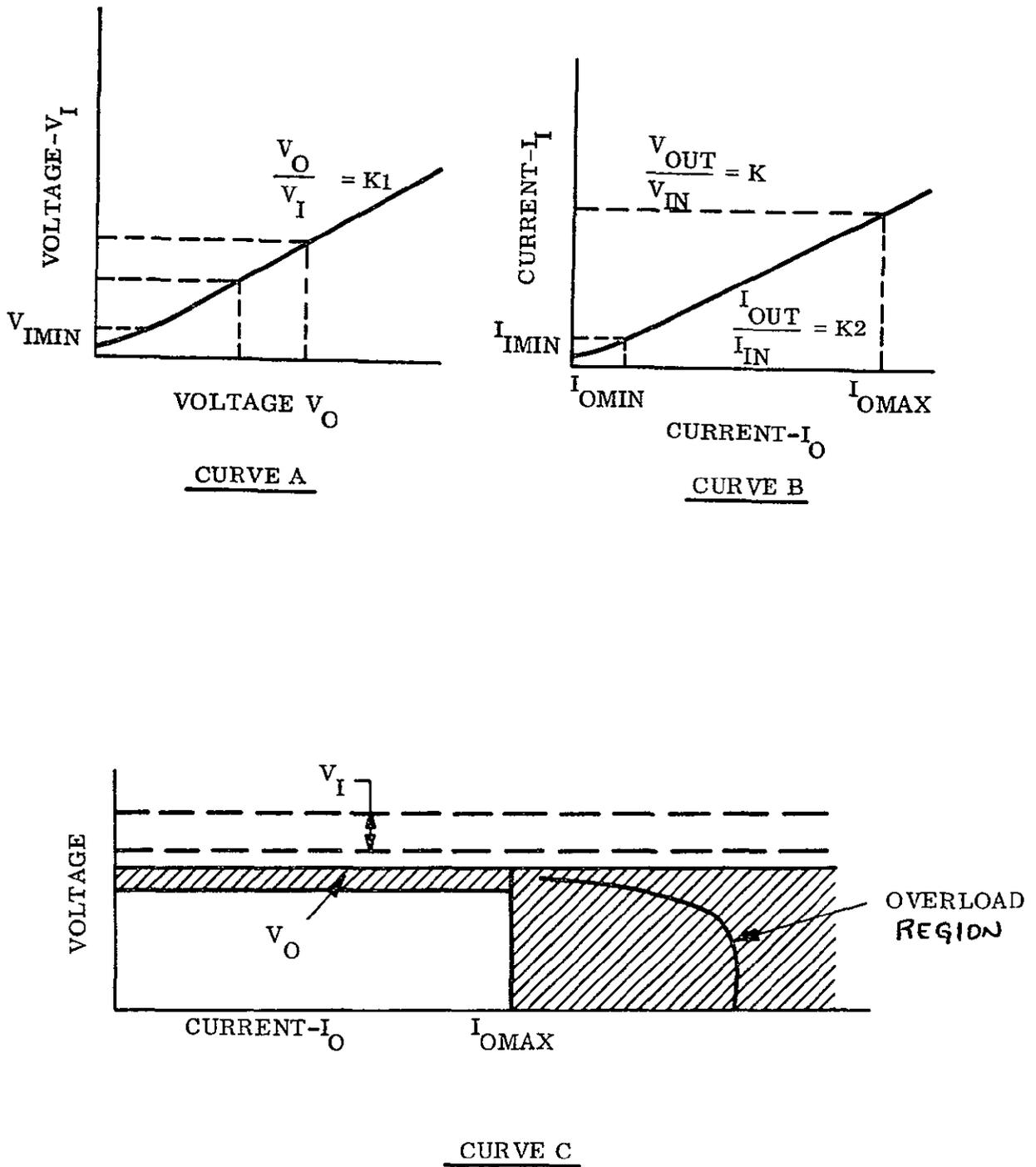
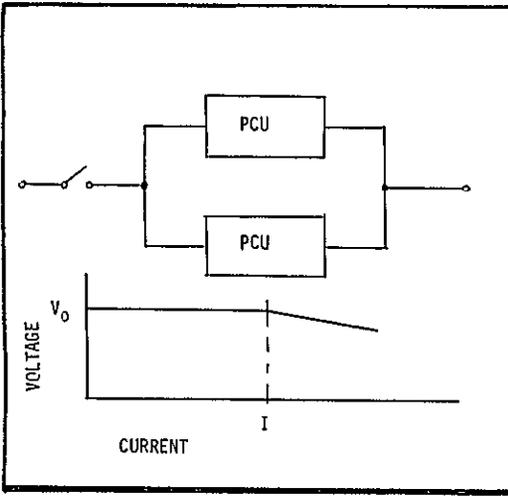
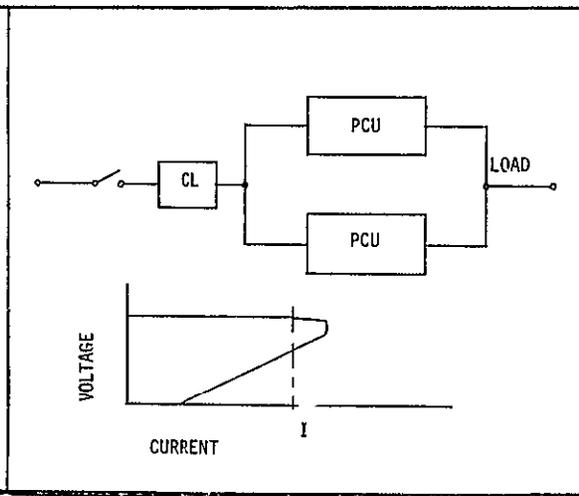


FIGURE C-4 INVERTER OR CONVERTER CHARACTERISTICS

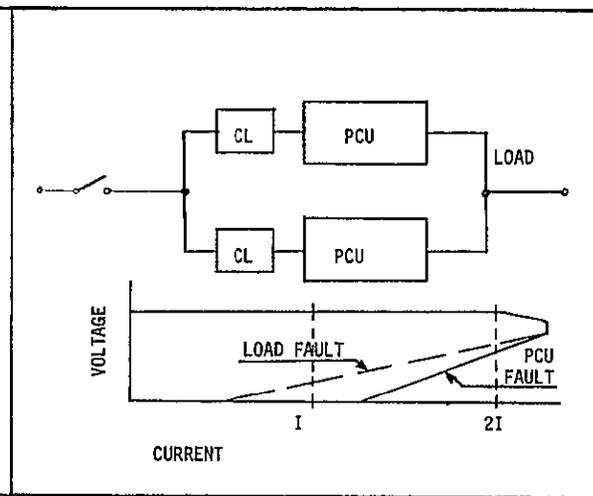
CASE I  
PARALLEL REDUNDANCY



CASE II



CASE III



STANDBY REDUNDANCY

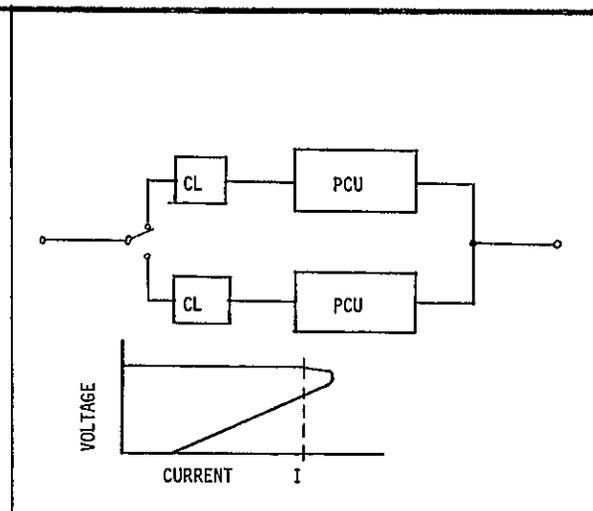
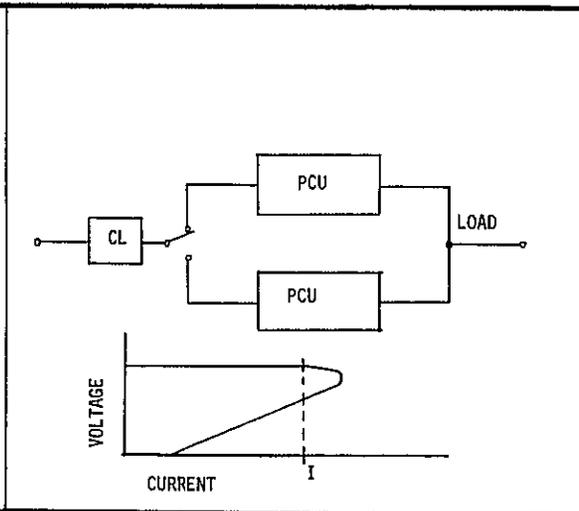
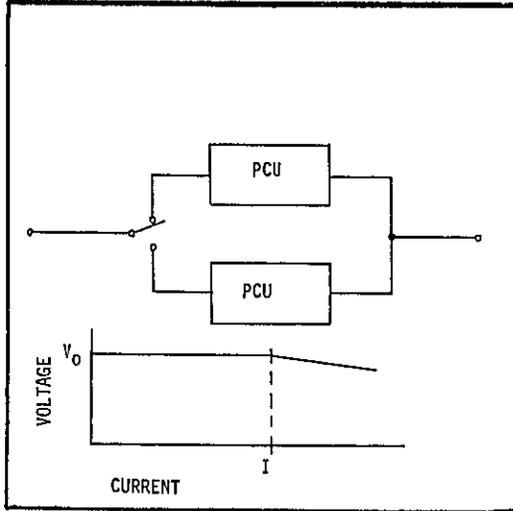


FIGURE C-5

CURRENT LIMITED REDUNDANCY CHARACTERISTICS

of Figure C-5, both input and output current is limited and  $V_0$  decreases under fault conditions. With current limiting and if a current limiter failure does not result in an increase in  $I_1$ , the failure criteria reduces to  $V_0 < V_{min}$  if  $V_1 = K$

By definition the source voltage will be constant except for periods where faults occur. Faults on the source will be removed so that the bus will return to its normal level in a finite time period. With appropriate time delays in the failure detector, the source may be considered constant. On this premise the failure criteria further reduces to  $V_0 < V_{min}$ . Table C-2 is a summary of failure criteria based on these discussions. The output voltage for parallel redundancy is by definition constant even with a power conditioner failure, therefore, a voltage,  $V_0'$ , that is representative of  $V_0$  is monitored. For completeness Table C-2 shows failure criteria for possible source and current limit failures. If input voltage and load faults are considered unlikely, the failure criteria reduces to  $V_0 < V_{min}$ .

The required action after failure of a power conditioner is to disconnect for parallel redundancy and to transfer for standby redundancy. This action is to reduce the possible source current. Without current limiting this is essential. With current limiting the actual current levels compared with the total source current margin could modify this rule.

TABLE C-2 FAILURE CRITERIA

<u>PARALLEL REDUNDANCY</u>	
Case I	$V_0' < V_{min}$ $I_1 > I_{max}$
	<ul style="list-style-type: none"> <li>• if <math>V_1 = K</math></li> <li>• if <math>I_0 &lt; I_{max}</math></li> </ul>
Case III	$V_0' < V_{min}$
	<ul style="list-style-type: none"> <li>• if <math>V_1 = K</math></li> </ul> <p style="text-align: center;">Current limiter limits <math>I_1, I_0</math></p> <p style="text-align: center;"><math>I_0, I_1</math> are always less than <math>I_{max}</math></p> <ul style="list-style-type: none"> <li>• with current limiter failure</li> </ul> <p style="text-align: center;"><math>I_1 &gt; I_{max}</math></p> <ul style="list-style-type: none"> <li>• Load inhibition is not necessary with a single load</li> </ul>
<u>STANDBY REDUNDANCY</u>	
Case I	$V_0 < V_{min}$ $I_1 > I_{max}$
	<ul style="list-style-type: none"> <li>• if <math>V_1 = K</math></li> <li>• if <math>I_0 &lt; I_{max}</math></li> </ul>
Case III	$V_0 < V_{min}$
	<ul style="list-style-type: none"> <li>• if <math>V_1 = K</math></li> </ul> <p style="text-align: center;">Current limiter limits <math>I_1, I_0</math></p> <p style="text-align: center;"><math>I_0, I_1</math> are always less than <math>I_{max}</math></p> <ul style="list-style-type: none"> <li>• with CL failure</li> </ul> <p style="text-align: center;"><math>I_1 &gt; I_{max}</math></p> <ul style="list-style-type: none"> <li>• load inhibition is not necessary with a single load</li> </ul>

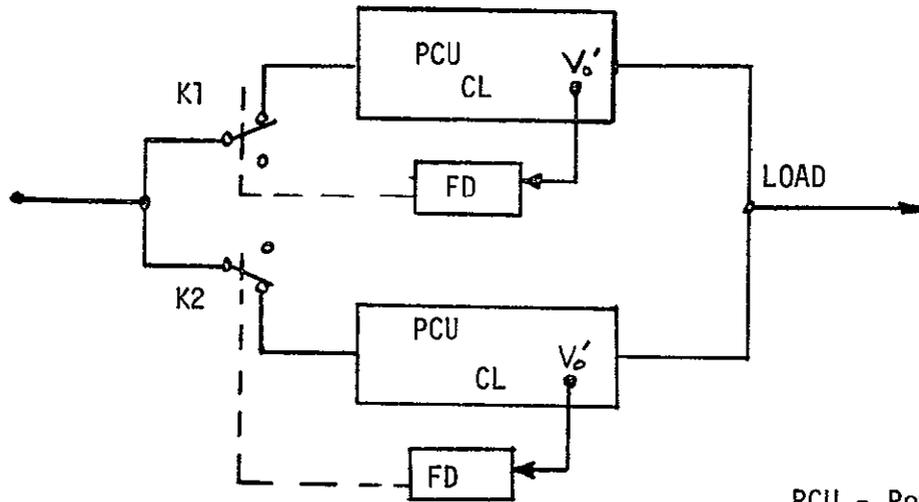
For parallel redundancy as shown in Figure C-2 the outputs are diode isolated to assure a continuous load voltage regardless of power conditioning failure. Diode isolation does not require that the outputs be switched as is the case for standby redundancy. When both the input and the output are switched, the switch should be located with the redundant power conditioning units. Failure detector requirements also suggest that the switch be located with the redundant power conditioner.

Parallel redundancy without current limiting and with a conditioner failure could draw current in excess of the source capability which would result in a load voltage decrease. In cases where the load voltage decrease is not acceptable, current limiting is essential. A general rule may be applied -- when parallel redundancy is used, current limiting of each power conditioner is recommended.

Current limiting for standby redundancy is not as critical in terms of its respective load since the load operation is interrupted when a transfer occurs. However, power conditioning faults may reduce the system distributed voltage, which could result in a power system requirement for current limiting. It was previously stated that a current limiter eliminates a detection requirement ( $I_1 > I_{max}$ ) for a failure detector. Since implementing the failure detector current sensor has the same relative complexity as a current limiter, a current limiter is recommended for the standby redundancy case, because a current limiter provides greater system utility in that source current is also controlled.

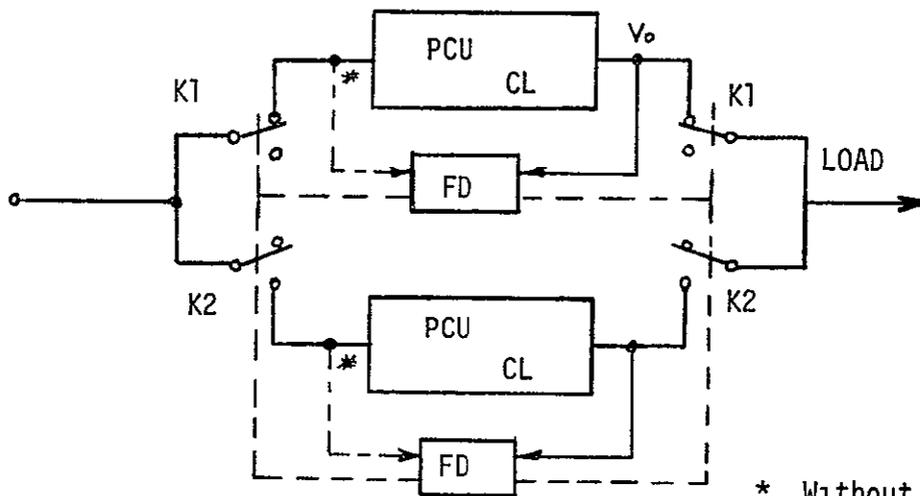
1J86-TOPS-555  
1 August 1970

Figure C-6 shows block diagram modifications of the basic redundancy configurations shown in TOPS-3-250. TOPS-3-250 should be revised to show these details.



PCU - Power Conditioning Unit  
 CL - Current Limiter  
 FD - Failure Detector

PARALLEL REDUNDANCY IA



\* Without current limiting

STANDBY REDUNDANCY IIA

FIGURE C-6 REDUNDANCY CONFIGURATIONS OF TOPS-3-250

CONCLUSIONS AND RECOMMENDATIONS

- The faulted power conditioner should be removed to reduce source current
- Switches should be located at the load when both the input and output lines are switched to minimize relay contacts and harness
- Failure Detector Conditions
  - Source faults will not occur (system design objective)
  - Single loads so not require load fault inhibits (false transfer is acceptable)
- Failure Detector Requirements
  - Parallel redundancy
    - Disconnect the failed power conditioner when
      - o  $V_o' < V_{min}$
      - o  $I_1 > I_{max}$  (without current limit)
  - Standby redundancy
    - Transfer failed power conditioner when
      - $V_o < V_{min}$
      - $I_1 > I_{max}$  (without current limit)
- Both redundancy methods require command access, fault verification, and a time delay to reduce false trips due to transient conditions

- Recommendation

Use current limiting for configurations with redundant power conditioners

Application of current limiting reduces failure sensor requirements, and a current limiter failure is assumed not to result in high input current unless the load has also failed

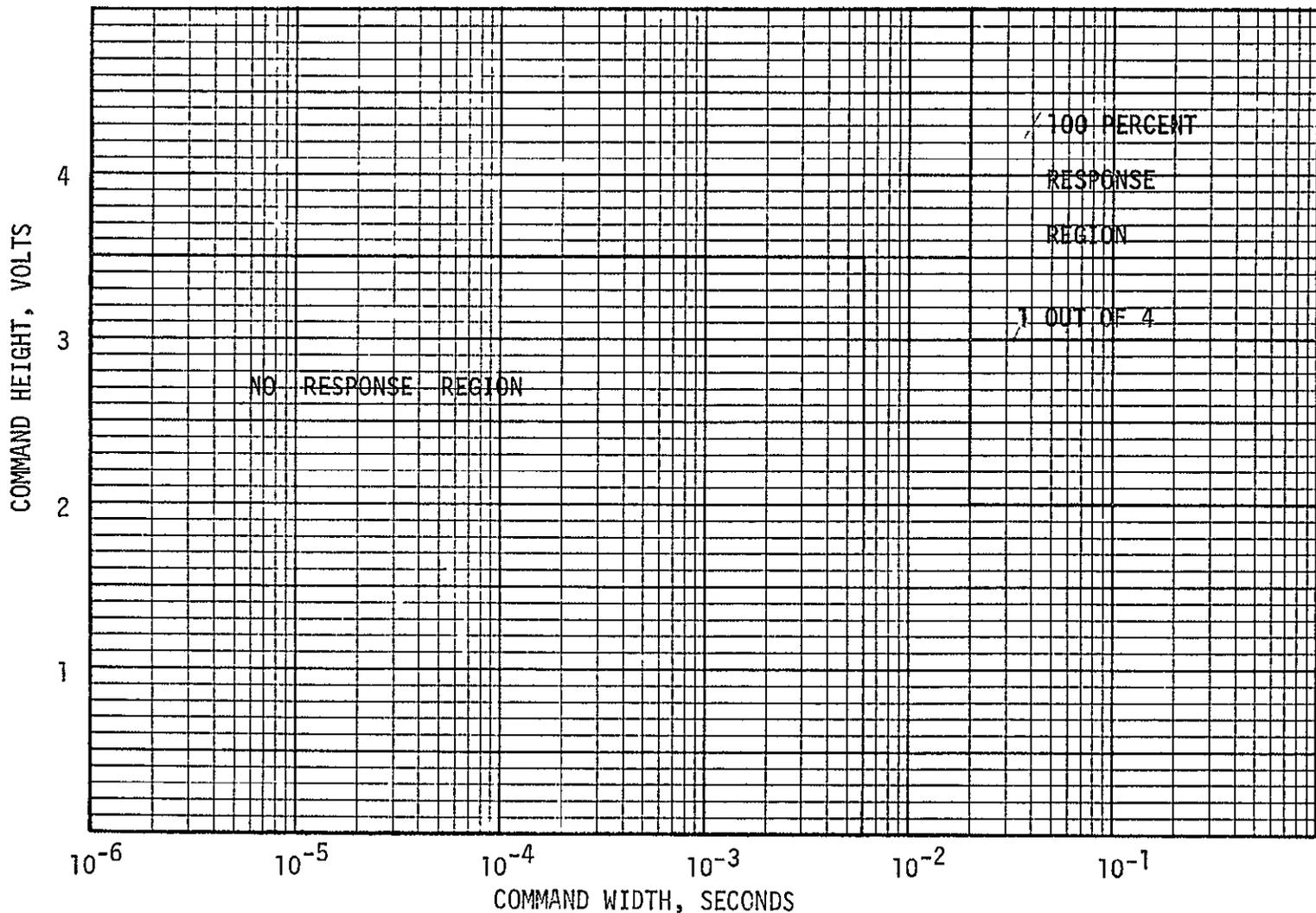


FIGURE D-4 SOLID STATE TURN-OFF CHARACTERISTICS

1 J86-TOPS-555  
1 August 1970

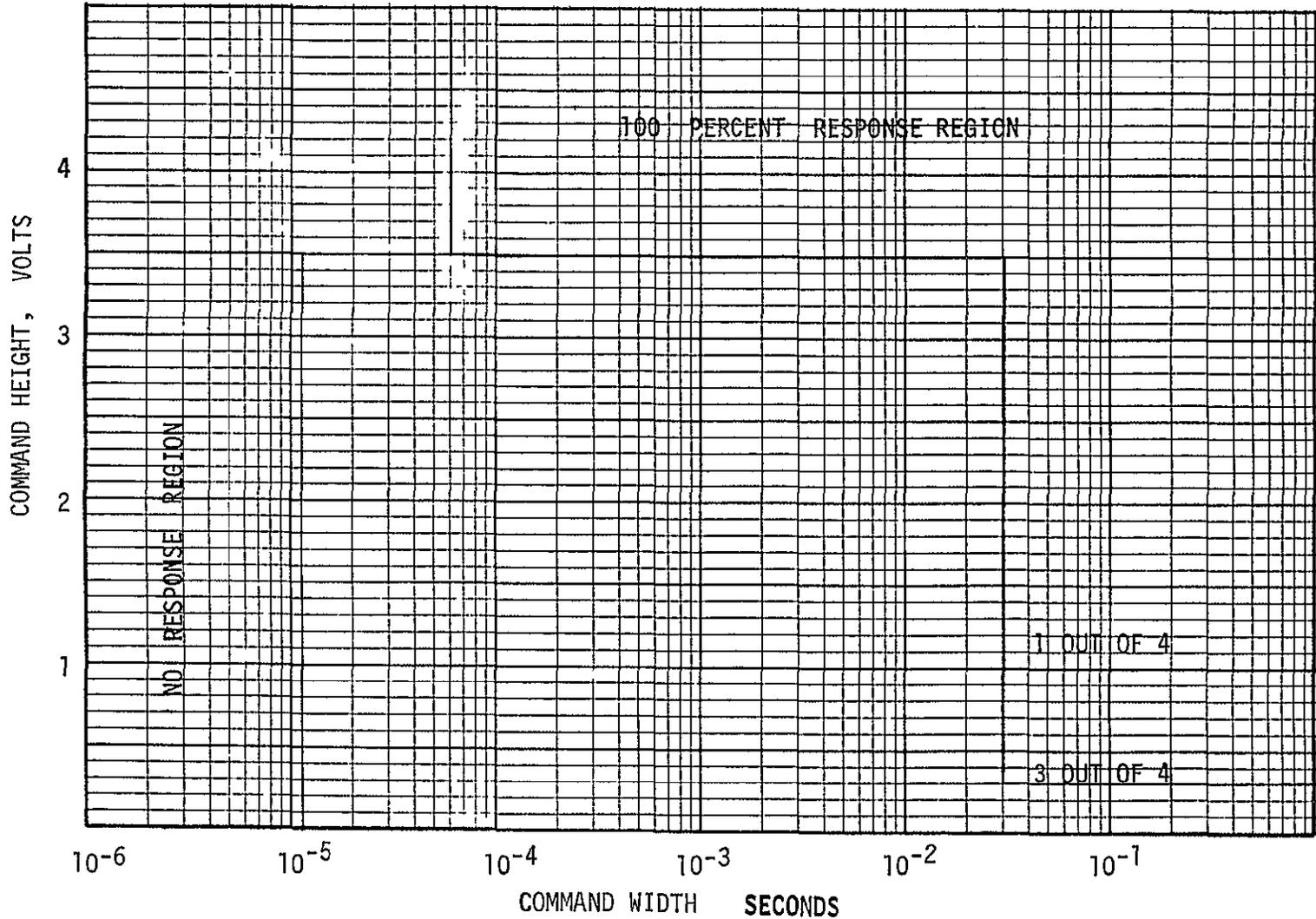


FIGURE D-5

RELAY SWITCH ON/OFF CHARACTERISTICS

1J86-TOPS-555  
1 August 1970

Generally the CCS interaction with the power system will be to control the power applied to the various loads. This control will depend on the particular mission sequence, the using subsystem health status, and the power margin. As long as the using subsystem is functioning normally and sufficient margin is available, operations can proceed according to planned sequences.

Under an imminent fault condition, the using subsystem monitors will detect the impending malfunction and route this information to CCS to enable corrective action in accordance with a stored program as a normal subsystem function and independent of the power status. An example of this is a saturated or shorted momentum wheel that does not respond to pulsed power. This is the first and normal corrective action implemented by CCS.

The second tier of using subsystem corrective action is implemented with power status monitors within the using subsystem as a part of their failure detection and corrective action requirements, and completely independent of all power subsystem functions except the principal one of providing power.

The third tier of corrective action is a power subsystem function implemented by CCS using a shunted current status monitor to determine power margin. If margins are insufficient, the CCS, through stored instructions, withholds power according to some priority criterion. As presently visualized, status information for margin determination will be multiplexed and distributed in a manner similar to the telemetry information.

The first three fault detection techniques do not result in an out-of-specification of any equipment except that responsible for the fault. There is no time criticality or race condition. However, the fourth tier of corrective action depends on an undervoltage condition on the main bus for detection, and the total processing time of the CCS to sample the fault, determine the corrective action, and issue the appropriate commands, including switch actuation time. Added to this must be a delay to prevent nuisance trips on short transients.

These first four tier corrective measures depend on CCS to detect the existence and location of faults, overload conditions or other abnormalities and to determine where and how corrective measures should be applied. Such corrective actions will generally involve switch actuations for load removal or the transfer from main to standby units as shown in the case of the main DC/AC inversion chain. It is estimated that 30 milliseconds maximum would elapse from the onset of a fault condition until total corrective action took place.

The Low Voltage Cut Off function serves as a back-up to the four CCS methods described above, and accomplished a powered-down mode by initiating simple, preprogrammed corrective actions. The existence of a voltage less than 27 VDC at the output of the RTG diodes for 100 milliseconds or greater is used as the criterion for initiating the corrective actions. Tentatively these actions would be

- a. Send a priority signal to CCS to backup the CCS power system undervoltage detector described under tier four above. This signal could precede any actions at the end of the 100 millisecond delay.
- b. Transfer power from main to standby elements within critical load categories.
- c. Transfer from main to standby power conditioning elements at the main bus and at each load with power conditioning redundancy.
- d. Interrupt power to all non-essential loads thru a single command to a multiplicity of load switches.
- e. Interrupt power to a single non-essential bus thru a single relay actuation.

The above actions may be carried out concurrently or sequentially, a factor which may be resolved more appropriately during system development tests.

## APPENDIX E ENERGY STORAGE STUDY

The concept of electrochemical energy storage was investigated to determine advantages, operational flexibility, and increased capacity to sustain failures that would accrue with the addition of a battery to the TOPS mission

The most important consideration with a long-term flight battery revolves around the high degree of operational flexibility provided. Principally batteries permit the application of loads greatly in excess of those capable of being satisfied by the prime power limited RTG source. Additionally, through power averaging, they potentially permit a reduction in the capacity of the prime power source. This can represent large cost savings because of the high expense of isotopic fuels. Evaluation of these and other factors is provided in this analysis.

### A Power Averaging

The load profile chart indicates a maximum power requirement of 460 watts during the Far Encounter phase of any particular planetary pass. This phase may last as long as twenty hours. For each watt supplied by nickel cadmium batteries (the only reasonable contender for the life requirements involved) the weight penalty is 2 pounds considering an energy density of 10 watt-hours/per pound and operation for 20 hours. For the contemplated RTG's, the weight penalty is about 0.5 pounds per watt. Thus the weight penalty of battery averaging is at least four times as great as increasing the RTG size to provide direct power. With depths of discharge less than 100 percent (decreasing the effective

energy density) and taking the losses of discharge conditioning into account the weight penalty difference is even more pronounced. For these reasons the use of batteries for power averaging cannot be justified for the TOPS mission.

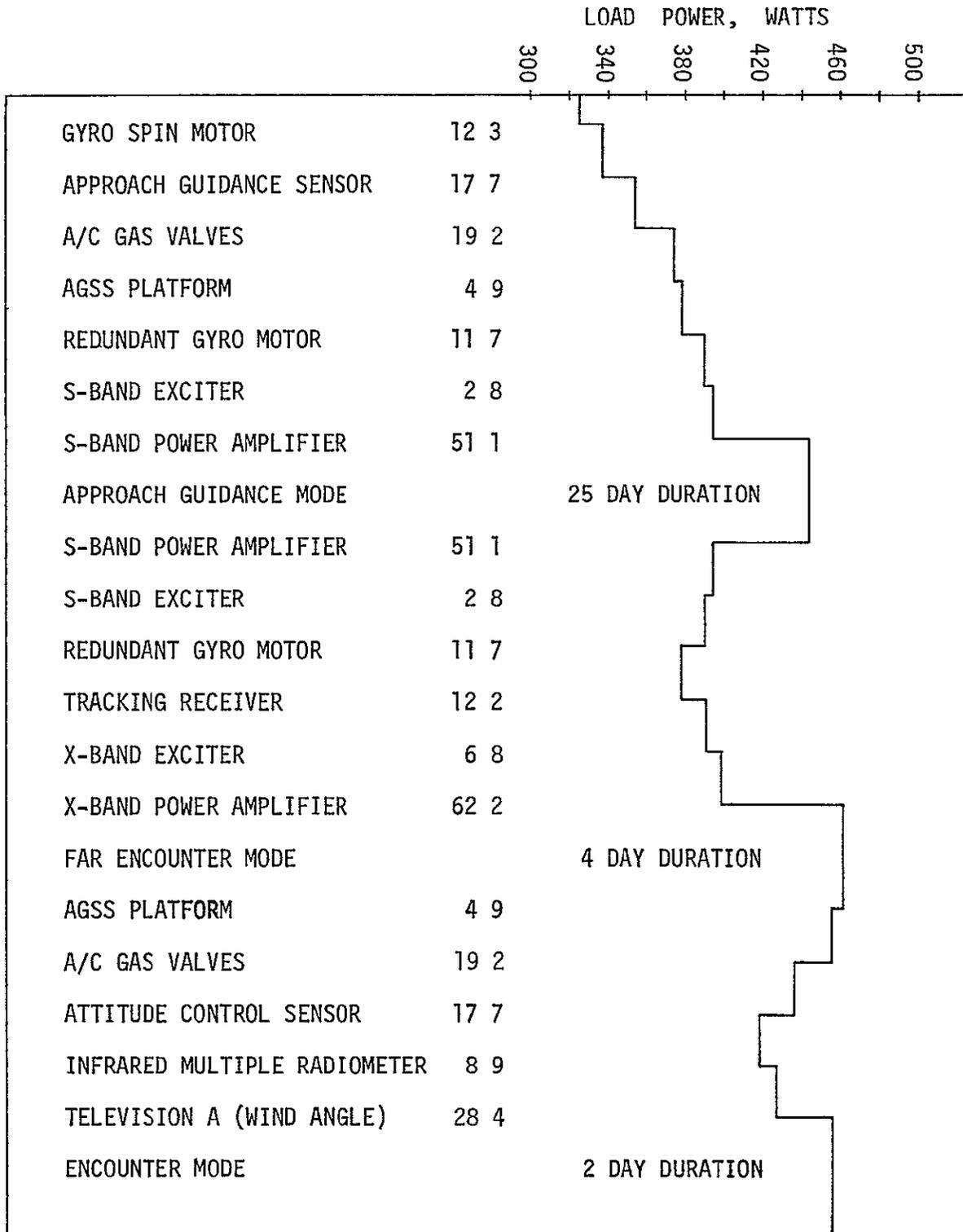
B Operational Procedures

Maximum power is required in the Far Encounter Mode. The loads switched on or off immediately before or after this mode were analyzed to define the minimum power and power margin for transient conditions. These loads are presented in the bar chart of Figure E-1. Prior to the Far Encounter Mode, the only applied load sequence is the tracking receiver, X-band exciter, and X-band power amplifier. This sequence is fixed by equipment characteristics, and requires that the last load applied is the largest, the power amplifier at 62.2 watts. The only alternative is to turn off other equipment that had been on to reduce the power demand during the power amplifier transient. These other loads must then be reapplied after the power amplifier has stabilized.

There is an inherent risk in needlessly disturbing a quiescent state, and the TOPS project decision on this question has been to reject any attempt to add artificial load sequencing in lieu of adequate power margin. In any event, the twenty hour duration would preclude any weight advantage with a battery, but would aid in reducing the effects of turn-on transients.

FIGURE E-1

TYPICAL LOAD SEQUENCE AT PLANETARY ENCOUNTER



C High Current Pulse Loads

Particular pyro loads cause short duration power demands significantly over and above those listed on the power profile. Suitable methods for supplying such loads are through the use of (1) capacitor - bank systems of the type used on previous Mariner - Class spacecraft, and (2) thermal batteries which have been used for many high current short pulse duration applications. These systems are reliable and are suitable for the 12 year TOPS mission, and eliminate batteries from further consideration.

The attitude control system uses six individual momentum wheels, two in each axis, with power to only one wheel at any instant except during a commanded turn. Power for the wheels is provided by a chain of pulses, each of two hundred milliseconds duration, that are time shared by the wheels as required. The logic samples each axis in turn and delivers, at most, one pulse to each axis in sequence. If no error signal exists in a specific axis when its turn comes up, the logic steps on to the next axis without delay. Additionally, the logic routes the pulse to only one wheel in each axis, maintaining the second wheel in stand-by. When a wheel nears saturation, it is dumped by the gas valves, and it takes two minutes to dump one wheel.

A single wheel is allowed to saturate during data transmission when the gas valves are inhibited. At this time the stand-by wheel is activated and the logic routes the power pulses to this wheel.

The spacecraft can do a commanded turn on wheels alone, and for this maneuver, both wheels of one axis are on continuously until the turn is complete

This indicates that wheel power may be considered low energy pulses, with a maximum full wheel power pulse of two minutes. The battery could be considered capable of furnishing two-minute pulses, or a chain of two hundred millisecond pulses with a total chain time of two minutes

The battery energy required is 11 watts for two minutes, or for fifty per cent depth of discharge a battery capacity of nominally 0.75 watt hours. Some additional capacity would be required if turns could occur back-to-back, and complexity would be required in terms of battery charging and discharging electronics

The solenoids for the gas valves consist of two in series, and are driven by a minimum pulse width of twenty seconds, but could be fired continuously until errors are brought to within the coarse rate roofs. The worst case is three axes firing continuously and simultaneously, as for example, after midcourse correction or in the event of impact with another body. During any of these periods, the momentum wheels are inhibited until the errors are brought to within the fine dead bands

The worst case solenoid power is thus three axes, two solenoids in series in each axis, two watts per solenoid, for a total of 24 watts. Since impact by a foreign body can occur at any time, such as during encounter, the power system margin must include sufficient watts to permit firing all three axes. Since momentum wheels would be inhibited, the net power margin for this mode is

24 watts required - 11 watts allocated for wheels -  
4.8 watts allocated for one axis solenoids = 8.2  
additional watts over the TOPS 3-250 allocation

The available specific impulse from the gas tanks is 180 seconds, and the total expendable gas is 120 pounds. To expell all this gas thru a set of two valves rated at sixty millipounds each would require fifty hours. For a nominally 100,000 hour Grand Tour Mission, this results in a duty cycle of 0.05% on the total gas valve system.

These valve pulses may be considered low energy pulses also, with a maximum probable duration less than two minutes. However, no upper limit on duration has been applied to valve firing. In any event, momentum wheel power and solenoid firing are logical candidate loads to be drawn from a battery if one is provided.

If energy storage is provided for these pulse loads, a back-up capability must exist to operate these pulse loads in a powered down mode if the

energy storage system fails. The nature of the radioisotope decay and thermoelectric generator degradation is such that a system sized to be adequate at last planetary encounter will have excess power at all other mission phases. It seems more realistic to consider that power demand will have diminished also thru loss of some experiments during the mission, rather than provide long-term energy storage for a ten year mission to satisfy the last twenty hours.

D Ripple Current

Analysis of steady state ripple in Appendix A indicates that filter designs which provide minimum system weight result in currents which may be 4 per cent higher than that indicated by steady state loads.

Thus the RTG power should be at least 4 percent higher than the indicated demand. The presently defined loads and RTG performance estimates indicate less than 4 percent margin for the last encounter. Since the RTG performance is of a preliminary nature this margin deficiency cannot be fully evaluated at this time other than to bring attention to this potential problem. Solutions may lie in increasing the RTG capability or possibly in accepting degraded mission performance by removing certain less essential loads.

E Degraded Mode

In general the notion of degraded mission modes must be considered for the case where one or more RTG's fail to produce power. The RTG's

are arranged to permit such failures without endangering the remaining RTG's through the use of isolation diodes and modularized shunt regulators. The mission worth under such degraded power conditions has not been evaluated as part of this study since such an evaluation can be more suitably performed as an aspect of overall system performance. As an aid in considering degraded power operations, Table E-1 indicates power margin at various encounter phases considering the loss of up to two of the four RTG's.

TABLE E-1 RTG POWER MARGIN, WATTS

Number of Operable RTG's	ENCOUNTER		PHASE	
	Jupiter	Saturn	Uranus	Neptune
4 out of 4	125	90	38	10
3 out of 4	-20	-48	-86	-108
2 out of 4	-168	-185	-211	-225

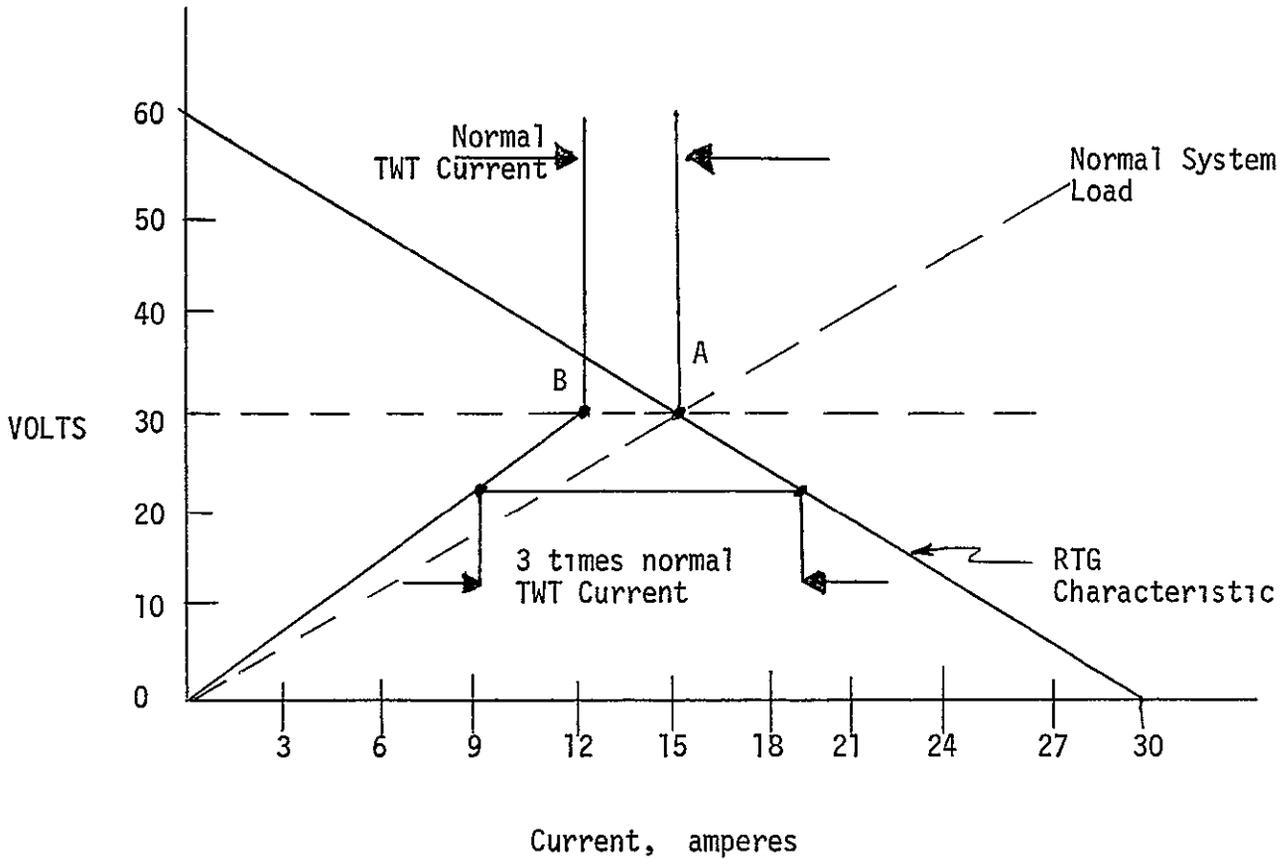
A cursory review of the power profile loads provides a measure of the practicality of degraded power operation. With the failure of one RTG at the Jupiter encounter, for example, the 20 watt deficiency indicated on Table E-1 could possibly be compensated by reducing heater power or removing several of the less significant science loads for the "Far Encounter" phase. Time sharing of certain loads may provide alternative solutions. For later encounters or larger RTG losses, severe changes in operation would appear necessary.

F Fault Clearing Capability

Analysis of each wire run is made to insure that there is a positive means of protecting the bus from a load fault, either by an in-line throttle to limit the current, or by opening the circuit by one-time fusing, circuit breaker or relay action, or by actually supplying sufficient energy into the fault to burn open the feeder supplying the fault. This last imposes a requirement that loads be separated into essential and non-essential feeders, and suggests that the power limited RTG be augmented with energy storage to provide the short duration power pulse required to fuse the wire

The high current possible with batteries make them ideal for fault clearing purposes. However, the RTG's may also have sufficient fault clearing capability. An estimate of this capability is provided below to determine if the battery is necessary for this purpose

In this estimate it is assumed that all loads are fused and that any fault may be cleared with a current at 3 times the normally rated load value by blowing the fuse. The figure below shows the relationship of the RTG voltage-current characteristic to the load characteristics. This relationship as shown assumes a nominal load of 460 watts with the RTG just capable of supplying this power. This represents a situation which might exist at the Far Encounter phase of the last planetary encounter



Point A represents the normal operating point with the system drawing 15.3 amps at 30 volts from the RTG. The TWT is the largest load and is rated at about 60 watts. Point B indicates the current drawn by all loads except the TWT. The load line through the origin and point B represents the impedance of these loads assuming they are purely resistive in nature. Assuming a complete short in the TWT, the system voltage would be depressed increasing the RTG current output. At 20 volts or lower the current through the TWT fuse would be larger than 3 times the normal rating and the fault would be cleared.

In the above example the largest load of the system was used. The clearing capability for smaller loads would be that much better. The conclusion is that sufficient fault clearing capability exists with the RTG's, and the use of batteries for that purpose is unnecessary. However, a transient undervoltage would be impressed on the vehicle, and all loads would have to be specified to withstand the undervoltage and recover to normal operation.

#### G Reliability

Reliability data for aerospace battery systems for a time period of 12 years is not available, but a preliminary assessment has been made based on published cell failure rates for one to six years, and extrapolated to 12 years (see Figure E-2). The resulting reliability numbers may be optimistic, but provide a basis for further study and point out the advantages of reducing the number of series cells in a battery. The "high voltage divergence" failure mode shown on Figure E-2 was not considered in the analysis since it was assumed that the low rate battery charging used in this type of application would not lead to this problem. The other three failure modes shown on Figure E-2 were summed up to produce Figure E-3. In this analysis it is assumed that the failure of any one cell by any of the failure modes is a failure of the battery.

Figures E-4, E-5 and E-6 are the calculated results using only the failure rates from Figure E-3. For a 12 year requirement, it is of interest to see

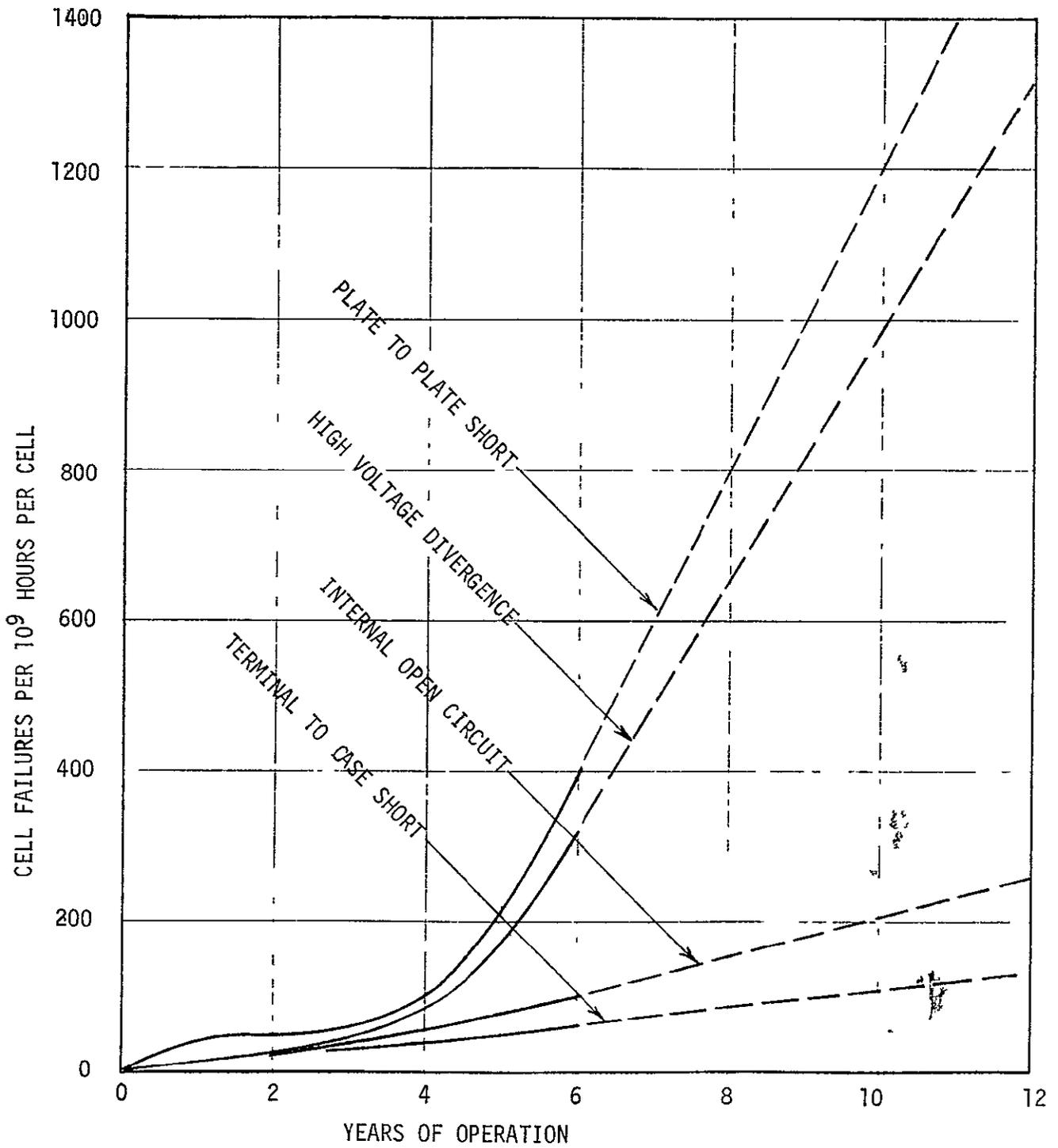


FIGURE E-2 CELL FAILURES DUE TO SEPARATE CAUSES

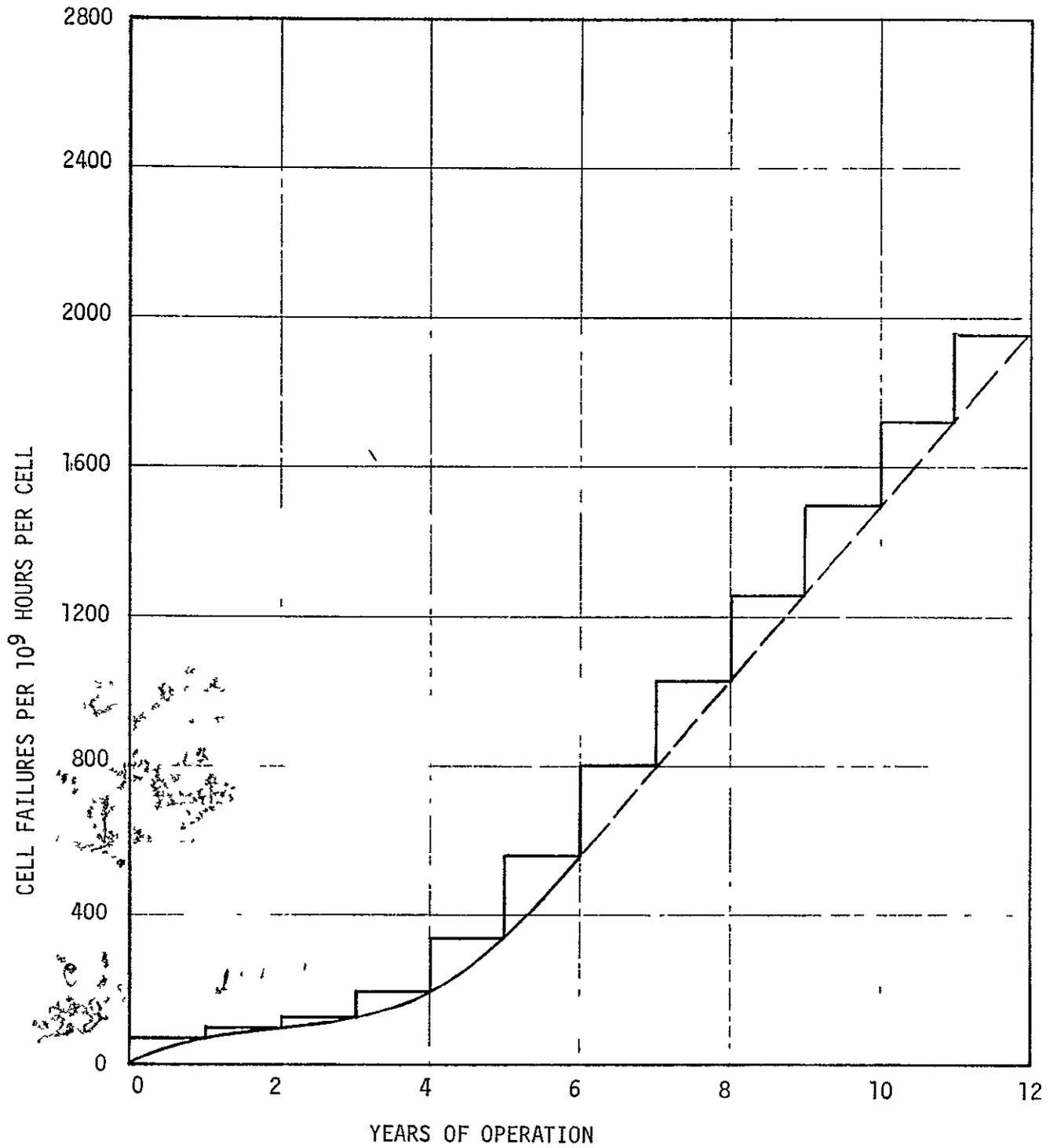


FIGURE E-3 CUMULATIVE CELL FAILURE RATES

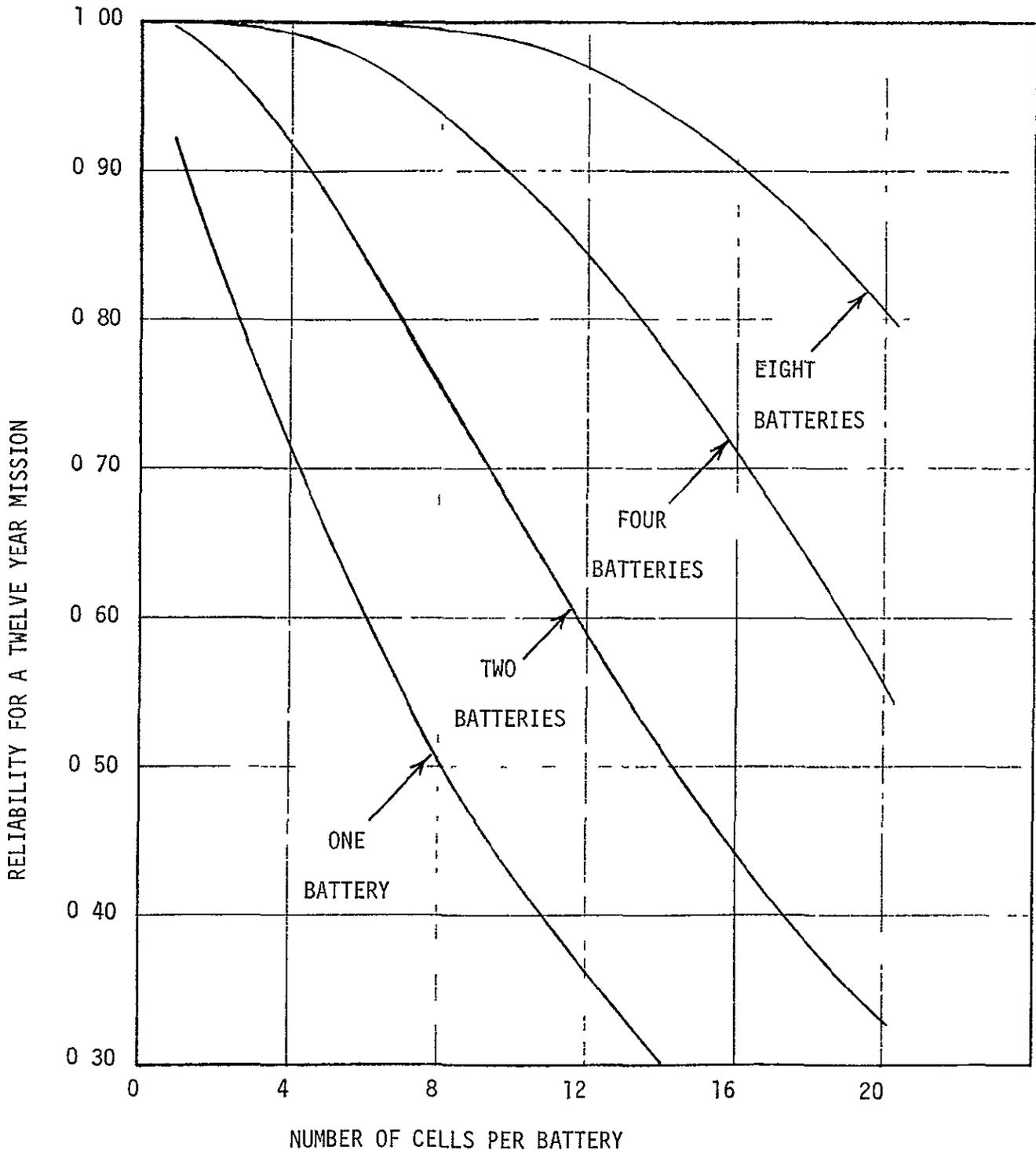


FIGURE E-4 RELIABILITY FOR A TWELVE YEAR MISSION

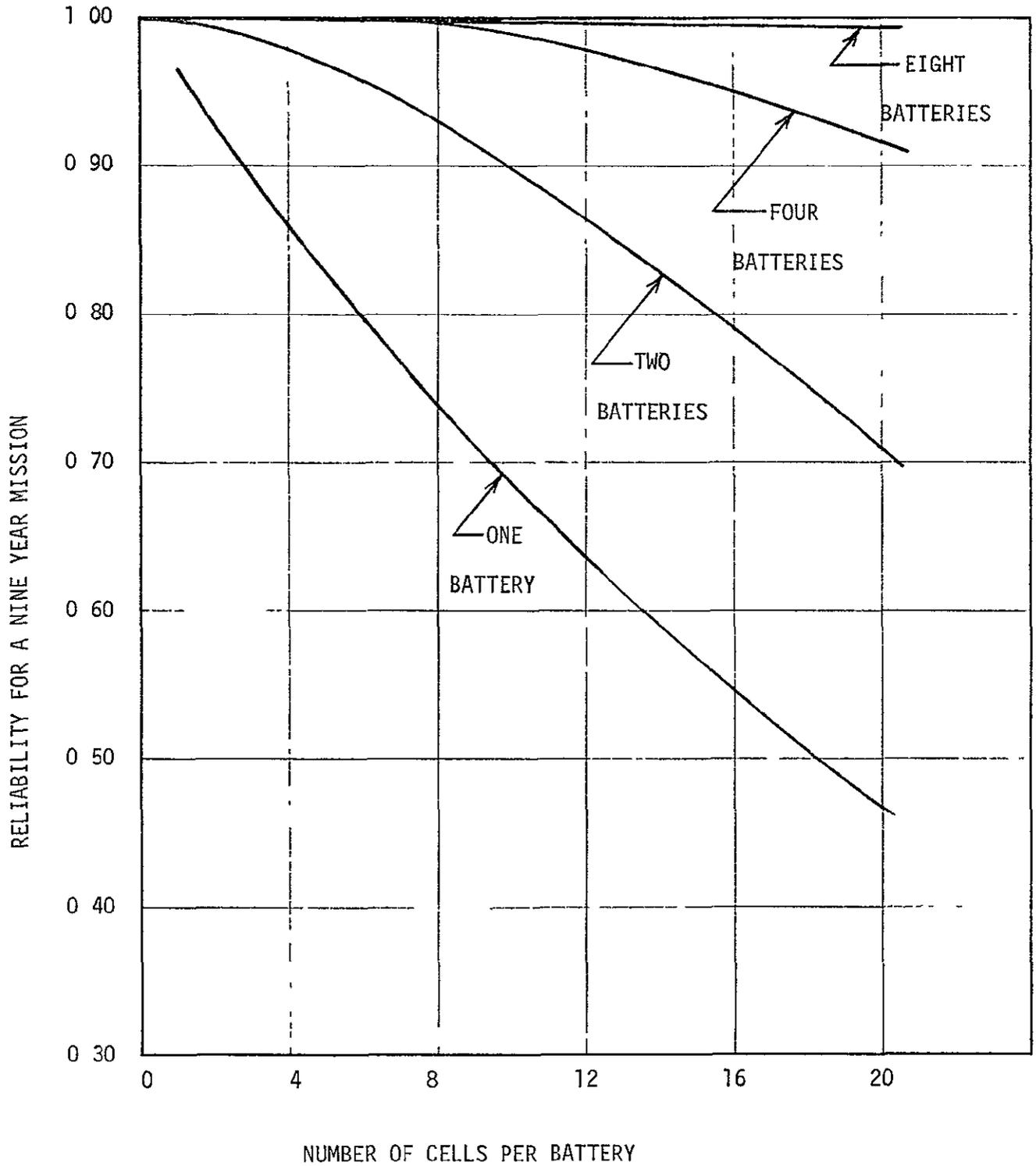


FIGURE F-5 RELIABILITY FOR A NINE YEAR MISSION

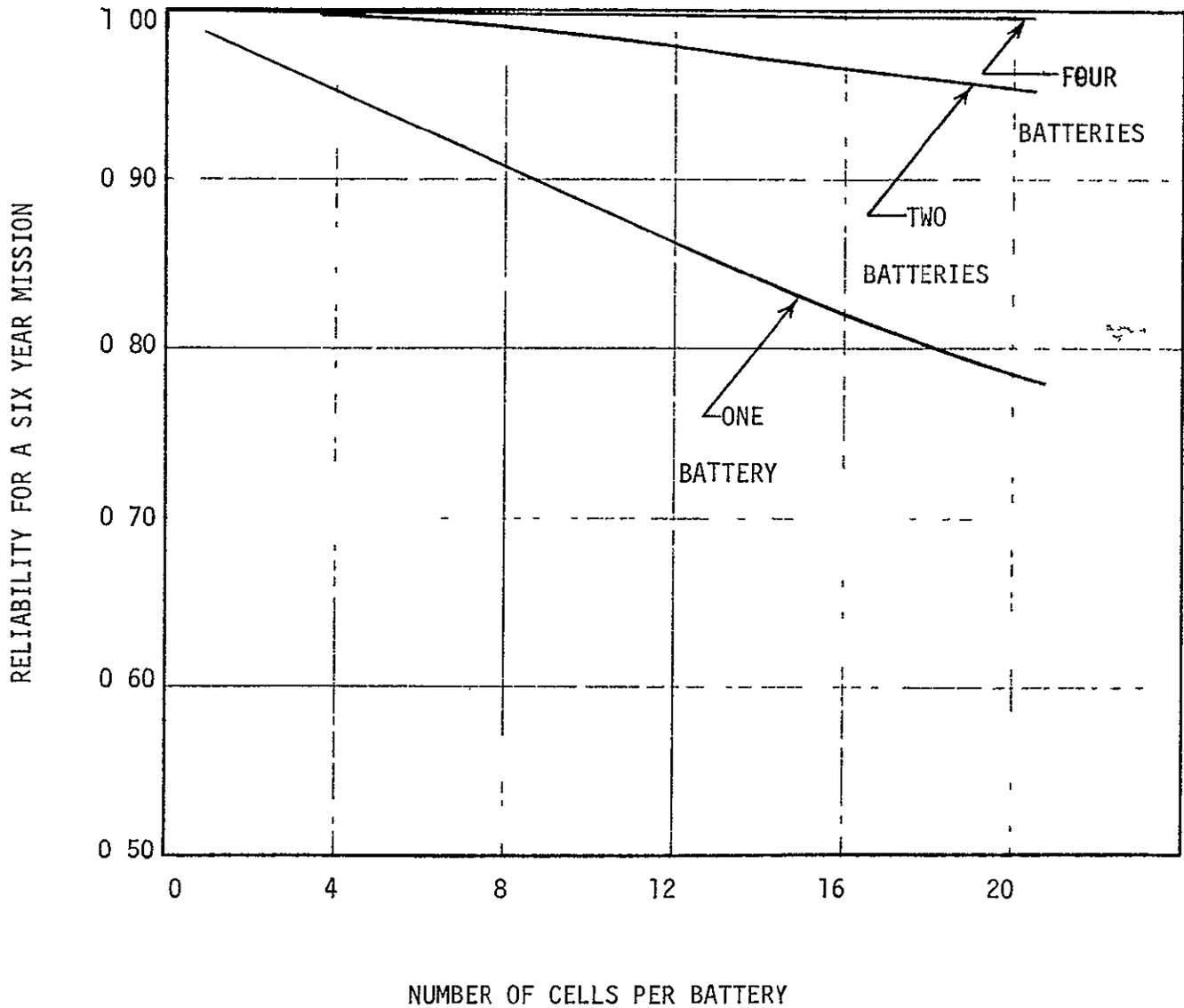


FIGURE E-6 RELIABILITY FOR A SIX YEAR MISSION

the great impact of the number of cells in series. The curves indicating 2, 4 and 8 batteries were calculated on the basis that one battery is required and all additional batteries are redundant. The 9 year and 6 year reliability calculations were made primarily to derive the curves in Figure E-7 to show the decreasing reliability with life requirement. The curves of Figure E-7 for two 4-cell batteries and two 20-cell batteries are cross plots from Figures E-4, E-5 and E-6, and any other combination of series cells and redundant batteries can be plotted similarly.

Any present commitment on the use of a long-life battery for TOPS would be made without the benefit of a demonstrated 12 year life capability. This is probably the most important single fact against the use of a long-life battery. Aside from this, the possible leakage of electrolyte may endanger other spacecraft equipment and possibly interfere with certain science measurements. Reliability is also compromised as a result of the additional integration complexity involving such functions as charge regulation, discharge regulation, battery temperature control, etc.

#### H Turn-On Transients

Another factor affected by power margin concerns the system response to step load changes. The traveling wave tube (TWT) represents the largest load increment in the spacecraft system. As presently designed the TWT could incur significant voltage transients (to 50% of nominal regulation)

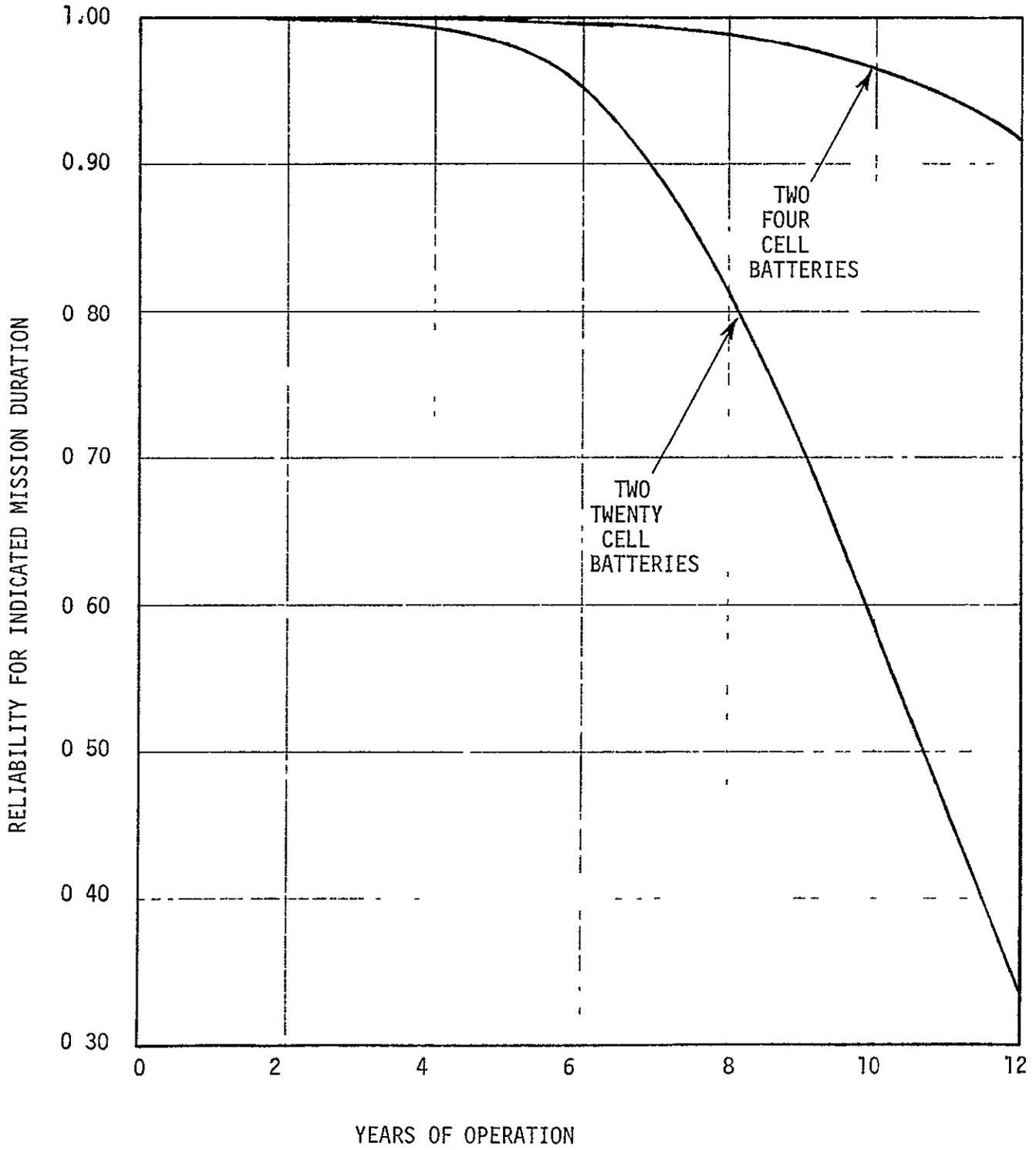


FIGURE E-7 RELIABILITY OF MULTIPLE CELL SYSTEMS

for periods lasting 20 to 30 milliseconds. Avoidance of this transient by increased margin does not appear practical since the inrush current is on the order of 4 to 5 times larger than steady state values. It is believed that this transient could adversely affect the overall system, possibly to the extent of causing false indication of failure which could initiate certain corrective sequences within the CCS or Low Voltage Cutoff (LVCO). Further study of this problem is necessary which may involve changes in the TWT circuitry, revisions in the general approach for sensing faults and initiating corrective action, or combinations of such changes.

Many continuous loads whose steady-state demands would be satisfied by the RTG have high starting current characteristics. The TWT mentioned earlier provides a case in point. Batteries would seem to minimize the turn-on transient disturbances. However, a variety of suppression techniques can also be employed to minimize transients and these should be thoroughly investigated before a battery is used for transient suppression purposes.

#### CONCLUSIONS

The use of long-term flight batteries for TOPS appears neither necessary nor desirable. The principal benefit of batteries would be to reduce turn-on voltage transients. It is considered that other less complex techniques can be used to relieve such transients. These would include a variety of suppression circuit techniques and the judicious application of filters to the more sensitive loads.

## APPENDIX F TRANSFORMER OPTIMIZATION STUDY

A computerized study was made to locate the optimum frequency-flux-material combination for transformers in the TOPS power subsystem

The optimum transformer occurs when an incremental decrease in weight would cause an incremental increase in lost power at a rate of 1.7 watts per pound

### Analysis Technique

A computer program was written to study five transformer types: Orthonol, 48 Alloy, and Supermalloy toroids, and Sillectron and Supermalloy cut C Cores. 48 Alloy was subsequently deleted because it did not differ significantly from Orthonol. Figure F-1 presents the physical construction of the transformers. Core dimension D was slowly increased and the window area completely filled with wire using the same amperes per square inch (ASI) for all windings and allowing very high ratings (24000 ASI) to start with small cores. As the iron area increased, the turns decreased and the window area increased, allowing the ASI to decrease rapidly. The program thus calculated sets of curves for different fluxes and frequency as illustrated in Figure F-2.

Two frequencies, for which there were core loss curves available, close to the 4 and 8 kilohertz sync frequencies were selected for close study. The effect of switching losses in the transistors was included to get a better tradeoff versus frequency. Specific formulas used are listed in Table F-1.

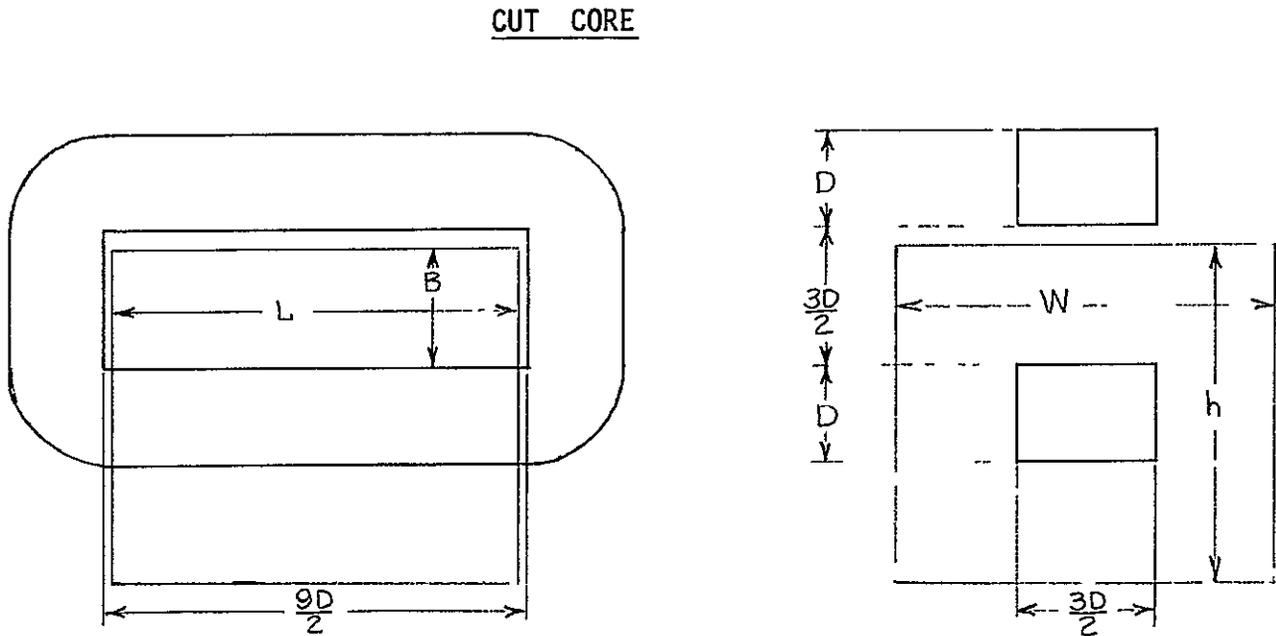
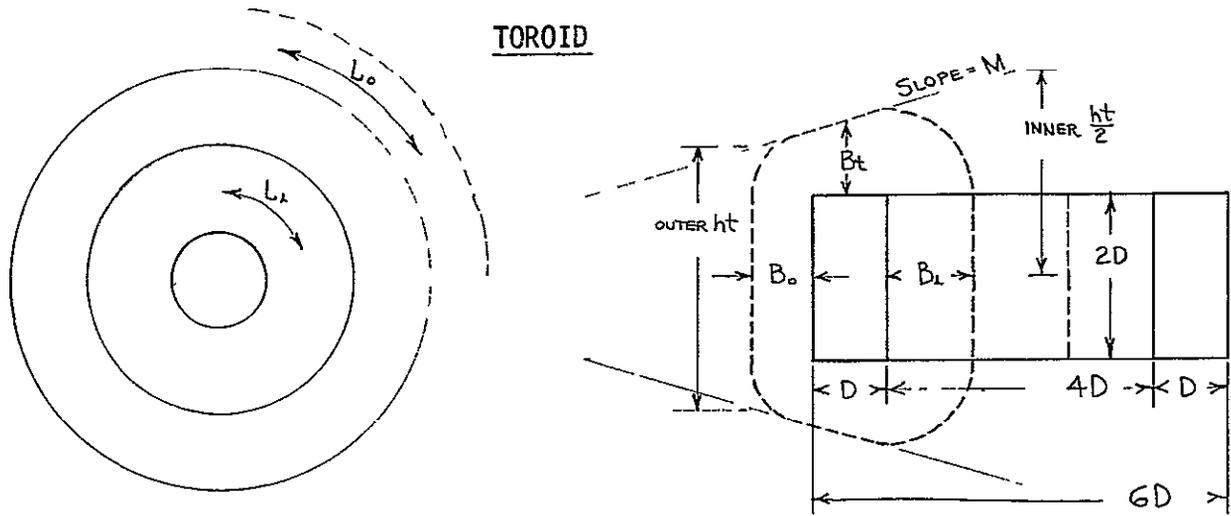


FIGURE F-1 TRANSFORMER PHYSICAL CHARACTERISTICS

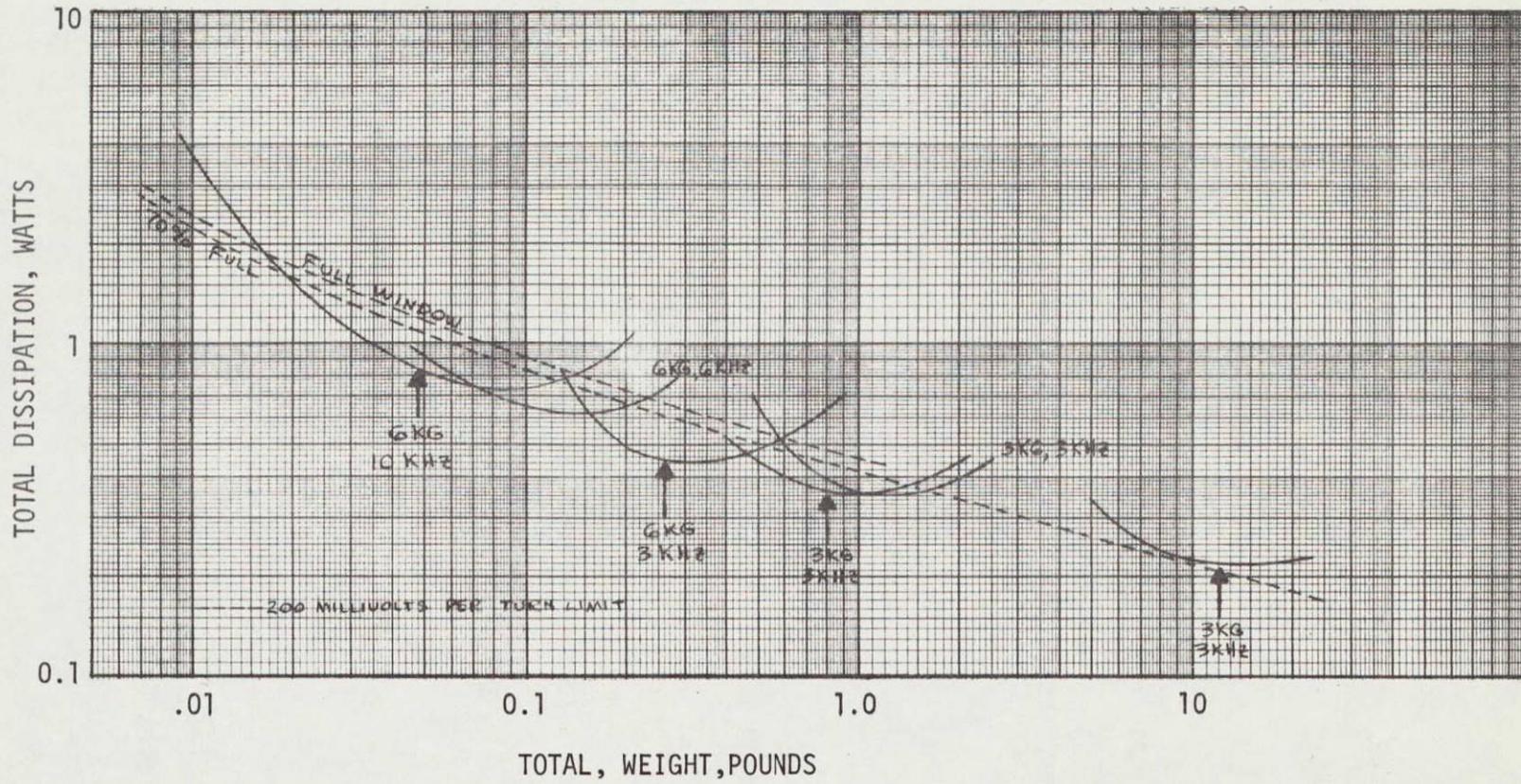


FIGURE F-2. OPTIMIZED MINIMUM DISSIPATION SUPERMALLOY TRANSFORMERS

TABLE F-1 FORMULAE

GENERAL

Usable Window = window x % Usable (WF) x Copper Stacking Factor (SF)

Area Current =  $\sum_{i=1}^{N \text{ windings}} K_i N_i A_i$

K = 2 for Center Tap  
N = Number of turns  
A = Current  
i = Winding Index

ASI = Current Area / Usable Window

Copper Power Dissipation =  $\sum_{i=1}^{NW} \frac{\text{sigma} \times \text{Mean length} \times (A_i N_i)^2}{N_i A_i / \text{ASI}}$

Winding Build =  $\frac{\text{Area Current}}{\text{ASI} \times \text{WF} \times \text{SF}} \div \text{length for the winding (L)}$

Toroid:

Winding Length (L) =  $2 \Gamma P \times \text{Radius from center for that winding}$

Core Volume =  $10 \Gamma P D^3$

Winding Volume =  $\Gamma P [(ht \text{ inner} + M \times R_i) (R_o^2 - R_i^2) - M/3 (R_o^3 - R_i^3)] - 10 \Gamma P D^3$

Where  $R_o$  = radius to outside of winding

$R_i$  = radius to inside of winding

C-Core:

Core Volume =  $24 D^3$

Winding Volume =  $h \times w \times 4.5D - 6.75D^3$

To get results most applicable to the expected requirements, a limit of 200 millivolts per turn (maximum) was imposed since five volt outputs are often required, and this granularity is required to adjust the output voltage level.

The computer program then calculated transformers by incrementally increasing the iron area (at a given flux and frequency) and filling the resulting window area with turns. The first transformer design accepted is when the ampere turns divided by the window area results in an acceptable ASI. The wire, core, and switching losses are then calculated along with weight, and "remembered". Additional designs are then calculated (by increasing the iron) until the total power loss exceeds that of the first acceptable design or until the volts per turn limit is reached. The program then calculates and prints a number of designs in the interval between the first acceptable design and the terminating design. Table F-2 is a copy of one printout, and Table F-3 is a copy of the program.

### Conclusions

The results of the previously described computer runs generate curves like those of Figures F-3, F-4, F-5, and F-6. The cutoff which determines the bottom "horizontal" line was the 200 millivolt per turn maximum. Figures F-7, F-8, F-9, and F-10 show the resulting "bottom line" for each core material. Smaller (lighter) transformers could be made with Orthonol and Silectron, for example, by using higher flux densities, but the 200 millivolt per turn limit forces high ASI, hence high copper loss. In general the volt per turn limit stops the designs to the left of the bottom of the convex curves shown in Figure F-2 which corresponds to higher copper loss than core loss. The minimum "bottom line"

FIGURE F-2 TRANSFORMER ANALYSIS PRINTOUT

TRANSFORMER ANALYSIS- WEIGHT, POWER, EFFICIENCY MATRIX  
RUN I.D.=HI WT ORTH & SUPPLY TOROIDS & SUPCIL C CORE

DO YOU WANT DETAILED PRINTOUT?=YES

PUT IN UP TO 6 WINDINGS, IN ORDER FROM CORE OUTWARD  
NUMBER OF WINDINGS, WHICH WINDING IS PRIMARY?= 3, 2

VOLTS, AMPS, KIND(2=CT) OF ALL WINDINGS  
= 6.4, 3.15, 2, 29.56, 0, 2, 32.64, 0.1, 1

PUT IN 4 FLUXES FOR EACH CORE TYPE, 0 MUST BE USED IF REAL FLUX NOT  
(1) ORTHANOL, (2) 48 ALLOY, (3) SUPERMALLOY, (4) C CORE  
FLUXES=2000, 1000, 0, 0, 0, 0, 0, 0, 2000, 1000, 500, 0, 1500, 1000, 500, 0,

FREQUENCIES NOT DESIRED(1, 2, 3, &/OR 4)=1, 2, 0, 4

MINIMUM CORE DIMENSION=.12

% WINDOW AREA USABLE FOR EACH MATERIAL= 70, 70, 70, 90

COPPER-STACKING FACTOR, RESISTIVITY(MICRO-OHM IN<sup>2</sup>/IN), WEIGHT(LBS/IN<sup>3</sup>),  
AND MAX CURRENT DENSITY(AMPS/IN<sup>2</sup>)= 0.6, 0.68, 0.32, 3000

SWITCH DATA- VSAT, RISE, & FALL TIME(MICRO SECONDS)= 0.25, 1, 1

WATTS/POUND FACTOR(0 FOR MATRIX), MAX VOLTS/TURN= 0, 0.2

\*\*\*\*\* 2 MIL ORTHONOL \*\*\*\*\*  
WINDOW AREA USED 70. %

GAUSS= 2000. FREQUENCY= 6000. CORE LOSS= 7.658 WATTS/LB  
FINAL D= 0.220 IN. D1= 0.174 IN. XD= 0.0231

WT	POW	EFF	CORWT	CUWT	CPOW	CUPOW	ASI	D	
0.122	1.334	0.946	0.044	0.078	0.335	0.765	2998.	0.174	0.187
0.131	1.256	0.949	0.047	0.084	0.360	0.665	2700.	0.178	0.196
0.140	1.227	0.950	0.050	0.090	0.385	0.607	2493.	0.182	0.205
0.150	1.203	0.951	0.054	0.096	0.413	0.554	2300.	0.187	0.215
0.161	1.149	0.953	0.058	0.103	0.443	0.475	2056.	0.191	0.225
0.173	1.138	0.954	0.062	0.111	0.474	0.430	1890.	0.196	0.236
0.185	1.133	0.954	0.066	0.119	0.509	0.388	1736.	0.200	0.247
0.198	1.133	0.954	0.071	0.127	0.545	0.351	1593.	0.205	0.259
0.213	1.137	0.954	0.076	0.136	0.584	0.315	1459.	0.210	0.271
0.228	1.148	0.953	0.082	0.146	0.626	0.283	1335.	0.215	0.284
0.244	1.134	0.954	0.088	0.157	0.671	0.233	1169.	0.220	0.297

TABLE F-2 (Continued)

\*\*\*\*\* 2 MIL SUPERMALLOY \*\*\*\*\*  
WINDOW AREA USED 70. %

GAUSS= 2000. FREQUENCY= 6000. CORE LOSS= 0.822 WATTS/LB  
FINAL D= 0.220 IN. D1= 0.174 IN. XD= 0.0231

WT	POW	EFF	CORWT	CUWT	CPOW	CUPOW	ASI	D	
0.125	1.037	0.958	0.046	0.078	0.038	0.765	2998.	0.174	0.187
0.134	0.938	0.962	0.050	0.084	0.041	0.665	2700.	0.178	0.196
0.143	0.886	0.964	0.053	0.090	0.044	0.607	2493.	0.182	0.205
0.154	0.838	0.965	0.057	0.096	0.047	0.554	2300.	0.187	0.215
0.165	0.757	0.969	0.061	0.103	0.050	0.475	2056.	0.191	0.225
0.176	0.718	0.970	0.066	0.111	0.054	0.430	1890.	0.196	0.236
0.189	0.682	0.972	0.070	0.119	0.058	0.388	1736.	0.200	0.247
0.203	0.650	0.973	0.076	0.127	0.062	0.351	1593.	0.205	0.259
0.217	0.619	0.974	0.081	0.136	0.067	0.315	1459.	0.210	0.271
0.233	0.593	0.975	0.087	0.146	0.071	0.283	1335.	0.215	0.284
0.250	0.539	0.977	0.093	0.157	0.076	0.233	1169.	0.220	0.297

GAUSS= 1000. FREQUENCY= 6000. CORE LOSS= 0.219 WATTS/LB  
FINAL D= 0.261 IN. D1= 0.207 IN. XD= 0.0231

WT	POW	EFF	CORWT	CUWT	CPOW	CUPOW	ASI	D	
0.210	1.535	0.939	0.078	0.131	0.017	1.285	2998.	0.207	0.132
0.225	1.404	0.943	0.084	0.141	0.018	1.152	2743.	0.212	0.139
0.241	1.283	0.948	0.090	0.151	0.020	1.029	2504.	0.217	0.145
0.258	1.172	0.952	0.096	0.162	0.021	0.916	2282.	0.222	0.152
0.276	1.069	0.956	0.103	0.173	0.023	0.812	2076.	0.227	0.159
0.296	0.974	0.960	0.110	0.186	0.024	0.718	1884.	0.232	0.167
0.318	0.925	0.962	0.118	0.199	0.026	0.662	1749.	0.238	0.175
0.340	0.843	0.965	0.127	0.214	0.028	0.580	1581.	0.243	0.183
0.365	0.767	0.968	0.136	0.229	0.030	0.505	1425.	0.249	0.191
0.391	0.729	0.970	0.146	0.245	0.032	0.462	1317.	0.255	0.200
0.419	0.666	0.972	0.156	0.263	0.034	0.399	1181.	0.261	0.210

GAUSS= 500. FREQUENCY= 6000. CORE LOSS= 0.058 WATTS/LB  
FINAL D= 0.360 IN. D1= 0.246 IN. XD= 0.0379

WT	POW	EFF	CORWT	CUWT	CPOW	CUPOW	ASI	D	
0.353	2.407	0.907	0.132	0.222	0.008	2.165	2997.	0.246	0.094
0.396	2.031	0.920	0.148	0.248	0.009	1.789	2574.	0.256	0.101
0.444	1.752	0.930	0.165	0.278	0.010	1.507	2232.	0.266	0.109
0.497	1.463	0.941	0.185	0.312	0.011	1.219	1896.	0.276	0.118
0.557	1.251	0.949	0.208	0.350	0.012	1.006	1627.	0.287	0.127
0.624	1.102	0.955	0.233	0.392	0.014	0.852	1415.	0.298	0.137
0.699	0.938	0.961	0.261	0.439	0.015	0.690	1203.	0.309	0.148
0.784	0.825	0.966	0.292	0.492	0.017	0.574	1036.	0.321	0.159
0.878	0.726	0.970	0.327	0.551	0.019	0.473	889.	0.334	0.172
0.984	0.639	0.973	0.367	0.617	0.021	0.386	758.	0.347	0.185
1.103	0.586	0.976	0.411	0.692	0.024	0.327	660.	0.360	0.200

TABLE F-2 (Continued)

\*\*\*\*\* 1 MIL SELECTRONIC C CORE \*\*\*\*\*  
WINDOW AREA USED 90. %

GAUSS= 1500. FREQUENCY= 5000. CORE LOSS= 3.480 WATTS/LB  
FINAL D= 0.291 IN. D1= 0.231 IN. XD= 0.0231

WT	POW	EFF	CORWT	CUWT	CPOW	CUPOW	ASI	D	
0.217	1.920	0.924	0.068	0.149	0.235	1.490	2986.	0.231	0.154
0.232	1.828	0.928	0.072	0.160	0.252	1.379	2776.	0.236	0.161
0.249	1.684	0.933	0.078	0.171	0.270	1.217	2518.	0.242	0.169
0.267	1.554	0.938	0.083	0.184	0.290	1.070	2281.	0.247	0.177
0.286	1.440	0.942	0.089	0.197	0.310	0.936	2059.	0.253	0.185
0.307	1.386	0.944	0.096	0.211	0.333	0.858	1905.	0.259	0.194
0.329	1.292	0.948	0.103	0.226	0.357	0.742	1711.	0.265	0.203
0.352	1.254	0.949	0.110	0.242	0.382	0.676	1578.	0.271	0.213
0.378	1.224	0.950	0.118	0.260	0.410	0.616	1456.	0.278	0.223
0.405	1.158	0.953	0.126	0.278	0.439	0.525	1297.	0.284	0.234
0.434	1.141	0.954	0.135	0.298	0.471	0.475	1192.	0.291	0.245

GAUSS= 1000. FREQUENCY= 5000. CORE LOSS= 1.585 WATTS/LB  
FINAL D= 0.323 IN. D1= 0.256 IN. XD= 0.0231

WT	POW	EFF	CORWT	CUWT	CPOW	CUPOW	ASI	D	
0.297	2.336	0.909	0.093	0.204	0.147	1.995	2951.	0.256	0.127
0.318	2.146	0.916	0.099	0.219	0.157	1.793	2703.	0.262	0.133
0.341	1.972	0.922	0.106	0.235	0.169	1.608	2473.	0.269	0.139
0.366	1.814	0.928	0.114	0.252	0.181	1.438	2259.	0.275	0.146
0.392	1.669	0.933	0.122	0.270	0.194	1.279	2058.	0.281	0.152
0.420	1.538	0.938	0.131	0.289	0.208	1.135	1872.	0.288	0.160
0.450	1.419	0.943	0.140	0.310	0.223	1.001	1699.	0.295	0.167
0.483	1.313	0.947	0.151	0.332	0.239	0.881	1538.	0.301	0.175
0.517	1.262	0.949	0.161	0.356	0.256	0.810	1426.	0.308	0.183
0.554	1.174	0.952	0.173	0.382	0.274	0.705	1284.	0.316	0.192
0.594	1.136	0.954	0.185	0.409	0.294	0.645	1187.	0.323	0.201

GAUSS= 500. FREQUENCY= 5000. CORE LOSS= 0.413 WATTS/LB  
FINAL D= 0.456 IN. D1= 0.304 IN. XD= 0.0403

WT	POW	EFF	CORWT	CUWT	CPOW	CUPOW	ASI	D	
0.497	3.644	0.865	0.155	0.342	0.064	3.386	2972.	0.304	0.089
0.561	3.074	0.884	0.175	0.386	0.072	2.807	2547.	0.317	0.097
0.633	2.577	0.901	0.198	0.436	0.082	2.300	2171.	0.330	0.105
0.715	2.151	0.916	0.223	0.492	0.092	1.864	1839.	0.344	0.114
0.807	1.842	0.927	0.252	0.555	0.104	1.542	1575.	0.358	0.123
0.911	1.575	0.937	0.284	0.627	0.117	1.262	1341.	0.372	0.134
1.028	1.347	0.946	0.321	0.707	0.132	1.019	1134.	0.388	0.145
1.160	1.195	0.951	0.362	0.798	0.149	0.849	975.	0.404	0.157
1.309	1.029	0.958	0.408	0.901	0.169	0.667	813.	0.420	0.170
1.478	0.958	0.961	0.461	1.017	0.190	0.570	708.	0.438	0.185
1.668	0.869	0.964	0.520	1.148	0.215	0.458	597.	0.456	0.200

TABLE F-3 TRANSFORMER ANALYSIS PROGRAM

```
00010 * TRANSFORMER ANALYSIS T.J.E. 2/2/70
00020 * STATEMENTS 8-30
00030 *
00040 * FORMATS 99-107,111-114
00050 DIMENSION XM(4,4),XK(4,4),FLUX(4,4),WF(4),AFOWK(5),AWT(5),AVE(4),
00060 &HZ(4),NFSKIP(4),CRO(4),V(6),A(6),N(6),KIND(6)
00070 ASCII ASC(10),DATE(2)
00080 PI=3.14159
00090 CALL DATE#TIM(DATE,HOUR) ; PRINT 99,DATE,HOUR
00100 PRINT:" TRANSFORMER ANALYSIS-WEIGHT,POWER,EFFICIENCY MATRIX"
00110 PRINT:" RUN I.D." ; READ:ASC(10)
00120 PRINT:" ";PRINT:" DO YOU WANT DETAILED PRINTOUT?" ; READ:ASC(1)
00130 PRINT:"PUT IN UP TO 6 WINDINGS,IN ORDER FROM CORE OUTWARD"
00140 PRINT:" NUMBER OF WINDINGS,WHICH WINDING IS PRIMARY?" ; READ:NW,NP
00150 PRINT:" VOLTS,AMPS,KIND(2=CT) OF ALL WINDINGS" ; PRINT:" "
00160 READ:(V(K),A(K),KIND(K),K=1,NW)
00170 PRINT:"PUT IN 4 FLUXES FOR EACH CORE TYPE,0 MUST BE USED IF
00180 & REAL FLUX NOT DESIRED"
00190 PRINT:" (1)ORIHANOL,(2)48 ALLOY,(3)SUPERMALLEY,(4) C CORE"
00200 PRINT:" FLUXES" ; READ:(FLUX(I,K),K=1,4),I=1,4)
00210 PRINT:" FREQUENCIES NOT DESIRED(1,2,3,&/OR 4)"; READ:(NFSKIP(I),I=1,4)
00220 PRINT:" MINIMUM CORE DIMENSION" ; READ:DB
00230 PRINT:" % WINDOW AREA USABLE FOR EACH MATERIAL"; READ:(WF(I),I=1,4)
00240 PRINT:" COPPER-STACKING FACTOR,RESISTIVITY(MICRO-OHM IN2/IN),
```

TABLE F-3 (Continued)

```

00250 &WEIGHT(LBS/IN3)," ; PRINT:" AND MAX CURRENT DENSITY(AMPS/IN2)"
00260 READ:SF, SIGMA, CURO, ASIMAX ; SIGMA=SIGMA*1.0E-6
00270 PRINT:" SWITCH DATA-VSAT,RISE,&FALL TIME(MICRO SECONDS)"
00280 READ:TR,TF ; TR=TR*1.0E-6 ; TF=TF*1.0E-6
00290 PRINT:" WATTS/POUND FACTOR(0 FOR MATRIX),MAX VOLTS/TURN"
00300 READ:PF,VPTMAX
00310 * SLOPES AND INTERCEPTS FOR CORE LOSSES
00320 XM(1,1)=1.32;XM(1,2)=1.23;XM(1,3)=1.11;XM(1,4)=1.03
00330 XK(1,1)=-.73;XK(1,2)=.03; XK(1,3)=.55 ; XK(1,4)=.875
00340 XM(2,1)=1.62;XM(2,2)=1.61;XM(2,3)=1.58;XM(2,4)=1.45
00350 XK(2,1)=-1.17;XK(2,2)=-.41;XK(2,3)=0.08;XK(2,4)=.53
00360 XM(3,1)=2.00;XM(3,2)=1.96;XM(3,3)=1.91;XM(3,4)=1.78
00370 * CORE DENSITIES(#/IN3)
00380 XK(3,1)=-1.76;XK(3,2)=-1.15;XK(3,3)=-.66;XK(3,4)=-.35
00390 XM(4,1)=1.80;XM(4,2)=1.77;XM(4,3)=1.94;XM(4,4)=2.00
00400 XK(4,1)=-.48;XK(4,2)=-.22;XK(4,3)=.20 ; XK(4,4)=.55
00410 CRD(1)=8.2*.03613*.89
00420 CRD(2)=8.2*.03613*.89
00430 CRD(3)=8.7*.03613*.89
00440 CRD(4)=.276*.83
00450 HZ(1)=1000 ; HZ(2)=3000 ; HZ(3)=6000 ; HZ(4)=10000
00460 POUT=0 ; DO 14 J=1,NW ; IF(J.EQ.NP) GO TO 14
00470 FOUT=POUT+A(J)*V(J) ; 14 CONTINUE
00480 NPRINT=11
00490 DO 15 I=1,4
00500 IF(I.EQ.4)HZ(2)=2000 ; IF(I.EQ.4)HZ(3)=5000
00510 IF(I.EQ.1)PRINT 111
00520 IF(I.EQ.2)PRINT 112 ; IF(I.EQ.3)PRINT 113 ; IF(I.EQ.4)PRINT 114

```

TABLE F-3 (Continued)

```
00530 PRINT 105,WF(1)
00540 CORRO=CRO(I)
00550 DO 17 M=1,4
00560 B=FLUX(I,M)
00570 IF(B.EQ.0)GO TO 17
00580 DO 16 K=1,4
00590 IF(K.EQ.NFSKIP(1))GO TO 16 ; IF(K.EQ.NFSKIP(2))GO TO 16
00600 IF(K.EQ.NFSKIP(3))GO TO 16 ; IF(K.EQ.NFSKIP(4))GO TO 16
00610 XLOGCL=XM(I,K)*( .43429*ALOG(B)-3.0)+XK(I,K)
00620 WPLB=EXP(2.30258*XLOGCL)
00630 FREQ=HZ(K)
00640 PRINT 104,B,FREQ,WPLB
00650 KIKWT=0 ; KIKPOW=0 ; IAVE=0 ; KIKPF=0
00660 TWT=0. ; TPOW=0. ; TWO=2.00
00670 D=D0 ; D1=0. ; DX=0
00680 9 CONTINUE
00690 D=SQRT(1.001*D*D)
00700 IF(DX.EQ.0)D=SQRT(D*D*(1.+.049/1.001))
00710 R1=2.0*D ; R0=3.0*D
00720 ACORE=D*2.*D*6.425 ; IF(I.EQ.4)ACORE=D*1.5*D*6.425
00730 CORVOL=10.*PI*D*D*D ; IF(I.EQ.4)CORVOL=24.*D*D*D
00740 CORWT=CORVOL*CORRO ; CORPOW=CORWT*WPLB
00750 VPT=(ACORE*B/1000.*FREQ/1000.)/25. ; N(NP)=V(NP)/VPT
00760 IF(VPT.GT.VPTMAX)KIKPOW=1
00770 A(NP)=0 ; CA=0
00780 IF(N(NP).LT.2)GO TO 12
00790 DO 8 J=1,NW
00800 IF(J.EQ.NP)GO TO 8
```

TABLE F-3 (Continued)

```

00810 XN=V(J)*N(NP)/V(NP) ; N(J)=XN
00820 IF((XN-IFIX(XN)).GT.0.5)N(J)=N(J)+1
00830 A(NP)=A(NP)+N(J)*A(J)/N(NP)
00840 IF(N(J).LT.2)GO TO 12
00850 8 CONTINUE
00860 AW=PI*K1*K1*SF*WF(1)/100.
00870 IF(I.EQ.4)AW=1.5*D*4.5*D*SF*WF(1)/100.
00880 DO 10 J=1,NW
00890 10 CA=CA+KIND(J)*N(J)*A(J)
00900 ASI=CA/AW
00910 1919 FORMAT(1H ,I8,F6.2,I8,E13.5,2F8.3,E13.5)
00920 ASI=CA/AW ; IF(ASI.GT.ASIMAX)GO TO 9 ; CUPOW=0
00930 IF(DX.NE.0)GO TO 22
00940 D=SQRT(D*D*.957) ; DX=D ; GO TO 9
00950 22 IF(D1.EQ.0)D1=.999999*D ; XL1=D
00960 XL1=D ; XLL1=1.5*D ; XLI1=2.*D ; XLO1=2.*D
00970 DO 11 J=1,NW
00980 CADEL=KIND(J)*N(J)*A(J)/ASI
00990 ADEL=CADEL/SF
01000 IF(I.EQ.4)GO TO 27
01010 R2=SQRT(R1*R1-ADEL/PI) ; R02=SQRT(R0*R0+ADEL/PI)
01020 XL2=XL1+R1-R2+R02-R0
01030 XLO2=XLO1+2.*(R02-R0) ; XLI2=XLI1+2.*(R1-R2)
01040 XMLT=(XLI1+XLI2+XLO1+XLO2)/2.+XL1+XL2
01050 XL1=XL2 ; XLI1=XLI2 ; XLO1=XLO2 ; R1=R2 ; R0=R02
01060 GO TO 28
01070 27 XL2=XL1+2.*ADEL/(4.5*D) ; XLL2=XLL1+2.*ADEL/(4.5*D)
01080 XMLT=XL1+XL2+XLL1+XLL2

```

TABLE F-3 (Continued)

```

01090 XL1=XL2 ; XLL1=XLL2
01100 28 CONTINUE
01110 CUPOW=CUPOW+SIGMA*XMLT*(ACJ)*N(J)**2./(CADEL/KIND(J))
01120 11 CONTINUE
01130 SLOPE=(XL12-XL02)/XL2
01140 CUVOL=PI*((XL12+R2*SLOPE)*(R02*R02-R2*R2)-2.*SLOPE/3.*(R0**3.-
01150 &R2**3.))-10.*PI*D*D*D
01160 IF(1.EQ.4) CUVOL=XL2*XLL2*4.5*D-6.75*D*D*D
01170 CUWI=CUVOL*SF*CUR0
01180 SLPOW=2./3.*2.*V(NP)*A(NP)*(TF+TR)*FREQ+VCESAT*A(NP)
01190 TWT=CORWT+CUWT ; TPOW=CORPOW+CUPOW+SLPOW
01200 IF(TWT.GT.90) GO TO 12
01210 IF(TWT0.EQ.0) TWT0=TWT ; IF(TWT.GT.1.E01*TWT0) KIKWT=1
01220 IF(TPOW0.EQ.0) TPOW0=TPOW ; IF(TPOW.GT.1.E01*TPOW0) KIKPOW=1
01230 IF(D.GT.100*D1) GO TO 12
01240 IF(PF.EQ.0) GO TO 25
01250 IAVE=IAVE+1 ; IF(IAVE.EQ.6) IAVE=1
01260 APOW(IAVE)=TPOW ; AWI(IAVE)=TWI
01270 IF(KIKPF.EQ.0) GO TO 23
01280 I1=IAVE+1
01290 XAVE=0
01300 DO 24 IAVE=1,4
01310 I1=I1-1 ; IF(I1.EQ.0) I1=5
01320 I2=I1-1 ; IF(I1.EQ.1) I2=5
01330 AVE(MAVE)=(APOW(I1)-APOW(I2))/(AWI(I2)-AWI(I1))
01340 24 XAVE=XAVE+AVE(MAVE)
01350 IF(XAVE/4..LT.PF) D=D*1.002001/1.004006
01360 IF(XAVE/4..LT.PF) D1=D

```

TABLE F-3 (Continued)

```

01370 23 IF(IAVE.EQ.4)KIKPF=1
01380 NPRINT=1
01390 IF(KIKPOW.EQ.1)D1=D
01400 IF(D1.EQ.D)GO TO 12
01410 GO TO 9
01420 25 CONTINUE
01430 IF(KIKPOW.EQ.0)GO TO 9
01440 IF(D.LT.1.26*D1)D=1.26*D1
01450 12 IF(D1.EQ.0)GO TO 13 ; XD=ALOG(D/D1)/10.
01460 IF(ASC(1).EQ."YES")PRINT 107 ,D,D1,XD
01470 IF(PF.NE.0)PRINT 106,XAVE/4.
01480 DO 13 JF=1,NPRINT
01490 IF(JF.GT.1)GO TO 26
01500 PRINT 102 ; IF(ASC(1).EQ."YES")PRINT 103
01510 26 D=EXP(ALOG(D1)+(JF-1)*XD)
01520 R1=2.*D ; R0=3.*D
01530 ACORE=D*2.*D*6.425 ; IF(1.EQ.4)ACORE=D*1.5*D*6.425
01540 CORVOL=10.*PI*D*D*D ; IF(1.EQ.4)CORVOL=24.*D*D*D
01550 CORWT=CORVOL*CORRO ; CORPOW=CORWT*WPLB
01560 VPT=(ACORE*B/1000.*FREQ/1000.)/25. ; N(NP)=V(NP)/VPI
01570 A(NP)=0 ; CA=0
01580 DO 18 J=1,NW
01590 IF(J.EQ.NP)GO TO 18
01600 XN=V(J)*N(NP)/V(NP) ; N(J)=XN
01610 IF((XN-IFIX(XN)).GT.0.5)N(J)=N(J)+1
01620 A(NP)=A(NP)+N(J)*A(J)/N(NP)
01630 IF(N(J).LT.1)PRINT:"N=",N(J)," JF=",JF
01640 IF(N(J).LT.1)N(J)=1

```

TABLE F-3 (Continued)

```

01650 18 CONTINUE
01660 AW=PI*R1*R1*SF*WF(1)/100.
01670 IF(1.EQ.4)AW=1.5*D*4.5*D*SF*WF(1)/100.
01680 DO 20 J=1,NW
01690 20 CA=CA+KIND(J)*N(J)*A(J)
01700 ASI=CA/AW ; CUPOW=0
01710 XL1=D ; XLL1=1.5*D ; XLI1=2.*D ; XLO1=2.*D
01720 DO 21 J=1,NW
01730 CADEL=KIND(J)*N(J)*A(J)/ASI
01740 ADEL=CADEL/SF ; IF(1.EQ.4)GO TO 29
01750 R2=SQRT(R1*R1-ADEL/PI) ; R02=SQRT(R0*R0+ADEL/PI)
01760 XL2=XL1+R1-R2+R02-R0
01770 XLI2=XLI1+2.*(R1-R2) ; XLO2=XLO1+2.*(R02-R0)
01780 XMLT=(XLI1+XLI2+XLO1+XLO2)/2.+XL1+XL2
01790 XL1=XL2 ; XLI1=XLI2 ; XLO1=XLO2 ; R1=R2 ; R0=R02
01800 GO TO 30
01810 29 XL2=XL1+2.*ADEL/(4.5*D) ; XLL2=XLL1+2.*ADEL/(4.5*D)
01820 XMLT=XL1+XL2+XLL1+XLL2
01830 XL1=XL2 ; XLL1=XLL2
01840 30 CONTINUE
01850 CUPOW=CUPOW+SIGMA*(XMLT*(A(J)*N(J))**2./(CADEL/KIND(J)))
01860 21 CONTINUE
01870 SLOPE=(XLI2-XLO2)/XL2
01880 CUVOL=PI*((XLI2+R2*SLOPE)*(R02*R02-R2*R2)-2.*SLOPE/3.*(R02**3.-
01890 &R2**3.))-10.*PI*D*D*D
01900 IF(1.EQ.4)CUVOL=XL2*XLL2*4.5*D-6.75*D*D*D
01910 CUWT=CUVOL*SF*CUR0

```

TABLE F-3 (Continued)

```
01920 SLPOW=2./3.*2.*V(NP)*A(NP)*(TR+TF)*FREQ+VCESAT*A(NP)
01930 TWT=CORWT+CUWT ; TPOW=CORPOW+CUPOW+SLPOW
01940 EFF=POUT/(POUT+TPOW)
01950 PRINT 100,TWT,TPOW,EFF ; IF(CASC(1).EQ."YES")PRINT 101,CORWT,CUWT,
01960 &CORPOW,CUPOW,ASI,D,VPT
01970 13 CONTINUE
01980 16 CONTINUE
01990 17 CONTINUE
02000 15 CONTINUE
02010 CALL DATE#TIM(DATE,HOUR) ; PRINT 99,DATE,HOUR
02020 99 FORMAT(1H0,2A4,F7.3)
02030 100 FORMAT(1H ,3F6.3)
02040 101 FORMAT(1H&,4F6.3,F7.0,2F8.3)
02050 102 FORMAT(1H0," WT POW EFF")
02060 103 FORMAT(1H&," CORWT CUWT CPOW CUPOW ASI D")
02070 104 FORMAT(1H-,"GAUSS=",F8.0," FREQUENCY=",F8.0," CORE LOSS=
",
02080 &F7.3," WATTS/LB")
02090 105 FORMAT(1H , " WINDOW AREA USED",F5.0," %")
02100 106 FORMAT(1H , " D WATTS/D POUNDS AVE=",F7.3," WATTS/POUND")
02110 107 FORMAT(1H , " FINAL D=",F7.3," IN. D1=",F7.3," IN.
02120 & XD=",F7.4)
02130 111 FORMAT(1H-,/,1H-,20(1H*)," 2 MIL ORTHONOL ",20(1H*))
02140 112 FORMAT(1H-,/,1H-,20(1H*)," 2 MIL 48 ALLOY ",20(1H*))
02150 113 FORMAT(1H-,/,1H-,20(1H*)," 2 MIL SUPERMALLOY ",17(1H*))
02160 114 FORMAT(1H-,/,1H-,20(1H*)," 1 MIL SELECTRONIC C CORE ",10(1H*))
02170 STOP
02180 END
```

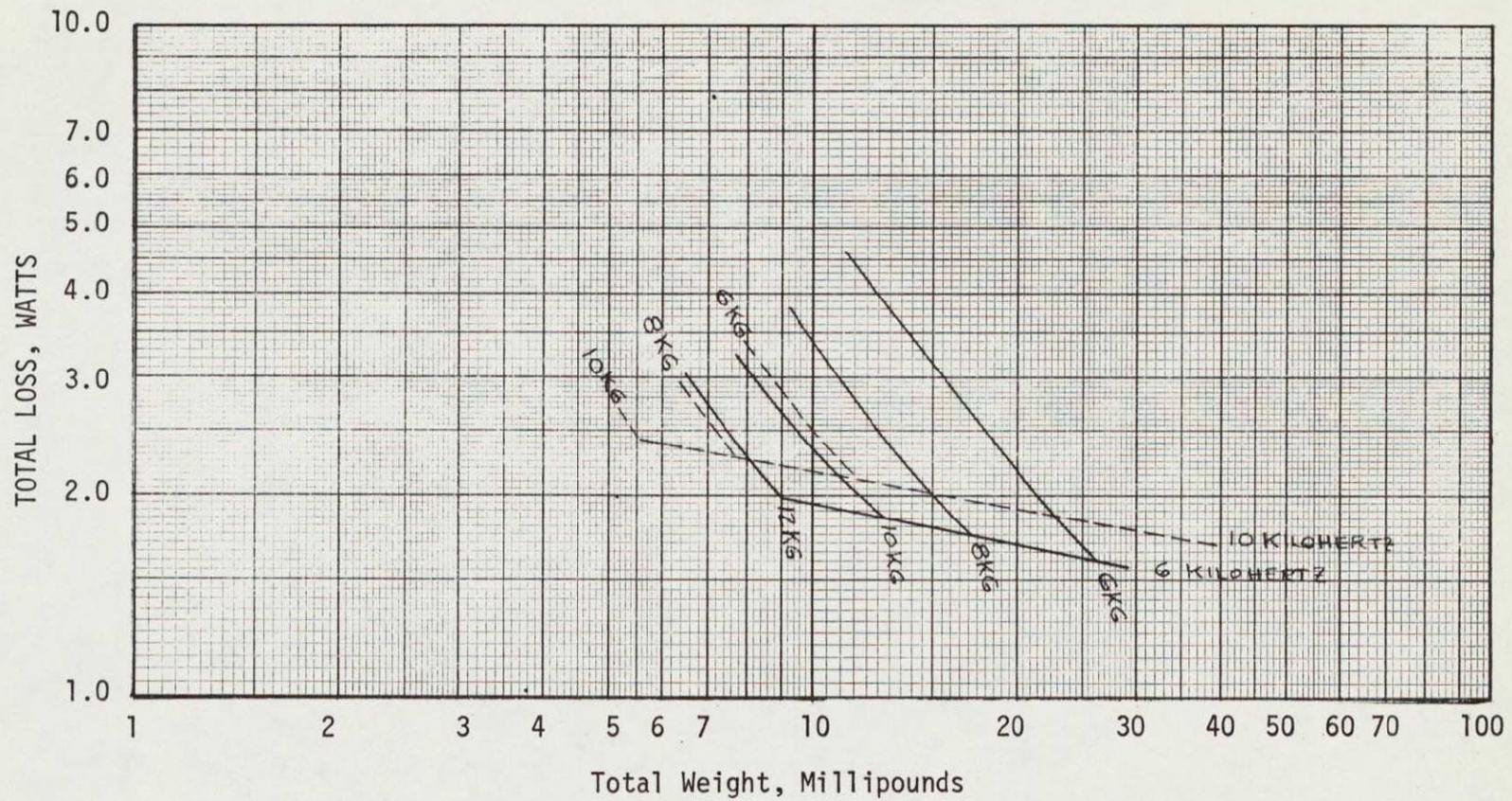


FIGURE F-3 CHARACTERISTICS OF ORTHONOL TOROIDAL TRANSFORMERS

200 MILLIVOLTS PER TURN MAXIMUM

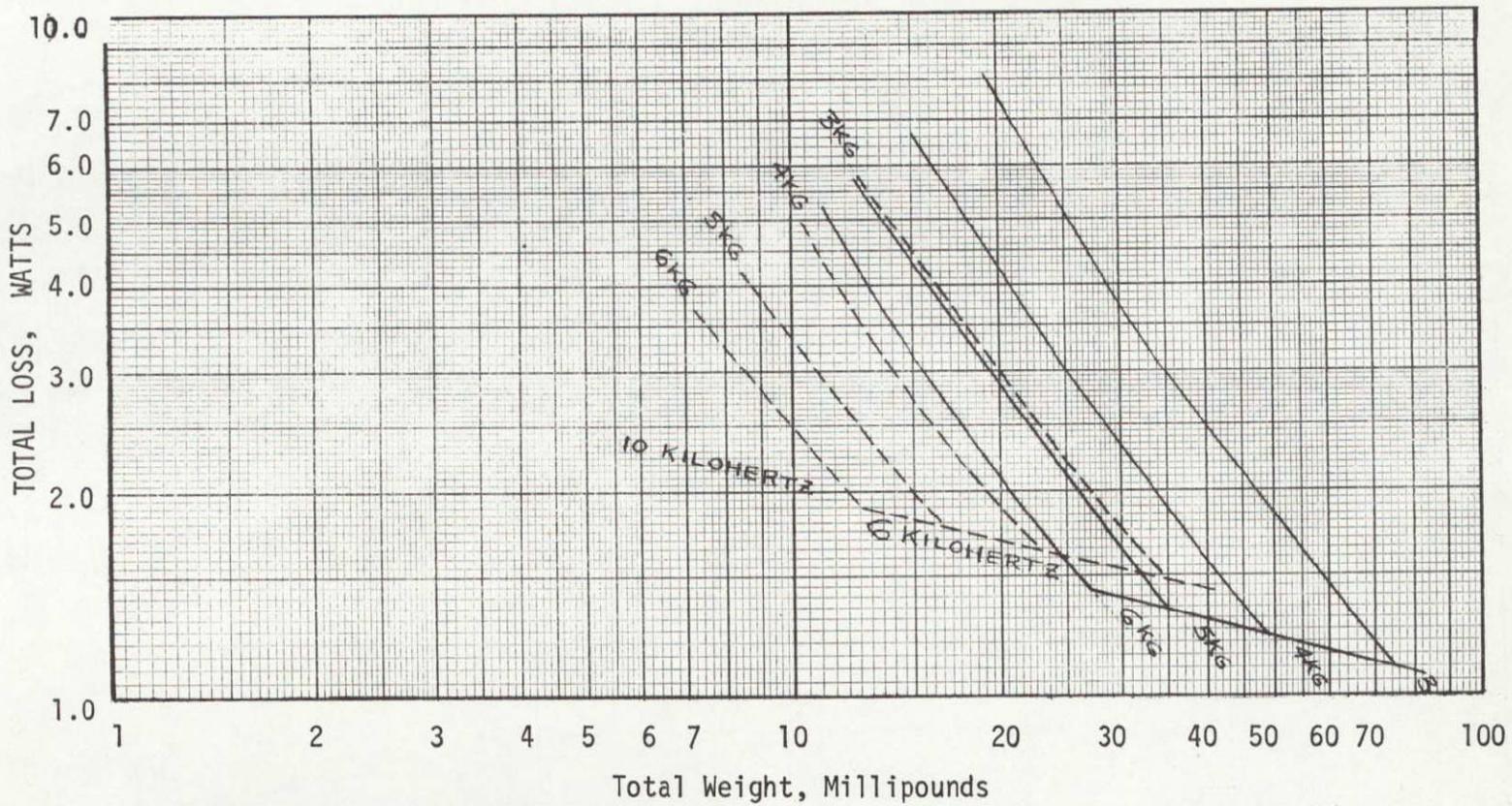


FIGURE F-4 CHARACTERISTICS OF SUPERMALLOY TOROIDAL TRANSFORMERS  
200 MILLIVOLTS PER TURN MAXIMUM

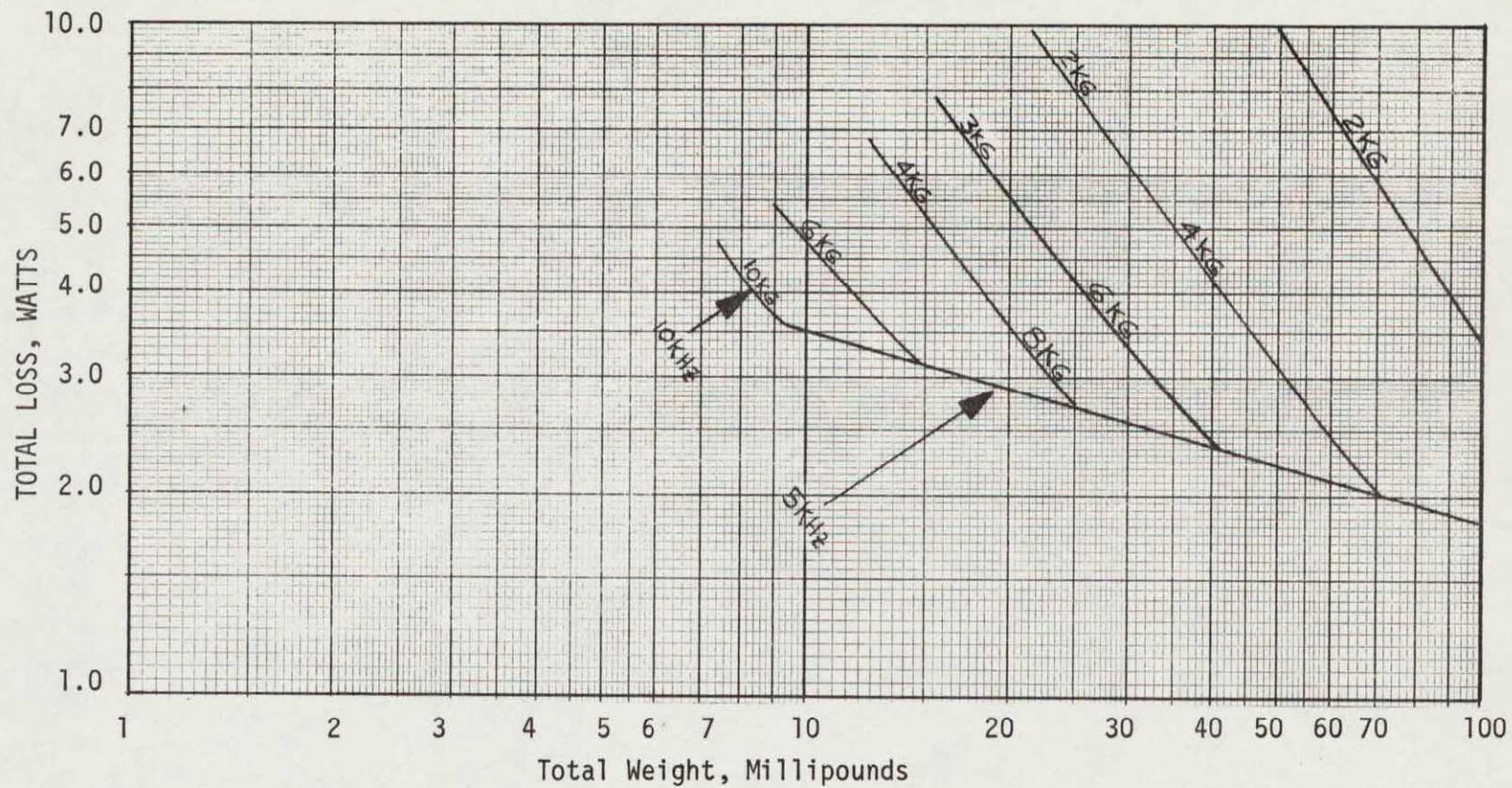


FIGURE F-5 CHARACTERISTICS OF SILECTRON CUT CORE TRANSFORMERS  
200 MILLIVOLTS PER TURN MAXIMUM

1J86-TOPS-555  
1 August 1970

F-19

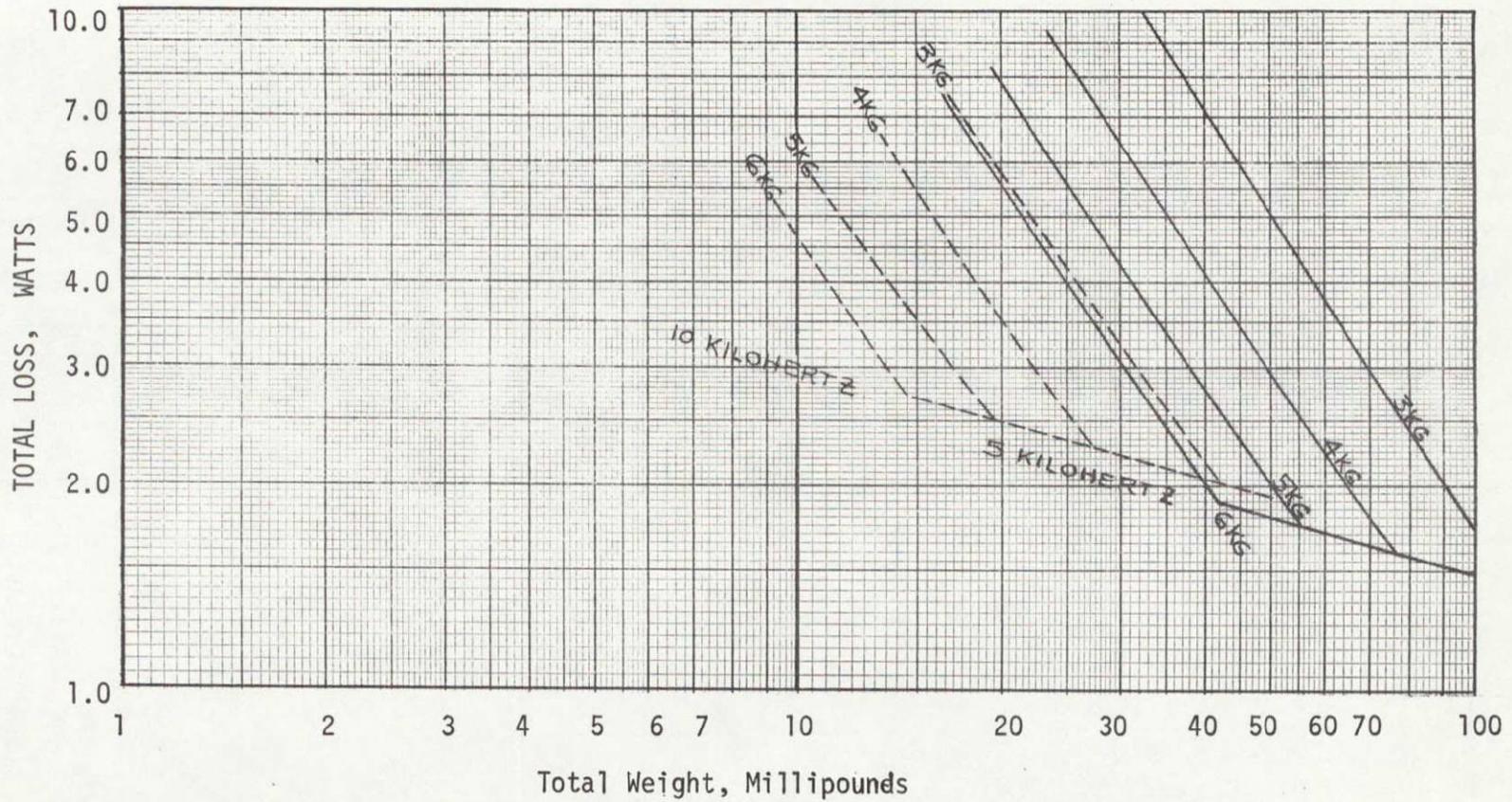


FIGURE F-6 CHARACTERISTICS OF SUPERMALLOY CUT CORE TRANSFORMERS  
200 MILLIVOLTS PER TURN MAXIMUM

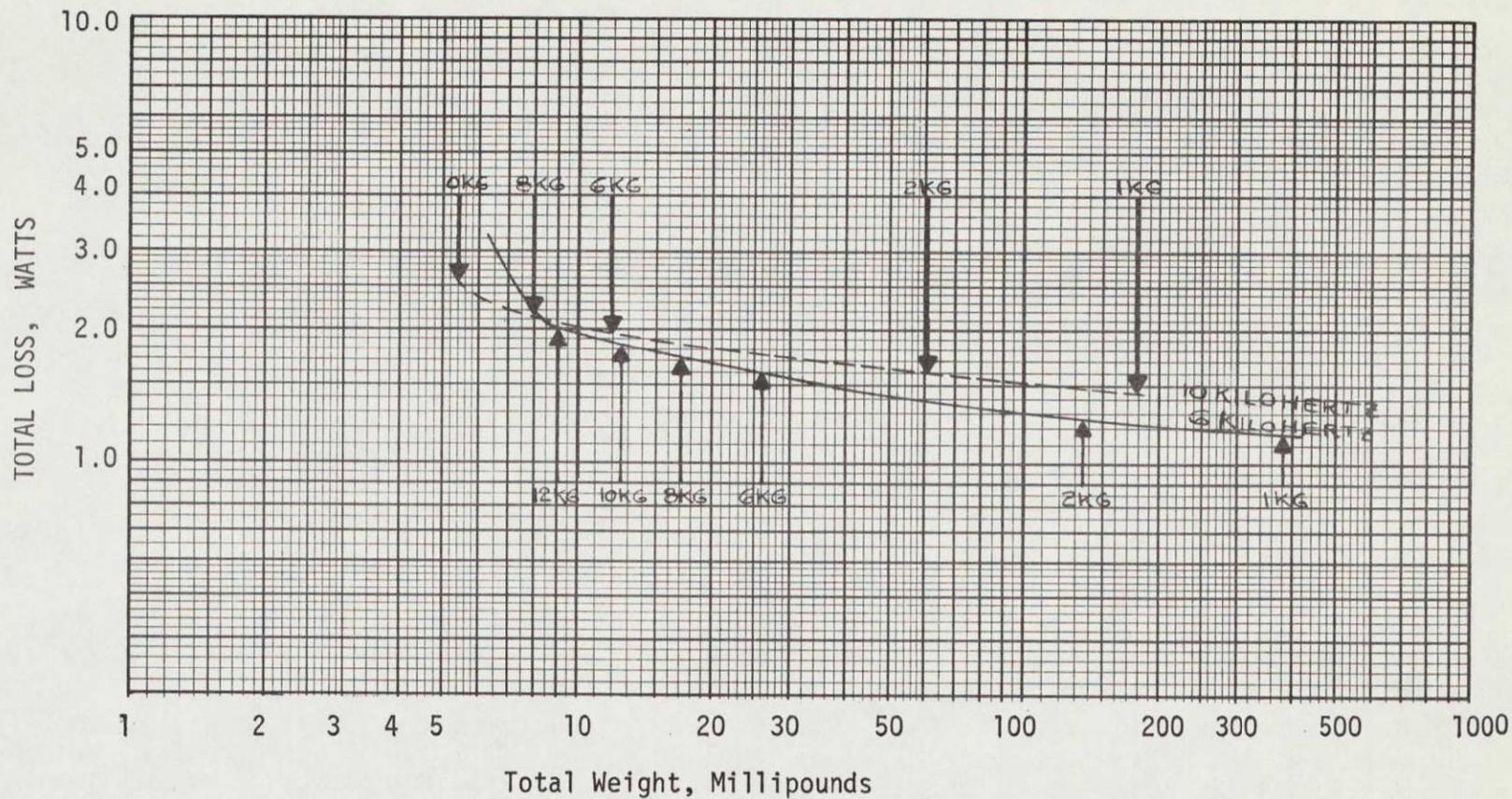


FIGURE F-7 LOCUS OF ORTHONOL TOROIDAL TRANSFORMERS  
200 MILLIVOLTS PER TURN MAXIMUM

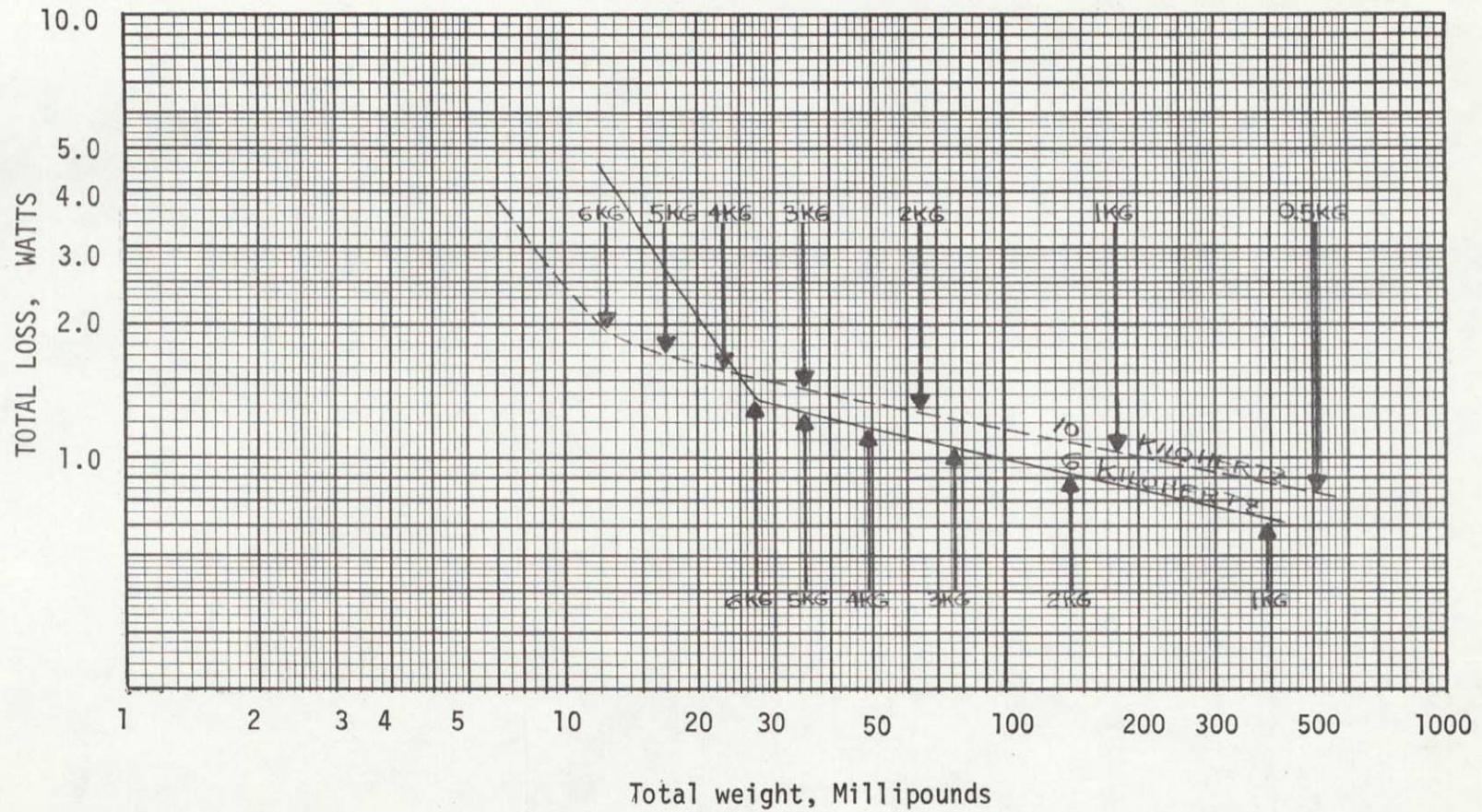


FIGURE F-8

LOCUS OF SUPERMALLOY TOROIDAL TRANSFORMERS  
200 MILLIVOLTS PER TURN MAXIMUM

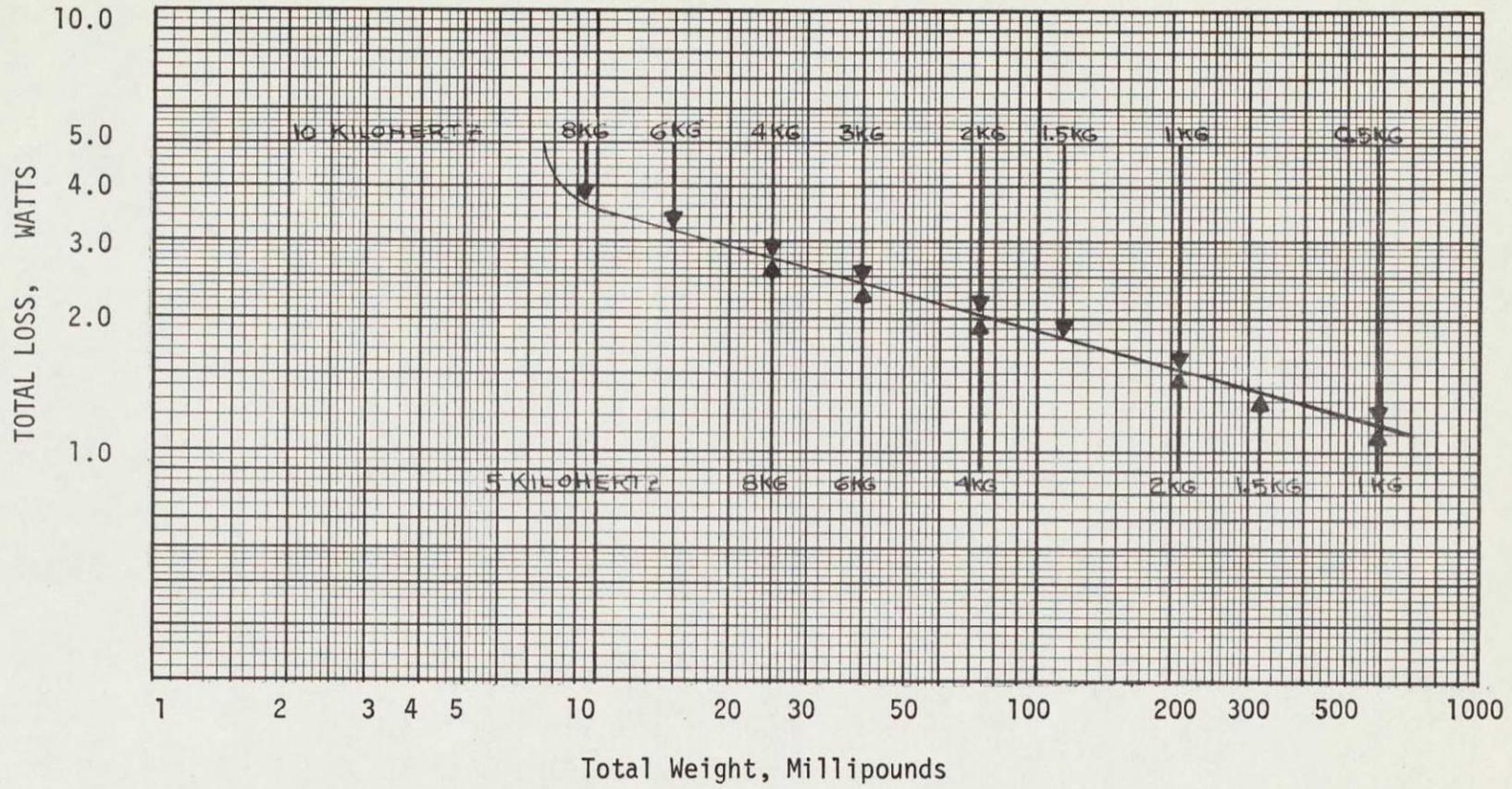


FIGURE F-9 LOCUS OF SILECTRON CUT CORE TRANSFORMERS  
200 MILLIVOLTS PER TURN MAXIMUM

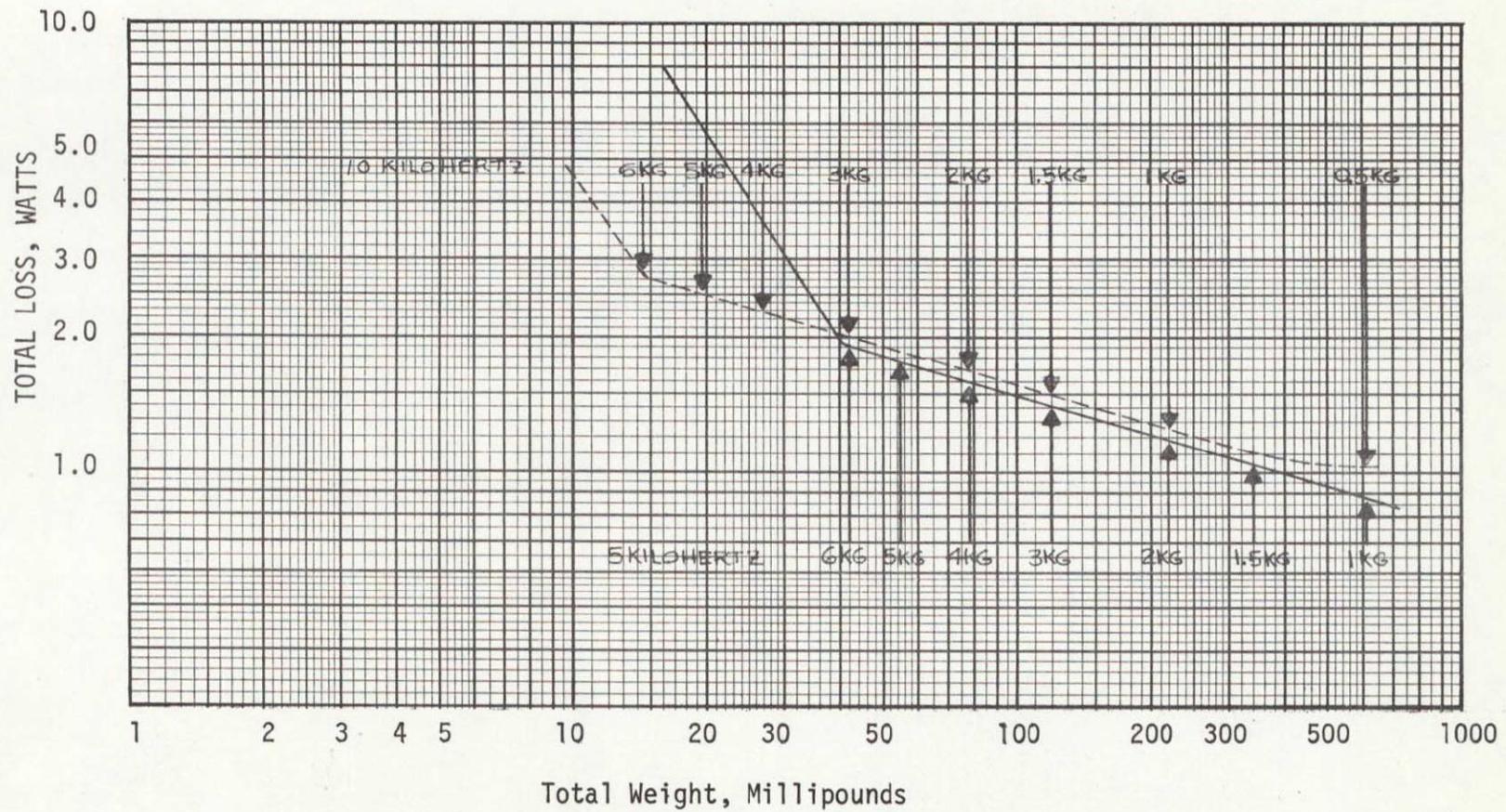


FIGURE F-10

LOCUS OF SUPERMALLOY CUT CORE TRANSFORMERS

200 MILLIVOLTS PER TURN MAXIMUM

for the different materials are shown together in Figure F-11. The approximate 1.7 watt per pound point was determined by calculating the slope for small lengths of the curve. Since the axes are logarithmic, the linear slope changes rapidly along the curve so the area indicated is approximately the location of the 1.7 watt per pound slope.

The "best" 1.7 watt per pound point is the supermalloy toroid. It must be noted, however, that power loss due to saturation spikes is not included and the difference in power loss between the toroid and C core is less than 1.4% of the transformer output power. The power loss difference for a C core at the same weight of the 1.7 watt per pound point of the toroid is less than 2.5% of the output power. It is also impossible to say whether the physical constraints selected are near optimum. It is also impossible to get cores in such incremental sizes as computed.

The general conclusion, then, is to use supermalloy at 8 KHz since the higher frequency and supermalloy were both better in the vicinity of the 1.7 watt per pound points.

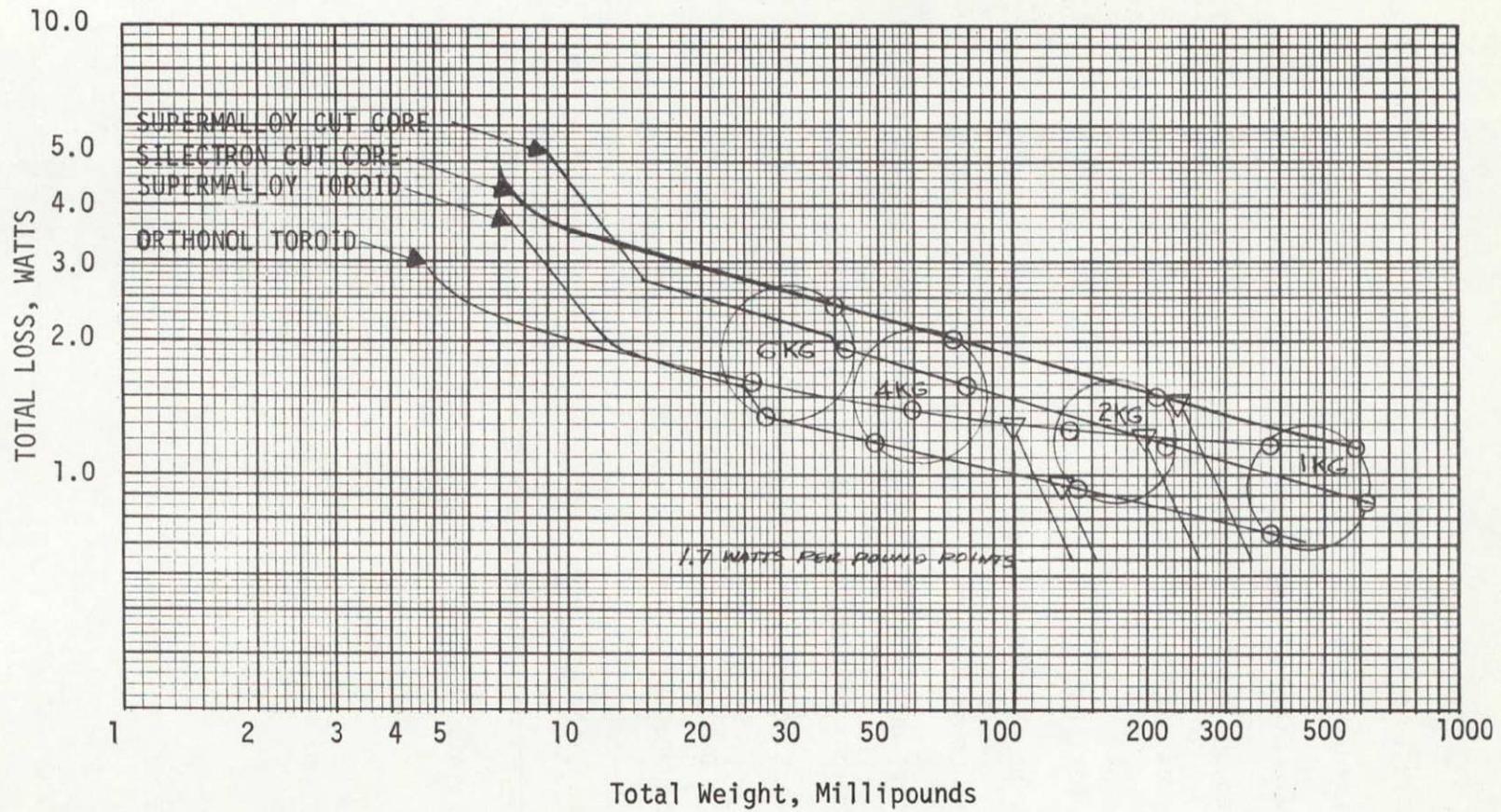


FIGURE F-11 COMPOSITE OF OPTIMIZED 18 WATT TRANSFORMERS  
200 MILLIVOLTS PER TURN MAXIMUM

## APPENDIX G OPERATIONAL PROCEDURES

Subsystem testing is performed at that phase of program development where all portions of the Power Conditioning Equipment have been assembled, and all external electrical interfaces are simulated by test equipment

System testing is performed after all the flight hardware has been assembled and interconnected in the spacecraft. At this time all simulated interfaces have been replaced with the prime equipment where practical

To perform subsystem/system testing, the following functions must be performed by the operational support equipment. This analysis includes complexity introduced by incorporation of a launch battery

### Supply Ground Power

The RTG's and the Launch Battery will be simulated by separate, independently adjustable power supplies whose V-I characteristics will be identical to the device being simulated (either the RTG's or the battery). Five supplies will be required

The interfacing of these power supplies to the PCE will vary as a function of the level of test being performed and is discussed in the respective test sections

### Supply Simulated Loads

Variable loads are required in order to dynamically operate and test the PCE. The implementation of loading depends on the level of test and is

covered in the respective test sections. The size of the total load will provide a simulated fault condition to activate the low voltage cut-off section of the PCE. The load simulator will determine the status of the power distribution switches of the PCE.

#### Record and Display Subsystem Performance

Internal circuitry will provide performance data via a telemetry link during flight. These same sensors with additional external measurements will provide the necessary information to verify subsystem/system level operation during ground testing. Presently identified internal measurements are

- voltage, current and temperature of each RTG
- current through each shunt regulator
- current through the auxiliary load
- launch battery current
- voltage of the main bus
- voltage of the protected bus
- voltage of the launch battery

External measurements are required to

- determine proper operation of the power distribution switches
- determine response time and output of the low voltage cut-off circuitry
- determine the magnitude of the applied load to the PCE.

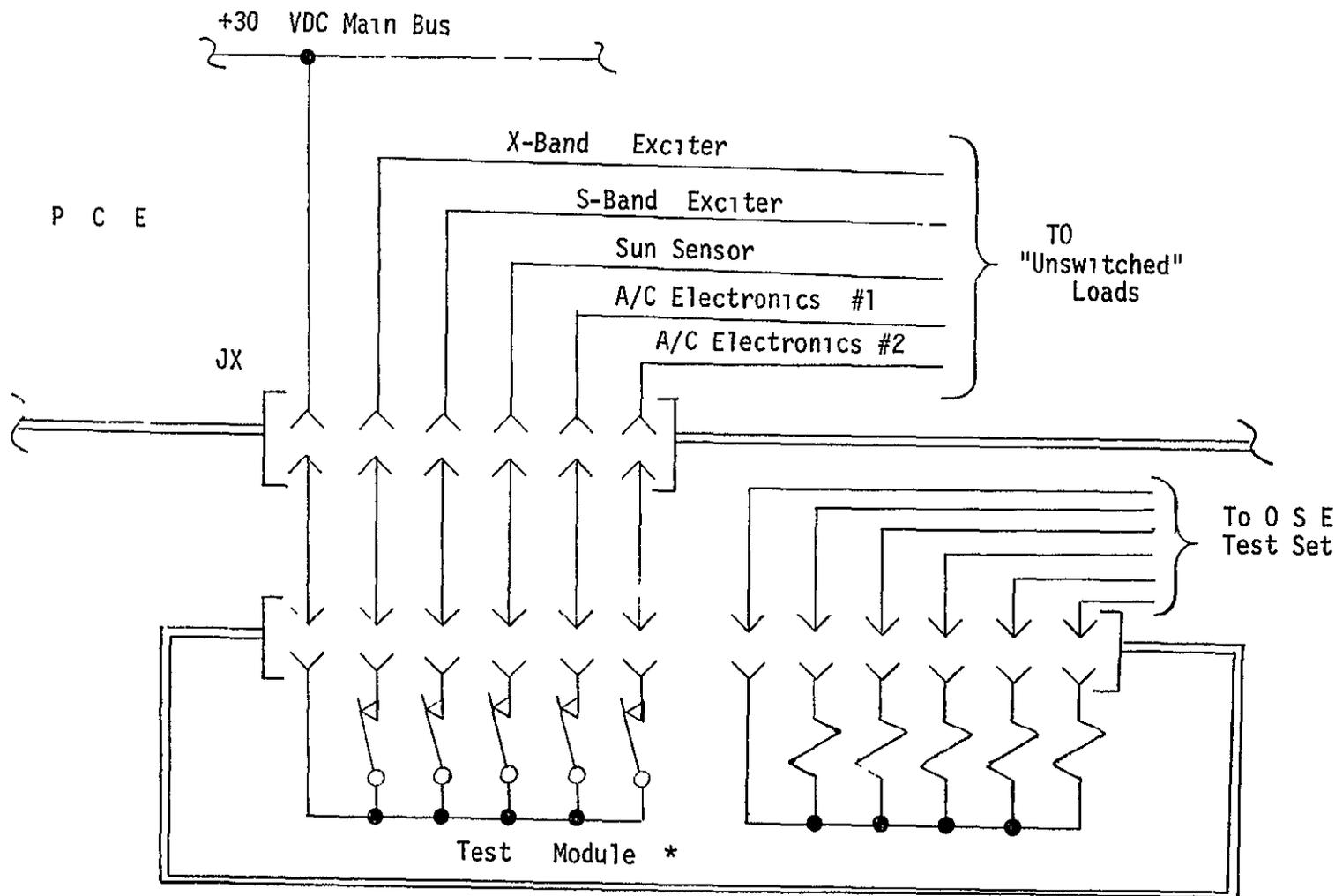
The internal sensors will be wired both to the telemetry interface and to a test connector on the PCE. This test connector will allow monitoring of internal conditions without requiring the telemetry system to be energized and operating.

This data will be transmitted to the PCE test set where it will be displayed for the test operator. At the same time, it will be recorded, compared with stored allowable limits, and an out of tolerance condition will be identified to the test conductor.

#### Switch "Hard Wired" Loads

As of this writing, some of the vehicle loads cannot be removed from the power bus. This is an unacceptable restriction during system test as a fault in one of these loads would require shut-down of the entire system. The OSE will provide switching for these loads as shown in Figure G-1. The main power bus is wired out of the PCE through a separate test connector into an adjacent test module. Normally closed switches in the test module will distribute the main power bus back into the PCE and then to the loads. Control of the switches is performed by the OSE. After system test and prior to fairing installation, the test module and its harness will be removed. A flight plug will be attached to the PCE test connector which will hard wire the main power bus to these loads. (Figure G-2)

G-4



\* Test module and cable will be removed prior to installation of fairing and transportation to launch pad

FIGURE G-1

PCE TEST MODULE INTERFACE

1386-TOPS-555  
1 August 1970

G-5

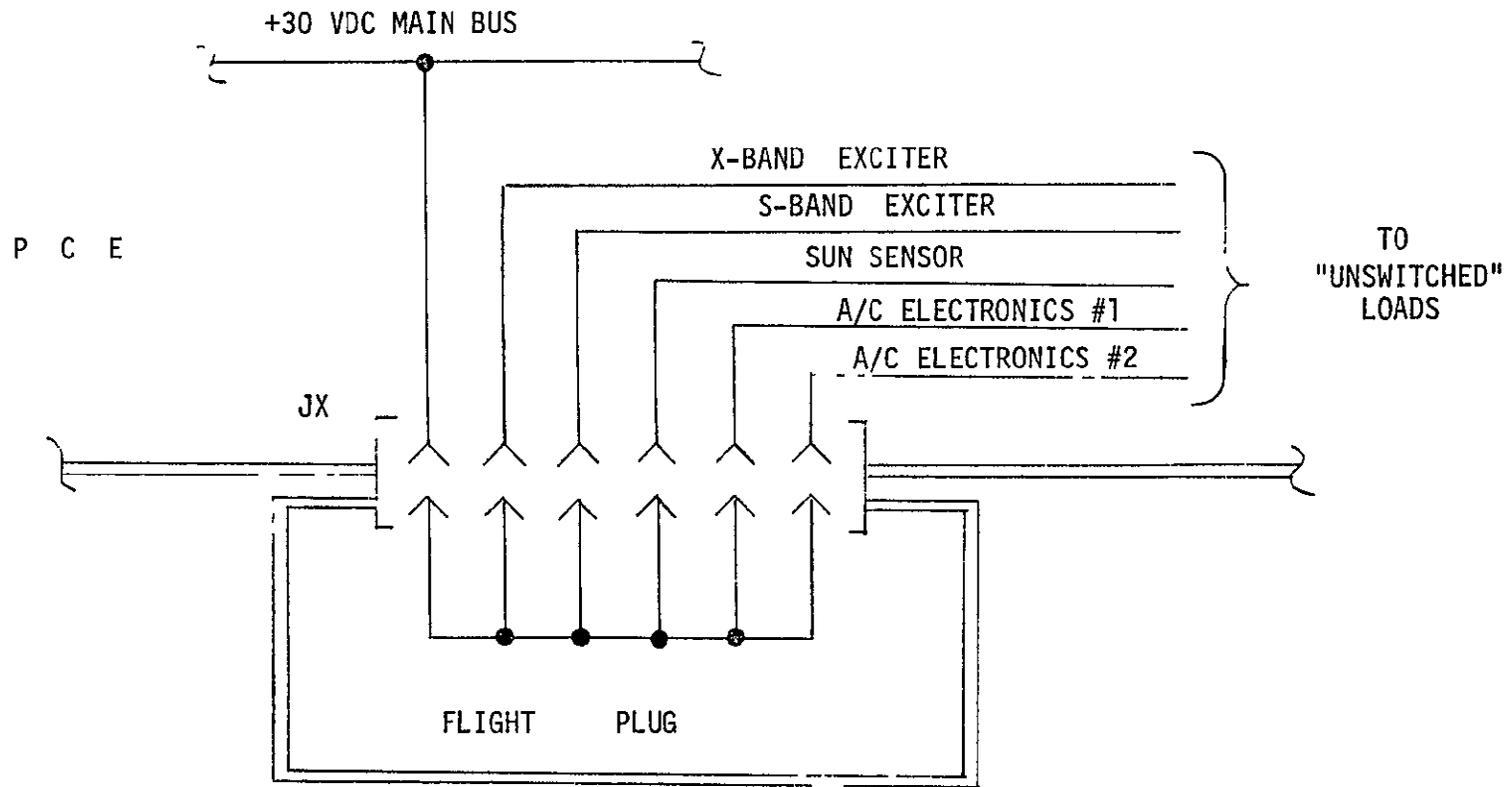


FIGURE G-2 PCE FLIGHT PLUG INTERFACE

1J86-TOPS-555  
1 August 1970

### Simulate Commands

During subsystem test, the CCS and FCS signals to the switching demodulators in the PCE must be simulated by the test equipment. These simulated commands will exercise the power switches through a normal mission sequence as well as an emergency shut-down sequence.

### Control RTG Isolation and Launch Battery Switches

To prevent oxidation of certain parts of the RTG's, they are to be cooled to a point where the output power at 30 VDC is zero. This limitation requires that ground power be supplied during the launch pad cycle, both before and after connection of the RTG's into the power subsystem.

As the output impedance of the RTG is very low, it must be open circuited so as to not load down the ground power unit (GPU). A motor driven switch controlled through the umbilical will provide this isolation.

A separate contact will be provided to open circuit each RTG, and a fifth switch will provide position information through the umbilical to the OSE.

A launch battery switch in the PCE performs two functions. One position connects the battery to the TOPS system. The other position removes the battery from the line and provides a path through the umbilical to the OSE battery charger.

Subsystem Test Equipment Configuration

The OSE GPU is cabled to the primary power input connectors J1 and J2 and to test connector J3. The path through J1 and J2 will be used to supply power during subsystem test. The input power path via J3 will be tested to verify its integrity and ability to carry vehicle current required on the launch pad. (Cable 6 on Figure G-3)

To test these two power paths, the output of the GPU will be switched. Control of this switching as well as current adjustments will be performed by the OSE Test Set thru Cable 7.

The OSE test module is connected to flight plug JX and controlled by the OSE test set thru cable 1.

A load simulator connected to the output power connectors (J8 through J12) will be controlled by the test set. The loads will be sized to correspond to actual flight loads with selectable capability to provide an overload condition. Total load current will be measured and transmitted to the test set thru cable 9.

The OSE interface simulator controlled by the test set thru Cable 8 supplies commands and measures telemetry information via cables 3 and 4. Simulation of the RTG temperature sensors is provided to the PCE to verify operation of the signal conditioners within the PCE thru Cable 5.

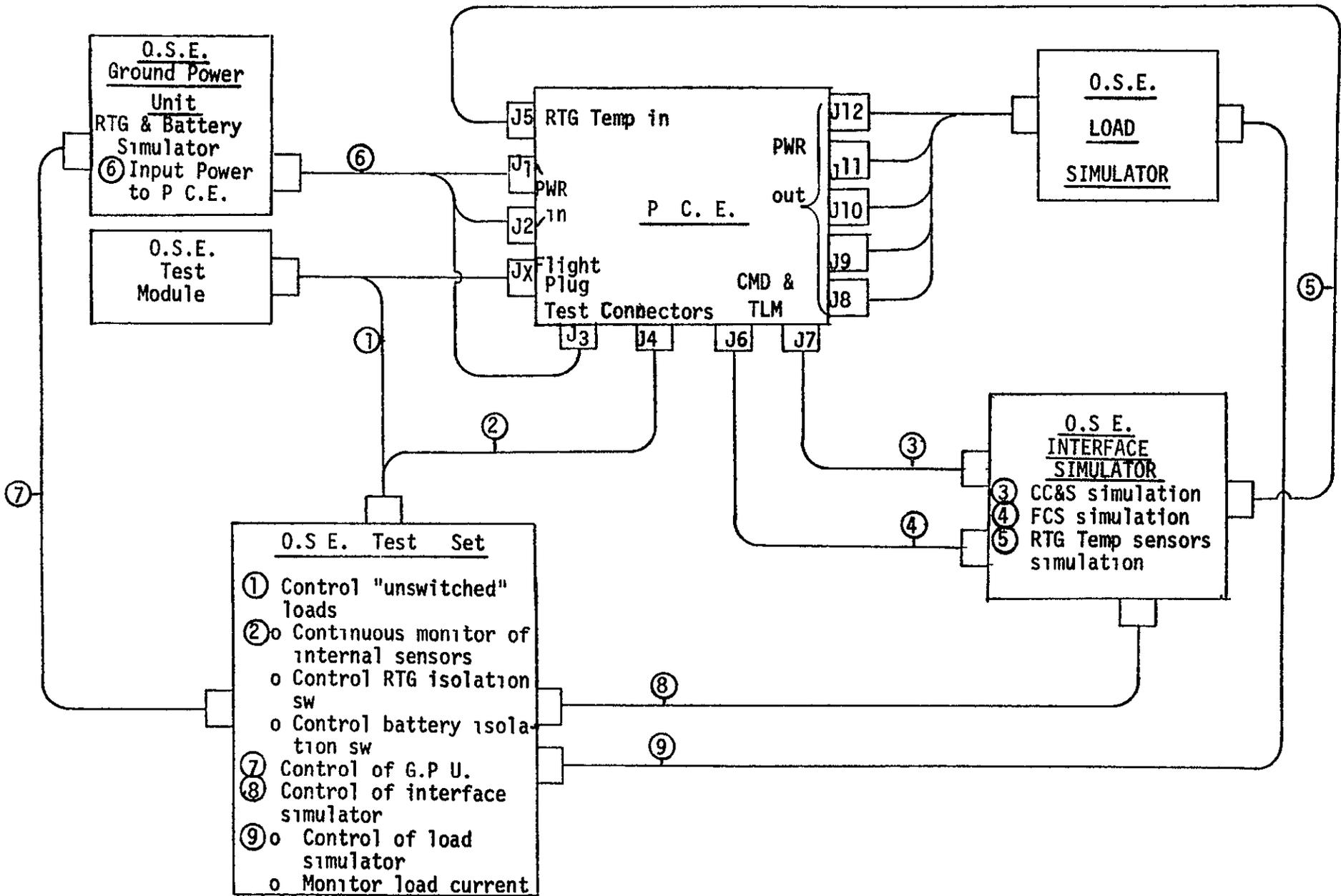


FIGURE G-3

SUBSYSTEM TEST EQUIPMENT CONFIGURATION

The connection between J4 and the test set, Cable 2, will provide continuous monitor of the PCE internal sensors. The RTG isolation switch and the battery isolation switch will be exercised through this cable.

### Subsystem Test Operation

#### Individual Shunt Regulator

The shunt regulators will be tested in two phases. The first test will verify operability of each regulator, and the second will test all four regulators in conjunction with the auxiliary load controller.

As each shunt regulator controls the output of only one RTG, it can be tested in the following manner:

The ground power unit will supply power to one input bus only through the prime input connector. The three other buses will remain off. The GPU will be limited so as not to exceed the power dissipation of the single shunt regulator. This restriction simplifies the test as it allows operation without sensing and sequencing external loads.

The RTG isolation switch is closed by the OSE test set and the GPU is ramped on. The input voltage and current monitors, the shunt current monitor, the main bus voltage monitor, and the protected bus voltage monitor will be compared to determine voltage regulation and shunt power dissipation. Shunt regulator response over the range of 0 to 40 watts will be recorded. At the end of this test, the GPU input power will be

transferred to the next input bus, and the same procedure repeated until all four shunt regulators have been tested

The shunt regulators must now be tested in conjunction with the Auxiliary Load Controller to determine voltage regulation over the full dynamic range of the RTG's, using the arrangement of Figure G-4

Power from all four of the RTG simulators in the GPU will be supplied through the prime input connectors. The OSE load simulator will not be used at this point since all the RTG power is used by the shunt/auxiliary load controller. Slowly ramping on the GPU from 0 to 600 watts will assure that the detection and switching circuits of the auxiliary load controller are operative. After completion, the GPU is turned off.

In order to determine the transient effect on the main bus due to load switching, a load of approximately 300 watts will be applied to the output by the OSE load simulator. The GPU will be turned on to a full load of 600 watts.

The sum of the current monitor in the load simulator and the shunt regulator-auxiliary load controller current monitors should equal the RTG input current. The voltage monitors on the main and protected bus will be observed and recorded continuously. A 120 watt load will be removed in the load simulator and the effect observed on the voltage monitors and shunt currents. The load will be re-applied and the results observed and recorded.



Next, the effect of sequencing loads on and off will be determined. Incremental loads of 100 watts each at a rate to be determined will be sequenced by the load simulator. Stepping up to full load and down to minimum load while observing main and protected bus voltages will verify the response time of the shunt regulator - auxiliary load controller required to maintain regulation.

#### Current Throttle

Two of the four RTG's are connected to the main bus via current throttles. Should a fault occur on the main bus which would cause the bus voltage to drop, these throttles will limit the current from their RTG's. This would allow these RTG's to satisfy the demands of the CCS on the "protected bus" as shown on Figure G-5.

To test these devices, a fault is simulated on the main bus to pull down the voltage.

The Ground Power Unit will supply RTG #1 bus and will be current limited to 5 amps (monitored by the PCE input current monitor). The OSE load simulator will supply a load of  $6\Omega$  (150w) that can be increased to a short circuit to reduce the main bus voltage to zero. This loading must be applied to output busses that are not switched by the low voltage cut off circuit since the LVCO will trigger below +27VDC and remove a portion of the simulated load. A test load path is provided on the test connector J3 and may be used for this operation. Proper operation of the current

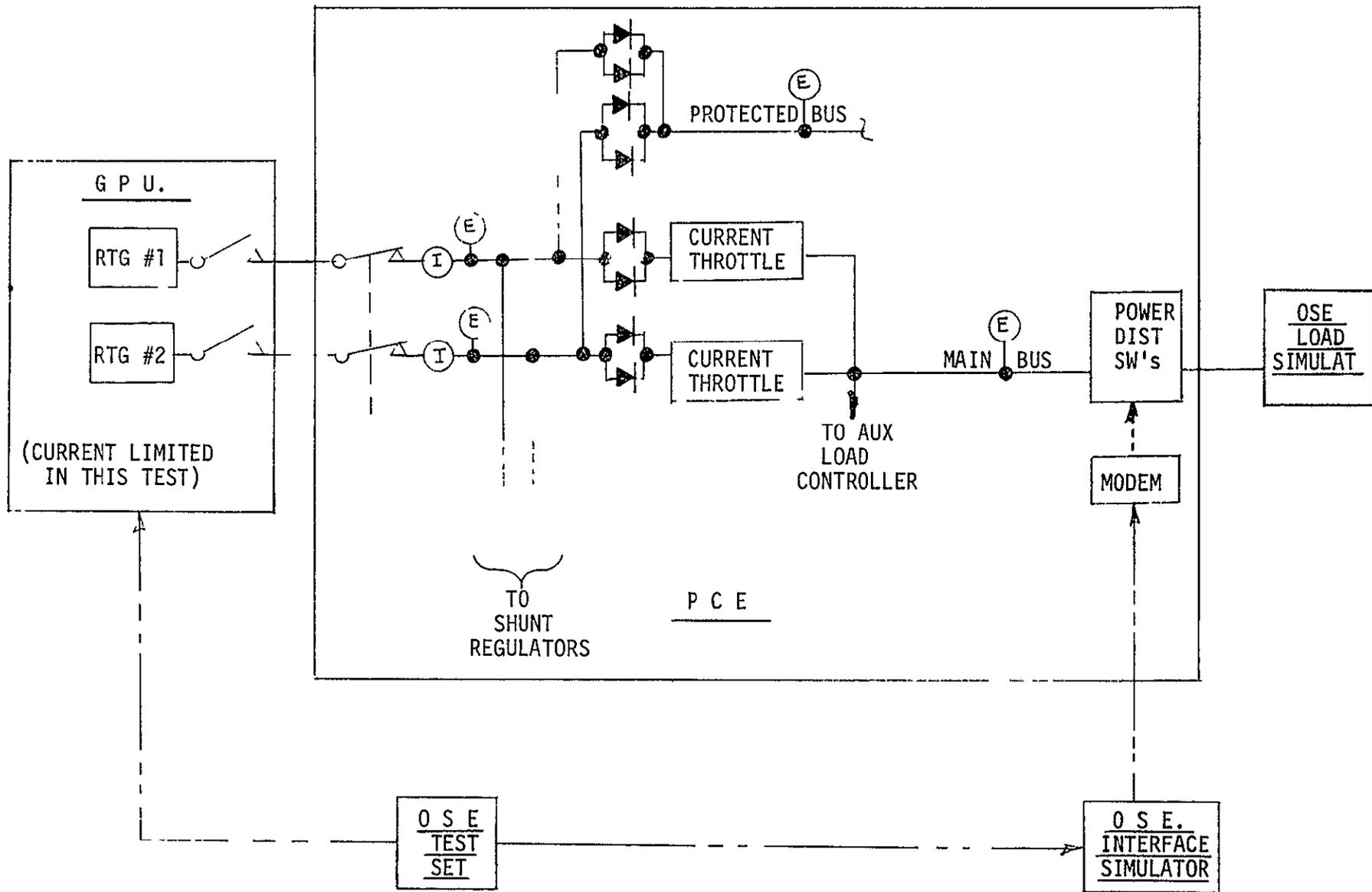


FIGURE G-5 CURRENT THROTTLE TEST

throttle can be determined by monitoring the voltages before and after the current throttle and the voltage of the protected bus. When operating within specification, the input voltage to the current throttle will be maintained at 30 volts minimum, and the protected bus maintained at this same level. The same procedure will be repeated for the current throttle of RTG #2.

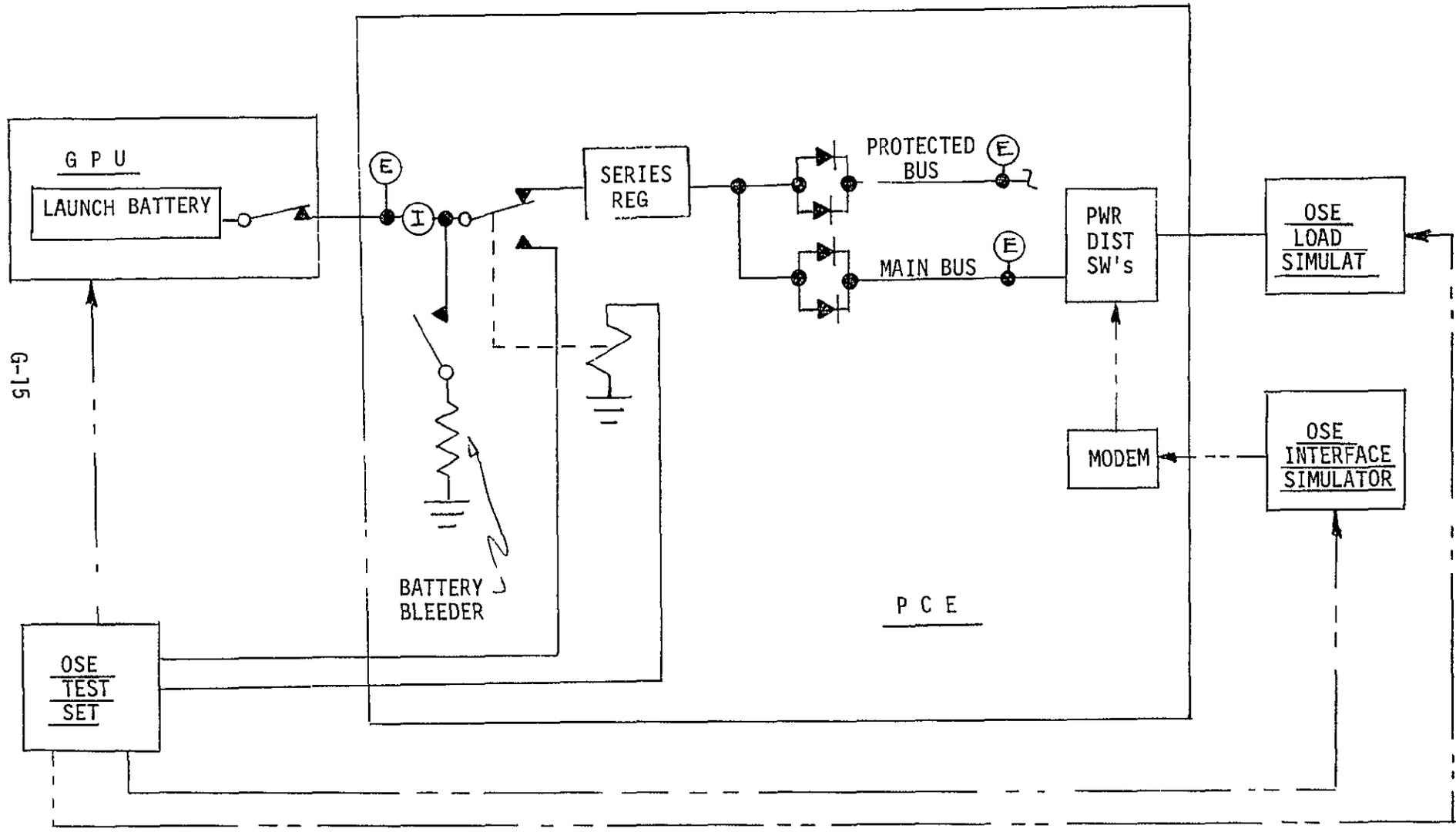
#### Series Regulator

The launch battery will be series regulated to 30 VDC at the main power bus. The OSE GPU will supply simulated launch battery power through the main power interface. The RTG simulators will remain off. An adjustable load will be applied varying from 0 to 300 watts by the load simulator. This arrangement is shown on Figure G-6. The battery voltage and current monitors and main bus and protected bus voltage monitors will be observed and recorded. Proper operation of the series regulator will be verified if the main bus voltage is maintained at 30 VDC  $\pm 1\%$  when the battery voltage is equal to or greater than 30 VDC.

#### Low Voltage Cut-Off

The LVCO circuit will perform load switching should the main bus voltage remain below +27 VDC for a period of time greater than 100 milliseconds.

The OSE load simulator will be configured to supply loads to the power distribution busses which feed the non-critical and redundant critical loads. The RTG #3 GPU simulator will be turned on to bring the main bus



G-15

FIGURE G-6 SERIES REGULATOR TEST

1J86-TOPS-555  
1 August 1970

up to +30 VDC. After the system has stabilized, the RTG #3 simulator will be turned down until the main bus voltage decreases below the operating point of the LVCO. The change in state of the power distribution switches will be monitored by the OSE load simulator. Interconnections for this test are shown on Figure G-7.

To verify that the LVCO does not operate prematurely during a low voltage condition, the test will be repeated but this time the RTG #3 simulator voltage will be cycled from 30 to less than 27 to 30 VDC in a period less than the 100 milliseconds required for LVCO operation. The load simulator will verify that none of the power distribution switches have changed state.

G-17

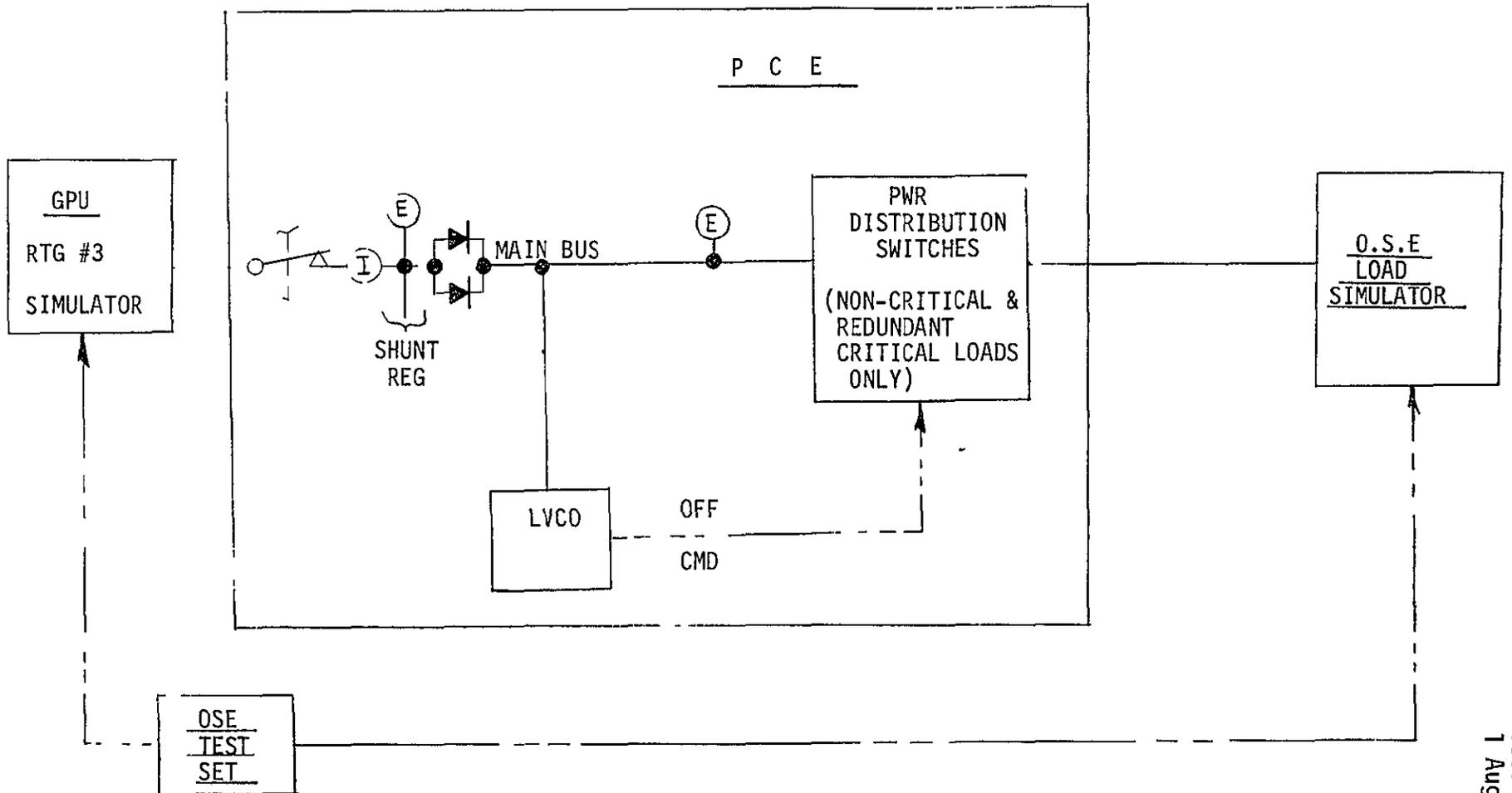


FIGURE G-7

LOW VOLTAGE CUT OFF TEST

**GENERAL  ELECTRIC**  
**SPACE DIVISION**  
**SPACE SYSTEMS ORGANIZATION**

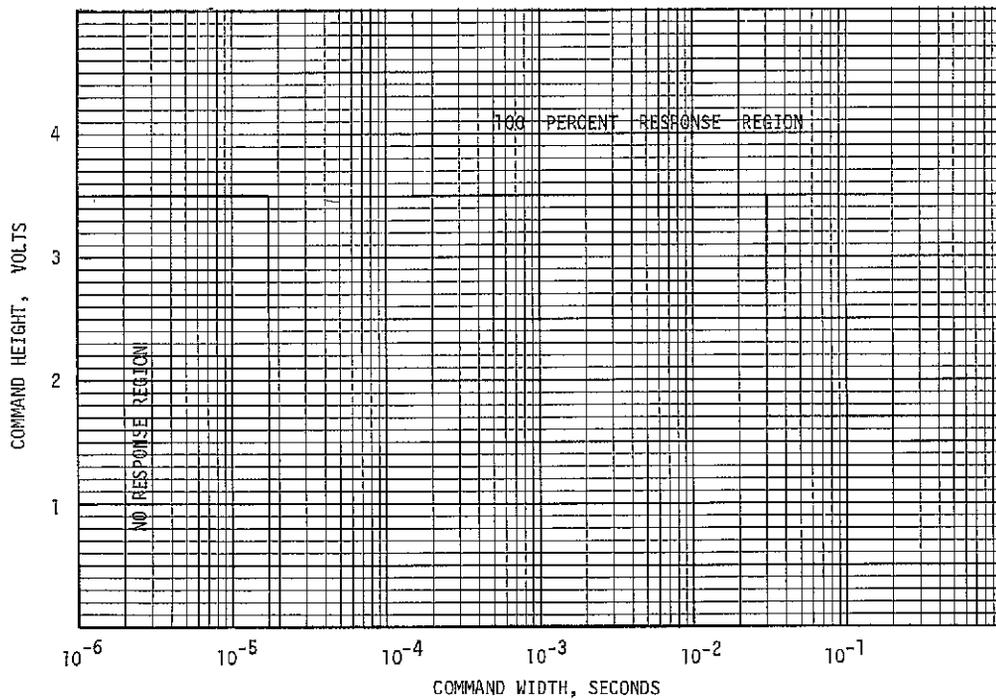


FIGURE D-3 SOLID STATE SWITCH TURN-ON CHARACTERISTICS



1386-TOPS-555  
1 August 1970

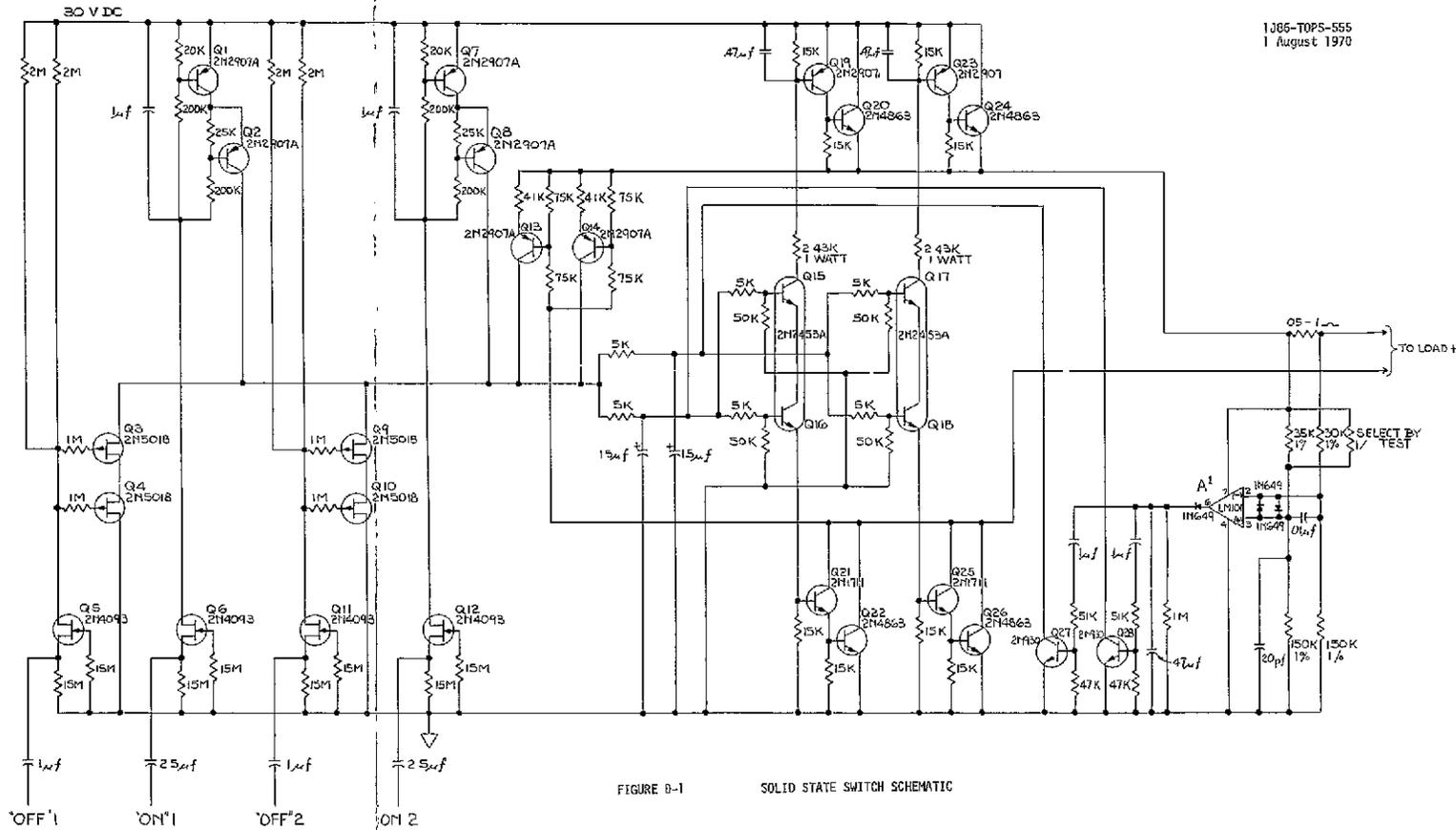


FIGURE D-1 SOLID STATE SWITCH SCHEMATIC

NOTES

RESISTORS  $\pm 5\%$ ,  $\frac{1}{8}$  WATT  
UNLESS OTHERWISE MARKED

D-2

FOLDOUT FRAME

FOLDOUT FRAME 2

APPENDIX D POWER DISTRIBUTION ASSEMBLY

Two types of load switches have been developed and are available for application to the TOPS mission. The first of these is a quad redundant solid state switch whose schematic is shown as Figure D-1, and the second is a quad redundant electromechanical relay switch shown on Figure D-2.

High, low and room temperature evaluation tests were performed on both switches to demonstrate command sensitivity, overcurrent turnoff sensitivity, and fault clearing time. Graphs of command sensitivity are shown on Figures D-3, D-4, and D-5. The shaded areas represent guaranteed non-response as an indication of noise immunity and guaranteed response to assure design margin for the standard command (-3.5 volts, 30 milliseconds). The solid state switch turnoff requirement reflects the 100°C no load condition which is a severe worst case. Turn-off time under simulated fault conditions from ten percent overload to short circuit showed a response time of 0.25 milliseconds minimum to three milliseconds maximum.

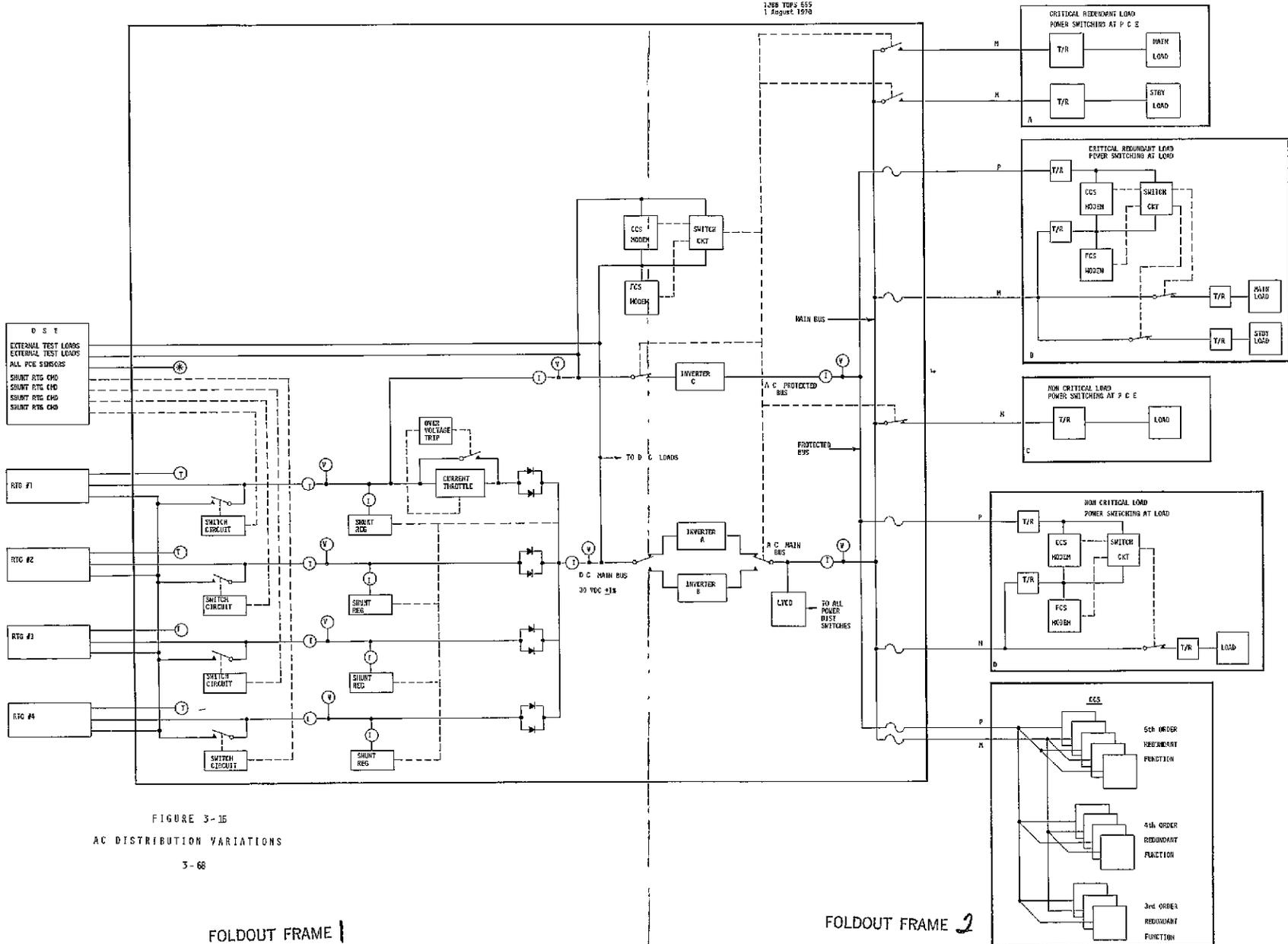
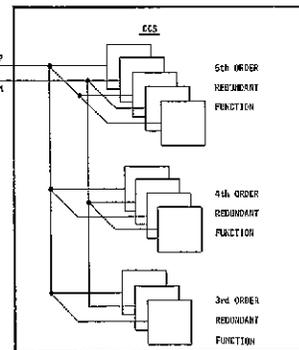


FIGURE 3-15  
AC DISTRIBUTION VARIATIONS

3-68

FOLDOUT FRAME 1

FOLDOUT FRAME 2



FOLDOUT FRAME 1

FOLDOUT FRAME 2

1086-TOPS 555  
1 August 1970

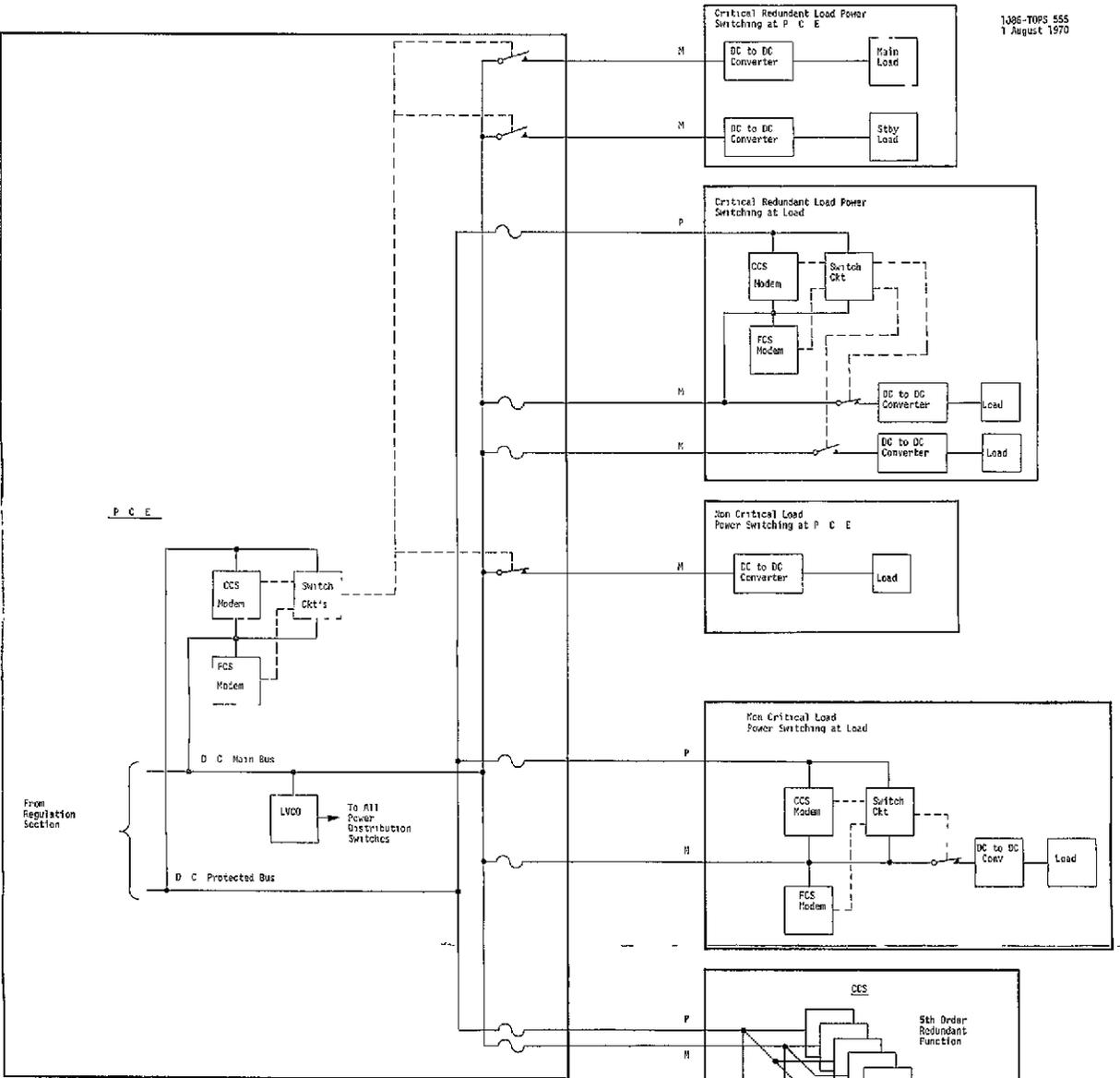


FIGURE 3-15  
DC DISTRIBUTION VARIATIONS

FIGURE 3-7

PRELIMINARY COMPONENT CHARACTERISTICS

COMPONENT/FUNCTION	SUMMARY	PERFORMANCE																				
<b>SHUNT REGULATOR ASSEMBLY</b>																						
<ul style="list-style-type: none"> <li>o Maintains constant RTG load</li> <li>o Regulates DC voltage</li> </ul>	<ul style="list-style-type: none"> <li>o 1 shunt for each RTG (4 total)</li> <li>o 2 assembly design                             <ul style="list-style-type: none"> <li>- controls and transistor assembly in PCE bay</li> <li>- Resistor assembly on separate panel</li> </ul> </li> <li>o 2 section sequence operation to minimize transistor dissipation</li> </ul>	<ul style="list-style-type: none"> <li>o Input/output voltage 30 VDC</li> <li>o Shunt current 0 to 3.2 amps (12.8 amps total)</li> <li>o Regulation <math>\pm 1\%</math></li> <li>o Efficiency <math>\sim 90\%</math></li> <li>o Transient response 100 microseconds</li> <li>o Dynamic impedance 0 to 10 ohms</li> <li>o Dissipation                             <ul style="list-style-type: none"> <li>- Transistor section 0 to 12.5 watts (0 to 50 watts total)</li> <li>- Resistor section 0 to 90 watts (0 to 360 watts total)</li> </ul> </li> </ul>																				
<b>POWER DISTRIBUTION ASSEMBLY</b>																						
<ul style="list-style-type: none"> <li>o Controls Power to Loads</li> <li>o Provides fault protection</li> </ul>	<ul style="list-style-type: none"> <li>o Houses power control devices                             <ul style="list-style-type: none"> <li>- Switches, solid state and/or mechanical relays</li> <li>- Power control circuits</li> <li>- Drive signal conditioners</li> </ul> </li> <li>o Houses fault protection devices                             <ul style="list-style-type: none"> <li>- Fuses</li> <li>- Current trips/limiters</li> <li>- Voltage cutoff circuits</li> </ul> </li> </ul>	<ul style="list-style-type: none"> <li>o Input power 30 VDC, 50 VAC</li> <li>o Input signals 5 volts TTL</li> <li>o Output Various switch actuations</li> </ul>																				
<b>POWER SOURCE AND LOGIC ASSEMBLY</b>																						
<ul style="list-style-type: none"> <li>o Provides source fault protection</li> <li>o Provides telemetry monitors</li> <li>o Provides RTG shunting during prelaunch phase</li> </ul>	<ul style="list-style-type: none"> <li>o Diode isolation circuit</li> <li>o Telemetry circuits</li> <li>o Switching devices</li> </ul>	<ul style="list-style-type: none"> <li>o Diode dissipation 15 watts</li> <li>o Telemetry 0 to 5 VDC analog output 10 kilohms signal impedance</li> </ul>																				
<b>MAIN INVERTER ASSEMBLY</b>																						
<ul style="list-style-type: none"> <li>o Inverts RTG power from DC to AC for general distribution</li> </ul>	<ul style="list-style-type: none"> <li>o Jensen inversion circuit, DC to square wave AC</li> <li>o Synchronized operation by external clock system</li> <li>o Reduced frequency free-run operation</li> <li>o Block redundancy</li> </ul>	<ul style="list-style-type: none"> <li>o Input voltage 30 VDC <math>\pm 1\%</math></li> <li>o Output voltage 50 VAC RMS <math>\pm 3\%</math></li> <li>o Load 90 to 400 watts</li> <li>o Rise time 1 to 5 microseconds</li> <li>o Power factor 1.0 to 0.95 lagging</li> <li>o Efficiency 90%</li> <li>o Frequency, synchronized 4096 Hertz <math>\pm 0.1\%</math></li> <li>o Frequency, free run 4050 Hertz <math>\pm 0.4\%</math></li> </ul>																				
<b>PROTECTED BUS INVERTER ASSEMBLY</b>																						
<ul style="list-style-type: none"> <li>o Inverts single RTG power from DC to AC for protected bus use</li> <li>o Maintains protected bus voltage in case of load fault by means of "Current Throttle"</li> <li>o Provides bypass of "Current Throttle" in case of fault</li> </ul>	<p><b>Inverter</b></p> <ul style="list-style-type: none"> <li>o Jensen inversion circuit, DC to square wave AC</li> <li>o Synchronized operation by external clock</li> <li>o Reduced frequency free-run operation</li> </ul> <p><b>Current Throttle</b></p> <ul style="list-style-type: none"> <li>o Series dissipative regulator operating on input voltage rather than output voltage to maintain "protected bus" at 30 VDC minimum</li> <li>o Overvoltage bypass circuit</li> </ul>	<p><b>Inverter</b></p> <ul style="list-style-type: none"> <li>o Input voltage <math>\pm 1.2</math> VDC <math>\pm 4\%</math></li> <li>o Output voltage 50 VAC RMS <math>\pm 8\%</math></li> <li>o Load 25 watts minimum 110 watts maximum</li> <li>o Rise time 1 to 5 microseconds</li> <li>o Power factor 1.0 to 0.95 lagging</li> <li>o Efficiency 90% at rated load</li> <li>o Frequency, clocked 4096 Hertz <math>\pm 0.1\%</math></li> <li>o Frequency, free running 4096 Hertz <math>\pm 0.1\%</math>, <math>-10\%</math></li> <li>o Redundancy functionally backed up by the main inverter</li> </ul> <p><b>Current Throttle</b></p> <ul style="list-style-type: none"> <li>o Input voltage 30 to 32 VDC</li> <li>o Output voltage 30 VDC <math>\pm 1\%</math> (normal mode) 0 to 30 VDC (throttle mode)</li> <li>o Load current 5.3 amperes maximum</li> <li>o Dissipation 10 watts (normal mode) 120 watts (throttle mode for up to 100 milliseconds)</li> </ul>																				
<b>GYRO INVERTER ASSEMBLY</b>																						
<ul style="list-style-type: none"> <li>o Converts RTG power from DC to two phase AC (90 degree displacement) for momentum wheel power</li> </ul>	<ul style="list-style-type: none"> <li>o Push-pull driven transformer with isolated output circuit</li> <li>o Frequency controlled by external clock signal with internal logic backup</li> <li>o Full square wave output voltage on each phase</li> </ul>	<ul style="list-style-type: none"> <li>o Input voltage 30 VDC <math>\pm 1\%</math></li> <li>o Output voltage 25 VAC <math>\pm 5\%</math></li> <li>o Load 6 watts per phase</li> <li>o Peak load 20 watts total</li> <li>o Phase unbalance 50%</li> <li>o Rise time 1.0 to 5.0 microseconds</li> <li>o Power factor 1.0 to 0.5 lagging</li> <li>o Efficiency 85% at full load, unity power factor</li> <li>o Frequency, clocked 1500 Hertz</li> <li>o Frequency, free running 1500 Hertz <math>\pm 0.4\%</math></li> <li>o Redundancy block redundant with loads</li> </ul>																				
<b>WHEEL INVERTER ASSEMBLY</b>																						
<ul style="list-style-type: none"> <li>o Converts RTG power from DC to two phase AC (90 degree displacement) for momentum wheel power</li> </ul>	<ul style="list-style-type: none"> <li>o Bridge driven autotransformer output circuits</li> <li>o Phase reversal capability by external command</li> <li>o 200 millisecond pulse control with 0 to 100 percent duty cycle capability</li> <li>o Frequency controlled by external clock signal with internal logic backup</li> <li>o Full square wave output voltage on each phase</li> </ul>	<ul style="list-style-type: none"> <li>o Input voltage 30 VDC <math>\pm 1\%</math></li> <li>o Output voltage 26 VAC RMS <math>\pm 5\%</math></li> <li>o Load 6 watts per phase</li> <li>o Phase unbalance 50%</li> <li>o Rise time 1.0 to 5.0 microseconds</li> <li>o Power factor 1.0 to 0.5 lagging</li> <li>o Efficiency 85% at full load, unity power factor</li> <li>o Frequency, clocked 400 Hertz <math>\pm 0.01\%</math></li> <li>o Frequency, free running 395 Hertz <math>\pm 0.4\%</math></li> <li>o Redundancy block redundant with loads</li> </ul>																				
<b>TRAVELING WAVE TUBE CONVERTER ASSEMBLY</b>																						
<ul style="list-style-type: none"> <li>o Converts RTG power to conditioned voltages for TWT use</li> </ul>	<ul style="list-style-type: none"> <li>o Two Jensen inversion circuits with external frequency control and internal free-run backup capability</li> <li>o Undervoltage and overvoltage trip circuit</li> <li>o Low power inversion circuit has current-limit high reactance transformer and provides full square wave output</li> <li>o High power inversion circuit has                             <ul style="list-style-type: none"> <li>- 90 second minimum delay</li> <li>- forced low frequency starting mode</li> <li>- full square wave output with rectification and filtering</li> <li>- 3 post regulators (adjustable)</li> </ul> </li> </ul>	<table border="1"> <thead> <tr> <th></th> <th>INPUT VOLTAGE</th> <th>REGULATION</th> <th>RIPPLE</th> </tr> </thead> <tbody> <tr> <td>HEATER</td> <td>5.0 TO 5.5 VRMS</td> <td><math>\pm 0\%</math></td> <td></td> </tr> <tr> <td>HELIX</td> <td>3400 TO 3500 VDC</td> <td><math>\pm 0.5\%</math></td> <td><math>&lt; 1.0</math> Vpp</td> </tr> <tr> <td>COLLECTOR</td> <td>1425 TO 1525 VDC</td> <td><math>\pm 1.0\%</math></td> <td><math>&lt; 2.0</math> Vpp</td> </tr> <tr> <td>ANODE</td> <td>100 TO 400 VDC</td> <td><math>\pm 1.0\%</math></td> <td><math>&lt; 1.0</math> Vpp</td> </tr> </tbody> </table> <ul style="list-style-type: none"> <li>o Efficiency 82% at full load</li> <li>o Frequency, clocked 2048/4096 Hertz</li> <li>o Frequency, free running 1874 TO 1973/3768 TO 3958 Hertz</li> <li>o Main Power Delay 110 seconds</li> <li>o Redundancy functionally redundant with other transmitters</li> </ul>		INPUT VOLTAGE	REGULATION	RIPPLE	HEATER	5.0 TO 5.5 VRMS	$\pm 0\%$		HELIX	3400 TO 3500 VDC	$\pm 0.5\%$	$< 1.0$ Vpp	COLLECTOR	1425 TO 1525 VDC	$\pm 1.0\%$	$< 2.0$ Vpp	ANODE	100 TO 400 VDC	$\pm 1.0\%$	$< 1.0$ Vpp
	INPUT VOLTAGE	REGULATION	RIPPLE																			
HEATER	5.0 TO 5.5 VRMS	$\pm 0\%$																				
HELIX	3400 TO 3500 VDC	$\pm 0.5\%$	$< 1.0$ Vpp																			
COLLECTOR	1425 TO 1525 VDC	$\pm 1.0\%$	$< 2.0$ Vpp																			
ANODE	100 TO 400 VDC	$\pm 1.0\%$	$< 1.0$ Vpp																			

3-28

1-906-1095-555  
1 August 1970

FOLDDOUT FRAME

FOLDDOUT FRAME

TABLE 3-7 COMMAND INTERFACE DEFINITION

COMMAND SIGNAL CHARACTERISTICS

INPUT VOLTAGE LOGICAL '1'	3.5 to 5.0 VDC
INPUT VOLTAGE LOGICAL '0'	0.0 VDC
MAXIMUM SINK CURRENT	3 MILLIAMPERES
PULSE DURATION	30 MILLISECONDS
RISE/FALL TIME (10% to 90%)	10 MICROSECONDS

VEHICLE CLOCK SIGNAL

INPUT VOLTAGE LOGICAL '1'	3.5 to 5.0 VDC
INPUT VOLTAGE LOGICAL '0'	0.0 VDC
INPUT CURRENT LOGICAL '1'	0.0 MILLIAMPERES
INPUT CURRENT LOGICAL '0'	-0.3 MILLIAMPERES
PULSE WIDTH AT MIDPOINT	3.0 MICROSECONDS
CLOCK FREQUENCY	4.096 KILOHERTZ
RISE/FALL TIME (10% to 90%)	2.0 MICROSECONDS

SIGNAL REQUIREMENTS

CCS COMMANDS

LOAD SWITCH 'ON'	80
LOAD SWITCH 'OFF'	80
PCE FAULT CLEARING	6

FCS COMMANDS

LOAD SWITCH 'ON'	80
LOAD SWITCH 'OFF'	80
PCE FAULT CLEARING	6

VEHICLE CLOCK PULSE	1
---------------------	---

TOTAL	<u>333</u>
-------	------------

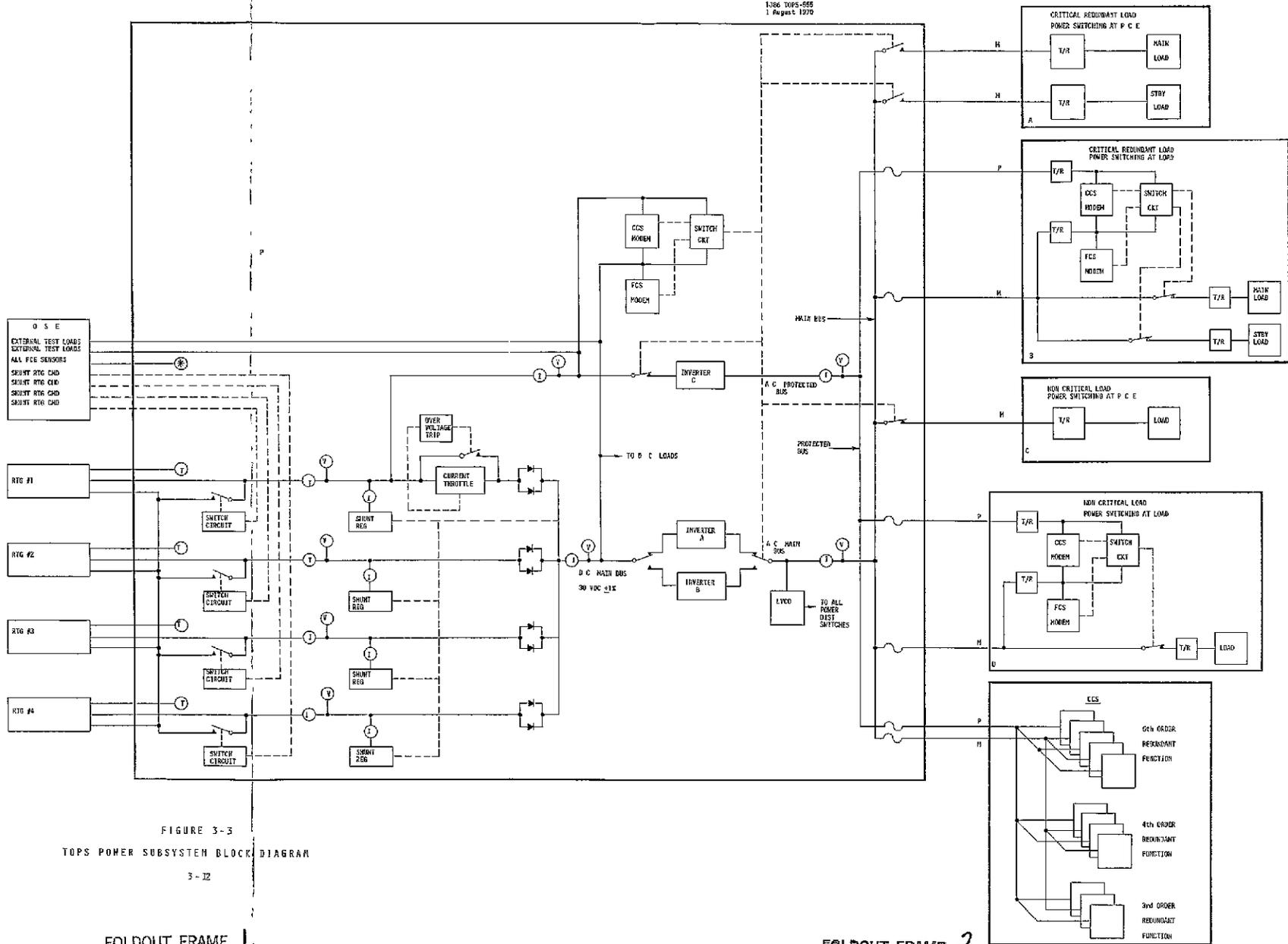


FIGURE 3-3  
TOPS POWER SUBSYSTEM BLOCK DIAGRAM

FOLDOUT FRAME 1

FOLDOUT FRAME 2

A more comprehensive subsystem diagram is shown on Figure 3-3. Significant features over those described earlier are as follows:

- 1 Telemetry measurement points are identified. These are discussed further in 3.2.4.
- 2 RTG shorting switches are installed as a convenient means for preventing the transfer of power from the RTG's during ground preparation and checkout operations.
- 3 An overvoltage trip is incorporated with the current throttle as a backup to a possible open circuit failure of the current throttle.
- 4 Double diode protection is provided for each RTG as discussed further in 3.3.3.2.
- 5 Several power control and distribution options are shown on the right-hand side of the diagram. Further discussion on these options is provided in 3.3.3.4.

### 3.2.2 Physical Configuration

Physically the power system consists of four RTG's; a single bay assembly containing the power conditioning equipment, and a Shunt Resistor Panel (SRP), which contains the resistors of the shunt regulator. Transformer-rectifiers for the detailed conditioning of load power, wheel inverters and TWT converters are considered to be part of the load subsystems. They are included here to permit an overall evaluation of power conditioning weight.

TABLE 2-1 - TASK DESCRIPTIONS

NO	TASK	SCOPE
1 0	Subsystem Requirements	Establish load profiles, mission constraints, technical interfaces, environments, etc through liaison with JPL
2 0	Subsystem Design	Develop design of the subsystem through definition of the following
	System Description	Electrical Configuration - Block diagrams, types of power, power level limitations, transient behavior  Physical Configuration - Size, volume, weight, thermal characteristics, location  Interfaces - computer, telemetry, command, attitude control, etc
	Operational Procedures	Test, ground checkout, flight operations
	Load Management	Power margin analysis
	Reliability	Design status evaluation, where and how redundancy should be applied
3 0	Trade Studies	Evaluation of principal design alternatives
	Distribution Studies	Select the best distribution method from the point of view of efficiency, flexibility, experience, reliability and any other pertinent factors
	Energy Storage Study	Synthesize two power systems with and without batteries. Compare these systems on the basis of weight and reliability. Provide recommendations as to preferred TOPS-PCE approach
	Bus Configuration Study	Evaluate several practical bus configurations from the point of view of tolerance to source and/or load failures and the degree to which service can be restored
	Shunt Regulation Study	Evaluate shunt regulation concepts from point of view of RTG protection, reliability, thermal load and electrical performance characteristics
4 0	Technology Development	Identify required development items and proceed with design & breadboard development
	Power Distribution Assembly	
	Shunt Regulator Assembly	
	TWT Converter	
	Two Phase Inverter Assembly	
	AC Power Conditioners	
	DC Power Conditioners	
	Power Source & Logic Assembly	
	Subsystem tests	Combine development components into a subsystem configuration & perform tests
	Advanced Circuit Development	Development of new and unique circuit concepts
5 0	Program Management	Manage manpower resources, finances, schedules

FOLDOUT FRAME 1

2-3

FOLDOUT FRAME 2

FOLDOUT FRAME 3

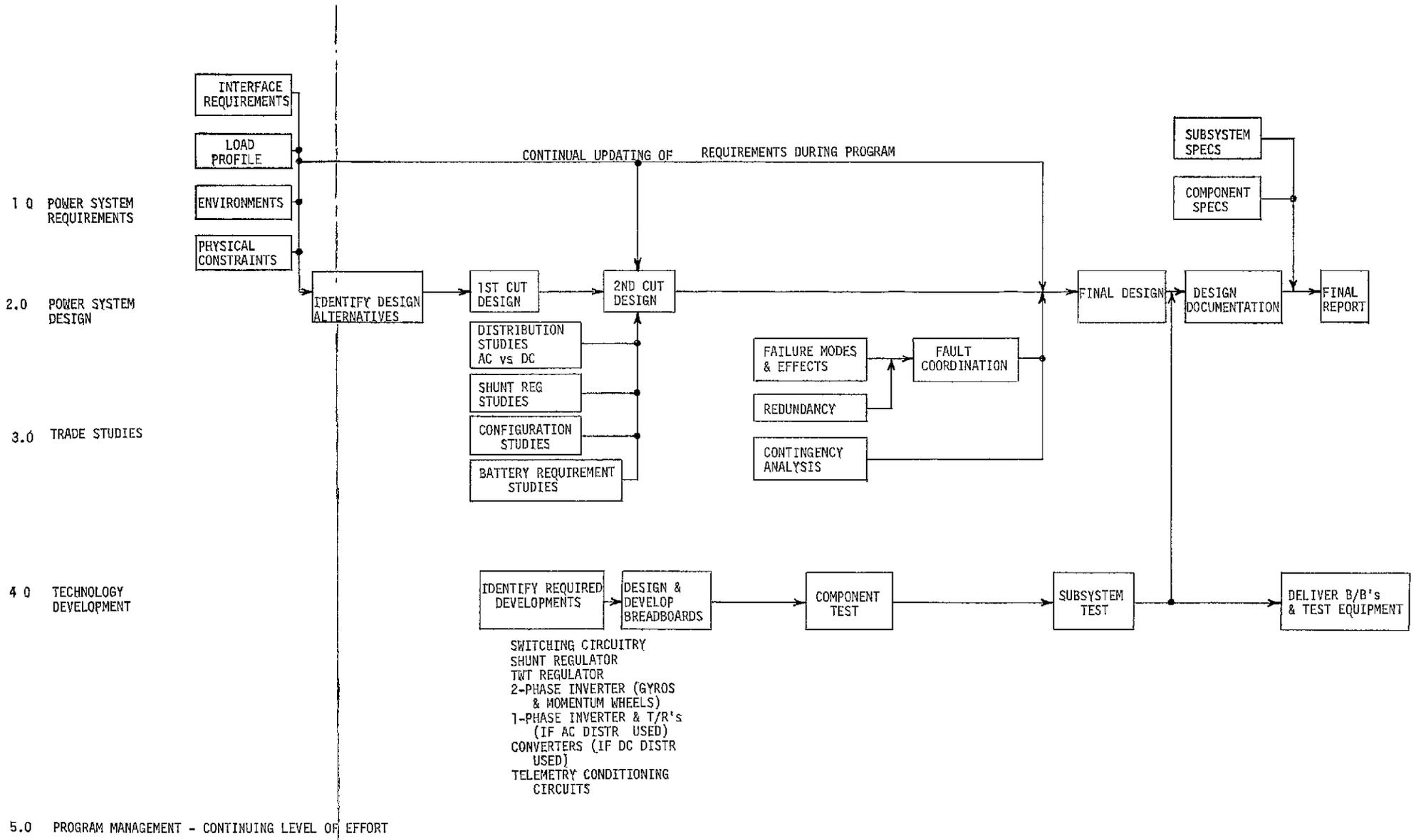


FIGURE 2-1 WORK FLOW DIAGRAM

SECTION 2 STUDY APPROACH

Original goals in the TOPS-PCE program were to establish component requirements early in the contract period with the objective of designing, fabricating and testing three engineering model sets of the PCE for delivery to JPL by July 1970. As the result of reevaluation and extension of the overall TOPS program schedule, the original goals have been modified as follows. Greater emphasis was placed on power system requirements and definition, with particular attention given to the interplay and interdependence with other TOPS subsystems. As planned, only one breadboard set of PCE was fabricated, tested and delivered in July 1970.

A Work Plan reflecting this change in emphasis is shown on Figure 2-1. The activities have been divided into five categories relating to (1) Power System Requirements, (2) Power System Design, (3) Trade Studies, (4) Technology Development, and (5) Program Management. A detailed description of tasks within each category is provided in Table 2-1.