CONCEPTUAL DESIGN AND FEASIBILITY EVALUATION MODEL
OF A 10^8 BIT OLGATOMIC MASS MEMORY

FINAL SUMMARY REPORT
VOLUME 2. FEASIBILITY EVALUATION MODEL

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CONCEPTUAL DESIGN AND FEASIBILITY EVALUATION MODEL OF A $10^8$
BIT OLIGATOMIC MASS MEMORY

Final Summary Report
Vol. 2  FEASIBILITY EVALUATION MODEL

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PREPARED FOR

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This report describes and evaluates the partially populated Oligatonic Mass Memory Feasibility Model. The purpose of this effort was to construct a system to verify the feasibility of the Oligatonic (Mirror) memory approach as being applicable to large scale solid state mass memories.
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1.0 Introduction

The oligatomic thin film technology offers a solid
state, fast access, non-destructive read-out mass
memory exhibiting both low volume and low cost.

This approach is sometimes called the oligatomic
(literally "few atoms") memory because the storage
medium is only about 100 angstrom units thick and
sometimes called Mirror Memory because the storage
medium physically looks like a mirror. These terms
will be used interchangeably throughout this report.

Definition

This memory is made using the mirror technology by
forming a storage "array" consisting of a small piece
of glass (e.g. 2" x 2" or 25.8cm²) upon which is
deposited a copper ground plane and a 100 Å
continuous film of nickel-iron. Storage elements are
not discrete, but are determined by the intersection
of orthogonal word and digit lines later placed over
the array. A large number of arrays are laminated
to a "center board" approximately a foot square,
four to six of which constitute the storage part of
the memory called a "central stack". Hybrid-word
and digit selection and sense preamplifier electron-
ics packages are mounted on similar sized "end boards."
The center boards and end boards are placed in proximity to one another on a planar surface and connected with hinges. Long word and digit line assemblies traversing from an end board across the centerboards (containing mirror arrays) to another end board are laminated in place and connected to end board electronics. A keeper is then laminated over the word and digit lines. The resulting assembly is folded up like a road map to give a memory stack containing storage elements, selection electronics and part of the sense electronics for a large number of bits. A stack of this construction containing 10 million bits would occupy less than one-half cubic foot.

Low Cost
There are very few parts to a mirror memory stack, as can be seen from the description above in addition there are no high density connections to be made because the high density word and digit line assemblies fan out over the end boards to low density connection to the electronics. Univac estimates that this memory can be made at low cost (.2 - .4¢/bit).

Reading
Reading is accomplished by applying a sinusoidal word current whose field oscillates the magnetic
vector through a small angle producing a flux change at twice the drive frequency. Phase of the output signal depends on the orientation of the magnetic vector with relation to the film "easy axis". Thus a "one" or a "zero" is indicated by the phase of the output signal. A shared reference signal is used to allow reading by means of a differential amplifier which compares the phase of the signal of interest to the phase of the reference. Removal of the sinusoidal word current leaves the magnetic vector in its initial state, thus defining a true non-destructive readout memory.

Writing
Writing is accomplished by applying the same word current as in the case of reading, causing the same magnetic vector oscillation while at the same time applying a steering digit current whose field causes the vector to creep to one or the other stable easy axis orientation depending on the polarity of the digit current.

History
The mirror (oligatomic) memory was conceived by E. J. Torok, Univac Defense Systems Division, Research Department in 1967. Initial work verifying the concept led to the operation of a few bits in 1968.
Several years were then spent searching for a combination of the right geometry and material composition offering a large array of bits operating with good margins. Array feasibility was demonstrated early in 1971. The next step in the development cycle was to demonstrate memory feasibility by operating arrays of storage elements spread over large areas as would be the case in a memory stack. This activity, funded by NASA, Huntsville, led to the feasibility model which is the subject of this report.

Feasibility Model
The NASA mass memory feasibility model is a partially populated version of a $10^7$ bit mass memory (Fig. 1.1, 1.2). It contains 8000 bits located at extreme and central areas of the stacks. These locations allow worst case drive currents to be evaluated while avoiding the cost of a fully populated unit. Selection electronics and sense pre-amps were designed and fabricated in hybrid form by thick film and beam lead chip technology. Forty-eight inch word and digit line assemblies were fabricated by a standard photo-lithographic etching process and the mirrors were fabricated by thin film vacuum technology. The feasibility model consists of an exerciser unit and a stack unit. The exerciser contains the control panel, power supplies and electronics for test patterns generation, writing, reading and error detections.
Fig. 1.1 Memory and Exerciser Unit
2.0 Theory of Operation

The oligatonic memory differs from conventional planar film memories in the following ways: (1) The film is 100 Å thick instead of 1000 Å. (2) The bit density (15,000 bits/in²) is 100 times that of conventional flat film memories (e.g., the Univac 1107 control memory or the S-3A solid stack memory) and can theoretically be made greater by another factor of 100; (3) the films are continuous mirrors instead of discrete spots, thus eliminating registration problems; (4) the word current is a pulsed radio frequency alternating current instead of a dc pulse; (5) the film signal is an rf sine wave at double the word current frequency instead of a dc pulse; (6) the sense amplifier is tuned to double the word current frequency (this eliminates capacitive and inductive word noise); (7) the memory has non-destructive readout (NDRO); (8) the memory is "bit organized" (a bit in the middle of an array can be written without disturbing any of its neighbors which allows a "square organization" with a minimum of selection electronics); (9) low level gates are used on the sense-digit lines so that only a few sense amplifiers need be supplied instead of a sense amplifier per line (this reduces cost, power and weight); (10) the word current amplitude is only 50 mA p-p instead of
nearly an ampere; (this means lower power, and is within the current capability of future monolithic integrated selection matrices); (11) switching is by a fast form of magnetization creep instead of rotation (this trades switching speed for higher margins).

The memory is constructed in 5 layers (Fig. 2.1). The glass substrates are coated with 40,000 Å of copper to form a ground plane. After an insulating layer of SiO, a 100 Å layer of Permalloy is vacuum deposited. Photo-etched overlays are attached on top with a spun-on layer of epoxy. A metal foil keeper is placed on top of the striplines. Hybrid word gates are connected to the end of the word lines, and hybrid low level sense-digit gates are connected to the end of each sense digit line. A 10 MHz oscillator supplies the word current. The sense amplifier is tuned to 20 MHz and is used to read a one bit word. The memory is made in a single plane, and then folded like a road map into a more compact package.

An exploded view (Fig. 2.2) of a small portion of the memory will be used to describe the element operation. Each intersection of a sense digit line and a word line defines a bit location.
BASIC STRUCTURE

Digit Lines
4 Mil on 12 Mil Centers

Word Lines
3 Mil on 6 Mil centers

DEPOSITED MAGNETIC FILM
100 Å NiFe

DEPOSITED GROUND PLANE

6 MIL GLASS

Fig. 2.1
If there is a reverse domain under an intersection, the bit is said to be a "1". If there is no reverse domain (i.e., if the magnetization is in the same direction as the surrounding area) the bit is said to be a "0".

The bit is written with a coincidence of word and digit current: A word gate is enabled, sending 50 mA p-p of 10 MHz current from the oscillator down a single word line. This by itself is not sufficient to switch a bit. However, at the same time a digit gate is enabled, sending 35 mA dc pulse down a single sense-digit line. This also is too small to switch a bit by itself. However, where the two lines intersect, the combined field is sufficient to switch the bit by magnetization creep. The polarity of the dc digit pulse determines whether the bit is written into the "1" state or the "0" state.

A bit is read out by enabling a single word gate. This causes the magnetization vector under the whole length of the word line to rotate back and forth with a frequency of 10 MHz. When this happens; the component of magnetization orthogonal to the sense line increases and decreases twice per cycle, so the flux around each sense-digit line changes at a 20 MHz rate. The output of a "1" state differs in phase by
180° from the output of a "0" state. Phase detection is performed using a dummy line (there is one dummy line for every 8 sense-digit lines). The low level gate at the end of the selected sense line is enabled, connecting the sense line to one input of a tuned differential preamplifier. The dummy line is connected to the other input. If both the dummy bit and the bit to be read out are in the same state (i.e., neither has a domain) the output of the differential amplifier is zero. If the bit to be read is in the domain state, its signal is opposite in sign to that of the dummy bit resulting in an output of the differential tuned amplifier. A peak detector converts the ac output to a conventional dc logic pulse.
3.0 Feasibility Model

3.1 General Description

The Film Mass Memory feasibility model consists of two physical modules, the Exerciser Unit and the Memory Unit. The interface between the two modules consists of a 34 conductor cable assembly unit and 3 coaxial cable assemblies. The 34 conductor cable assembly provides the memory unit with addressing logic voltages and d.c. power. The coaxial cable assemblies transmit word and digit current (input data) to the memory unit, and sense voltage (output data) from the memory unit.

3.2 Memory Unit

The memory unit contains the stack assembly. Also contained within the memory unit is the sense amplifier, integrated circuit wire wrap panel (for drive line decoders and stack cable assembly terminations) discrete circuit card wire wrap panel (for logic level translation cards, second level sense selector card, and sense comparator card) and the necessary cable assemblies.

3.2.1 Stack Assemblies

The stack assembly consists of the following subassemblies: 4 memory centerboards, two sense-digit selection boards, two sense-digit termination boards, two word selection boards, and two word termination boards. Attached to the outside of the folded stack is the second level...
word selector card.

a. Memory Centerboard Subassembly

Each memory centerboard has 49 locations measuring 45 x 50 mm for magnetic storage arrays. Each magnetic storage array is fabricated on .178 mm thick glass substrates by vacuum deposition processes. Each centerboard has 2 locations which are populated with tested magnetic storage arrays and are directly addressed by the selection circuits.

Two other locations on each centerboard are populated with untested magnetic storage arrays for purposes of word current monitoring and can be addressed only by physical wiring changes. In addition, 15 other locations have magnetic memory storage arrays immediately under the electronically addressable word and digit lines to represent a uniformity distributed transmission line impedance. The remaining 30 locations are populated only with glass substrates.

Each centerboard contains approximately one half total length of the 4 digit line and 2 word line assemblies which comprise the directly addressed line. Each centerboard also has 2 indirectly accessed digit line assemblies for word current monitoring.
Each digit line assembly 7016709-00 consists of 8 active lines, one dummy line, and one spare line which can be used as an active or dummy line depending on the voltage connections made to the sense digit selector circuit.

Each word line assembly 7016708-00 consists of two groups of 18 lines of which 32 are active and 4 are spare lines. Activation of the spare lines is accomplished by changing connections on the enable inputs of the word line selector circuits.

Counting only active lines, there are 64 sense digit lines and 128 word lines directly accessible in the complete stack. The locations of the active lines in this partly populated stack have been chosen so that a performance evaluation will demonstrate that a fully populated stack is technically feasible.

1. Sense - Digit Selection Board
There are 2 of these subassemblies in the stack each of which consists of 4 hybrid sense-digit selector circuits 7016688, their associated external discrete components (including a multipin input connector and 4 coaxial output cable
assemblies) and the printed circuit base board assembly 7016705.

2. Sense - Digit Termination Board
There are two of these subassemblies in the stack which consist of a ground layer printed circuit baseboard and the digit line assembly termination pins.

3. Word Selection Board
There are 2 of these subassemblies in the stack each of which consists of 4 hybrid word selector circuits 7016687, a multipin input connector, 8 twisted pair cable assemblies, and the printed circuit baseboard assembly 7016706.

4. Word Termination Board
There are 2 of these subassemblies in the stack each of which consists of 4 hybrid termination circuits 7016689 and a ground layer printed circuit baseboard.

b. Second Level Word Selector Boards
This subassembly mounts on the side of the frame next to the folded stack. It consists of a hybrid word selector 7016687, a multipin input connector, a coaxial cable assembly, 16 twisted pair output connectors, a two layer printed circuit assembly 7016710, and a number of discrete components. Some
of these discrete components are used to
match the word current generator (located in
the exerciser) to the load representing the
second level word selector, twisted pair cable
assembly, first level word line selector, and
the word line assembly.

c. Stack Mounting Hardware
Mounting hardware is attached to each subassembly
item a 1 through a 4 inclusive as shown
in the Memory Stack Assembly Drawing, 7016665.

3.2.2 Sense Amplifier
The sense amplifier is a commercial unit manufac-
tured by RHF Electronics Laboratory Model EVT
2004 RFI Serial 5-621-1. Salient characteristics
are 90 db voltage gain at a center frequency
of 20 MHz and a bandwidth of 4 MHz.

3.2.3 Integrated Circuit Wire Wrap Assembly
This unit is manufactured by Augat, model
8136-DG. It is designated as Panel A3 and
serves three functions, 1) as a mount for the
seven MC4006 P decoder circuits required for
address decoding, 2) as a multipin socket to
terminate the five stack cable assemblies
.consisting of 14-14-pin connector plugs) 3)
as a mount for the resistors terminating the logic
signals which emanate from the exerciser unit
via the 34 conductor interface cable. Circuit and plug assignments are shown on drawing 7016703.

3.2.4 Discrete Circuit Card Wire Wrap Panel
This panel is Univac fabricated. It is designated as Panel A4, and is used to house 14 type 7016690 translator cards (designated EXP - 6550A1) the second level sense selector card 7016711, and a single sense comparator card (designated ICBM-4). All of these cards are pluggable via 15 pin male card connectors. Card assignments are also shown on drawing 7016703.

3.2.5 Memory Unit Chassis Assembly
This assembly 701663 consists of a metal framework with front and back panels which houses the stack, sense amplifier, and panels A3 and A4. This assembly then slides into a standard commercial enclosure (Optima E - 081920 D Instrument case).

3.3 Exerciser Unit
The exerciser unit consists of the exerciser control panel, integrated circuit wire wrap panels A1 and A2, discrete circuit card panel A5, five dc power supplies (commercial grade), rear panel (with cooling fan), and the exerciser unit chassis assembly. Primary power required for this unit is 60 Hz single phase 115 ± 10 volts with a load capacity of at least 5 amperes.
3.3.1 Control Panel

The control panel has two functional groupings of controls. The left 1/3 of the panel consists of the controls for: primary power, secondary power increment, memory digit and word current increment, and sense threshold. In addition a meter in conjunction with two other switches monitors these voltages and currents. The remaining two-thirds of the panel consists of the controls and indicators necessary to exercise the memory unit. Because of the number and complexity of these controls a separate checkoff list for functional checkout is included in a separate section, 3.2

3.3.2 Integrated Circuit Wire Wrap Panels A1 and A2

These two panels together are required to hold the integrated circuits necessary to exercise the memory unit and to permit their interconnection. A plug strip at the rear of each panel permits the 8 front panel interface cable assemblies to be removed easily should maintenance be required. The circuit locations chart, drawing 7016703, shows the location of the 119 integrated circuits and the 8 interface cable assemblies used in this assembly.
3.3.3 Discrete Circuit Card Panel A5
This panel is used to mount the digit driver card designated (DIGIT DRIVER 8NK) and the word driver card designated (WORD DRIVER 8NK). Each card is pluggable via a 15 pin male connector. The output of the word driver card is transmitted via a coaxial connector and a coaxial cable assembly to J9 on the rear panel. The word driver frequency is nominally 10 MHz and is crystal controlled. Power capability of the word driver output stage permits an output current of 35 ma rms in a 400 ohm resistive load. Digit driver current capability is ± 75 ma dc. in a 100 ohm resistive load. The output current on each card can be incremented or decremented separately a predetermined amount by means of front panel controls.

3.3.4 Power Supplies
Five dc power supplies are used to power the exerciser and memory. The list below gives the nominal supply voltage, vendor name and model, and whether the voltage can be incremented via the front panel switch.
<table>
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<th>MODEL NO.</th>
<th>INCREMENTED</th>
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<td>+5</td>
<td>LAMBDA</td>
<td>LXS-B-5</td>
<td>No</td>
</tr>
<tr>
<td>-5</td>
<td>LAMBDA</td>
<td>LCS-B-01</td>
<td>Yes</td>
</tr>
<tr>
<td>+25</td>
<td>LAMBDA</td>
<td>LCS-B-03</td>
<td>Yes</td>
</tr>
<tr>
<td>-25</td>
<td>LAMBDA</td>
<td>LCS-B-03</td>
<td>Yes</td>
</tr>
<tr>
<td>+100</td>
<td>TEC LITE</td>
<td>LPS-102</td>
<td>No</td>
</tr>
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The purpose of incrementing or decrementing the voltage supplies is to demonstrate the functional reliability of the memory circuits (line selectors, logic translators, current drivers, sense preamplifiers and sense amplifier). The exerciser logic supply is not altered since the reliability of these commercially available circuits is well known.

3.3.5 Rear Panel

The rear panel serves to mount the following components: cooling fan, power receptacle, fuse holder, memory interface connector J12, word current output jack J9 digit current output jack J10, exhaust air louvers, and test point jack J13.

3.3.6 Exerciser Unit Chassis Assembly

This assembly consists of the framework to which items described in Sections 3.3.1 through 3.3.5
inclusive are attached, according to drawing 7016662. This complete assembly slides into an Optima model E-081920 HD Instrument Case enclosure. A necessary part of this assembly are the power cord and interface cable assemblies: 1 multiconductor and 3 BNC (male connector ends).
3.4 Block Diagram

The NASA Feasibility Evaluation Unit Block Diagram (Fig. 3.1) consists of a memory assembly, memory array, address selection circuitry, pattern and data selection circuitry, data checking circuitry, and a timing section.

The memory assembly contains the selection circuitry for accessing the memory array. The word selection matrix system has 128 first level gates and 16 second level gates. These gates distribute the 10 MHz word current to the 128 word lines. The sense-digit selection matrix system has 64 low level gates, 8 sense preamps with gates and 8 high level digit gates. The 64 low level gates are common to both writing and reading functions.

The memory array section is assembled from 4 center boards. The center boards are only partially populated. The 2048 bits on each board are accessed by 64 word lines and 32 sense-digit lines. The combined memory array section is represented by 128 word lines and 64 sense-digit lines.

The address selection circuitry consists of FET drivers that selectively enable 24 word gates, 8 sense-digit gates. These FET drivers are selected by 6 decoders.
which are operating off the address counters.

The pattern and data selection circuitry consists of the digit driver, bipolar generator, address and data mode controls, and automatic pattern control. These circuits allow manual or automatic data and pattern, writing and reading of the memory array.

The data checking circuitry consists of a video detector, a strobed comparator, data register, data compare, and error counter. A narrow pulse is used to strobe the comparator to sample signal amplitude during an interval of minimum noise. The data is then at a logic level and is stored in the data register. The indicator lights give a visual result on each bit or a total can be read off the error counter.

The timing section provides 8 timing pulses of equal intervals. These intervals are distributed thru the system to enable the proper sequence.
3.5 Circuit Diagrams

Included in this section are all the diagrams with the exception of those for commercial purchased power supplies. No attempt will be made to describe each of these circuits; however, there is a discussion of the hybrid circuits made at Univac in Section 4.2.

- Switches and Indicator Lights
- Power Distribution
- Circuit Location Chart
- Clock, Divider, Phase Counter and Decoder
- Word Address Counter
- High Digit Address Counter
- Sense-Digit Address Counter
- Decoders
- Digit Driver and Input Register
- Output Register and Error Compare
- Word Driver 8NK
- Digit Driver
- Memory Stack Circuit Layout
- Word Line Terminator Circuit
- Decoder/Memory Selector Interface
- Sense-Digit Line Selector 8NK
- Second Level Sense Selector
- Digit Selection Board
- FET Selection Line Driver
- Word Line Selector Circuit
- Second Level Word Selector
- Sense Amplifier
- Signal Envelope Detector
- Comparator Card
Fig. 3.13
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**UNIVAC**

**WORLD TELEGRAPH CIRCUIT**

**Fig. 3.15**
**PART NO.**

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**FOR MATE REQUIREMENTS SEE**

**UNIVAC**

**FEDERAL SYSTEMS DIVISION**

**UNIVAC PARK, PAUL, MINN. 55111**

**WORD LINE SELECTOR CIRCUIT**

**DIMENSIONS IN INCHES TOL ON**

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**APPROVED**

**NEXUS ASSY USED ON**

**APPLICATION**

- Threads: Ext F/3A, Int Cl 2B

**SCALE**

- CT

**CLASS**

- SW

**SHEET OF**

- 1

**Fig. 3.21**
4.0 Evaluation

4.1 Introduction

This evaluation covers the functional operation of the special hybrid circuits developed by Univac for this application and the functional operation of the stack. The sections on Stack Description (Sec. 4.3) and Evaluation Method (Sec. 4.4) establishes the baseline for the Functional Stack Operation (Sec. 4.5) discussion. While there are conclusions drawn throughout Section 4, the summary of the conclusion for the total feasibility model is presented in Section 5.
4.2 Hybrid Circuit

4.2.1 Electrical Function

There were three hybrid circuits which were developed for this contract from the discrete circuit breadboard stage. All performed as expected.

a. Sense Digit Line Selector - The first of these the sense digit line selector Fig. 4.1 (same as 3.17) selects 1 of 8 active digit lines connected to the active input terminals. (Pins 1,3,5,7,9,11,15) Each input terminal (pins 1,3,5,7,9,11,13,15,17 and 19) is connected to source terminal of an 2N4856 (N channel JFET) and terminated with a 60 resistor to ground (pins 2,4,6,8,10,13,14,16,18, and 20). Eight of the JFET's serve as low level gates for sense signal and high level gates for digit current. The gate terminals of each of these FETs (1-8) are connected to a resistive AND circuit one terminal of which goes to the first level select pins (32-39) and the other goes to the common group select pin (40).

The drain terminals of each of these FETs are wire OR ed together and connected to the emitter of a 2N2222 NPN transistor through an ac coupling capacitor. The active drain bus is connected to outside world via pin 25 and also to the source of another JFET (9) serving as a second level digit gate. The gate
terminal of this last FET is connected to a resistive AND circuit, one terminal of which is connected to the hybrid chip or group select (pin 40) and the other to the digit write select (pin 31).

A single JFET (11) serves as a low level gate for the dummy sense signal (pin 17) and as a high level gate for dummy digit current during the initialization procedure. The drain of this FET is connected to pin 24, the source of the second level dummy digit gate (10) and to the base of the 2N2222 through an ac coupling capacitor. The gate terminal of the second level dummy digit FET (10) is connected to a resistive and one terminal of which is connected to the group select (pin 40) and the other of which goes to pin 29. The gate terminal of the first level dummy FET is connected only to pin 40 through a resistor.

A single JFET (12) is a spare device. The drain is brought out to pin 22 and the gate connected to the group select pin 40, and to pin 28 through a resistor. The spare can be used to replace either a defective first level active gate (1-8) or the dummy gate (11) by appropriate external wiring.

The collector of the 2N2222 transistor is brought out to pin 27. External discrete components,
(which includes a parallel tuned transformer) provide the transistor with the proper collector voltage and couples the sense signal (which is the difference between the base and emitter voltages) to the second level of sense selection. The emitter is connected to pin 26 through a resistor to limit the transistor collector current. Pins 23 is an isolated ground for the transistor stage and pin 21 is an extension of the input grounds. The drain of second level active digit (9) and dummy digit (11) FETs are connected together at pin 30 which is the common digit bus input. Voltages for the gate terminals of the FETs are 0 volts when selected and -25 volts when unselected. The large gate resistors (20K) are used to maintain the gate voltage near the source and drain voltages which linearizes the transfer curve and reduces the generation of second harmonics. The transistor stage is designed to operate at a collector voltage +5 volts and an emitter voltage of -5 volts. The active and dummy drain buses are brought out to pins 25 and 24 to enable the spare to serve as either a dummy or active gate and also to permit external balancing of the sense preamplifier (2N2222) inputs.
To select any function on the chip (or in the group), the group select pin 40 must be high (zero volts). To select a digit-sense line, one pin of (32-39) must be high. When reading pins 29 and 31 must be low (-25 volts). When writing an active line, pin 31 must be high and pin 29 must be low. During the initialization procedure (when writing the dummy) pin 29 must be high and pin 31 low.

There is a maximum digit current of 45 ma which can be applied to the digit bus, pin 30. Larger values than this require a large enough drain to source voltage which will tend to reduce or increase the drain to source resistance depending on the current polarity. The end result is non-uniformity of digit currents throughout the memory array. The digit current uniformity was within ± 10% in the feasibility model.

The differential amplification of the WZ7Z2 works for low level (microvolt) signals of either polarity. As the signal level increases to the millivolt level, one polarity will be distorted due to diode action of the base emitter junction. This is not a problem in the feasibility model.

A single chip of this type is used as the second
chip to reduce the second harmonic distortion.
c. Word Line Termination - This chip consists of 18 terminating resistors - $8\Omega + 10\%$. The input terminals are arranged to exactly match the word-selector chip. The terminals on the opposite side of the chip are all connected to the internal ground levels.

4.2.2 Mechanical Characteristics
a. General - All three hybrid circuits utilized a standard lead frame having a configuration of 20 pins (on 50 mil centers) on either side of the 1 x 1.25 package.
b. Fabrication
1. Screen Printing
   (850°C) on 2 x 2 x .025 inch 96% alumia substrate
   1st screen- Termination Pads: 165 mesh screen, DP-8553 Platinum/Gold
   2nd screen- 1st metal: 325 mesh screen, Alloys C-5011 Gold
   3rd screen- Birox Resistors: 250 mesh screen
      Word Gate - 10 ohms per square Birox
      Sense Digit - 10K ohms per square Birox
      -100K ohms per square Birox
2. Ring Frame Attachment
   -1.0 x 1.0 Cermaic Ring Frame (.880 x .880 x .060 cavity)
   -Ring Frame attached by screening ESL 4009
level of sense selection.

b. Word Line Selector - The word line selector consists of two arrays of 9, 2N4856 JFETs as shown in Fig. 4.2 (same as 3.21). Each of the 9 FETs have an input pin connected to its source. Each gate is connected to a separate select pin through a 5K resistor. All 9 drains are connected together and brought out to pins 30 or 31, the word current input terminals.

When a FET is selected the gate voltage must be high (zero volts) and the 10.3 MHz word voltage present at the appropriate input 30 or 31. All unselected lines are at -25 volts. The selected FET is in a low resistance state permitting bipolar current flow. At current levels higher than 65 ma (p-p) waveform distortion appears (due to modulation of the on resistance). Currents in the feasibility model are below 60 ma (p-p).

One FET of each group of 9 is used as a spare device in the feasibility model. Only eight of these chips are required as first level gates for the 128 active lines. A single chip serves as a 1 of 16 line second level selector in the feasibility model. A single parallel turned 20.6 MHz trap is used between the word driver and the second level word line selector.
Fig. 4.2
solder glass to base substrate and on ring frame using 165-200 mesh screen.

- Preglaze 3½ min. @ 450°C.

- Seal ring to cover - Weight with 50 gms and fire for 20 minutes at 475°C. This causes approximately 4% decrease in 10K ohms resistor paste and 2% decrease in 100 ohm resistor paste values. Gold bonding areas are burnished with a fiberglass typewriter eraser prior to and after glass sealing.

3. Device Bonding

Devices are bonded by applying a small amount of Alloys Unlimited T-2003 conductive gold epoxy to bonding pads. (Approx. .010 in diameter drop of paste applied with a .005 inch wire in a pin vise). Capacitors are bonded in similar manner by applying gold paste to both substrate terminations. After placing devices in proper location, the assembly is heated at 250°C for 1 hour. In the case of the sense-digit circuit the beam lead transistor is thermo compression bonded prior to other devices since substrate temperature required is 325°C.

4. Wire Bonding

FET devices and capacitors are bonded using a Kulike and Soffa 472 ultrasonic gold wire ball bonder.
Approximate settings are:

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<th>Time</th>
<th>Force</th>
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<tr>
<td>2nd bond</td>
<td>4.50 low</td>
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Bond pull test with .001 inch diameter gold wire (3-5% elongation) produce typical force levels of 5-6 gms.

5. Electrical Test

6. Lead Attachment

Substrate termination bonding pads (Platinum/Gold) are dip soldered in a solder pot containing 10/90 Tin/Lead solder at 610-620°F. Alpha 711-35 flux is used to precoat pads prior to dip soldering. Care should be taken to prevent flux or solder from contacting the interior of the package. The leads are etched beryllium copper (.006 inch thick) which have been plated with 100 microinches of nickel and 70 microinches of gold. The leads are solder dipped on the end 3/16 inch of the lead frame. Substrates and leads are cleaned with Dupont 8529 flux remover followed by cleaning in TP-35 freon and TF freon.

The Platinum/Gold termination pads which have been pretinned are coated with a thin layer of 711-35 flux and the tinned lead frames positioned and aligned to the substrate. The complete assembly
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is placed on a 3 x 3½ inch ceramic substrate with 1 x 1 x .025 ceramic substrates placed under lead frames to position them at the proper height. The entire assembly is placed on a hot plate (650°C) and heated until solder reflows, then removed. Flux is removed and parts cleaned in a manner similar to the post tinning procedure. Complete removal of flux is essential prior to the final sealing operation. Shorting buss is cut from lead frames at this time.

7. Electrical Test and Precap Visual

8. Sealing

Units are baked at 130°C for 2-4 hours in a vacuum oven prior to sealing. Sealing is accomplished using a 1.0 x 1.0 x .025 inch alumina substrate and a perform made from Duroseal b-stage fiberfilled epoxy, .007 inch thick. This frame-type perform has outside dimensions of 1.0 x 1.0 and inside dimensions of .800 x .800 inches.

The ceramic substrate which is used for a cover is screened with appropriate markings prior to sealing. Material used is Wornowink series M marking ink (Mixed 12 parts resin, 1 part catalyst by weight). Curing is accomplished
at 125-150°F for one hour.

The epoxy perform is attached to the cover by placing a drop of solvent (acetone or MEK) on the corners of the preform, positioning the preform on the underside of the cover and curing at 190°F in a circulating air oven for 20 minutes. The cover with attached preform is aligned over the package ring frame and clamped in place using a bulldog paper clamp. The assembly is heated at 250°F for ten minutes and temperature is increased and the assembly cured for a minimum of 20 minutes at 350°F. The assembly is removed from the oven and cooled prior to removing clamping force. A bead of Eccocoat C26 is placed over the solder joints, where lead frames are attached, and cured per vendor recommendations.

9. Final Electrical

All previous electrical tests prior to sealing are performed in a similar manner to the following brief outline:

1. Measure source-drain resistance at 50 ma current. This should be less than 25 ohms.
2. Measure turn-off threshold across gate-drain junction with proper bias applied. This should measure 9 volts or less.
4.3 Stack Description

a. Major Assemblies

The stack consists of the following major components: 4 memory center boards, two digit selection boards (DSB-1, and DSB-4) with hybrid circuits, two digit termination boards DSB-2 and DSB-3), where the digit overlays are connected to ground, two word selection boards (WSB-1 and WSB-2) with hybrid circuits, and two termination boards (TB-1 and TB-2) with hybrid terminating resistors.

A plan view of stack is shown in Fig. 4.3 with the substrate identification numbers and drive line addresses.

b. Centerboard Assembly

The centerboard assembly consists of the following major components 1) 4 base boards 2) 8 functional magnetic arrays 3) 4 word line overlays 4) 8 addressable digit line overlays 5) 4 non-addressable digit line overlays 6) 68 non-functional magnetic arrays 7) 120 glass substrates 8) keeper material bonded over each centerboard subassembly 9) hinges and hardware.
Fig. 4.4 is a photograph of the centerboard assembly prior to bonding the keeper over each centerboard subassembly. Extremely dark areas are the locations of magnetic arrays. Medium dark areas show where the adhesive and the substrates make good contact. Light areas represent poor adhesive contact to the glass and point out potential problem areas. This could be due to insufficient hot press pressure, poor adhesive coating, or subsequent delamination during the assembly process.

c. Overlays

The overlay artwork was made on flexible film with a Gerber plotter, using a computer generated pattern. Photo lithographic and etching techniques were used to fabricate the overlays from the laminate.

The line widths were preadjusted for the expected etch factor so that the final assemblies would be within specification. The laminate for the overlays was made by a vendor to our thickness specifications: 0.5 mil Kapton bonded to 0.5 mil copper with the total thickness not to exceed 1.4 mils.
The finished digit line overlays were to have a width of 4 mils, and spacing of 12 mils. Each digit overlay contained 10 lines of which only one could be bad prior to assembly. The finished word overlays were to have a width of 3 mils on 6 mil centers. Each word overlay contained 36 lines of which two could be bad prior to assembly. Some bad lines had to be tolerated to achieve a usable yield within the time schedule allowed.

All overlays were tested with a digital ohmmeter for opens and shorts and then visually inspected. No etchouts or bumps were allowed which exceeded 50% of the line width in the area of addressable digit and word line intersections.

Figures 4.5 and 4.6 show the dc resistances of the actual memory overlays prior to assembly. Only two digit lines were open and definitely defective initially.

After assembly of the stack had been completed and prior to evaluation the line resistances were again checked. The following table is a list of known bad address due to defective lines (open or shorted)
### Sense/Digit Overlay Line Resistance Measurements

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Fig. 4.5
Word Overlay Line Resistance Measurements

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<td>27.3</td>
</tr>
<tr>
<td>33</td>
<td>24.4</td>
<td>26.0</td>
<td>25.3</td>
<td>27.1</td>
</tr>
<tr>
<td>34</td>
<td>24.5</td>
<td>26.0</td>
<td>25.2</td>
<td>27.1</td>
</tr>
<tr>
<td>35</td>
<td>24.2</td>
<td>25.6</td>
<td>25.9</td>
<td>26.8</td>
</tr>
<tr>
<td>36</td>
<td>24.1</td>
<td>26.5</td>
<td>25.8</td>
<td>26.7</td>
</tr>
</tbody>
</table>

Fig. 4.6
Dy Lines

000 6 (Replaced w/spare)
001 6 (Replaced w/spare)
011 S, 2, 4, 7 Not used in Evaluation
100 2 (Replaced w/spare)
101 4 (Replaced w/spare)
110 4?
111 1, 3, 4, 5, 7 Not used in Evaluation

Wy Lines
0111 3, 5, 7

Because of the large numbers of bad lines in Dy groups 011 and 111, no attempt was made at evaluation. The cables carrying sense information from these addresses have been disconnected prior to shipment.

Late on Feb 3, a partially defective hybrid word selection circuit showed up at wordgroup address 0011. Due to the delivery schedule it could not be replaced. Even if time were not a factor, the overlays would have to be removed and be replaced without damaging the lines. Previous experience has shown this to be unlikely. As a result, the twisted pair carrying the word current from the second level word selector card has also been disconnected before shipment.
Since this selection group was not functional, some of the line tabs were removed from the selection circuit to facilitate a word line impedance measurement. In the process, the lines were damaged, as was expected, and are also no longer functional.

d. Magnetic Arrays
The magnetic arrays were fabricated by vapor deposition on 9 mil glass substrates. Fig. 4.7 shows the crosssection of the magnetic array mounted on the baseboard with both overlays and the keeper bonded to it. The dimensions shown in Fig. 4.7 were the design goal, the actual measurements cannot be determined without a destructive test of the centerboard assemblies.

Prior to beginning the deliverable stack assembly, a mechanical dummy was assembled to gain experience. This stack was sectioned with Fig. 4.8 showing the results.

The eight magnetic arrays used in the deliverable stack were tested on a single bit basis prior to
Fig. 4.7 Crossection of Centerboard Showing Magnetic Array Construction
Fig. 4.8 Sketch of the Sectioned Dummy Centerboard Showing Actual Dimensions
assembly. The test data is shown in Fig. 4.9. This data shows a lower digit current $I_{DW}$ to write a saturated 1 than was needed during stack evaluation testing. A larger digit line to magnetic film spacing than that maintained in the single bit test could yield these results. If the digit line were significantly further away, the field would be less for a given current and it would spread further creating a neighbor bit disturb problem.

4.4 Evaluation Method

a. Functional Description of Writing and Reading

The first functional criteria for any alterable memory is the ability to write and read data. In the oligatomic memory technology, a logical 1 is represented by formation of a magnetic domain in the storage media under the intersection of the selected word and sense digit lines. A logical 0 is represented by no domain formed at the intersection. If a one has been written, a zero is obtained by annihilation or erasure of the domain. Therefore, writing a logical zero or erasing a logical one are equivalent. In the feasibility unit, a bipolar digit pulse is used to minimize disturb problems (see Section 4.5c for further explanation).
<table>
<thead>
<tr>
<th>#</th>
<th>$I_W$</th>
<th>$I_{Dw}(1')$</th>
<th>Ide</th>
<th>$I_{Dd}$(disturb)</th>
<th>$H_C$</th>
<th>$H_K$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ma(p-p) Nucleate Full '0'</td>
<td></td>
<td>25%</td>
<td>100%</td>
<td>oe</td>
<td>oe</td>
</tr>
<tr>
<td>P-7618-2</td>
<td>50</td>
<td>11</td>
<td>18</td>
<td>6</td>
<td>22</td>
<td>24</td>
</tr>
<tr>
<td>P-7620-4</td>
<td>50</td>
<td>13</td>
<td>22</td>
<td>6</td>
<td>25</td>
<td>29</td>
</tr>
<tr>
<td>P-7626-2</td>
<td>50</td>
<td>10</td>
<td>16</td>
<td>6</td>
<td>22</td>
<td>28</td>
</tr>
<tr>
<td>P-7626-4</td>
<td>50</td>
<td>14</td>
<td>20</td>
<td>6</td>
<td>22</td>
<td>25</td>
</tr>
<tr>
<td>P-7626-5</td>
<td>50</td>
<td>10</td>
<td>16</td>
<td>8</td>
<td>23</td>
<td>28</td>
</tr>
<tr>
<td>P-7632-2</td>
<td>50</td>
<td>10</td>
<td>19</td>
<td>5</td>
<td>22</td>
<td>27</td>
</tr>
<tr>
<td>P-7632-4</td>
<td>50</td>
<td>12</td>
<td>18</td>
<td>3</td>
<td>17</td>
<td>17</td>
</tr>
<tr>
<td>P-7622-5</td>
<td>50</td>
<td>10</td>
<td>17</td>
<td>6</td>
<td>22</td>
<td>25</td>
</tr>
<tr>
<td>P-7626-4</td>
<td>45</td>
<td>18</td>
<td>28</td>
<td>10</td>
<td>27</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td>50</td>
<td>14</td>
<td>22</td>
<td>7</td>
<td>30</td>
<td>31</td>
</tr>
<tr>
<td></td>
<td>55</td>
<td>9</td>
<td>12</td>
<td>8</td>
<td>16</td>
<td>26</td>
</tr>
</tbody>
</table>

Fig. 4.9 Magnetic Array Test Data (Before Assembly)
This means that complement data is first written at the selected location followed immediately by true data during the same memory cycle.

Differential sensing is used in the feasibility unit with the reference line or dummy shared for each 8 active digit lines. The dummy must remain in the logical zero state, if information contained in any of its 8 shared lines is to remain accurate.

The differential output (single ended) is gated at the second level sense-selection card to the high gain tuned sense amplifier. The output of the sense amplifier is detected by an envelope detector which feeds one side of a strobed differential comparator. The reference side of the comparator is controlled by the threshold voltage adjustable from the front panel. The output of the comparator is stored in a flip flop until the beginning of the next memory cycle. The flip flop output is sent to a compare circuit which compares output data with input data from either the pattern generator or the input register. The non-compared output is accumulated in the error counter.
b. Initialization

To insure that all memory arrays start with identical dummy states, a special write procedure called the Initialization Procedure is used. During this procedure, first all active digit lines are driven by a -110 mA current pulse which lasts for the full write cycle. Then all the dummy digit lines are driven from this same source. This procedure was used prior to each evaluation test to insure that all previous domains were erased. A low word current should be used or the word current interconnect cable disconnected during this procedure.

c. Read Zeroes

After the initialization procedure all addresses are read. In the evaluation tests the threshold voltage was the independent parameter, with the error counter output the dependent parameter. After the useable range of threshold voltage has been covered, the test is completed and the data is converted to graphical form. If the input data register was set, the output of the error counter represents those bits greater than or above the threshold voltage. A typical
Read Zero curve is shown in Fig. 4.10. If the input register had been cleared instead, the error counter would read all the bit outputs below the threshold. The read zero curve is important for two reasons: 1) it shows how well the system performs (see Sect. 4.5a Noise Analysis) 2) it is used as a basis for comparison for other data.

d. Write 1's

After the initialization procedure, and the read zero data has been obtained, a write all ones program is written into all addressable bit locations (dummy bit lines remain unselected except in the read mode or initialization procedure). To verify this data all addressable bit locations are then read using the adjustable threshold control and the error counter output. A typical read ones curve is also shown in Fig. 4.10.

The vertical height between the Read Zero and Write Ones curve represents distribution of one outputs as a function of the threshold voltage.

This curve is also plotted in Fig. 4.10 and is obtained by subtracting the raw Write One's
LOW WORD R&W, 52 MA  HIST. -100 MA LOW WORD
HI DIGIT W/ERASE
+36 -33 MA

50%

DIGIT GROUPS 000, 001, 100 101, only.

Fig. 4.10
data from the Read Zero data.

Ideally the Read Zero and Write One curves should be separated by a threshold gap so that no zeroes can be misinterpreted as ones. The slope of the Write one distribution should initially be steep and reach a plateau of 100 percent of the bits tested for a range of threshold voltages. A memory exhibiting this ideal curve could be expected to have wide operating margins (not considering disturb phenonema).

e. Write Zeroes - Erase Ones

After writing all ones and reading their amplitudes the next test is to restore the bits written to the zero state. All active digit lines are first written and then read as a function of threshold voltage. There are three ways to present this data 1) plot the raw data 2) subtract the read zero data from the raw data 3) subtract the raw data from the write one data. All three methods were used in the data given in the Appendix at one time or another. Graphs of 1 or 2 are titled Write Zeroes or Erase Ones to differentiate the data from the Read Zero curves taken after initialization. The third graph is titled
either Writeable-Eraseable Ones or Write Ones - Write Zeroes.

f. Curve Families

Since the best operating point for all of the bits could only be approximated prior to the evaluation, initial data was taken with combinations of digit and word current as another parameter. Usually the word current was fixed and the digit current varied in increments by S7. Later data was taken with a somewhat different setting of the digit currents for each position of S7. Data taken after Jan. was obtained with a different meter measuring threshold voltage. A calibration curve for each meter is given in the Appendix: Evaluation Data.

4.5 Functional Stack Operation

a. Noise Analysis

1. Random Noise

High density in a memory array usually comes at the expense of output signal (power being fixed). At the outset it was realized that a high gain limited bandwidth sense system must be used to achieve a detectable signal. Initial stack evaluation showed on the average a saturated 1 to 0 ratio of 2:1. About 1.2 uv of rms random noise could be expected at the sense preamplifier input. However, the peak value of the noise can exceed the average value many fold, so a safety factor should be applied when the signal
approaches this value.

The noise at the output of the sense amplifier with the word driver disconnected was near 500 mv (p-p). The gain of the sense amplifier-filter combination is nearly 16,000 in the pass band. Dividing the noise output by the gain gave an input of 31 uv.

However, there are two additional tuned amplifier stages ahead of the sense amplifier. Although the cascaded gain could not be accurately measured it was estimated to be near 10. The noise voltage referred to the input of the sense chain would be then on the order of 3 uv (p-p) or 1 uv rms and is then the same as the theoretical value and cannot be significantly reduced except by further bandwidth limitation. If the bandwidth were reduced by a factor of ten then the random noise could be reduced by approximately three which would be significant.

The overall bandwidth of the sense system is 3 MHz. The initial design specification for the sense amplifier called for 2 MHz bandwidth. This had to be modified because the time schedule and resources prohibited either the special order from the vendor or the
alternative of a special design, fabrication, and assembly effort.

The expected signal from a saturated one was expected to be a maximum of 100 uv (p-p) assuming a coupling factor of unity. This is rarely achieved in practice without easy axis flux closure as in a core or plated wire element. The maximum true 1 signal observed during the evaluation was 1.6 volts (p-p) which is 10 uv when converted to the sense line output. A reduction in expected signal to this level is most logically explained by a poor coupling factor. This could be due to an ineffectual keeper and too great a digit line-magnetic film spacing. A better coupling factor or raising the sense frequency are the only practical approaches to increasing the signal at the same bit density.

Since the gain of the sense preamplifiers are not precisely known, a lower limit of 2 might alter the above discussion. This would require the bulk of the random noise at the sense amplifier input to be generated in the previous stages. The 1 uv of input noise would become 2 uv after being amplified by the preamps.
The additional 29 uv would be generated by the preamps. The input for a true 1 signal of 1.6 volts (p-p) would then be 50 uv (p-p). This amount of signal reduction is more easily explainable by a reduced coupling factor and keeper efficiency. However, the answer to obtaining a better 1 to zero ratio here is a lower noise sense gate, preamplifier circuit. In either case the exact gain and noise of the sense system must be determined accurately to determine the direction of effort to increase the 1 signal or decrease the random noise.

2. Positional Noise

Initial evaluation testing showed that after writing all ones a significant number could not be verified. To isolate the problem only one digit group was tested at a time by removing all but the desired sense output cables from the second level sense selection card. On this basis individual groups could be found that performed better than others but none could be observed to come close to
even 80 percent ones. The groups were then split in half in the word address direction. The address counter can be set at any starting address so Wy 1000 Wx 000 was chosen. This was done for all six useable digit groups, 011 and 111 were excluded due to bad lines. Data was first obtained from the upper half word addresses, then all addresses were cycled and the differences noted. In this way data from the near and far end of the digit line could be identified.

Data from digit groups 000, 001, and 010 (on DSB-1—see Fig. 4.3) showed a much larger percentage of the bits writing on word addresses in the first half of the register than in the second half. They also show a read zero curve which breaks at a higher threshold value in the first half compared to the last half. Thus bits written at the far end of the digit lines could be detected better than those at the near end. But bits at the near end had a lower read zero threshold voltage. The bits at the far end of the digit line are nearest the terminated or low voltage end of the lower word line half. Bits at the near end of the digit line are at the high voltage end of the
upper word line half.

Data from digit groups 100, 101 and 110 (on DSB-4) showed a larger percentage of bits writing on word addresses in the upper half of the register than in the lower half. The read zeroes curve in the lower half register broke at a lower value of threshold voltage than that of the upper half. The bits written at far end of the digit line could be detected better than those at the near end. Bits at the near end had a lower read zero threshold voltage. Bits at the far end of the digit lines are nearest the low voltage end of the upper word line half. Bits at the near end of the digit line are at the high voltage end of the word line half. Figure 4.11 shows address locations of the magnetic arrays and overlays in the stack.

The above data shows a definite and regular dependence on position. To determine if it was strictly a noise problem, the common mode word noise was investigated. An amplifier with a gain of 6 and tuned to the word driver frequency of 10.3 MHz was connected to each of three digit lines on DSB-1. Figure 4.12
<table>
<thead>
<tr>
<th>Word Addr. (Wy-Wx)</th>
<th>Overlay</th>
<th>Substrate</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000 - 000</td>
<td>3</td>
<td>P7626-5</td>
</tr>
<tr>
<td>0011 - 111</td>
<td>3</td>
<td>P7632-5</td>
</tr>
<tr>
<td>0100 - 000</td>
<td>4</td>
<td>P7620-4</td>
</tr>
<tr>
<td>0111 - 111</td>
<td></td>
<td>P7618-2</td>
</tr>
<tr>
<td>1000 - 000</td>
<td>1</td>
<td>P7632-2</td>
</tr>
<tr>
<td>1011 - 111</td>
<td>1</td>
<td>P7632-4</td>
</tr>
<tr>
<td>1100 - 000</td>
<td>2</td>
<td>P7626-4</td>
</tr>
<tr>
<td>1111 - 111</td>
<td></td>
<td>P7626-2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>S/D Addr. (Dy)</th>
<th>Overlay</th>
<th>Substrate</th>
</tr>
</thead>
<tbody>
<tr>
<td>111</td>
<td>A</td>
<td>P7626-5</td>
</tr>
<tr>
<td>110</td>
<td>B</td>
<td>P7632-2</td>
</tr>
<tr>
<td>101</td>
<td>F</td>
<td>P7632-5</td>
</tr>
<tr>
<td>100</td>
<td>4</td>
<td>P7632-4</td>
</tr>
<tr>
<td>011</td>
<td>3</td>
<td>P7620-4</td>
</tr>
<tr>
<td>010</td>
<td>6</td>
<td>P7626-4</td>
</tr>
<tr>
<td>001</td>
<td>D</td>
<td>P7618-2</td>
</tr>
<tr>
<td>000</td>
<td>E</td>
<td>P7626-2</td>
</tr>
</tbody>
</table>

Fig. 4.11 Address Locations of Magnetic Arrays and Overlays in the Stack
**.01 v/cm**

**Word Line** 100 **Wx**

<table>
<thead>
<tr>
<th>Wy</th>
<th>Word Group</th>
<th>Digit Line 1</th>
<th>Digit Line 2</th>
<th>Digit Line 3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0000</td>
<td>1.2</td>
<td>.8</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td>0001</td>
<td>1.4</td>
<td>.8</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td>0010</td>
<td>1.2</td>
<td>.8</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td>0011</td>
<td>1.6</td>
<td>1.0</td>
<td>1.4</td>
</tr>
<tr>
<td></td>
<td>0100</td>
<td>1.3</td>
<td>1.0</td>
<td>1.4</td>
</tr>
<tr>
<td></td>
<td>0101</td>
<td>1.4</td>
<td>1.0</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td>0110</td>
<td>1.0</td>
<td>.8</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>0111</td>
<td>1.0</td>
<td>1.1</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td>1000</td>
<td>2.8</td>
<td>.8</td>
<td>4.4</td>
</tr>
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<td>2.8</td>
<td>2.0</td>
<td>4.0</td>
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<td>1010</td>
<td>3.1</td>
<td>2.0</td>
<td>4.0</td>
</tr>
<tr>
<td></td>
<td>1011</td>
<td>3.2</td>
<td>2.3</td>
<td>4.2</td>
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<tr>
<td></td>
<td>1100</td>
<td>2.6</td>
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<tr>
<td></td>
<td>1101</td>
<td>2.9</td>
<td>2.0</td>
<td>4.0</td>
</tr>
<tr>
<td></td>
<td>1110</td>
<td>5.0</td>
<td>2.8</td>
<td>7.2</td>
</tr>
<tr>
<td></td>
<td>1111</td>
<td>3.9</td>
<td>2.8</td>
<td>4.4</td>
</tr>
</tbody>
</table>

**Word Line** 010

|    | 0000       | 1.0          | .8           | 1.2          |
|    | 10         | 1.3          | .8           | 1.2          |
|    | 11         | 1.2          | .8           | 1.2          |
|    | 100        | 1.4          | .9           | 1.2          |
|    | 101        | 1.2          | .9           | 1.2          |
|    | 110        | 1.3          | .9           | 1.2          |
|    | 0111       | 1.0          | .8           | 2.0          |
|    | 1000       | 2.8          | 1.0          | 4.4          |
|    | 10         | 2.8          | 2.0          | 4.0          |
|    | 11         | 3.0          | 2.0          | 4.0          |
|    | 100        | 3.4          | 2.4          | 4.4          |
|    | 101        | 2.8          | 1.8          | 4.0          |
|    | 110        | 3.0          | 1.8          | 4.0          |
|    | 1111       | 4.0          | 2.8          | 4.4          |

**Digit Line 1**  **Digit Line 2**  **Digit Line 3**

<table>
<thead>
<tr>
<th>Spare</th>
<th>Spare</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Next 001</td>
<td>001</td>
<td>011</td>
</tr>
</tbody>
</table>

Fig. 4.12 Word Noise as a Function of Word Address
shows the relative word noise voltages measured (1 unit = 10 mv). There are two trends to this data: 1) noise is greater in the upper half word addresses by a factor of 3 to 4 than in the lower half. 2) Digit line 2 had an intermediate value of noise compared to line 1 and 3 regardless of the word address. The higher word noise occurs at word addresses where a smaller number of bits can be written. As would be expected the higher word noise voltages are observed at the driven end of the word line. The reason for a lower read zero threshold curve for these addresses cannot be explained by this data but may be due to the common mode rejection ratio of the preamp varying with frequency.

The trend of a lower noise voltage at Digit line 2 shows that either the word current distribution is not uniform throughout this half of the word line or the word line impedance is not uniform. The time schedule prevented this analysis from being pursued further than making impedance measurements of the word and digit line with an ac bridge and a TDR (time domain reflectometer).
3. Intersection Noise

During initial phases of evaluation testing in the BYTE mode, some byte addresses were observed to appear to hold complement data when actually all addresses had been written with the same data. This could be explained by a dummy location having changed state at the address in question. However, the effect was also observed when all zeroes were written. Since all bits do not have exactly the same read zero output (due to sense-gate terminating impedance variation), the complement pattern could still be observed in some neighboring word lines. The balance between the inputs of the differential sense preamp depends on both the amplitude and phase at the terminals. This balance could be upset by the digit lines and dummy lines shifting positions relative to the magnetic film in a local area due to assembly problems (dust, adhesive thickness variation, etc.).

During noise reduction experiments with the sense-digit selector (hybrid) circuit, the data could be changed at a normally good position. This was done by varying the impedance at the dummy or active differential...
input terminals on the circuit package. Thus it was concluded that these local areas represented a noise variation dependent on the word line-digit line intersect spacing. This effect is commonly called the cross-point capacitance problem.

4. System Noise

The most common type of system noise not previously discussed are due to ground current loops. Operation of a memory stack with bit outputs measured in microvolts requires a minimum of ground loop currents to be successful.

The system noise is most easily checked by initializing and reading all zeroes at various threshold levels. Comparison of the read zero curves obtained in this manner will show that they are shifted in position and have different slopes. Much of this change is due to changes in the grounding paths of the stack components when in the unfolded position. For this reason read zero data was taken just prior to folding the memory stack for delivery and also immediately after installation in the memory unit. This was not done previously since it
was feared that too much flexure of the word and digit overlays would cause line fractures.

Other contributions to a shift in the read zero curve are (1) change in sense comparator reference voltage, (2) change of meter M1 (the first one malfunctioned halfway through evaluation requiring a temporary substitute until a replacement was procured) and (3) too small or large a strobe delay or too great a strobe width. The problem involving the strobe delay is related to the recovery time of the envelope detector. Selection noise at the input of the sense amplifier drives the envelope detector near saturation resulting in a recovery time problem. For this reason a 20 usec cycle time was not achieved. A redesign of the detector could permit operation at 2-20 usec cycle time.

Another source of noise noticeable at cycle times faster than 20 usec is the induced noise in the sense loop caused by logic switching. The way to eliminate this problem is to change the logic circuit layout, and reducing the number of timing pulses traveling to and from the front panel controls. This approach was impractical in the feasibility model.
c. Read Zeroes, Write Ones and Erase Ones Tests

1. Word and Digit Current

Initial settings of word and digit currents were determined from the single bit data of 4.9 and from past experience during array testing. Early tests were conducted with word currents of 52, 56, or 64 mA (p-p) and digit currents of +36 -33, +30 -25, and +22 -20 mA. Later the +36 mA was increased to +40 mA in an attempt to write more bits.

2. Noise Reduction

Results obtained when all the sense groups were connected were disappointing. Suspecting a noise problem, each digit group was investigated separately and on some, noise reduction circuits were installed. The best noise reduction was obtained when an inductance (which resonated with 55 pf ± 10 pf at the 20.6 MHz sense frequency) was connected between ground and the active differential preamp input. A dc isolation capacitor (820 pf) was used in series with the inductor to prevent shunting of the digit current during the write operation.
3. Individual Group Testing

At this point it was decided to test each digit group separately to the best operating region of word and digit current. The definition of "best" for these tests was the largest number of writeable eraseable bits. In all, 9 combinations of word and digit current were tried for each digit group except 011 and 111. A typical set of curves for Dy 000 is shown in Figure 4.13 for lower half word addresses and Fig. 4.14 for upper half word addresses. These data were taken at the same time with a low word current (52 mA) and a high digit current (+35 -30 mA). Other data in the set for the 8 other combinations currents are in the appendix. The use of low word and high digit current represented the best of the 9 combinations in terms of maximum number of writeable eraseable bits.

It was during the individual group testing that the positional dependence of the data was first noticed.

When the other 5 digit groups were checked each showed a similar preference for a low value of word current and a medium or high
LO WORD R&W
HI DIGIT W & ERASE
HIST. -100 ma
LOWORD

WORD
0111 - DOWN

BIT'S ABOVE VT

RD 0's

WR 1's

ERASE 1's

VT

Fig. 4.12

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value of digit current. Single addresses were read at medium and high values of word current after being initialized or written to the one state with a low word current and a digit current. The scope connected to the sense amp output showed evidence of word disturbs during continuous reads by their outputs suddenly increasing, decreasing, or become unstable. Not all addresses behaved this way but enough did so that word currents higher than 55 mA were avoided.

This read disturb problem also occurred with some dummy bits before the initialization circuits were installed. At that time, the only way the dummy could be written was with a word current and the internal digit driver. The digit driver could not deliver enough current to insure that the dummy was in a stable state so it tended to read disturb.

The "best" individual group data was obtained on Dy 001 where 74% of the bits wrote and erased with a word current of 52 mA and a digit current of +40 -30 mA. When the word current was reduced to 45 mA, 59% of the bits wrote and erased. These data are shown in Figs. 4.15.
LO WORD ~50+ ms R&W
HI DIGIT W 8 ERASE
+40-30 ms

--- WRIs - WROs

--- RD O's

Fig. 4.15
and 4.16 respectively.

3. Testing of All Useable Groups

All of the useable digit groups were tested first as one large group and then individually prior to folding and installing the stack in the memory unit. In the data shown for Fig. 4.17, 40.5% of the addressed bits were writable and erasable with a word current of 52mA and a digit current of +36 -33 mA.

Later another set of data was taken on the individual groups with a word current of 45 mA and a digit current of +40 -30 mA. This data given in Figs. 4.18a through 4.18d shows that Dy 010 gave the poorest performance with only 27% of the bits writing and erasing. Groups 100, 101, and 110 showed 47% bits writing and erasing while groups 000 and 001 showing 62.5% of the bits writing and erasing. Overall a maximum 40.5% of all the bits wrote and erased with these drive currents.

Using the same values of word and digit current as in the preceeding test the same groups were retested after folding and installation of the stack in the memory. This data is shown in Figs. 4.19a through 4.19f. All of the
LOW WORD ~ 45 mA READ
HI DIGIT W & ERASE
+40 - 30 mA

DIGIT GROUP 001

-- WR1'S - WRO'S

RD0'S

WR1'S

Fig. 4.16
LOWORD READ HIST., 100 mA LOWORD,
HI DIGIT W/ ERASE
+36 - 33 mA

40.5%
ALL DIGIT GROUPS EXCEPT 011 & 111

Fig. 4.17

DIGIT GROUPS
011 & 111
DISCONNECTED

0 10 20 30 40
0 10 20 30 40

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SPERRY RAND
Fig. 4.18a
Fig. 4.18b
Dig. 4.18d
Fig. 4.19a

LOW WORD RAW
HIGH DIGIT WE ERASE DIGIT GROUP 000

FOLDED STACK

RDO's

WRI's

WRO's

BITS ABOVE V_T

V_T

40 50 60 70 80
Fig. 4.19b

READ "0"S

WRITE "1"S

WR "0"S
LO WORD
HI DIGIT
READ "0"S
WR "1"S

FOLDED STACK

Fig. 4.19c
LO WORD R&W  HIST.-110 LC WORD
HI DIGIT W&ERASE  DIGIT GROUP 100

FOLDED STACK

READ 0's

Fig. 4.19d

BITS ABOVE Vt

40 50 60 70 80

VT
LO WORD RAW
HI DIGIT WRITE
HIST.-NO LO WORD
DIGIT GROUP 101

FOLDED STACK

Fig. 4.19e

RDO's

WR's

WRO's

BITS ABOVE V_T

V_T

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Fig. 4.19f

The graph shows the distribution of data points with the following axes:
- Vertical axis: Bits Above VT
- Horizontal axis: VT

The graph includes the following areas:
- RD 0's
- WR 1's
- WRO 0's

Legend:
- LO WORD
- R & W
- HIST.
- NO 20 WORD
- 1/1 DIGIT
- W & ERASE
- 1/10 DIGIT GROUP

The graph is labeled "Folded Stack."
groups except 010 showed a decrease in the number of ones which could be erased. Group 101 showed the largest decrease in this regard. Overall a maximum of 31% of the bits wrote and erased after the stack was installed in the memory unit. There are many possible explanations for the change in data before and after folding with the most plausible one being noise introduction via ground current loops. If this were the case, the read zero curves should have shifted in terms of threshold voltage or changed shape showing a different distribution of zero amplitudes. Comparing data for 000, 001, 100, and 101, Fig. 4.20a after folding with 4.20b, the same groups before folding do not show a large change in shape or offset. The curve for the unfolded stack is steeper between 44 and 48 on the VT scale than the curve in the folded condition. This should not be a contributing factor since the write one distributions have not reached their peak at this point.

Other explanations for the change in performance could be a change in radiated noise or a change in the earth's magnetic field due to a shift in centerboard positions. All tests were carried out in the same room within a radius of
LO WORD READ AS mG

FOLDED STACK

READ ZERO CURVES
6 OF 8 DIGIT GROUPS

Fig. 4.20a
LO WORD R&W
HI DIGIT WE ERASE
HIST. 100, LO WORD

DIGIT GROUPS 000, 001, 100, 101

Fig. 4.20b
1 meter, the centerboards were always parallel to the floor so a gross change in earth's magnetic field is unlikely. Either radiated or ground loop noise remain the most likely choices barring an undetected malfunction.
4. Disturb Testing

Previous write one-erase one data showed that to obtain the maximum number of responsive bits a low value of word current and a high value of digit current should be used. At this point, the write digit current was increased from 36 to 40 mA with the restore current set to 30 mA. A number of groups were rechecked with these currents and no substantial increase in responsive bits was observed. At this point it was decided that a further increase of digit current would gain nothing so disturb testing was begun.

In the disturb test an alternate pattern of 1's is written so that half of the memory locations are written as a checkerboard. This pattern was written after initialization and zeroes were read. The alternate one pattern was read and the spaces in the checkerboard were disturbed once with zeroes. The ones were again read. The typical response for any of the groups when written with a low word and high digit current is shown in Fig. 4.21. The trend is clear, the number of bits which were ones at any threshold value have been cut in half; either the bits disturbed to 50% output or half the bits disturbed to 0% output.
A check was made to determine whether the bits were being influenced by neighboring word or digit lines by writing some patterns manually in a 64 bit memory area on one substrate. The disturb mechanism was from the adjacent bit line rather than the word line. The digit currents were subsequently lowered and the number of bits which could be written to the one state were drastically reduced. At this point, time remaining for further detailed evaluations was limited so only general observations can be made.

An increase of digit current is required to write the maximum number of bits. At this value a large number of bits disturb due to the combination self word current and neighbor digit current. Reducing the digit current means a reduction in the number of bits written or those which can be read. The disturb problem is eased somewhat by reducing the digit current. Increasing the word current to write a maximum number of bits is inadvisable because of the read disturb problem. The following conclusions can be made if noise can for a moment be neglected, 1) The digit field spreads too far influencing the neighbor bits, 2) Either current variations, spacing variations, or magnetic variations prevent
WRITE "1" EO-05  FOLDED STACK
DISTURB W/O'S EE-00

READ 0's

Fig. 4.21
all bits from writing at the same value and, 3) On
the system level margins do not exist. Because
noise cannot be neglected these conclusions must
be qualified.
5.0 Conclusions

The mass memory feasibility model carried the mirror technology from the array level to the stack level. It demonstrated feasibility of the hybrid selection electronics and it demonstrated the low cost achievability for the mirror memory stacks. Problems were encountered with noise and disturb (as often occurs with the first attempt to build an operating model with a new technology). Solutions for these problems have been formulated and with commitment of limited additional resources, considerable improvement of memory operation can be achieved.

The hybrid circuit development was extremely successful, all the circuits were fabricated on schedule with very high yields. Only two circuit failures occurred during the eight weeks of system evaluations. One of these circuits could be moved and analyzed to determine the failure mode. In addition to the good yields, it appears that the electronic circuit density can be increased by a factor of two.

One of the most critical tasks was the fabrication of .003" (.0076 cm) wide lines on .006" (.015 cm) centers with a length of 44" (111.8 cm). A yield of approximately 50% was obtained during the fabrication of these lines; however, some problems occurred during the stack assembly and testing. During this time 10% of the lines developed opens and shorts. Causes of failure of these lines should be investigated.
The success of the read/write testing was to a great extent masked by system noise which appears to be due to variations in capacitance between a) the word line and the active digit line and b) the word line and the dummy digit line (cross point capacitance). The best octant of the memory has approximately 75% good bits in the read/write mode of testing. It appears that this figure would be substantially increased if the signal to noise ratio were improved. The signal could be increased by increasing the drive frequency and by interchanging the position of the word and digit lines (move the digit line to the position close to the film). The present position of the digit line was selected on a small scale test where the system noise was not an important factor.

There are two types of noise in the stack which appear to be related to the cross point capacitance problem. There is a position orientated noise in two mirror image positions where the word line voltage is the highest. Since the cross point capacitance noise is directly proportional to the voltage between the word line and the digit lines, one would expect that the cross point capacitance noise would be largest in these areas. This could be verified by interchanging the position of the word drive boards to see if the high noise areas reversed.
There is also a random bit or interset noise which appears to be related to the cross point capacitance. Verification involves sectioning the stack to examine the dimensional tolerances of the distance between lines. The overall noise could be decreased by reducing the bandwidth of the sense circuitry.

The checkboard pattern testing showed that there is an adjacent bit disturb problem. The following techniques could be employed to decrease this effect: turn the word current off prior to the termination of the digit current, increase the thickness of the ground plane, increase the digit line spacing and use a metal substrate.

Since there are several technical problems that were defined during the evaluation portion of this contract, it is proposed (Section 6.0) that a new set of centerboards be constructed and tested to verify the proposed solutions in a modified design.
6.0 Recommendations

It is recommended that the results of this first iteration to build a mirror memory stack be applied to the design of new centerboard assemblies. These new assemblies would be fabricated in such a manner that they could replace the old assemblies in the memory unit for testing and evaluating the new design. Summarized below are the proposed tasks for the effort.

1. Reposition the word driver boards to verify the cause of the stack orientated noise.

2. Section the magnetic position of the stack to determine the dimensional tolerances.

3. Perform small scale element tests to determine the best approach or approaches to reduce the disturb and increase the signal.

4. Construct new centerboard assemblies with the most promising approach or approaches as defined as a result of part 3.

5. Electronics changes
   a. Terminate the word current prior to the termination of the digit current.
   b. Decrease the sense loop bandwidth.
   c. Increase the word drive frequency.

6. Replace the centerboards in the feasibility model and evaluate the new centerboard design.
7.0 Appendix

7.1 Original Data
NO WRITING DETECTABLE