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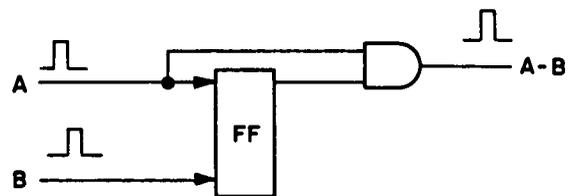
## Frequency Control Circuit for All-Digital Phase-Lock Loops

A phase-lock loop implemented entirely with digital circuits (see Note 1) references all its operations to a fixed high-frequency service clock (crystal oscillator) operating at the highest speed which the digital circuits permit. The general principle of the frequency correction mechanism involves deletion of every  $n$ th pulse in the pulse train from the oscillator to an output divider for the steady state, and  $(n-m)$  and  $(n+m)$ , respectively, for correction in either direction; in this way, the bump-size is kept as small as possible and of the same general size for correction in either direction. The output from a simple counter/divider which can be programmed to divide by one of a set of integers controls a pulse-delete gate resulting in the instantaneous frequency of the reference signal:  $f_n = (n-1/n)f_0$ , where  $f_0$  corresponds to the uncontrolled frequency of the reference signal. A change of  $n$  to the next larger or next smaller integer does not result in the same frequency change, i.e., for small  $n$ 's the changes are large and for large  $n$ 's the changes are small. For  $(n < 10)$  the frequency changes are too large and too nonlinear to be usable in a control system.

A wide-range control circuit has been developed which provides essentially linear control of the frequency of the reference signal and extends the acquisition range from 10 to 50 percent. It requires only two counters of the simplest possible type in combination with a control circuit consisting only of a flip-flop and a gate.

Deleting one pulse every  $n$ th pulse requires that  $n$  be an integer. For smallest possible control steps,  $n$  must then include all possible integers  $\geq 2$ . The implementation of  $f_n = (n-1/n)f_0$  [designated B] con-

tains a programmable counter/divider which can be programmed to divide by 2, 3, 4, 5, . . .  $n$ . The output of this counter controls a pulse-delete gate in the pulse train from the oscillator to the output divider.



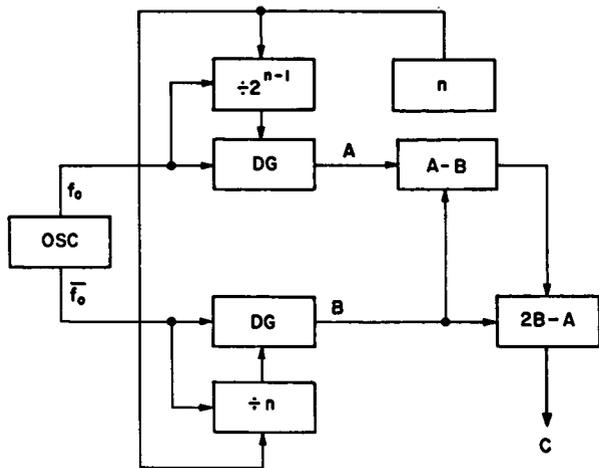
 Clock

Another simple counter is a binary ripple counter which divides by  $2^0, 2^1, 2^2, 2^3, 2^4, \dots, 2^n$ . Selection of any one stage of such a counter for control of a pulse-delete gate results in function  $f_n = [2^n - 1]/2^n f_0$ , designated A. This function is by itself essentially unusable as a control function.

If, however, the difference  $A-B$  is subtracted from B, the result becomes a desirable function. For control purposes, this function is essentially linear and usable for all  $n$ 's ( $2 \leq n$ ), resulting in a 50-percent control range. Both the  $A-B$  and  $B-(A-B)$  functions are implemented easily, each requiring only a flip-flop and a gate.

As indicated in the functional block diagram, the inputs to the divide-by- $n$  divider and the divider which divides by  $2^{n-1}$  are derived from the true and complement outputs from the oscillator, respectively. This will assure that A and B are of different phase and that for  $n=2$ ,  $A-B=0$ . It is apparent that if the same phase were used for both A and B,  $A-B$  would be ambiguous.

(continued overleaf)



The A-B and 2B-A circuits are identical and very simple, as shown in the schematic diagram. A flip-flop is set and reset on A pulses and B pulses, respectively. If two B pulses occur within the period between two A pulses, an output pulse is registered.

For the divide-by-n counter/divider, a number of counter flip-flops are set to the binary equivalent of n. The set operation takes place over set gates, and the flip-flops are connected to count down. The output of an all-zero gate will enable the set gates and again

set the flip-flops to n. Setting takes place from a zero condition, requiring only a single term for each flip-flop. The counter/divider which divides by  $2^n$  is in itself trivial, but with n being the selection number and available in binary notation, a base-two-to-base-ten conversion network is required.

**Notes:**

1. The all-digital phase-lock loop is described in NASA Tech Brief B73-10350 .
2. Requests for further information may be directed to:

Technology Utilization Officer  
 NASA Pasadena Office  
 4800 Oak Grove Drive  
 Pasadena, California 91103  
 Reference: TSP 73-10351

**Patent status:**

NASA has decided not to apply for a patent.

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