

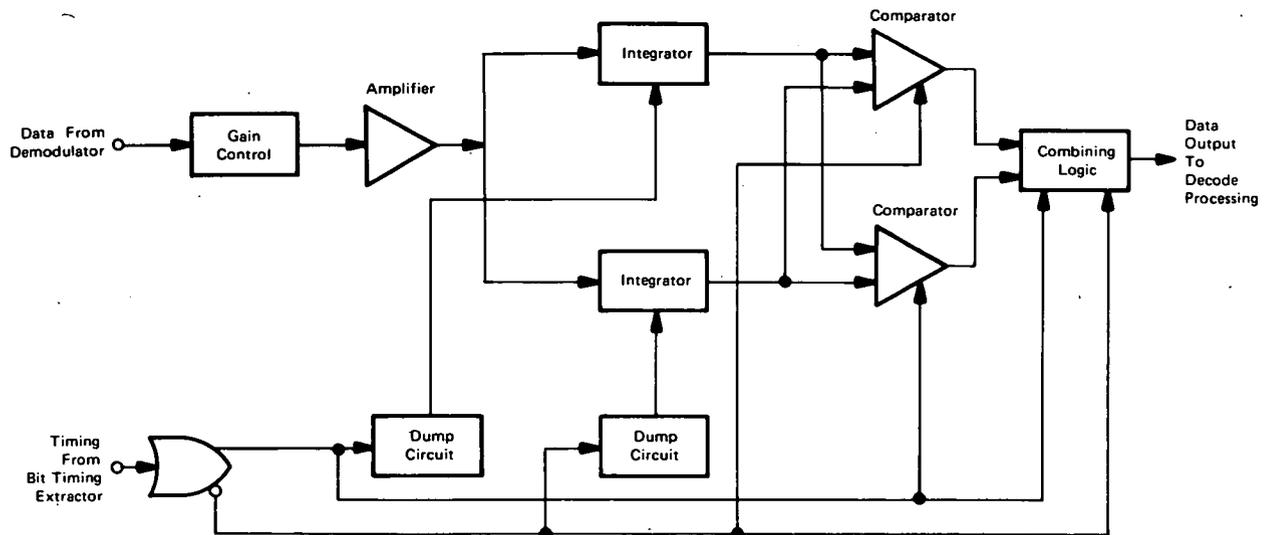
NASA TECH BRIEF

Lyndon B. Johnson Space Center



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Data-Matched Filter



Functional Block Diagram of Integrate-Sample-and-Dump Matched Data Filter

A new data-matched filter includes an improved integrator section that is linear from 1 kBPS to 30 MBPS. Incoming data and noise are normalized and amplified before being fed into an integrate-sample-and-dump circuit. A block diagram of the filter is illustrated.

After amplification and normalization, the incoming data bits are fed, alternately, to a pair of integrators. While one integrator is operating, the content of the other is on hold, sample, and dump. A clock derived in a bit-timing extractor times and controls the integrators. The frequency of the clock is one-half the data rate.

The integrated signals are sent to one of two, high-speed latching comparators where the received bits are identified as "zeros" or "ones". Each comparator receives a complementary strobe signal from the timing signal. The timing is arranged so that each comparator state is strobed just after the corresponding integration, and just before dumping.

The two comparator outputs are sampled sequentially to provide a single reconstituted data stream that corresponds to the original data sequence. This is the output to decoding and other processing.

Patent status:

Title to this invention has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457 (f)], to the RCA Corp., Camden, New Jersey 08102.

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