

Volume IV

Final
Report

September 1972

Special Long-Life
Assurance Studies

**Long-Life Assurance
Study for Manned
Spacecraft Long-Life
Hardware**

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SPECIAL LONG-LIFE
ASSURANCE STUDIES

LONG-LIFE ASSURANCE STUDY
FOR MANNED SPACECRAFT
LONG-LIFE HARDWARE

Approved

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FOREWORD

This document is Volume IV of a five-volume final report prepared by Martin Marietta Corporation, Denver Division for the National Aeronautics and Space Administration, Manned Spacecraft Center (NASA-MSC) under Contract NAS9-12359, *Long-Life Assurance Study for Manned Spacecraft Long-Life Hardware*. This study was performed with J. B. Fox, Manned Spacecraft Center, as Technical Monitor and R. W. Burrows, Martin Marietta, as Program Manager. Acknowledgment is made to the individual contributors identified in each volume and to R. A. Homan and J. C. DuBuisson, Task Leaders for the electrical/electronic and mechanical areas, respectively.

The five volumes submitted in compliance with Data Requirements List T-732, Line Item 4, are as follows:

- Volume I - Summary of Long-Life Assurance Guidelines;
- Volume II - Long-Life Assurance Studies of EEE Parts and Packaging;
- Volume III - Long-Life Assurance Studies of Components;
- Volume IV - Special Long-Life Assurance Studies;
- Volume V - Long-Life Assurance Test and Study Recommendations.

CONTENTS

	<u>Page</u>
I. INTRODUCTION	I-1 and I-2
II. A STUDY OF TEMPERATURE CYCLING AS EMPLOYED IN THE PRODUCTION ACCEPTANCE TESTING OF ELECTRONIC ASSEM BLIES ("BLACK BOXES")	II-1 thru II-68
III. A STUDY OF ACCELERATED TESTING TECHNIQUES	III-1 thru III-101
IV. A STUDY OF ELECTRONIC PART SCREENING TECHNIQUES	IV-1 thru IV-65
V. INDUSTRY SURVEY OF ELECTRONIC PART DERATING PRACTICES	V-1 thru V-40
VI. VIBRATION LIFE EXTENSION OF PRINTED CIRCUIT BOARD ASSEMBLIES	VI-1 thru VI-17
VII. TOLERANCE FUNNELING AND TEST REQUIREMENTS STUDY	VII-1 thru VII-10

I. INTRODUCTION

CONTENTS

	<u>Page</u>
I. INTRODUCTION	I-1 and I-2

I. INTRODUCTION

This volume contains the special studies performed under the *Long Life Assurance Study for Manned Spacecraft Long Life Hardware*. While Volumes II and III contain detailed studies of specific types of parts and components, this volume contains studies applicable to many types of hardware. These special studies are:

- 1) A Study of Temperature Cycling as Employed in the Production Acceptance Testing of Electronic Assemblies ("Black Boxes").
- 2) A Study of Accelerated Testing Techniques.
- 3) A Study of Electronic Part Screening Techniques.
- 4) Industry Survey of Electronic Part Derating Practices.
- 5) Vibration Life Extension of Printed Circuit Board Assemblies.
- 6) Tolerance Funnelling and Test Requirements Study.

The study on temperature cycling of electronic assemblies encompasses a comprehensive industry survey and thorough analysis of industry practices and experiences in this technique. As a result of analyzing the accumulated data, a specific thermal cycling policy for long-life missions is recommended.

The study of accelerated testing techniques documents the state-of-the-art, the applications, and the limitations of both qualitative and quantitative approaches to materials, solder joints, electronic parts, electronic assemblies, mechanical/electromechanical hardware, batteries, bearings, valves, and transducers. Mathematical models and statistical requirements are presented for the use of step stress, constant stress, and progressive stress accelerated tests using the cumulative damage criterion, the inverse power rule, and the Arrhenius model. In addition, weak link testing, enhanced defect testing, and dynamic mission equivalent testing is discussed.

The study of electronic part screening techniques is addressed to unconventional screening approaches. "Zero-time" screens such as current-noise analysis, third harmonic analysis, and linear discriminant analysis are reviewed. Other unconventional approaches included are the optimization of stress screens, parameter drift screening, short-time overload testing, neutron radiography, monitored shock and vibration, laser scanning, and automatic inspection techniques.

The electronic part derating survey includes a summary of derating practices used by 12 aerospace agencies/programs. Recommended long-life mission derating guidelines representing a composite of these practices is derived from the summary, in addition, design practices guideline, to be utilized in conjunction with derating practices, are included.

The printed circuit board vibration life extension study includes performance of a test program on printed circuit boards to determine the capability of such items to withstand long periods of vibration. It also investigates the feasibility of reducing vibration time during qualification testing by increasing the vibration level. A summary of the test results, recommendations for accelerated test approaches, and areas requiring further development and evaluation, are identified.

The tolerance funneling study includes a brief review of the concept. Suggested guidelines for tolerance funneling of module, component, and subsystem test limits are provided, together with a discussion of their derivation.

II. A STUDY OF TEMPERATURE CYCLING AS EMPLOYED IN
THE PRODUCTION ACCEPTANCE TESTING OF ELECTRONIC
ASSEMBLIES

by R. W. Burrows

CONTENTS

	<u>Page</u>
II. A STUDY OF TEMPERATURE CYCLING AS EMPLOYED IN THE PRODUCTION ACCEPTANCE TESTING OF ELECTRONIC ASSEMBLIES ("BLACK BOXES")	II-1
A. INTRODUCTION	II-1
B. STUDY OBJECTIVE	II-2
C. CONCLUSIONS	II-3
D. RECOMMENDATIONS	II-6
E. DISCUSSION	II-7
1. Purpose of Temperature Cycling	II-7
2. Summary Table of Industry Survey Results	II-7
3. Data Analyses	II-7
4. Failure Criteria	II-13
5. Risks Associated with Repairs	II-17
6. Is Temperature Cycling Degrading?	II-21
7. Remarks in AGREE Testing	II-27
8. Remarks in Rate of Temperature Change	II-28
9. Relationship between Multiple Temperature Cycling and Thermal Vacuum Testing	II-30
10. Cost Effectiveness of Temperature Cycling	II-32
F. INDUSTRY SURVEY	II-34
1. Collins Radio Co.	II-34
2. General Electric Company - Aerospace Electronics	II-38
3. Lockheed Missile and Space Co.	II-38
4. Boeing Company - Aerospace Group	II-48
5. Hughes Aircraft Company	II-50
6. Aerospace Corporation	II-50
7. Decca Radar, Ltd.	II-51
8. Motorola	II-53
9. Honeywell, Incorporated	II-54
10. Radiation Incorporated	II-55
11. TRW Systems	II-59
12. Goddard Space Flight Center	II-59
13. Hewlett-Packard Co.	II-60
14. Bendix Corporation	II-60
15. Westinghouse - Aerospace Electrical Systems	II-61
16. Martin Marietta Aerospace, Denver Division	II-61
17. Barnes Engineering Co, Defense and Space Division	II-61
18. Delco (A. C.) Electronics	II-61
19. Raytheon - Equipment Division	II-62
20. Sandia Corporation	II-62

21.	RCA - Astro-Electronics Division	II-62
22.	Marshall Space Flight Center	II-63
23.	Grumman Aircraft Engineering Co.	II-63
24.	Texas Instruments	II-64
25.	JPL	II-65
26.	Supplier A	II-65
27.	Supplier B	II-66
G.	LIST OF COMPANIES/AGENCIES/PERSONNEL SURVEYED	II-66
H.	REFERENCES	II-68

Figure

1	Apollo Baseline Temperature Cycle	II-1
2	Summary of Industry Survey Data Indicating Six to Ten Cycles Are Required for Elimination of Incident De- fects	II-12
3	Summary of Industry Rate Data	II-14
4	Expected Failures during Ten Temperature Cycles as a Function of Equipment Complexity	II-15
5	Generalized Temperature Cycling Failure Rate Curves as a Function of Equipment Complexity	II-16
6	Test Data Showing No Increase in Failure Rate with as Many as 250 to 300 Temperature Cycles	II-23
7	Agree Environmental Profile	II-28
8	Comparison of Temperature Change Rates in Various Types of Temperature Testing	II-29
9	Hypothetical Electronic Assembly Showing Temperature Stress on Bonds	II-30
10	Relationship of Support Costs to MTBF	II-32
11	Collins Radio Company Temperature Cycling vs Failure Rate Data	II-36
12	Relationship of Rate of Infant Mortality Failure to Agree-3 Test Time	II-37
13	Data from Figure 12, Replotted	II-37
14	General Electric LRU Temperature Cycle Performance	II-39
15	General Electric LRU Temperature Cycle Failure Distribution	II-40
16	Temperature Cycling vs Failure Yield--Unit Types 1 to 7	II-45
17	Temperature Cycling vs Failure Yield--Unit Type 9	II-45
18	Temperature Cycling vs Failure Yield--Unit Type 8	II-45
19	Temperature Cycling vs Failure Yield--Combination of Unit Types 8 and 9	II-45
20	Temperature Cycles vs Failure Yield--All Units 1-9	II-46
21	Comparison of Failure Rates by Unit Complexity	II-47
22	Boeing Company - Temperature Cycling vs Failure Yield	II-49

23	Aerospace Corporation - Temperature Cycling vs Failure Data on Twenty-One Transponders	II-51
24	Typical Data from Decca Radar Limited, Illustrating Knee at Four to Six Temperature Cycles	II-52
25	Radiation Incorporated - Temperature Cycling vs Reliability Improvement	II-58

Table

1	Proposed Guidelines for Temperature Cycling Acceptance Testing of Electronics Hardware	II-6
2	Distribution of Temperature Cycling Failures between Marginal Design, Poor Workmanship and Defective Parts . .	II-8
3	Typical Examples of Defects Screened Out by Temperature Cycling	II-9
4	Summary of Recommended Temperature Cycles from Industry Survey	II-10
5	Companies Supplying Failure Rate vs Temperature Cycle Data	II-11
6	Estimates of the Number of Additional Temperature Cycles Required to Maintain an Approximately Constant Risk of a Post-Acceptance Test Failure	II-19
7	Guidelines for Additional Temperature Cycles to be Conducted in the Event of a Failure	II-20
8	Burn-In and Demonstration Test Data	II-24
9	Lockheed Missile and Space Company Temperature Cycling vs Failure Yield	II-42
10	Lockheed Missile and Space Company Temperature Cycling vs Failure Yield	II-43
11	Lockheed Missile and Space Company Temperature Cycling vs Failure Yield	II-44
12	Motorola Temperature Cycling vs Failure Data	II-54

II. A STUDY OF TEMPERATURE CYCLING AS EMPLOYED IN THE PRODUCTION ACCEPTANCE TESTING OF ELECTRONIC ASSEMBLIES ("BLACK BOXES")

A. INTRODUCTION

Temperature cycling, as an acceptance test of production assemblies, is widely used as a test screen for the detection of workmanship and parts defects at the "black box" level. It also reveals design deficiencies when it is not extensively employed during development and qualification testing. It is usually used in conjunction with vibration. It is combined with vacuum exposure when appropriate, and it is particularly applicable to electronic equipment.

On the Apollo Program the temperature cycle shown in Figure 1 was established as a baseline. One constraint on the derivation of this baseline was that a test was desired which would be effective but would not precipitate gross requalification testing of Apollo hardware (qualification testing had been largely completed when the Apollo acceptance test program was upgraded).

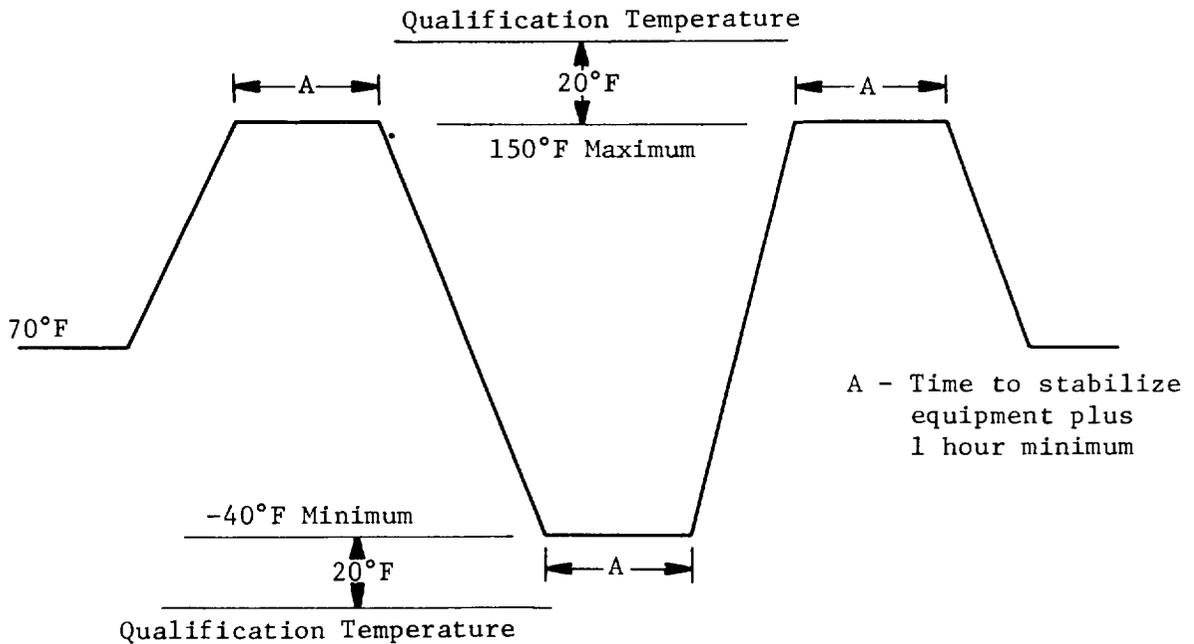


Figure 1 Apollo Baseline Temperature Cycle

B. STUDY OBJECTIVE

The objective of this study is to review and analyze current temperature cycling practices to determine if the Apollo baseline test should be modified for future manned spacecraft programs.

C. CONCLUSIONS

1. A survey of 26 companies/agencies shows that the preponderance of opinion is that more than one thermal cycle is required.
2. Test data from seven companies shows that 6 to 10 cycles are required for the elimination of the incipient defects. Six cycles appear adequate for black boxes of about 2000 parts, while 10 cycles are recommended for equipment containing 4000 or more parts.
3. The following companies subscribe to 6 to 10 cycles: Martin Marietta Aerospace, General Electric, TRW, Lockheed, Collins Radio, Radiation Incorporated, and Aerospace Corporation.
4. Hughes Aircraft Company has developed mathematical models to predict how many cycles are required to achieve a specified reliability depending on the previous amount of screening, the quality of parts used, and the exact thermal conditions and profile for the parts being screened. Many more than 10 cycles are sometimes required, per their model.
5. When unscreened parts are used and temperature cycling of assemblies is employed as the main production screen, more than 10 cycles may be required. Programs of 16 to 25 cycles have been used.
6. Temperature ranges of -65°F to 131°F are the temperatures most commonly used. Most parts will withstand temperature cycling with power off through a temperature range of -65°F to 230°F . Heat rise with power on under test cooling conditions should be calculated to limit the chamber temperature to a maximum safe value. The maximum safe range of component temperature and the fastest time rate of change of hardware temperatures will provide the best screening.
7. The rate of temperature change of the individual electronic parts depends on the chambers used, the size and mass of the hardware, and whether the equipment covers are taken off. In general, the rate of change of internal parts should fall within 1°F per minute and 40°F per minute, with the higher rates providing the best screening. A temperature range between 160°F and 225°F is recommended.

8. Temperature cycling with good parts and packaging techniques is not degrading even with several hundred cycles. However, the packaging design must be compatible with the temperature cycling program or the acceptance test yield will be reduced (to zero in some special cases). This compatibility is established by temperature cycling the pre-production hardware.
9. The equipment should be closely monitored during the operating portions of the cycle. It is desirable to turn off the equipment during chamber cool-down or self-generated heat will prevent the internal parts from reaching the desired low temperature.
10. When multiple temperature cycling is used as an acceptance test, it is standard practice to allow repairs without requiring a repeat of the entire test. Some programs have required no failure free cycles, some have required the two final cycles to be failure free, and one program (involving very simple hardware) required 20 consecutive failure free cycles. It is recommended that one final failure free cycle be required, together with criteria for extending the number of temperature cycles as a function of the difficulty and magnitude of the repair.
11. Implementing temperature cycling is most compatible with PC board construction and least compatible with large, complex, potted cordwood modules where failure means scrapping the entire module.
12. The concept of augmenting the black box temperature cycling with additional cycling at the PC board level should be considered. Hughes Aircraft, on one program, "stores" their assembled PC boards in a temperature chamber for one week during which time 158 temperature cycles are accrued. The boards are not powered or monitored. This comprises a very cost-effective approach to reliability.
13. An approximation of the types of failures detected in mature hardware by temperature cycling is:

Design Marginalities - 5%
Workmanship Errors - 33%
Faulty Parts - 62%

14. Much of the data in this report is derived from programs using AGREE testing per MIL-STD-781B. The AGREE cycle combines temperature ramps, temperature soaks, and low level (2g) vibration. The concensus is that the temperature soaks and the low level vibration play a very minor role and, therefore, the AGREE technique is essentially equivalent to a temperature cycling test, with the screening strength of the test dependent on the temperature range, the temperature rate of change, and the number of cycles.

D. RECOMMENDATIONS

It is recommended that future programs adopt an environmental test acceptance program for electronic black boxes consisting of the Apollo proven 6g rms random vibration, minimum; thermal-vacuum testing when applicable; and a temperature cycling program, in accordance with Table 1.

Table 1 Proposed Guidelines for Temperature Cycling Acceptance Testing of Electronic Hardware

<u>Type of Equipment</u>	<u>No. of Temperature Cycles</u>
Simple (100 electronic parts)	1
Moderately complex (500 electronic parts)	3
Complex (2000 electronic parts)	6
Very complex (4000 electronic parts)	10

Temperature Range

The suggested range is -65°F to 131°F, or as a minimum, a temperature range of at least 160°F is recommended.

Temperature Rate of Change

The rate of change of internal parts should fall within 1°F and 40°F per minute. The higher rates provide the best screening.

Temperature Soak Times

The next temperature ramp may be started when the internal parts have stabilized within 5°F of the specified temperature and the functional checks have been completed.

Equipment Operation

Equipment should be energized and operated during temperature cycling, except the equipment should be turned off during chamber cool-down to permit internal parts to become cold.

Equipment Monitoring

While it is desirable to continuously monitor the equipment during the temperature cycling, cost considerations may dictate otherwise. In such cases, periodic checks plus close monitoring of the final cycles is appropriate.

Failure Criteria

The last cycle shall be failure free. Each repair should be reviewed for the possibilities of introducing new defects into the hardware and additional temperature cycles added when appropriate. If repairs are complex or difficult to make and inspect, or many unscreened parts are used as replacements, additional cycles should be implemented as appropriate to the individual case.

E. DISCUSSION

1. Purpose of Temperature Cycling

Temperature cycling in black-box acceptance testing is an effective screen for design, workmanship, and electronic parts defects. Table 2 shows that with new, immature hardware temperature cycling should reveal design, workmanship, and electronic part problems with an approximately equal distribution. As the design and assembly processes mature the design problems should diminish significantly and approach zero, the workmanship problems should diminish to some extent, and then the parts problems constitute the major bulk of the failures. If extensive temperature cycling is employed during hardware development, as it should be, then "design" failures during the production program should be minimal, and "workmanship" and "parts" problems should dominate. The number of parts problems is influenced by the extent of the screening accomplished at the parts level. However, significant part problems are frequently detected by temperature cycling of the assembled black boxes even when the individual parts have been subjected to Hi-Rel screening.

Examples of problems detected are listed in Table 3.

2. Summary Table of Industry Survey Results

Table 4 summarizes the data obtained from 26 companies. Of these 26 companies, the practice of multiple temperature cycling was a very strong, unified, company policy with four companies: Collins Radio, Decca Radar, Radiation Incorporated, and Honeywell, Incorporated. Four other companies in the past few months have moved towards a strong policy of multiple temperature cycling. These companies are Martin Marietta Aerospace, TRW, Lockheed, and Aerospace. The remaining companies either do not have a strong policy or are large and diverse, such that multiple temperature cycling may be employed within certain divisions, or on certain projects, or when desired by a particular customer.

3. Data Analyses

Seven companies, listed in Table 5, supplied test data relating failures to the number of temperature cycles.

Figure 2 plots the data from the seven companies and indicates that from 6 to 10 cycles are required for the elimination of incipient defects.

Table 2 Distribution of Temperature Cycling Failures Between Marginal Design, Poor Workmanship and Defective Parts

Company	Maturity of Hardware	Percentage of Failures by Categories:		
		Design	Fabrication Workmanship	Parts
General Electric	Immature	33%	33%	34%
	Mature	Approaches 0	10%	90%
Collins	Immature	33%	33%	34%
	Mature	25%	25%	50%
Lockheed	Immature	10%	50%	40%
	Mature			
Motorola	Mature	Approaches 0	10%	90%
Decca	Mature	5%	40%	55%
Martin Marietta	Mature	5%	35%	60%
Boeing	Mature	Approaches 0	50%	50%
Honeywell	Mature	Approaches 0	40%	60%
Averages for Mature Equipment		5%	33%	62%

*Table 3 Typical Examples of Defects Screened
Out By Temperature Cycling*

Martin Marietta Aerospace

Packaging problems, such as bridging of conformal coating
Shorts and opens in transformers and coils
Defective potentiometers
Intermittent solder and weld joints
Shorted power transistor
Defective capacitors
Cracked dual inline integrated circuits

Collins Radio Co.

Poor solder joints, welds, seals
Nearly shorted wire turns and cabling due to damage or im-
proper assembly
Fractures, cracks, nicks, etc in materials due to unsatisfac-
tory processing
Out-of-tolerance parts and materials

NASA-MSD (Apollo)

Resistor core cracked due to absence of elastomeric buffer
coating
Hairline crack in transistor emitter strap ground connection
Damaged mica insulation washer causing transistor short
Improper staking of tuning coil slug causing erratic output
Cold solder joints
Open within multi-layer boards due to mishandling in processing
Diode internally open at low temperature
Drift problems

Decca Radar Limited

Defective transistor
Intermittent shorts in coils
Lugs shorted to ground
Drift and erratic operation problems

Supplier B

Problems with small gage wire (less than No. 40) in motors,
transformers, and other electromechanical devices
Failure of plastic encapsulated parts

Radiation Incorporated

Drift problems
Integrated circuit problems

Table 4 Summary of Recommended Temperature Cycles From Industry Survey*

Supplier/Agency	No. of Cycles Recommended	Temperature Employed (°F)	Temp. Range (°F)
Lockheed Missiles and Space Co.	8 to 10	-20 to 160	180
General Electric Co.	6 to 10	-65 to 131	196
Aerospace Corporation	6 to 8	Variable	-
Decca Radar, Ltd.	20	5 to 131	126
Radiation, Incorporated	10 to 25	-65 to 131	196
TRW Systems	8	Variable	-
Martin Marietta Aerospace	6 to 10	Variable	-
Boeing Co.	3 to 12	-65 to 131	196
Hughes	Variable	Variable	-
Motorola	22	-65 to 160	225
Collins Radio Co.	9 to 25	-65 to 160	225
Honeywell, Incorporated (Denver)	12	-13 to 131	144
Hewlett Packard Co.	16	32 to 131	99
Grumman Aircraft Engineering Co.	4 to 6	Variable	-
Bendix Corporation	6	Variable	-
Delco (AC) Electronics	5	-20 to 120	140
Raytheon - Equipment Div.	5	32 to 160	128
RCA	3**	Variable	-
Westinghouse	3 or 4	Variable	-
Sandia Corporation	3 to 5	-65 to 160	225
Texas Instruments	2 to 10	-67 to 131	198
Barnes Engineering Co.	2 or more	Variable	-
Goddard Space Flight Center	1**	Variable	-
JPL	?**	Variable	-
Supplier A	5	-65 to 131	196
Supplier B	1	-65 to 165	230

* These are the opinions of the individuals consulted. They may or may not represent the current practice of the referenced companies.

** Additional cycles are required at the subsystem/system level thermal-vacuum tests.

Table 5 Companies Supplying Failure Rate Versus Temperature Cycle Data

Company	Type and Size of Data Sample	Were Hi-Rel Parts Used?	Was Vibration a Part of the Cycle?	Temperatures Employed
General Electric	80 Radar Systems	Yes	No	-65 ^o F to 131 ^o F
Lockheed	80 Command Control Systems	Yes	No	Variable - Most temperature differentials were 160 ^o F
Boeing	150 SRAM Systems	Yes	Yes (2g)	-65 ^o F to 131 ^o F
Collins Radio	360 Radios	No	Yes (2g)	-65 ^o F to 131 ^o F
Decca Radar	10 Radar Systems	No	No	5 ^o F to 131 ^o F
Motorola	270 Radar Augmenters	No	Yes (2g)	-65 ^o F to 160 ^o F
Aerospace	21 Transponders	Yes	Yes	Unknown

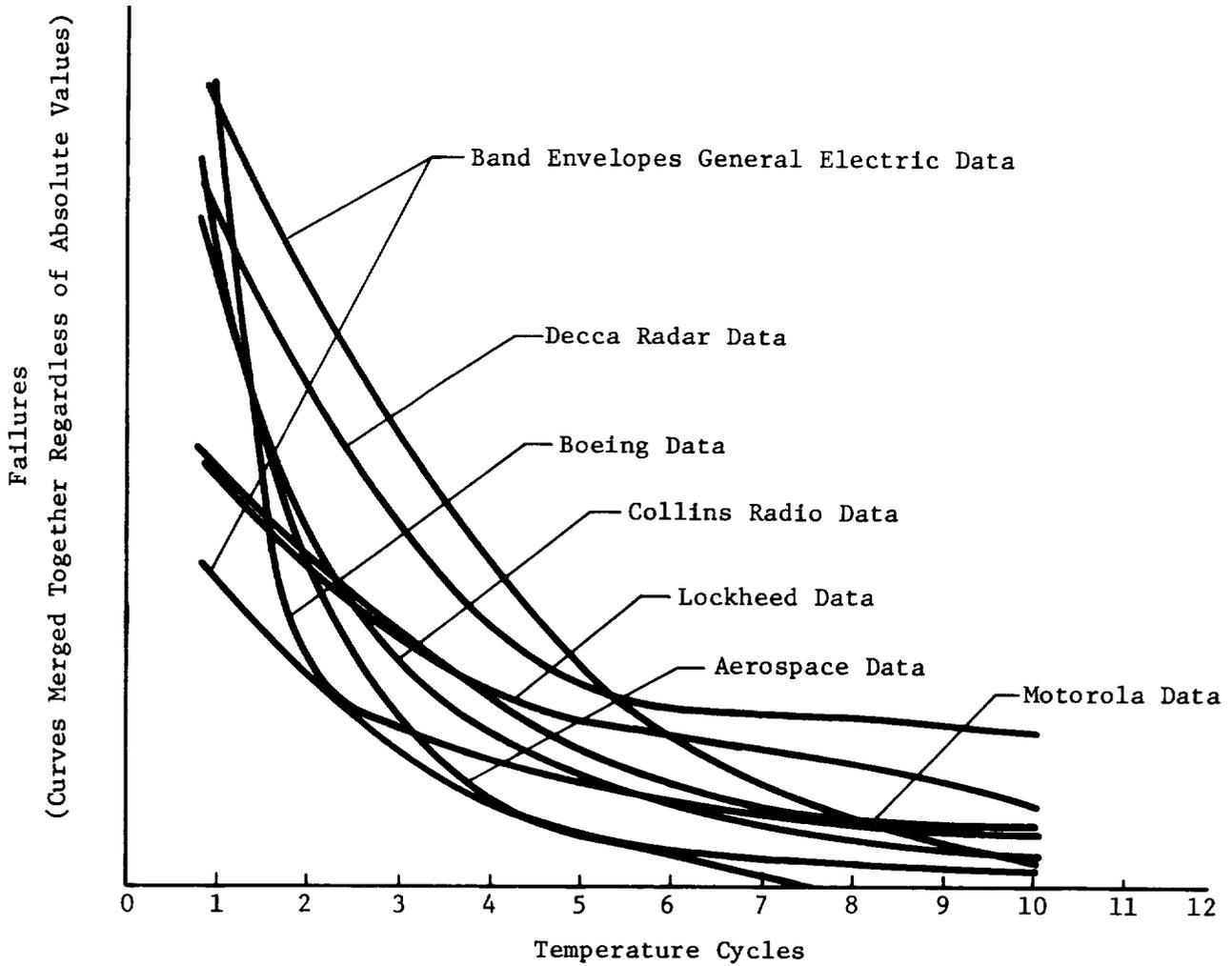


Figure 2 Summary of Industry Survey Data Indicating Six to Ten Cycles Are Required for Elimination of Incident Defects

Actual failure rate data is shown in Figure 3. The spread of the data in Figure 3 is primarily due to differences in the complexity of the equipment. The curves of Figure 3 indicate that more cycling is required with the more complex equipment before the curve approaches a constant failure rate, but a technical explanation for this is lacking. However, even if this proves not to be the case, the guideline recommending more cycling on the more complex equipment still remains justifiable on the basis that the more complex equipment constitutes a greater failure risk and it is therefore cost-effective to impose more stringent screening.

In Figure 3, there is no apparent correlation between Hi-Rel parts vs non-Hi-Rel parts. Such a correlation exists but is masked by other variables.

Figure 4 shows the influence of complexity in failure rate and provided the "average" curve from which the generalized "typical" curves of Figure 5 were derived. The curves of Figure 5 were then used to estimate the risks accruing from the repair of failures and to establish the criteria for additional temperature cycles in the event of a failure.

4. Failure Criteria

The recommended guideline of one final failure free cycle is not only compatible with Apollo and Skylab, but it also represents a logical compromise between two different schools of thought as typified by General Electric and Collins Radio:

- 1) On the G.E.-LRU radar program involving 10 temperature cycles (later reduced to 6 as the hardware matured), the approach was to require the last two cycles to be failure free.
- 2) Collins Radio believes there is no technical rationale for requiring any failure free cycles. Their reasoning is that, if sufficient cycles are used to reach the flat, constant failure rate portion of the curve, there is no purpose in requiring further failure free cycles. For example, if a failure is encountered on the tenth and last cycle, there is little justification for running more cycles because the failure rate of the hardware would not be benefited by the additional cycles.

However, one justification for a final failure free cycle after a simple repair is that it provides confidence on the repair, even though the statistical risk in not performing the cycle appears very small.

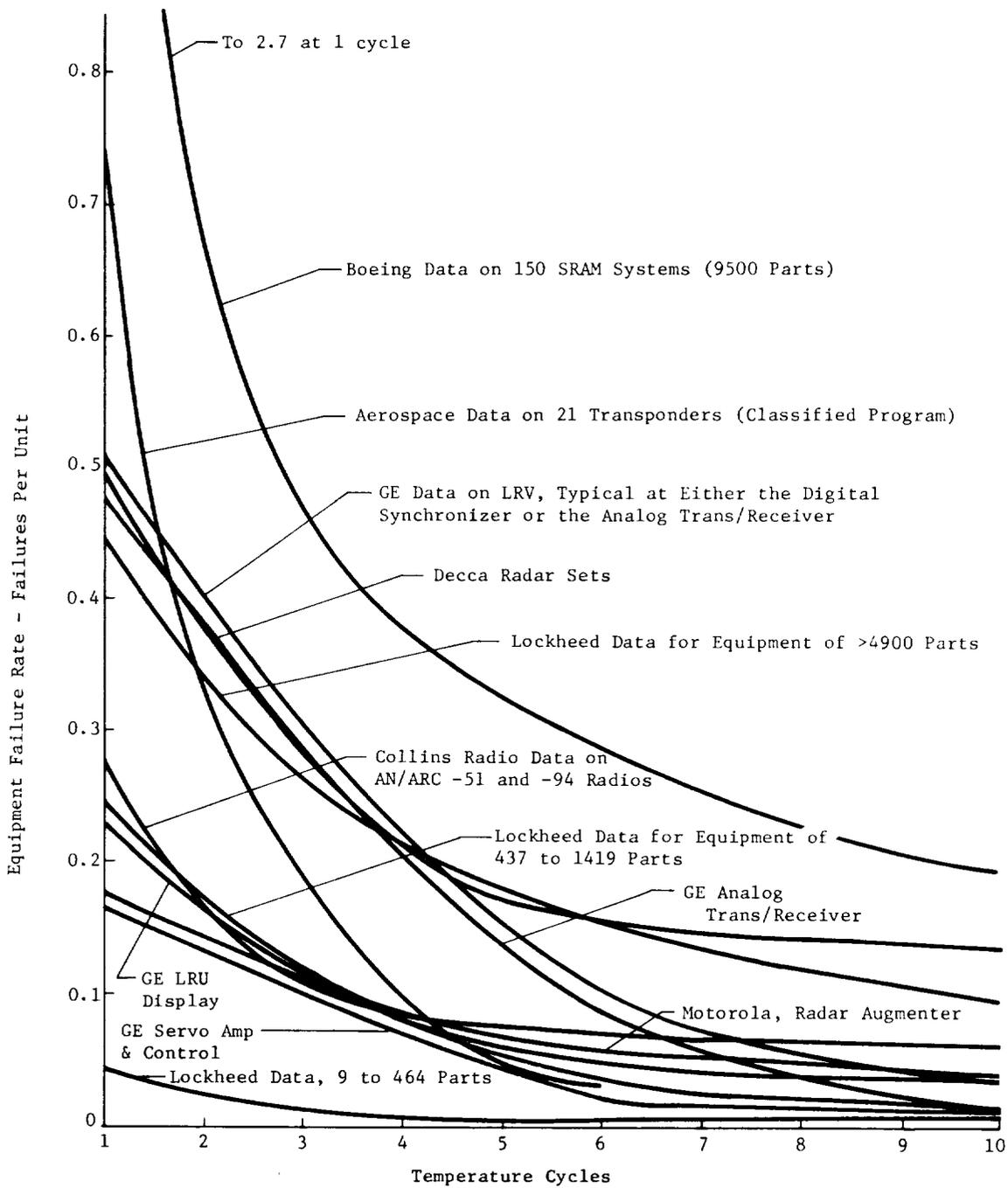


Figure 3 Summary of Industry Failure Rate Data

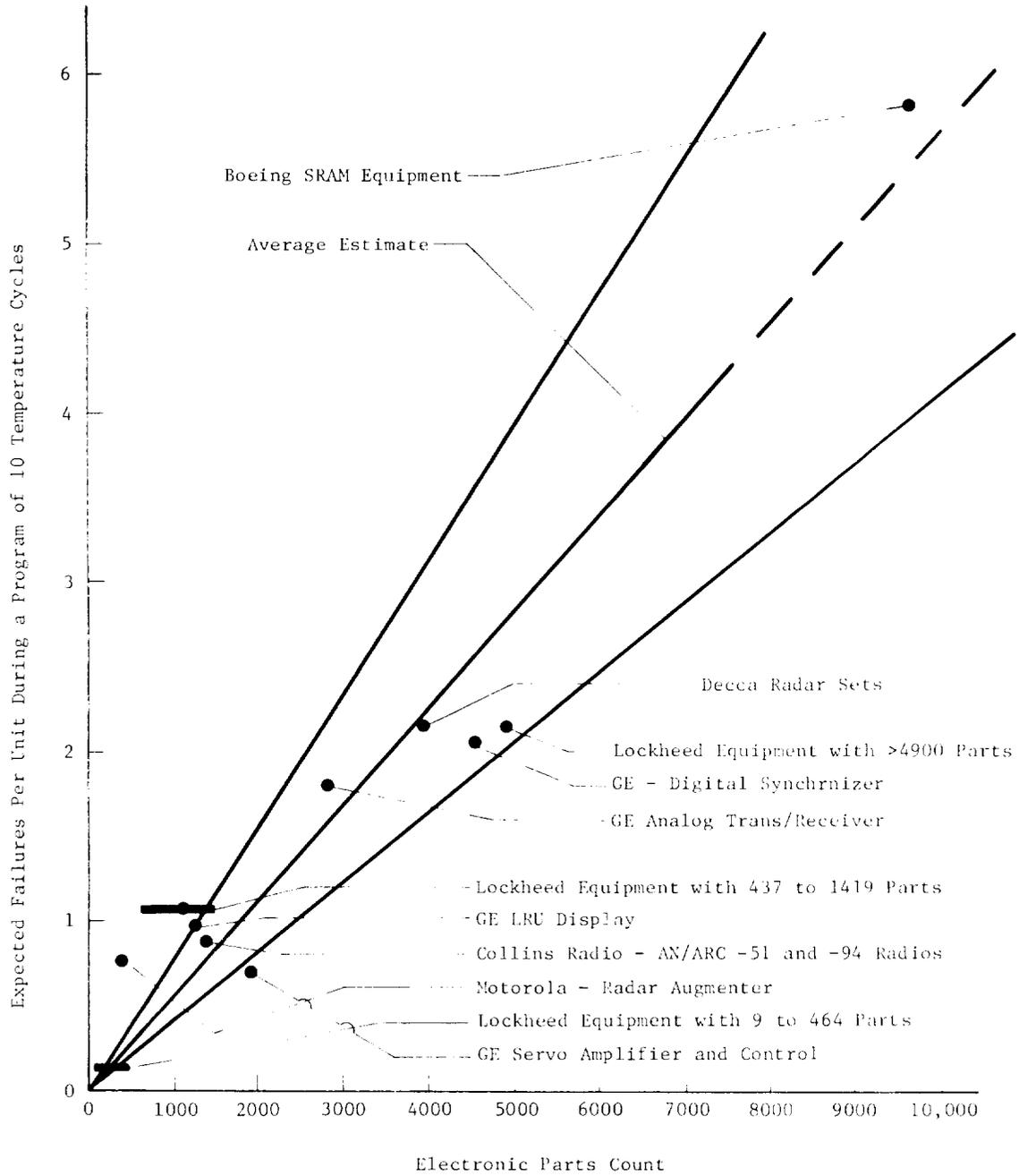


Figure 4 Expected Failures During Ten Temperature Cycles as a Function of Equipment Complexity

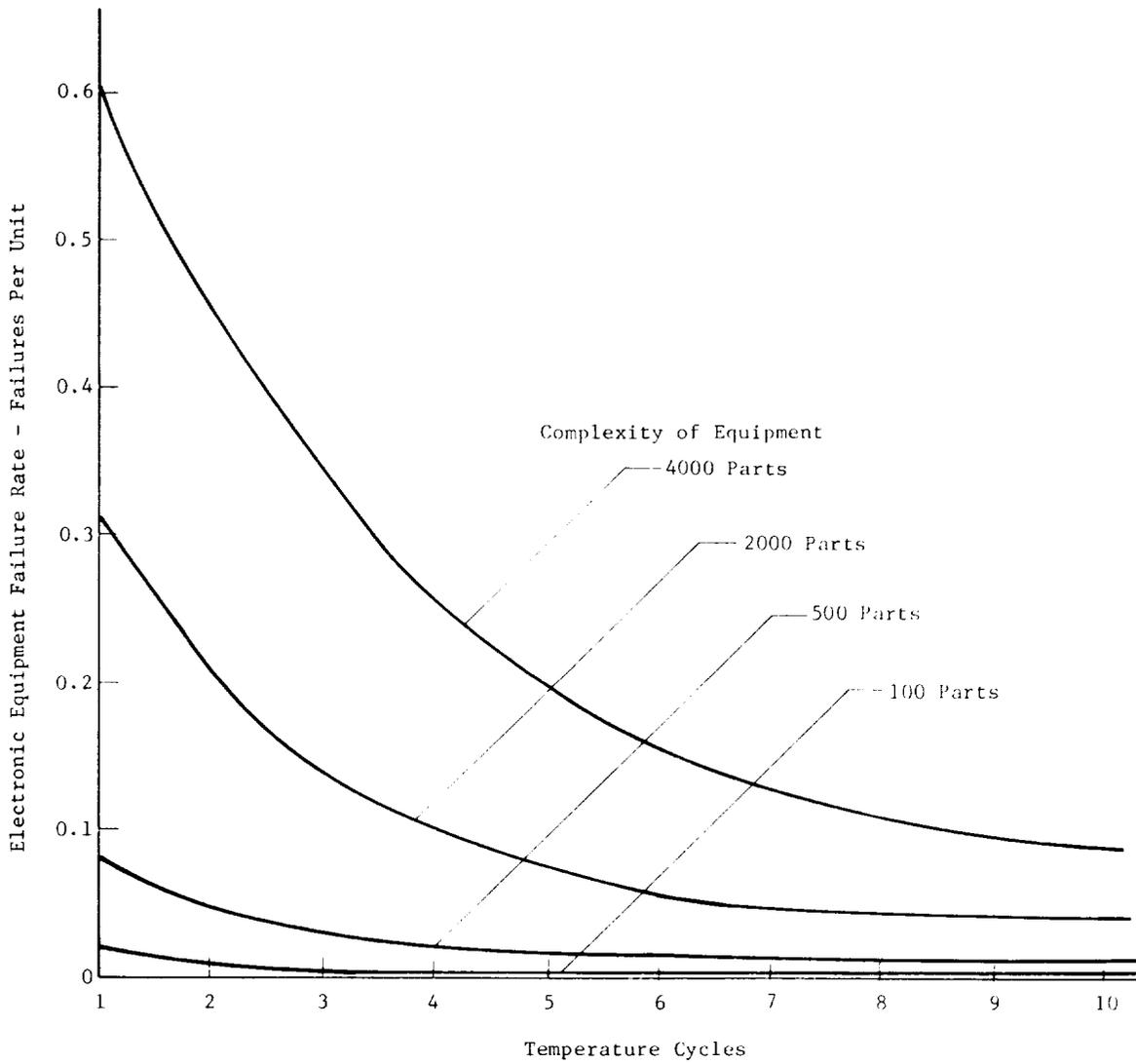


Figure 5 Generalized Temperature Cycling Failure Rate Curves as a Function of Equipment Complexity

5. Risks Associated with Repairs

If a failure and a repair occurs near the last temperature cycle, the question arises as to whether the unreliability introduced by the repair negates the benefits of temperature cycling. This hazard involves two different risks:

- 1) The risk of degrading the hardware by the repair operation.
- 2) The risk of replacing a part with another part that has not been screened by temperature cycling.

With respect to the first risk, if access to the defective component can be easily achieved without disturbing other parts and connections, and if the actual repair can be reliably made and inspected, then the final failure free cycle is felt to be adequate. If such is not the case, then a judgment decision should be made requiring two, three, or four failure free cycles for the affected portion of the hardware. Any repair should be closely inspected under 20 power magnification with attention not only to the repair itself, but also to possible damage to surrounding parts, solder splash, etc.

With respect to the risk of replacing defective parts with parts that have not been screened by temperature cycling, the question can be answered in terms of quantitative risks by considering the failure risks of a typical package of 2000 electronic parts, represented by Figure 5, and an assumed program of six temperature cycles. Assume a failure is encountered on the sixth and last cycle and a simple repair is made consisting of replacing one part and resoldering its connection. The risk of failure of the new part on its first severe temperature cycle encountered in the field will be $0.30 \div 2000$ or 0.015%. Since the remainder of the equipment (the other 1999 parts) has approached a constant failure rate condition of about 4% per cycle, the total risk of a field failure has been increased from 4% to 4.015% by the repair, a negligible increase in risk. It can be seen that the temperature cycling program has reduced the chance of a field failure (assuming the field environment equivalent to one severe temperature cycle) from 30% to 4% and the repair has then increased this risk to only 4.015%. This assumes, of course, that the workmanship associated with the repair was equivalent to the original standards, was as inspectable as the original hardware, and the repair process did not degrade the surrounding parts.

Following this same line of reasoning, but assuming that the repair involved *more* than a single part, a different conclusion will result. For example, assume that the 2000 part electronic package consists of four potted modules of 500 parts each, and that a part in one module fails on the sixth cycle, necessitating a replacement of the entire module. In this case six temperature cycles would ordinarily reduce the risk from 30% to 4%, but the replaced module will increase the risk by $0.30 \div 4$ or about 7%, and produce a total risk of about 10%. Four failure free cycles required at this point, would significantly reduce the risk, from about 10% to about 5.7% for the rather extreme packaging configuration assumed.

These two risk approximations support a conclusion that a very simple, reliably accomplished, replacement of one or several electronic parts introduces negligible risk, but repairs involving many parts, such as a module replacement, will negate the objectives of the test unless additional, failure free, temperature cycles are run. It is evident that criteria for multi-temperature cycling must define the course of action to be taken in the event of a failure. Therefore, the detailed risk calculations presented in Table 6 were performed. Inspection of this table shows that, in pure technical terms, a very simple repair does not justify an additional failure free cycle, but if this policy were adopted, it is envisioned that an endless debate might be precipitated on two issues: One issue being that since repairs are usually more difficult to perform than the original fabrication, one failure free cycle should be performed to provide confidence in the repair. The other issue is that since the Apollo and Skylab programs required $1\frac{1}{2}$, or 1, failure free cycles, the concept of eliminating the failure free cycle is an unjustifiable departure from an established precedent. In consideration of these two factors, the guidelines of Table 7 were derived from Table 6 by replacing the zeros in the table by a requirement for 1 cycle.

Table 6 Estimates of the Number of Additional Temperature Cycles Required (After an Assumed Failure and Repair on the Last Baseline Cycle) to Maintain an Approximately Constant Risk of a Post-Acceptance Test Failure

PERCENTAGE OF TOTAL PARTS REPLACED	CYCLES AFTER REPAIR	% FAILURE RISK OF THE UNREPAIRED PORTION	% FAILURE RISK OF THE REPAIRED PORTION	% TOTAL FAILURE RISK *
4000 Electronic Parts - Baseline Program of 10 Temperature Cycles.				
0 to 0.1%	0	8.0	0.06	8.06
0.1 to 1%	2	7.9	0.34	8.24
1% to 5 %	4	7.6	1.00	8.60
5% to 10%	6	7.2	1.20	8.40
2000 Electronic Parts - Baseline Program of 6 Temperature Cycles				
0 to 0.1%	0	4.0	0.03	4.03
0.1% to 1%	1	3.9	0.20	4.10
1% to 5%	2	3.8	0.60	4.40
5% to 10%	4	3.6	0.75	4.35
500 Electronic Parts - Baseline Program of 3 Temperature Cycles				
.1 to 1%	0	1.0	0.08	1.08
1% to 5%	1	1.0	0.20	1.20
5 to 10%	2	0.9	0.25	1.15
100 Electronic Parts - Baseline Program of 1 Temperature Cycle				
1% to 5%	0	0.2	0.08	0.28
5% to 10%	1	0.2	0.10	0.30

*The above risks assume the repair can be easily and reliably performed without degrading any other parts.

Table 7 Guidelines for Additional Temperature Cycles to be Conducted in the Event of a Failure

Percentage of Total Parts Repaired/Replaced	Number of Final Consecutive Temperature Cycles Which must be survived by the Repaired/Replaced Portion of the Hardware*			
	4000 Parts (10 cycles)	2000 Parts (6 cycles)	500 Parts (3 cycles)	100 Parts (1 cycle)
0 to 0.1%	1	1	N/A	N/A
0.1% to 1%	2	1	1	N/A
1% to 5%	4	2	1	1
5% to 10%	6	4	2	1

*Additional cycles, as appropriate, should also be added when the repair cannot be easily and reliably performed.

As an example for further clarification, assume an electronic device has 4000 electronics parts and a program of 10 temperature cycles has been adopted. On the second cycle, a cold solder joint is detected and is repaired. This repair would be considered "Proven" by its survival throughout the remaining cycles. However, on the 8th cycle, a potted module fails and is replaced by a module containing 160 parts. The 10-cycle program must then be extended to 12 cycles in order to "prove" the new module by 4 consecutive failure-free cycles. Further assume that on the 12th cycle, an R.F. choke fails in another section of the device and is replaced. This would necessitate extending the program to a total of 13 cycles, for the final failure free cycle. It should be noted that, in any event, the last cycle must be failure free.

In summary, it is concluded that if a repair can be easily and reliably performed, and involves only a few new parts, the repair and the new parts are adequately verified by the final failure free cycle, but if the repair operation is difficult, and disturbs other parts, or if the repair involves many new, uncycled, parts, then additional temperature cycles are needed after the repair. Because of the difficulty of specifying criteria in this area, it has been concluded that the decision must be made on an individual basis as appropriate to the specific hardware being tested. The foregoing discussion can be used as general guidance for the specific item in question.

6. Is Temperature Cycling Degrading?

A more properly phrased question is: Does temperature cycling do more good than harm? Or in more technical terms, "Does each successive temperature cycle reveal *more* defects than are brought to the *brink* of failure, to fail on the next cycle?" Or in reliability terms, "Does the failure rate increase or decrease with temperature cycling?" Those companies surveyed which have been long engaged in extensive AGREE testing are extremely positive about the benefits of extensive temperature cycling, while those without this background and experience frequently raise the "degradation" spectre.

Although this writer has discovered no specific data supporting an increasing failure rate characteristic for a complex electronic assembly, certain situations can be imagined which could produce such a characteristic. Suppose for example that the equipment contains 100 conformally coated transistors on plastic stand-offs without lead stress-relief (a situation identified by MSFC as undesirable and very prone to solder joint failure from temperature cycling). Further assume that the assembly process has been so uniform that all transistor solder joints fail on the fifth temperature cycle. Then the overall equipments failure rate curve would show a marked increase at 5 cycles. In this hypothetical case, it would be catastrophic to give the equipment 4 cycles, with the fifth cycle occurring in flight. On the other hand, it would be more desirable to give the equipment 10 cycles than to give it none. This undesirable condition, in a properly executed program, would have been detected and eliminated in the development and qual test programs. The above remarks are intended only as food for thought as the reader struggles with the question of degradation.

R. L. Vander Hamm (Collins Radio) made this statement (Ref 1) as a result of 10 years experience with many AGREE tests in a variety of equipment types:

"Quality and well-designed parts and materials are fully capable of withstanding the extended, temperature-cycling, AGREE-test environment. No example can be cited of a quality part (if used properly) failing at an excessive rate during AGREE testing. And, equally important, when a chronic failure mode does appear in a particular part, it can usually be easily corrected by the competent vendor."

This statement is substantiated by the data supplied by Collins Radio and shown in Figure 6 and Table 8. Figure 6 indicates that "no major ill effects are induced with as many as 250 to 300 cycles." This conclusion is based on the fact that, after about 12 cycles, the curve remained flat out to 300 cycles. An interesting feature of Figure 6 is that the curve is flat at 5, indicating that the AGREE cycle used had an accelerating effect of about 5.

Collins Radio further reports that in a new contract from McDonnell-Douglas to supply radios for the new F-15 fighter, they will use AGREE Test Plan 3 on two radios for reliability demonstration tests, and it is expected that the radios may receive 600 cycles each. Yet Collins is confident that degradation effects will not be encountered in this program.

The Decca Radar Co. of England manufactures thousands of marine radars. Ten percent of their monthly production is subjected to 20 AGREE type temperature cycles, then refurbished and sold.

This author queried Mr. Harris of the Decca Radar Co. about the degrading effects of temperature cycling. The following statement is excerpted from his replying correspondence:

"We would most certainly agree that, in general, thermal cycling is not degrading to discrete electronic parts or assemblies providing that they have been properly manufactured in the first place. Faulty batches of components, dry joints, pinched cables, etc, do show up under stress. On completion of the test period all equipments are re-inspected by the Quality Assurance people and completely refurbished before being sold to the customer. But I would emphasize that all equipment which is subjected to this temperature cycling *is* sold to the customer and certain customers who are aware of the procedure would like to think they could select an equipment that had been through the environmental test procedure, rather than take delivery in the normal way. Unfortunately when equipments are delivered they are made up from a random selection of units from Finished Unit Stock and this prevents the customer from getting a completely environmental tested equipment and also prevents us from following the history of the equipments after they leave environmental test. The refurbishing which takes place, generally consists of replacing cathode ray tubes which have, by necessity, been changed quickly during the test and bringing the exterior paintwork and appearance up to factory standard.

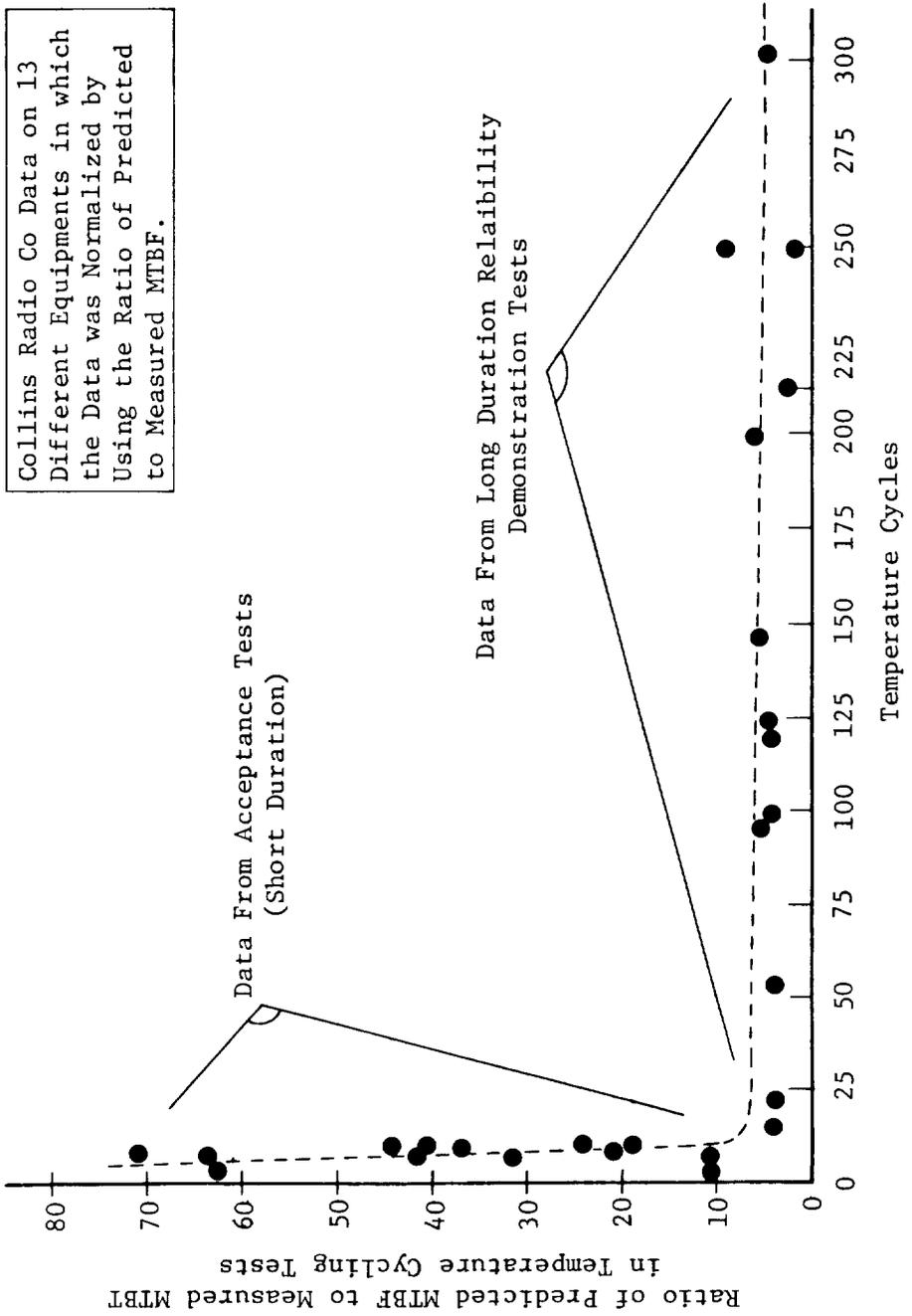


Figure 6 Test Data Showing No Increase in Failure Rate with as Many as 250 to 300 Temperature Cycles

Table 8
Burn-In and Demonstration Test Data

Equipment No.	Equipment Description	Demonstration Test Temperature Limits	Total Demonstration Test Hours	Average On Hrs Per Unit in Demonstration Test	Average # of Temp. Cycles Per Unit in Demo. Test	Ratio of Pred. Military MTBF to Demo. Test MTBF	Burn-In Temperature Limits	Burn-In Test Length	Burn-In "On" Time	Burn-In Temp. Cycle Per Unit	Ratio of Pred. MTBF to B.I. MTBF
1	W/F Com.	-40, +55°C	5,000	500	125	4.8	-40, +55°C	48 Hrs	32	8	72
2	UHF Com.	-54, +55°C	15,000	70	14	2.6	-54, +55°C	48 Hrs	30	6	11
3	W/F Com.	-40, +55°C	17,000	850	212	2.4	-25, +55°C	24 Hrs	12	3	63
4	Radar	-54, +55°C	3,000	1000	250	9.8	-54, +55°C	48 Hrs	30	6	32.5
5	Radar	-54, +55°C	2,300	700	140	5.5	-54, +55°C	72 Hrs	45	9	17.5
6	Transponder	-54, +55°C	5,000	1250	313	5.0	-54, +55°C (+71 for 1 Hr)	48 Hrs	24	6	42
7	DME	-40, +55°C	3,600	600	120	4.8	-40, +55°C	72 Hrs	45	9	40.5
8	Nav. Ra	-40, +55°C	2,306	230	58	4.1	-40, +55°C	36 Hrs	36	9	24
9	Coupler	-54, +55°C	6,000	300	75	5.2	+54, +55°C	24 Hrs	12	3	10
10	ADF	-54, +55°C	5,150	1000	250	1.8	-40, +55°C	72 Hrs	36	9	37
11	UHF Com.	-54, +71°C	110,000	150	22	1.8	-54, +71°C	96 Hrs	56	8	20
12	Coupler	-54, +71°C	1,600	800	200	5.6	-54, +71°C	72 Hrs	36	9	44
13	Altimeter	-54, +55°C	2,200	220	110	4.2	-54, +55°C	20 Hrs	10	5	63.5

"We have no evidence that the temperature cycling we carry out has any degrading influence on any solder joint, printed boards with brittle copper (which is one of the normal hazards of PC boards), or potted modules which could affect their performance during the normal life of an equipment which is 10 to 15 years; but, at the same time, it must be remembered that we are designing equipment for service on board merchant vessels where *some* unreliability is accepted and, although as yet we have not found any failures which could be related to thermal cycling I cannot presume to say that the standard of reliability at which we are aiming bears any relation to the standards required in spacecraft. The requirements for reliability of any equipment must obviously be related to the environment in which it is expected to work and be maintained and whilst the reliability programme which we are using produces very good results for the marine environment I would hesitate to be dogmatic where space requirements were concerned."

To pursue the degradation issue further, the basic capabilities of electronic hardware to withstand temperature cycling is summarized below.

a. Electronic Parts - Qualification of electronic parts generally includes 5 to 15 temperature cycles from -85°F to a high temperature usually between 257°F and 347°F . The rates of temperature change for temperature cycling in air is about 3°F per second. Severe temperature shocks in hot and cold liquids are also used, involving rates of about 100°F per second. Electronic parts within a black box in a black box temperature cycling test typically undergo a comparatively slow temperature change of about 0.03° per second. It can be seen that electronic parts have a much greater capability in terms of both temperature extremes and rate of change than required in black box temperature cycling.

A recent RCA paper (Ref 2) on thermal fatigue tests on the RCA 2N3055 power transistor in a number of different current applications is interesting. In the severest power transistor application (ΔT of 145°C and maximum junction temperatures of 200°C) the first failure did not occur until 449 cycles, and in most of the less severe applications, more than 10,000 cycles were required to produce the first failure.

b. *Multilayer Printed Circuit Boards (MIB)* - H. C. Hurley (Ref 3) conducted tests for RADC on MIB's using three environments, the most severe of which was temperature cycling between -85°F and 230°F, using rates of change of about 0.1°F per second. In this test cycle the first electrical opens were detected on the control samples at 150 cycles. However, with boards intentionally manufactured with brittle copper, 50% circuit failure occurred at 20 cycles (versus 300 cycles for the good quality control samples).

c. *Solder Joints* - Martin Marietta, Orlando Division (W. P. Wood) conducted a test program in which solder joints on PC boards were subjected to 1000 severe temperature shocks by alternately plunging the boards into dry ice and alcohol at -100°F and boiling water at 190°F. (The water tended to become contaminated by alcohol.) At 20 cycles two of the 2405 joints had developed visible cracks. After 1000 cycles 721 joints of the 2405 joints tested had developed visible cracks. Several hundred of the cracked joints were then electrically checked and no electrical opens were found. *It must be emphasized that these were joints on which no lead stress had been imposed.*

The above indicates that, *by themselves*, electronic parts, PC boards, and solder joints have great capability to withstand temperature cycling. The problem usually begins when this hardware is packaged into an assembly.

Some typical troublesome problems are summarized.

- 1) Electronic components assembled on PC boards without stress relief bends impose loads on the solder joint, and temperature cycling may produce solder joint cracking. Heavy coats of conformal coating on even a stress relief bend can negate the beneficial effect of the bends.
- 2) Transistors mounted on plastic spacers and coated with conformal coating will produce cracked solder joints in a few temperature cycles if the leads are not stress relieved. This problem arises because the coefficient of thermal expansion for plastics is about 8 to 30 times greater than Kovar transistor leads, or Dumet diode leads.
- 3) Large multi-pin modules soldered into the PC board may result in solder joint cracking, particularly if the conformal coating bridges between the module and the board.

- 4) Cordwood modules potted with a rigid, *solid*, polyurethane or epoxy may produce cracked joints and even crush weak parts such as glass diodes on the very first application of a temperature cycle.
- 5) Filters, motors, and transformers containing fine wire (no. 48 or No. 50) may constitute a problem. To avoid the problem, wire sizes larger than No. 40 should be used.
- 6) Single or double sided PC boards without plated through holes are undesirable.
- 7) Breakage of glass diodes can be expected if great attention is not given to the encapsulating material and the process.

The above situations must be designed out of hardware for long life applications, regardless of whether stringent thermal cycling is employed in acceptance testing. Proper use of thermal cycling during development and qualification testing will insure a packaging design that is compatible with the use of stringent temperature cycling during production acceptance testing.

7. Remarks on AGREE Testing

The philosophy of reliability testing was first introduced in 1957 in the report by the Advisory Group on Reliability of Electronic Equipment (AGREE). This philosophy is now reflected in MIL-STD-781B, 15 November 1967. This document defines procedures to be followed in both (1) qualifying new equipment to a required MTBF level and (2) then maintaining this level on the production units. When AGREE testing is used on 100% of the production hardware, it basically constitutes an environmental acceptance test somewhat similar to what is currently being done on many spacecraft programs, except that AGREE requires a greater number of temperature cycles than is usually employed. The AGREE Environmental Profile is shown in Figure 7.

Wright Field is the major proponent of MIL-STD-781B, with the Navy a close second. The Air Force Launch Vehicle and satellite programs, and NASA do not utilize 781B to any significant extent. The reason for this may be related to the low production quantities required by a typical spacecraft contract, and a feeling that AGREE testing is not cost-effective on contracts involving only a few production units. However, it is this writer's opinion that the temperature cycling philosophies of MIL-STD-781B are applicable without question, even though the issue of reliability demonstration remains controversial on small production programs.

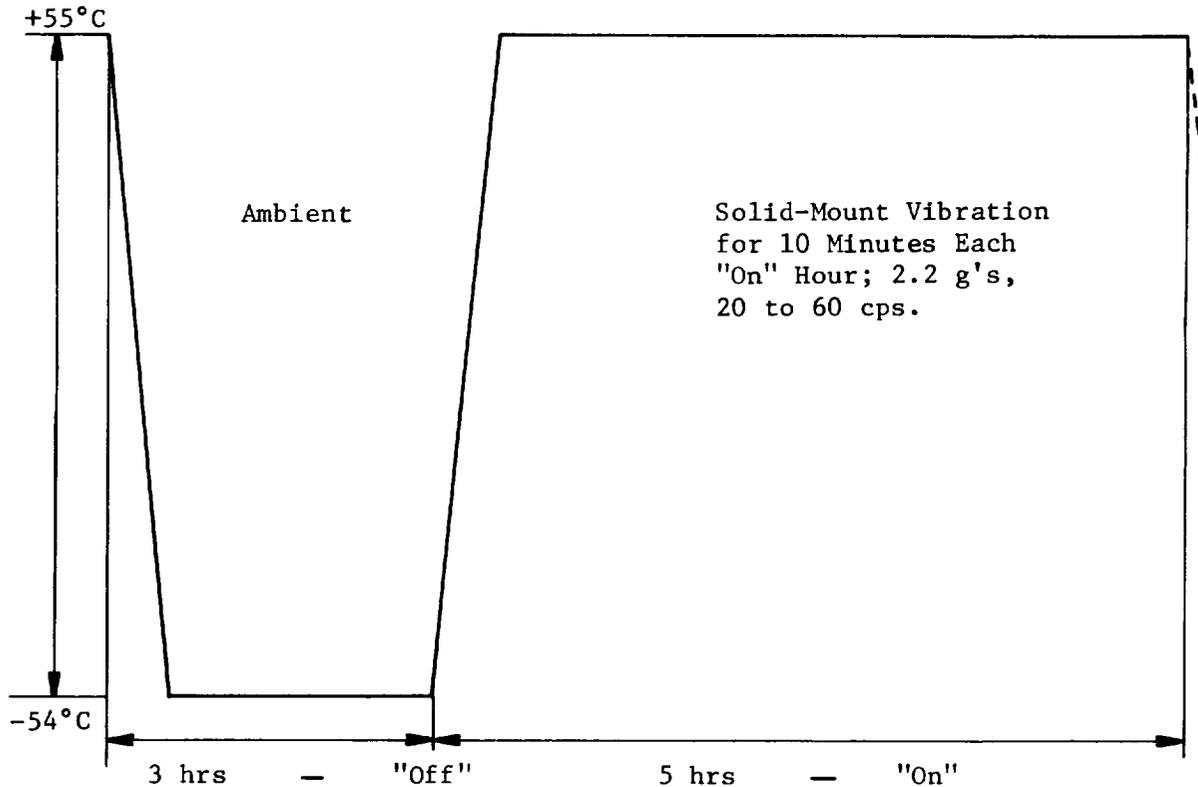


Figure 7 Agree Environmental Profile

8. Remarks on Rate of Temperature Change

Occasionally, concern is expressed that black box "degradation" may be caused by a too rapid temperature change. It should be remembered that even though a closed black box is plunged from cold air at -65°F to hot air at 160°F , the *internal* parts will require several hours to reach 160°F due to the insulating effects of the case. Curve D of Figure 8 shows that the rate of change of the internal electronic parts in a conventional temperature cycling test is quite slow, as compared with Curve A (conventional electronic part temperature shock test by immersion in liquids), or Curve B (conventional electronic part temperature shock test in air). Curve C approximates the more rapid temperature change that can be obtained if the black box covers are removed. This practice is encouraged by General Electric Co. Rapid changes are also encouraged by Supplier B, and Hughes Aircraft Company.

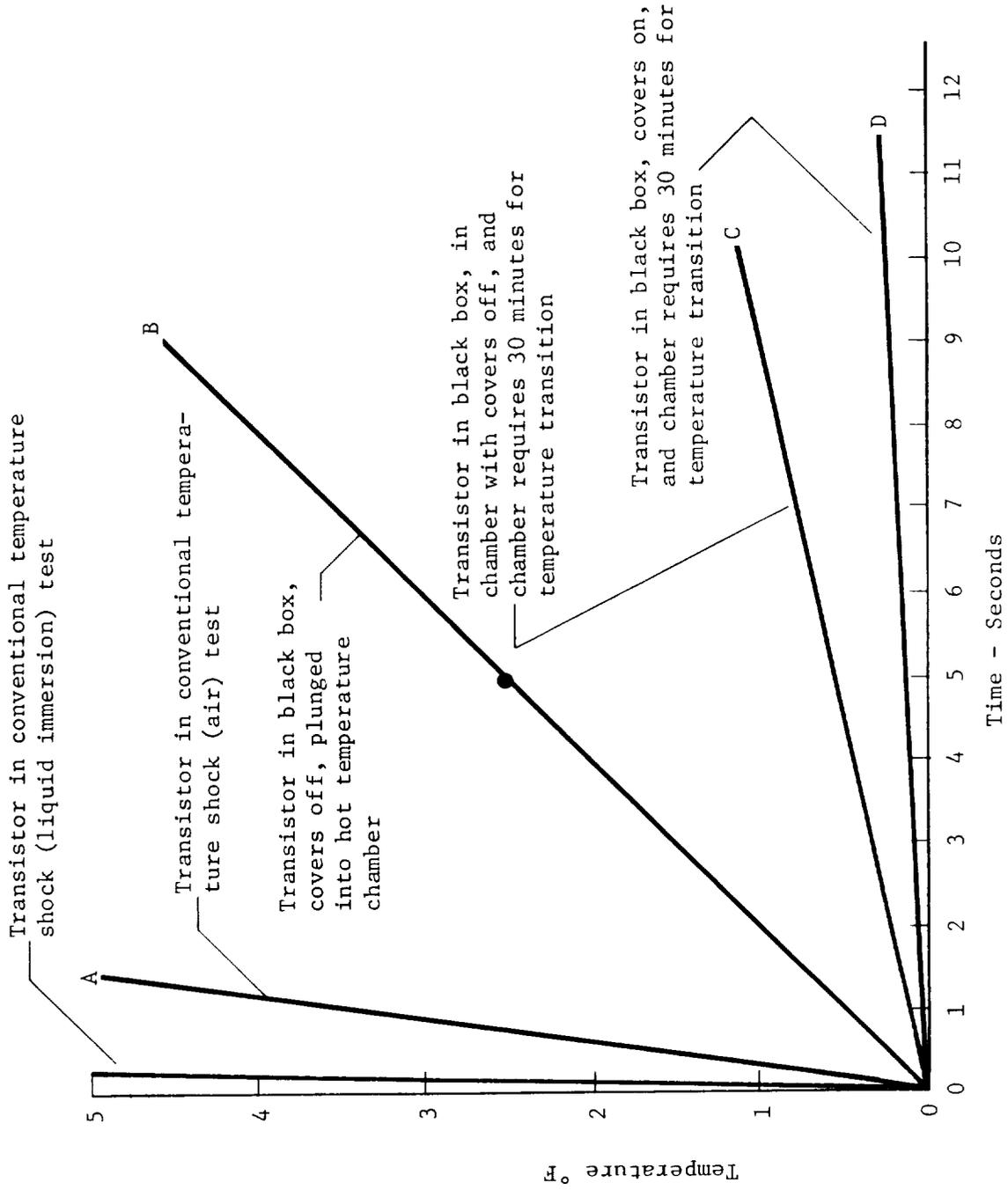


Figure 8 Comparison of Temperature Change Rates in Various Types of Temperature Testing

A simple explanation of how a very rapid temperature change introduces stresses on bonds due to differential thermal expansion is shown by the following hypothetical assembly (Fig. 9).

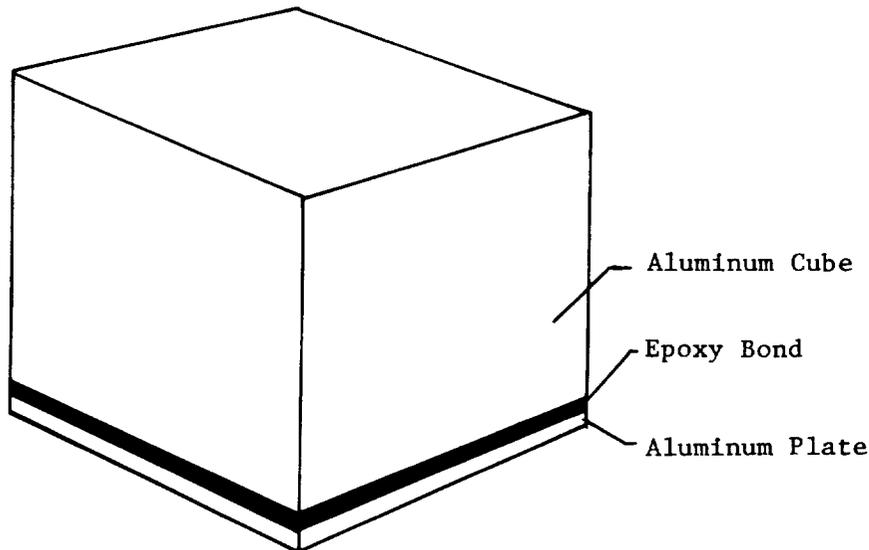


Figure 9 Hypothetical Electronic Assembly Showing Temperature Stress on Bonds

If the above assembly is subjected to a slow temperature change, no shear stresses are developed between the cube and the plate (aside from those introduced by the epoxy). However, if the assembly is subjected to a very rapid change, say immersion in a hot liquid, the temperature of the plate will rise much more quickly than the cube, and significant shear stresses are developed at the bond because the plate will expand before the cube begins to expand. Such effects are present when the high rates of Curve A Figure 8 are used, and are present to a much lesser extent with the comparatively slow rates of Curve D.

9. Relationship Between Multiple Temperature Cycling and Thermal Vacuum Testing

Multiple temperature cycling is employed by many manufacturers who deliver black boxes to prime contractors, particularly on Air Force (WADC) and Navy contracts. On the other hand, agencies who are responsible for NASA spacecraft at the systems level generally do not employ multiple temperature cycling but do employ thermal-vacuum testing, usually at several levels of assembly, starting with one cycle on the black boxes. Since this report recommends increased use of increased temperature cycling

at the black box level, the question arises as to whether multiple temperature cycling, say 10 cycles, should be accomplished as a thermal-vacuum test, or whether the two tests, temperature cycling, and thermal-vacuum, should be conducted as separate tests. Our recommendation is that they should be conducted as *separate* tests. The rationale for this conclusion is presented in the following paragraphs.

Thermal-vacuum testing, to effectively assess out-gasing phenomena, must consist of *long duration* soaks at low and high temperatures with emphasis on the long duration, high temperature, soak. Hence one cycle of a thermal vacuum test may take days, or weeks in a costly thermal vacuum test facility since heat transfer is accomplished by radiation. Also, the temperature ramps are quite slow, too slow for the most efficient detection of incipient failures. Also, extending the duration of a thermal-vacuum test out to, say 10 cycles, would be both very time consuming and very expensive.

Another consideration is that in a systems level thermal-vacuum test the temperature levels may be too mild to achieve the intended purpose of detecting incipient failures. For example, if a spacecraft has a thermal control system, the prime objective of the thermal-vacuum test would be to demonstrate proper performance of the thermal control system and the individual black box temperature excursions may be quite mild.

It therefore appears much more desirable to conduct multiple temperature cycling on the black boxes using conventional, ambient air, temperature chambers, and then to follow this test with the conventional thermal-vacuum test, and of course, the conventional 6g (minimum) vibration test. At later stages of assembly, thermal vacuum testing (but not multiple temperature cycling) would also be applied at the subsystem and systems level, along with appropriate vibration or acoustic exposures, facilities permitting.

However, it appears that, in planning a multiple temperature cycling program for black box acceptance testing, the proposed guidelines of Table II could be used, but modified with some credit being given for the number of thermal-vacuum cycles to be accumulated at higher levels of assembly and test. It is suggested that this credit be estimated, not on a 1 to 1 basis, but on a 2 to 1 basis, because of the lessened effectiveness of thermal-vacuum testing in detecting non-vacuum-related workmanship defects.

Mr. Gomberg's paper (Ref 7), abstracted in the Industry Survey Section of this report, describes an RCA study of spacecraft programs which has resulted in a shift of emphasis away from thermal-vacuum testing and toward temperature cycling.

10. Cost Effectiveness of Temperature Cycling

A prime concern of NASA-MSD is the reduction of support costs; that is, the total cost of reacting to failures incurred by the customers (and the producer) after the hardware is delivered to the field.

The following information is directly quoted from Mr. R. L. Vander Hamm's paper (Ref 1):

"Support to the airline/commercial customer during equipment operation involves many things. Included are normally required activities for new equipment such as training in operational and maintenance characteristics of the equipment and assistance in solving installation problems. A variable cost, however, is related to the degree of support provided depending on MTBF, or, the operational reliability of the equipment. These services, provided at no cost to the customer, typically include: Frequent trips by field service and design engineers to investigate and correct reported chronic problem areas, providing a supply of extra equipment spares to maintain operations, supplying field retrofit kits to correct chronic problems, issuing formal service bulletins and supplying associated spare parts, and, return of equipment to the factory for repair and rework. The relative magnitude of these costs is represented in Figure 10.

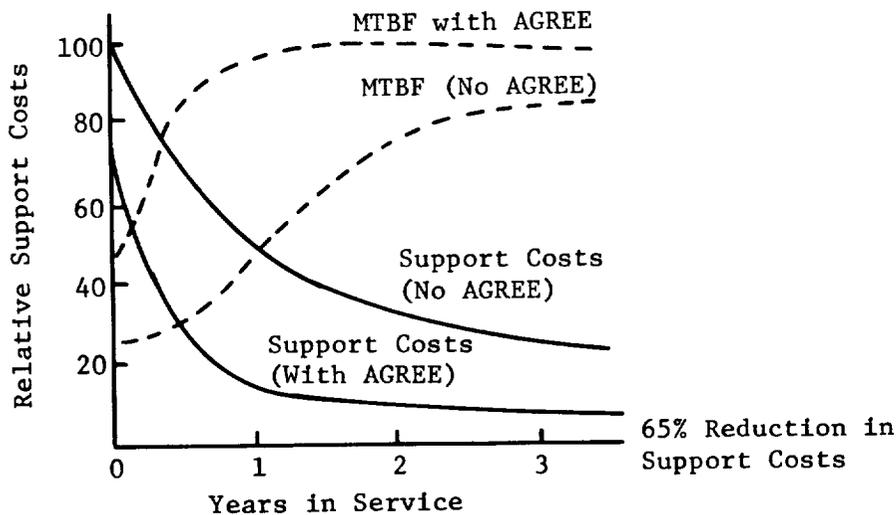


Figure 10 Relationship of Support Costs to MTBF

"It has been established that for an equipment of average complexity (1200 to 1600 parts) delivered in relatively large quantities and operationally reflecting the "normal" reliability growth curve, the support costs will reach six figures, or, approximately two to five percent of selling price. For the same equipment, given the benefit of a comprehensive reliability program including AGREE testing, these support costs should be reduced by as much as sixty or sixty-five percent. (There are other significant savings in the second case, such as reduced cost of manufacturing and engineering support to manufacturing. Also to the credit of the second example is the purely subjective estimate of increased sales due to better equipment reputation and customer good will.)

"Having established the costs to support a conventionally designed and produced electronic equipment and the same costs for a similar 'debugged' equipment, do the cost savings warrant expenditure necessary to perform the reliability test program? The answer is a resound yes! Total costs for a reasonably comprehensive reliability program during design, and extensive AGREE-testing on prototype and early production models, would not exceed \$20-35,000, on the average. Note that this sum is considerably less than the extra costs of supporting an 'unreliable' equipment."

F. INDUSTRY SURVEY

1. Collins Radio Co.

This company adopted temperature cycling in 1959, basing their approach on the early version of MIL-STD-781B. They produce both commercial and military equipment and employ a number of different approaches depending on their customers. They have 100 temperature chambers in almost constant operation.

On production acceptance testing, Collins' policy can be generalized as follows:

Commercial Equipment	3 to 6 cycles, -40°F to 131°F
Most Military Equipment	9 to 12 cycles, -65°F to 160°F
Some Military Equipment	16 to 25 cycles, -65°F to 160°F

The cycles are 6 to 8 hours in length, 50% hot and 50% cold.

On the S-3A aircraft for Lockheed and the E-2C aircraft for Grumman, about 25 temperature cycles are being employed.

Collins has found temperature cycling so beneficial that they perform temperature cycling on commercial products, even when not required by contract. On commercial equipment with a one-year warranty, the acceptance test usually settles out at about 6 temperature cycles. Three temperature cycles are still employed even when no warranty considerations are involved.

A common pre-production (development) test is to run the equipment 500 to 1000 hours (160 cycles). They have had problems with plastic encapsulated devices and one problem with potted cordwood modules.

It is common practice to periodically select production units which have completed the above tests, and put them in another chamber for a period of many weeks for exposure to another hundred or so temperature cycles for demonstration of MTBF. The length of this exposure depends upon the MTBF requirements of the particular contract. After this test, the test hardware is inspected, refurbished, and sold as production units. The refurbishment consists of paint touch-up and replacement of parts with a wear-out failure mode such as power amplifier tubes and blower motors. There is no indication that service life is shortened by the refurbishment.

During the temperature cycling test of Hi-Rel black boxes, repeated exposures to vibration at one to two g's at 20-60 cycles are accomplished using a shaker built into the chamber. Mr. Rutledge estimates that the proportion of failures induced by temperature cycling is 95%, with the 2g vibration playing a very minor role.

Mr. R. L. Vander Hamm believes that constant temperature burn-in of black boxes is quite ineffective and does not recommend combining constant temperature burn-in with temperature cycling burn-in.

In temperature cycling, Collins uses a nominal rate of change of 5°C per minute and believes that rapid rates approaching temperature shock conditions should be avoided as unrealistic. They adjust their temperature cycles in accordance with the thermal mass of the hardware. That is, larger equipments usually are given an 8 hour cycle and smaller equipment, a 6 hr cycle. It is felt that soak time at temperature is not greatly significant, as compared to the two other factors of rate of change and the temperature excursions used.

Usually, the same temperature range is used in Qualification Testing, that is, no margin between Qualification and Acceptance Test levels. However, assurance of no degradation in acceptance testing is certainly provided by the margin in the number of cycles, since they nominally run 160 cycles in their preproduction (development) testing.

With respect to the trade-off between Hi-Rel parts and the number of temperature cycles, the approach, when high reliability is desired, is to increase both the severity of parts screening and the temperature cycling, and the use of high rel parts is never used as a rationale for decreasing the temperature cycling.

Figure 11 presents data from a paper by R. L. Vander Hamm (Ref 1) showing failure rate versus the number of temperature cycles. Collins uses this curve as typical for their electronic equipment.

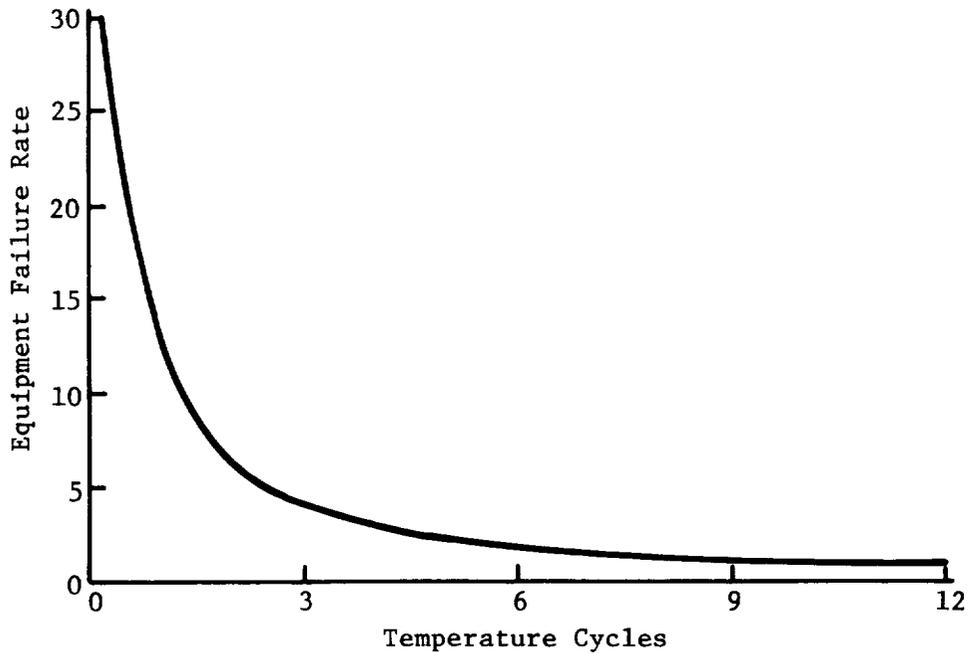


Figure 11 Collins Radio Company Temperature Cycling vs Failure Rate Data

More specific Collins data (Ref 4) from AGREE-3 testing of the AN/ARC-51 and AN/ARC-94 is presented in Figure 12. Data was accumulated over a period of about two years from monthly reliability tests. About 300 AN/ARC-51's and 60 AN/ARC-94's were tested. The effectiveness of temperature-cycling and its relationship with test time are clearly shown. The data of Figure 12 was replotted as Figure 13 in order to facilitate comparisons with the other data of this report.

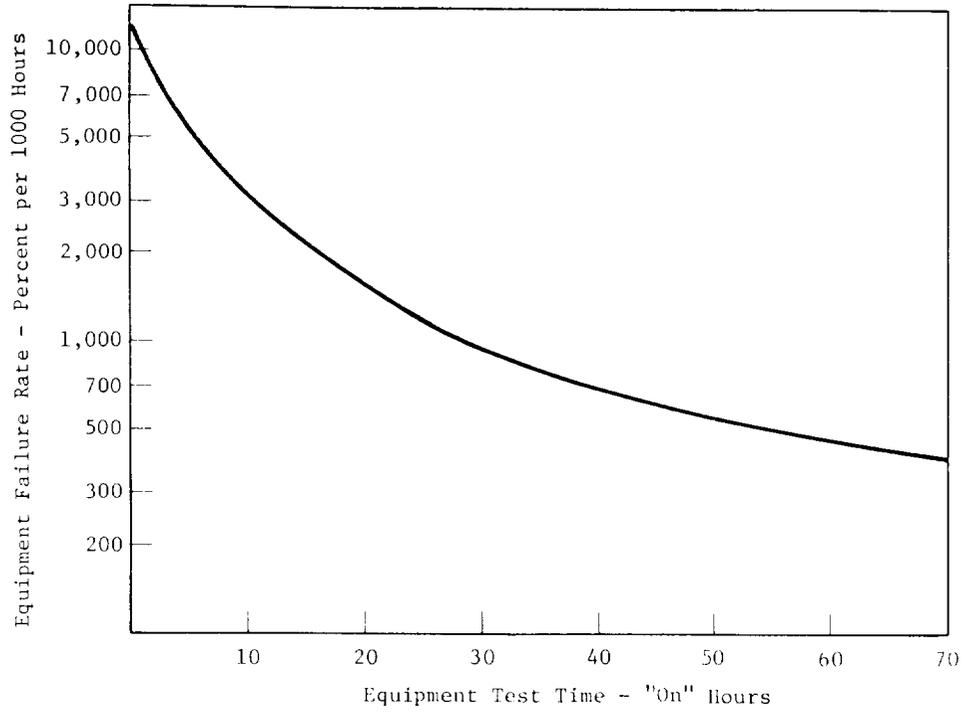


Figure 12 Relationship of Rate of Infant Mortality Failures to Agree-3 Test Time (AN/ARC -51 and AN/ARC -84)

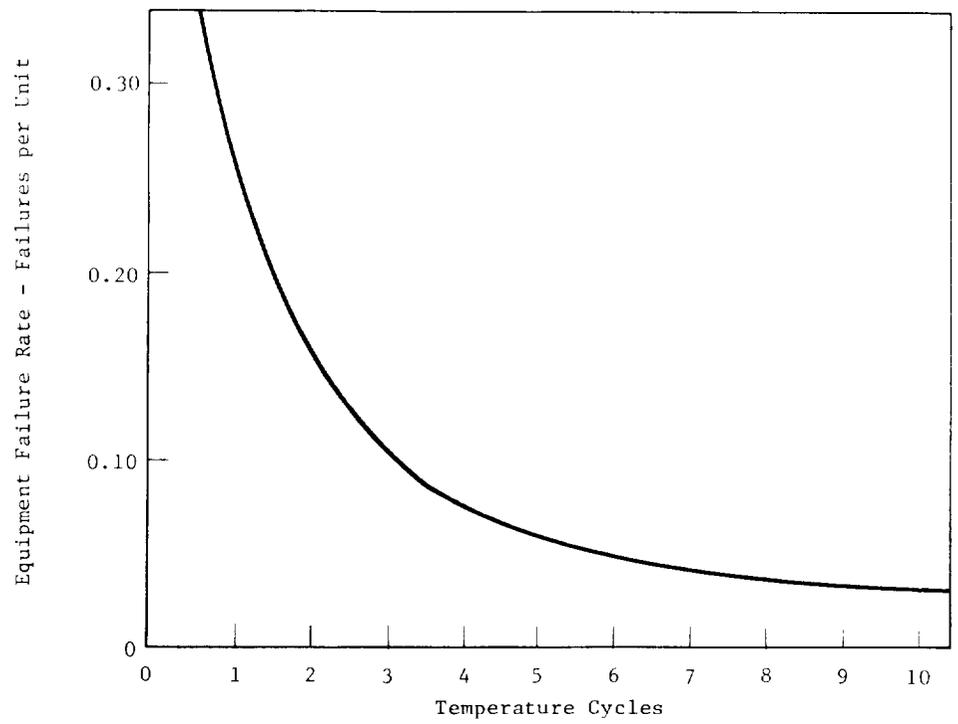


Figure 13 Data From Figure 12, Replotted

2. General Electric Company - Aerospace Electronics

The use of temperature cycling varies with the particular contract. A typical approach is described. Again, the AGREE approach is being employed on radars for the F-111. This is a large production contract involving about 20 radars a month. Early acceptance testing employed 10 AGREE temperature cycles, but as the equipment matured, the number of cycles was reduced to 6. The last 2 cycles are required to be failure free. The average production radar experiences about 7 cycles, but isolated units, in early production, received as many as 20 temperature cycles. The temperature range is -65°F to 131°F. Qualification units accumulated 18,000 hours of reliability demonstration testing, amounting to hundreds of temperature cycles. Mr. S. G. Miller feels that the benefit of a temperature cycling test is derived almost wholly from the temperature ramps and the soak time at maximum and minimum temperature is of minor importance. He also recommends *rapid* temperature changes as being very desirable, and to facilitate a more rapid temperature change on the electronic parts, the covers over the equipment are removed and the chamber air blown through the equipment. Mr. Miller also emphasized that the temperature cycling program should be planned with consideration for the anticipated used environments.

The data supplied by Mr. Miller on the F-111 LRV radar systems show that 6 to 10 cycles are required before the curve becomes flat. This data is presented as Figures 14 and 15. In these tests, the AGREE 2g vibration exposure was not used, since it is felt to be ineffective.

3. Lockheed Missile and Space Co.

Mr. C. Leake and Mr. D. C. Hill have been addressing exactly the same objective as this writer and have arrived at the conclusion that about 8 to 10 cycles and a temperature range of 160 to 180°F is required for complex electronic equipment. Generally, Lockheed controls the rate of change to less than 7°F per minute, but consideration is being given to more rapid rates. Mr. Leake believes that the additional number of cycles required in the event of failure should be determined on the basis of the amount of rework necessary to replace the failed part, the number of parts replaced, and whether or not temperature cycles were employed at the lower levels of assembly, such as the PC board level.

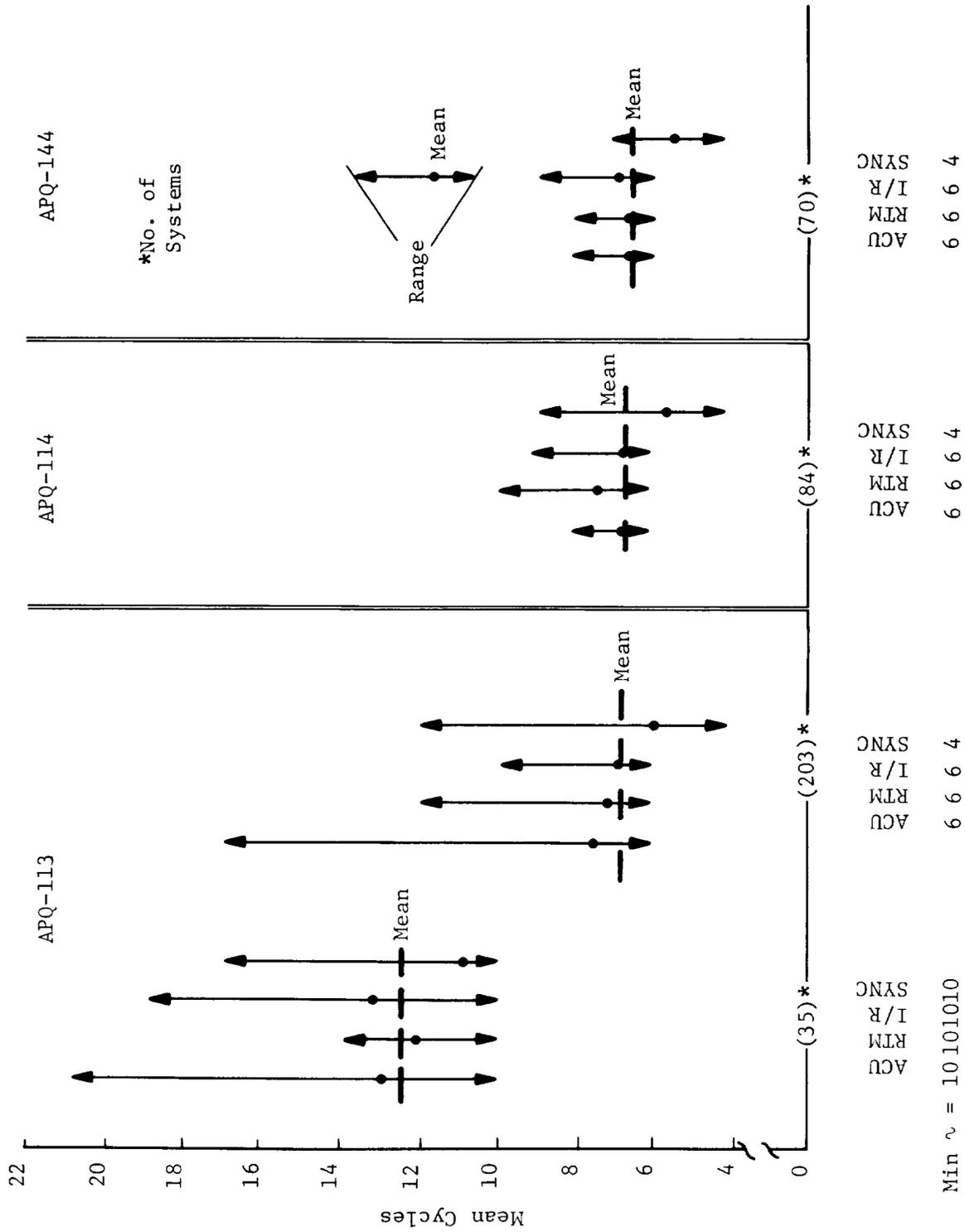


Figure 14 General Electric LRU Temperature Cycle Performance

June 1970 thru December 1971

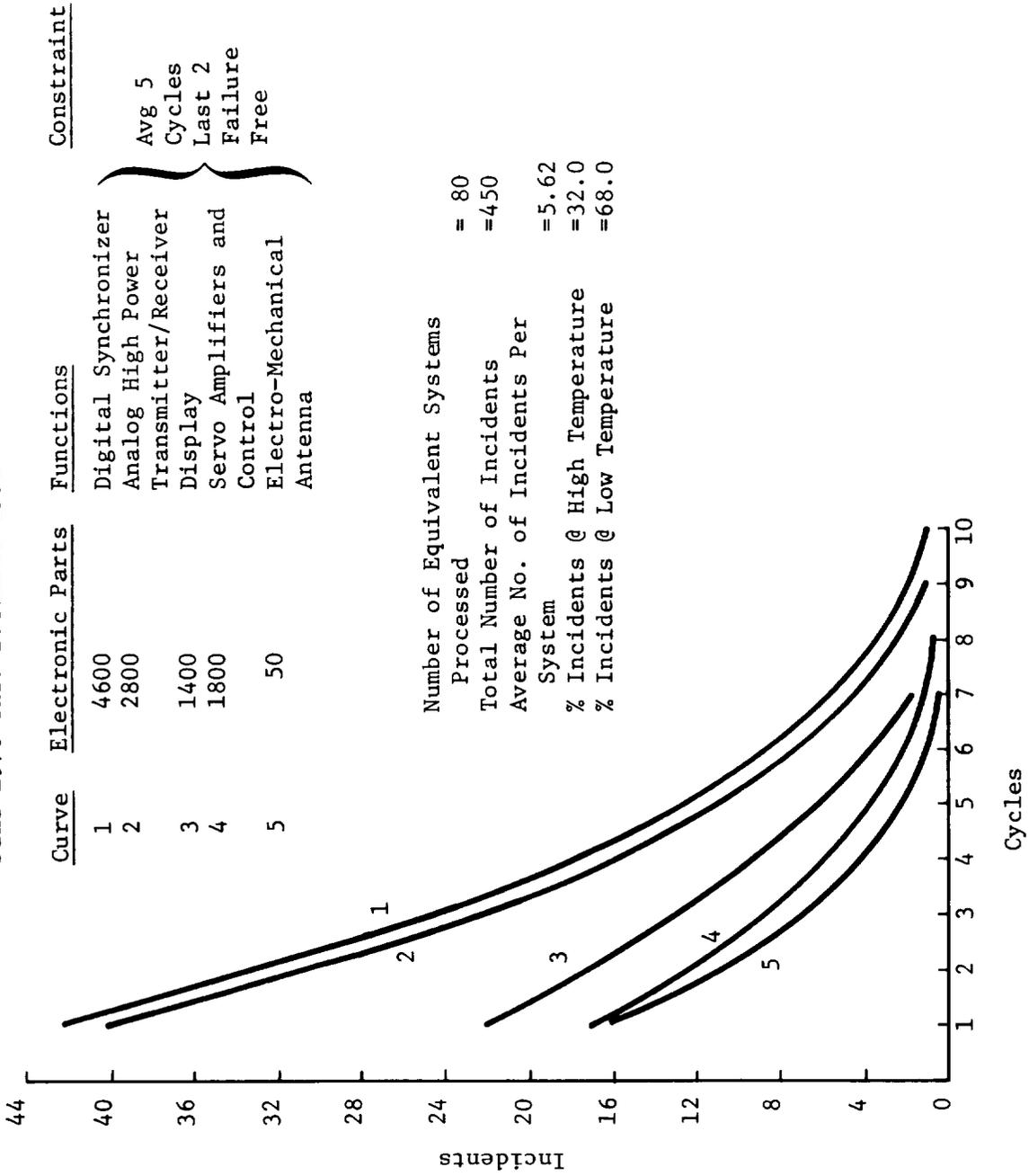


Figure 15 General Electric LRU Temperature Cycle Failure Distribution

Several other items of interest are also being considered at Lockheed by some programs. One is that all temperature cycles in the initial acceptance test would be completed prior to any repair of the box (unless the failure noted could damage other parts of the unit). This would be done in order to reduce the amount of repetitive rework. Another is that complete functionals would be required only in the last several temperature cycles in order to reduce cost. Monitoring of critical functions for failure would be accomplished in other temperature cycles.

The data presented on Tables 9, 10, and 11 and Figures 16 thru 21 were derived by Mr. Hill in his study of a major space program at LMSC which conducted a series of special tests, including additional temperature cycles, on nine different types of its complex communication and control equipment prior to flight. In this analysis, only those temperature cycles with differentials of 120°F to 160°F were included. (Thermal-vacuum system testing temperature cycling was not included since these do not provide significant temperature differentials on the equipment on this program.) Most temperature cycles included had 160°F differentials. All of the hardware used 100% screened Hi-Rel type electrical parts (that is JAN-TX or MIL-ER parts or parts with equivalent screening). Figures 16 thru 21 show the equipment temperature cycling failure rate (i.e., failures in temperature cycling divided by the number of units tested) as a function of temperature cycles. Figure 16 shows all communications and control equipment ranging in electrical parts count from 437 to 1419; Figures 17 and 18 show individual large components (electrical parts count of 4988 and 9822) while Figure 19 shows a combination of the two, and Figure 20 is a combination of all 9 equipment or unit types. The solid line is a smoothed least square polynomial fit of the data points shown on the curves. Two curves are shown for unit type 8 in Figure 18. The upper curve includes a group of failures attributed by the manufacturer to a selection of specific integrated circuit parameters due to a design sensitivity problem. Many of these integrated circuits were not analyzed so that the exact cause is unknown. The actual temperature cycle failure rate curve for this unit probably lies somewhere between the two curves shown. The data used for the lower curve was chosen for use in the combination curves of Figures 20 and 21.

Table 9 Lockheed Missile and Space Company Temperature Cycling vs Failure Yield

- Failure in temp cycling
- ATP or special test temp cycle
- No failure
- Troubleshooting temp cycle
- Not a new failure

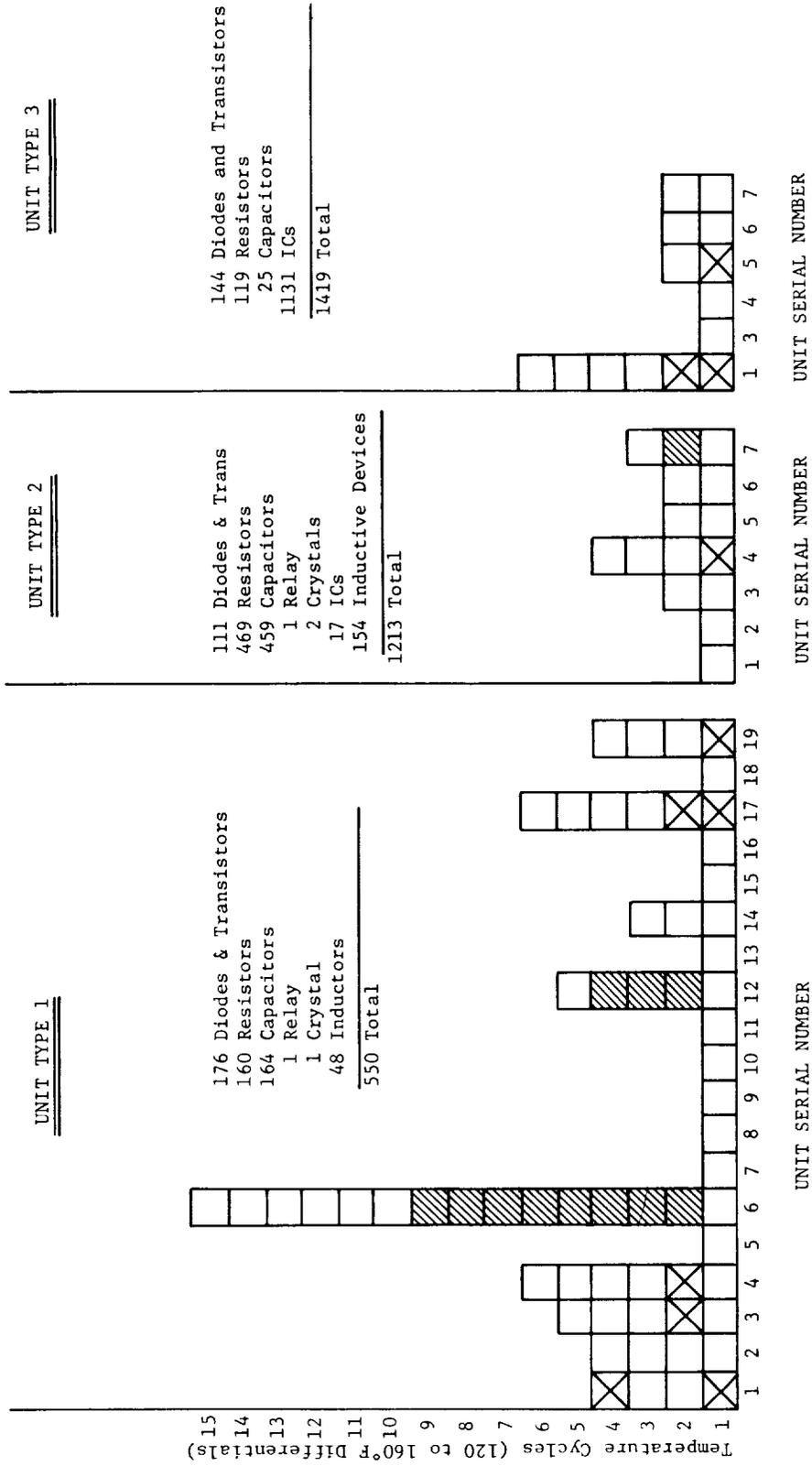


Table 10 Lockheed Missile and Space Company Temperature Cycling vs Failure Yield

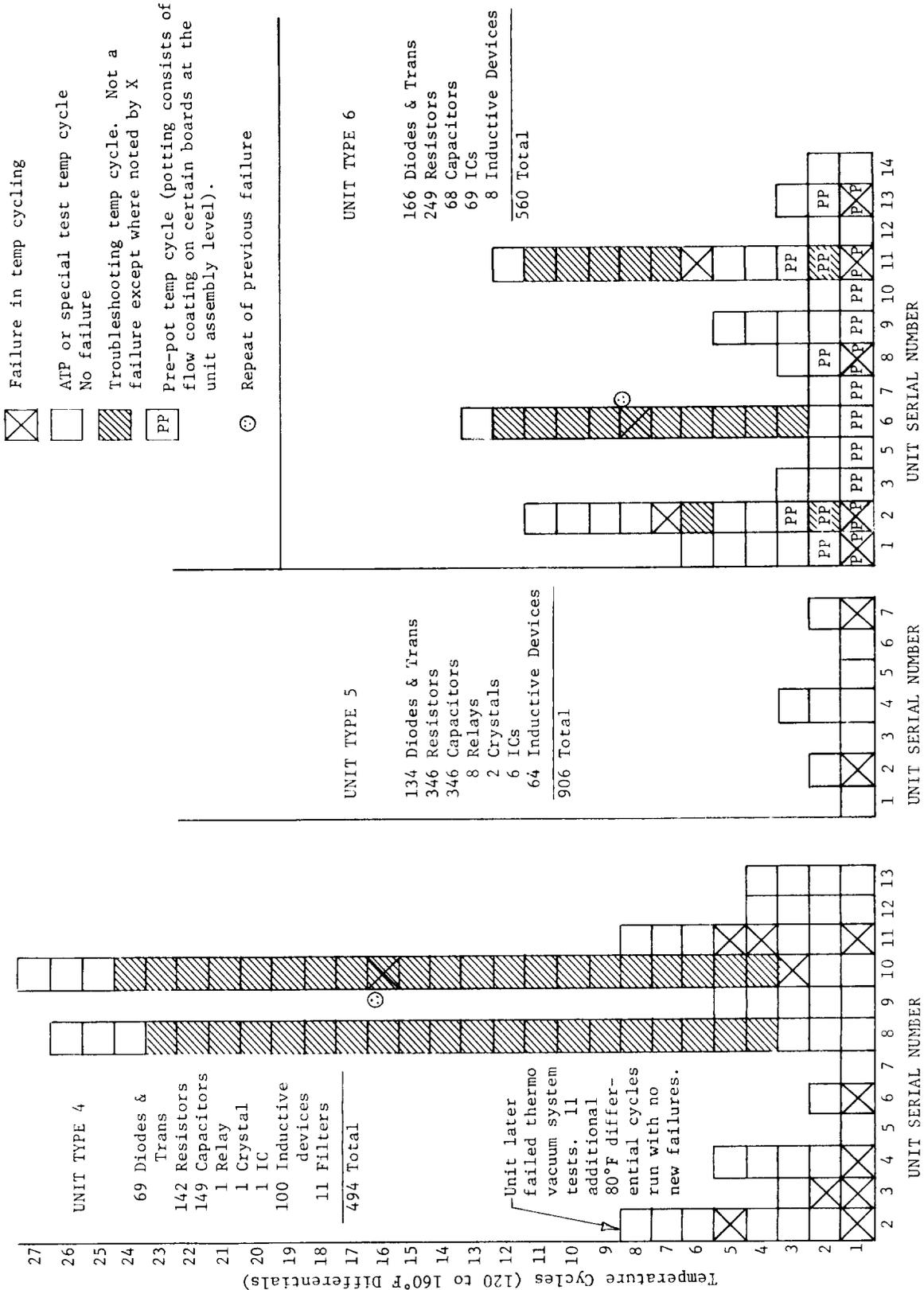
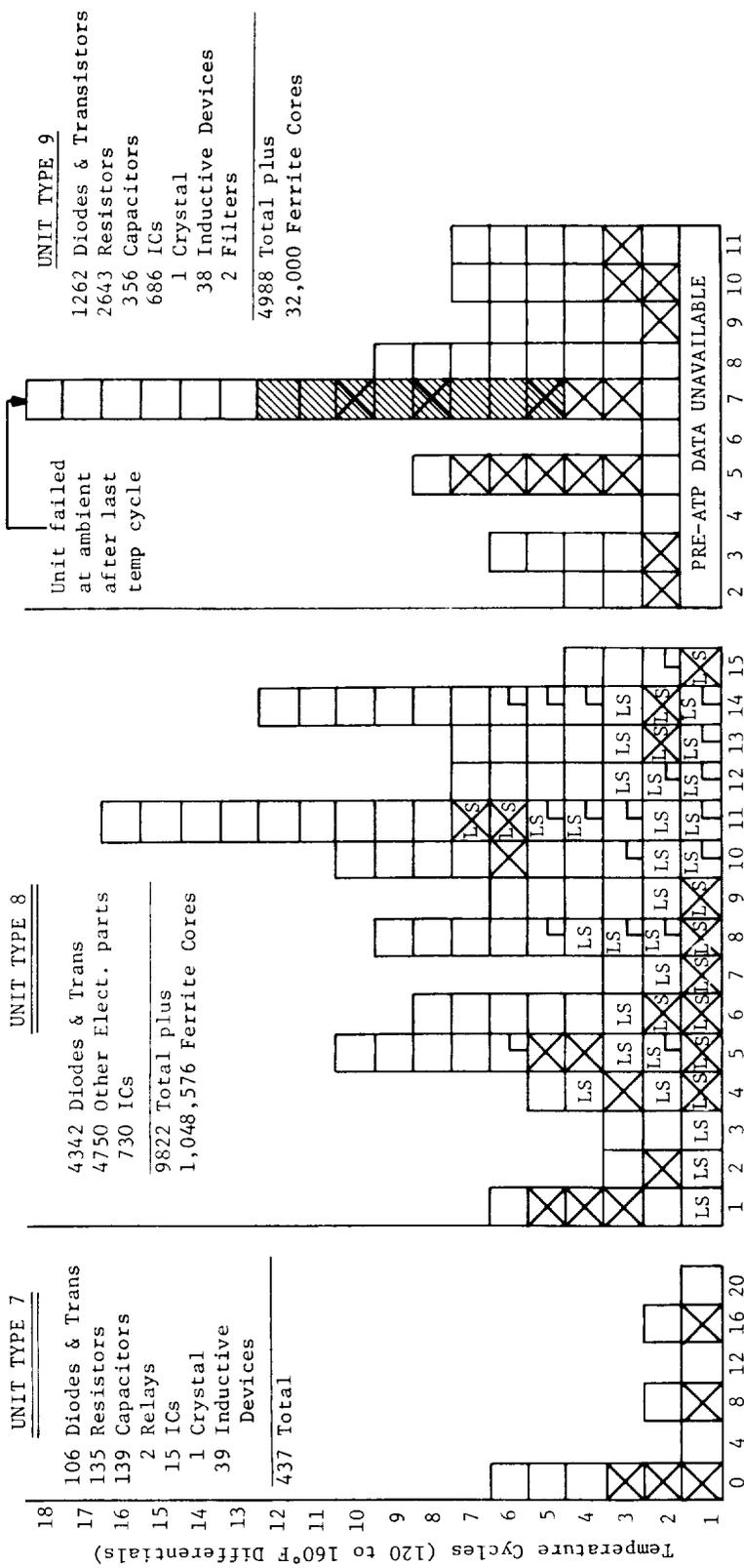


Table 11 Lockheed Missile and Space Company Temperature Cycle vs Failure Yield

- Failure in temp cycle
- ATP or special test temp cycle
- No Failure
- Troubleshooting temp cycle. Not a new failure except where noted by X
- Lab set temp cycle. Only workmanship or defective piece parts failures included where shown by X
- Failure in temp cycle. Most failures associated with IC parameter selection



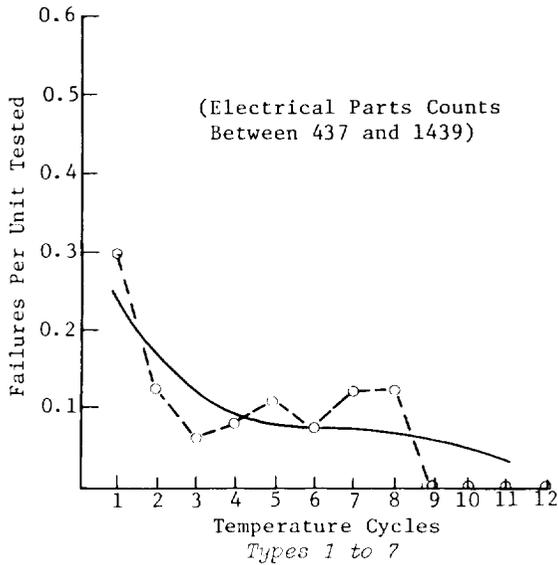


Figure 16 Temperature Cycling vs Failure Yield--Unit Types 1 to 7

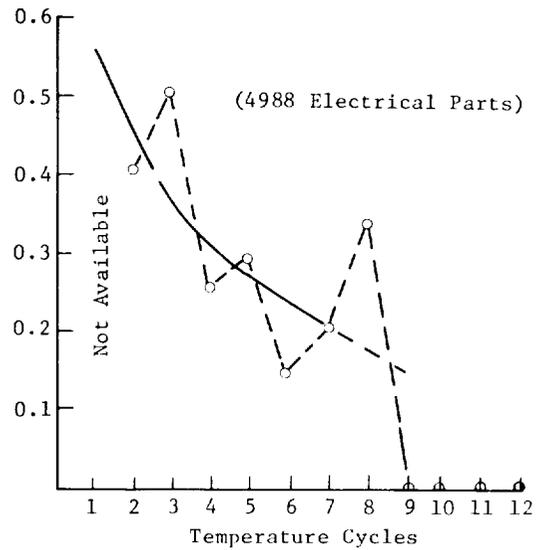


Figure 17 Temperature Cycling vs Failure Yield--Unit Type 9

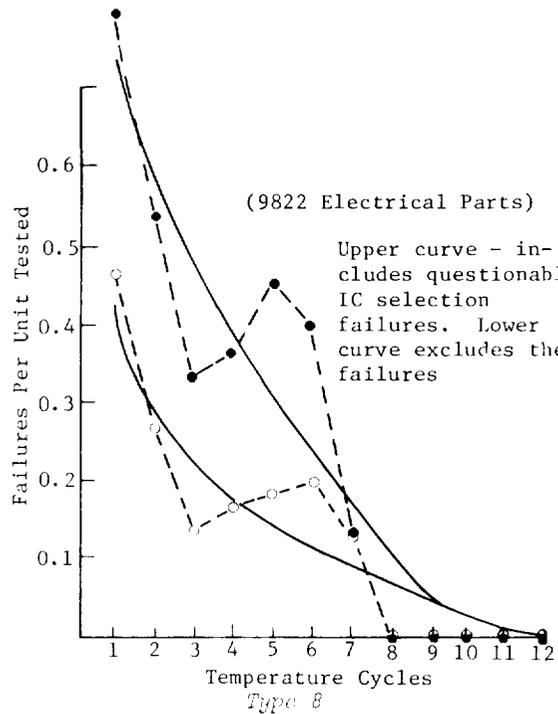


Figure 18 Temperature Cycling vs Failure Yield--Unit Type 8

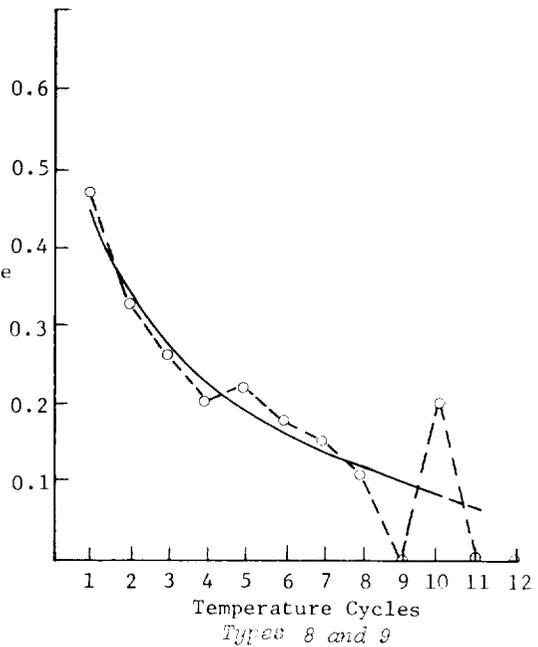


Figure 19 Temperature Cycling vs Failure Yield--Combination of Unit Types 8 and 9

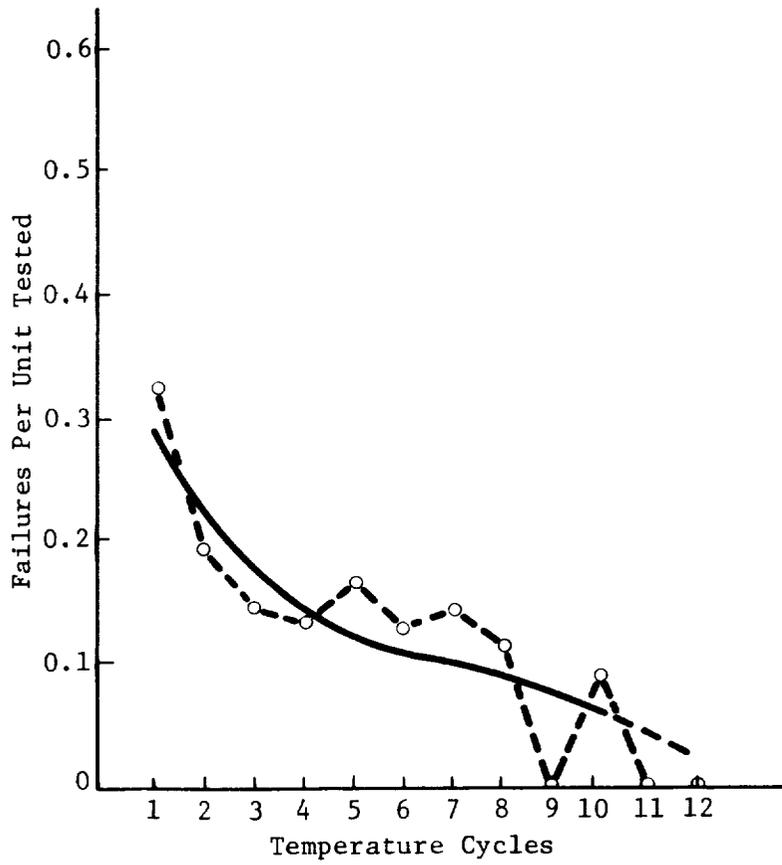


Figure 20 Temperature Cycles vs Failure
Yield-All Units 1-9

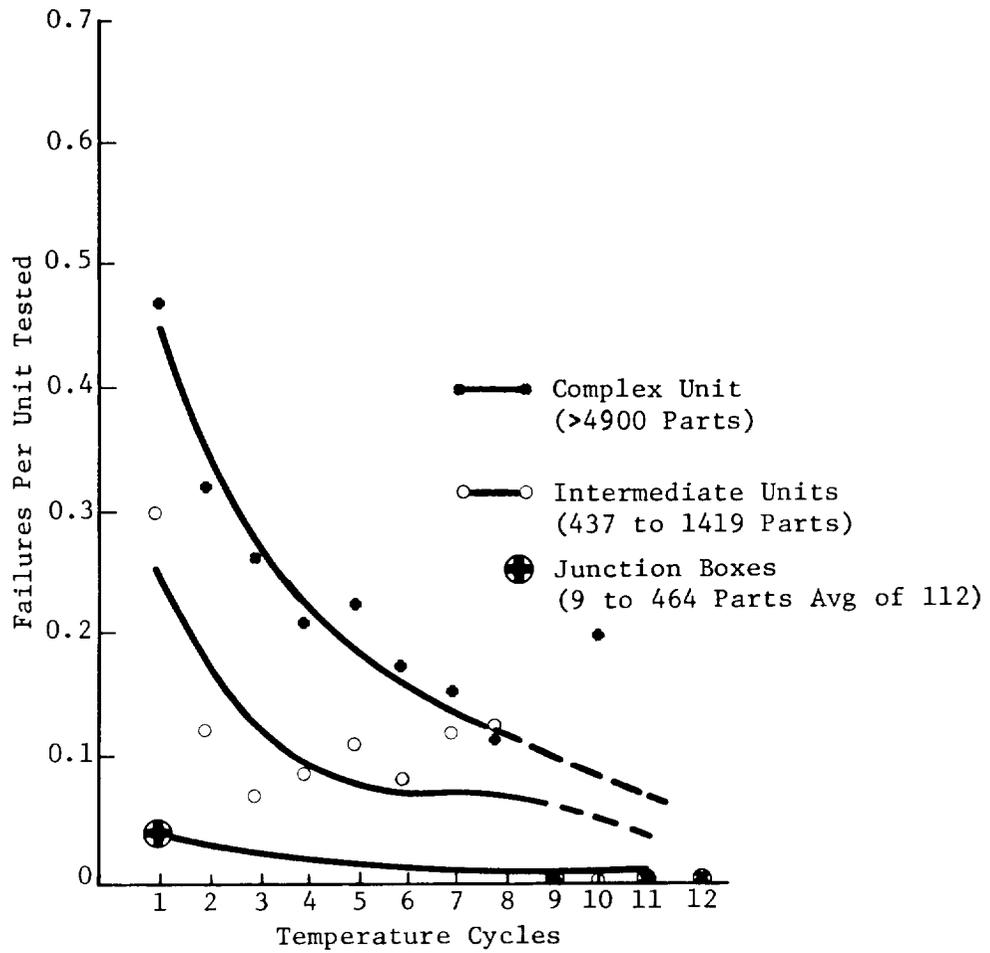


Figure 21 Comparison of Failure Rates by Unit Complexity

4. Boeing Company - Aerospace Group

Mr. J. E. Arnold provided the following data from their SRAM system, involving 7 articles, and a total complement of about 9500 electronic parts.

The SRAM Production Reliability Verification Test (PRVT) program was initiated at the start of production to ensure that a highly reliable and cost-effective weapon system was delivered to the Air Force. Fifteen CEI/ECC types of hardware are committed to this test program and, as of March 31, 1972, approximately 1,062 units of hardware have successfully passed the required tests.

Production Reliability Verification Testing is conducted in accordance with the requirements of MIL-STD-781B. Test Plan XXIX governs the test program and has been modified by contract to impose a single criterion for hardware acceptance: the completion of the specified test operating hours, failure-free. Fifty hours (12 cycles) of test operating time are specified for all articles of hardware except two. The environmental requirements of Test Level E of MIL-STD-781B are imposed on all tests of production articles. Each unit under test is subjected to thermal test cycles from -65°F to 131°F and receives 10 minutes of low amplitude vibration (2.2 gs) during each operating hour. The units are operated during the temperature rise portion of each cycle and during the high temperature stabilized period. Performance is monitored during the entire "On" period for proper operation. At the conclusion of a successful PRVT test period, each hardware unit must also pass successfully a functional acceptance test.

The Boeing Company supplies seven articles of SRAM Carrier Aircraft Equipment which receive PRVT. Six of these perform multiplex functions and one is a voltage regulator. These black boxes range in complexity from 143 electronic parts to about 2500 electronic parts, including over 700 integrated circuits. PRVT data from this group of equipment has been evaluated and composite results are shown in Figure 22.

Analysis of failures that have occurred during the PRVT program indicates that the primary failure-inducing factor is the temperature rate of change. The vibration environment (2.2 g) has almost no effect.

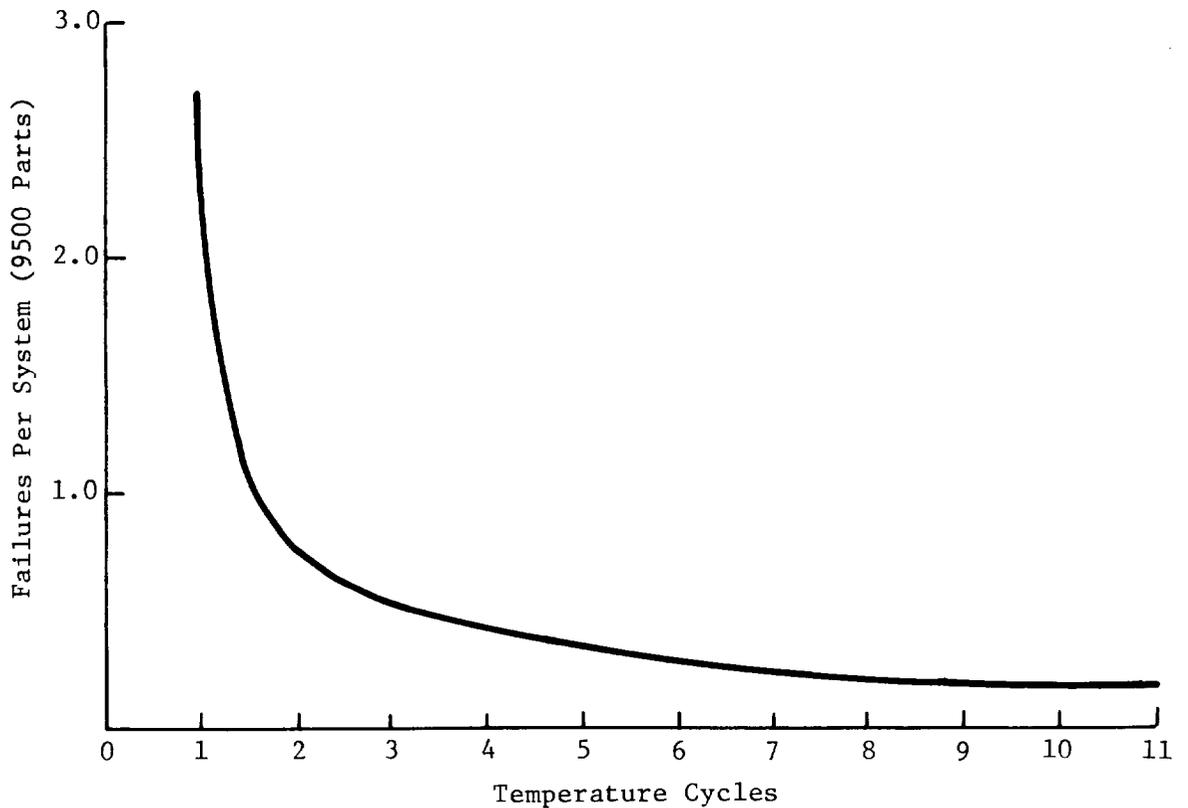


Figure 22 Boeing Company - Temperature Cycling vs Failure Yield

Mr. Arnold reports that in the early phase of the program about 80% of the failures involved workmanship, process, and people problems, but as the program matured, this decreased and, at present, about 50% are workmanship problems and 50% are problems with parts, principally integrated circuits. Hi-Rel parts are used in about 90% of the applications.

Mr. Arnold reports that 86% of the defects are detected in the first three cycles. However, if high reliability is the objective, then more than three cycles are desirable.

5. Hughes Aircraft Company

Mr. C. Ryerson reports that Hughes has developed mathematical models to predict how many temperature cycles are required to achieve a specified reliability depending on the previous amount of screening, the quality of parts used, and the exact thermal conditions and profile for the parts being screened. Many more than 10 cycles are sometimes required. They also adjust the number of cycles on the basis of the actual time-rate-of-change of the temperature in the most thermally isolated portion of the hardware. More cycles are employed when the rate of change is low due to the thermal mass of the hardware.

Ryerson emphasizes that the best screening is achieved by using the maximum safe range of component temperature and the *fastest* time-rate-of-change of hardware temperatures. Most parts will withstand temperature cycling with power off through a temperature range of -65°F (-54°C) to 230°F (110°C). Heat rise with power on under test cooling conditions should be calculated to limit the chamber temperature to a maximum safe value.

In previous spacecraft programs, such as Surveyor, tremendous stress was put on parts screening using methods such as Degradation Analyses (parameter drift) screening as developed at Hughes. In the current economic environment, where the part screening program is apt to be cost-constrained, other approaches have been developed and used, depending on the customer, such as the use of Jan TX parts, plus temperature cycling at both the PC board and black box level. On some programs, the screening of assembled PC boards consists of one week of rapid cycling in a chamber, during which time the boards accrue 158 temperature cycles. It has been found most cost-effective not to energize and functionally monitor the boards during the cycling.

A current paper by Ryerson, describing an integrated planning approach, is "Relating Factory Test Results to Field Reliability, Requirements for Field Maintenance and Total Life Cycle Costs," presented at the 29th Military Operations Research Symposium, Air Force Academy, Colorado Springs, Colorado, June 28, 1972.

6. Aerospace Corporation

Mr. Edward Clark has performed an independent survey and has concluded that, based on the Lockheed data, and other data, six to eight temperature cycles should be employed. Data on twenty-one transponders for a classified Air Force program was contributed by Mr. Clark, and is shown as Figure 23.

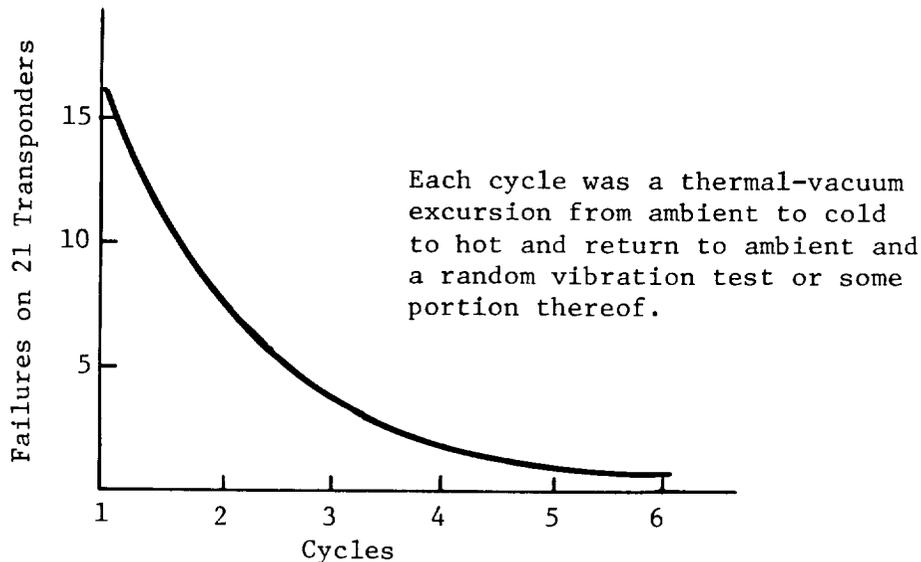


Figure 23 Aerospace Corporation - Temperature Cycling vs Failure Data on Twenty-One Transponders (Classified Air Force Program)

7. Decca Radar, Ltd.

This company manufactures marine radars in large quantities and has analyzed equipment reliability for over 16,000 ships.

In the early 1960's, a program to improve reliability was initiated. One of the features of this program was to adopt the AGREE procedure, essentially a demonstration of MTBF under environmental exposures. Many of the pre-production models are first submitted to the AGREE temperature cycling procedure as well as the first equipment off the production line. Thereafter, 10% of each month's output is tested. Each month the MTBF is measured to determine whether or not the quality of production is being maintained. Equipment are tested in batches of ten randomly selected from the previous week's production. The test involves 20 cycles and lasts for 500 hours. The temperature chamber is cycled daily from

5°F to 131°F and back to 5°F. Equipment is cycled on and off daily. After cold stabilization, the equipment is turned on and operated at 20% below nominal voltage. During the high temperature, the input voltage is set to maximum. Papers (Ref 5) by J. Harris and D. W. Sears detail the approach.

Mr. J. Harris of Decca Radar Limited has contributed the data, shown in Figure 24, to this study.

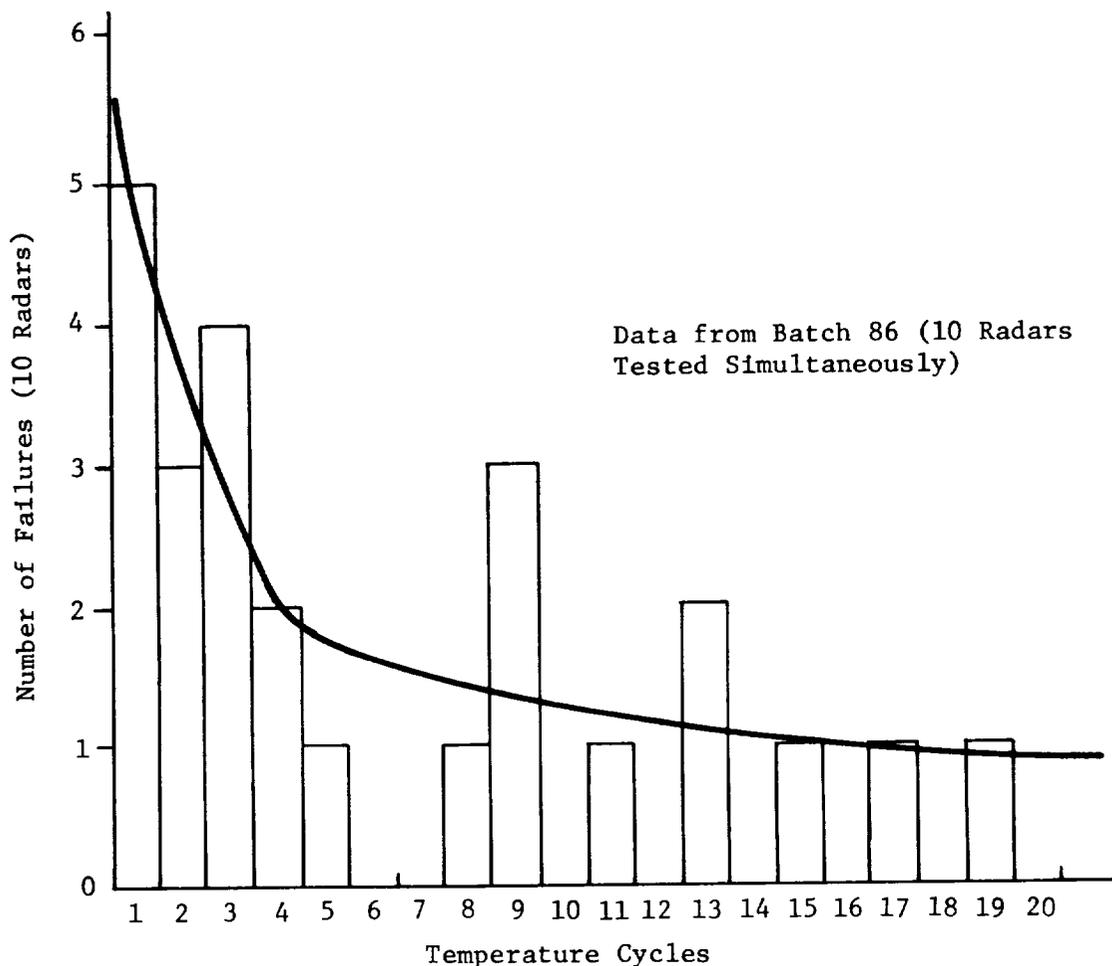


Figure 24 Typical Data from Decca Radar Limited, Illustrating Knee at Four to Six Temperature Cycles

Mr. Harris reports that most batches tend to show a knee in the staircase waveform although it is more pronounced in some cases than others. The position of the knee varies from batch to batch but certainly occurs between 4 and 6 thermal cycles.

Note that the failures tend *not* to be uniformly distributed. No failures were encountered on Cycles 6, 7, but 3 failures occurred on Cycle 9. This seems to be typical behavior rather than atypical, since the Lockheed data shows similar behavior. For example, Unit Type 8, Serial Number 1 (Table 11) survived the first two cycles, but failed in each of the next three cycles. This simply means that the defects in the hardware are not uniformly distributed with respect to degree of marginality. If a great number of defects existed, they would tend to be uniformly distributed, but since the defects constitute a small number, from a statistical viewpoint, they tend not to be uniformly distributed.

One statement excerpted from the papers by Harris and Sears is of interest:

"An interesting fact emerges when we survey the reliability of all our radars in service, many of which have been in service for 18 years, is that although equipments continue in service for many years, and like us get older each year, the reliability figure does not indicate an equipment wear-out period."

8. Motorola

Data submitted by Mr. M. Braman is presented in Table 12. The production test program for the APN receiver, radar augmentor, consisted of 22 eight-hour temperature cycles from -54°C to 71°C , and vibration of 2 gs, 24 hz, 10 minutes per hour. The device contained about 420 electronic parts and the sample size was 370 devices.

Table 12 Motorola Temperature Cycling vs Failure Data

	<u>After 3 Cycles</u>	<u>After 6 Cycles</u>	<u>After 9 Cycles</u>
Failures (Total)	46	23	15
Failures/Unit	0.12	0.06	0.04
Types of Failures			
Diodes	5	6	5
Microwave Diodes	6	5	1
Transistors	17	4	4
FET's	1	0	0
Tantalum Capacitors	1	2	1
Integrated Circuits	4	0	0
Diode Attenuators	2	0	1
Workmanship	3	2	1
Unknown	7	4	2

9. Honeywell Incorporated

Mr. Ken Brackney submitted the following data, pertaining to a tape recorder program for the U. S. Navy. The contract was initiated in 1967 and currently, about 150 devices are in the field. Integrated circuits and transistors are burned-in for 168 hours, but without environmental screening. Assembled PC boards are then given 20 temperature cycles from -80°F to 185°F using 9°F per minute AGREE chambers, and with PC boards not energized. The final completed units are subjected to 4 pre-acceptance test cycles and 8 acceptance test cycles from -13°F to 131°F. Since their contract requires a final 50 failure-free-hours, test failures occasionally necessitate an extension of the test period, such that the average delivered tape recorder has received about 14 cycles (in addition to the 20 cycles at the PC board level). This represents a total of 34 temperature cycles. Since the equipment anomalies are manifest during the temperature ramps, long soak times at temperature are not deemed particularly beneficial.

During temperature cycling, the assemblies are also given 2 g's peak vibration for 10 minutes in each hour. This vibration exposure is not producing any significant failures, but is being continued since it is contractual.

Mr. Brackney estimates that about 60% of the failures screened out by the test program are part failures, about 40% are workmanship defects or are unclassifiable.

This temperature cycling acceptance test program was initiated without extensive prior use of temperature cycling either in development testing or in Qualification Testing. As a result, problems were encountered when the acceptance test program was first initiated, but these problems were successfully resolved. Some of the problems encountered were the cracking of glass diodes and other "weak" parts due to the difference of thermal expansion coefficients with the polyurethane conformal coating, cracking of resistor coatings, and failure of a fine wire attached to a larger wire inside a crystal can relay. This latter problem necessitated two vendor changes.

10. Radiation Incorporated

Radiation has used several approaches to temperature cycling, with variations largely dependent on customer specifications and the type of equipment. On unmanned spacecraft programs of the OAO, Nimbus and ERTS class, two or three cycles between the design temperature extremes were accumulated during acceptance testing; at least one cycle of the test program acquired during thermal vacuum testing in accordance with customer specifications. In general, boxes tested at Radiation for these programs were subsequently subjected to the GSFC cycling practices at subassembly and spacecraft levels as discussed in the preceding paragraph.

On several military avionics programs, AGREE techniques have been applied at both box-level screening and reliability demonstrations. One of these programs requires 20 consecutive failure-free cycles in accordance with Test Level E of MIL-STD-781B (-54°C to 55°C) prior to shipment. This is a relatively simple equipment consisting of less than 200 electrical parts, and the total failure rate is sufficiently low to permit this approach.

For more complex equipment, Radiation's experience on the AN/ASW-25 Digital Data Communications Set is an interesting case history. This equipment is the essential data link in the Navy All-Weather

Carrier Landing system and has a reliability requirement of a minimum 1000 hour MTBF (one failure or less in 1000 hours of testing). Contractual requirements dictated that all systems be tested for 100 hours (16 cycles) of formal demonstration in the environment of Test Level E of MIL-STD-781. The results of such testing on each month's production constituted a single test in which the minimum requirements were to be demonstrated.

The initial approach was to conduct a "manufacturing run-in test" (MRIT) of up to 24 hours at bench ambient conditions prior to submitting the units to the formal demonstration tests. Early in the program, tests on 234 systems demonstrated an MTBF of 259 hours. Part failure rates in these early demonstrations were considerably higher than those predicted using MIL-HDBK-217A, and the first step toward reliability improvement was to replace I.C.'s having gold-to-aluminum bonding systems. MRIT was also increased to 75 hours. Subsequent tests on equipments with these improvements resulted in an MTBF of 327 hours.

At this point it was noted that the initial test systems demonstrated a much higher reliability when failures from the first reliability tests were repaired and the units retested. Limited data from some of these systems resulted in an MTBF in excess of 1200 hours. As a result, a preconditioning program of a minimum of 75 hours (12 cycles) of Test Level E testing was instituted on all equipments, and the MTBF of several subsequent demonstrations continued to exceed 1200 hours. It was theorized that extending the preconditioning period would lead to further demonstrated reliability improvement by eliminating additional "infant mortality" failures. This was confirmed by demonstration testing of systems with a minimum of 100 hours (16 cycles) of preconditioning, and by further tests after 200 hours (32 cycles) of preconditioning. Initial tests under these conditions demonstrated MTBF's in excess of 1500 and 1700 hours respectively. At the present time, the 200 hour preconditioning period has been adopted as a standard, and systems having this testing have subsequently demonstrated a cumulative MTBF of 1692 during 140,671 unit-hours of testing. The cumulative MTBF of all systems since the 75 hour preconditioning began is 1527 hours during 209,644 unit-hours of testing.

A curve to show the approximate average MTBF as a function of the number of cycles of preconditioning prior to demonstration is shown on Figure 25. As in all statistical tests, individual test results may have varied somewhat from the curve. The data starts at 12 cycles because data is limited below that point. The reader is cautioned not to extrapolate the curve for fewer than 12 cycles because of the lack of confirming data for short periods of preconditioning. The salient observations are that preconditioning provides the means for the AN/ASW-25 equipment to:

- 1) Achieve specification requirements.
- 2) Realize further reliability improvement by additional preconditioning.

When Hi-Rel screened parts are used, fewer than 16 to 25 cycles seem to be appropriate. In one program supplying multiplexers containing Hi-Rel parts to the Minuteman Program, it was found that 10 temperature cycles were sufficient since there were very few failures after that point.

Mr. T. M. Barlow of Radiation's Reliability Engineering Section recommends the following guidelines for temperature cycling:

- 1) Longer periods of cycling should be considered for equipment using standard military parts than for those using screened or "hi-rel" parts. Sixteen to 25 cycles are recommended for equipment containing unscreened MIL-Spec parts and about 10 cycles are appropriate for equipment containing Hi-Rel parts.
- 2) Cycling is effective in determining weaknesses of soldered connections. It is more useful on this construction than on welded assemblies.
- 3) To minimize repair and rework costs during the test program, ease of maintainability is essential on equipment subjected to stringent temperature cycling.

Reliability Improvement
of AN/ASW-25

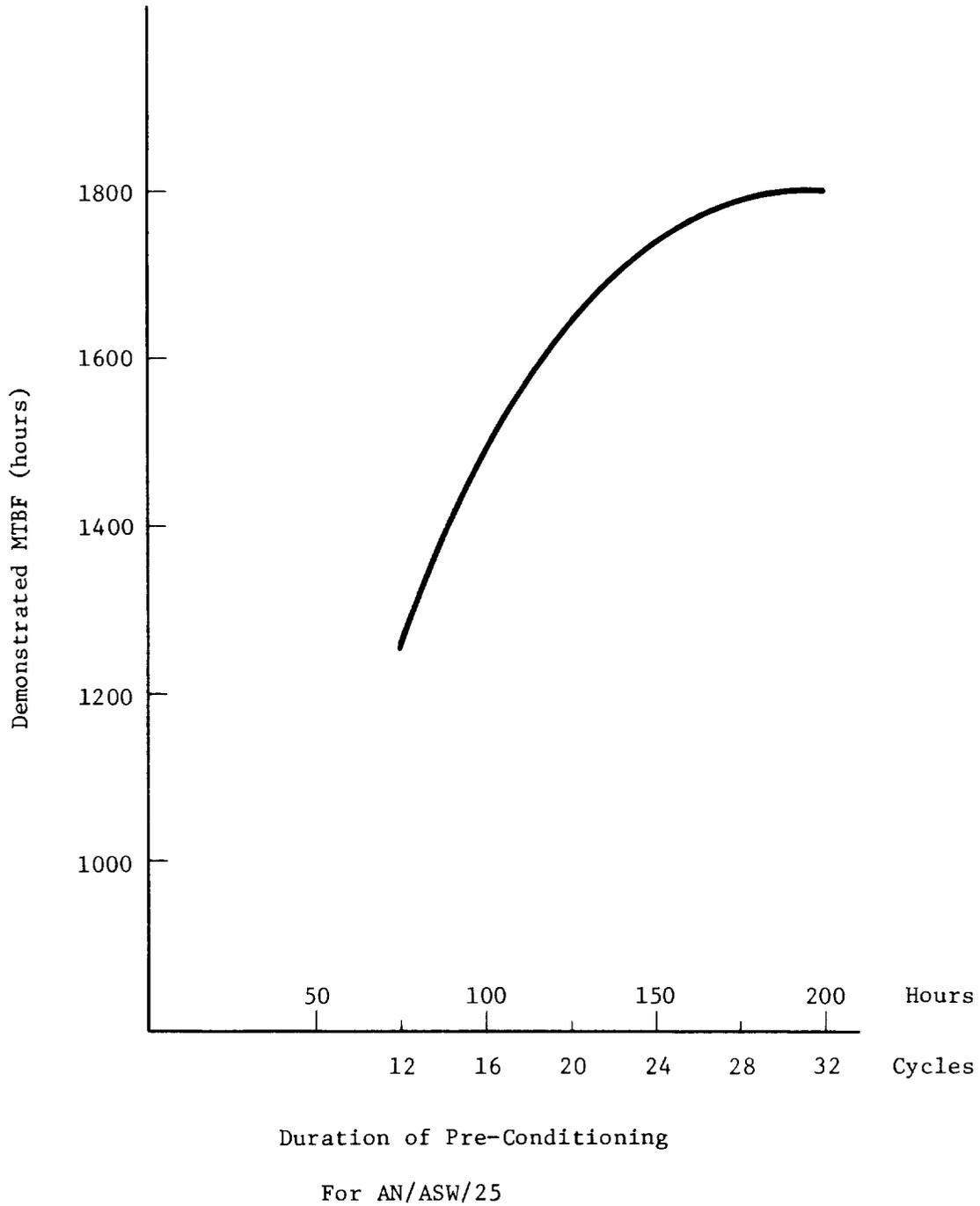


Figure 25 Radiation Incorporated - Temperature Cycling vs Reliability Improvement

11. TRW Systems

Mr. Ron Hoover reports that TRW has employed one thermal cycle at the black box level. During spacecraft thermal-vacuum system testing, another 5 or 6 cycles are accumulated. The black box test is generally 12 hours at the low temperature and 12 hours at the high temperature, with temperatures a function of the specific spacecraft design and mission. A vacuum of 5×10^{-5} Torr is used. The systems test is nominally about 10 days. The temperature ramps require about 10 to 12 hours with functional testing conducted at the high and low temperature plateaus.

The above practice is presently being modified by current studies at TRW and also by the data herein, exchanged during the Long Life Assurance Study. In a very recently contracted classified spacecraft program, TRW, in consonance with the Air Force, adopted an environmental acceptance test program for the "black boxes" consisting of vibration and eight temperature cycles, using the steepest temperature ramps allowed by the test chambers. The last two temperature cycles are required to be failure free. Margins of 10°F were employed between acceptance and qualification, with the temperature ranges in the order of 100 to 150°F . The range for acceptance testing were somewhat constrained because the qualification temperatures were already established.

12. Goddard Space Flight Center

The nominal practice is to employ thermal vacuum testing at three levels of assembly. Black boxes are tested for 24 hours hot and 24 hours cold, subsystems are tested for 40 hours hot and 40 hours cold, while the entire spacecraft receives 2 cycles: 12 hours hot, 12 hours cold, then 40 hours hot and 40 hours cold.

Where spacecraft shadowing effects are present, the above approach is augmented by the addition of a 3 hour cold soak. With equipment operating at over 200 volts, the test times are lengthened for the black box acceptance test to assure corona and arcing problems are detected. Subsystem spares are given longer exposure to hot and cold conditions to compensate for the fact that they will not receive the higher level assembly testing. A gross summarization of this approach is that black boxes receive about 4 thermal cycles, but only one cycle at the black box level.

13. Hewlett-Packard Co.

Mr. Ted Dennison reports that their product line is primarily commercial, but even so, they have initiated an experimental burn-in program at the black box level as a reliability improvement measure which they felt necessary because of the increasing complexity of their equipment. The burn-in is conducted for 7 days at 131°F, and is currently being done on every other production unit to acquire field failure data on the effect of the burn-in. They have also been studying the application of thermal cycling and may adopt a program of about 4 cycles per day for 4 days (16 cycles), from 32°F to 131°F. The selection of 32°F rather than a lower temperature is based on their existing temperature chamber capability but is reasonable for commercial equipment and its intended environment.

An interesting feature of their *development* test program approach is that they employ a type of step-stress temperature cycling test in which the equipment first receives four cycles from 0 to 40°C, then four cycles from -10 to 50°C, four cycles from -20 to 60°C, and then four cycles from -30 to 70°C, for a total of 16 cycles. In this approach, the relative seriousness of each failure mode is established and better decisions regarding the scope of the corrective action can be made.

Also, in development testing, prototypes are burned in for successive periods at 16 hours, starting at 50°C, then at 60°C and so forth until 100°C is reached, or until some constraining limit is reached for the specific hardware being tested.

14. Bendix Corporation

Miss Peggy Gogin reports that Bendix has employed AGREE type temperature cycling using 4 cycle and 6 cycle programs for the acceptance testing of production hardware. She reports that on another program, using the AGREE 2g vibration only, no failures were encountered and feels that the benefits of the AGREE cycle lie in the temperature ramps, rather than the soak time at high and low temperature, or the vibration. Miss Gogin recommends six temperature cycles for future programs and cautions that the packaging design must be adequate. Rigidly potted cordwood modules and conformally coated glass parts were cited as hazardous.

15. Westinghouse - Aerospace Electrical Systems

Mr. Earl Bruns reports the current practice is one cycle. His opinion is that for long-life space missions, it may be desirable to increase this to 3 or 4 cycles. They employ soak times of 4 hours after temperature stabilization.

16. Martin Marietta Aerospace, Denver Division

The past policy has been to employ 1 temperature cycle in black box acceptance, with a temperature range of at least 100°F. On the Titan Program, some black boxes are receiving less than 100°F, but because of the use of potted cordwood modules, there is reluctance to increase the severity of the temperature cycling program unless additional hardware can be procured and tested to prove that greater ranges and more cycling can be safely implemented without decreasing the yield during acceptance testing and initiating redesigns. This situation arose because, like the Apollo program, the temperature cycling program was initiated after the qualification test program was completed.

On new programs, six to ten cycles are now being recommended, together with temperature ranges exceeding 100°F, such as 160°F.

17. Barnes Engineering Co., Defense and Space Division

Temperature cycling varies with customer requirements but they feel 2 or more cycles are necessary for the detection of workmanship defects. Temperature cycling is sometimes combined with burn-in testing for 96 to 105 hours.

18. Delco (A.C.) Electronics

Mr. Bill Nelson, Apollo Reliability Program Manager, believes that the number of temperature cycles should be varied in accordance with the type of black box and the environment in which it is to be used. In general, he recommends 5 cycles for black boxes and 20 cycles for components. It is believed that time-at-temperature is not of major significance since the failures occur during the temperature ramps. He has experienced little degradation from temperature cycling except in the small wire sizes used in electromechanical equipment and motors. He emphasized the importance of eliminating No. 51 and No. 52 gage wire.

The rate of temperature change should be slow enough to detect intermittent changes, such as -20°F to 120°F in 1 hour.

19. Raytheon - Equipment Division

Mr. Sheffret believes one cycle is not adequate and recommends a minimum of 5 cycles. Nominal temperatures in use are 32°F to 160°F, with one cycle requiring 9 to 10 hours, with a soak time at temperature of 1 hour minimum. On some programs temperature cycling is combined with a burn-in test.

20. Sandia Corporation

Mr. J. F. Calek reports that Sandia employs both temperature shock and temperature cycling. Temperature cycling is often used during component development to verify designs. It is also used on occasion for screening purposes in certain production problem situations. The number of cycles is a variable depending on test objectives.

With regard to temperature cycling, Mr. Calek is leaning toward 3 to 5 cycles, at nominal temperatures of -65°F and 160°F. Engineering judgment, past experience, end-item requirements, and development test instrumentation results are combined to define the temperature cycling profile for production acceptance purposes. This tends to have most impact on rise and soak times, rather than the temperature range or the soak time.

21. RCA - Astro-Electronics Division

A paper by Mr. Louis Gomberg is of considerable interest (Ref 6). This paper described a study toward improving the cost-effectiveness of spacecraft test programs, and is briefly abstracted herein: In 1967, test program failure histories were studied for Relay I, Relay II, Lunar Orbiter, RAE, and a classified program. The detailed data from Reference 7 shows that most of the failures encountered in thermal-vacuum testing were precipitated by temperature and would not have required a vacuum to evidence the failure. For example, on Lunar Orbiter, 260 failures occurred in thermal-vacuum but only four required vacuum to evidence the failure. Accordingly, it was concluded that thermal-vacuum testing of *all* black boxes, at the Black Box level, should be discontinued and additional temperature cycling substituted. The recommended approach is to analyze each hardware item and to impose thermal vacuum testing only on those items deemed sensitive, by analyses, or prior experience. Such items, usually restricted to high power transmitters, bearing devices with labyrinth seals, and mechanical devices with exposed moving parts, represent less than

10% of the total population. Most of the electronic hardware, batteries, and hermetically sealed devices are not thermal-vacuum tested at the black box level, but do receive temperature cycling. Currently, most of the hardware receives three temperature cycles at the black box level plus an additional three cycles during the system-level thermal-vacuum testing.

Mr. Gomberg reports that this more cost-effective approach was proposed to the Air Force as a Value Engineering Change, was adopted, and has proven successful on a classified Air Force program.

22. Marshall Space Flight Center

Mr. Duane N. Counter of the Astronautics Lab strongly emphasizes the use of temperature cycling on the development and qualification test hardware to prove proper electronic packaging. MSFC has conducted very extensive investigations on the control and elimination of solder joint cracking and all the aspects of stress relief bends, solder joint configurations, conformed coatings, potted modules, PC boards, thermal expansion of parts, etc. Because of this experience, Mr. Counter emphasizes the very extensive use of temperature cycling to verify the packaging during the development and qualification test programs, but cautions that production hardware subjected to excessively severe thermal cycling may induce wearout failure modes, the solution of which may over-penalize the design.

Mr. Counter recommends that on future spacecraft programs, the number of cycles should be increased beyond one or two, but emphasizes that the temperature cycle must be *realistically* established and should not over-penalize the design, remembering that each packaging design must be proven to be free from wear-out failure modes. This proof is acquired during development and qualification testing.

23. Grumman Aircraft Engineering Co.

Mr. Ralph Esposito participated in the formulation of the Apollo acceptance test program on LEM. While most equipment received $1\frac{1}{2}$ cycles, some selected equipment received a greater number of cycles. Defects were revealed on the second, third, etc, cycles, and Mr. Esposito feels that four to six cycles is much preferable to $1\frac{1}{2}$ cycles. He mentioned that the selection of a more stringent Apollo approach would have had costly requalification test program impacts, since the acceptance test program was finalized

after the Apollo fire and after much equipment had been qualified. He emphasized the importance of using the Qualification Test to demonstrate the capability of the equipment to undergo thermal cycling acceptance testing without degradation.

Mr. Esposito also stressed the importance of very close functional monitoring during the temperature ramps and felt that the 1 hour soak time at temperature could be reduced since equipment anomalies are evidenced during the ramps and seldom during the 1 hour soak period at temperature.

Grumman is currently conducting a company funded study with the objective of optimizing acceptance test methods.

24. Texas Instruments

Mr. William Brown reports that they frequently use the AGREE approach. From two to twelve cycles are employed, with the number of cycles dependent upon the particular equipment and the particular contract. In one program, a complex avionic package, half the units were given 12 cycles. The additional 6 cycles proved to be beneficial, and 12 cycles were adopted. On another program involving radar equipment, 3 pre-acceptance cycles and 4 acceptance cycles were employed. On contracts not requiring temperature cycling, it is common practice to still employ 2 to 4 cycles as a cost-effective approach for reducing field problems. For example, the expenditure of \$30,000 for the testing of 12 systems is postulated to save more than \$30,000 in reacting to field problems. Mr. Brown reports that the trend of their customers is toward increased temperature cycling.

Regarding the relative effectiveness of the 2g vibration exposure, Mr. Brown feels that 90 to 95% of the failures are due to the temperature cycle.

With regard to the relationship between Hi-Rel parts and the number of temperature cycles used, the approach, when high reliability is required, is to increase *both* the part screening program and the number of temperature cycles used. In other words, the use of Hi-Rel parts is not used as a rationale for decreasing the temperature cycling program.

Nominal temperatures employed are -65°F and 131°F. Longevity tests for MTBF demonstration are also conducted when required by the contract. One such program involves testing 3 units, 3000 hours each (about 360 cycles each).

25. JPL

Mr. Jerry Swanson reports that past programs have emphasized thermal vacuum testing at the systems level, but not temperature cycling of black boxes at ambient conditions. However, there is considerable interest in this at JPL, and Mr. Swanson is reviewing past hardware problems to determine if temperature cycling would have been beneficial. He envisions that temperature cycling will receive greater utilization in future programs. Some testing may be accomplished to aid the development of their temperature cycling policy.

26. Supplier A

On contracts involving small quantities (5 or 10 units) of hardware, a minimum of one temperature cycle is employed. The nominal range is -55°C to $+55^{\circ}\text{C}$. On production contracts involving large quantities, such as 50 articles, from 12 to 20 temperature cycles are used. This difference in approach is due to several factors:

- 1) The small build contracts are executed in an environment of extreme emphasis of process control and workmanship.
- 2) On production contracts involving larger quantities of hardware, the economic consequences of hardware returned from the field for rework would be severe and justify stringent screening prior to delivery.
- 3) The production contracts can better afford extensive temperature cycling.

The engineer consulted recommended 5 cycles as a good nominal choice for the Hi-Rel manned spacecraft of the future.

It was felt that soak time at temperature was not important and the next temperature ramp can be initiated when the equipment (internally) reaches the desired temperature.

In the various contracts being implemented by Supplier A, burn-in times of 50 to 250 hours are also employed in black box acceptance testing. It was also felt that temperature cycling does not degrade the equipment. Thermal vacuum and vibration are also employed in acceptance testing, and their experience is that temperature cycling was more productive than vibration in screening out equipment weaknesses.

Another engineer commented on the susceptibility to failure in temperature cycling of plastic encapsulated parts and small wire gages (less than No. 40) in motors, transformers, and other electromechanical devices.

27. Supplier B

This supplier of guidance systems and the associated complex electronics is currently supplying equipment in rather large volume to a military user. The acceptance test includes a confirmation of functional performance at both high and low temperatures and so in effect, they are employing one temperature cycle. However, due to very stringent performance requirements and the need for matching and selecting parts to achieve the performance requirements, one unit may receive 6 to 8 temperature exposures. On this same program, sample equipment are also selected from the monthly production. Some of these are subjected to 28 "slow" 18 hour temperature cycles from -40°F to 120°F. Another test is also employed in which the equipment is rapidly transferred between two chambers at -65°F and 165°F, with 4 hours in each chamber. This latter test, more rapid, has been found to be much more effective in detecting potential problems and failures. Based on this experience, the cognizant engineer at Supplier C recommended one "rapid" temperature cycle for 100% production acceptance testing.

G. LIST OF COMPANIES/AGENCIES/PERSONNEL SURVEYED

Collins Radio Co., Cedar Rapids, Iowa. Mr. R. L. Vander Hamm and Mr. James Rutledge. (319) 395-1000 ext 2667.

Grumman Aircraft Engineering Co., Bethpage, Long Island, New York. Mr. Ralph Esposito. (516) LR 5-9176.

Honeywell Incorporated, Englewood, Colorado. Mr. Ken Brackney. (303) 771-4700 ext 806.

Lockheed Missiles and Space Co., Sunnyvale, California. Mr. Charles E. Leake, Dept 62-05. P.O. Box 504, Bldg 104. (408) 742-0824.

Boeing Co., Seattle, Washington. Mr. James E. Arnold. (206)
773-2662.

Hughes Aircraft Company, Aerospace Group, Culver City, California.
Mr. Cliff M. Ryerson. (213) 391-0711 ext 4622.

Motorola Co., Scottsdale, Arizona. Mr. Maurice Braman.
(602) 949-3033 ext 2792.

Delco (A.C.) Electronics Division of G.M., 7929 S. Howell Ave,
Milwaukee, Wisconsin. Mr. William Nelson. (414) 762-7000
ext 2939.

Raytheon-Equipment Division, 190 Willow St, Waltham, Massachusetts
02154. Mr. E. Sheffret. (617) 899-8400 ext 248.

Sandia Corporation, Albuquerque, New Mexico. Mr. J. K. Calek.
(505) 264-4546.

Decca Radar, Ltd., Croydon, Surrey, Great Britain. Mr. J. Harris
and Mr. D. W. Sears.

Westinghouse - Aerospace Electrical Systems, Lima, Ohio. Mr. Earl
Bruns. (419) 224-0121 ext 4147.

Hewlett Packard Co., Palo Alto, California. Mr. Ted Dennison.
(415) 493-1501 ext 2172.

JPL, Pasadena, California. Jerry Swanson, Mail No. 233-201.
(213) 354-2344.

TRW Systems, 1 Space Park, Redondo Beach, California. Mr. Ron
Hoover, Bldg M-1, Room 1531 (213) 536-2533; Mr. Robert Schedvin,
Bldg R-5, Room 1230 (213) 536-2566.

Goddard Space Flight Center, Greenbelt, Maryland. Mr. B. C.
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General Electric Company - Aerospace Electronics, French Road,
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Radiation, Inc., Melbourne, Florida. Mr. T. M. Barlow. (305)
727-5028.

Martin Marietta Aerospace, Denver Division, Denver, Colorado.
Mr. R. W. Burrows. (303) 794-5211 ext 2325.

Bendix Corporation, Teeterborough, New Jersey. Miss Peggy Gogin
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RCA Astro-Electronics Division, Princeton, New Jersey. Mr. Louis
Gomberg. (609) 448-3400 ext 2187.

Aerospace Corporation, 2350 El Segundo Blvd, El Segundo, California.
Mr. Edward Clark. (213) 648-6618.

Texas Instruments, Box 6015, Dallas, Texas 75222. Mr. William
Brown. (214) 238-4934, Mail Station 296.

Supplier A - Preferred to remain anonymous.

Supplier B - Preferred to remain anonymous.

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2. V. J. Lukach, L. Gallace, W. Williams: "Thermal Cycling Ratings of Power Transistors." *Proceedings of the 1972 Annual Reliability and Maintainability Symposium.*
3. H. C. Hurley: *Thermal Cycle Effects on MIB Reliability.* Federal Systems Division, International Business Machine Corp.
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III. A STUDY OF ACCELERATED TESTING TECHNIQUES

by R. A. Homan and R. W. Burrows

CONTENTS

	<u>Page</u>
III. A STUDY OF ACCELERATED TESTING TECHNIQUES	III-1
A. INTRODUCTION	III-1
B. GUIDELINES FOR ACCELERATED TESTING	III-4
1. General	III-4
2. Materials	III-4
3. Solder Joints	III-4
4. Electronic Parts	III-5
5. Electronic Assemblies	III-5
6. Mechanical/Electromechanical Hardware	III-6
7. Batteries	III-6
8. Bearings	III-6
9. Valves	III-7
10. Transducers	III-7
11. Enhanced Defect Testing	III-8
12. Dynamic Mission Equivalent Testing	III-8
C. DISCUSSION	III-9
1. General Comments	III-9
2. Materials	III-10
3. Solder Joints	III-21
4. Electronic Parts	III-24
5. Electronic Assemblies	III-51
6. Mechanical/Electromechanical Hardware	III-56
7. Batteries	III-62
8. Bearings	III-64
9. Valves	III-69
10. Transducers	III-71
11. Enhanced Defect Testing	III-72
12. Dynamic Mission Equivalent Testing (DME)	III-73
D. A STATISTICAL MODEL FOR ELECTROMIGRATION INDUCED FAILURE IN THIN FILM CONDUCTORS	III-77
E. REFERENCES	III-98 thru III-101

Figure

1	Temperature Dependent Failure Mechanisms within One Device	III-12
2	TGA/Isothermal Comparison for Dow Corning 6-1106	III-13
3	TGA/Isothermal Comparison for Viton A	III-14

4	TGA/Isothermal Comparison for Epon 828	III-16
5	TGA/Isothermal Comparison for Choseal	III-16
6	TGA/Isothermal Comparison for Glass Filled Diallylphalate	III-17
7	TGA/Isothermal Comparison for Dacron Parachute Material	III-18
8	Accelerated and Normal Stress Failure Distributions . .	III-25
9	Cumulative Failure Plot-Constant Temperature	III-29
10	Cumulative Failure Plot-Constant Time	III-29
11	Arrhenius Regression Plot	III-30
12	Distributions on Regression Curves	III-31
13	Cumulative Damage Failure Line	III-32
14	Cumulative Damage Diagram	III-33
15	Weibull Plot-Constant Voltage	III-34
16	Weibull Plot-Constant Time	III-35
17	Inverse Power Regression Plot	III-36
18	Fixed Time Interval Step Stress Test	III-36
19	Distribution Curve with Breaks	III-39
20	Maximum Arrhenius Acceleration Factor	III-41
21	High and Low Activation Energy Regressions	III-41
22	Constant Stress Extrapolations	III-43
23	Constant and Progressive Stress Test Times	III-46
24	Constant and Progressive Stress Test Weibull Plots . .	III-46
25	Temperature Test Results	III-55
26	Fatigue S/N Curve	III-57
27	Prot Endurance Limit Curve	III-58
28	Cumulative Damage Curve Extrapolation	III-60

Table

1	Temperature Correlation Data	III-23
2	Test Time Comparison for a Jupiter-Saturn-Pluto Grand Tour Type Mission	III-75

III. A STUDY OF ACCELERATED TESTING TECHNIQUES

A. INTRODUCTION

In today's aerospace environment where hardware is being developed and tested in a relatively short time and is expected to survive for extended periods of time, it is obvious that credible accelerated life test technology should be utilized. On Space Shuttle payloads, Space Station, and outer planet explorations, where total missions approach ten years with little or no maintenance, the ability to demonstrate hardware performance on an accelerated basis with a high degree of confidence is needed.

Since many organizations in many different technologies have been actively pursuing the development of accelerated life test methodologies, it is very desirable to assimilate and evaluate this data so that logical, rational approaches can be identified and utilized. This chapter summarizes the current state-of-the-art of accelerated testing.

It is our observation that two different categories of accelerated life testing exist:

- 1) A Quantitative Accelerated Life Test provides a numerical conclusion about the life of a product; e.g., 13.7 years;
- 2) A Qualitative Accelerated Life Test provides proof that the product will survive for a very long time; e.g., greater than 10 years.

The development of quantitative accelerated life tests that provide valid and accurate correlation with real-time data has been limited to relatively simple items such as materials and discrete parts. Success on these simple items has been achieved because only one primary life terminating failure mechanism dominated.

More complex assemblies, such as batteries, bearings, integrated circuits and electronic assemblies have a more complex array of life limiting failure mechanism which change with the choice of test temperature. Here, accelerated life testing becomes more qualitative than quantitative; but experience has shown that qualitative approaches can successfully produce long-life hardware.

For this reason, no potential qualitative test approach should be rejected merely on the grounds that it is not quantitative. This philosophy will aid in quieting the adversaries of accelerated life testing who base their arguments on the fact that accurate correlation has not been achieved.

The basic difficulty in developing a valid, correlatable accelerated test of complex devices is illustrated in Figure 1.

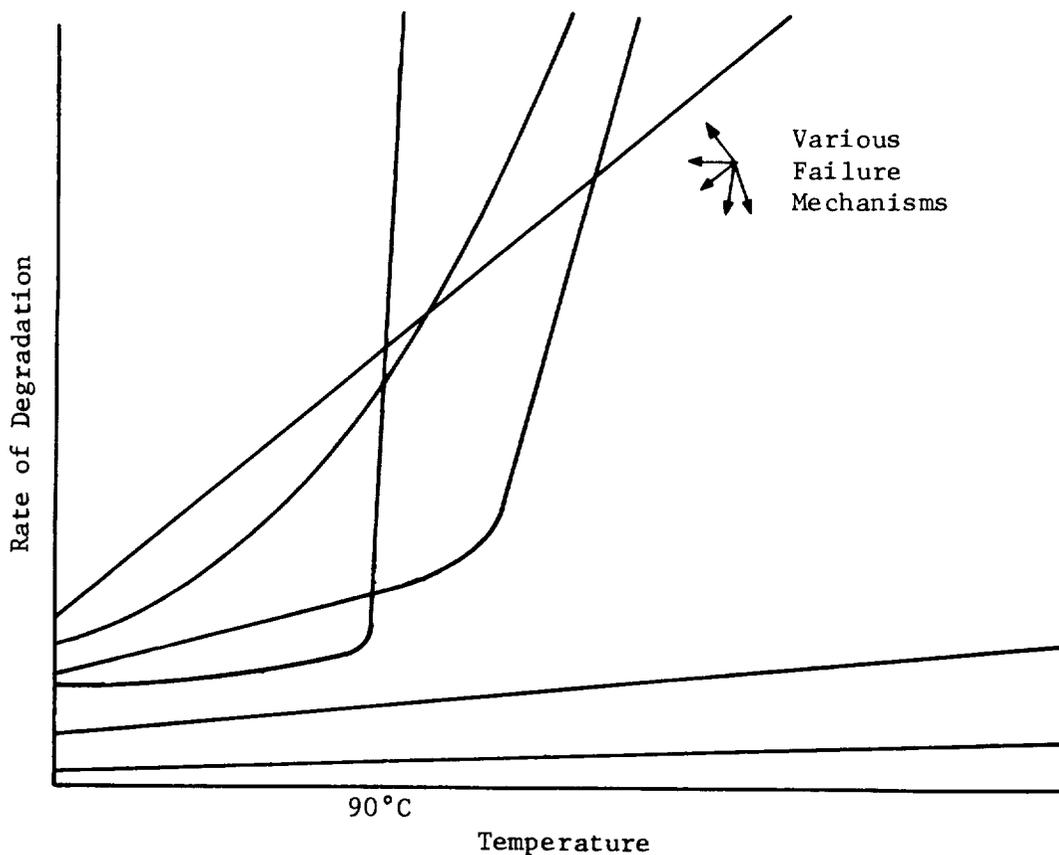


Figure 1 Temperature Dependent Failure Mechanisms Within One Device

This figure illustrates the problem with a more complex device such as a battery. Such a device has a complex array of life-limiting failure mechanisms, and the relative contribution of each failure

mechanism changes with the choice of test temperature. With this hypothetical situation, acceleration by increasing the temperature would have to be limited to 90°C. Then, with enough time and resources, a time-temperature correlation curve could be developed for this specific, hypothetical device. But this correlation would not be valid if the device was changed, either by design changes, part changes, or changes in the critical processes. The original correlation curve would certainly not be applicable for a slightly different device of the same generic class.

There is yet another distinction that should be made regarding accelerated testing. Some accelerated tests are true accelerated tests in that failure mechanisms are actually accelerated by raising a stress level, usually temperature. Other so-called accelerated test approaches are actually real-time, nonaccelerated tests, in which degradation is accurately measured and then extrapolated into future time to provide an estimate of life capability.

The above principles have been presented to enable the reader to better understand the various subjects subsequently presented in this study.

B. GUIDELINES FOR ACCELERATED TESTING

1. General

Quantitative accelerated test techniques have been developed for very simple parts and for materials. For more complex devices containing multiple failure mechanisms, each mechanism usually has a different, and non-linear acceleration factor; valid quantitative methods neither currently exist nor are they apt to be developed in the foreseeable future. This category includes electronic assemblies, batteries, bearings, valves, transducers, and other electromechanical hardware. However, reliable qualitative accelerated test methods exist; and these methods merit continued development and application in programs requiring long-life. Past history has shown that qualitative accelerated life test techniques have produced hardware with increased life and reliability, even though they do not provide a quantitative life assessment.

This chapter presents a concise summary of the state-of-the-art, describes current research, and identifies those techniques which should be further encouraged.

2. Materials

The use of the Thermogravimetric Analyses technique can yield significant schedule and cost savings as a partial cost-effective substitute for real-time, long duration, thermal vacuum testing. The application, advantages, and limitations of this technique are discussed in the subchapter on the accelerated testing of materials. This technique is currently being developed by Martin Marietta Aerospace.

3. Solder Joints

Every long-life spacecraft program should verify the integrity of solder joint configurations by extensive temperature cycling beginning with the earliest prototypes. This is usually accomplished in an ambient air temperature chamber, using a nominal cycle of about one hour. A two-minute cycle consisting of immersion in cold and hot liquids is about three times as severe and yields a test program time reduction of 90. This is very attractive, when the temperature cycling program requires thousands of cycles, as was the case with the Apollo Telescope Mount Gyro Precessor.

4. Electronic Parts

Electronic part accelerated test techniques are more advanced than other part types. It can be effectively utilized on semiconductors, resistors, and capacitors. Step stress and high temperature constant-stress tests, utilizing the Arrhenius model, are recommended as the most advanced approach for semiconductors. Further development of techniques is required for complex devices such as LSI/MSI. The inverse power rule and progressive stress or constant stress tests are the recommended approach for capacitors. It is not necessary to perform accelerated tests to obtain quantitative data such as failure or hazard rates. Simple qualitative tests can provide conservative life estimates, margin information, and data for comparative evaluations or estimating screen level effectiveness. Accelerated testing can be applied effectively when such data is needed. It is recommended that these approaches be used selectively as these requirements arise, as opposed to imposing a general accelerated test requirement on a program.

The temperature and power screening levels imposed by Bell Telephone Laboratories on discrete semiconductors and integrated circuits for high reliability applications are much higher than generally used in the industry. The commonly used levels and durations are almost benign by comparison. These high levels were derived through experience with accelerated testing that indicates the commonly used levels may not be the most effective. It is recommended that further studies be made to examine the feasibility and desirability of implementing higher temperature screening (burn-in) levels on selected parts.

5. Electronic Assemblies

Both multiple temperature cycling and AGREE (MIL-STD-781B) testing are very powerful forcing functions for improving the reliability of electronic assemblies. Their wider use in development, qualification and production acceptance testing should be encouraged. Temperature cycling is less costly to implement than AGREE because of the contractual risks of AGREE testing to the producer; but AGREE testing should be considered for wider use by NASA, particularly on the larger procurements where its application becomes more cost-effective. Based on an industry survey of 26 companies, both methods were more effective than constant temperature burn-in.

Step-stress testing to failure by progressively increasing the temperature, as developed by Grumman, should also be considered as a good development tool to detect and rectify weak links. Although this technique has no application in qualification or production acceptance testing, it is considered an excellent development test technique.

6. Mechanical/Electromechanical Hardware

Accelerated test approaches are not developed or utilized to the extent existing for materials, solder joints, electronic parts, and electronic assemblies. Several different approaches are described in the text, including the cumulative damage method utilized by E. Rabinowicz of MIT.

7. Batteries

Valid quantitative accelerated life test techniques have not been developed for batteries. Current investigations at the Naval Ammunition Depot and at Batelle Memorial Institute should be monitored, but a significant state-of-the-art breakthrough is not anticipated. The allocation of additional resources is not recommended. Qualitative approaches, by increasing the temperature and depth of discharge, have application in battery development programs to understand the failure mechanisms, since the data can be utilized for design improvements.

8. Bearings

Valid quantitative accelerated life test techniques have not been developed. However, further efforts should not be discouraged since every attempt yields additional data and insight into failure mechanisms. It appears feasible, according to LERC bearing experts, to accelerate a life test by increasing the temperature, when the bearing is designed to operate in the elastohydrodynamic lubrication regime. Long-life bearings should be designed wherever possible, to operate in this regime.

Recent developments in bearing technology have shown that a previous method of accelerating life by increasing the radial load is invalid.

Some so-called accelerated life tests on bearings are not true accelerated tests, but are efforts to extrapolate measured real-time degradation out to a life prediction. These techniques provide a rather inaccurate prediction. But they do serve to provide

the bearing technologists with valuable data that is used to extend the life of bearings, even though a valid quantitative life prediction is not achieved.

For the bearings in the future reusable space vehicles, the issue of designing bearings to withstand many repeated exposures to severe vibration without reduction of life due to fretting corrosion (false brinelling) becomes paramount. Economic resources should be directed towards the solution of this problem.

9. Valves

Increasing the cycling rate of valves is a valid accelerated test approach when long-term aging mechanisms are either not present or have been designed out. When aging phenomena is present, then the increased cycling rate approach must be augmented by other accelerated test programs. Examples of aging phenomena are corrosion by fluids, cold flow of teflon seats, and bonding of a metal seat to a metal poppet due to metal diffusion. A current program being conducted by TRW for JPL on the diffusion problem and on acoustic signature testing is of interest.

The development of acoustic signature testing is being pursued by both TRW and GE. This technique will not provide a true accelerated test, but it has the potential of identifying degradation within the valve due to wear or aging. These trends could be extrapolated to a prediction of life. This technique is usually inaccurate since the amount of degradation necessary to cause failure is difficult to accurately establish.

In general, valve specialists consider accelerated testing to be untrustworthy; but utilize it in the absence of a valid, quantitative technique. As with bearings and batteries, every attempt to develop a valid method yields reliable information for improving the product, even though an accurate quantitative life estimate is not achieved.

10. Transducers

The principal long-life problem with transducers is not wearout, but long-term stability (calibration shift). For existing devices which have proven stability based on months of real-time test data, there is little need for accelerated approaches. For newly developed devices, each specific design should be analyzed for the potential application of accelerated test techniques. For

example, experience at Martin Marietta Aerospace has shown that a minimum of five temperature cycles, exceeding use levels by 30°F, are desirable to guarantee long-term stability. For very long-life programs, 20 temperature cycles are recommended.

11. Enhanced Defect Testing

In certain instances, this type of testing can quickly yield valuable data, although it is not strictly classifiable as accelerated testing. An example of its use is a program by IBM in which Multilayer Printed Circuit Boards were fabricated with a number of controlled defects and then temperature cycled to failure. This program quickly revealed that the ductility of the copper was the most important factor for long-life.

12. Dynamic Mission Equivalent Testing

This technique, developed by JPL, is applicable as a systems level spacecraft test. The test acceleration is achieved, not by the use of increased stress levels, but by operating the spacecraft hardware to simulate one or many actual missions, except that the non-operating, or quiescent periods are omitted. Since this testing does not cope with dormant aging phenomena, the DME program must be augmented by other accelerated test programs which address the specific dormant aging problems.

C. DISCUSSION

1. General Comments

The obvious method of obtaining service life information on a product is to test it under worst-case service conditions for the required service period or until it fails. This is the most reliable method, providing the widest acceptance of test results with the greatest confidence. This approach is realistic and desirable on new products when historical data is lacking, when the required service life is short, and when sufficient test time is available prior to placing the product in service. If the time allowed is insufficient to thus verify service life capability, then accelerated test approaches become attractive. An accelerated test approach is considered herein to be any method which provides information on or verifies a service life greater than the test time. The objective of such testing is to reduce the time and the cost required to obtain the desired information.

A widely used approach to accelerated testing consists of increasing the degradation rate of a part by applying stress levels and/or cyclic stress rates which are greater than those seen in normal use. The time required to produce a given amount of degradation or a failure is thus reduced and is said to be accelerated. If the relationship between degradation rate and applied stress is known, then the time required to achieve the same results under normal stress conditions can be calculated. Confidence in this extrapolation of test time to an estimated "real" time is related to the accuracy by which the relationship between stress and degradation rate is known. This in turn requires an understanding of the specific mechanisms causing failure and an accurate mathematical model of the physical laws governing these mechanisms. The accelerated test stress type and level must not introduce new failure mechanisms and must be within the range of validity of the models used.

Accelerated tests have been performed for the purposes of achieving quantitative results such as estimates of failure distributions, estimates of mean life, determination of operating parameter rate of change with time, estimates of mean time between failures (MTBF's) or failure rates, determination of fatigue life and factors of safety, establishment of warranties, determination of margins and ratings, selection of screen test levels, and calculation of relationship between operating temperature and mean life. When valid

results are achieved at the accelerated level, extrapolation to any other level within the range of validity can be made. The results can thus be applied to a wide range of in-service applied stress levels. Achieving quantitative results from accelerated testing requires the greatest degree of sophistication and care in test design, test performance, and data analysis.

Accelerated testing for the purposes of achieving qualitative results such as comparison of new or competitive products or evaluating the uniformity of product quality levels has also been performed. The various approaches, rationales, and limitations to accelerated testing are summarized in References 1 through 3. Reference 3 contains 524 bibliographical entries on the subject in addition to a critique of published test results.

In this chapter, recent results of solder joint thermal cycling tests and materials accelerated tests are presented. The materials accelerated test program included heavily filled polymers and utilized the thermogravimetric analysis technique. Accelerated weak-link testing of electronic assemblies is critiqued, and the status of electronic part and mechanical/electromechanical hardware testing is reviewed.

2. Materials

a. Introduction - The long life capability of polymers in a vacuum at a specific temperature is generally established by real-time testing for periods of several days to as long as 1 year, depending on the mission length and the conservatism of the contractor. Acceleration of the conventional thermal-vacuum materials test by increasing the temperature 10° to 50°F is an obvious approach. But this approach is not generally used because (1) a different acceleration factor exists for each material, and (2) there are so many materials, the approach is impractical.

The Thermogravimetric Analysis (TGA) method described herein provides accurate and exceedingly rapid results on long term decomposition processes of polymers which is not gained by conventional thermal-vacuum testing. Mass spectrographic analysis of decomposition products can be used in conjunction with the TGA if it is desired to obtain an indication of their nature. The TGA test, including sample preparation and data reduction, can be accomplished in less than 4 hours.

The remaining problem is the development of techniques and confidence in translating the chemical degradation data into reliable predictions of material property changes. However, even with this limitation, TGA can, at this time, replace a major portion of the real-time thermal vacuum test program and yield more accurate long-life projections at much lower cost.

b. Thermogravimetric Analysis Testing - The TGA method of testing materials can be used as an accelerated test technique to predict long term thermal degradation kinetics. Slow thermal degradation over a long period of time may result in a loss of structural integrity. Also the degradation products may condense on and degrade other equipment. This may be of particular concern if the degradation products are corrosive or interactive with other parts and materials in the system. Two recent studies performed by Martin Marietta Aerospace were concerned with thermal degradation kinetics of materials. The study of Reference 4 was concerned with the aging of explosive and pyrotechnic propellant materials. A detailed test program utilizing the TGA approach was developed for determining and demonstrating the survivability of the chosen materials. A list of such materials capable of withstanding sterilization cycling at 260°F and 10 year aging under conditions of 10^{-6} torr and 150°F was compiled for the NASA Langley Research Center.

An investigation of polymer degradation kinetics was performed in the study of Reference 5. The validity of predicting these kinetics at normal use temperatures from high temperature TGA measurements was evaluated. The TGA approach on polymers has the advantage that a large variety of materials can be tested quickly and economically as opposed to an isothermal approach. Also, isothermal methods do not readily distinguish between degradation of polymer and the evolution or degassing of dissolved materials such as unreacted monomer or catalyst. A summary of the test approach and the results as reported in Reference 5 are included herein.

1) *Polymer TGA Test Approach* - Six polymers were selected for TGA testing. These were Dow Corning Silicone 6-1106, DuPont Viton A, Shell Chemical Epon 828, Chomeric Inc. Choseal silver filled conducting silicone, glass filled diallylphthalate, and Dacron. Small samples of each polymer weighing approximately 10 mg each were taken through total decomposition in a Mettler Thermoanalyzer I equipped with a DTG (TGA derivative) output and a vacuum capability. The DTG provided the rate of weight loss at the test temperature and the TGA provided the weight loss at that temperature.

The heating rate was 10°C per minute for all materials except Dacron. The degradation rate of Dacron is so rapid at TGA temperatures that a smaller rate of 2°C per minute was used. Evacuation of the system to 5×10^{-6} torr was performed prior to the start of heating.

Isothermal weight loss measurements were also made on samples of each material for the purpose of comparing large sample isothermal test results with predictions made from the small sample TGA measurements. The samples used for isothermal testing weighed from 4 to 6 grams each. The isothermal test system consisted of a furnace and controller, ion pump, appropriate valving and ion gauges, and an Ainsworth Recording Semi-Micro Vacuum Balance. Two thermocouples were placed in the vacuum space near the test sample and one was imbedded in a separate piece of the material under study as a temperature reference. There was no difference in temperature between thermocouples. Heating was started after the system was evacuated to 5×10^{-6} torr. The weight loss was recorded for 12 hours at each temperature.

2) *Derivation of Polymer Arrhenius Relationships* - The simple first order kinetic equation

$$dx/dt = k_t (A_o - x)$$

was found to apply very well in describing the degradations. In this equation dx/dt is the rate of weight loss, x is the weight loss, A_o is the initial weight of the "active component" suffering loss, and k_t is the rate constant at test temperature T . The active component is that portion of the original sample undergoing degradation at the test temperature such as solvent, catalyst, monomer, or polymer. The thermoanalyzer yielded dx/dt from the DTG output and x was obtained from the TGA. Analysis of the TGA curve yielded the values of A_o for each component. For polymers with a simple TGA curve indicating only one active component, A_o was the total weight loss. For polymers where the TGA curve showed degradation to be more than a one-step decomposition, the weight loss for each step was calculated yielding A_o for the particular component degrading during the step.

For the isothermal data, dx/dt was obtained from the slope of the weight loss curve near the end of a run at temperature and x was obtained from the weight loss curve. The values of A_o were taken as the fraction of total initial sample weight as determined from the TGA analysis.

From the above equation and the data obtained, the values of k at various temperatures were determined and plotted on Arrhenius scales of $\log k$ versus inverse absolute temperature. The TGA/DTG and isothermal Arrhenius relationships are shown on the same plot for each polymer in Figures 2 through 7.

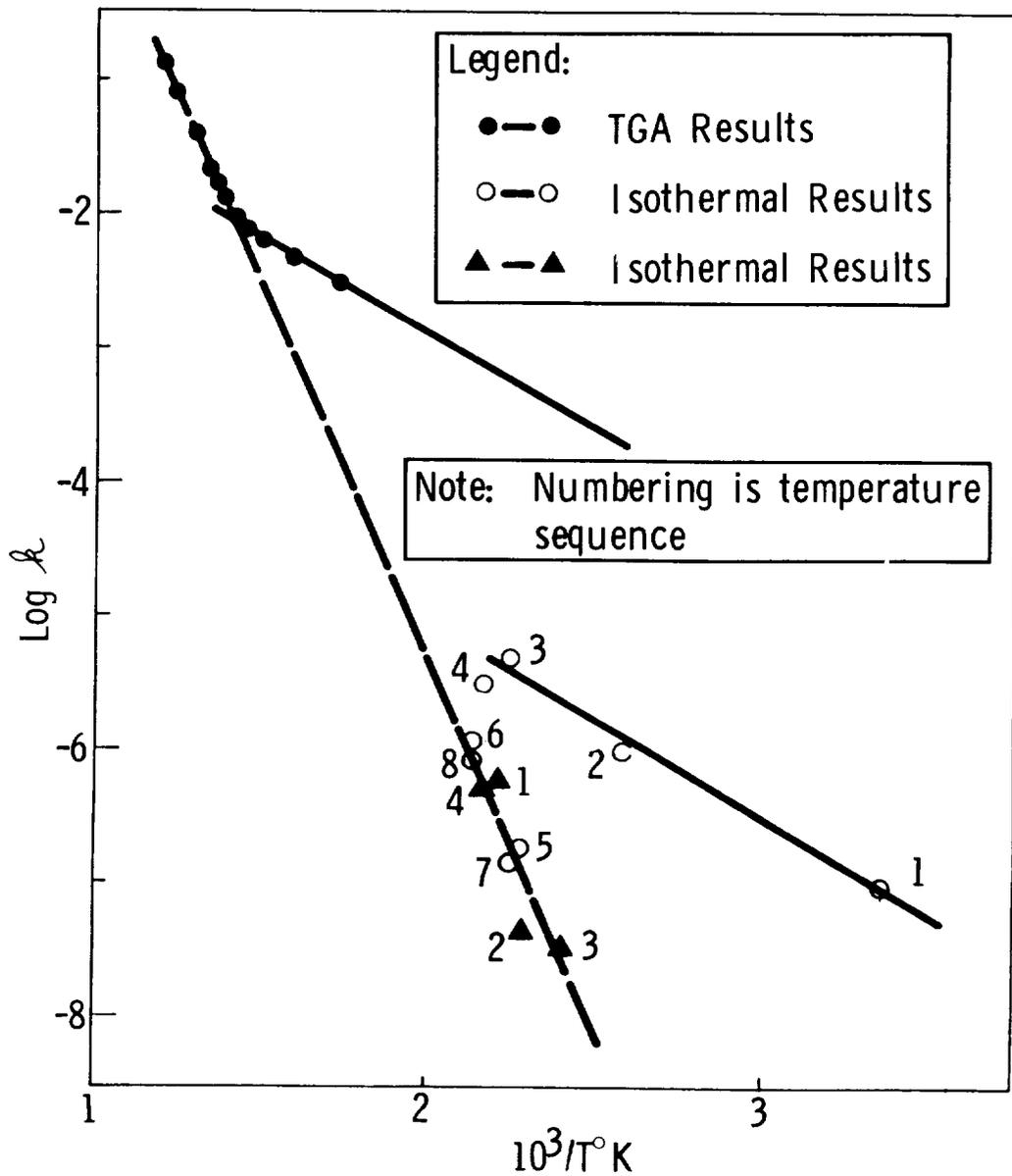


Figure 2 TGA/Isothermal Comparison For Dow Corning 6-1106

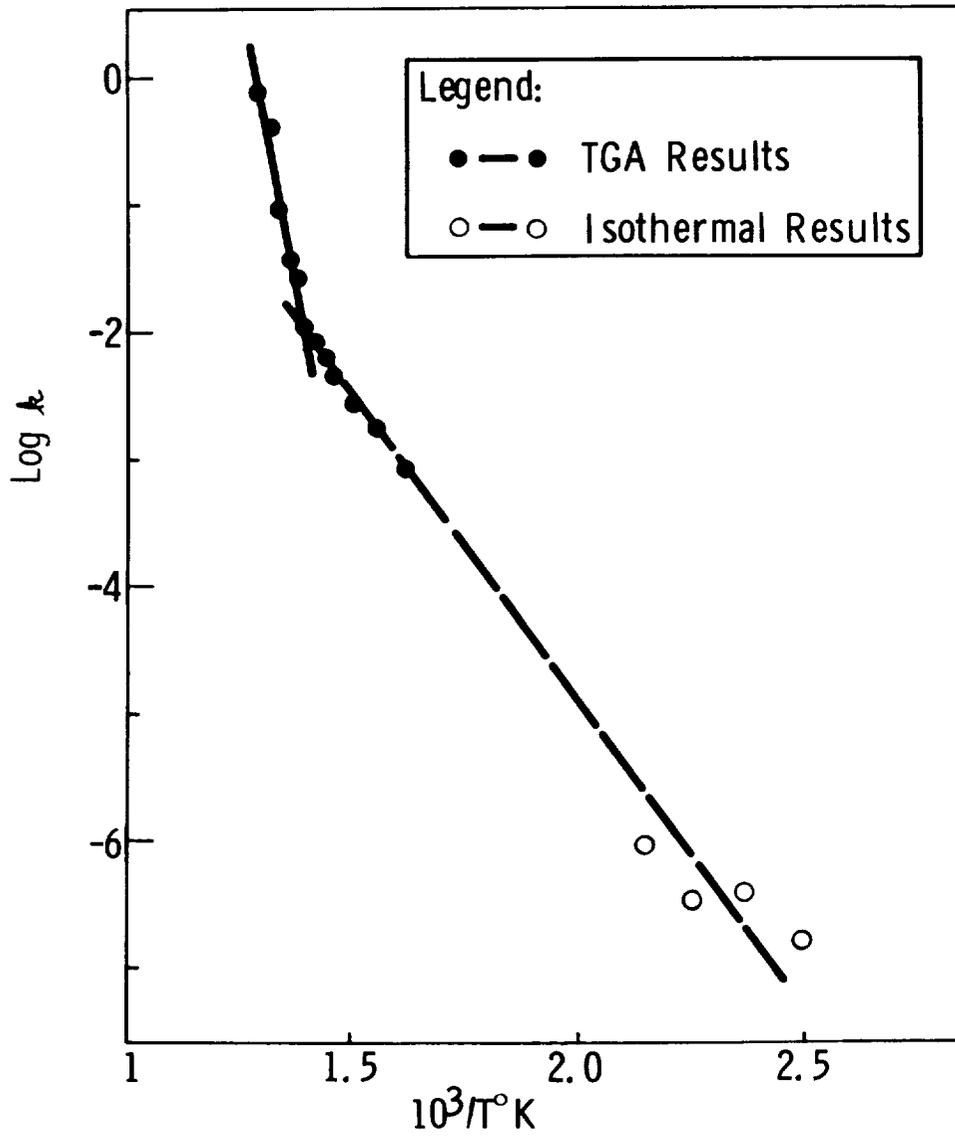


Figure 3 TGA/Isothermal Comparison For Viton A

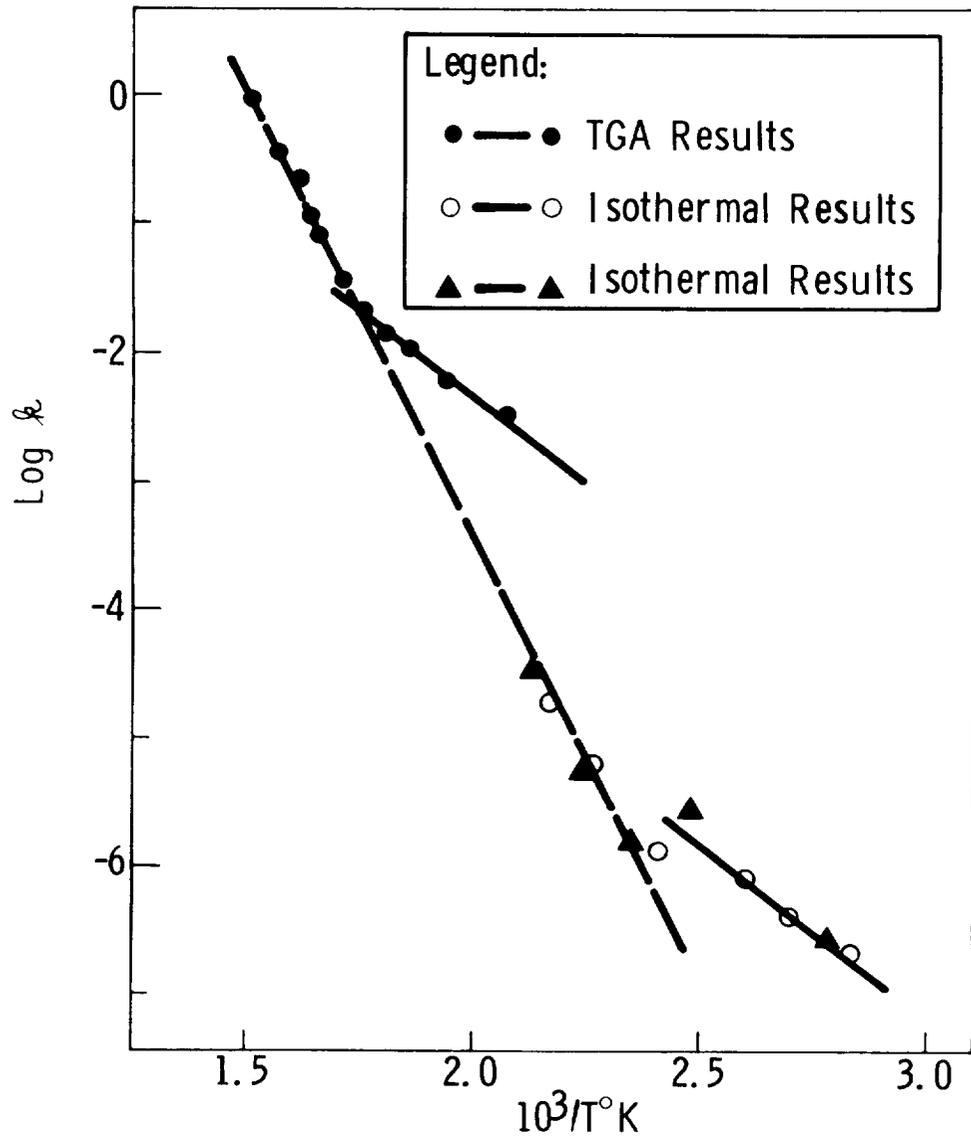
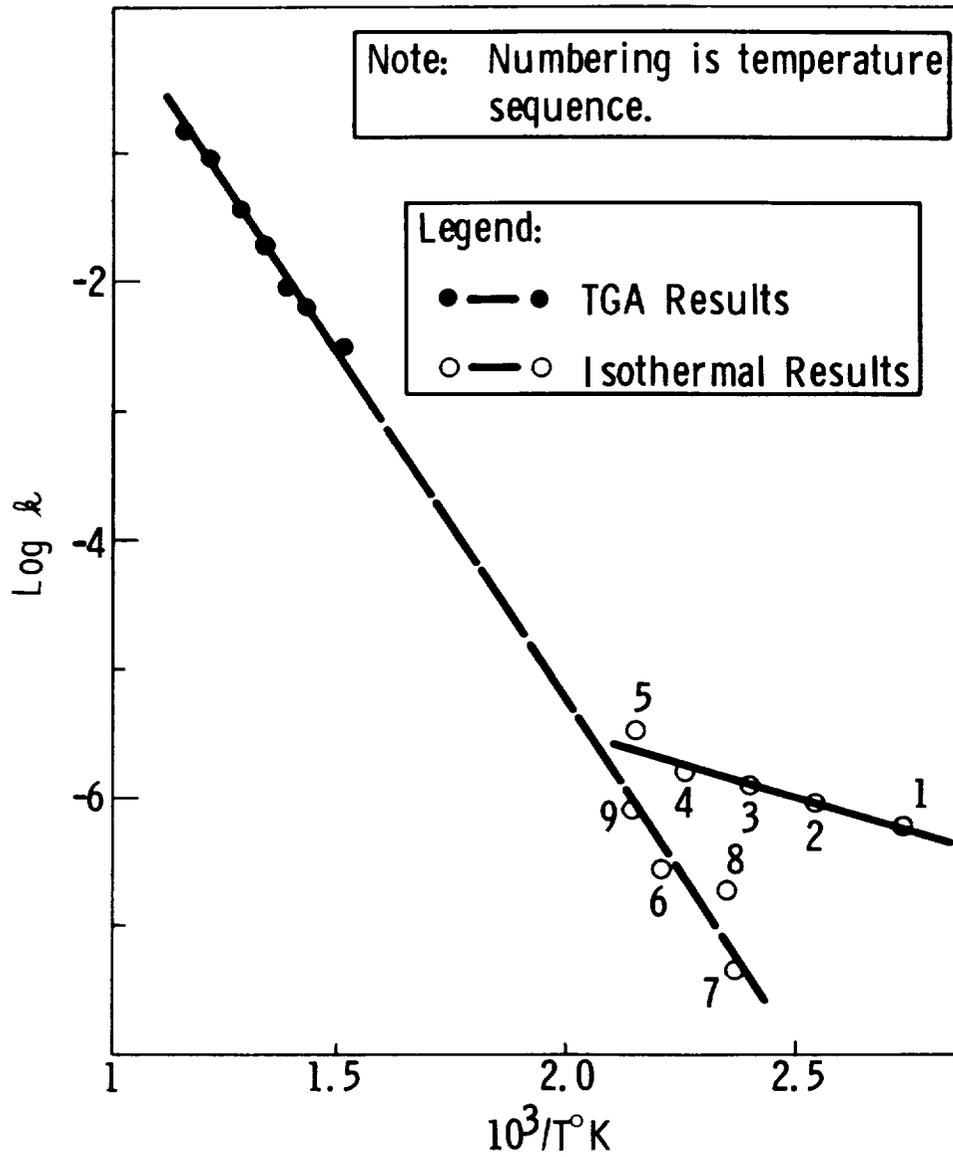


Figure 4 TGA/Isothermal Comparison For Epon 828



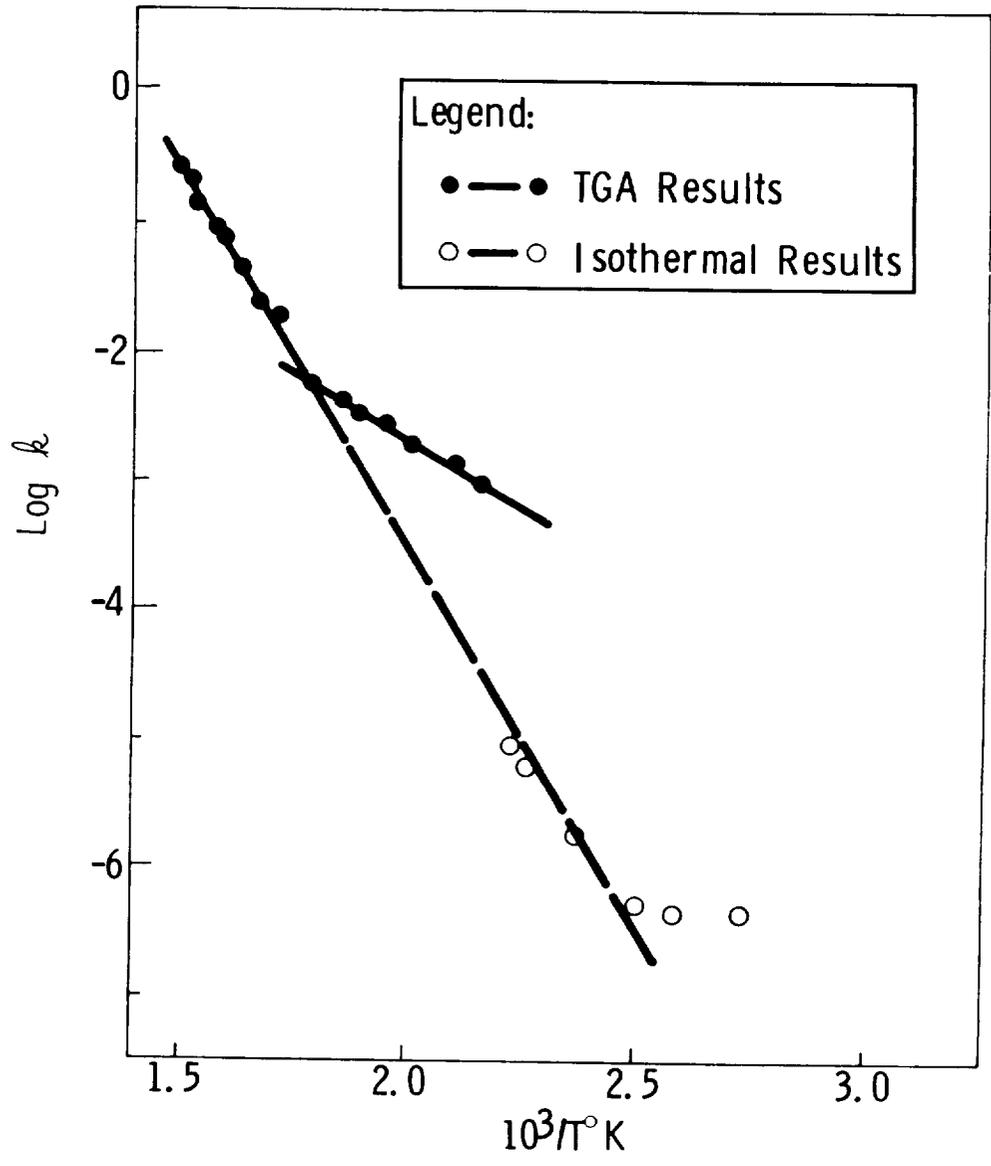


Figure 6 TGA/Isothermal Comparison For Glass Filled Diallylphthalate

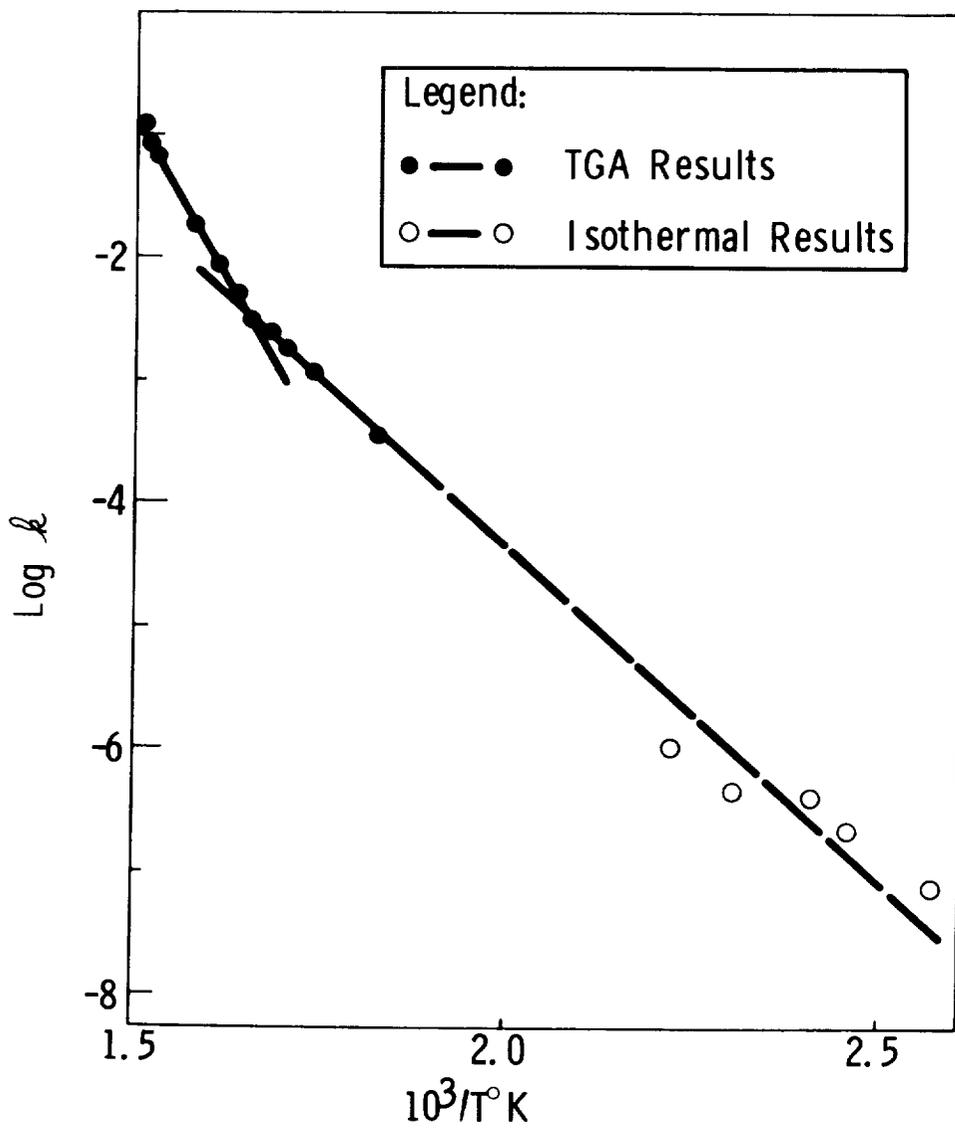


Figure 7 TGA/Isothermal Comparison For Dacron Parachute Material

3) *Polymer TGA Test Results* - Figure 2 shows the Arrhenius relationships obtained from the TGA and isothermal tests of Dow Corning Silicone 6-1106. The smaller TGA slope is associated with the "solvent" such as unreacted monomer or catalyst. It is not a true activation energy. At the lower temperatures and early in the TGA test where this slope appears, the weight loss is predominantly "solvent" loss. For long term space missions the thermal degradation of the polymer itself is the important consideration since the "solvent" will be degassed very early in the mission life. The amount of "solvent" is insignificant with respect to the amount of polymer. Thus, after the "solvent" is degassed during the early stages of the TGA test, the subsequent Arrhenius relationship reflects the correct activation energy for decomposition of the polymer and the larger TGA slope yields an activation energy of 26.4 kcal/mol for decomposition of Dow Corning 6-1106.

The open circles of Figure 2 are isothermal results where the temperature of the sample was increased periodically from ambient to 200°C with a 12 hour dwell at each temperature. The triangles are isothermal results on another sample where the initial temperature was 200°C. With the increasing temperature sequence, an activation energy type slope is found for the "solvent." However, with the decreasing temperature sequence, the "solvent" is removed rapidly during the initial portion of the weight loss curve for point 1 and no "solvent" points are observed. It is seen that for decomposition of the polymer itself, the rate constants at lower temperatures are accurately predicted by extrapolation of the TGA activation energy line.

Figure 3 shows the Arrhenius relationship obtained from the TGA and isothermal tests of Du Pont Viton A. The TGA yields two activation energies. The high temperature region exhibits an activation energy of 85 kcal/mol. The isothermal results at lower temperatures are accurately extrapolated from the lower temperature region of the TGA Arrhenius plot. The activation energy in this region is 25.6 kcal/mol.

Figure 4 shows the Arrhenius relationship obtained from the TGA and isothermal tests of Shell Chemical Epon 828. The results of these tests were similar to those obtained for Figure 2. An exception is that both isothermal sequences were performed in an increasing temperature manner starting from ambient temperature. The decomposition activation energy is 30.8 kcal/mol. Again the TGA degradation prediction is excellent.

Figure 5 shows the Arrhenius relationship obtained from the TGA and isothermal tests of Chomeric Inc. Choseal. Choseal is a conducting silicone heavily filled with silver. The TGA curve showed a simple one-step decomposition with $A_0 = 18.8\%$ of the total weight.

Thus, this silicone was very nearly filled with about 80% silver. For the TGA analysis there is only about 1.9 mg of silicone so that solvent evolution is not apparent. However, with the much larger sample weight used for the isothermal test, a solvent evolution is obtained. The activation energy for decomposition of the polymer is 24.0 kcal/mol. Figure 5 shows that even with a heavily filled material there are excellent results in predicting the kinetics at moderate temperatures from TGA analysis.

Figure 6 shows the Arrhenius relationship obtained from the TGA and isothermal tests of glass filled diallylphthalate. The diallylphthalate was used in a Microdot, Inc. electrical connector. From the TGA curve, the active component was found to be 43.6% of the sample weight. The activation energy for this diallylphthalate is 24.1 kcal/mol. Again, for this heavily filled material the rate constants at moderate temperatures are accurately predicted from the TGA analysis.

Figure 7 shows the Arrhenius relationship obtained from the TGA and isothermal tests of Dacron parachute material. As with Viton A (Figure 3) there is no solvent evolution in either the TGA or the isothermal tests. The activation energy in the higher temperature region is 48.3 kcal/mol. The isothermal results at lower temperatures are accurately extrapolated from the lower temperature region of the TGA Arrhenius plot. The activation energy for decomposition in this region is 26.5 kcal/mol.

The results displayed in Figures 2 through 7 show that, in all cases, the small sample TGA analysis provided accurate predictions of large sample polymer decomposition kinetics at lower temperatures. This is of considerable importance as a long term degradation mechanism of polymers. Solvent in the polymers would be degassed early in the life of long term missions or may be removed during thermal-vacuum preflight tests and checkouts. Throughout the course of this investigation, the solvent isothermal Arrhenius slope was observed to be nearly identical to that obtained by the TGA but displaced to lower values of k by a factor almost exactly 10^{-2} . (See Figures 2 and 4.) This observation may be used to estimate the solvent quantity or degassing lifetime from TGA if desired.

4) *Polymer TGA Test Program Conclusions* - Results of this program have shown that the true thermal decomposition of polymers can be identified and separated from effects of the solvent in TGA tests. The rate constants of the decomposition mode applicable to realistically sized specimens operating at normal use temperatures can be determined accurately in TGA tests. The first order rate equation is applicable to this mode. The rate equation and the determined rate constants can be used to predict thermal degradation of polymers operating for any desired time at a given temperature. The activation energies applicable for normal usage temperatures of the polymers tested by the TGA approach were determined to be:

Dow Corning Silicone 6-1106, 26.4 kcal/mol

Du Pont Viton A, 25.6 kcal/mol

Shell Chemical Epon 828, 30.8 kcal/mol

Chomeric Inc. Choseal, 24.0 kcal/mol

Glass filled diallylphthalate, 24.1 kcal/mol

Dacron parachute material, 26.5 kcal/mol

3. Solder Joints

The life of solder joint configurations in a usage environment of temperature changes varies from a few cycles (in the case of a multipin module bridged with conformal coating on a PC board) to thousands of cycles (in the case of an unstressed copper lead solder joint).

Extensive use of temperature cycling to validate the adequacy of the electronic packaging is a requirement for long-life assurance. Such testing is usually accomplished in a temperature chamber using air as the heating and cooling medium, with each cycle requiring a nominal time of about one to eight hours. The cycle time selected is usually longer with equipment having appreciable thermal mass and shorter with equipment of low thermal mass, such as individual PC boards. However, in special cases it is desirable to accelerate the cycling by plunging the equipment alternately between hot and cold liquids thereby reducing the duration of each temperature cycle to minutes, or even seconds.

A particular case (Reference 6) is presented as an example: The requirement for a 12,000 thermal cycle goal from -10°C to $+55^{\circ}\text{C}$ on the ATM Gyro Precessor precluded a slow test to prove out ATM designs. Therefore, three new methods were evaluated. First, an automatic, dual chamber, air blast thermal cycling machine was monitored. It was found to be unsatisfactory because it required 8 to 10 minutes to thermally saturate a normal size (5 by 5 inch) PC board assembly that had been soaked at the opposite temperature extreme (-65°C to $+125^{\circ}\text{C}$). This evaluation showed that any air cycling machine would be too slow.

Second, small parts of PC assemblies (approximately two inches square) were dipped in hot oil at 300°F and liquid nitrogen at -320°F . Surprisingly, the solder joints withstood these thermal shocks. After several dozen cycles, they began developing the same type of solder joint deterioration and cracking that had been observed previously on gradual air cycling. However, the hot oil began softening the conformal coating, was messy to handle, and was difficult to inspect accurately.

Third, similar parts were alternately dipped in boiling water and isopropyl alcohol cooled by dry ice chunks. These materials maintained constant temperatures and did not affect the PC assemblies. The usual types of deterioration and cracking of the solder joints developed after a few score cycles. The small PC assemblies changed temperature in approximately 10 seconds. Larger assemblies required 20 to 30 seconds. This approach was selected.

An automated cycling machine was then built that would hold 16, 5x5 inch PC assemblies. This machine rotated groups of four assemblies on each of four arms, dipping them alternately into a tank of boiling water and a tank of isopropyl alcohol cooled with dry ice. Each group of boards were in each tank 45 seconds; they would then drain 15 seconds before entering the next tank.

This technique was then used to test many solder joint configurations and the results are presented in Reference 6.

Of particular interest is the correlation curves which related the slow air cycle to the fast hot water, cold alcohol cycle. This correlation is shown as Table 1.

Table 1 Temperature Correlation Data

Cycle Data	Percent of Solder Joints Cracked				
	5	10	15	20	
Air Cycle, 45 minutes to 1 hour, -55°C to +125°C (180°C delta)	60	69	88	110	Cycles
Water-Alcohol, 2 minutes, -75°C to +100°C (175°C delta)	15	25	32	38	Cycles
Acceleration Factor	4	2.8	2.7	2.9	--

It was concluded that the fast two-minute test was approximately three times as severe as the slower one-hour air test. The schedule benefits of the accelerated test are clearly evident. For example, MSFC has recommended that unproven solder joint configurations should be validated by 200 conventional temperature cycles. Using the slow one-hour, air test, and working one shift per day, this would require 25 days. On the other hand, if a 67 cycle "accelerated" test was substituted, the test could be performed in less than three hours. The time compression of 90 results because the accelerated test is thirty times faster, and only one-third the number of cycles is needed for equivalent damage.

The above discussion does not address the question of the correlation between laboratory and field results.

During this study, a search was made for data which correlated solder joint cracking in the field with solder joint cracking as observed in laboratory temperature cycling. There is a dearth of information on this subject. One effort, accomplished by IBM and reported in Reference 7, is summarized. On the Saturn program an intermittent failure due to a cracked stud-type joint on a relay lead in the Flight Control Computer was encountered. In the ensuing investigation, it was decided to implement solder joint fixes and to requalify the new solder joint configurations by laboratory temperature cycling. The new qualification test was arrived at in the following manner: It was determined from inspection of field units that the maximum solder joint crack rate was 4.8 percent for a period of 14 months. It was established that qualification testing should be based on a 24-month period. It was projected that the actual crack percentage would be 8.4

percent in 24 months. Laboratory temperature cycling of similar PC boards showed that 46, 20-minute temperature cycles, between -20°C and 85°C, were required to produce a crack rate of 8.4 percent. A safety factor of 1.5 was desired, so a qualification test program of 60 cycles was selected and used to evaluate the improved solder joint configurations. In this program, the failure criteria for a cracked joint was: "any visible line of material separation which is accompanied by frostiness and a coarse granular appearance and is detected at no more than 30X."

4. Electronic Parts

a. Introduction - Accelerated testing techniques can be particularly beneficial in the electronic parts area in view of the dynamic nature of the industry. The rapid rate of technological advances occurring not only tends to create a relatively high "standard parts" obsolescence factor, but creates a situation where the greatest advantages of performance or power/volumetric efficiency have been in existence for a short period of time. Little reliability history exists on specific parts. Paradoxically, they may be more reliable than their predecessors or competitors, but lack of data or experience may preclude their use. Accelerated testing may be viewed as an accelerated means of obtaining knowledge and experience.

There has been much activity in electronic part accelerated testing as reflected by the amount of literature on the subject regarding cost and technical benefits, as well as test results, approaches, problems, and limitations. The subject has been controversial and viewed with suspicion. However, interest persists. In this section the methods of test and analysis are reviewed, results are summarized, and the problem of the complex electronic part discussed.

b. Acceleration Factor - The acceleration factor is defined as the ratio of failure time under normal stress conditions to the failure time under high stress conditions. The high stress is assumed to increase the rate of time dependent processes which degrade the part to ultimate failure. Failure can be catastrophic or an out of tolerance condition. The high stress is often referred to as an accelerated stress. If t_2 is the failure time under accelerated stress, t_1 the failure time under normal stress, and τ the acceleration factor, then:

$$t_1 = \tau t_2$$

[1]

It is further assumed that all parts in a test group are equally affected by the acceleration factor and that the acceleration factor is a function of stress conditions only. Therefore, failure distributions under constant accelerated stress conditions must have the same form as if the parts had failed under constant normal stress conditions. The time scale of the normal stress distribution would be expanded by the acceleration factor τ when compared to the accelerated stress distribution. However, they must be of the same type. If bimodal under normal conditions then accelerated stress distributions must be bimodal, etc.

These requirements can be very helpful in anticipating and checking accelerated test results. If experience shows that a particular part fails with a normal distribution then a normal distribution would be expected on a large sample tested under accelerated conditions. Further, the cumulative distribution function $F(t_1)$ at time t_1 must be equal to the cumulative distribution function $F(t_2)$ at time t_2 . This is illustrated in Figure 8 for normal distributions. The percentage failures in the shaded areas are indicated by $F(t_2)$ at time t_2 and $F(t_1)$ at time t_1 . For the shaded areas to be equal, the number of σ_2 's from t_2 to t_2 must be equal to the number of σ_1 's from t_1 to t_1 . Therefore:

$$(\bar{t}_2 - t_2)/\sigma_2 = (\bar{t}_1 - t_1)/\sigma_1 \quad [2]$$

or

$$t_1 = (\sigma_1/\sigma_2)t_2 + (\sigma_2 \bar{t}_1 - \sigma_1 \bar{t}_2)/\sigma_2 \quad [3]$$

This is consistent with equation [1] only if:

$$\tau = \sigma_1/\sigma_2 = \bar{t}_1/\bar{t}_2 = t_1/t_2 \quad [4]$$

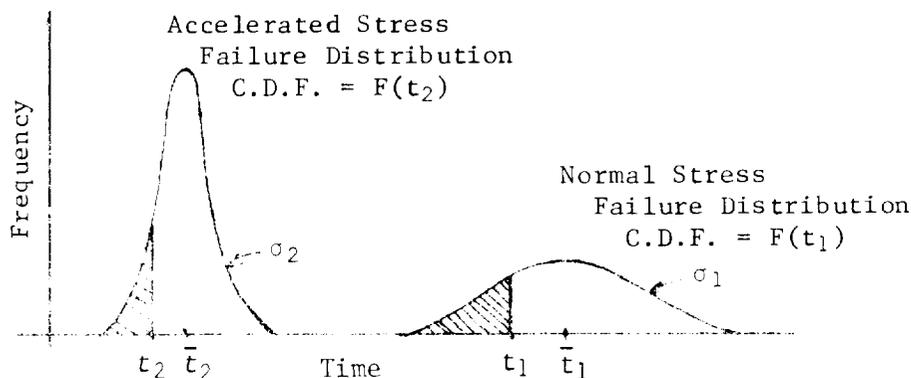


Figure 8 Accelerated and Normal Stress Failure Distributions

Equation [3] is also valid for log normal failure distributions if all parameters are related to log transformation of time. Letting $\sigma_{\ell 1}$ represent the standard deviation of the natural logarithm of times to failure under accelerated conditions, and similarly subscripting the other parameters, Equation [3] becomes:

$$\ln t_1 = \left(\frac{\sigma_{\ell 1}}{\sigma_{\ell 2}}\right) \ln t_2 + \left(\frac{\sigma_{\ell 2} \bar{t}_{\ell 1} - \sigma_{\ell 1} \bar{t}_{\ell 2}}{\sigma_{\ell 2}}\right) \quad [5]$$

or

$$t_1 = t_2^{\sigma_{\ell 1}/\sigma_{\ell 2}} \exp \left[\frac{\bar{t}_{\ell 1} - \bar{t}_{\ell 2} \sigma_{\ell 1}/\sigma_{\ell 2}}{\sigma_{\ell 2}} \right] \quad [6]$$

Therefore, for log normal accelerated and normal stress failure distributions to be consistent with Equation [1] it is necessary that:

$$\sigma_{\ell 1} = \sigma_{\ell 2} \quad [7]$$

and

$$\tau = \exp \left[\frac{\bar{t}_{\ell 1} - \bar{t}_{\ell 2}}{\sigma_{\ell 2}} \right] \quad [8]$$

The two-parameter Weibull distribution, with slope β and characteristic life θ , has a cumulative distribution function:

$$F(t) = 1 - \exp - [t/\theta]^\beta \quad [9]$$

Letting subscript 1 denote parameters at normal stress levels and subscript 2 denote parameters at accelerated stress levels, cumulative distributions $F(t_1)$ and $F(t_2)$ will be equal only when:

$$[t_1/\theta_1]^{\beta_1} = [t_2/\theta_2]^{\beta_2} \quad [10]$$

or

$$t_1 = \theta_1 [t_2/\theta_2]^{\beta_2/\beta_1} \quad [11]$$

Therefore, for accelerated and normal stress Weibull distributions to be consistent with Equation [1] it is necessary that:

$$\beta_1 = \beta_2 \quad [12]$$

and

$$\tau = \theta_1/\theta_2 \quad [13]$$

These results are also valid for exponential distributions if β_1 and β_2 are set to unity. Here the characteristic life is the MTBF or the inverse of failure rate λ . Thus, for constant failure rate or exponentially distributed parts to comply with Equation [1]:

$$\tau = \theta_1/\theta_2 = \lambda_2/\lambda_1 \quad [14]$$

The above distributions are most often utilized in accelerated test data analysis and interpretation of results. It is important to note that the conclusions drawn for each distribution are valid only for constant stress data and an acceleration factor constant with time.

c. The Arrhenius Model - The usual stresses used in electronic part accelerated testing are temperature, voltage, and power. Temperature is the most common stress. Power dissipation is often used as a means of generating acceleration temperatures and thus avoid expensive high temperature test fixturing. The Arrhenius reaction rate model:

$$R = A \exp - B/T \quad [15]$$

or

$$R = A \exp - \Delta H/kT$$

where

R = process or degradation rate;

A = constant of proportionality;

ΔH = activation energy in electron-volts;

k = Boltzmann's constant in electron-volts per degree Kelvin, and;

T = temperature in degrees Kelvin.

The model is widely used as the basis for physically explaining results of accelerated temperature tests. A wide variety of empirical data fits this model. It has been used to explain the 10°C rules for insulation deterioration, as well as semiconductor leakage currents. High temperature test results on diverse items, such as light bulbs, plastics, resistors, and semiconductors,

have been explained with this model. The Arrhenius equation is a first order approximation of the more generalized Eyring reaction rate model (Reference 1) which includes temperature as a stress, as well as providing for other acceleration parameters. These models require that the basic process causing damage, such as oxidation, diffusion, migration, etc, proceeds linearly in time under a given set of environmental conditions. Although the damage process proceeds linearly in time, a measurable parameter of an electronic part will change in a manner reflecting the usually complex relationship between process effects and the parameter. Failure occurs where accumulated damage has sufficient effect to place a parameter outside of defined limits.

If a single process is operating to cause part failure and all operating conditions except temperature are held constant, then the acceleration factor relating two temperatures is, from Equation [15]:

$$\tau = \exp B(1/T_1 - 1/T_2) \quad [16]$$

where

T_1 = lower temperature in degrees Kelvin;

T_2 = accelerated temperature in degrees Kelvin, and;

$B = \Delta H/k.$

This is the ratio of damage rate at accelerated temperature to damage rate at a lower temperature. Because it is only a function of temperature, independent of time, Equation [1] is assumed to apply.

Equation [15] is the basis for the practice of plotting test data on scales of inverse absolute temperature and logarithm of time. If failures are distributed log normal in time, then a plot of constant temperature cumulative failure test data on normal probability paper with logarithmic ordinate would appear as in Figure 9. Vertical spacings between the constant temperature lines therein are proportional to differences of inverse absolute temperature in accordance with Equation [15]. In accordance with Equation [7] it is expected that test data at different temperatures will plot as parallel lines.

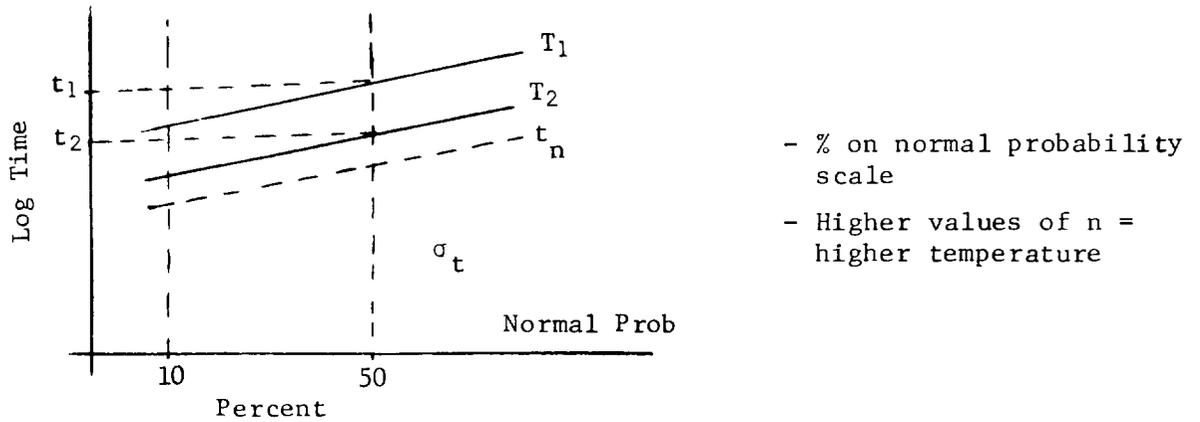


Figure 9 Cumulative Failure Plot-Constant Temperature

An equivalent plot which has been applied usefully in step stress testing is the constant time plot of Figure 10. From Equation [15], if failures are distributed log normally in time at constant temperature, then they will be distributed normally with a hyperbolic (or inverse) transformation of absolute temperature at constant time. In Figure 10 the vertical spacings between constant time lines are proportional to the differences in logarithms of time. Because the slopes in Figure 9 are equal, the lines in Figure 10 must also be parallel.

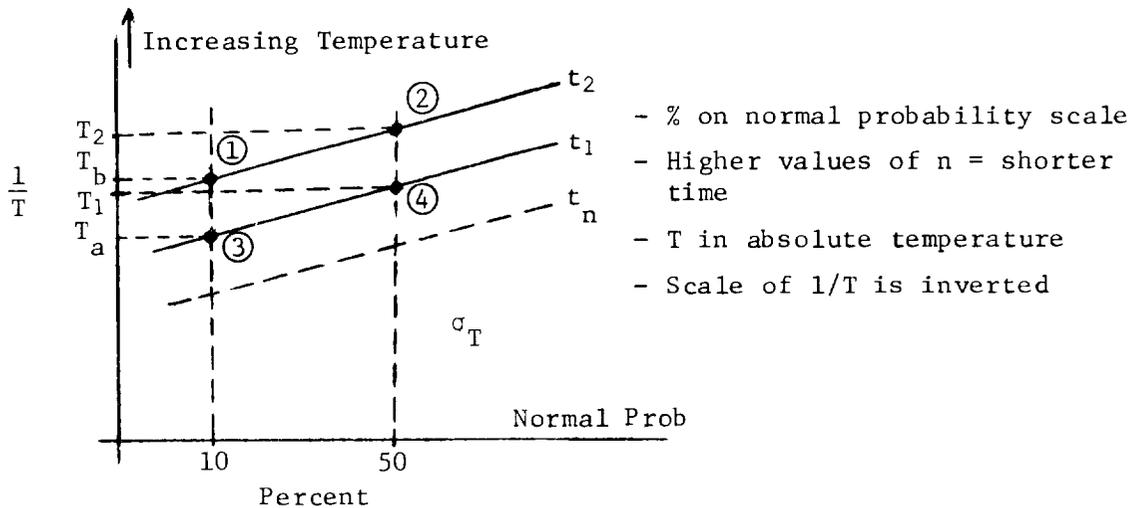


Figure 10 Cumulative Failure Plot-Constant Time

From either Figure 9 or 10, the regression plot of Figure 11 can be formed. The numbered data points in Figures 10 and 11 correspond to each other. Using the 50% failure line on Figure 11, the regression curve slope is:

$$m = [1/T_2 - 1/T_1] / (\ln t_1 - \ln t_2) = [1/T_2 - 1/T_1] / \ln \tau \quad [17]$$

which is equivalent to Equation [16]. The negative reciprocal of this slope is proportional to the constant B and therefore the activation energy. High activation energies are thus evidenced by low negative slopes of the regression curve.

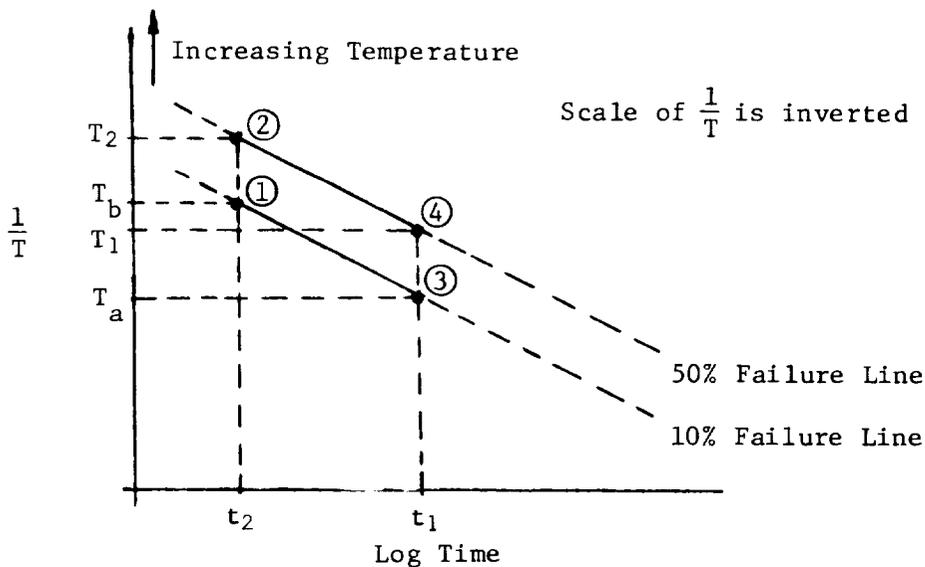


Figure 11 Arrhenius Regression Plot

From plots of cumulative failure data, such as in Figure 9 or 10, regression lines for any desired failure percentage can be made and the time to reach this percentage under any estimated temperature stress estimated by extrapolation.

The normal distributions of the transformed time and temperature variables are shown superimposed on a regression plot in Figure 12. It is evident that an equivalent expression for Equation [17] is:

$$m = -\sigma_T / \sigma_t \quad [18]$$

Where σ_T and σ_t are the standard deviations of the transformed temperature and time variables respectively. From Equations [16] and [17]:

$$B = \Delta H/k = \sigma_t / \sigma_T \quad [19]$$

Showing that the ratio of the standard deviations of failures in transformed time to the standard deviation of failures in transformed temperature is proportional to the activation energy. Also from Figure 12, $\tau = t_1/t_2$ in verification of Equation [8].

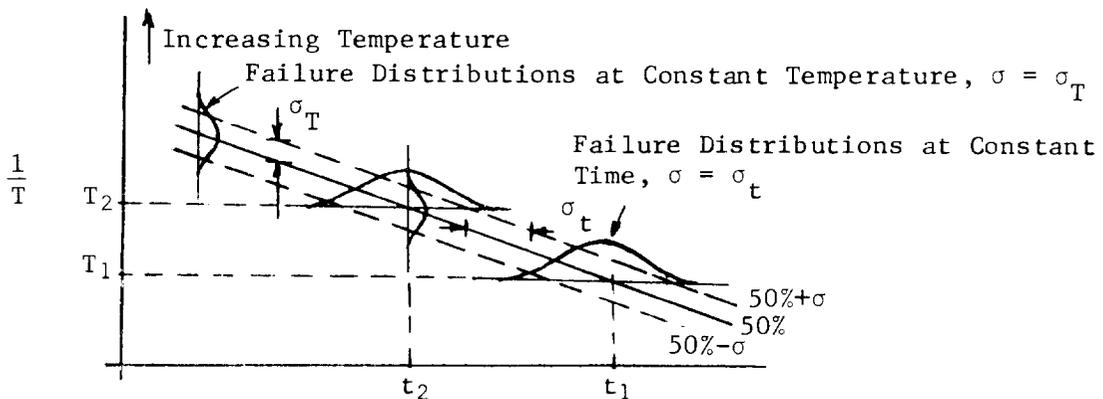


Figure 12 Distributions on Regression Curves

d. *Cumulative Damage Criterion* - If failure of a part occurs when an Arrhenius damage level is reached, then the temperature history is immaterial because Equation [15] requires damage at a given temperature to be linear in time. Cumulative damage techniques then apply to parts complying with the Arrhenius model. The cumulative damage criterion is stated as:

$$\sum \left(\frac{t_n}{L_n} \right) = 1 \quad [20]$$

where t_n is the time spent at temperature T_n and L_n is the life of the part at temperature T_n . If only two temperatures are considered and a part is operated for a time t_1 at temperature T_1 and then at temperature T_2 to failure at time t_2 :

$$\frac{t_1}{L_1} + \frac{t_2}{L_2} = 1 \quad [21]$$

This is shown graphically in Figure 13 where a failure will occur along line $L_1 - L_2$. It is immaterial if T_1 is performed prior to or after T_2 as long as the times t_1 and t_2 at each temperature remain the same.

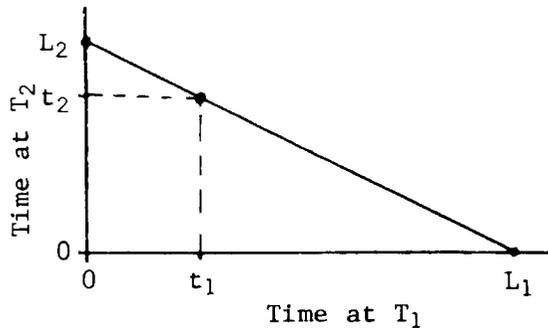


Figure 13 Cumulative Damage Failure Line

A constant damage diagram is a hyperbolic curve as shown in Figure 14. The abscissa scale is linear in time. The ordinate scale is nonlinear in temperature. The operational rectangles represent the lifetimes L_n at temperatures T_n and enclose equal areas because of the properties of the hyperbola. The operational rectangle area is proportional to damage level required for failure. For parts complying with the Arrhenius model, the ordinate scale is proportional to Equation [15], or $\exp - B/T$. A locus of variable temperature history when traced on this diagram will terminate at failure when the area underneath it is equal to the operational rectangle area.

The cumulative damage criterion applies to any rate model and any stress where the damage at a given stress level occurs linearly in time and provided that lifetime is independent of the sequence in which stress is applied.

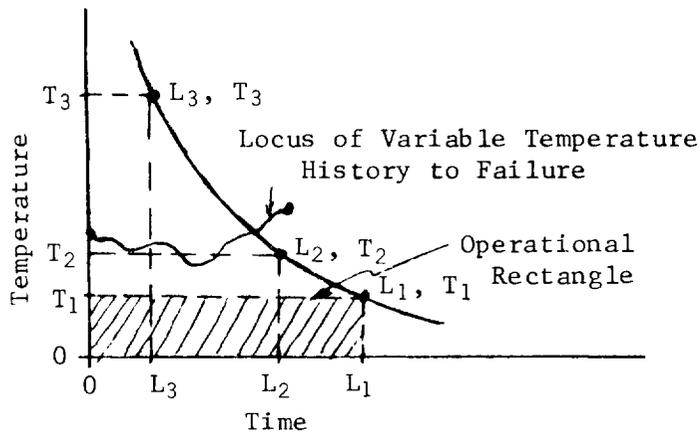


Figure 14 Cumulative Damage Diagram

e. *Inverse Power Rule* - In electronics, the inverse power rule has been used as a rate model for voltage degradation of capacitors and dielectrics. The rule can be stated as:

$$R = AV^n \quad [22]$$

where

R = damage rate

A = a constant

V = applied voltage

n = a constant

If all other operating conditions, such as temperature, are held constant, then the acceleration factor relating two voltages is given by this rule to be:

$$\tau = (V_2/V_1)^n \quad [23]$$

where

τ = acceleration factor

V_2 = accelerated voltage

V_1 = lower voltage

Thus, if capacitors will fail at times t_2 at accelerated voltages, then the times t_1 to failure at lower voltages will be expressed by Equations [1] and [23]. The inverse power rule has been derived from the Eyring reaction rate model (Reference 8) by using $\ln V$ for the stress function therein. Weibull distributions have been used considerably in the analysis of capacitor accelerated data. A plot of constant voltage test data plotted on Weibull paper is shown in Figure 15.

In accordance with Equation [12] the test data at different voltages will plot as parallel lines. The horizontal spacing between the constant voltage lines is proportional to the difference in the logarithms of the voltages.

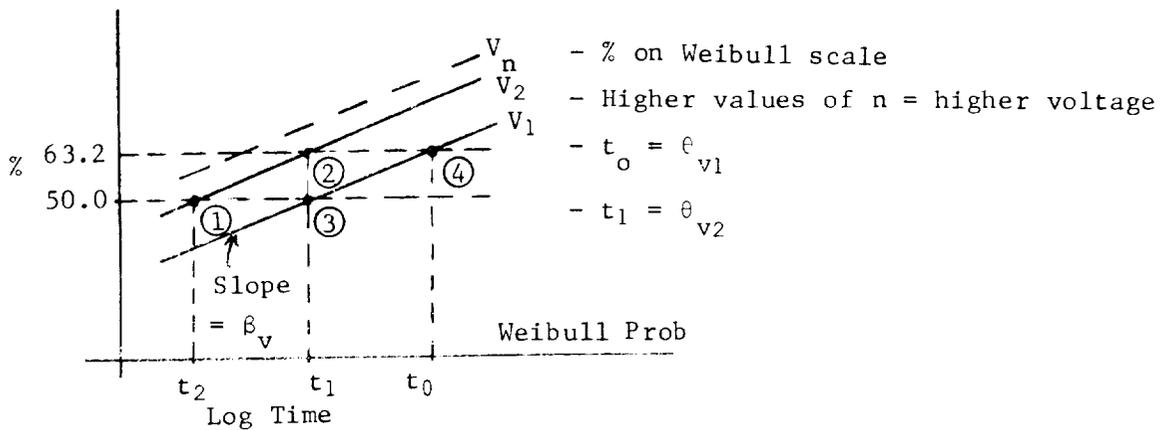


Figure 15 Weibull Plot-Constant Voltage

An equivalent plot is the constant time plot of Figure 16, which may be considered for voltage step stress data analysis of capacitors. From Equation [22] it can be determined that if failures have a Weibull distribution in time at constant voltage, then they will have a Weibull distribution in voltage at constant time. In Figure 16 the horizontal spacings between constant time lines are proportional to the differences in the logarithms of the time. Because the slopes in Figure 15 are equal, the lines in Figure 16 must also be parallel.

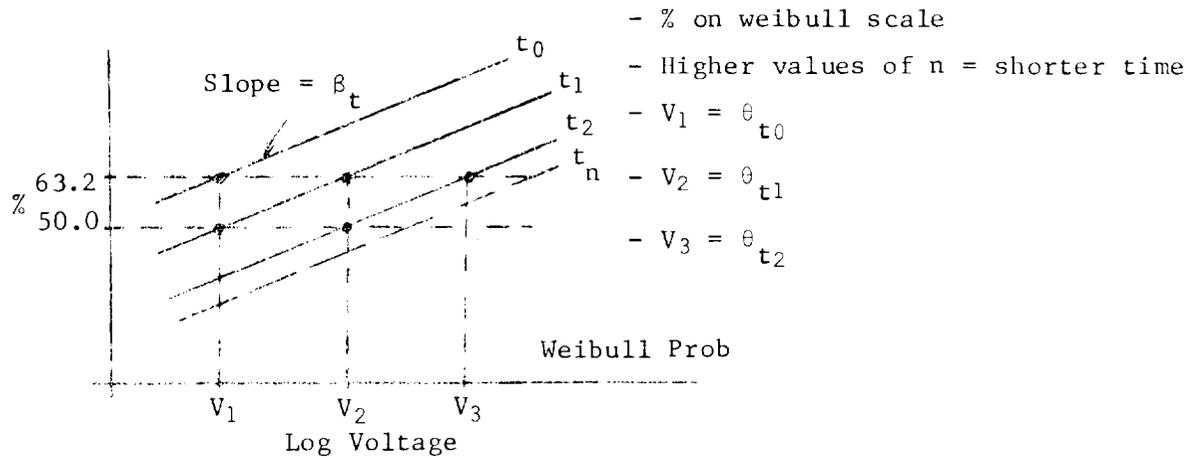


Figure 16 Weibull Plot-Constant Time

From either Figure 15 or 16, the regression plot of Figure 17 can be made. The numbered data points in Figures 15 and 17 correspond to each other. Using the 50% failure line in Figure 17, the regression curve slope is:

$$m = (\ln V_1 - \ln V_2) / (\ln t_1 - \ln t_2) = (\ln V_1 - \ln V_2) / \ln \tau \quad [24]$$

which is equivalent to equation [23]. The negative reciprocal of this slope is equal to the exponent n . Since the slope of Figure 17 is equal to the negative ratio of the slope in Figure 15 to the slope in Figure 16, another expression for m is:

$$m = -\beta_v / \beta_t \quad [25]$$

and

$$n = \beta_t / \beta_v \quad [26]$$

Also, in Figure 17, the acceleration factor $\tau = t_1/t_2 = t_0/t_1$ between voltages V_2 and V_1 . From the 63.2% failure line $t_0 = \theta_{v1}$

and $t_1 = \theta_{v2}$, therefore:

$$\tau = t_0/t_1 = \theta_{v1} / \theta_{v2} \quad [27]$$

in confirmation of equation [13].

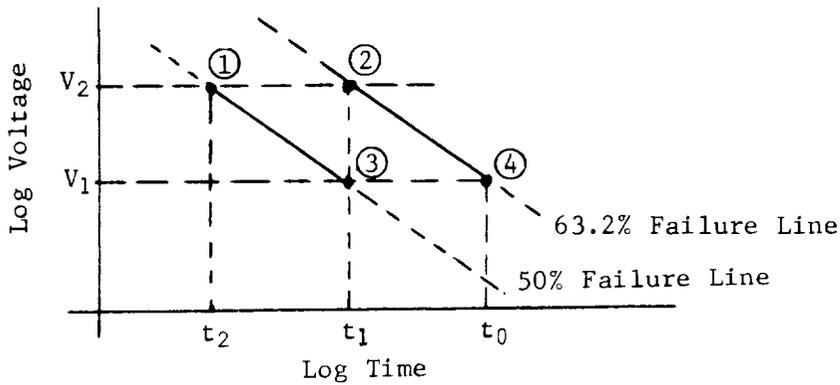


Figure 17 Inverse Power Regression Plot

f. *Step Stress Testing* - The concept of step stress testing was pioneered by Bell Telephone Laboratories (Reference 9). A wide variety of parts have been tested by this method, such as, germanium and silicon transistors, integrated circuits, resistors, capacitors, and diodes. References 8 through 12 are step stress test reports on these part types. The step stress test consists of testing parts at fixed time intervals and incrementing the stress in "steps." Figure 18 shows the process diagrammatically.

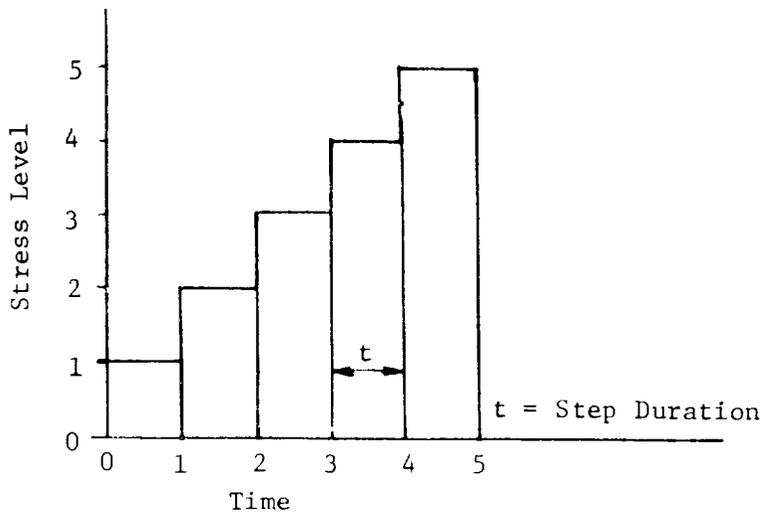


Figure 18 Fixed Time Interval Step Stress Test

The usual stress is temperature, power, or a combination of these. The Arrhenius model is used for all parts except capacitors where the inverse power rule is used. Parts are usually measured initially so that the test group is verified to be good and data is available for computation of parameter shifts. The test group is then entered into test at time 0 and stress level 1. They remain on test for the time interval 0-1 and then are removed from test and allowed to cool to room temperature. The parts are then measured again to determine if any failures have occurred. Failures are usually defined as parameters exceeding prescribed limits on values or deltas. Failures may be removed from the test group at this time for analysis or left in the group if higher stress effects on the part are still desired. Next the remainder of the group is placed on test again at stress level 2 for the time interval indicated in Figure 18 as 1-2, then removed from test and measured again. The step durations, or time intervals t from 0-1, 1-2, etc., are always equal. The stress increments are usually equal either in magnitude of each increment or in magnitude of a function of stress in each increment. For instance, in temperature step stress tests, the temperature increments are usually equal in degrees centigrade or equal in the change of reciprocal degrees Kelvin. The steps are continued until the desired number of failures are achieved, usually a minimum of 50% up to 100%. The failure distribution for the selected time interval and stress type is thus obtained. Cumulative failure data may be plotted as in Figure 10.

The assumption is generally made that damage achieved in previous steps is insignificant compared to that achieved in the step causing failure. The error introduced by this assumption is that the percentage accumulated failures attributed to a given stress level may be too high. A method of correcting for effects of previous steps is given in Reference 9. However, if any error exists, it is in a safe direction as the percentage failures are too high for the temperature against which they are identified. Also, if stress increments are sufficiently large, damage from previous steps is insignificant in comparison to that provided by the step where failure occurs.

The above procedure provides cumulative failure data necessary for construction of one of the constant time lines in Figure 10. The step duration is the constant time value. If a regression curve is desired such as in Figure 11, a minimum of two constant time lines are required. For any failure percentage, this provides two points on the regression curve. A separate group of

parts, each subjected to a different step duration time, is required for each point desired on the regression line. Three or more groups of parts will provide three or more points, and thus provide a check on results as they must be in a linear relation if the Arrhenius analysis is valid.

In some of the earlier works such as that reported in Reference 13, germanium transistors were step stressed with durations of 20 minutes, 2 hours, and 24 hours. The resulting failure rate predictions were compared to 25 million device hours logged in 1000 hours storage tests which provided the same estimates. It is reported that the first two computer designs utilizing these devices exhibited actual failure rates of 7 and 25 fits, respectively, while the extrapolation predicted 10 fits. Failure rates of silicon transistors used in the Ballistic Early Warning System's initial installation were also accurately predicted by step stress tests. Silicon transistors were tested in the temperature range of 150°C to 350°C. Sample sizes in such testing have generally been small, approximately 25 devices per group of parts (Reference 9). The number of steps used is approximately 5. Temperatures above 370°C cannot be used because new mechanisms come into effect (gold-silicon eutectic). Most testing is performed with a maximum temperature of about 300°C. As devices become more reliable, the step stress test becomes more difficult. Early devices tested with step durations of 2 to 10 hours could easily define failure distributions before new mechanisms were introduced. Many products produced after 1963 would not provide a reasonable quantity of failures in such short time periods. The step durations had to be increased to approximately 168 hours. Hence, as the product reliability is increased, the test time and the quantity of parts tested must be increased as the stress level is limited. The advantage over constant stress testing is greatly reduced. A product which will not demonstrate a failure distribution within 1000 hours at 300°C cannot be effectively step stress tested.

In performing step stress tests and plotting the cumulative failure distributions, as in Figure 10, results are often as shown in Figure 19. The change in slope is an indication that the original group contained inferior parts and were not eliminated until temperature T_1 was reached. If the inferior parts had not been in the original group, the distribution obtained would have been that shown by the dotted line having the same slope as the higher temperature failures, but displaced to the left because of lower cumulative percentages.

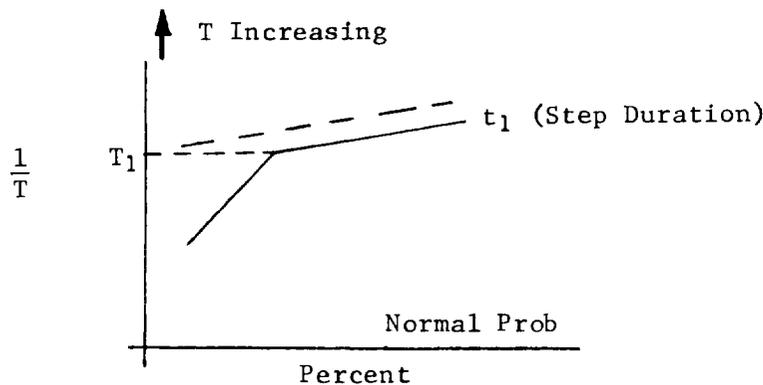


Figure 19 Distribution Curve With Breaks

This information is useful to determine more effective screen test levels. The damage supplied by temperature T_1 for time t_1 eliminates the inferior parts. A screening time and temperature providing equivalent damage can be selected from the regression curve of Figure 11.

The most powerful accelerated tests would be those where the models used and the constants therein are universal, i.e., they can be used regardless of part design or source. The approach is much less effective if new constants must be determined for each type of capacitor or transistor from each source. From results of step stress and constant stress accelerated testing at Bell Telephone Laboratories performed for more than 10 years, there is an indication that all diffused silicon devices with aluminum metallization exhibit an activation energy of approximately 1.07 electron volts. Current screening requirements for high reliability parts by Bell Telephone Laboratories are more severe than is usually required in the industry. Silicon transistors are usually screened at 275°C to 300°C for 20 to 100 hours. Integrated circuits are usually screened at 200°C to 250°C for 100 hours. Qualification life tests have also been performed at these levels for a maximum of four to five thousand hours or until a median failure level has been achieved. Step stress testing activity is decreasing and is used primarily on new parts. It is desirable to obtain unscreened parts for step stress testing to determine or verify screen test levels. With increasing part reliability, high temperature constant stress testing is more effective for determination of regression curves.

The question arises in high stress screening if the screening process itself consumes an inordinate amount of part life. With an activation energy of 1.07 electron volts, a 250°C test for 10 hours is equivalent to 4×10^6 hours at 60°C. If a part is screened at that level and then placed in service for 10 years (87,600 hours) at a junction temperature of 60°C, the total 60°C life requirement (including the burn-in) is 4.09×10^6 hours. The high temperature burn-in consumes more than 400 times the required service life. However, if the regression curve and constant temperature tests show that the parts have a median life of 1000 hours at 250°C, then the median life at 60°C is 4×10^8 hours. Ten years of operation after high temperature burn-in then constitutes approximately 1.02% of the median life. Reference 14 details procedures for analyzing data from accelerated test failure distributions and regression curves. Populations including "freaks" are considered. It is stated therein that considerable evidence supports the belief that the log normal distribution is appropriate for semiconductors and hazard rates are accordingly calculated.

Accelerated tests utilizing the Arrhenius model and the accompanying distribution diagrams and regression curves used for analysis require that a single process or mechanism is dominant in causing failure. Casually performing high stress tests and plotting curves can lead to erroneous conclusions and estimates. A break in the distribution as shown in Figure 19 could also be caused by a new mechanism becoming dominant. Reference 15 identifies many of the considerations and precautions in high stress test performance of semiconductors. Failure analysis should be performed to verify that the same mechanism is in operation. Because the activation energy is constant for the mechanism, a similar break would be achieved in constant temperature high stress test distributions (of the type in Figure 9) due to equation [19]. Although a single process is dominant in causing failure, there are certainly other processes in operation within a device at high temperatures. The amount of acceleration imparted to each process is a function of its activation energy. From equation [16] the acceleration factor for a given temperature difference can be determined for any activation energy. Assuming a maximum test temperature of 300°C and a low operating temperature of 35°C (not uncommon for some low power devices), the maximum acceleration factor achievable is shown in Figure 20 as a function of activation energy.

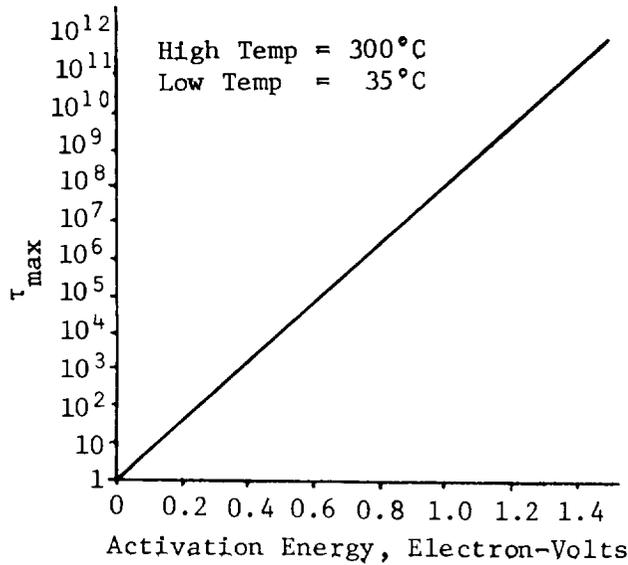


Figure 20 Maximum Arrhenius Acceleration Factor

Figure 20 shows that processes with high activation energies are more easily accelerated than those with low activation energies. Processes with an activation energy higher than that associated with the failures achieved are of no concern. However, low activation energy processes may not be accelerated enough to produce failure in the high stress test. Although undetected in the high stress test, they may be of concern in long service life applications as shown in Figure 21.

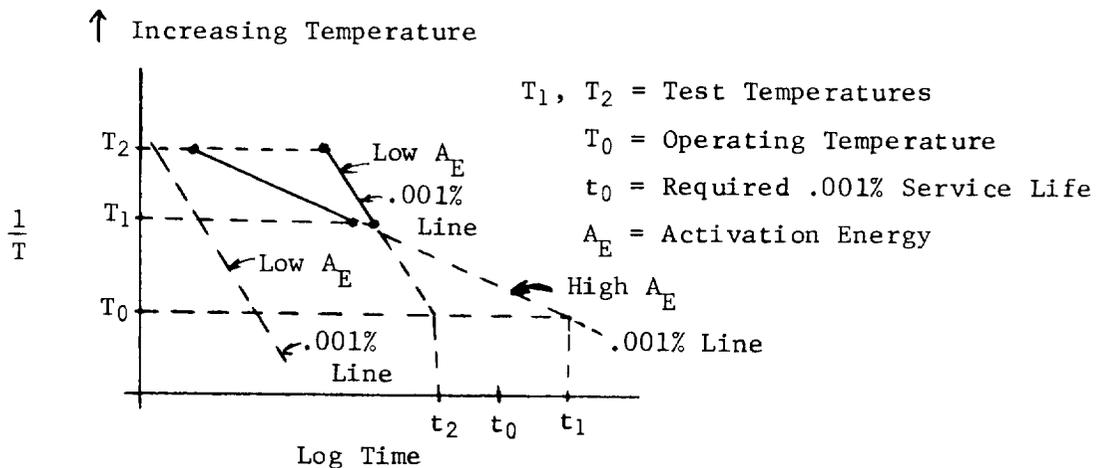


Figure 21 High and Low Activation Energy Regressions

Figure 21 shows that a low activation energy process may be the cause of failure in long service life applications instead of the higher activation process used for estimating hazards. For this situation to exist, the regression lines must be related as shown. If the low activation energy process 0.001% failure line is located as shown by the parallel dotted line, then failures from this process will be detected in short time tests or real time experience. Portrayal of this unique condition indicates the necessity for the fullest possible understanding of the construction, material combinations, and the mechanisms involved in parts used for long life missions, particularly in newly developed parts. It is desirable that all degradation processes applicable be easily accelerated and therefore have high activation energies. Low activation energy process evaluations can only be carried out in long-term tests, and such processes are life-limiting in long service life applications.

g. Constant Stress Testing - The simplest constant stress test merely consists of placing devices on test at a stress level in excess of the intended use level for a specified period of time. This is a common approach in sample lot acceptance tests and qualification life tests. In semiconductors, the temperature stress level is usually around 125°C junction temperature. The time periods vary, but 1000 hours is not uncommon. An individual test provides little information on the part, but large quantities of 1000-hour life test data are generated which provide insight into approximate failure rates of generic classes. Individual part types within a generic class, however, may vary considerably from the generic class rate. These simple tests demonstrate that the parts meet certain minimum requirements which, by experience, provide assurance of product quality. Other stresses commonly applied to parts as a means of providing assurance of product quality are centrifuge tests, vibration tests, and temperature cycling. The levels are generally far in excess of those anticipated in use, but are well within the capability of properly constructed parts. These tests do not provide margin, safety factor, or life distribution information.

If a failure distribution is desired, the constant stress test can be extended in time to partial or complete failure of the test sample. With moderate stress levels, a clear disadvantage exists because the test time for the majority of parts would be inordinately large. A means of reducing test time is to increase the stress level. If similar failure mechanisms occur at the

accelerated stress level as at normal use levels, extrapolation may be possible to other stress levels. Tests at more than one stress level will provide additional data for extrapolation.

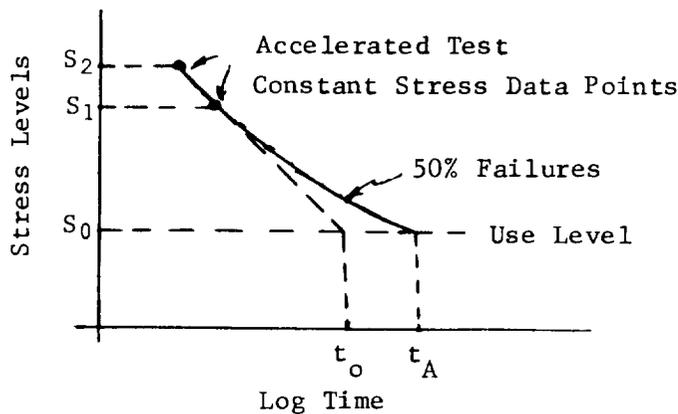


Figure 22 Constant Stress Extrapolations

One method which has been used to provide conservative estimates is that shown in Figure 22. Here the part is assumed to have a median failure line as a function of stress which is nonlinear as shown. The stress scale is usually linear unless the physical laws of degradation are known which relate degradation rate to stress. The time scale is logarithmic if large time extrapolations are being made. The actual time to median failure at the use stress is t_A . When a linear extrapolation through the accelerated test data points is made, the estimated time for median failure is t_0 . As the estimate t_0 is always less than the actual time for median failure t_A , the estimate is conservative. The assumption that t_A is greater than t_0 requires the failure line to have a continuously decreasing negative slope as stress decreases from infinity to the use level.

Instead of time on the abscissa, cycles have been used for parts such as relays and switches. This approach is very useful as it can be applied to any type of stress and knowledge of the physical relationship of stress to failure time is not required. The failure mechanisms operating at the high stress levels, however, must be the same as experienced in normal use. Methods such as step stress testing may be utilized in preliminary tests to determine maximum stress levels. A limitation is that this empirical approach provides no information on the safety factor existing in the conservative estimate.

The Arrhenius model provides more precise quantitative results and is useful for analysis of constant high temperature test data. The constant temperature failure distributions are plotted as in Figure 9 to obtain the regression curves of Figure 11. Again, it is often advantageous to utilize step stress tests in conjunction with the constant temperature test to determine temperature levels.

The versatile Weibull distribution is often used in analyzing constant stress data. Algorithms to compute the Weibull parameters by inserting values of temperature, current, voltage, etc. have been generated for specific parts. The disadvantage of these statistical approaches is that a physical model of the failure process or mechanism is usually lacking to justify the algorithm. Thus each algorithm is limited to the part statistically analyzed or to a narrow range of similar parts. Another approach which has been used on switches and relays is the assumption of a constant ratio of the Weibull hazard rates. (Reference 16). This approach uses an algorithm relating four sets of Weibull parameters. Two sets are those derived from (1) previous constant stress normal use, and (2) accelerated constant stress data. The third set is derived from present accelerated stress data. The fourth set is the predicted failure distribution of the group of parts from which the present accelerated data was derived. A disadvantage is that normal use distribution which require long test times must be obtained for each part type.

h. Progressive Stress Testing - Progressive stress testing is performed by increasing the stress at a constant rate. An example is the TGA tests of section C.2 in this report. Progressive stress testing in electronics has been performed primarily on capacitors where the inverse power rule is usually used, and the applied stress is voltage. The acceleration factor of equation [23] is no longer a constant, and equation [1] does not apply. If the rate (r) of voltage increase is constant, then the voltage (V) applied to the capacitor at any time (t) is:

$$V = rt \quad [28]$$

And from equation [22] the damage rate is:

$$R = Ar^n t^n \quad [29]$$

The cumulative damage (D) to a capacitor is the integral of this equation:

$$D = Ar^n t^{n+1} / (n+1) \quad [30]$$

If this capacitor is instead subjected to a constant voltage (V), the cumulative damage is:

$$D = AV^n t \quad [31]$$

If time t_1 is required to accumulate a damage level which fails the capacitor at voltage V_1 under constant stress conditions, then the time t_2 required to fail this capacitor with a progressive stress test is determined by equating equations [30] and [31]. The relationship between t_1 and t_2 is:

$$t_1 = (r^n / V_1^n) t_2^{n+1} / (n+1) \quad [32]$$

Weibull distributions have been applied to both constant stress and progressive stress test results. From equations [11] and [32], the exponents of t_2 are equal if:

$$\beta_2 / \beta_1 = n+1 \quad [33]$$

The relationships in equations [32] and [33] have been used to determine the values of n for various capacitors (Reference 8). If equation [32] is plotted on log-log paper using failure data from constant stress and progressive stress tests, the slope of a line such as the median failure line would have a slope of $1/(n+1)$ as shown in Figure 23.

The progressive stress test voltage at failure is rt_2 . If this is denoted as V_2 , then from equation [32]:

$$t_1 = (V_2/V_1)^n t_2 / (n+1) \quad [34]$$

which shows that when $V_1 = V_2$, or the constant stress test is performed at the progressive stress failure voltage, the progressive stress test failure time is longer by a factor of $(n+1)$ as illustrated in Figure 23.

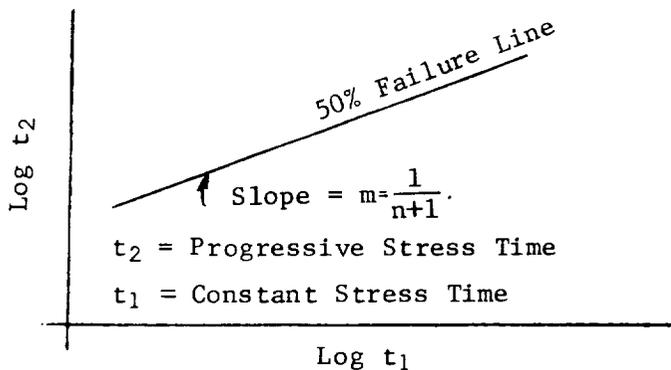


Figure 23 Constant and Progressive Stress Test Times

When progressive and constant stress Weibull distributions are plotted, the relationship of equation [33] appears as in Figure 24.

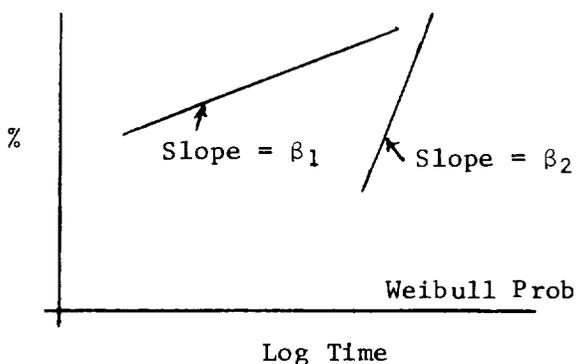


Figure 24 Constant and Progressive Stress Test Weibull Plots

The progressive stress test approach for parts complying with the inverse power rule must be performed with several precautions. The exponent n varies with temperature and, therefore, the temperature should be constant. The sensitivity of n to temperature varies with capacitor types. A small error in the estimation of n may produce large errors in the regression curve of Figure 17. The rate of voltage increase also must be maintained with precision. There is evidence that the inverse power rule itself may produce errors in long life estimates. For instance, storage age has been identified as influencing the value of n on some part types.

i. Electromigration - A model for electromigration induced failures of thin film conductors has been proposed which apparently resolves inconsistencies on this subject reported in previous literature. A report which derives the model is reproduced in Section D. Of particular interest is the dependence of the model on the thermal resistance of the thin film stripe to the substrate heat sink, as well as the grain structure node density function. As electromigration may be a life limiting mechanism of devices using thin film conductors, it is suggested that tests to quantitatively verify the validity of this model be performed. If the model is verified, then it would be possible to accurately characterize thin film strips under a wide variety of use conditions and to develop accelerated tests with improved predictive capability.

j. Summary - The various rules, approaches, and methods of analyses commonly used for electronic part accelerated testing have been briefly reviewed. Although quite varied, the test approaches contain one common factor--the stresses under consideration are increased above normal use levels. The variations occur in the types and combinations of stresses and the method of application. The purposes for performing these tests and the application of results are even more varied. For instance, the British Post Office Telecommunication Headquarters has recently utilized step stress tests (Reference 17) to establish threshold voltage drift specification requirements for MOS integrated circuits intended for long life usage. IBM used the Eyring model and accelerated tests to determine failure mechanisms and acceleration factors associated with voltage, temperature, humidity, and encapsulation of the flip chip mounting process (Reference 18). General Electric utilized step stress tests (Reference 19) in physics of failure studies on the double heat sink diode for product improvement and determining failure mechanisms, as well as methods of removal by initial characterization and stress screening. They also (Reference 20) utilized power and temperature step stress tests with steam pressure and high temperature humidity tests to evaluate plastic transistors with refractory/gold metallization, gold leads, and a new passivation. Bell Telephone Laboratories (Reference 21) used temperatures from 200°C to 300°C to determine long-term IGFET threshold voltage shifts and to determine a screen test that selects parts with long life stable characteristics. Boeing used high stress tests in centrifuge, thermal shock, current, and voltage in developing a reliability prediction model for microcircuits (Reference 22). The literature is voluminous on accelerated tests performed to determine or estimate margins, safety factors, burn-in levels,

failure rates, hazard rates, and specification requirements. They have also been used for qualification purposes, determination of failure mechanisms, evaluation of product changes, comparison evaluation between part types or sources, and monitoring of successive production lots for quality shifts.

In Reference 23 it is stated that the state-of-the-art in part level accelerated testing is far less advanced than generally believed. Evaluation of accelerated testing validity is based therein on the points of: (1) general acceptance of the statistical and engineering assumptions, (2) existence of an algorithm to connect accelerated test results to life estimates at rated stress levels, (3) existence of empirical proof that the algorithm yields accurate, repeatable results, and (4) existence of a physical model to explain observed results in terms of laws of failure. There is no known accelerated test that meets all four requirements.

Step stress and constant stress high temperature accelerated tests utilizing the Arrhenius or Eyring process rate models and log normal failure distributions meet all requirements except (1). There is some objection that all failure modes and multiple simultaneous process effects are not considered in use of the Arrhenius model. An associated factor is that the degree of acceptance of quantitative accelerated test results (such as prediction of hazard rates) is directly related to the confidence in the correlation between accelerated and normal use conditions.

Predicting a log normal distribution with a mean life of 4,600 years from small sample, high temperature tests is somewhat difficult for some people to accept. It is even more difficult to demonstrate. However, in References 14 and 15, a strong appeal is made for acceptance of this approach. Apparently, the amount of acceptance is increasing and the confidence of the user is seemingly directly related to the amount of experience he has in these methods. Undoubtedly, further progress in statistical methods and physical modeling to accommodate multiple processes and failure modes is needed. Use of accelerated testing has been of great benefit in understanding failure mechanisms. Apparently the obverse is true in that better understanding of these mechanisms benefits test design and performance.

The early work in step stress and constant stress as performed by Bell Telephone Laboratories on items such as germanium transistors derived estimates of failure rates which were actually verified in production systems. This work at high stress levels, however, led to many other benefits. For instance, when the

parts were taken to destructive levels, a more intimate knowledge was obtained of the ultimate capabilities or margins, as well as stress levels which induce new failure mechanisms. The stress levels which are most effective in eliminating marginal or weak parts were also defined with greater accuracy, as well as the probable consumption of useful life of good parts by these stress levels.

The true ratings of the parts were also determined which enabled application of derating practices less subjective. For the submarine cable life objectives of 20 years, these techniques were very valuable in enabling decisions on selecting parts from competitive sources, identifying optimum screen levels, estimating reliability, identifying part weaknesses and therefore areas for improvement, providing confidence in product integrity from lot to lot, applying derating more intelligently. The large amount of data and experience accumulated has enabled them to confidently apply stress levels to parts which make the standard screens seem benign by comparison. As indicated in the Study of Electronic Part Screening Techniques in this volume, this had led to the present situation where only a nominal amount of evaluation testing is required prior to implementing a high temperature screen.

The approaches identified herein have been applied primarily to discrete parts. Integrated circuits have also been tested, but additional problems arise with highly complex parts such as LSI and MSI. Any part which in effect is a complex circuit and may have fail-safe, feedback, or redundancy within it may make internal failures undetectable. Complex sequential logic devices are so difficult to test that it is impractical to perform periodic complete functional tests during a high stress test program. One approach is to incorporate test element groups which have terminals brought out for use in evaluating total circuit performance. Another approach is to utilize test vehicles which are constructed to representative or worst case construction features of the material/process combinations used in the production devices. These are used in accelerated tests to evaluate the production devices. Another approach which would evaluate the production internal geometries directly is to provide a special interconnection metallization pattern on the chip. This would bring external terminations to internal geometries of interest. These geometries could then be accelerated tested conventionally. Some manufacturers will provide the specially metallized parts, at times called "kit" parts, at nominal cost. This approach not only would bring internal transistors and diffused resistors to the

outside world for failure detection, but for controlled biasing purposes as well. Further study is needed on this subject as conventional approaches are inadequate and new approaches have not been developed sufficiently.

k. Conclusions and Recommendations - The state of the art in electronic part accelerated testing is represented by the step stress and constant stress approach utilizing the Arrhenius or Eyring process rate models. This approach can be used on all semiconductors and resistors. It is the most powerful in having application to a wide range of parts because of universal activation energy constants.

The inverse power rule and Weibull analysis approach represents the state of the art for accelerated testing of capacitors. It is less powerful because of limited range of application of the power exponent to different parts.

Statistically derived algorithms and distribution predictions represent the state of the art for accelerated testing of switches and relays. This approach is less effective because of the need to perform tests establishing the algorithms and the limited durability and range of application of the algorithms.

The other approaches considered can be useful for simple comparative parts evaluations or determining margins and safety factors.

Conventional accelerated test approaches cannot be satisfactorily applied to complex LSI/MSI parts. Further development of approaches to evaluate the basic material/process combinations and applying the results to the procured product is needed.

The imposition of a general program requirement for accelerated testing of electronic parts is not recommended. However, it *is* recommended that accelerated testing be selectively applied as one of the means of comparative evaluations of parts for: (1) addressing a known reliability problem, and (2) for obtaining accelerated knowledge of new part types intended for long life system usage.

5. Electronic Assemblies

a. *Introduction* - It is stated in Reference 24 that valid, quantitative accelerated testing on complete systems or major assemblies has never been accomplished. The reason for this is depicted in Figure 1. Nevertheless, qualitative accelerated testing of electronic assemblies is very widely and very beneficially used in the aerospace industry.

The accelerating stress is almost always temperature. The tests are usually more oriented toward improving reliability by detecting marginal designs, parts, packaging, and workmanship than they are oriented towards establishing a life prediction.

The forms of accelerated testing most commonly used are:

- 1) Burn-in at a constant elevated temperature;
- 2) Temperature cycling;
- 3) AGREE testing per MIL-STD-781B. This is a combination of the above two approaches, plus vibration;
- 4) Step-stress testing to failure.

b. *Burn-in at a Constant Elevated Temperature* - An industry survey of 26 companies accomplished during the study of temperature cycling is presented in the previous chapter. This survey indicated that over 90% of the failures occurred during the temperature ramps, during temperature tests consisting of both temperature changes, and soaks at high and low temperature. A few failures occurred during the constant temperature soaks. It was concluded that "black box" burn-in at a constant high temperature was much less effective than temperature cycling. However, one company, Radiation Incorporated, finds it valuable for stabilizing the performance of transmitters. Another application of high temperature burn-in is during development testing where it is desirable and permissible to exceed the qualification test temperature in order to accelerate and detect failures from hot spots, such as inadequate heat sinks on power transistors. However, it is usually a more reliable approach to actually measure the temperature of potential hot spots. Even though high temperature increases the failure probability, the failure may not actually occur during the burn-in period unless very long periods are used.

In summary, it is concluded that high temperature burn-in at qualification or acceptance test levels is relatively ineffective as compared with multiple temperature cycling. High temperature burn-in at levels exceeding qualification test levels should be considered for selective use during development testing, particularly on high power devices where the heat problem is significant. An extension of this concept is exemplified by the Grumman step-stress approach described later.

c. Temperature Cycling - Temperature cycling as applied to electronic assemblies is one of the most valuable and cost-effective tools available for achievement of increased reliability. In the interest of brevity, the reader is referred to Chapter II, which treats this subject. Temperature cycling should be encouraged and more widely utilized for the following purposes:

- 1) Development "black box" prototypes should be temperature cycled at the very earliest opportunity to verify that the packaging concept is sound with respect to adequate level stress relief and proper selection and application of conformal coatings or potting materials. Problems of marginal circuit design and with parts are also discovered early.
- 2) Acceptance testing should employ temperature cycling in accordance with the guidelines presented in Chapter II.
- 3) Qualification tests should employ sufficient temperature cycles to demonstrate that the production equipment will not be degraded by acceptance testing.
- 4) Temperature cycling should be also considered for application at the assembled PC board level, not only at the black box level. The Hughes approach (described in Chapter II) of temperature cycling PC boards, non-operating, and unmonitored, is especially attractive because of its low cost.
- 5) Multilayer boards should also be temperature cycled to ensure that later problems of cracking in the plated-through-holes do not occur.

d. AGREE Testing per Mil-STD-781B - This test, combining temperature changes, temperature soaks, and low level vibration is fully described in Chapter II. It is widely used by Wright-Patterson Field and the U.S. Navy. The industry survey described in Chapter II revealed that the principal benefit of the test is in the temperature changes. The temperature soaks and the low level 2g

vibration play a minor role. The conclusion that the 2g vibration is relatively ineffective is compatible with the MSC policy that the minimum effective level for acceptance test screening is 6g rms.

Data supplied by Collins Radio on many different equipments, and presented in Chapter II indicates that the measured MTBF during the AGREE test, was about one-fifth the predicted MTBF, indicating an acceleration factor of about five. Other sources believe the acceleration factor is significantly greater than five.

The traditional use of the AGREE test is a contractual reliability demonstration test in both qualification and acceptance testing. When used in this role, it is a very powerful forcing function for the achievement of reliability, because the contractor cannot deliver hardware until the measured failure rate has met the pre-established contractual requirements. Accordingly, when this approach is contractually implemented, it is important that the requirements are realistically set to achieve compatibility between both producer and consumer risks. Companies without prior experience with AGREE testing can be expected to be quite apprehensive. This apprehension may be reflected in high cost estimates.

e. Step-Stress Testing to Failure - Grumman has used step-stress testing of electronic assemblies. The test approach is reported valuable for reliability improvement, evaluation of sources, and as a design development tool. The concept is to detect and correct weak links until failures will only occur at conditions well outside of the expected operating envelope. For obvious reasons, this test approach is not suited for the qualification test or the production hardware. Reference 25 describes specific examples of this approach. These examples are abstracted.

Grumman utilized temperature, vibration, and humidity in combined environments. The environments were applied in increasingly severe steps to a prototype analog converter. The environments were increased to levels above expected black box use levels, but within the design limits of individual components in the assembly. The test specimen used was the first prototype which was similar to the final design configuration.

The first failure occurred at a temperature of 75°F and a vibration amplitude of 2 g's. This failure involved a servo amplifier which had been identified as the critical item in a previously performed reliability estimate and stress analysis. A major design deficiency was identified in the servo assembly. Design modifications were made and replacement with a design of a different form factor from a different manufacturer solved the problem. Other minor design rework to the analog converter solved other problems noted during test.

After four steps of overstress testing, the equipment could successfully withstand a vibration amplitude of 12 g's at a temperature of 175°F. Ten failures occurred during this period, were analyzed, and resulted in design improvements. Four additional stress steps were performed, and the test was terminated with the equipment operating successfully at 200°F at a vibration amplitude of 15 g's. (The qualification level was to be 10 g's at a temperature of 150°F.) Total accumulated test time in overstress testing was 156 hours.

The first developmental unit was subjected to a demonstration test without incorporation of the design changes identified in the overstress test. Seven failures occurred, five identical to failures experienced in the overstress test. The overstress test design changes were incorporated into the second development unit. From demonstration testing, it appeared that a minimum improvement in MTBF of 5 to 1 was directly attributable to the overstress tests.

A second example involved a design competition for a high voltage power supply for an airborne display system. Three sources were in the competition, funded to the same specifications which included functional requirements, the form factor, and the criteria for success. This criteria was not an MTBF demonstration, but a simple overstress test to failure on three units of each design. Detailed test procedures furnished to each competitor identified the techniques and environmental levels that would be used in evaluation. Each competitor was given access to the overstress laboratory. They were allowed to perform breadboard and prototype tests against the procedures furnished. No penalty was assessed for failures occurring during these developmental tests. All sources took advantage of the laboratory facilities. Two of the sources terminated overstress testing after the first series of failures, using these results as a basis for design improvement.

They did not utilize the opportunity to recheck the adequacy of their design changes. The third source made a concerted effort to continually check his design to higher levels of environment and initiating further design changes to correct the failures. As may be anticipated, the results of this competition were as shown in Figure 25.

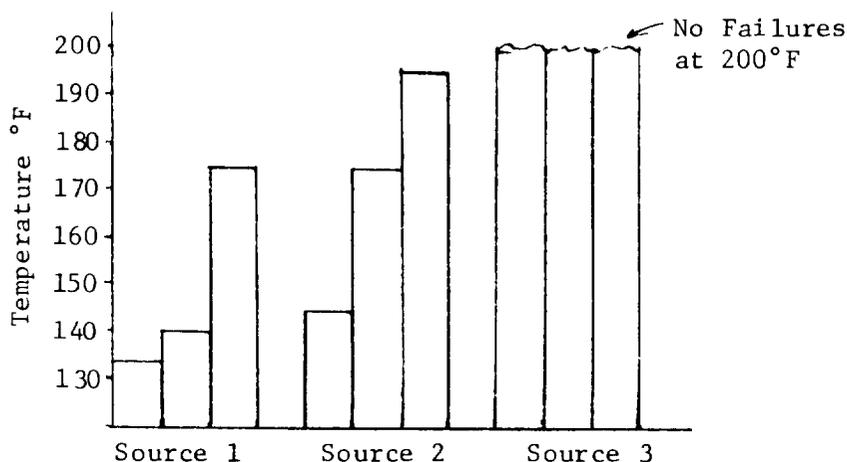


Figure 25 Temperature Test Results

Although vibration, altitude, and humidity tests were used in the competition, no significant effect of these environments was noted since much of the equipment was encapsulated. Not only did the first two sources fail at lower temperatures, but an inconsistency in the designs is reflected by the variations in ability of each assembly to withstand temperature. Test articles from the third source operated successfully up to 200°F without failure. The test articles from the third source were retained and accumulated more than 1700 hours of testing without failure at the time that the report was written.

The above examples from Grumman are cases where the overstress approach was of great value in obtaining design improvements and safety factors during hardware developmental stages. It is reported that more than 65% of the failures occurring under overstress conditions are duplicates of experienced operational failures.

An approach similar to this is recommended in Reference 24. It states that a series of subassembly tests should be performed during the early design phases at environmental levels somewhat above the normal stress level. Again, it is pointed out that the designer obtains information on the manner in which his design fails, and he can often redesign to provide a greater safety margin. All problems should be analyzed and resolved before design release. Although statistically significant reliability data is not derived, it is regarded as probably being one of the best techniques for improving and assuring reliability.

6. Mechanical/Electromechanical Hardware

Reliability data on mechanical hardware has been difficult to obtain because many mechanisms are specialized, few in quantity, designed for special applications, and have multiple failure mechanisms. Just how long a life a mechanism may have will depend on the existence of time dependent processes, such as wear, fatigue, and corrosion. Overstress testing, such as proof testing to verify a design or fabricated assembly, is common and establishes the initial capability to meet minimum requirements of strength. Other overstress tests have been devised to determine endurance limits of materials either to estimate life under cyclic loads or to determine safe loads which will provide unlimited life. Even on controlled material samples, variations in results are affected by specimen sizes and shape, surface finish, the method of fabrication, temperature, previous stress history, and test conditions. The only truly safe method of determining endurance limits of fatigue is to simulate the life load profile on an actual part.

The model generally used for fatigue is similar to the rate equation [22]:

$$D/N = AS^n \quad [35]$$

where D/N is the damage per stress cycle N , A and n are constants, and S is the stress which must be above the endurance limit. If the stress S_1 causes failure at N_1 cycles, the damage D_1 at that time is:

$$D_1 = AN_1S_1^n \quad [36]$$

If the damage accumulated at any stress is assumed to create failure when level D_1 is reached, then the cumulative damage criterion applies similar to equation [20] except that the number of cycles N is substituted for time, and L is cycle life. Equation [36], holding D_1 constant, produces the S-N curve of Figure 26.

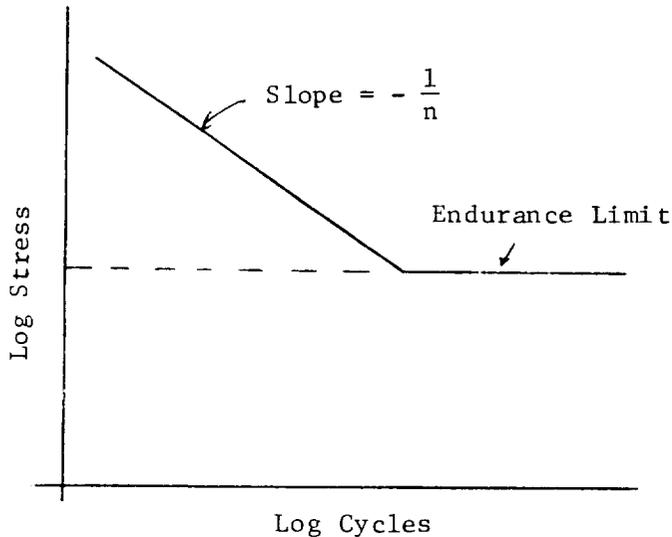


Figure 26 Fatigue S/N Curve

Much of the work in fatigue overstress testing has been applied to the determination of the S/N curve. Much conflicting data, not only between experimenters, but between successive results of the same experimenter, has resulted. The summation of equation [20], called Miner's rule, has varied from 0.18 to 23.0 (Reference 26). However, the usually accepted value is unity. The rule is also influenced by stress history. A high stress succeeded by a low stress will often produce results different than if the application of stress were reversed.

For the special case where $n = 1$, the S-N curve is a hyperbola on linear scales. A progressive stress test, known as the Prot test, has been used to determine the endurance limit. The stress is started at a level estimated to be below this limit and is then increased at a constant rate. The cyclic rate is held constant.

It can be shown from equation [35], when $n = 1$ and if the rate of stress increase is denoted as r , the stress at failure S_f is related to the endurance limit E by:

$$S_f = E + (2 D/A)^{1/2} r^{1/2} \quad [37]$$

This relationship is shown in Figure 27. The assumption that $n = 1$ is not a very satisfactory one for non-ferrous metals. However, the method has been used with promising results on Acrylics, Polystyrene, and Nylon (Reference 27). Although the approaches used for accelerated tests, such as the Prot method, and the models used, such as the cumulative damage criterion, are controversial in their assumptions, they have been utilized extensively in materials testing. The motivation is to reduce test time in determining material parameters. A critique of the cumulative damage criterion, and variations in techniques used to modify it and improve the accuracy, is given in Reference 28. An example of the variations obtained with Miner's rule is given in Reference 29 where it is shown that in some cases the rule was accurate or conservative, but in other cases was dangerous.

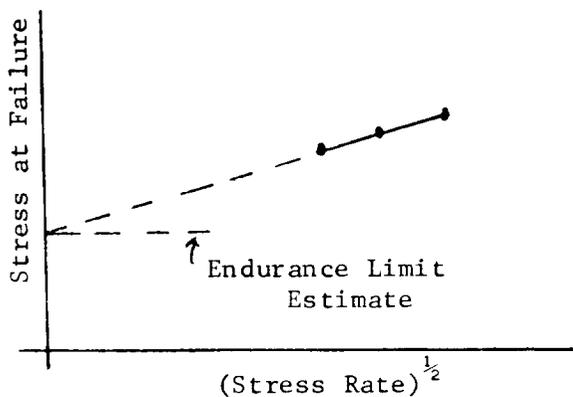


Figure 27 Prot Endurance Limit Curve

A material property that has been utilized with some success in accelerated testing is the threshold stress intensity factor required to produce crack growth by stress corrosion. Laboratory tests on 23 high strength ferrous alloy combinations were reported in Reference 30. These were 23 combinations of material,

heat treatment, and welding conditions. The accelerated test consisted of placing notched and fatigue-cracked specimens in a corrodant solution and tension loading them in a laboratory. Identical specimens were tension loaded in racks at the seacoast. The thresholds obtained from the seacoast environment were used as standards. Of the 23 material combinations, 20 showed agreement between laboratory and seacoast tests. The other three combinations showed differences which were attributable to experimental problems. The laboratory tests took a maximum of 1000 hours, which was one to three orders of magnitude lower than the seacoast tests.

Another material property successfully correlated in accelerated tests is the temperature relationship to creep. The relation proposed in Reference 31 is that for a given stress, the time t in hours to rupture, is related to the absolute temperature T by the equation:

$$T(20 + \log t) = \text{constant} \quad [38]$$

This relationship is based on the Arrhenius Model in equation [15]. Eight ferrous alloys were investigated and impressive correlations were obtained for rupture strength data between:

(1) 10,000 hours at 1000°F and 13 hours at 1200°F, (2) 1000 hours at 1200°F and 12 hours at 1350°F, (3) 1000 hours at 1350°F and 17 hours at 1500°F, and (4) 1.1 hours at 400°F and 1000 hours at 300°F.

Accelerated methods of obtaining material properties, such as fatigue endurance limits, creep rates at various temperatures and stresses, and stress corrosion threshold values are valuable, but difficult to apply in predicting the life of an assembly utilizing various materials. The stresses, wear, lubrication properties, etc., provide complexities which make it impossible to relate all life limiting basic material processes to the assembly life in operation.

An approach used on ball and roller bearings and gears has been employment of the inverse power rule similar to equations [22] and [35]. The stress is the load, and Weibull distributions are generally used for analysis. Another approach used on components is reported in Reference 32 and is called measured weakening. The technique consisted of pre-cracking a gearing mechanism to accelerate fatigue. It is reported that the gear when placed in system tests failed in 20% of the normal test time and introduced

no new failure mechanisms in the system. The test has value in that knowledge of gear life is obtained after a crack has been introduced. The real time to produce a crack due to overload, however, is uncertain and therefore the correlation to service life is uncertain.

An interesting investigation of the cumulative damage criterion was made in Reference 33. The criterion was used in tests on light bulbs, bearing balls, electric drills, and fractional horsepower motors. The failure diagram of Figure 13 was used as the basis for the test. Life tests were first carried out to failure at a high stress determining L_2 . A second group of specimens were then operated for a period of time t_1 at low stress, and then operated under high stress to failure which occurs at time t_2 if damage is cumulative. Two points on the cumulative damage line are thus obtained as shown in Figure 28.

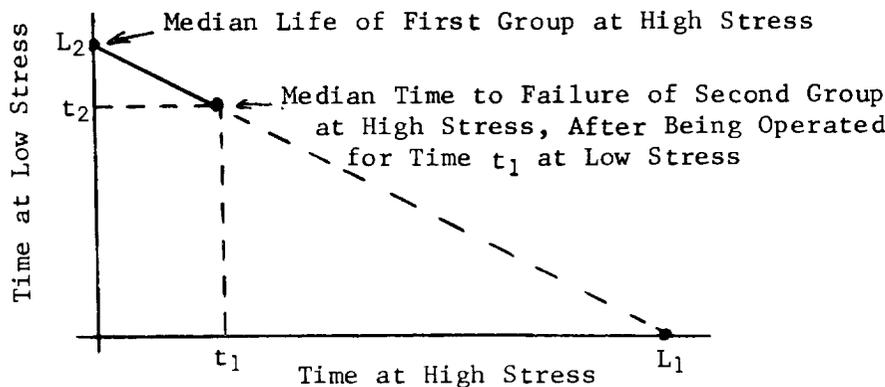


Figure 28 Cumulative Damage Curve Extrapolation

The median life L_1 at low stress is then obtained by extrapolation. The bearing balls were lubricated with turbine oil, and operated at 14,000 rpm. The high stress load was 600 lbs and the low stress load was 440 lbs. The electric drills were a low cost hand drill. For the normal stress test they were run unloaded continuously until the chuck ceased to rotate. Two high stress conditions were used; one with a fan load and the other with the fan in a box to increase the back pressure. The fractional horsepower motors were surplus items purchased in quantity. To induce failures within reasonable time, the lubricant was washed out of the bearings and distilled water substituted. This was the low

stress condition. Again, two high stress conditions were used. One was lubricant with 1% aqueous solution of sulfuric acid, the other was lubricant with 5% concentration sulfuric acid. In all cases, both high before low, and low before high stress sequences were used to further test the application of the cumulative damage concept to these parts.

The failure modes were, of course, diverse. The electric drills failed by wearing down of the brushes, the process being adhesive and electrical erosive wear. The fan increased the current and thus the erosion. The bearings developed spalls. The electric motors stalled due to a combination of adhesive and corrosive wear. The failure distributions of the bearings were Weibull, while that of the motors and drills were bimodal. The normal stress and accelerated stress distribution had the same form for each part type. It was concluded that the results were consistent with the cumulative damage concept even though three separate wear processes were occurring, that of surface fatigue, corrosion, and electrical erosion. The test results of all parts were grouped on one cumulative damage curve by normalization. Instead of actual time on the two scales of Figure 28, percent of life at high and low stress was used. All data followed the line well, except one bearing point. The data indicates that the procedure used in the test program could very well have wide application. Further investigation is needed in methods of applying accelerated stresses and in determining the parts suitable for testing by the cumulative damage criterion.

It appears that the state of the art in mechanical/electromechanical hardware accelerated testing is most advanced in the investigation of the materials of which they are comprised. Accelerated testing to determine creep properties is the most advanced. The other approaches such as Prot testing, the cumulative damage model applied to fatigue, and determination of stress corrosion thresholds are largely empirical and lack a physical foundation as applied. Accurate correlation, at the component level, of accelerated test results to normal use results cannot presently be made. The cumulative damage method at the component level appears promising, but needs further study.

7. Batteries

Demonstrating or determining battery life by accelerated testing is not currently feasible due to the many complex electrochemical reactions and the impact of externally applied environments and controls on these reactions. Material selection, manufacturing processes, proprietary additives in plate separators and electrolytes further aggravates the problem. In fact, there is a general feeling among battery experts, that accelerated life testing of batteries to obtain a useful and meaningful life prediction is impractical.

The problem of formulating a valid accelerated test is due to the complexity of the interrelated failure mechanisms, all of which are non-linear. The degradation characteristics are different between electrochemical couples. As an example of the complexity of the problem, the characteristics of the nickel-cadmium cell are described to identify the problems involved. None of the variables stated have linear relationships.

The normal reactions within a nickel-cadmium cell cause the cell efficiency to decrease resulting in an increase in thermal output as the temperature increases and the charge rate decreases. Average charge efficiency increases with greater depths of discharge, but decreases as the average state of charge approaches 100%. Life is dependent on the depth of discharge and the operating state of charge. Since the charge voltage varies with temperature, state of charge and charge rate, the charge control technique is a very important variable. In addition, orbital conditions, or cruise modes, significantly effect the life. Extended repetitive cycling, or float charge, depresses discharge voltages and limits effective capacity to a given voltage. Open circuit charge stand causes high end-of-charge voltages. Battery reconditioning can change the degradation characteristics and adds another unknown variable.

Even though a valid, "quantitative," test does not exist for batteries, "qualitative" accelerated test approaches, using high depths of discharge and increased temperature, are occasionally used in battery development and evaluation programs. They provide information on failure mechanisms and data for product improvement. However, as previously stated, such test results cannot be viewed as providing a valid and accurate life estimate for any specific set of projected usage conditions.

Present industry and government effort in the area of accelerated life testing of nickel-cadmium batteries falls into the following two categories:

- 1) Development of test methods for reducing the total time required for actual testing; e.g., possible substitution of 3 to 12 months of testing for five years.

In this category, is the work conducted by Battelle Memorial Institute for Goddard Space Flight Center up to mid-1970, and which is presently under investigation by the same organization for the Air Force (WPAFB).

- 2) Development of an analytical model for statistically projecting the cycle life of a battery system based on available life test data under various conditions of battery depths of discharge and temperature.

The work being carried out by the Naval Ammunition Depot (Crane, Ind.) is in this category.

These two activities are summarized below.

a. Battelle Memorial Institute - They have just completed studies of accelerated testing of secondary satellite batteries under USAF Contract AF33(615)-3701. The final report is scheduled for publication in late 1972. The study began with the development of general recommendations for the design and analysis of accelerated life tests. A mathematical model was developed based on stress-strain relationships involving temperature, voltage, gas pressure and mechanical parameters. Tests were conducted primarily on Ni-Cd batteries to determine the proportionality constants between stress and strain or between stress and rate of strain. Efforts were made to relate quantitatively with aging, failure mechanism and battery performance. Some of the stress levels acceptable for accelerated life tests were determined. The mathematical model was modified as tests data became available. However, it appears that accurate and valid correlation factors for real-time to accelerated time tests have not yet been established. Since the final report was not available at the time of this writing, detailed comments on the study results could not be made.

b. *Naval Ammunition Depot (Crane, Indiana)* - This agency has conducted life testing of batteries from all principal suppliers, under varying conditions of temperature and depth of discharge. Periodically, the failure data is analyzed and predictions are made of the future performance of those batteries not yet failed. These predictions are then compared with the actual failure data to determine the degree of correlation. These data have provided meaningful battery application guidelines relating to temperature and depth of discharge, but have not resulted in the development of a valid "quantitative" accelerated life testing technique universally applicable to batteries.

The life data presented in Reference 34 has been evaluated (Reference 39). Even with the limited data available, a semblance of a reduced life test program becomes apparent. It appears that in spite of the apparent variations in the Crane results, that the data is normal with few exceptions. As a result of this analysis, actual life testing can be reduced 50% by assuming a normal distribution and testing to failure only 50% of the test sample.

8. Bearings

The lubrication and bearing research section of NASA-LeRC reports that accelerated life testing is still in an embryonic stage. Valid quantitative methods are not available. There is little agreement between authorities on the best procedures to adopt.

Accelerated life testing of bearings, like batteries, is not developed to the point where there is a recognized, credible approach among bearing technologists. The RADC Handbook on Accelerated Testing Technology, Volume II, (Reference 3) describes an accelerated method where acceleration is achieved by increasing the radial load, increase the rate of wear in accordance with the empirically desired relationship:

$$L = \left(\frac{C}{P}\right)^3$$

Where:

L = Life in Millions of Cycles

C = Basic Load Rating

P = Actual Load

The above was based on the supposition that bearings fail from metal fatigue. Since this 1967 report, significant progress has occurred in the technology, such as the refinement of the Elasto Hydro Dynamic (EHD) theory of lubrication, and additional insights have been gained through spacecraft failures. For example, for long-life bearings, it is desirable to design them to operate in the EHD regime where the lubricant film is maintained thick enough to prevent asperity (metal-to-metal) contacts. In this case, bearing failure occurs not from metal fatigue, but from either degradation of the lubricant, or loss of the lubricant. However, this simple straightforward philosophy of life dependency has recently been clouded by the discovery that race degradation may still occur due to the penetration of the EHD film into surface microcracks, with consequent, high frequency pressurization of these imperfections. This results in surface fatigue regardless of the fact that there is not metal-to-metal contact.

Despite the uncertainties introduced by the above, LeRC bearing experts suggest that the most valid method of conducting an accelerated test of bearings operating in the EHD regime would be to achieve the acceleration by increasing the temperature thereby accelerating the loss of lubricant.

In the EHD lubrication mode, the lubricant film is sufficiently thick to prevent asperity contact, lubricant loss by evaporation or migration is the predominant failure mode. While failure from chemical degradation has not been uncommon (due usually to excessive heating) it should be possible to avoid this type of failure by proper design and lubricant selection, and thus should not constitute a valid failure mode for accelerated testing.

A feasible basis for accelerated testing in the EHD mode is to operate at elevated temperature thereby increasing the rate of evaporation. Increased temperature will also lower viscosity which will decrease film thickness, but as long as EHD conditions are maintained this should be of little concern. An alternate approach would be to compensate for the loss of film thickness by increasing the speed. Predicted life would then be a function of the Evaporation Rate Ratio times the Accelerated Test Life. The effect of migration would probably have to be assessed by separate experiments to determine the affect of the temperature on migration for the particular bearing and associated lubricant reservoir. The latter effect would be affected by the influence of the zero-g environment on the mechanics of surface energies.

In the case of boundary lubrication, the situation becomes more complex. More parameters must be contended with, and failure by wear becomes a concern. Evaluation tests should be first employed to limit potential accelerated life test approaches to the most promising candidates.

A paper by Meeks, Christy, and Cunningham of Hughes Aircraft (Reference 35) presents a number of considerations in accelerated testing. This section of their paper is presented in its entirety:

"Any attempt at accelerated testing of ball bearings must consider the probable failure modes and attempt to isolate the effects of any acceleration factors introduced and to relate the results to actual performance at design conditions. The three most likely modes of failure of lightly preloaded, well designed, satellite despin bearing systems during a 10-year operating period are: (1) lubrication degradation due to chemical contamination, polymerization, decomposition, and/or catalytic effects of bearing component materials; (2) loss of lubricant due to evaporation or surface migration; and (3) cage, ball, and race wear or damage.

"Lubrication breakdown due to causes such as temperature effects, catalytic effects of wear particles, or contamination is very difficult to evaluate except by real-time testing. However, a combination of laboratory chemical analysis and bearing testing can yield valuable insight into long-term performance that might be expected.

"Lubrication loss by evaporation and/or surface migration can be predicted analytically by molecular-flow theory and estimated by surface-physics theory. Localized effects of small thermal gradients, bearing and housing geometry, and surface barrier coatings can appreciably affect performance, however, and attenuation must be given in design, and results confirmed by test, to achieve optimum oil supply control system performance. Bearing test temperatures can be raised to accelerate lubricant losses; however, the results must be interpreted in light of thermodynamic flow loss, and surface-physics loss theory. The lowering of viscosity by elevated temperature also reduces bearing hydrodynamic oil film thickness unless the rotation speed is changed to produce a compensating effect.

"Wear is significantly affected by lubrication film thickness, and any attempt at accelerating life testing should maintain film thickness representative of the actual application. Film thickness can be varied by increasing preload and rpm, which will accelerate bearing wear but in a manner less predictable than the lubricant evaporation because the wear rate is affected in a complex way by preload, which affects the amounts of sliding and of fatigue wear. Many other variables must be considered, such as microscopic asperity temperatures, oil viscosity pressure coefficients, ball-cage dynamics, oil distribution and transfer dynamics, and time-dependent lubricant chemical changes."

Reference 35 also reports on an "accelerated" life test program. However, it should be emphasized that the tests were not true accelerated tests, but a program in which real-time (non-accelerated) test results from 220 days of vacuum testing were *extrapolated* to provide life estimates. In these tests, two different lubricants were used: Versilube F-50, and a hydrocarbon oil having a high pressure additive. Bearings were tested at 55, 120, and 180 rpm's and at three preload levels; 10, 20, and 40 lb. The test was conducted at 54.4°C to control the oil-film thickness to boundary lubrication levels (i.e., no significant elasto-hydrodynamic film load support) that occur in typical satellite despin bearings.

The measurements recorded during the test were: (1) bearing torque, (2) temperature of the outer race of one bearing in each module, and (3) electrical resistance through the bearings. The electrical resistance was measured at periodic intervals by an electrical contact attached to one outer race of each bearing pair. The current path was from the outer race, through the bearing balls, to the inner race, and thence to a common shaft and slipring. The test current used for this measurement was 100 μ A. This measurement is used to establish the percent metal-to-metal contact occurring; i.e., detect the extent of boundary lubrication operation.

Analysis of the ball-to-race contact resistance data demonstrated that the 55-rpm bearings were operating entirely in the boundary lubrication regime, and the 120- and 180-rpm bearings were in the transition regime between boundary and hydrodynamic lubrication.

The oil losses from the modules showed an average rate of approximately 25 mg/year, which is within the range of predicted rates and is easily tolerated because several hundred milligrams of oil can be stored in a bearing system of this size.

The oil in the F-50 lubricated bearings had polymerized extensively in the low-speed and high-preload modules and less so in the high-speed modules. An excellent inverse correlation between theoretical oil-film thickness and amount of polymer was observed. The reason for this is believed to be the very high temperature, hundreds of degrees Fahrenheit, produced at the microscopic asperity contact points occurring with very thin oil films. This produced polymerization of the F-50. F-50 oil polymerizes or cross-links at approximately 600°F.

From these tests, the effects observed were extrapolated to make estimates of probable bearing/lubrication system life. The estimated life of F-50 lubricated, small-size bearings at 55 rpm's before significant torque fluctuations (greater than two times average) occur, is less than one year, due to thermally induced chemical changes in the oil. The ultimate failure life of such bearings lubricated with F-50 was conservatively predicted to be probably less than two years. The hydrocarbon-lubricated bearings could be expected to last considerably longer than two years with uniform torques. The oil supply losses were low enough for up to 10 years life for either lubricant. Quantitative measurements of wear showed that wear is inversely proportional to oil film thickness.

From the analysis of the data from these tests, several factors offer encouraging support for the validity of carefully controlled accelerated bearing tests. Very good correlation was observed between: (1) predicted film thickness in the boundary regime for the 55-rpm bearings, (2) the transition regime (between boundary and elasto-hydrodynamic) for the 120- and 180-rpm bearings, and (3) the ball/race electrical contact resistance data. Also, the amount of oil polymerization and wear in the 55-rpm bearings with F-50 lubrication (which operated entirely in the boundary lubrication regime) were much higher than the amounts in the 120- and 180-rpm bearings (which were in the transition lubrication regime). This agrees with prior bearing testing that shows high microscopic-asperity temperatures occur in pure boundary conditions, becoming progressively less as hydrodynamic conditions are approached.

The final conclusion was that more work must be done before highly accurate correlations of accelerated test results and real-time conditions can be attained.

In the case of reusable vehicles like the Space Shuttle, the major problem is not one of developing very long-life bearings, but bearings which will withstand many repeated missions with vibration levels appreciably exceeding Apollo and Skylab levels.

Vibration shortens bearing life by causing fretting corrosion (false brinelling). The achievement of long-life bearings then hinges on designing the bearing system to prevent the occurrence of fretting corrosion. It therefore appears that the allocation of technical resources for the Space Shuttle in the bearing area would be better directed towards this life-shortening vibration problem rather than towards the development of valid accelerated life tests. Of course, an accelerated life test employing vibration as a primary degrading mechanism, would be a viable subject to pursue for reusable space vehicle applications.

9. Valves

Most valve specialists believe present accelerated testing methods are unreliable, but utilize them since more valid techniques are not available.

Accelerated testing of valves is generally accomplished in several phases, and not by a single test. For example, the cycle life of the valve is commonly verified by using an increased cycle rate. Although this test is very widely used, it does not cope with time-dependent phenomena which may be present such as creep, corrosion, metal diffusions, etc. For long life valves, it is desirable, but not always feasible, to design out or minimize the time-dependent failure mechanisms. When this is accomplished, the increased cycle rate test yields a valid cycle life projection. The cycling rate must be constrained to prevent secondary effects such as local depletion of lubrication, local hot spots due to friction, or overheating due to power of the solenoid.

When time-dependent phenomena are present, these must be identified and subjected to the appropriate test evaluations which, in many cases, can be accelerated by increasing the temperature. A classic example of an aging mechanism that is somewhat independent of cycle life is the cold flow or creep that may occur during long dormant periods with a valve with a Teflon seat or poppet. It has been demonstrated that Teflon seats with unit stresses to

4000 psi can be designed for long life with very astute seat design. However, an accelerated high temperature test is needed to verify the absence of cold flow. Empirical data from Martin Marietta Aerospace indicates that 2 weeks at 148.9°C should demonstrate a 10 year capability for valves operating at or below room temperature, but experimental data is required to validate this conclusion.

Another example of an aging mechanism is the potential bonding of the seat and poppet when subjected to high bearing stress for long periods of time. This problem is addressed in a current study by TRW for JPL (Reference 36) is entitled *Study of Advanced Techniques for Determining the Long Term Performance of Components*. TRW conducted diffusion tests in which copper and chromium plated Inconel, representing the seat and poppet materials, were clamped together with a load of about 33,000 psi and subjected to 500°C for times of 10, 200, and 400 hours. Bonding did not occur, and since it was estimated that the acceleration factor of the 500°C test was about 100, this junction would not experience bonding for at least 5 years. Although bonding did not occur, mechanical adhesion did occur. The adhesive was due to deformation of the copper, causing it to be "locked in" on the uneven surface of the chromium. TRW concluded that this technique appeared valid for evaluating metal seat-poppet couples. They plan additional work in this area. It was recommended that corrosion tests should also be accomplished before and after diffusion to establish if any net material transfer affects the extent of corrosion or its mechanism.

Yet another example of aging and environmental mechanisms is in the valve solenoid. Long term stability of the potting compound needs to be verified by materials testing methods such as the Thermogravimetric Analysis technique. Accelerated temperature cycling should then be conducted on the potted solenoid to establish compatibility between the thermal expansion characteristics of the potting and the small wires which are more subject to failure with hard, non-resilient, potting compounds.

TRW (Reference 36) also reports on a study of acoustic signatures. This subject is also under investigation by GE (Reference 37). The transmittance of acoustic energy through a component provides a sensitive method of detecting changes or anomalies in the discontinuities within a valve. A change in the signature can be an indication of a degradation or aging process or an indication of

a defect. This technique is not in itself an accelerated test method, but it is an instrumentation method with the potential of detecting and measuring some aging phenomena. In some cases, the trend data could probably be extrapolated to provide an end-of-life prediction.

10. Transducers

Most transducers do not have wear-out failure mechanisms, but are subject to long-term drift and stability problems. This is particularly true of pressure transducers. In general, the transducer industry does not consider accelerating testing as trustworthy. They have not developed or utilized it to a significant extent. Accelerated approaches to demonstrate long-term stability should be developed and employed to a greater extent, particularly on newly developed instruments with unproven stability. On strain gage pressure transducers where the diaphragm is operated at less than 40% of the yield, the life of the diaphragm is considered to be several million cycles; and the use of accelerated pressure cycling is not deemed necessary. However, with potentiometric types where wear of the wiper and resistance element is the major life limiting factor, accelerated pressure cycling should be employed to demonstrate life. The use of accelerated temperature cycling should be widely employed to access long-term stability of pressure transducers. For example, one manufacturer who felt that his device was stable, was very surprised by the loss of stability which resulted from a few temperature cycles.

Most pressure transducer manufacturers use less than five temperature cycles as part of the acceptance test to demonstrate stability. It has been concluded from experience at Martin Marietta Aerospace that five cycles is the absolute minimum and that 20 cycles should be considered for long-life applications. These temperature cycles should exceed the usage environment, operating and non-operating, by a margin of about 30°F on both the high and low extreme. This test should be preceded by the conventional heat treat or high temperature annealing process which eliminates welding stresses and other localized areas of high stress.

Accelerated temperature cycling is also applicable to some types of temperature transducers where there is concern about either the permanence of the hermetic seal or the integrity of internal electrical connections.

Many transducers are supplied with electronic hardware. In such cases, the approaches discussed for electronic parts and assemblies are applicable.

There are literally hundreds of different transducer designs. The effective application of accelerated testing must be based on a study of the design details and the potential life problems associated with a specific device. The above generalizations are intended as a guide for establishing a test program for a specific device. When mature devices are selected with proven long-term stability, using real-time tests conducted over a period of many months, there is little justification for accelerated testing. However, many devices are now employing new concepts and approaches; and accelerated testing is desirable for assuring long-life. In developing a new transducer for a long-life application, it is desirable to design out all potential aging phenomena. Elimination of all non-metallic materials is a significant step towards this goal. One example is the thin-film-strain-gage-pressure-transducer.

11. Enhanced Defect Testing

Enhanced defect testing could be considered a type of acceleration testing in that data defining the most significant failure modes is gained very rapidly. This is because defects are intentionally enhanced and failures are then forced by the application of stress exceeding usage conditions. This type of testing is obviously constrained to the research and development area. It is used to gain knowledge about the significance and consequences of various defects in a given item of hardware. A classic example is the work of H. C. Hurley of IBM. This enhanced defect test program provided major insights into the life and reliability problem of the Multilayer Printed Circuit Board (Reference 38). In this program, many different multilayer boards were fabricated with various design parameters and with many processes out of control in order to introduce a series of controlled defects. Boards were fabricated with good and poor lamination quality, with holes drilled both clean and with smeared epoxy, and with both ductile and brittle copper in the plated-through-holes. The boards were then subjected to accelerated temperature cycling (3 hour cycles from -65°C to 110°C) until electrical failures occurred due to cracking from the mismatches of thermal expansion within the board.

This program revealed that the particular defect of brittle copper is the major concern. Smear drilled holes contributed to failure to a lesser extent, and lamination defects played a minor role.

The effects of copper layer thickness and hole design were also evaluated; but the most significant finding was that the defect of brittle copper in the plated-through-holes was extremely serious, overshadowing most other defects.

The approach of Enhanced Defect Testing should be considered for application in the research and development of new and critical products when the relative failure mechanisms need to be identified and assessed.

12. Dynamic Mission Equivalent Testing (DME)

This testing, applicable to a total spacecraft at the systems level, is an accelerated test in the sense that it is a mission simulation test excluding the non-operating, dormant, periods. For example, a nine-year Jupiter-Saturn-Pluto Grand Tour mission could be simulated by ground systems testing in 119 hours; a time compression of 663 to 1. Critical environments can be applied during the test and the total mission simulation can be repeated to increase the level of confidence.

DME is a form of compressed time testing developed by JPL where non-operating periods are omitted in a manner similar to conventional accelerated cycle testing of valves and relays. Dynamic mission equivalent testing basically applies this time compression approach at the systems level. Aging phenomena not dependent on cycle life or operating time must be evaluated by separate test programs.

Many spacecraft components operate for only short durations followed by a long duration of quiescence. A major portion of the failure probability occurs during either the relatively short operating periods and/or relatively short periods of environmental stress. It is often feasible to eliminate or shorten the quiescent periods in order to accumulate many cycles of testing. DME testing is a technique for organizing test planning to optimize test effectiveness via selective simulation of mission stress cycles thereby achieving significant time compression. DME does not depend upon stress acceleration, hence, it can be used on flight equipment. DME techniques can be applied to either component or system level tests. To be valid, the DME test technique must consider all functional and environmental parameters which can affect life or reliability. Caution must be exercised to be certain that a component does not in fact degrade sufficiently during quiescent periods to nullify the validity of shortening these time periods. In general the DME approach is:

- 1) Define mission profile;
- 2) Subdivide profile into dynamic (non-equilibrium) and static (equilibrium) portions;
- 3) Eliminate/reduce static portions where all parameters are simultaneously quiescent;
- 4) Compress the time profile when one or more parameters are always dynamic (changing) by accelerating the rate of change in the parameter (but only when component response is not affected);
- 5) redefine the mission profile for test purposes incorporating Items 3) and 4) above.

To illustrate the use of the DME techniques, Table 2 is presented. A Jupiter-Saturn-Pluto Grand Tour mission is used as the example. For each mission phase, the approximate DME test time has been estimated. The durations of the real-time mission phases are cursory estimates. The test time for the J-S-P mission (nine years) can be compressed to 118.8 hours; a time compression of 663 to 1!!

DME, as used by JPL, does not employ acceleration by raising stress levels. It is recommended that consideration be given to the merits of incorporating acceleration by also employing thermal cycling during the test sequence. This would be especially valuable during development testing, and as a final screening test, along with thermal vacuum testing, on the flight spacecraft.

As indicated, the DME technique reduced the test time by a factor of 663 to 1. The test specimen could be subjected to one complete DME environmental cycle (118.8 hrs) in one five-day work week. The test cycle should be repeated until sufficient confidence in test specimen performance is gained.

Please note that Table 2 is for illustrative purposes only, although based upon a *projected* J-S-P Grand Tour mission profile. The profile assumed seven trajectory modifications (burns). Communications and tracking are ON 40 days prior to trajectory modification. All equipment is turned ON about 3 days prior to planet encounters. In addition to the DME test cycle, some equipment must be subjected to additional life cycling--such as the attitude control system which is operating during the entire mission; the cycling of valves and engine burns could be accomplished in separate high frequency cycling tests.

Table 2 Test Time Comparison for a Jupiter-Saturn-Pluto Grand Tour Type Mission

Mission Phase	Mission Time, hours	DME Test Time, hours
1. Launch	0.13	0.13 (once only)
2. Earth Orbit	0.50	0.50 (once only)
3. Trajectory Boost	0.10	0.10
4. Tracking & Communicaton ON	240	0.20
5. Trajectory Change	0.05	0.05
6. Cruise, Quiescent	10,871	6.00
7. Tracking & Communication ON	960	0.20
8. Trajectory Change	0.05	0.05
9. Cruise, Quiescent	108	6.00
10. Jupiter Encounter, all ON	84	1.00
11. All ON, Dump Data	24	24.00
12. Tracking & Communication	216	0.20
13. Trajectory Change	0.05	0.05
14. Cruise, Quiescent	12,635	6.00
15. Tracking & Communication ON	960	0.20
16. Trajectory Change	0.05	0.05
17. Cruise, Quiescent	115	6.00
18. Saturn Encounter, all ON	65	1.00
19. All ON, Dump Data	24	24.00
20. Tracking & Communication	216	0.20
21. Trajectory Change	0.05	0.05
22. Cruise, Quiescent	25,080	6.00
23. Tracking & Communication	960	0.20
24. Trajectory Change	0.05	0.05
25. Cruise, Quiescent	25,080	6.00
26. Tracking & Communication	960	0.20
27. Trajectory Change	0.05	0.05
28. Cruise, Quiescent	180	6.00
29. Pluto Encounter, all ON	60	1.00
30. All ON, Dump Data	24	24
Total Hours:	78,863	118.85
Time Compression:		663 to 1

The DME times were based upon the following assumptions:

- 1) The quiescent cruise phases are adequately simulated by allowing the equipment to cool off, about six hours;
- 2) The tracking and communication equipment life is degraded primarily from ON-OFF cycling that produces thermal cycling and electrical transients. This equipment should be temperature stabilized in about 0.2 hours;
- 3) The more severe equipment stress and wear occurs during the post encounter period when all equipment is operating and data continuously transmitted. Full real-time testing is deemed necessary for these three 24-hour mission phases;
- 4) All testing is in a thermal-vacuum test chamber that simulates the expected spatial environments;
- 5) Tracking and communication equipment are turned ON 40 days prior to a trajectory change (burn), time scales permitting, and;
- 6) The observatory periods (cameras on) are encounter minus 50, 75, and 250 days for Jupiter, Saturn and Pluto respectively. The observation periods are not reflected in Table 2. Adjustment in DME should be made for affected components.

D. A STATISTICAL MODEL FOR ELECTROMIGRATION INDUCED FAILURE IN THIN
FILM CONDUCTORS

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A STATISTICAL MODEL FOR ELECTROMIGRATION
INDUCED FAILURE IN THIN FILM CONDUCTORS

by

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ABSTRACT

A Statistical Model for Electromigration
Induced Failure in Thin Film Conductors

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A statistical model has been developed that relates the electromigration-induced failure rates of metallized conductors to the physical processes that cause such failures. The analytical formulation of this model suggests: i) a resolution of the controversy regarding the relationship between mean times-to-failure and the current density, ii) a potentially more useful statistical analysis for failure rates, and, iii) the possibility that electromigration failure rates and their statistics may be computed after making only a few simple measurements to characterize the system.

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I. Introduction.

Electromigration induced failures in thin metallized stripes have received considerable attention in recent years, but the usefulness of this work has been limited by the lack of a well defined statistical model that would permit relating conductor lifetimes to specific physical mechanisms. For example, considerable uncertainty remains regarding the correct method for extrapolating the results of accelerated tests, obtained at high current densities or elevated temperatures, to predict mean times-to-failure under normal operating conditions. Moreover, no physical basis has been provided to justify the common use of lognormal statistics in the analysis of experimental data. In this investigation, a statistical model that appears capable of resolving these and other questions has been developed and compared with previously published data.

II. Electromigration Damage Mechanisms in Thin Metallic Conductors.

According to the theory of current-induced mass transport developed by Huntington and Grone,¹ the driving force for electromigration arises from the momentum exchange between moving conduction electrons (or holes) and the atoms comprising the conductor. The process is related to ordinary

thermal diffusion, which, however, is perturbed by the fact that atoms are assisted across their saddle point positions into nearby vacancy positions by a force resulting from the presence of the "electron wind."

The rate at which atoms move under the influence of the current flow is controlled by both the temperature of the conductor and the strength of the electron wind. These two factors have been included in the expression for the velocity of atomic migration, v , derived by Huntington and Grone:¹

$$v = (j\rho Z^* e) [D_0/kT] \exp(-Q/kT), \quad (1)$$

in which the first term in parentheses is the driving force provided by the electron wind, the second term is the temperature dependent mobility of the atoms; and j is the current density, ρ the resistivity of the conductor, $(Z^* e)$ the effective charge of the migrating atom, $D_0 \exp(-Q/kT)$ the diffusion coefficient, Q the activation energy for diffusion, k Boltzmann's constant, and T the temperature of the conductor.

Experimental measurements on bulk conductors in which dimensional changes, or marker motion, are monitored during the electromigration process have, for the most part, established the validity of equation (1).^{1,2} However, the mechanism of uniform thinning by mass migration is not sufficiently rapid to account for the failure rates observed in thin film stripes. At least part of this discrepancy arises from finite divergences of the atomic flux that are generated by temperature gradients or structural inhomogeneities.^{3,4,5}

1) Temperature gradients.

Since the atomic velocity given by equation (1) is dependent upon temperature, local temperature gradients will cause a divergence in the atomic flux. For an electron conductor, such as aluminum, a depletion of mass will occur wherever the electron flow is in the direction of increasing temperature.³ Conversely, an accumulation

of mass occurs wherever the electron flow is in the direction of decreasing temperature. Metallized thin film stripes, however, usually are in such good thermal contact with their substrate that the resultant temperature gradients are not very severe, and their influence on failure rates appears to be small.^{4,6}

ii) Structural irregularities.

Considerable experimental evidence indicates that electromigration in metallized films is confined mainly to grain boundaries.^{3,6,7} For example, recent measurements^{3,7} of the activation energy, Q , for the electromigration process in Al polycrystalline thin films show that the value is about 0.5 eV-0.7 eV, which is of the magnitude expected for grain boundary diffusion.* This structural sensitivity has been confirmed by electron microscope studies^{3,9} on Al films, which revealed hillock and void formation associated with the grain boundary structure. The voids, which form as a consequence of flux divergences at appropriately oriented non-symmetrical nodes, grow with time and eventually coalesce to form an open gap across the conductor. The effect is particularly severe in films that exhibit a relatively small grain size, because large numbers of nodes are then available to serve as nuclei for the formation of voids.^{4,10} If the grain size is too large, however, the probability increases that a single grain will cover the entire stripe width. Under these circumstances, a new source of flux divergence is introduced; the single grain acts as an effective barrier to atoms migrating from the negative side, preventing replacement of atoms that are transported away by connecting boundaries on the other side of the grain.^{4,10}

* Activation energies for bulk diffusion in aluminum are approximately 1.4 eV.⁸

In the following section, a model will be developed for the electro-migration-induced failure of conductive stripes containing many grains across each transverse section. The model is based upon the void formation mechanism, which is relevant to Al, the material most widely used in thin film conductors. It should be noted however that films made from certain other materials, e.g., silver, appear to fail by a grain boundary grooving mechanism, in which the entire boundary becomes depleted in thickness.¹¹ The reasons for this difference are only partially understood, but it is expected that the approach followed here could be modified to include this related mechanism.

III. Development of the Model.

The observations described in Section II suggest that the electro-migration-induced failure of conductive stripes may be represented in a simple mathematical formulation. The model employed here is based explicitly on the following assumptions:

- i) The flow of current through the metal stripe creates voids at grain boundary nodes that are oriented suitably relative to the current flow and the longitudinal temperature gradient. The resulting porosity, p , increases at a rate proportional to the density of grain boundary nodes, n , the current density, j , the resistivity, ρ , and the mobility of the metal atoms along the grain boundaries, μ .

$$\frac{dp}{dt} = Cnj\rho\mu, \quad (2)$$

where C is an unspecified constant of proportionality.

- ii) Pore formation reduces the cross-section of the metal stripe available for carrying the current, thereby increasing the local current density within the remaining section,

$$j = j_0 / (1-p), \quad (3)$$

where j_0 is the initial current density in the pore-free stripe.

iii) The increased current density causes an increase in the current-enhanced motion of the metal atoms comprising the stripe, but it also increases the local Joule heating within the remaining conducting portions of the stripe.

iv) The local temperature, T , within the stripe increases above the ambient temperature, T_0 , by an amount that is proportional to the local Joule heating,

$$\Delta T = T - T_0 = j^2 \rho / h. \quad (4)$$

v) This increase in temperature leads to a corresponding increase in the mobility, μ , of the metal atoms along the grain boundaries,

$$\mu = D / kT = (D_0 / kT) e^{-Q/kT} \quad (5)$$

where D is the diffusion coefficient for motion along the grain boundaries, and Q is the activation energy for this process.

vi) The increase in temperature leads also to a change in the resistivity, ρ , of the metal,

$$\rho = \rho_0 (1 + \alpha(T - T_0)), \quad (6)$$

where α is the temperature coefficient of resistance. If the total current passing through the stripe remains constant, this increased resistivity causes an additional increase in the local rate of Joule heating, and in the effective electric field ($j\rho$), experienced by the atoms in the saddle point position.

vii) At a position along the length of the stripe where the grain boundary configuration and the temperature gradient combine to create suitable conditions, porosity will begin to develop, slowly at first, and then progressively more rapidly until it exceeds a critical value, at which time the stripe will fail catastrophically. This critical

value of the porosity may depend somewhat on the nature of the metal used for the stripe and the environment to which it is exposed. For the present purposes, it will be assumed that failure occurs when the local temperature within the stripe exceeds the melting point of the metal, but under other circumstances it may be more appropriate to select that temperature at which the metal begins to react vigorously with the substrate or the external environment.

Under these circumstances, the time to failure, T_F , is given by the expression:

$$T_F = \frac{1}{2Cn} \left[\frac{\tau_o k T_o}{j_o \rho_o D_o \exp(-Q/kT_o)} \right] f(x_o, x_1, Q, T_o) \quad (7)$$

$$\text{where } \tau_o = \Delta T_o / T_o = j_o^2 \rho_o / h T_o, \quad (7a)$$

$$f(x_o, x_1, Q, T_o) = \int_{x_o}^{x_1} \frac{\exp(-Qx/kT_o) dx}{x^2 (1-x + \alpha T_o)} \quad (7b)$$

$$x_o = \tau_o / [1 - \tau_o (\alpha T_o - 1)], \quad (7c)$$

$$x_1 = 1 - T_o / T_m, \quad (7d)$$

and T_m = melting temperature of the metal (or the critical temperature at which catastrophic failure occurs).

The function $f(x_o, x_1, Q, T_o)$ has been evaluated numerically to determine the variation of T_F under several possible experimental conditions, with the results shown in the next section.

IV. Application of the Model.

A. Relationship between T_F and j_o .

The relationship between the velocity of atomic migration and current density derived by Huntington and Grone¹ suggests that the mean time-to-failure, $\langle T_F \rangle$, should be inversely proportional to j_o , i.e.,

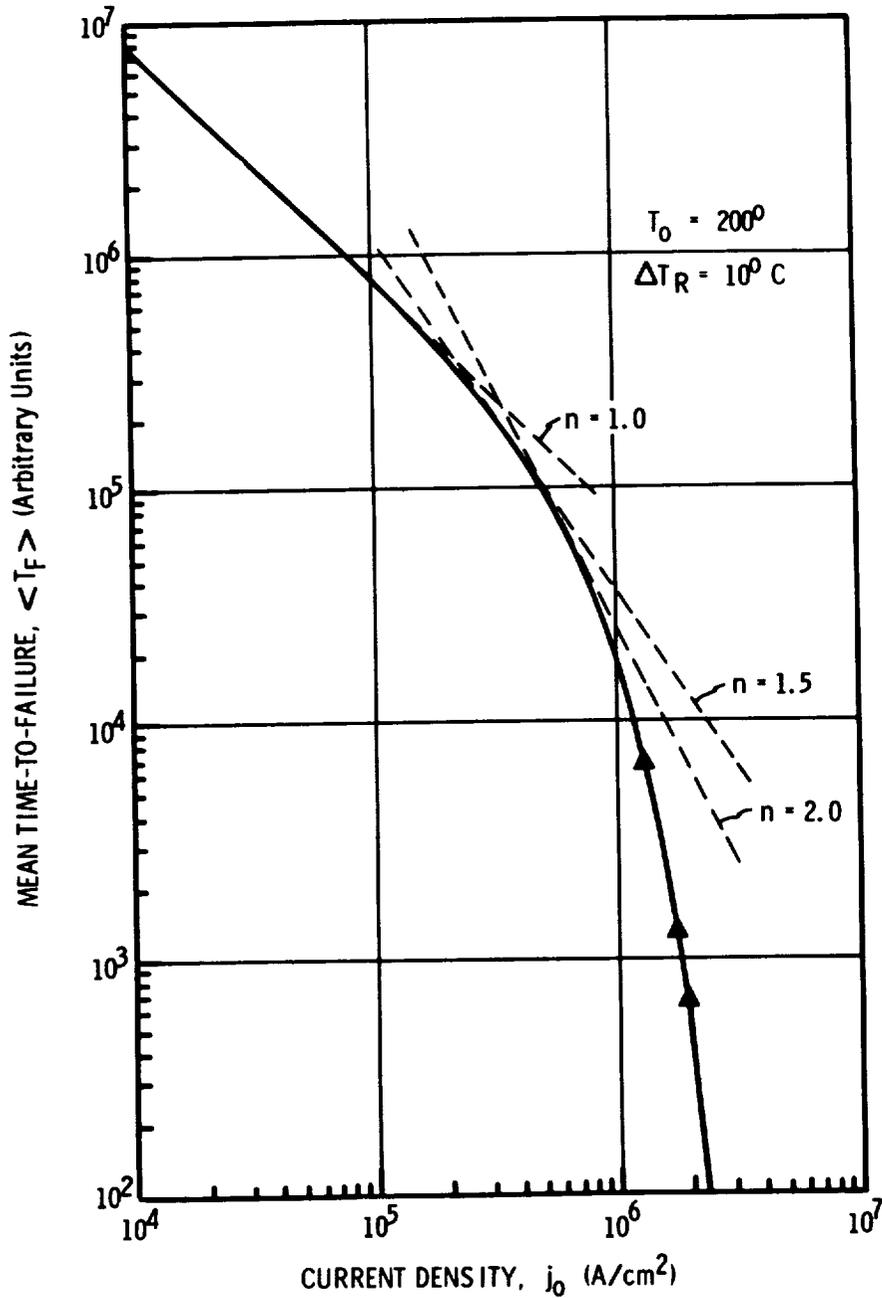


Fig. 1. Comparison of calculated dependence of $\langle T_F \rangle$ on j_0 (solid line) with slopes corresponding to Black's¹² data ($n=2$), Attardo's¹³ data ($n=1.5$), and the Huntington, Grone¹ theory of electromigration ($n=1$). Triangles are data points of Blair et al.¹⁰ normalized to the time-to-failure scale chosen here. The parameter ΔT_R characterizes the thermal contact of the stripe to its heat sink as described in the text.

$$\langle T_F \rangle \propto j_o^{-n}, \quad (8)$$

where $n=1$, but this relationship is not obeyed for current densities greater than approximately 10^5 A/cm². For example, Black¹² has reported that an exponent, $n=2$, characterizes his data in the range $0.5 \times 10^6 < j_o < 2.8 \times 10^6$ A/cm², whereas Attardo¹³ reports $n=1.5$ in the range $10^5 \lesssim j \lesssim 10^6$ A/cm². Moreover, the results of Blair et al¹⁰ are consistent with a value $n=4-5$ in the range $1 \times 10^6 < j_o < 2 \times 10^6$ A/cm². The mathematical formulation of the present model, equation (7), indicates that the time-to-failure varies with current density in a complex manner, and that a simple power law dependence is inadequate to describe the experimental observations over more than a small range of current densities.

The behavior of T_F as a function of j_o predicted by the model is illustrated graphically in Figs. 1 and 2. The theoretical curves were computed by numerically integrating equation (7), using the following parameters characteristic of Al and of the conditions under which experimental data normally are obtained:

$$\alpha = 0.004/^\circ\text{C}$$

$$Q = 0.7 \text{ eV (for grain boundary diffusion)}$$

$$T_m = 659.7^\circ\text{C (melting point of Al)}$$

$$T_o = 200^\circ\text{C}$$

In addition, the value of τ_o was computed from (7a) using the result of Rosenberg and Barenbaum¹¹ that a current density $j=1 \times 10^6$ A/cm² produces a temperature increase $\Delta T_R < 20^\circ\text{C}$ in a typical Al stripe initially at room temperature. Thus, from (7a)

$$\tau_o \approx \Delta T_R (1 + \alpha(T_o - 300)) (1/T_o) (j/1 \times 10^6)^2. \quad (9)$$

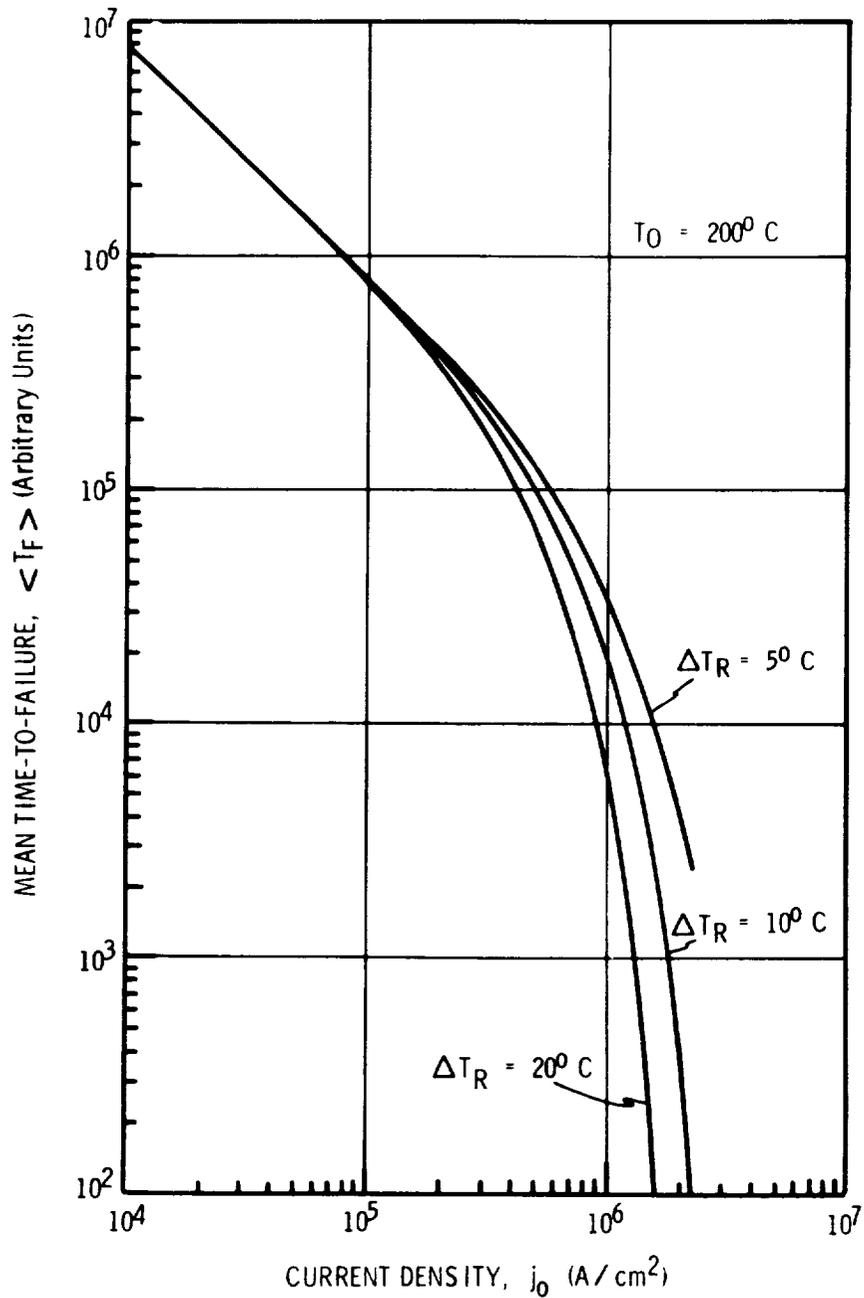


Fig. 2. Time-to-failure curves computed for different values of the parameter ΔT_R . The wide divergence of the curves at high current densities suggests that accelerated tests will be meaningful only when the precise nature of the thermal contact between stripe and environment has been established.

For the curve shown in Fig. 1 a value of $\Delta T_R = 10^\circ\text{C}$ was chosen arbitrarily. This curve is compared in Fig. 2 with the behavior expected on the basis of equation (7) for either a poorer thermal contact with the environment ($\Delta T_R = 20^\circ\text{C}$), or a better thermal contact ($\Delta T_R = 5^\circ\text{C}$).

It is apparent from an inspection of the two figures that the present model is capable of resolving the seemingly inconsistent results discussed above. The slopes determined by Black¹² ($n=2$) and by Attardo¹³ ($n=1.5$) are tangent to the curve predicted by the model, Fig. 1, within the range of current densities employed in their respective experiments. The data of Blair et al.¹⁰ also fit the theoretical curve quite accurately when normalized to the time-to-failure scale chosen in the figure.* In addition, the curve becomes asymptotic to a straight line with $n=1$, at low current densities consistent with the Huntington and Grone¹ model for atomic migration.

The three curves shown in Fig. 2 are a subset of the family of curves characterized by the parameter ΔT_R , all of which have asymptotic slopes corresponding to $n=1$ at low current densities. They illustrate the important role that thermal contact to the substrate plays in determining times-to-failure, especially in the range of current densities where most accelerated life data are obtained. Thus, at $2 \times 10^6 \text{ A/cm}^2$ the model predicts that a stripe-substrate combination characterized by relatively good thermal contact, $\Delta T_R = 5^\circ\text{C}$, should exhibit a mean lifetime approximately one hundred times longer than one in which the thermal contact is only four times poorer, $\Delta T_R = 20^\circ\text{C}$.

This result appears to have important implications for the proper analysis of accelerated life test data. Although it has been realized that interconnects used in integrated circuits can tolerate the passage of high

*The time-to-failure scale is presented in arbitrary units since the constant of proportionality, C , in equation (7) has not as yet been evaluated.

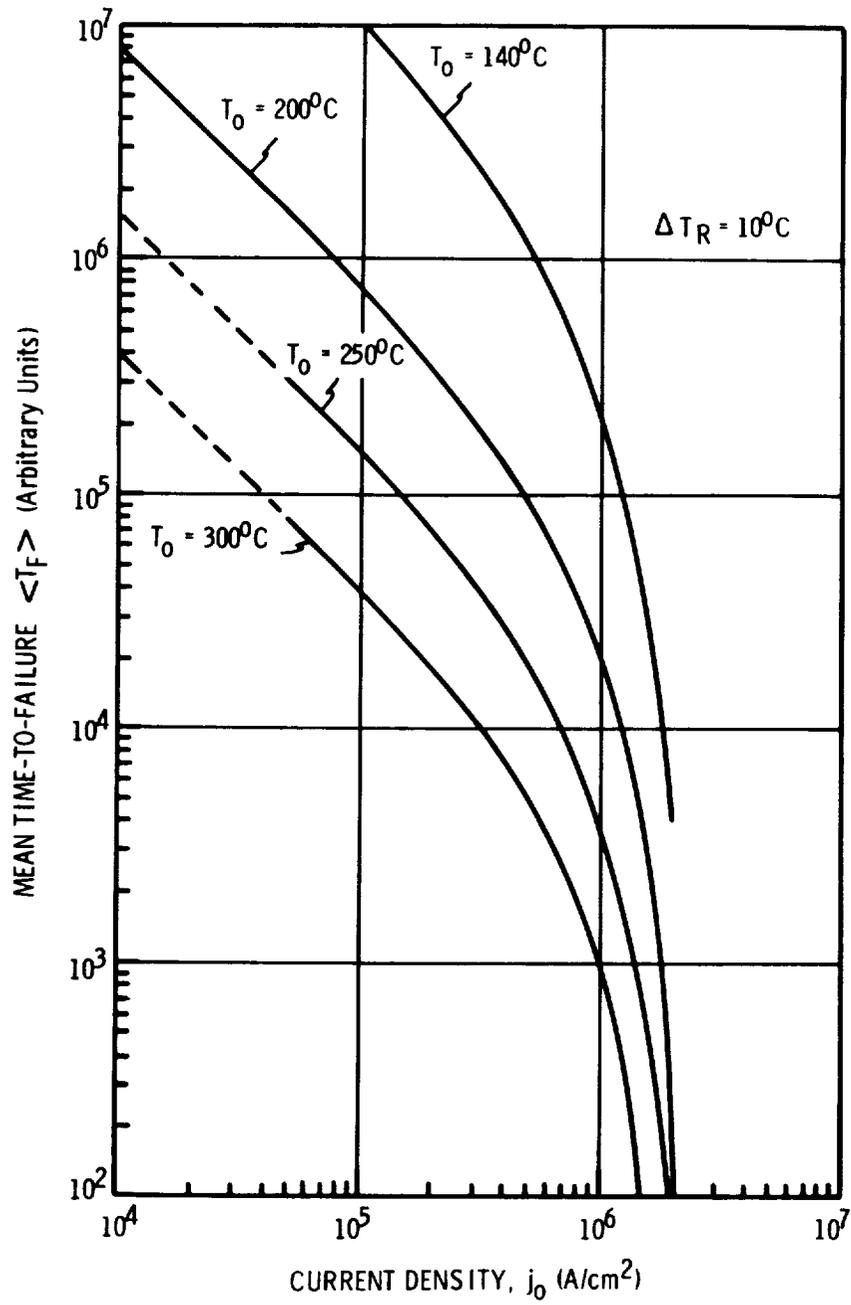


Fig. 3. Influence of the baseline temperature, T_0 , on times-to-failure as predicted by the model for a thermal contact equal to that used for Fig. 1.

current densities ($>10^5$ A/cm²) only because they are bonded to a massive heat sink, little attention has been given to the precise quality of the thermal contact. According to the present model, this factor cannot be ignored except at the risk of generating questionable or perhaps misleading information. Moreover, the results suggest further that tests done in an oil bath, for example, in which ΔT_R is reduced artificially, may have no real relevance to the expected behavior of failure rates under conventional conditions, unless appropriate corrections are applied.

B. Temperature dependence and activation energies.

The predicted influence of the baseline temperature, T_0 , on the T_F vs j_0 dependence is illustrated in Fig. 3. In Fig. 4, these computed data are replotted employing the conventional approach used to estimate activation energies. Despite the complexity of the original function, equation (7), from which these curves were computed, it is observed that the behavior is represented accurately as a straight line within the indicated ranges of current density and baseline temperature. Interestingly, however, the result indicates that the apparent activation energies determined in this manner can deviate from the value associated with the migrating atoms (assumed here to be 0.7 eV) by an amount that depends on parameters related to the testing conditions. Thus, the calculated curves indicate that the apparent activation energy, Q^+ , decreases from approximately 0.7 eV at low current densities to 0.65 eV when $j_0 = 2 \times 10^6$ A/cm². For larger values of ΔT_R (poorer thermal contact), this deviation is expected to be even more pronounced. Even at low current densities, however, Q^+ is expected to differ slightly from Q , by amounts that depend on the temperature coefficient of resistance, α , in the material comprising the stripe.

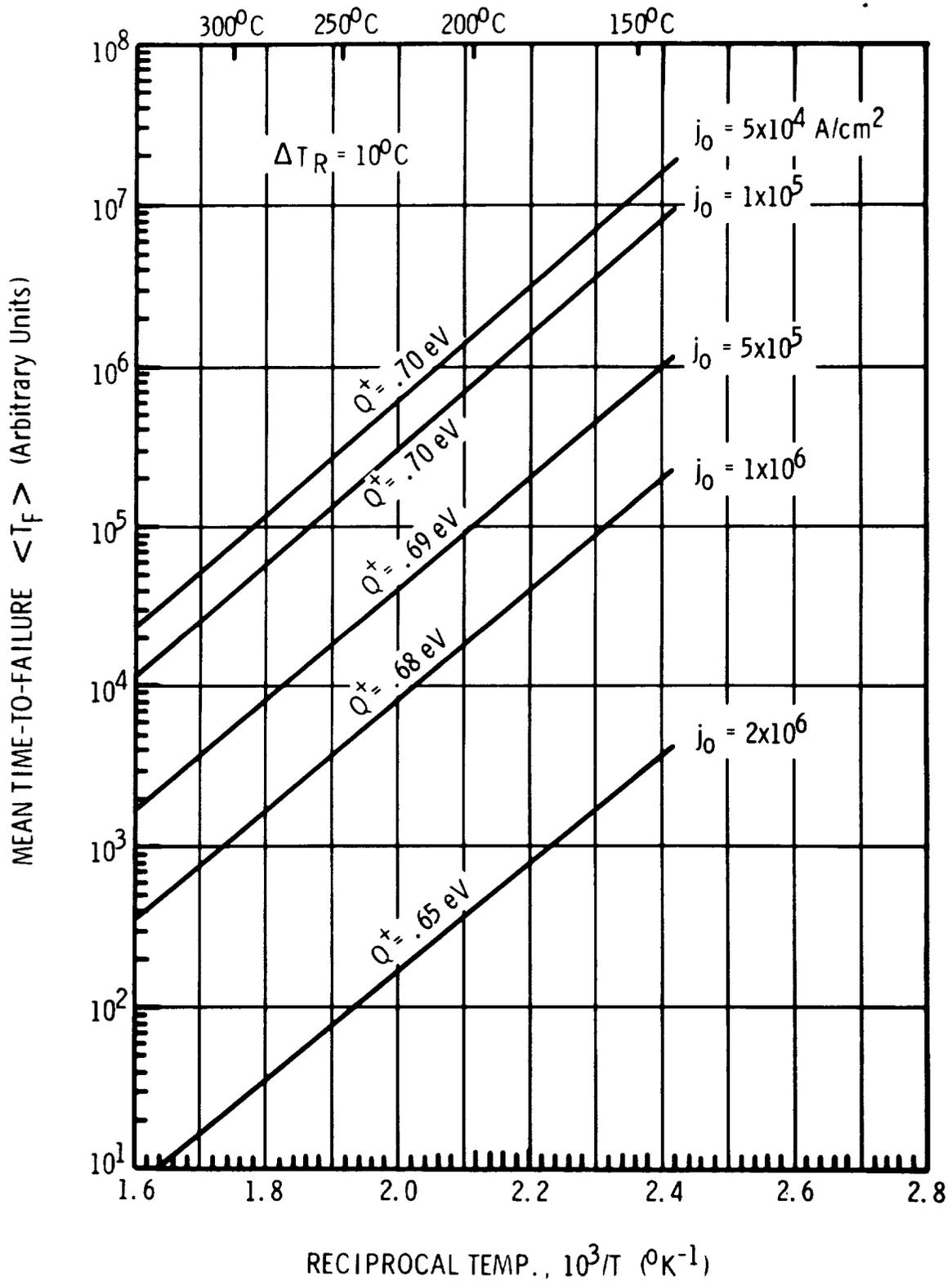


Fig. 4. The computed temperature dependence of times-to-failure represented in an Arrhenius plot. Although the curves appear to be accurate straight lines, the slopes yield only apparent activation energies, Q^+ , which vary with the testing conditions.

In addition, the value of Q^+ obtained by this procedure may exceed Q significantly in appropriate circumstances (j_0 or T_0 very large).

These results indicate that the time to failure is a complex function of the baseline temperature, and cannot be represented in a simple manner by an Arrhenius plot to give directly an activation energy for the processes involved. The heretofore unexplained variation in activation energies observed by some investigators^{4,12} may perhaps be understood on this basis.

C. The statistics of electromigration induced failures.

Statistical distributions of electromigration failure times for Al stripes under accelerated test conditions have been reported by Attardo and Rosenberg.⁴ In their work, it was assumed that T_F obeys a lognormal statistical distribution, and indeed their experimental data appear to be represented rather well on this basis. No physical justification was provided for this assumption, however, and consequently some doubt remains that lognormal statistics can be used reliably for extrapolation purposes.

An alternative, and potentially more accurate method of analyzing the statistics is suggested by the analytical formulation of the present model, equation (7), which establishes a relationship between the time-to-failure and the node density across the width of the stripe,

$$T_F \propto \frac{1}{n} .$$

Because n is a random variable, it would be expected that the statistical parameters of T_F could be derived from a mathematical transform of the distribution function associated with n .

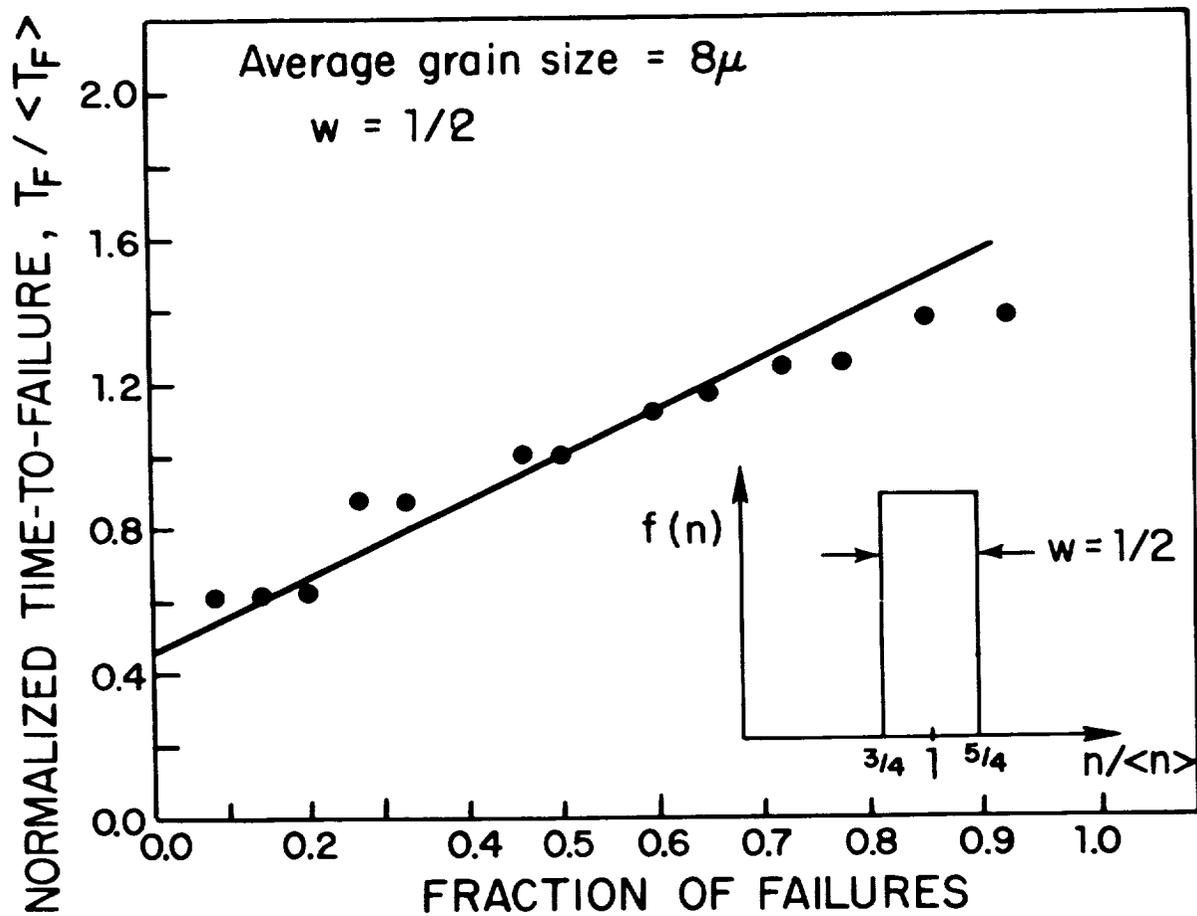


Fig. 5. The statistical data reported by Attardo and Rosenberg⁴ for an Al stripe with an 8μ mean grain size replotted according to the present analysis. Inset shows the node density function, $f(n)$, used to approximate characteristics of the grain structure shown in Fig. 3 of their article.

To test this hypothesis a frequency function for n was determined from the micrograph, published by Attardo and Rosenberg,⁴ for an Al stripe with a mean grain size of $8 \mu\text{m}$. The function was then approximated by a rectangular curve, $f(n)$, where

$$\begin{aligned} f(n) &= 0; 0 < (n/\langle n \rangle) < (1-w/2), \\ &= 1/w; (1-w/2) < (n/\langle n \rangle) < (1+w/2), \\ &= 0; (n/\langle n \rangle) > (1+w/2), \end{aligned}$$

as shown in the inset of Fig. 5. A value of $w=1/2$ was found to represent rather well the distribution of nodes in this film. The ramp-like distribution function obtained from this frequency curve was then mathematically transformed using standard procedures¹⁴ and the result used to construct graph paper on which the data of Attardo and Rosenberg⁴ could be re-plotted.

The results, shown in Fig. 5 indicate that the present approach provides a fit to the data that is as good as or better than the lognormal distribution used previously without specific justification. Because the statistical model proposed here has been derived directly from a knowledge of the basic physical mechanism involved, it is expected to permit more accurate prediction of failure rates than the empirical approach used previously.

V. Conclusions.

The proposed model has been subjected to experimental verification thus far by demonstrating agreement with published data only. The broad scope of the agreement achieved and the apparent resolution of inconsistencies reported in the previous literature suggest that the model may be useful for subsequent studies of electromigration induced failures. For this purpose, however, it would be desirable to obtain more detailed

quantitative verification. Certain critical experiments are suggested by the analysis. Specifically, insufficient attention has been given in the past to the nature of the thermal contact between the stripe and its heat sink. This parameter is exposed by the model as an important factor in determining failure rates, particularly under accelerated test conditions. A quantitative examination of this aspect of the problem appears desirable, therefore, to test the validity of the simple linear heat exchange relation employed in this model, and to evaluate the effects of different degrees of thermal contact. Second, the simple rectangular frequency function, $f(n)$, employed here is only a first approximation to the true characteristics. Detailed studies using more accurate representations of $f(n)$ will be needed to verify the statistical analysis.

If such tests provide a satisfactory validation of the model, measurements of the node density function, $f(n)$, and the Joule heating parameter, τ_0 , would suffice to characterize the lifetimes of stripes under a wide variety of conditions. The results described here would be useful also for developing accelerated life tests with improved predictive capability.

Finally, the approach followed here suggests the possibility that statistical models for other intrinsic degradation processes may be developed from analyses of the basic physical mechanisms involved.

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IV. A STUDY OF ELECTRONIC PART SCREENING TECHNIQUES

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CONTENTS

	<u>Page</u>
IV. A STUDY OF ELECTRONIC PART SCREENING TECHNIQUES	IV-1
A. INTRODUCTION	IV-1
B. CONCLUSIONS	IV-2
C. ADEQUACY OF CONVENTIONAL SCREENS	IV-4
D. LINEAR DISCRIMINANT ANALYSIS SCREEING	IV-16
E. PARAMETER DRIFT SCREENING	IV-22
F. CURRENT-NOISE ANALYSIS SCREENING	IV-30
G. THIRD HARMONIC ANALYSIS SCREENING	IV-35
H. SHORT-TIME OVERLOAD TESTING	IV-37
I. OPTIMIZATION OF STRESS SCREENS	IV-42
J. UNCONVENTIONAL SCREENING TECHNIQUES	IV-52
1. Neutron Radiography	IV-52
2. Combined Shock and Vibration, Monitored	IV-53
3. Laser Screening	IV-54
4. Automatic Inspection	IV-54
K. BELL LABORATORIES CORRESPONDENSE	IV-56
L. REFERENCES	IV-63 thru IV-65

Figure

1 Z-Value Distributions	IV-17
2 Leakage Current during PDS	IV-25
3 Transistor Failures in PDS Test	IV-25
4 Degradation Paths	IV-28
5 Degradation Figure of Merit	IV-28
6 Diode Life Test Results	IV-34
7 Capacitor Life Test Results	IV-34
8 High and Low Grade Failure Distributions	IV-43
9 Strength Distributions	IV-43
10 Screen Stress Level Effect	IV-44
11 Stress Level Reject Curve	IV-47
12 Life Test Failure Distributions	IV-48
13 Effectiveness Indicators	IV-49

Table

1	Transistor Problems	IV-5
2	Diode Problems	IV-6
3	Fixed Resistor Problems	IV-7
4	Variable Resistor Problems	IV-8
5	Capacitor Problems	IV-9
6	Integrated Circuit Problems	IV-10
7	Relay Problems	IV-12
8	Switch Problems	IV-13
9	Circuit Breaker Problems	IV-14
10	Critical Parameters and Drift Limit	IV-23
11	Resistor Screen Test Effectiveness and Efficiency . .	IV-40

IV. A STUDY OF ELECTRONIC PART SCREENING TECHNIQUES

A. INTRODUCTION

The effectiveness of screening tests currently performed on electronic parts can be partially measured by the quantity of defectives which are passing these tests and which show up later during hardware fabrication, test, or usage. The usual screen tests such as parameter measurements, thermal and mechanical shock, vibration, radiography, hermiticity, constant acceleration, etc., have evolved, over the years as methods to detect basic defects caused by material or process anomalies during manufacture. When a defect is encountered, often the user will generate another screen by adding a test to the procurement specification to prevent future occurrences. The screens being utilized on the common electronic parts are fairly standardized for many of the tests both as to type and to levels or durations. The tendency is to add new tests while retaining existing ones.

In addition to eliminating the more obvious defectives (screening out unreliable devices), more subtle screens have been attempted to further identify (within the remaining "good" devices of a lot) those items which have the probability of longest life. The perfect set of screen tests would positively eliminate all defective parts and precisely predict the operating life of each acceptable part with minimum time and cost expenditures.

In this study, some fundamental questions regarding screen tests in general will be analyzed. Both conventional and unconventional screening techniques will be reviewed.

B. CONCLUSIONS

1. The most significant reliability problem common to most electronic part types is that of ionic and/or particulate contamination. This problem is significant for transistors, diodes, resistors, integrated circuits, relays, and switches.
2. Conventional screens are not adequate to detect and eliminate all contaminated parts. Further, some of the screens may degrade ionic contaminated parts to a condition where failure is potentially imminent in service life.
3. Other prevalent part defects inadequately detected by conventional screens are semiconductor bonds with heel cracks, integrated circuit microcracks at contact windows, and seal leaks of wet tantalum capacitors. These defects may also be advanced by conventional screens such that failure could be potentially imminent in early service life.
4. Conventional screens are oriented to elimination of parts with specific defects or weaknesses. In general, conventional screens are not designed either to screen out parts on the basis of life expectancy or to provide information regarding longevity of the parts being screened. It is strongly recommended that the high stress screen approach, such as that performed by BTL Laboratics be investigated as discussed in Section I.
5. The degradation analysis approach and step stress or constant stress testing to destruction are the most feasible techniques to obtain cost and time effective information on relative life expectancy of individual parts or longevity estimates of part lots.
6. The Linear Discriminant Analysis approach is not considered appropriate in real-time, real-cost programs. The method is too uncertain, purely statistical, and unrelated to physical kinetics. The one advantage it has is that there is no other linear combination of parameters which will provide a better "zero-time" screen.
7. Current-noise testing is not an efficient screen test if the noise index is used as a reject criteria. It is recommended that this approach be utilized only for detecting mavericks in a production lot, such that parts which have outlier noise levels are considered reliability risks.

8. Third harmonic analysis screening is unsuitable for semiconductors. Further study is needed to determine its efficiency on discrete linear devices. It may be more efficient than current-noise testing. At worst, it may also be useful to detect mavericks by means of outlier harmonic content.
9. Short-time overload tests in the order of 1 to 2 hours are potentially one of the most effective ways to screen resistors. It can probably replace burn-in and power conditioning tests. Elimination of burn-in should not be made without data establishing the maximum overload temperature required and the optimum duration. One approach is the optimization method of Section I, coupled with physics of failure verification of realistic failure mechanisms.
10. Of the unconventional screen tests, neutron radiography has potential in inspection for contamination, particularly for switches, relays and circuit breakers. It may be useful on capacitors but should not be used on semiconductors containing boron dopant. The newer particulate contaminate tests such as combined shock and vibration are promising but not 100% effective. Laser scanning is a promising and needed tool for probeless testing of integrated circuits, particularly bipolars. Other approaches such as electron beam probing is required for MOS circuits. The automatic visual inspection techniques, although highly desirable, need considerable development effort before being feasible.

C. ADEQUACY OF CONVENTIONAL SCREENS

A review of failure experience is useful in that a measure of screen test effectiveness is obtained and an analysis of screening methods to eliminate these failures can be made. A summary of ALERT reports and other current industry electronic part failure experiences through March 1971 was published (CR114391) in February 1972 by Lockheed Missiles and Space Co., Inc. for Ames Research Center under Contract NAS2-6060 (Ref 1). The predominant problems experienced with the electronic part types of interest are listed in Tables 1 through 9.

From these tabulations it is evident that contamination is the most significant problem common to most of the part types. Transistors contained loose solder, weld splatter, TCE, and moisture. Diodes contained weld splash, solder balls, moisture, and loose silicon chips. Fixed resistors were contaminated with aluminum and variable resistors contained metallic chips. Integrated circuits contained moisture, glass splatter, solder, eutectic residues, and carbonized material. Relays contained iron particle, weld splatter, header slivers, flux, human hair, teflon and other fibers, flaked plating, excessive moisture, and ammonium chloride. Switches contained epoxy, flux, solder, and sealing cement.

The conventional screens of temperature cycling, high temperature storage, mechanical shock, electrical testing, radiographic inspection, burn-in, visual inspection, and vibration will detect many contaminated parts; but cannot be relied upon to eliminate all contaminated parts. Radiographic inspection, for example, will not detect aluminum, teflon, or fiber particles. Radiographic inspection also has a resolution limitation of slightly less than one mil on materials opaque to X-ray. Also, the success of vibration tests, monitored or, not, depends on the particulate first being shaken loose as well as on the probability that the particle will cause malfunction at the time of measurement. In addition, tests such as burn-in or temperature storage may degrade parts having corrosion-causing contaminants without carrying the mechanism to a detectable failure. The danger is that the screened part may have degraded to a condition where failure is potentially imminent in service life.

Table 1 Transistor Problems

Problem	No. Of Alerts/ Items	Problem Causes	Conventional Screens	Remarks
Lifted Bonds	7	Poor bonding processes. Excessive bonding pressure causing bond distortion and cracking at the heel.	High temperature storage, thermal shock, acceleration, burn-in, electrical testing.	Power cycling will induce fatigue and accelerate cracked and necked wire failures. Marginal bonds could be degraded by conventional screens and still pass.
Metalization	3	Moisture contamination or residual TCE from cleaning process.	Thermal shock, acceleration, hermetic seal, burn-in, electrical testing.	Hermetic seal will prevent contamination from using environment. Process - induced contaminants may cause degradation of parts during conventional screens without precipitating failure.
Parameter Deviation	3	Moisture contamination in encapsulated gas ambient. Moisture in package due to defective hermetic seals.	Dew point test, hermetic seal.	Dew point test could be ineffective with well-passivated devices. Moisture contamination could cause corrosion.
Conductive Contamination	9	Loose solder, weld splatter, slack leads, or poor lead dress.	Acceleration, electrical testing, radiographic inspection.	Radiographic inspection limitations are generally particles of .001 in. size or larger. Acceleration may be ineffective for particulates.
Parameter Deviation	6	Channeling due to lack of channel stop protection.	High temperature reverse bias, burn-in, electrical testing.	Conventional screens are adequate.
Mechanical Anomalies	3	Corroded leads, notched leads, plating pin-holes, and bare spots on leads.	Visual inspection.	Conventional screen is adequate.

Table 2 Diode Problems

Problem	No. Of Alerts/ Items	Problem Causes	Conventional Screens	Remarks
Inadequate Bonds	4	Gold-germanium lead solder of plastic devices unable to withstand cordwood module temperature stress, defective stud gold plating caused poor die bond, poor "S" ribbon bond to metalization, excessively crimped aluminum gate lead in SCR.	High temperature storage, thermal shock, burn-in, electrical testing.	Conventional screens are adequate.
Conductive Contamination	2	Weld splash, solder balls, loose silicon chips.	Acceleration, electrical testing, x-ray, visual examination, high temperature storage, thermal shock	Acceleration is not always effective for particulates. X-ray limitations are generally particles of .001 in. size or larger.
Moisture Contamination	2	Seals defective at manufacture or due to installation allowed moisture to enter the device.	Hermetic seal, high, temp reverse bias, electrical testing, visual examination.	Conventional screens are adequate.
Mechanical Anomaly	3	Poor external lead welds, contamination of leads resulting in corrosion and breakage, or corrosion and solderability failure.	Visual examination.	Conventional screens are adequate. High quality standards and tight process controls would minimize the problem.

Table 3 Fixed Resistor Problems

Problem	No. Of Alerts/ Items	Problem Causes	Conventional Screens	Remarks
Open Resistor Element	1	Thin film element cut during trimming.	Burn-in, short time overload, D.C. resistance.	Conventional screens are adequate to detect resistance elements with inadvertent small thin film widths.
Fractured Cores & Substrates	2	Excessive stress on cores during capping. Glass substrates cracked after thermal cycling. Resistors failed open, intermittent open.	D.C. resistance, temperature cycling, overload, D.C. resistance, tap test (X-ray & visual inspection as applicable)	Conventional screens are adequate to detect devices with cracked cores or cracked or excessively stressed substrates.
Parameter Deviation	3	Reduction of fused palladium oxide-silver-glass in hydrogen atmospheres caused large decreases in resistance.	D.C. resistance, burn-in D.C. resistance, temperature cycling, D.C. resistance.	Conventional screens are adequate to detect incompatibility of encapsulants when palladium oxide resistors are used.
Parameter Deviation	1	Electrostatic charge developed by resistors in plastic bags caused resistance to decrease.	D.C. resistance after removal from package.	Mechanism causing resistance change is little understood. Prevention of charge build-up may be desirable.
Open Resistance Element Wire	5	Inadequate support of wires by potting, stress on lead wire connection to resistance wire by improperly centered bobbin, improper weld of wire to end cap.	D.C. resistance, short-time overload, temperature cycling, twist test.	Conventional screens are effective in detecting marginal wirewound resistors with these defects.
Galvanic Corrosion	1	Aluminum contamination of bobbin and inadequate cure of coating caused opens and resistance increase due to galvanic action.	D.C. resistance, burn-in, temperature cycling, D.C. resistance, visual inspection.	Conventional screens may degrade contaminated wirewound resistors without failing them. Process control and effective cleaning steps are important.
Parameter Deviation	1	Facuity insulation on Bifilar wound resistor caused short between turns and decrease in resistance.	D.C. resistance, burn-in short-time overload, thermal cycling, D.C. resistance.	Conventional screens are adequate to detect insulation defects when bifilar wound resistors are used.

Table 4 Variable Resistor Problems

Problem	No. Of Alerts/ Items	Problem Causes	Conventional Screens	Remarks
Parameter Deviation	3	Coil contamination caused intermittent opens to rotor, metallic chips caused internal shorts, potting compound outgas reaction caused increased resistance.	D.C. resistance, burn-in, temperature cycling, D.C. resistance, peak noise, continuity.	Conventional screens may not eliminate all contamination problems.
Loss of Wiper Adjustment	3	Eccentricity between drive gear and resistor, defective gear caused by defective gear casting mold.	D.C. resistance, peak noise, continuity.	Conventional screens are adequate except where wear-out modes exist.
Canted Shaft	1	Retainer ring improperly installed causing canted shaft and loss of wiping action.	D.C. resistance, temperature cycling, D.C. resistance, peak noise, continuity, visual examination.	Conventional screens are adequate.
Inadequate Connection	2	Weak solder bridge on butt joint between resistance element and terminal pin failed causing open. Intermittent caused by poor center to end shaft joint.	D.C. resistance, temperature cycling, D.C. resistance, peak noise, continuity.	Conventional screens are adequate.

Table 5 Capacitor Problems

Problem	No. Of Alerts/ Items	Problem Causes	Conventional Screens	Remarks
Solder Reflow	4	Application of heat required to connect ceramic capacitors into circuit caused the internal lead-attach solder to melt resulting in opens and shorts.	None. Conventional screen do not reach solder reflow temperature.	High temperature solder should be utilized in ceramic capacitors. Excessive soldering heat should be avoided during assembly in equipment and thermal shunting utilized.
Mechanical Anomaly	2	Ceramic capacitor leads cracked due to residual stresses retained after cold working. Thus causing cracked welds. Cracked cases caused by incorrect resin and epoxy mixture.	Visual examination.	Conventional screens are adequate.
Slug Separation	2	Poor solder bond between slug and base of solid tantalum capacitor.	Temperature cycling, burn-in, seal test, capacitance, dissipation factor, insulation resistance.	Conventional screens are adequate. Radiographic inspection is also important.
Parameter Deviation	2	Solid tantalum capacitor shorted due to dielectric breakdown. Poor solder bonds caused high dissipation factor.	Temperature cycling, burn-in, seal test, capacitance, dissipation factor, insulation resistance.	Conventional screens are adequate.
Electrolyte Leakage	5	Incompatible expansion coefficients, elastomer defects, degradation of elastomers by solvents, and improperly cured materials caused electrolyte leakage in wet slug, TA foil, and Al. Electrolytic capacitors.	Temperature cycling, burn-in, seal test, capacitance, dissipation factor, insulation resistance.	Seal leak problems may be time dependent and not immediately detectable by conventional screens.
Parameter Deviation	1	Voids between end cap and element caused high series resistances in glass capacitor.	Temperature cycling, insulation resistance, capacitance, and dissipation factor.	Conventional screens are adequate.
Intermittent Open	3	Inadequate bonds of lead to foil in mylar and paper capacitors caused intermittents. Poor resistance weld in polystyrene capacitor caused intermittents.	Temperature cycling, burn-in, seal test, capacitance, dissipation factor, insulation resistance.	Conventional screens are adequate.

Table 6 Integrated Circuit Problems

Problem	No. Of Alerts/ Items	Problem Causes	Conventional Screens	Remarks
Microcracks at Window Cutout	2	Steep oxide steps cause thin metalization at contact windows and metalization tends to separate.	Minimum of 30 cycles temperature cycling, 100% electrical tests. Scanning electron microscope scan on sample.	Marginal devices may not be screened.
Lifted Chips and Cracked Die	4	Pyroceram bonding of silicon chip to package provided poor adhesion. Proper pyroceram mix may not have been used. Cracked die resulted from temperature coefficient mismatch between silicon die and pyroceram.	100% precap visual, temperature cycling, variable frequency vibration, constant acceleration. 100% electrical testing, radiographic inspection.	Conventional screens are adequate.
Wire Corrosion	1	Glass splatter from sealing hardglass flatpack to kovar lid deposited on aluminum lead, possibly reacting with contaminants and moisture in the package and corroding the wire to an open condition.	100% recap visual, gross leak test.	Conventional screens are adequate.
Voids and Overetched Metalization	1	Holes in photoresist permitted etchant to penetrate masked area.	100% electrical tests	Conventional screens are adequate.
Open Bonds	5	Improper alloying schedule causing poor aluminum adhesion to silicon, formation of gold-aluminum intermetallic, overbonding with excessive temp/pressure, improperly placed bonds, rebonding after silicon is exposed.	100% precap visual, stabilization bake, mechanical shock, thermal shock, constant acceleration random vibration, sample bond pull tests.	Conventional screens are adequate, however tight process controls and high quality standards are important.
Open Metalization	5	Corrosion of aluminum in presence of moisture (Hydrated alumina), scratches during handling and assembly, thinning over oxide steps, aluminum pulling toward alloyed contact, faulty oxide removal.	Precap visual, stabilization bake prior to seal, hermetic seal tests, temperature cycling, power burn-in at elevated temperature. Sample scanning electron microscope scans.	Tight process controls and handling procedures required. Processes and designs should be reviewed for adequate metalization thickness and grain size. Devices prone to migration failure may not be screened.
Bulk Shorts	3	Dopant spikes during diffusion, dendritic growths caused by silicon crystal imperfections and pinholes, diffusion anomalies resulting in isolation junction breakdown.	Precap visual, thermal bakes, operating life tests.	Process controls required in addition to conventional screens.
Metalization Shorts	9	Unetched metalization and smears, extraneous conductive material from leads, bonds, eutectics, or solders from bonding die attach, or package sealing procedures, carbonized material on die surface.	Precap visual, radiographic, electrical tests.	Conventional screen may not detect all potential shorts. Improved process controls and cleaning procedures required. Die passivation should be required.

Table 6 (concl)

Problem	No. Of Alerts/ Items	Problem Causes	Conventional Screens	Remarks
Metalization or bond to Silicon Shorts	4	Oxide pinholes, metalization mask misalignment, lead bond at edge of die, bond made over oxide step, poor scribing and dicing, stress cracks in oxide.	Precap visual, temperature cycling, overvoltage test, electrical tests.	Conventional screens are adequate. Most problems of the type can be eliminated by better processing standards and controls.
Lead Shorts	7	Leads too long, improper chip orientation, sagging leads, leads touch edge of die, loops shorting to package. glass seal precipitating lead between leads.	Precap visual, vibration tests, shock tests, radiographic inspection, electrical tests.	Conventional screens are adequate.
Operational Degradation	9	Design deficiencies, inversions caused by phosphorous glass passivation, reaction of output transistor with plastic case material, missing diffusion.	Electrical tests at ambient and extreme temperatures.	Conventional screens are adequate. Avoid use of plastic devices.
Operational Degradation	2	Overfritting of glass during die bonding causing glass to extend up the side and onto chip surface, cracked die, photoresist residue, pyroceram voids.	Precap visual, radiographic electrical tests, environmental per MIL-STD-883-Method 5004.	Conventional screens are adequate. Avoid glass frit bonding approach.
External Anomaly	3	Package identification obliterated by solvents, chip bond eutectic overflowed to aluminum bond on substrate forming intermetallics.	Precap visual, radiographic, high temperature storage, thermal cycling, shock, acceleration, variable frequency vibration.	Conventional screens are adequate.

Table 7 Relay Problems

Problem	No. Of Alerts/ Items	Problem Causes	Conventional Screens	Remarks
Contacts Fail to Make	8	Contamination between contacts of iron particles, weld splatter, header silvers, cracked getters, solder flux, fibers, flaked plating, teflon and frozen moisture on contacts.	High and low temperature run-in, sinusoidal vibration, particle impact noise detection, contact resistance, pickup voltage, dropout voltage.	Conventional screens may not detect all potential failures.
Contacts Fail to Make	6	Improper heat treating resulted in deformation of contact blades, teflon spacer cold flowed, and a bent torsion spring held up an armature due to omitted shim, fractured armature arm, improper armature/pole alignment, oversize/undersize parts.	High and low temperature run-in, sinusoidal vibration, particle impact noise detection, contact resistance, pickup voltage, dropout voltage.	Conventional screens are adequate. Good process control is important.
Contacts Fail to Make	2	Open coil caused by poor pigtail-to-coil solder connection, shorted coil due to insulation breakdown.	High and low temperature run-in.	Conventional screens are adequate. Good process control is important.
Contacts Fail to Break	2	Solder flux contaminant in relay eventually caused sticking and high resistance contacts.	High and low temperature run-in, contact resistance, pickup voltage, dropout voltage.	Conventional screens may not detect all potential failures.
Contacts Fail to Break	7	Misdrilled bearing hole, galling between armature and spring, actuator touching relay case when slight pressure is applied, fractured actuator arm, oversize/undersize parts.	High and low temperature run-in, contact resistance, pickup voltage, dropout voltage.	Conventional screens are adequate. Good process control is important.
Contact Shorts	5	Conductive contamination including metallic particles, slivers, solder, splash, weld splash, and solder plugs.	High and low temperature run-in, sinusoidal vibration, particle impact noise detection, contact resistance, coil resistance, pickup voltage dropout voltage.	Conventional screens may not detect all potential failures.
Shorts to Case	2	Armature retainer came off shaft and welded between the 28V terminal and case, retaining nut backed off armature shaft and shorted terminal to case.	High and low temperature run-in, sinusoidal vibration, particle impact noise detection, contact resistance, pickup voltage, dropout voltage.	Conventional screens are adequate. Good process control is important.
Decreased Insulation Resistance	4	Ammonium chloride contamination and electrolytic corrosion causing short to case, defective insulation, inadequate contact gap, improper lead positioning.	High and low temperature run-in, dielectric withstand voltage, insulation resistance.	Conventional screens are adequate. Good process control is important.
Mechanical Anomaly	4	Cracks in terminal leads due to hydrogen embrittlement, cracks in header glass, dents in case, poor terminal plating.	Visual examination.	Conventional screens are adequate. Good process control is important.

Table 8 Switch Problems

Problem	No. Of Alerts/ Items	Problem Causes	Conventional Screens	Remarks
Open	3	Contaminants of epoxy, sealing cement, oxide and sulfide films, and solder flux caused open and high resistance contacts.	Electrical and mechanical characteristics.	Conventional screens may not detect all potential failures. Tight cleaning and process controls are important.
Short	1	Conductive contamination including solder balls and other debris caused shorts and intermittents.	Temperature cycling, run-in test, sinusoidal vibration, visual examination, radiographic inspection, electrical and mechanical characteristics.	Conventional screens may not detect all potential failures. Tight cleaning and process controls are important.
Short	3	Switch contact improperly swaged at mounting point came loose, a switch activating pin weld failed and loose conductive parts caused shorts and intermittent operation.	Sinusoidal vibration, temperature cycling, run-in test, electrical and mechanical characteristics.	Conventional screens are adequate.
Mechanical Anomaly	1	Cracked cases and corrosion of cadmium plated switches.	Visual examination.	Conventional screens are adequate.

Table 9 Circuit Breaker Problems

Problem	No. Of Alerts/ Items	Problem Causes	Conventional Screens	Remarks
Open	1	Defective plunger assembly chipped because of interference and plastic chip between contacts caused bending and permanent open condition on attempt to close breaker.	Mechanical and electrical characteristics.	Conventional screens are adequate.
Latching Difficulty	1	Chips from defective plunger assembly and/or a loose plunger guide caused difficulty to latch and inability to latch.	Mechanical and electrical characteristics.	Conventional screens are adequate.
Undesirable Tripping	2	Launch environment shock and vibration.	Mechanical and electrical characteristics.	Conventional screens are adequate. Circuit breakers in shock and vibration environment should be rigidly mounted, pinned, and exercised prior to vibration periods to guarantee mechanical trigger is in full-on position.

The other failure mechanisms which are not adequately detected by conventional screen tests are semiconductor bond heel cracks, integrated circuit microcracks at contact windows, and seal leaks of wet tantalum capacitors. (See Tables 5 and 6.) These mechanisms may also be advanced by conventional screens such that failure could be potentially imminent in service life. Reference 2 discusses integrated circuit contamination and microcrack problems experienced in 1971 at MSFC. It also discusses difficulty in screening and preventing these mechanisms.

Process controls and proper designs must be relied upon to minimize these problems. Cleanliness and inspections during carefully performed assembly and a final inspection just prior to sealing could minimize most contaminants except those derived from the sealing operation itself. Neutron radiography may be a useful supplement to X-ray inspection of relays and capacitors. Design utilizing splash shields and passivation of chips make semiconductors less susceptible to contamination. Metalization and wire systems other than aluminum could eliminate microcracks in windows and at bond heels. Control of oxide step steepness is also helpful.

In-depth discussions of screening, process control requirements, and design approaches for each part type including recommendations are included in the individual electronic part studies in Volume II.

D. LINEAR DISCRIMINANT ANALYSIS SCREENING

In the conventional screen test approach, all parts meeting the requirements of parameter measurements, environmental tests, and burn-in are defined acceptable by means of the criteria to which they are tested. However, within any group of acceptable parts, variations in quality will always exist regardless of stringencies imposed in process controls, inspections, and screening tests. It is not expected that all acceptable parts, even of the highest quality, will fail or wear out simultaneously. The acceptable group will always contain certain parts which are superior to the others in life capability. Superiority in life capability can also be viewed as stability. The desired life or stability characteristics required of a part are often application dependent. For examples, stability of resistor temperature coefficient over a long period of time may be important in one application, while stability of resistance value at given temperature important in another. The Linear Discriminant Analysis approach is an attempt to select, from a group of conventionally screened high quality parts, those parts which are superior in regards to stability of the desired characteristic.

The parameters and limits used for parts acceptability during the usual screen tests are those which by experience or judgment are known to provide the required quality. The data obtained in these tests, such as parameter measurements and delta shifts during burn-in, are also utilized in the Linear Discriminant Analysis. However, the measurement values are inserted in a mathematical function of the parameters called the linear discriminant function. The linear discriminant function has the general form:

$$Z = k_1X_1 + k_2X_2 + \dots + k_nX_n \quad [1]$$

where the k's are constants and the X's are values of the parameters. For example X_1 may be initial leakage current in microamps, X_2 percent change in gain during burn-in, etc. The numerical value Z of the discriminant function is known as the Z-value. Once the discriminant function has been established a Z-value can be computed for each part. The parameters X_n can be any measured or calculated parameter of the part. The approach assumes that an indication of future part performance can be had from a relationship between certain parameters measured initially. These parameters are known as indicator parameters. However, all parameters are not indicators of future performance or independent of one another. The quantity n in equation [1] is usually 2 or 3.

The application of this method is illustrated in Figure 1. Z-values are calculated for each acceptable part after burn-in data is accumulated. Parts which are not superior are indicated as inferior, although they are good parts, meeting the requirements of a conventional screen. It is assumed in Figure 1 that the discriminant function is designed so that the Z-values of the inferior and superior parts will form two distinct distributions. \bar{Z}_i is the mean Z-value of the inferior parts and \bar{Z}_s is the mean Z-value of the superior parts.

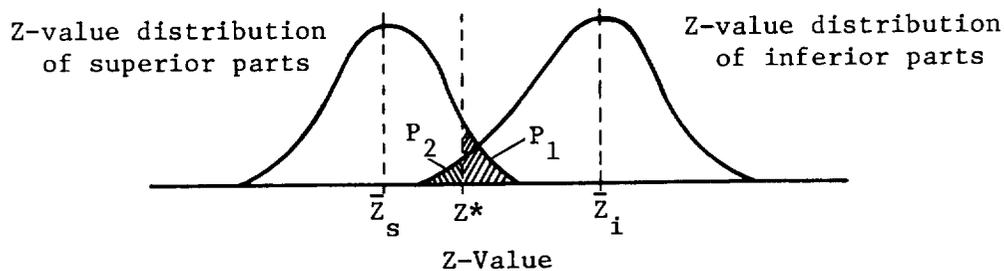


Figure 1 Z-Value Distributions

The value Z^* is called the critical value and is the criterion used for classification of parts into superior and inferior categories. In practice, the Z-value of each part is computed and all parts with Z-values greater than Z^* are classified inferior while those with Z-values less than Z^* are classified as superior. If the distributions of inferior and superior part Z-values are as shown in Figure 1, then the area P_1 represents the percentage of superior parts which will be misclassified as inferior, and the area P_2 represents the percentage of inferior parts which will be misclassified as superior. The critical value Z^* can be chosen to reduce one of the areas at the expense of the other.

Assuming that indicator parameters exist for the part under consideration, and that a linear function of these parameters as in equation [1] will form distributions as shown in Figure 1, the basic problem is to determine the value of k_n . From equation [1], the mean Z-value of the inferior parts is seen to be:

$$\bar{Z}_i = k_1 \bar{X}_{1i} + k_2 \bar{X}_{2i} + \dots + k_n \bar{X}_{ni} \quad [2]$$

and that of the superior parts is:

$$\bar{Z}_s = k_1 \bar{X}_{1s} + k_2 \bar{X}_{2s} + \dots + k_n \bar{X}_{ns} \quad [3]$$

where the subscripts i and s refer to data obtained from the inferior and superior parts respectively. The difference between these Z -value means is:

$$\bar{Z}_i - \bar{Z}_s = k_1 (\bar{X}_{1i} - \bar{X}_{1s}) + k_2 (\bar{X}_{2i} - \bar{X}_{2s}) + \dots + k_n (\bar{X}_{ni} - \bar{X}_{ns}) \quad [4]$$

From Figure 1 it may appear desirable to make this difference as large as possible to increase the ease and efficiency of discriminating between superior and inferior parts. This could be accomplished easily, as seen from equation [4], by merely increasing the values of k_n . However, increasing the k values will increase the dispersion of Z -values obtained from equation [1], and the resulting overlap shown in Figure 1 may give higher probabilities of misclassification. It is therefore required that values of k be determined which maximize equation [4] relative to its standard deviation, or to maximize the ratio:

$$t = \left(\bar{Z}_i - \bar{Z}_s \right) / S_{\bar{Z}_i - \bar{Z}_s} \quad [5]$$

which is equivalent to maximizing the ratio:

$$t_1 = \left(\bar{Z}_i - \bar{Z}_s \right) / \left[\sum (Z_i - \bar{Z}_i)^2 + \sum (Z_s - \bar{Z}_s)^2 \right]^{1/2} \quad [6]$$

By taking the partial derivatives of equation [6] with respect to each of the k 's and equating to zero, it can be shown that the values of k_n which maximize this ratio satisfy the following set of linear equations:

$$\begin{aligned} \bar{X}_{1i} - \bar{X}_{1s} &= k_1 S_{11} + k_2 S_{12} + \dots + k_n S_{1n} \\ \bar{X}_{2i} - \bar{X}_{2s} &= k_1 S_{12} + k_2 S_{22} + \dots + k_n S_{2n} \\ \bar{X}_{ni} - \bar{X}_{ns} &= k_1 S_{1n} + k_2 S_{2n} + \dots + k_n S_{nn} \end{aligned} \quad [7]$$

where the S 's are sums of products similar to those used in least squares analysis and are defined by:

$$S_{mn} = \sum (X_{mi} - \bar{X}_{mi}) (X_{ni} - \bar{X}_{ni}) + \sum (X_{ms} - \bar{X}_{ms}) (X_{ns} - \bar{X}_{ns}) \quad [8]$$

From the considerations associated with equation [4] through [8], the following procedure (Ref 3) is used to derive the linear discriminant function of equation [1]:

- 1) A set of parts is chosen for testing simulated use conditions. The test group is assumed to present the propulsion to be screened. The test generally consists of a load life test of a duration equal to the required life. (For example, the test to be performed on resistors may be operation for 2000 hours at rated power and at an ambient temperature of 125°C.)
- 2) Indicator parameters are selected which by experience of judgment are believed to be significant in indicating future performance of the part type to be analyzed. Measurements of selected parameters are taken initially and after burn-in as required. If doubt exists regarding the status of a parameter as an effective indicator, it should be included, as later analysis will reveal its significance. (For resistors, the initial measurement parameters which have been used are voltage coefficient of resistance, temperature coefficient of resistance, and current-noise voltage.) Initial resistance measurements are made for the purpose of determining delta shift during burn-in. The post-burn-in measurement is resistance only. This constitutes four candidate indicator parameters, or $n = 4$ in equation [1]. The indicator parameters, X_1 through X_4 , are values of a) voltage coefficient of resistance; b) temperature coefficient of resistance; c) current-noise voltage; d) percent change of resistance during burn-in.
- 3) The load life test is performed after the post-burn-in measurements of step 2) are taken. After performance of the load life test, measurements of the parameter which is required to be stable are taken. All test parts are classified as inferior or superior as a result of these measurements. (for resistors, the criterion may be a required minimum percent resistance change during the 2000-hour load life test. An alternate approach is to order the values of percent change and identify resistors with the largest delta values as inferior. For example, it may be desired to select 30% of the most stable resistors in a given lot for critical use. The top 70% of the ordered list would be classified inferior while the most stable 30% of the test group would be classified superior.)

- 4) The indicator parameter data obtained in step 2) are separated into two sets corresponding to the classifications made in step 3). One set is the data of parts classified inferior and the other set is the data of parts classified superior.
- 5) From the two data sets of step 4) the products of equation [8] are calculated. The set of linear equations [7] is then solved for the values of k which maximize equation [5]. The k values thus obtained provide optimum separation and minimum overlap between the Z -value distributions of inferior and superior parts shown in Figure 1.
- 6) The linear discriminant function is established by inserting the values of k , determined in step 5) into equation [1]. Z -values for each of the test parts are then calculated from the data obtained in step 2). The Z -values are ordered and a values of Z^* chosen, which provides the discrimination between superior and inferior classifications predetermined in step 3).

If proper discrimination of the test group is obtained by the above procedure, it is assumed that use of equation [1] with the values of k determined in step 5), and use of the value of Z^* determined in step 6), will discriminate between inferior and superior parts in the remainder of the lot and possibly in future lots. Many options are open to the investigator. For instance, the data obtained in step 2) may be analyzed in various combinations to determine the optimum 2-parameter, 3-parameter, etc, discriminant function. These analyses indicate the effectiveness of various parameters as indicators, and the optimum combination of indicators that may be used. Also, analysis of the Z -value distributions obtained may indicate that transformations of the data may be required to obtain normality. Analysis of the distributions can also be made to determine values of Z^* required to minimize costs resulting from misclassification (Ref 3), or to obtain a set of superior parts with a given probability of containing inferior parts.

An example of the linear discriminant analysis approach is given in Reference 4. A group of 501M Minutemant transistors were tested and a discriminant function developed to identify parts capable of meeting unusually tight limits and delta changes of leakage and gain parameters. Analysis of the Z -value distributions showed that a maximum of 2.84% inferior parts should be

misclassified as superior (95% confidence) when using the particular critical value of Z^* chosen. Of 3100 parts classified as reliable by the linear discriminant function and the chosen Z^* , 87 parts (2.8%) failed the tightened limits after 600 hours of test. It was concluded that a linear discriminant function can be used effectively to screen out inferior parts from a production lot.

The principal advantage of this approach is that the systematic method provides assurance that no other linear or transformed combination of parameter measurements will yield a criterion with smaller probabilities of misclassification.

The main disadvantage of this method is that a load life test duplicating the actual load conditions and life durations is required to establish the discriminant function. Extended tests duplicating long life mission times and stress profiles are obviously impractical. Also, it is expected that the discriminant function will vary with the particular part tested. The approach is purely statistical, and unless a physical explanation can be established relating the indicator parameters with superior part performance, no universality can be expected in the parameters of the discriminant function. The k values may indeed vary from type to part type within the same part class. Also, the discriminant function may vary with test conditions and criteria for superiority. Even successive lots of the same part from the same manufacturer could require different discriminant functions due to gradual unintentional process changes, as well as process and material variabilities.

Because of these uncertainties and difficulties, it is recommended that the Linear Discriminant Analysis method be considered inappropriate as a general approach to the long life electronic part problem. However, it is recommended that the method be held in reserve and tested for appropriateness when occasion demands selection of the more stable parts from the particular group. In this event, it is also recommended that short term accelerated tests be performed in lieu of the long term life tests normally prescribed for establishment of the discriminant function.

E. PARAMETER DRIFT SCREENING

The basic premises in the Parameter Drift Screen (PDS) approach are that all of the parts in a given lot of a specific part type are not identical, that the parts which will fail first are predetermined to a certain extent, and that, as in the Linear Discriminant Analysis approach, certain parameters exist which are "critical" in indicating which parts will fail first. In the PDS approach, however, each critical parameter is considered separately, whereas, in the Linear Discriminant Analysis approach they are considered in linear combinations. It is assumed that the mechanism which causes one part to fail first, rather than another, is taking place gradually, and is evidenced by the gradual change or "drift" of the critical parameters.

Parts subjected to burn-in often exhibit a normally expected parameter drift due to various stabilizing processes. Initially, these stabilization processes usually exhibit wide variations in drift of the critical parameters and mask the more subtle changes which may be occurring simultaneously due to material or material-processing defects. These more subtle changes are therefore generally undetectable during a short term burn-in, particularly when initial and final parameter measurements only are made. However, delta shift limits during burn-in are useful in eliminating parts with grosser defects.

The simplest PDS approach to detect the more subtle indicators of part failure is to perform a power aging test subsequent to the standard screen tests of temperature cycling, burn-in, high temperature bake, and constant acceleration. Tight drift limits of the critical parameters during the power aging test are used to assure that parts which continue to drift excessively subsequent to the initial burn-in are rejected. It is these parts (other than "random" failures) which are expected to fail first in a long-life application. It is assumed that drifts due to stabilization processes have been completed during the initial standard screening burn-in.

An example of this approach is given in Reference 5 where approximately 11,000 semiconductors were tested. Before starting the PDS power aging test, the parts were subjected to standard screening tests which included a 250-hour burn-in at rated junction temperature. The successfully screened parts were then placed into a 500-hour PDS power aging test and the critical parameters measured every 100 hours. The critical parameters and drift criteria for each part type were as shown in Table 10.

Table 10 Critical Parameters and Drift Limit

Type of Part	Critical Parameter	Drift Limits
Diodes and Rectifiers	1. Forward voltage drop 2. Reverse leakage current	± 0.05 Volt $\pm 20\%$
Varactor Diodes	1. Junction capacitance 2. Quality factor 3. Reverse leakage current	$\pm 10\%$ $\pm 10\%$ $\pm 10\%$
Silicon-Controlled Rectifiers	1. Forward leakage current 2. Reverse leakage current 3. Forward voltage drop	$\pm 20\%$ $\pm 20\%$ ± 0.1 Volt
Zener Diodes	1. Zener voltage 2. Reverse current 3. Zener impedance	$\pm 1\%$ $\pm 20\%$ $\pm 10\%$
Transistors	1. Collector-emitter saturation voltage 2. Collector-base leakage current 3. Collector-emitter leakage current 4. Emitter-base leakage current 5. Direct current gain	± 0.05 Volt $\pm 20\%$ $\pm 20\%$ $\pm 20\%$ $\pm 10\%$

The general drift criteria were adjusted for special cases to accommodate test equipment repeatability and accuracy limitations. For example, the drift limits for planar transistor leakage currents were the larger of $\pm 20\%$ or 2.0 nanoamperes. Of the parts which successfully passed initial screen tests, a further 12% were rejected by the PDS tests.

One of the interesting results of this test program was measure of effectiveness on the 2N2512 NPN epitaxial planar transistor. No rejects occurred in initial screening during burn-in, which did not include a delta limit criteria. However, of 1092 parts which were subjected to the subsequent PDS test, 97 were rejected. An extended life test was then performed on 94 of the PDS rejected parts and 100 of the PDS accepted parts. The extended life test consisted of 1500 additional hours of operation at maximum rated junction temperature. None of the PDS accepted parts exceeded specification parameter limits during this test. However, 15 of the PDs rejected parts exceeded rated leakage current limits during the extended life test.

An indication of the continuing gradual operation of the non-stabilizing degradation process was achieved on the 2N930 planar silicon transistor. One lot of these parts had a high percentage (20%) of PDS rejects due to surface inversion leakage. The leakage current continued to increase on the rejected parts throughout the PDS, while it stabilized on the accepted parts. Comparison of leakage current of the rejected and accepted parts is shown in Figure 2. It is significant to note that neither leakage current limits nor a one nanoampere leakage current delta shift criterion during the pre-PDS screen test is capable of detecting the rejects.

On some part types, the PDS rejects occurred during the first 100 hours of testing. On others, rejects occurred during later 100-hour intervals. The cumulative rejects for all transistors (nine types tested) is shown in Figure 3. This curve indicates that some transistors may require more than 500 hours of PDS power aging to detect all the rejects.

In Reference 6 it is reported that TRW utilized an 832-hour power conditioning test following a 168-hour burn-in on Intelsat III semiconductors. The power conditioning test was an extension of the burn-in test. Parameter measurements during the 1000-hour combined test were taken at 0, 168, 600, 750, and 1000 hours, providing five data points for parameter drift calculations. As this was a 100% test of the lot, no Group B 1000-hour lot sample life tests were performed. Identification of all data was maintained with the serialized part from which it was derived. In a refinement of the PDS approach the performance stability of *each* part was evaluated rather than merely rejecting all parts exceeding specified drift limits. Thus, in the group of parts which passed the PDS delta shift criteria, further rejection of specific parts with suspect drift patterns was made. On Intelsat III, part acceptability was based on review of the parameter data for each part. Parts whose parameter drift patterns were erratic, differed significantly from the norm of a lot, or exhibited a degradation toward failure, were rejected for flight use.

In reviewing results of the 27 semiconductor lots subjected to this program, the impact of the 832-hour power conditioning test was of primary interest. Two lots were totally rejected because of failures during this portion of the test. Only four lots were failure-free. It was concluded that:

1. The two lots which were rejected would probably have passed a Group B 1000-hour sample life test.
2. The 168-hour burn-in is not sufficient to eliminate every defective part. Extended power conditioning PDS tests are needed for this purpose.

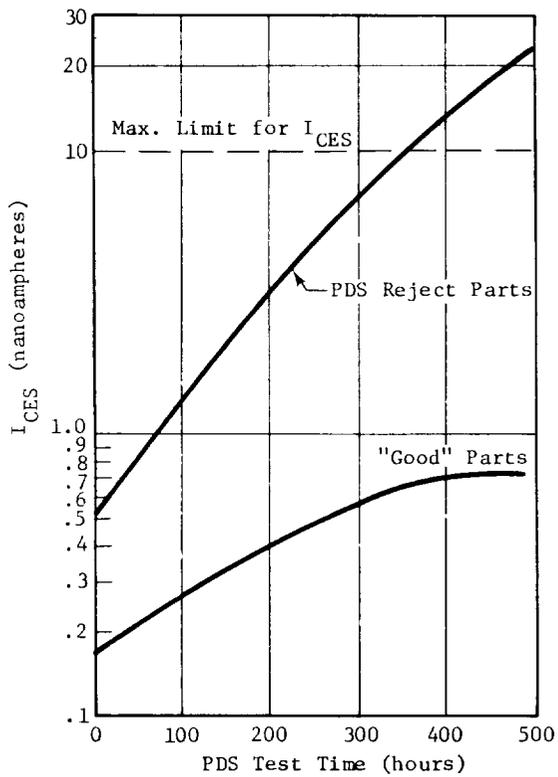


Figure 2 Leakage Current during PDS

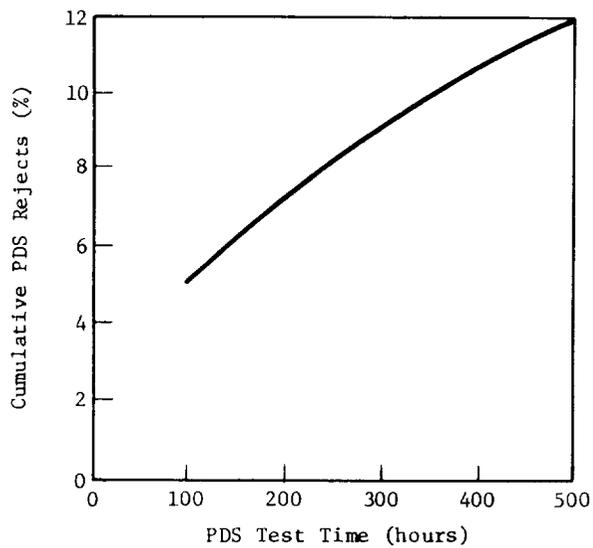


Figure 3 Transistor Failures in PDS Test

Another variation of the PDS approach, called Degradation Analysis by Hughes Aircraft Company, is described in Reference 7. The degradation analysis approach, similar to the others described above, requires a period of extended power aging on 100% of the parts. A mandatory prerequisite to the power aging test is an effective screen test to eliminate parts with assembly defects. The screen test includes a 168-hour burn-in at maximum rated conditions. The power aging test is usually a 504-hour extension of the burn-in test. However, other aging conditions have been used (Ref 8), such as power on-off cycling for periods of up to 1500 hours to simulate a normal use schedule.

Figure 4 shows typical degradation paths that may be followed by the critical parameters during burn-in and power aging. All the paths shown remain within specification limits throughout the test, but exhibit distinctly different kinds of drift and stabilization behavior. Path A shows the normal type of stabilization process that might be expected in semiconductors. It consists of a relatively large early drift and very little change after stabilization. Path B, however, is one which cannot be expected to stay within specification limits for an extended period of time. It may be indicative of a material or material-processes deficiency. A comparison between Paths A and B illustrates the importance of the path in revealing future behavior of the part as opposed to specification limits or delta shift limits. Both A and B have the same delta changes and are within limits, but parts following Path B would be considered unacceptable for long term missions. The erratic behavior of Path C may be the result of several weaknesses within a part. It cannot be depended upon for reliable performance even through measured values and delta shift may be within the acceptable limits for good parts. Path D shows very little drift with respect to the others. Although the final value is closest to the lower specification limit, it may represent the most reliable of all the parts. Another important consideration is the drift behavior of a part in comparison to others in the same group or population. If the behavior deviates appreciably, its reliability is open to suspicion.

The degradation analysis approach utilizes four sets of parameter measurements made during the burn-in and power aging tests. These are made initially, after 168 hours of burn-in, and after 168 and 504 hours of power aging. Data from these measurements are utilized in computer programs to assess the behavior of each individual part and to compute lot statistics. The stabilization path followed by each individual part during test is evaluated quantitatively by means of a number known as the degradation figure of merit (DM). Figure 5 illustrates the meaning of this figure of merit as it applies to a part parameter following path type B. The values of the indicator parameter at the four measurement times are shown connected by straight lines with slopes S_1 and S_2 during power aging. The drift limits shown are the parameter values which will not meet typical circuit requirements. Another straight line of slope S is a projection which continues the trend of change. The figure of merit DM is the time after power aging that the projected trend of slope S intercepts the drift limit. The model used for estimation of slope S is based on the ratio of S_2 to S_1 . It is computed algebraically as follows:

$$S = S_2 \cdot |S_2/S_1| \quad [9]$$

The time DM cannot be treated as an expected time to failure, but is a measure of the stability behavior of the part. It is weighted by the proximity of the final reading to ultimate failure. As a figure of merit it can be used to compare parts against each other or against the populations from which they come or against known good devices. A minimum figure of merit can be used as one of the criteria for selection of parts to be used in long-life missions. For a part parameter following degradation path A, the figure of merit DM is conservative with a constantly decreasing slope.

An application of this approach on the Early Bird satellite is reported in Reference 8. Over 19,000 parts were tested including transistors, diodes, resistors, and capacitors. Degradation analysis data was obtained during 1000-hour and 1500-hour on-off power aging tests. Parts were graded into three categories on review of the computer outputs which included figures of merit for each part. Potentially unreliable parts were graded as rejects. The best parts were graded flight quality. The rest were graded flight residual to be used for non-flight usage. Although the parts were the highest quality parts which could be obtained against special controlled specifications, 30% were screened out by this method as being unsuitable for flight use, even though the operational parameters were still within specification limits.

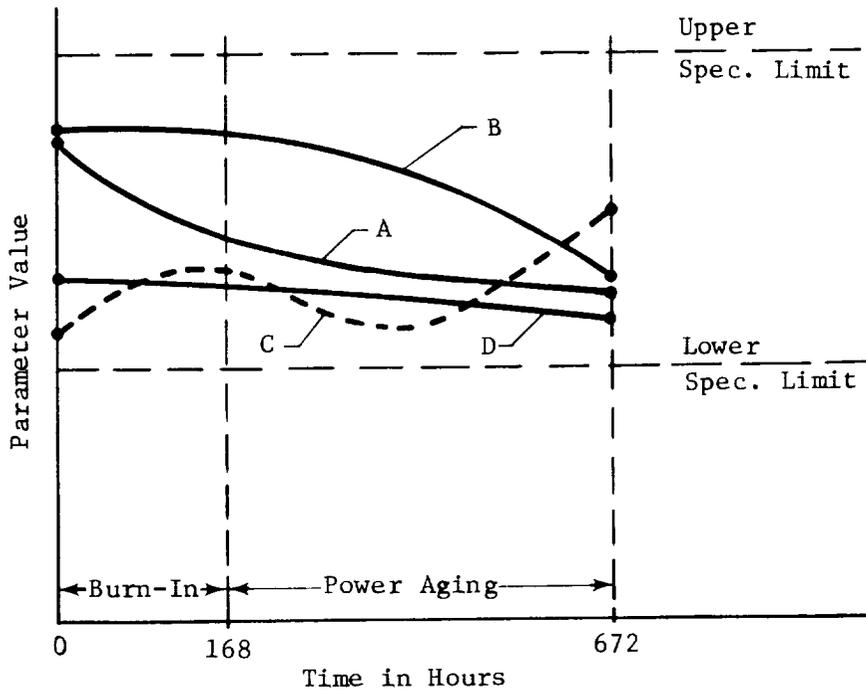


Figure 4 Degradation Paths

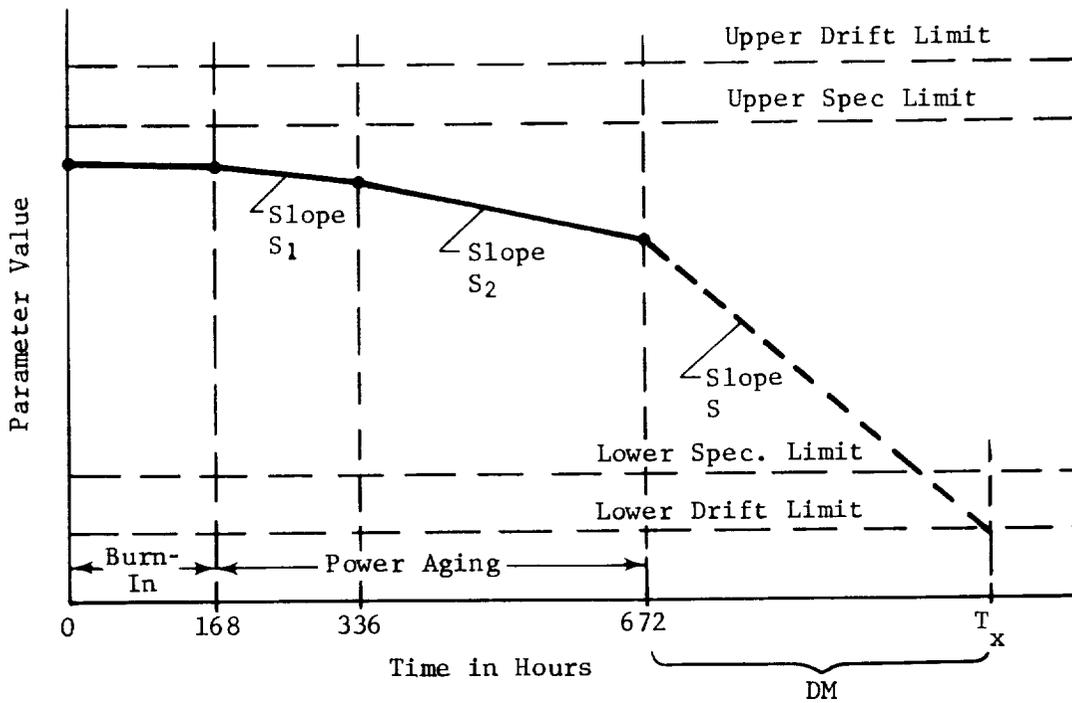


Figure 5 Degradation Figure of Merit (DM)

All of the PDS approaches have the advantage of assuring a degree of parameter stability in the parts screened. The more refined methods, such as Degradation Analysis, provide a further benefit of permitting selection for flight use of the specific parts indicating superior long-life stability characteristics.

Parts screened with PDS are more costly due to the extended power aging tests, the additional parameter measurements and the precision required, the data analysis effort, and the higher selectivity which results in a greater reject rate. For the OGO satellite containing approximately 80,000 parts, it was estimated that (Ref 6) a comprehensive PDS program for electronic parts would cost in excess of two million dollars. Reliability tradeoffs resulted in screening only diodes and transistors on a 100 percent basis at a cost of \$250,000.

It is recommended that the PDS approach be utilized in a parts screening program where long-life stability is a necessity. As opposed to imposition of this approach as a general requirement for all parts, it is recommended that the PDS method used, the degree of refinement implemented, and the parts which it is applied, be determined by means of program tradeoff studies.

F. CURRENT-NOISE ANALYSIS SCREENING

Current-noise analysis screening has received considerable attention as a technique to detect unreliable parts because it is relatively inexpensive and has little impact on schedule. This technique is one of the "zero-time" screening tests which attempts to forecast future part performance on the basis of noise characteristic measurements made in early life. Reference 9 states that some investigations have concluded that there is significant correlation between noise measurements and long term performance. However other investigations have concluded that the correlation is too weak for screening purposes.

All parts exhibit a "thermal" noise as a result of random electron movement within the conducting medium. The RMS value of the noise voltage is a function of temperature and resistance. Current noise is the increase in noise level, over thermal noise, which occurs when a current is passed through the conducting medium. For resistors (Ref 10) current noise is generally the greatest in carbon composition types, less in deposited carbon types, still less in metal film types, and unmeasurable in wire wound types. As in mechanical hardware, where excess audio noise may be an indication of impending malfunction, an abnormality in the current noise of apparently identical resistors may be an indication of defects. Although thermal noise has a flat distribution of power through the frequency spectrum, current noise exhibits an inverse power versus frequency characteristic. The effect is, therefore, more pronounced in the lower frequencies, largely below 100 kHz.

A correlation between noise and defects in tin-oxide film resistors is reported in Reference 10. The resistors tested utilized a transparent film of tin-oxide on a cylindrical glass substrate. They were adjusted to value by cutting a helix into the film. The resistors were uncoated to facilitate examination. On visually examining resistors exhibiting abnormally high noise levels, defects causing current constrictions were observed which could reasonably cause the noise due to higher than normal current densities. The resistors were then powered while under observation with a binocular microscope. A shorting probe was used to divert the resistor current from the defect. By probing the part in this manner, the source of noise production could be located with precision. On diverting the current from the defect, a distinct reduction in noise is reported. One group of defects, called series-type defects, consisted of film scratches, wide chips,

film porosity, cracks or checks in the substrates glass, and excessive cap to film contact resistance. These were called series-type defects because the entire resistor current passed through the region with abnormally high density. Shunting defects were also observed which consisted of foreign material bridging the spiral cut, and bridges of undisturbed film across the cut path.

A correlation between current noise level (using the system of measurement in Ref 11) and load life test results was then investigated. Standard tin-oxide resistors were selected for test wherein the possibility of defects was high. The general purpose resistors were 1/2 watt, 150,000 ohm constructed with high resistivity film, high turn-per-inch helixing, and small size. Noise measurements were made on 4000 units and results ranged from -35 dB to +25 dB. One hundred samples, with noise values evenly distributed throughout this range, were selected for 1000 hour-cycled-load-life-testing. It was determined from the load life test, by means of the drift and temperature coefficient data obtained, that a noise index of -21.3 dB would have eliminated all resistors with erratic or abnormal performance. Although all resistors exhibiting substandard performance were noisy, not all noisy resistors were substandard. If all 4000 resistors in the original group were screened to this noise index, rejecting all units with an index greater than -21.3 dB, there is indication that most of the substandard units would be eliminated. However, a significant number (approximately 16%) of apparently good resistors would also be rejected. None of the "quiet" resistors showed abnormal performance during the load life test.

The tests performed do not necessarily show that noisy resistors are poorer than quiet resistors, but that units exhibiting current noise characteristics greater than other devices of their family are reliability suspects. Carbon composition resistors exhibit a total lack of correlation. Carbon deposition resistors, however, have exhibited a correlation between abnormal behavior in load life and higher value of noise.

A typical application of this approach is reported in Reference 12, where 909 tin oxide resistors were tested using a noise index rejection limit of -15 dB. Twenty-three resistors were rejected. It is stated that there was no apparent correlation between either resistance value and current noise or between applied voltage and current noise. Also, different manufacturing lots of the same resistance value exhibited different current noise characteristics. It is observed that resistors which are outliers of the lot should be rejected even when they are well within the noise index specified.

Excess noise of transistors at 1000 Hz was investigated as a function of lifetime in Reference 13. In order to reduce test time, an aging temperature of 350°C was used for silicon devices 2N697, 2N914 and 2N1565. It was found that the low frequency noise for individual parts remained fairly constant throughout most of the test, while other parameters such as base current changed gradually. As failure of the part was approached, the excess noise changed very rapidly, increasing by two to three orders of magnitude, well before other parameters evidenced a marked change. It was concluded that low frequency excess noise can provide a warning of impending failure in transistors that is more sensitive than other parametric measurements.

In Reference 14, excess noise was considered to consist of two components. One is called "clean" noise which is statistically regular and the other irregular component is called burst noise. It was postulated that burst noise is closely associated with parameter drift and results from nonstationary processes arising from irreversible breakdowns and chemical actions. Burst noise was investigated on tin-oxide film resistors, diodes, lead sulphide photoconductive cells, tantalum capacitors, silicon temperature sensing resistors, germanium transistors, dry cell batteries, and carbon film resistors. Noise from items such as carbon film resistors, diodes, and transistor junctions showed the inverse power versus frequency characteristics. However, noise from electro-chemical processes such as in the dry cell battery showed that the power varied inversely as a function of the frequency raised to a power between 1 and 2. Tests were performed to determine correlation between noise and parameter drifts of germanium transistors. Parameters investigated were gain and leakage current. No such correlations were able to be established as a result of these tests.

In Reference 15, an evaluation of radio frequency noise in the range of 2 to 30 megahertz was made on 1N645 silicon diodes and on solid tantalum capacitors. The intent was to establish and validate RF noise measurements as a technique for screening these parts. In the course of performing RF interference tests required for military equipment, Honeywell had occasionally observed high noise levels which resulted from intermittent faults within the equipment. Mechanical shock at times would aggravate the condition, and faulty parts on a subassembly could be located by tapping each part with a phenolic rod to determine which one caused the highest noise. The evaluation program included a study to optimize the techniques for measuring RF noise. To evaluate RF noise measurements as a screening test, conventionally screened diodes and capacitors were subjected to noise measurements and then placed on life test. Correlation between noise level and life performance was attempted, and an investigation into failure mechanisms which cause RF noise was made.

Of 20,200 diodes screened conventionally and subjected to RF noise measurements, 86 passed all specifications and exhibited excessive noise. Of 9,808 capacitors screened, 67 noisy parts were detected which passed all other requirements. The percentage of noisy parts was, therefore, relatively small. One of the sources of diode RF noise was determined to be microplasma. One sectioned diode was examined in a darkroom and it was noted that light intensity of the discharges and the RF noise intensity behaved similarly as temperature and applied voltage was varied. Sectioning of 20 noisy diodes at the end of test provided no other definite conclusions regarding noise sources and causes of poor operation. RF noise in the capacitors was in the form of spikes, rather than of a sustained nature. It was believed that the noise was generated from variations in the oxide film thickness due to irregularities in the tantalum surface. Breakdown and subsequent healing at irregularities would result in current impulses and noise.

The results of life tests are shown in Figures 6 and 7. Seventy-eight noisy diodes and forty noisy capacitors were placed on life test, the diodes for 3000 hours and the capacitors for 2000 hours. Failure criteria were the specification limits for diode leakage current and forward voltage drop, and capacitor dissipation factor and leakage current. Quiet capacitors and diodes were simultaneously placed on test at maximum rated conditions for comparison purposes. It is seen from Figures 6 and 7 that the noisy diode failure percentage was almost twice that of the quiet diodes. The noisy capacitor failure percentage was almost three times that of the quiet capacitors. It was concluded that parts containing high RF noise have a higher incidence of failure than parts that do not exhibit such noise.

On completion of the life test, all diodes that were still operating were re-measured for RF noise. It was found that almost all diodes were quiet. Of 49 initially noisy diodes still operating, 44 had become quiet. On the other hand, three of the initially quiet diodes had become noisy. It was postulated that the noisy diodes defects, once they survived life test, had cured themselves, and that quiet diodes become noisy before failure.

From the various investigations and test results published, it is concluded that defects in many types of parts exhibit themselves by excess current noise and/or RF noise. However, very little correlation has been established between noise level and type of defect or device life. It is recommended that noise testing be utilized only for detecting mavericks in a production lot, such that parts which have outlier noise indices are considered reliability risks.

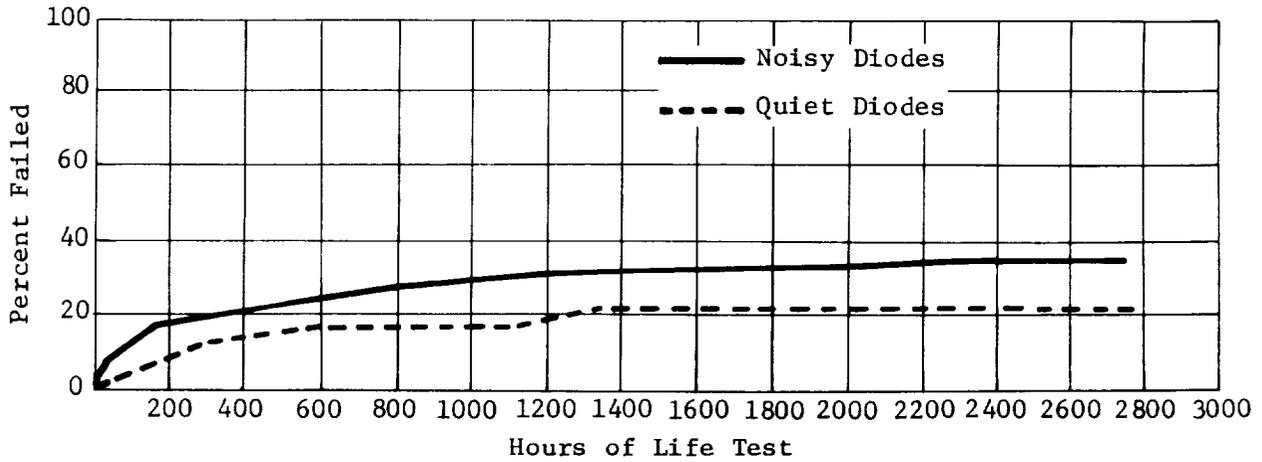


Figure 6 Diode Life Test Results

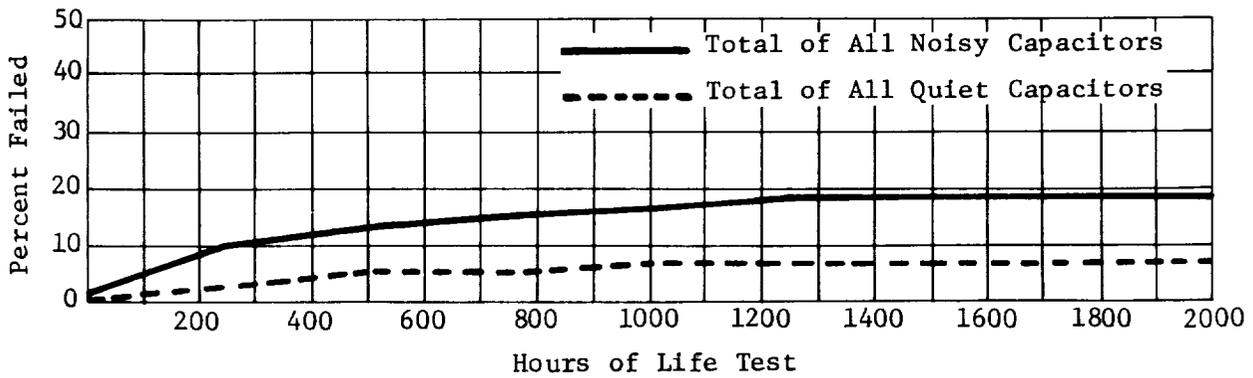


Figure 7 Capacitor Life Test Results

G. THIRD HARMONIC ANALYSIS SCREENING

Harmonic analysis screening is similar to current-noise testing in that it is also a "zero time" test which is economical to perform and has little schedule impact. It utilizes the principle that normally linear devices, such as resistors and capacitors, will exhibit non-linearities when containing defects such as poor connections, film discrepancies, or small movements caused by electrostatic forces. In *Electronics Magazine*, of 4 April 1966, it is reported that the L. M. Ericsson Telephone Co. of Stockholm found a close correlation between the noise in a linear component and the harmonic distortion the component causes when a pure sine wave is applied. The third harmonic technique was implemented to improve the speed of screening which was previously performed by wide band noise testing. Noise testing typically consumed about one-half second per resistor, while the third harmonic equipment could process resistors at a rate of 20 per second. Non-linearities are indicated by third harmonic content when a sinusoidal 10 kilohertz wave is applied to the part. As this is applied to batch processing, a sorting device is coupled to the tester to separate rejects. Similar to current noise testing, further reliability of a batch can be achieved by eliminating parts whose non-linearity is an outlier of the batch.

Although third harmonic testing has received relatively little attention in this country, it was investigated as a promising technique for detecting surface related defects in integrated circuits (Ref 16). Fifty integrated circuit packages (100 gates) from each of four manufacturers were used in the principal experiment. These represented two logic configurations and two fabrication technologies. An additional 15 packages (30 gates) from each manufacturer served as controls and spares. Two of the circuit types were TTL dual four-input gates and the other two were DTL dual four-input gates. All circuits were initially subjected to a stabilization bake for 20 hours at 250°C to erase past history and stabilize characteristics. Initial data was taken after stabilization bake. Devices were checked for normal switching action. Sundry parameters, including second and third harmonic distortion, were measured. Although some distortion is always present in any integrated circuit biased in the Class A linear mode, it had been previously postulated and verified that excess distortion could result from surface inversion layers, especially when they occur over active regions of the device. Harmonic content of the circuit output was measured when driven with a pure sinusoidal fundamental signal.

All specimens, except the control samples, were then exposed to a preconditioning environment of 5×10^4 roentgen cobalt-60. The purpose of preconditioning was to accelerate formation of inversion layers in the devices with such defects. A second set of measurement data, including harmonic distortion, was then taken. A comparison of the pre- and post-radiation data revealed no parameter trends or correlation between parameter changes and the exposure. It was assumed that the surface passivation of the circuits was very good.

Following preconditioning, all specimens, except the control samples, were put on life test for 4080 hours at a temperature of 165°C . The specimens were biased, unloaded, and driven by a 1.0 kHz square wave generator. A final set of data was obtained to identify failures and to determine the changes which occurred in harmonic distortion. There were eleven pertinent failures. No correlation was found to exist between failures and high harmonic distortion. It was noted that specimens, which exhibited large harmonic distortion, generally had more obvious deficiencies. It was concluded that harmonic distortion measurements are of little practical value for screening integrated circuit surface defects.

From these results, it is concluded that the value of third harmonic analysis screening is limited to linear passive parts and is unsuitable for active parts. Also, the value of this approach probably lies in the detection of mavericks in a production lot as exhibited by above average distortion values. Further investigation of this approach should be made before implementation as a screening requirement.

H. SHORT-TIME OVERLOAD TESTING

Overload testing is commonly performed on resistors to enhance detection of defects such as contamination, thin spots in wires and films, termination problems, and to detect weaknesses that may cause failure under circuit transient conditions. A large variation in voltages, durations, and power levels used exists among the various types of resistors, and also between users of a given type. Generally, all discrete resistors have a voltage and power capability in excess of their ratings. At times, when resistors are used under continuous transient conditions, such as in pulse applications, there may be little relationship between normal ratings and the transient capability. Conventions such as pulse power rating of 10 times DC power rating and pulse voltage rating of 1000 volts per inch may not be realistic. Such conventions may handicap a design by unnecessarily requiring a physically large component. An interesting study (Ref 17) which was performed by Sandia Corporation demonstrated the short time capability of various resistors. For instance, it was found that wire wound resistors could withstand from 8 to 48 kV. of 20 micro-second pulse voltage, depending on wattage rating and resistance. Metal film resistors varied from 200 volts to 50 kilovolts, and carbon composition resistors varied from 200 volts to 20 kilovolts. Pulse power capability varied from 500 times rating for carbon composition, to 1000 times rating for metal film, to 5000 times rating for wire wound resistors. The larger resistance values and power ratings had the greatest capability. In viewing these results, it must be considered that during the tests, average power was always within the resistor rating, the duty factor was less than 1%, and the criteria for success was the capability to withstand a minimum of 100 pulses without catastrophic failure. The results illustrate, however, the general increase in capability with reduced test time.

The more conventional short time tests are those utilized in conjunction with military specifications such as MIL-R-39017, MIL-R-39005, and MIL-R-55182. They are variously referred to as power conditioning, overload, or short time overload tests. The power levels may be from 1-1/2 to 5 times rated power and the durations from 10 minutes to 24 hours, depending on type of resistor and user. Power conditioning tests are designed to stabilize the resistor. Overload tests are designed to precipitate defectives to failure. The overstresses should be high enough to eliminate "bad" parts but within the capability of "good" parts. A common criteria for rejection is an allowable percent resistance change during overload. This requires resistance measurements before and after test.

Another approach, not as widely used, was developed by Dale Electronics, Inc. for use on wirewound resistors they supplied for Minuteman. It is called the GARD system, which is an acronym for Graphic Analysis of Resistance Defects. In this approach, resistance measurements are not made, but a recording of percent resistance change is made during the application of a controlled pulse of maximum non-destructive power. The power level is selected to bring the resistance element temperature up to a point which is just below that which would damage the resistive material. It is generally 5 to 20 times the rated power applied for a period of 5 seconds or less. It is claimed that since the temperature rise is effected in such a short time period, the differential expansion creates higher stresses than would be encountered in normal operation. As resistance changes are recorded, the graph not only provides a record of the total delta shift during test, but also displays the time variation of resistance changes. Good resistors of the same type and value display smooth parallel curves. A deviant resistor shows up as a ragged curve or a smooth curve with a different slope. Defects such as shorted turns, bad welds, conductive contamination, and poor terminations show up as ragged curves. Wire which will exhibit excessive shift over extended load life or has an excessive temperature coefficient of resistance will show up as a smooth curve with a deviant slope.

It is claimed that a 5 second GARD test can supersede the standard burn-in approach which is usually 100 hours. Test results have indicated that (1) in no case has the GARD system failed to detect defects which would result in catastrophic failure, (2) in no case has the GARD system failed to detect a defective part which would fail the load lift test of Established Reliability Specifications, (3) in all cases the GARD test has been more sensitive and screened out more defects than the 100 hour burn-in test, and (4) good correlation has been achieved with failure analysis. Substitution of GARD testing for burn-in will also reduce cost and cut delivery time by about a week.

Reference 18 describes typical results of tests which were performed to verify the effectiveness of GARD. These included the manufacture of parts with built-in defects, large quantity GARD testing of standard production units and analyzing rejects, comparing results of GARD tests with standard burn-in tests, and relating results of long term life tests with GARD test predictions. It is reported that all units manufactured with intentional defects were detected in GARD tests. From continuous production

GARD tests, a total of 2,095 parts were rejecte/ in one period of time. All were failure analyzed. Physical or material defects were verified in 97% of the units. It was believed the other 3% contained metallurgical or stress induced anomalies difficult to detect by analysis. As the GARD test is non-destructive to good parts, burn-in was also performed subsequent to GARD on many samples. A typical result reported on a sample of 1400 resistors is that GARD detected all burn-in rejects and an additional 4.3% which passed burn-in. A typical 1000 hour load life test on 1,824 resistors showed that GARD detected all units which exceeded a 0.15% resistance change. On another test of 2,800 resistors, GARD detected all outliers of the group distribution after 1000 hours of overload. On another group of 25,000 resistors, GARD, momentary overload, and 100 hour burn-in tests were performed in that sequence on all resistors. The GARD test rejected 102 units, the momentary overload rejected 27 units, and the burn-in test rejected 11 units. The GARD test detected all burn-in rejects but only 23 of the momentary overload rejects. Another 19 units rejected by GARD would have been rejected by momentary overload if an outlier criteria had been used.

Shallcross and Sage have also utilized this approach to a lesser extent. The users have included JPL and BTL. Autonetics, for Minuteman, has been the major user. JPL presently uses GARD on Dale resistors only, but also requires a 168 hour burn-in because it is believed that GARD does not provide stabilization or strain reliefs that are derived from longer term tests. The approach has been used to a lesser extent on film resistors. Gross defects such as bridging or thinned metalizations have been detected, but in general the power must be brought to levels which are damaging to good parts in order to detect more subtle defects.

In Reference 19, the effectiveness of various screening tests for thin film resistors is analyzed. The tests considered were 100 hour burn-in, current noise, short time overload, and power conditioning. The approach used was to subject a group of parts to the particular screen test being evaluated, note the rejects, and then submit both accepted and rejected parts to a 1000 hour load life test. Tightened limits ($\pm 0.25\%$ resistance change) were used to classify load life failures. The burn-in consisted of full rated load at 125°C, 1 1/2 hours power on, 1 1/2 hours power off. Reject criteria was $\pm 0.10\%$ delta change. The current noise criteria was -20 dB at rated load. The short time overload consisted of 2.5 times continuous working voltage for 5 seconds.

Reject criteria was $\pm 0.10\%$ delta change. The power conditioning test consisted of four times rated load for six hours, and reject criteria was $\pm 0.25\%$ delta change in resistance. The results of test data analysis is shown in Table 11:

Table 11 Resistor Screen Test Effectiveness and Efficiency

Screen Test	% of Parts Rejected by Screen	% of Rejects Which Passed Load Life Test	% of Load Life Failures Detected in Screen
Burn-In	3.4	58	92
Current Noise	67.6	91	74
Short Time Overload	11.4	50	71
Power Conditioning	8.9	77	69

On the basis of this data, the burn-in tests as performed appears to be the most effective as 92% of the load life failures were detected. The other three screens were about equally effective, but the current noise test used was very inefficient as 91% of the rejected parts did not fail load life testing. It is possible that a different current noise reject criteria coupled with outlier detection may have been more effective and efficient. The power conditioning and short time overload tests are both similar overstress tests, the difference being in level and time duration. Outlier detection may also have increased the efficiency and/or effectiveness of the other screens.

The short time overload tests can be roughly categorized by time duration. The very short term tests such as GARD are in the order of seconds, overstress power conditioning tests or overload tests are in the order of hours. Tests in the order of seconds are performed at 5 to 20 times rating, tests in the order of hours are performed at 1 1/2 to 5 times rating. Bell Telephone Laboratories utilizes a one hour overload test on thin film resistors for some high reliability applications. These are conducted at 4 to 5 times rating and the usual 100 hour burn-in is not required. Wirewound resistors are tested for 1 to 2 1/2 hours at 1 1/2 to 2 times the power rating.

The large variety of short time overload tests used indicates the need to tailor such tests to individual parts. *A universal short time overload test does not appear feasible.* The very short tests such as GARD appear to be effective on wirewound resistors but not suitable for thin film resistors. *It is recommended that GARD tests be used only on those wirewound resistors where data exists to support its effectiveness,* such as on the Dale product. Evaluation of effectiveness on other products is necessary before implementation. To assure the highest quality product, burn-in or a longer term overload test is also necessary (1) to eliminate defects which require a time under stress and (2) to provide stabilization. For both wirewound and thin film resistors, overload tests in the order of one to two hours can probably be used effectively in lieu of either the GARD approach or a long term burn-in approach. It is recommended, however, that elimination of burn-in and use of such overload tests be implemented only where data exists which justifies this approach. Where data does not exist, evaluation must be performed to determine the maximum overload temperatures desired and the optimum time at these temperatures.

I. OPTIMIZATION OF STRESS SCREENS

The variations that exist between manufacturers in designs, materials, processes, and controls result in corresponding variations in reliability grades for each part type. Screening will not improve the lifetime of any individual part, but can remove the incipient failures so that the life distribution of the survivors has a greater mean value than the original group. It is to be expected that with a given screen, the mean life and the dispersion will vary from manufacturer to manufacturer and to a smaller degree from lot to lot. The variation from lot to lot will be minimal where high quality, well controlled processes are utilized such as in "hi-rel" lines.

The conventional standard screen tests are related to life capability only in that the most unreliable parts are eliminated. However, these tests do not determine the longevity or reliability grade of the survivors. Considerable variation in life capability could exist therein. Emphasis must be placed on identifying time dependent failure mechanisms, minimizing them by proper part design, and establishing means of detecting them in early stages of their activation. In Volume II of the RADC Reliability Notebook it is pointed out that constant failure rates for most parts does not exist. Physical and chemical degradation laws require the failure rate to increase with time. Some semiconductor failure rates have continued to decrease with time, indicating the "wear-out" period or the right hand rise in the bathtub curve is considerably beyond experience accumulated to date and may be in excess of hundreds of years for many parts. Where the failure rates have been observed to decrease with time, investigation has shown that the situation is in reality extended debugging or screening-in-service on the left hand side of a bathtub curve with a gradual negative slope.

Figure 8 shows the comparison between a lower and an upper grade reliability product.

Wide variations in distributions can be expected from a manufacturing line producing the lower grade parts, while distributions from a line producing upper grade parts will be similar from lot to lot. It is much more difficult to discriminate between the low and high reliability parts of the lower grade distribution. Stress screens (such as burn-in, constant acceleration, overload, thermal shock, etc.) attempt to perform this discrimination on

the basis of part strength. The lower reliability parts presumably contain weaknesses or defects which can be precipitated to failure (or to a detectable change) by a stress level and duration which does not adversely affect the higher reliability parts. If the strength distributions of good and bad parts are markedly distinct, as in Figure 9, then any stress in the range separating the two distributions will be effective as a screen.

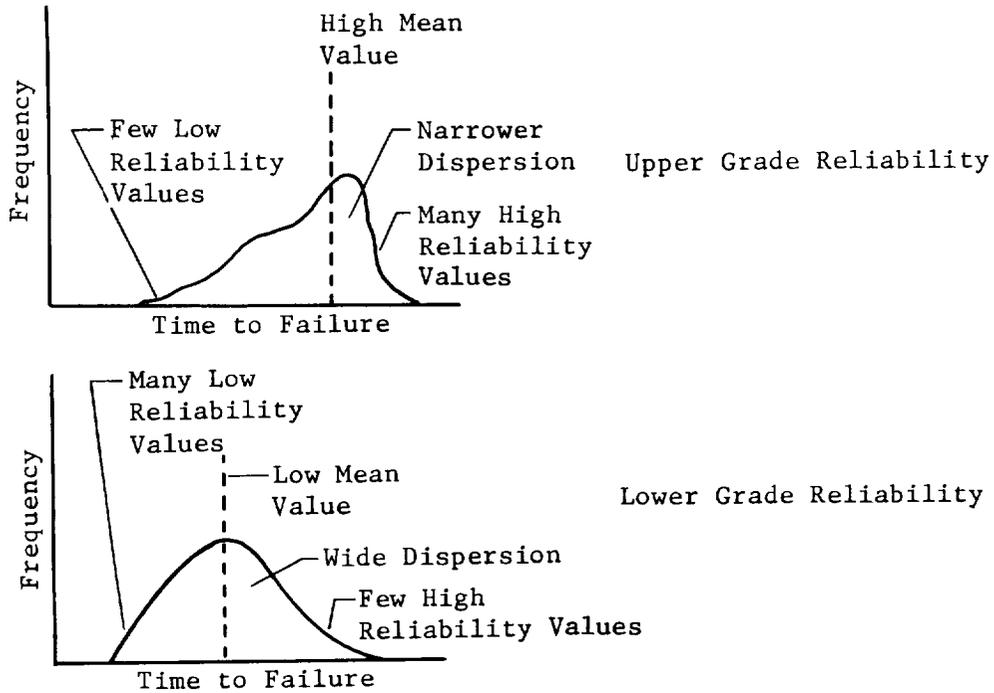


Figure 8 High and Low Grade Failure Distributions

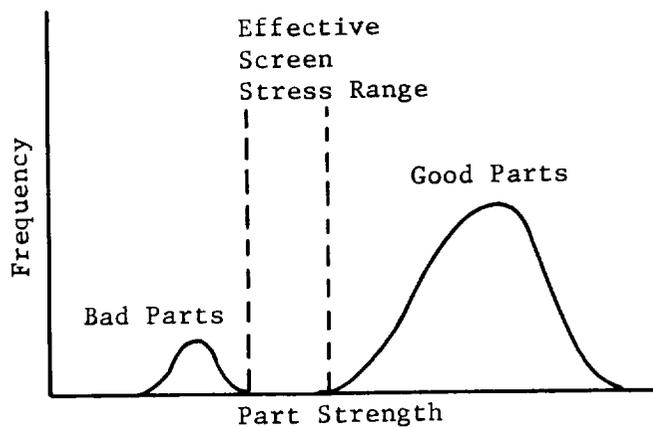


Figure 9 Strength Distributions

The situation illustrated in Figure 9 occurs when abrupt unintentional changes in materials, processes, or workmanship happen. A portion of wire welds, for example, may be weak due to corroded or contaminated materials in combination with schedule variables. Pull tests in the effective stress range would eliminate such bonds, but would not adversely affect good bonds. Each stress must be oriented to detect a specific weakness or failure mechanism. The distributions of Figure 9 are not separated so markedly when processes/materials fluctuate considerably (lower grade product) and the margin of the part varies widely from time to time. In this case, a screen stress level may well indeed degrade the low margin product. The effectiveness of screen test stress levels is enhanced by adequate product margin.

Figure 10 illustrates the effect of screen test stress level on a group of parts which have stress strengths as shown in Figure 9. Very low stress levels are ineffective because of the inability to detect bad parts. Levels which are too high are damaging to good parts. An effective stress range is shown for this situation which will accomplish the screening objective. For long-life purposes, the optimum stress level is defined as the screening stress level which provides survivors having the maximum average life in service. The optimum stress level should lie within the effective stress range and, from the definition, close to the upper boundary. For long-life purposes it is important that weak or defective parts be eliminated with maximum efficiency.

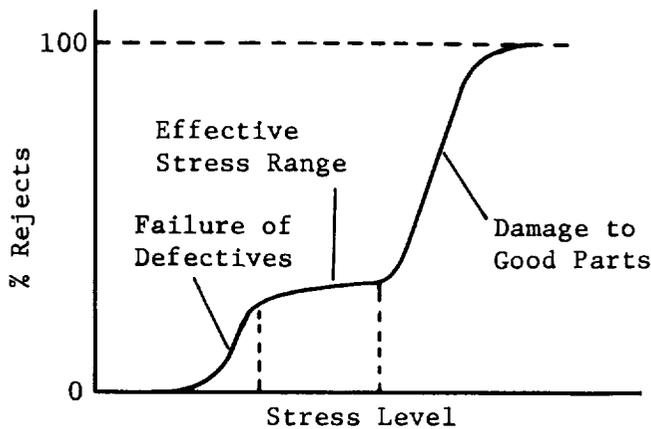


Figure 10 Screen Stress Level Effect

An optimum screen stress level which is suitable for the product from one manufacturer may not be suitable for the product of another, even if the parts are interchangeable. To a lesser extent, optimum levels may vary from lot to lot within a given manufacturer's product. Variations will cause shifts and changes in the shape of the reject curve of Figure 10. If a single screen test level is required for all the variations, the optimum level will be a compromise lying, insofar as possible, within the effective stress range of all products. The optimum level will provide the degree of weak part acceptance and good part damage which still results in maximum average survivor service life. If these considerations are extended to classes of parts, it is difficult to visualize an optimum level existing for all parts within the class, such as for all silicon transistors or for all film resistors. Many of the standard screen tests and levels which have evolved, however, are justified by a huge amount of data and experience testifying to their adequacy.

The consideration of screen stress level to obtain maximum life has been centered on the part capability and not on its use. It is assumed that for any set of service conditions, the survivors of an optimum screen will have a longer average life than the survivors of a non-optimal screen. This assumption may not be valid if parts are subjected to use stress types or environments (such as radiation) that were not utilized in the screens. In general, it is desired that the good part capability be greater than the screen stress level, the bad part capability be less than the screen stress level, and the screen stress level be greater than the usage stress level.

Although the conventional standard screens may be adequate for most parts, there may be specific occasions when it is desirable to optimize them. For example, such as when defects are known to be passing these screens, or when a new part containing unique metallurgical or process systems is being considered for use. The simplest approach is a qualitative one. From Figure 10 it is implied that the optimum screen stress level is near the upper limit of the effective stress range.

Another way of viewing this situation is that the optimal screen is close to the level which would degrade good parts. Then merely finding the highest stress level which a good part can withstand without degradation should be an approximation of the optimum level. This level can possibly be economically determined by means of step stress testing, as described in Chapter III, "A Study of Accelerated Testing Techniques," included in this volume. Verification of the stress level determined can be made by submitting

groups of parts to a 1000-hour life test. One group should be screened to conventional levels and another group screened to the optimum level. To obtain failures during this period, the 1000-hour life test can be performed at an accelerated stress level. An approach similar to this is reported in Reference 20 where the effects of higher screen stresses on integrated circuits is evaluated. Although an optimum screen level was not being investigated, a set of more stringent (non-optimized) temperature cycling, mechanical shock, constant acceleration, high temperature bake, and burn-in screens were found to reduce the failure rate by 0.03%/1000 hours as opposed to the conventional screens previously used. This reduction was estimated by comparing 1000-hour maximum rated stress test results on two groups of parts. One group was screened to the conventional levels, and the other group was screened to the higher levels.

An example of a more quantitative method to determine optimum screen test levels is illustrated by Figure 11. This shows a hypothetical reject curve, similar to Figure 10, which may pertain to an actual part. The shape of this curve may be obtained by step stress tests to 100% failure on a single group of parts which represents the population to be screened. Quantities of parts are shown subjected to six stress levels within the destructive range so that the quantity which passes each stress level is 30 pieces. The quantities and approach shown are intended only to be illustrative of the technique. The minimum test level S_1 can be chosen near the maximum rating of the part. The maximum test level in this instance is shown as the 75% reject level. As S_1 (minimum test level) and S_6 (maximum test level) have been determined, then intermediate stress levels can be selected depending on the desired number of test groups, in this example six. After performing the stress levels shown in Figure 11, the 30 survivors from each group are then placed in a life test as shown in Figure 12. If greater confidence is required, the quantity in each initial test group could be increased accordingly. The test samples should be unscreened to the particular stress being evaluated.

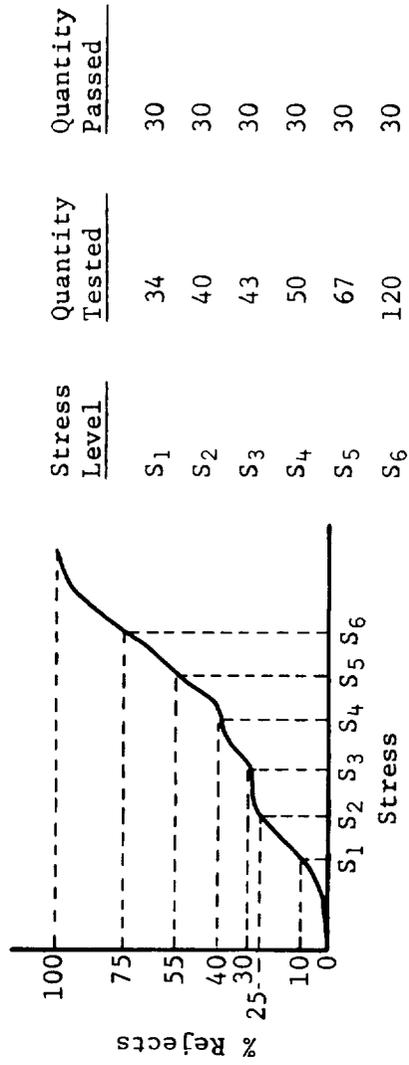


Figure 11 Stress Level Reject Curve

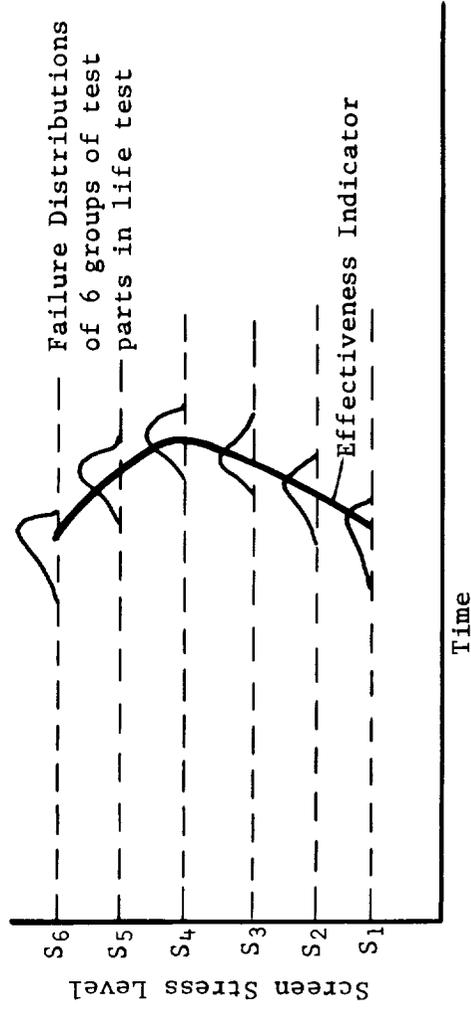


Figure 12 Life Test Failure Distributions

The failure distributions of each surviving group in Figure 12 are shown for a case in which the screen stress type and level can be optimized. The S_1 and S_6 groups from the lower and higher stress levels, respectively, demonstrate the obverse aspects of ineffectiveness. The mean life of group one is shorter because stress level S_1 was too low to remove all defectives while the mean life of group six is shortened because stress level S_6 was high enough to degrade the survivors. The optimum level lies between S_2 and S_5 , and for the test levels illustrated, is S_4 . A curve drawn through the means of each distribution is an effectiveness indicator. If this indicator can be generated to approximate continuous increases in stress level, then obviously the peak of this curve is the optimum screen test level.

Figure 13 illustrates various indicator curves that may be expected from such optimization stress level investigations.

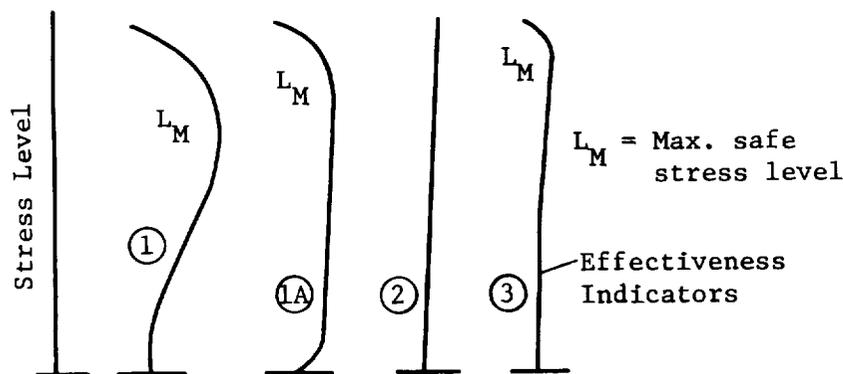


Figure 13 Effectiveness Indicators

Indicator type 1 is similar to that shown in Figure 12 and represents an effective screen stress, with a definable optimum level. Type 1A is similar to type 1 except that effective levels exist over a broad range. Indicator type 2 shows a totally ineffective screen stress, and type 3 shows a stress that may be applied safely to a level L_m . Optimization investigations of this nature would be prohibitively expensive and time consuming if carried to the extreme of each stress on each part type from each manufacturer, particularly if sequential screen stress and/or synergistic screen stresses are considered.

If accelerated tests are acceptable, the time to perform the life tests in Figure 12 can be reduced. The failure distributions obtained under accelerated conditions must be the same as under normal

conditions. Fortunately for many failure mechanisms, (particularly those operating in accordance with the cumulative damage and the Arrhenius rate models,) this situation apparently does exist. When effectiveness curves, such as shown in Figure 13 are obtained, a valuable relationship between screen stress level and longevity of the parts is established.

The success reported by Bell Laboratories with high stress screening (Chapter III) indicates that the stress levels used are possibly close to the upper limit of the effective stress range shown in Figure 10. These high stress levels (300°C junction temperature for transistors) make the conventional burn-in levels seem benign in comparison. The question arises as to the effectiveness of conventional burn-in levels and the relative location on the stress curve of Figure 10. These lower stress levels may lie either in the lower portion of, or possibly below an effective stress range. The implication is obvious. With such a large difference in stress levels, it is doubtful that both approaches could have even approximately the same degree of effectiveness. Also, if the high stress approach does not provide damage or significant consumption of life, it should be the superior and therefore preferred approach for screening long-life parts. The likelihood of a defective or "maverick" part escaping the high stress screen should be significantly reduced.

It is recommended that the Bell Laboratories high stress screen approach be investigated further. Correspondence with Mr. D. S. Peck of Bell Laboratories was made during the course of this screening study. The transmittal letter and his reply are reproduced in Section K, herein. The conviction is expressed that the lower stress levels are not as effective as the high stress levels as justified by their experience. This approach is attractive as a potentially economical and effective means of improving long-life reliability, providing that minimal evaluation effort is involved. It is suggested that investigation of this approach be pursued to definitize the means of implementing high stress screening as opposed to performing research regarding the basic validity or the precise physical models involved. The implementation should take maximum advantage of experience obtained by others previously, thus minimizing the duplication of costly learning curves which may include false starts and initial errors. The implementation approach should consider the following:

- 1) Identification of specific parts which have been successfully high stress screened. Collection and review of back-up data which was used to justify or establish the screen.
- 2) Inclusion of the screen requirement directly in specification for those parts in 1) which are to be used in high reliability applications.

- 3) Determine the feasibility of applying the high stress screen to entire classes of parts such as silicon, planar, aluminum metallized transistors.
- 4) Identify the minimum evaluation effort required prior to high stress screen implementation on transistors and integrated circuits.

In Reference 21, eleven integrated circuit types were subjected to step stress limit tests in power, centrifuge, and thermal shock. All devices, except one type, were tested through 150,000 g's without significant failure. The one device type had 50% failure at 120,000 g's, which were die bond failures. It was determined that insufficient heating failed to create a good joint between the glass frit and package bottom. Again, on thermal shock limit tests, the circuits showed a marked resistance to extreme limits. Six of the eleven types had no failures after 150 cycles from -195°C to $+200^{\circ}\text{C}$. Failures occurred primarily on an obsolete glass and metal flatpack and on ceramic devices. The limit tests were not performed to optimize screens, but to provide insight into failure mechanisms and to examine the relationships of stress environment to failure rate in conjunction with deriving an integrated circuit reliability prediction model. However, high temperature storage tests on unstressed parts and survivors of the centrifuge and thermal shock limit were performed. Of 22 comparative groups (two temperatures, 300°C and 350°C for each of 11 part types), three of the unstressed samples were superior, ten of the limit tested samples were superior, and the other nine comparative samples were approximately equal in failures after 1000 hours of test. The implication is that for many of these parts, higher levels of centrifuge and thermal shock may provide a more effective screen test.

J. UNCONVENTIONAL SCREENING TECHNIQUES

In this section some unconventional electronic part screening techniques are briefly reviewed. They are unconventional in that they have found little or no industry use, to date. Some are new and in the process of development. As they are not in wide use, they may be controversial. The particular techniques considered may have applicability to the pressing problems of contamination and complex integrated circuit testing.

1. Neutron Radiography

The advantage of neutron radiography is that the attenuation of a neutron beam is proportional to scattering cross-section and is independent of atomic number while X-ray attenuation increases with atomic number. Hydrogenous materials have high neutron attenuation coefficients and are therefore particularly suited for neutron imaging. Materials, such as lead, iron, titanium, and aluminum have low coefficients. This has made neutron radiography particularly suited for inspection of items such as metal enclosed explosives and epoxy bonded honeycomb. Hydrogen embrittlement of titanium welds shows easily, and it is possible to determine moisture content in ceramics with this method.

The basic neutron radiographic systems are described in Reference 22. They each consist of a source, a collimator, a conversion screen, and an image recorder. Neutrons emanating from the source are generally isotropic. The collimator is used to extract a nearly monodirectional beam from the source. The collimated beam passes through the specimen being radiographed, is spatially modulated by the attenuation characteristics of the specimen, and activates the conversion screen accordingly. An activity image is created on the conversion screen which is transferred to the image recorder by ionizing radiation from the conversion screen. The image recorder can be X-ray film. If the neutron beam contains no gamma radiation component, direct exposure of the X-ray film can be made. The best resolution with the film placed in contact with a thin conversion screen is approximately one mil (Ref 23).

Many of the contaminants common in electronic parts, particularly the non-metallics, cannot be detected by X-ray inspection. Neutron radiography may have applicability as a supplement to X-ray in detecting such contaminants. In Reference 24 it is stated that lint between relay contacts can be imaged. Also, parts such as

barium titanate capacitors, which show up opaque on X-ray, are easily inspected for construction detail with neutron radiography. Application of neutron radiography to aerospace inspection problems such as O-ring seating within steel flanges is briefly discussed in Reference 25.

The major drawback is the requirement for a source, which can be isotopic, and accelerator, or a reactor. Obviously, wide-spread neutron radiographic capability at electronic part manufacturing facilities cannot be anticipated. Such inspection will have to be performed by the user, either in his own facility, or by use of available existing facilities.

2. Combined Shock and Vibration, Monitored

Reference 26 reports that observation of deliberately induced conductive particles into integrated circuit packages showed that the particles would bind to certain locations. Presumably, a bound particle may cause no trouble during vibration or parametric testing, but may be torn loose by a subsequent shock and cause a short. A combined shock and vibration approach was developed to improve on existing conductive particulate contamination detection methods. A rotary vibrating polisher was modified with a mounting plate; the combined assembly provided a maximum acceleration of 6 g's at 20 Hz. Shock is provided by a solenoid hammer which imparts 150-200 g's to integrated circuits mounted on the plate. It was determined that a shock of less than one millisecond duration in excess of 50 g's is required every few seconds to release a bound particle and maintain it in an unbound state. The low frequency vibration is designed to impart a high velocity to the particle and cause it to traverse the package and induce a short between susceptible conductors within a few minutes of vibration/shock.

Analysis showed that the minimum collision momentum exchange time, or shorting event, was 10^{-7} seconds. The test circuit therefore required a bandpass of 10 MHz to detect all shorting events. The integrated circuit is monitored by the test circuit for the occurrence of shorts during vibration/shock testing. The test time required for a short to occur is dependent on particle dimensions, package volume, and circuit terminal configuration.

This approach appears to provide an improvement over existing particle detection techniques, but may not be 100% effective. In Reference 27, high speed movies (5000 frames per second) were taken of particle behavior in components with glass cases to determine detection circuit requirements and optimum particle excitation conditions. It was found that the monitored test does not provide 100% effectivity and both X-ray and acoustical methods are needed at times depending on component conditions.

3. Laser Scanning

The laser scanning system described in Reference 28 has the distinct advantage that mechanical probing is minimized. A laser beam is directed to a mirror which scans the beam horizontally at a 600 Hz rate and vertically at a frame rate variable from 1 to 10 Hz. A standard microscope focuses the beam to a one micron spot size on the device being scanned, usually an integrated circuit chip. Two mechanical probes are used to sense the effects of scanning, one on the power supply line and the other on the ground pad of the chip. As the beam scans the chip, it penetrates the semiconductor material depending on the chip structural features at the location of the beam. In the region where metalization exists, the laser will not penetrate. In other areas, the beam changes the conductivity of the material and the effect can be seen as a varying current on the power supply line. A scope synchronized to the laser scan is used to display the current variations and obtain a picture of the chip structure. Both structural faults and electrical characteristics of internal devices can be evaluated. In Reference 28, both optical and laser scan photographs are shown of a chip, for instance, which has an open in the metalization. Diffused resistors, metalization, transistors, and isolation junctions can be shown with variable enhancement by means of changing the supply voltage and laser intensity. For many digital integrated circuits, nearly all transistors can be forced into the on state, either by the laser light acting as a pseudo base current or by an appropriate setting of the supply voltage.

In Reference 29, it is reported that a second laser has been added to the system which can be directed to any area of the chip and activate any transistor. The second laser can overcome base impedances of 1 to 2 kilohm and in effect exercise the integrated circuit through all possible states with near probeless testing. Transistor gains have been measured using the video pulse data, with 2 to 3% accuracy, and internal base resistances and leakage currents have been analyzed.

4. Automatic Inspection

Automatic inspection techniques are attractive from the standpoint that human judgment and error can possibly be eliminated, rapid check of close dimensional tolerances may be feasible, and the automatic inspection system should not develop fatigue. One of the optical approaches investigated recently (Reference 30) projects a production part image onto a photographic negative of the master.

If the production part is illuminated properly and if the proper range of densities and contrast exist on the master negative, the resultant composite image will be a uniform gray in all areas where the production part is identical to the master. Depending on the relationship between the negative and the part being inspected, areas of difference will result in bright and dark areas. The resultant image is scanned with a television camera and displayed if desired. The video signal from the camera contains pulses corresponding to the dark and bright areas, the pulse width being proportional to dimensional differences between the master and the part being inspected. The information in these pulses can be used to provide automatic accept or reject decisions if the pulse widths correspond to dimensional mismatches beyond acceptable tolerances. This type of system requires accurate positioning of the inspected parts, but again the pulse signals themselves may be used to provide the positioning. It is reported in Reference 30 that inspection accuracies of 2-1/2 microns have been demonstrated and that this can possibly be improved. The speed of inspection is determined by the speed of mechanically handling the parts.

Another approach consists of comparing the part to be inspected against a master part rather than photographic negative. A flying spot scanner provides a dot of light which sweeps the inspected area. A beam splitter divides the light between the inspected part and the master. The light reflected from each is detected by photomultipliers and the outputs are electronically subtracted. Again, where the parts are identical, the difference is zero, but where they differ, the signal contains pulses.

Gross inspection requirements, such as checking printed circuit boards for missing parts or for accurate patterns is entirely feasible with these techniques. However, it is claimed that they can be used to inspect detailed features of integrated circuits. A rapid, accurate, automatic inspection to criteria, such as MIL-STD-883, would certainly be desirable.

K. BELL LABORATORIES CORRESPONDENCE

Included herein are reproductions of a transmittal letter to Mr. D. S. Peck of Bell Laboratories and his reply. This correspondence was entered into as a part of this study in investigation of high stress screening for improved long-life reliability of semiconductors.

MARTIN MARIETTA CORPORATION

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DIVISION**

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28 June 1972

Mr. D. S. Peck
Bell Telephone Laboratories
555 Union Boulevard
Allentown, Pennsylvania 18103

Dear Mr. Peck:

Attached is a listing of transistors by 2N number which is used as a basic selection guide by our circuit designers. This is a preferred type listing and, while it does not cover all requirements, approximately 90% of our procurement volume is with these types.

As I indicated in our telephone conversation on Monday, we are performing a study for the Manned Spacecraft Center (MSC, Houston) related to Shuttle. The study will include recommendations for screening various electronic parts. In the constrained cost environment that exists in the aerospace industry today, we feel that our recommendations must provide the most cost effective approach obtainable. The methods which you have been advocating for some time are very attractive in this respect, particularly in the area of burn-in levels. The high junction temperatures under reverse bias and/or forward power conditions make conventional test levels appear benign in comparison.

The performance of high stress screening is assumed to be relatively straight forward and economical to implement once stress levels and durations are identified. It may even be possible to effect savings on screened parts due to shorter test durations. The problem is primarily one of justification and minimizing the amount of evaluation testing to determine levels and durations. It is hoped that your extensive experience with high stress screening can be utilized as a basis for recommending it to NASA.

The attached transistor list is anticipated to be nearly identical to that which will be used for Shuttle. It should serve as a typical example to evaluate feasibility of this approach. It would be very desirable if you have used many of the parts (or equivalents) on this list and have subjected them to high stress screens. Your thoughts and comments on the approach we are contemplating would be appreciated. It would be particularly valuable if it is possible for the following questions to be addressed:

1. Which parts on the list have been successfully high stress screened in your usage?

Mr. D. S. Peck

28 June 1972

2. What type of evaluation tests (if any) would you suggest for those parts on the list you have not used?
3. Are there further evaluation tests you foresee on parts which you have previously used and which you have previously high stress screened?
4. Do you think it feasible to specify, without further evaluation testing, a universal test level and duration on certain classes of parts? (Such as silicon, planar, passivated, aluminum metallized transistors.)
5. Do you foresee any technical or legal barriers to utilization of your past experience as either the basis for general justification of the approach, or for minimizing evaluation testing by NASA on specific parts?
6. What method of implementing high stress screening would be most mutually beneficial to Bell Telephone Laboratories and NASA?

If you wish to discuss any of these items in further detail, my telephone number is (303) 794-5211, extension 4327. Thank you very much for your courtesy and cooperation in returning my call.

Very truly yours,

S/ R. A. Homan 6/28/72

R. A. Homan
Staff Engineer
Electronic Test and Analysis

RAH:11
Attachment



Bell Laboratories

555 Union Boulevard
Allentown, Pennsylvania 18103
Phone (215) 439-6011

AIR MAIL

July 28, 1972

Mr. R. A. Homan
Staff Engineer
Electronic Test and
Analysis
Martin Marietta Corporation
Post Office Box 179
Denver, Colorado 80201

Dear Mr. Homan:

This is in response to your letter of June 28, 1972, regarding the high stress screening of transistors for NASA applications. Your interest in this technique is very much appreciated since we feel that the data which we have indicates clearly that the retention of freak devices is very probable when screens are used at lower stress levels, and these devices will cause failure rates considerably above those that the product is capable of providing. Although we have had very little opportunity to compare actual field reliability of product bought to our specifications with the usual commercial or military product, we do have the experience of obtaining failure rates below 10^{-8} /hour with transistors made to similar specifications.

I can address the specific questions in your letter as follows:

1. The parts on your list which we have screened at high stress are the 2N2222A, 2N2369A, 2N3251A, 2N2905A, and 2N3467.

2. The type of evaluation tests which we would suggest for the parts we have not used would be, first, the establishment of the actual thermal resistance and from that a power condition which would result in a junction temperature of 300C; second, the establishment of a life distribution to confirm that the product can take a 16-20 hour screen at this condition without generation of unusual failure modes and that the main life distribution is at a time consistent with the reliability objectives. This would accomplish an evaluation for failure modes related to the movement of ionic charges at the silicon surface with resultant inversion of the surface. Other evaluations, to determine design suitability for hermeticity, strength under shock or vibration, etc. would presumably be no different than what might be in the present program.
3. With regard to the parts which we have previously used, I do not expect that further evaluation tests would be required but it would probably be desirable that we review the specification and the earlier test results, an exercise which I have not done yet.
4. The data which we have available on a large number of planar silicon transistors with aluminum metallization suggests a common screening condition required to eliminate freak devices with respect to the surface inversion failure mechanism. This would be the 20 hours at 300C junction temperature indicated above, or an equivalent time at lower temperature according to the 1-eV activation energy of this mechanism. I believe, on the other hand, I would be somewhat reluctant to specify a current and voltage condition assumed to attain that junction temperature without at least evaluating that the devices will not have other problems such

as, for example, second breakdown. The answer for integrated circuits is considerably more complicated; although the same failure mechanism can be expected and must be screened for, the choice of (1) operating certain obtainable junctions to the 300C level, (2) reverse-biasing obtainable junctions at a high oven temperature or (3) operating the circuit in some dynamic condition at high temperature, may be a difficult one to make without some degree of evaluation. Even at high temperature and reverse bias, the high leakage currents developed at high temperature could change the circuit condition into some different operating mode, losing the value of the intended reverse bias. Hence, measurements of the integrated circuit characteristics with increasing temperature are necessary in order to determine the maximum stress which is appropriate.

5. I would assume that our past experience with specifications of this type would be of technical value to NASA, although we recognize that we have looked at a relatively small portion of the parts of interest. The legal question of utilization of our past experiences to minimize NASA testing should, I believe, be taken up with the Western Electric Company, 195 Broadway, New York City, and I am told that an appropriate contact by NASA could be through Mr. D. Allen, Manager of Government Communications Contracting.
6. It is difficult to foresee if there is any particular method of implementing high-stress screening to be most beneficial mutually to Bell Telephone Laboratories and NASA. I would presume, for example, we would not necessarily be interested in the same list of part types. Perhaps this question could be discussed more completely if NASA wishes to explore with Western Electric any further details regarding what assistance we could provide.

Mr. R. A. Homan - 4

I hope that these above comments provide the answers you are looking for, at least for the immediate present. You are probably aware that I have published information regarding the handling of test data from high-stress screening, the extrapolation to normal application stresses and evaluation of the expected failure rate. Such information, of course, is readily available to NASA. I would hope that our long experience with this kind of treatment could be of benefit to the space program.

Very truly yours,

A handwritten signature in cursive script, appearing to read "D. Stewart Peck".

D. Stewart Peck
Head
Transistors, Electron Tubes
and Device Reliability
Department

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V. INDUSTRY SURVEY OF ELECTRONIC PART DERATING PRACTICES

by R. A. Homan

CONTENTS

	<u>Page</u>
V. INDUSTRY SURVEY OF ELECTRONIC PART DERATING PRACTICES . .	V-1
A. INTRODUCTION	V-1
B. DERATING PRACTICES	V-3
C. DERATING GUIDELINES, ELECTRONIC PARTS	V-18
1. Introduction	V-18
2. Purpose	V-18
3. Derating Guideline Factors	V-18
D. DESIGN PRACTICE GUIDELINES	V-25
1. Worst Case Analysis	V-25
2. Test Points	V-26
3. Transient and Power Sequence Protection	V-26
4. Grounding	V-26
5. Shielding and Isolation	V-26
6. Analog Circuit Design	V-27
7. Pulse, Logic, and Low Level Switching Circuit Design . .	V-29
8. Power Switching Circuit Design	V-33
9. Power Supplies	V-34
10. Capacitors	V-34
11. Resistors	V-35
12. Transistors	V-36
13. Diodes	V-37
14. Transformers	V-37
15. Relays	V-38
E. REFERENCES	V-40

Figure

1 Capacitor Derating	V-12
2 Diode Derating	V-13
3 Microcircuit Derating	V-14
4 Relay and Switch Derating	V-15
5 Resistor Derating	V-16
6 Transistor Derating	V-17

Table

1	Capacitor Derating	V-5
2	Diode Derating	V-7
3	Microcircuit Derating	V-8
4	Relay and Switch Derating	V-9
5	Resistor Derating	V-10
6	Transistor Derating	V-11

V. INDUSTRY SURVEY OF ELECTRONIC PART DERATING PRACTICES

A. INTRODUCTION

It is generally recognized, in accordance with the laws of chemical and physical degradation, that increasing the electrical, thermal, and mechanical stresses on electronic parts will decrease either the time to failure or the time required to accumulate a given amount of degradation. Conversely, decreasing these stresses will prolong the time to achieve degradation, reduce the probability of catastrophic failure, and thus improve reliability. Derating is defined as the practice of limiting these stresses on electronic parts to levels well within their specified or proven capabilities, in order to enhance reliability. The need to derate parts in application is clearly established (Reference 1). Even the best parts when operated at maximum rated stress levels do not have low enough failure rates for highly reliable complex systems. A major contributing factor in the success of many space programs has been a conservative design approach incorporating substantial derating of parts (Reference 2).

Reliability prediction models such as those contained in Reference 3 recognize the effect of stress and environment on reliability. Once reliability requirements are established, the maximum stress level can be determined from curves of reliability versus stress. A dilemma exists, however, when such curves are established by past history and applied to new parts. As parts are improved, the curves will become conservative. As pointed out in Reference 1, curves of reliability versus stress are generally not well-proven. Historical information based on field data obtained from various equipments operating under conditions similar to those of interest must be used. In this chapter, twelve derating policies used on various space programs are reviewed and compared. From this review, a composite derating is derived for each electronic part investigated and is presented as a recommended guideline.

Derating will compensate for variability of part longevity among parts which comprise a purchased lot. It provides a margin of safety should questionable devices survive incoming inspection and screening tests (Reference 2). It also provides added protection from system anomalies unforeseen by the designer (Reference 4).

Although the time to achieve a given level of degradation is prolonged, failure rates in applications will vary widely depending on the tolerance of each circuit to part drift. To assure low failure rates, the designer should strive to achieve the greatest possible circuit tolerance (Reference 1). Therefore, in addition to derating guidelines, application notes similar to those provided in References 5 and 6 are also listed herein as recommended guidelines for each part type.

B. DERATING PRACTICES

In some respects, derating practices are somewhat subjective in that either the manufacturers' ratings or the users' procurement specification ratings are used as the basis from which to derate. The published ratings always contain margins of safety. These margins are within the limiting values of stress conditions which will result in permanent impairment of the serviceability of individual parts. The safety margin of a part to a given stress is a function of the manufacturers' design as well as the uniformity and repeatability of his production. It is expected, therefore, that these margins will not only vary considerably between part numbers of a given part type, but will vary between interchangeable parts supplied by different manufacturers. In general, these margins, related to the ultimate capabilities of the parts are unknown. Derating of specification values results in variations of the true safety margin in an application, depending on the conservativeness of part design and manufacturers' production uniformity. Although the actual safety margin of each part to both threshold and time dependent stresses is generally unknown, they will be increased by derating. It behooves the user, lacking knowledge of these margins, to derate to the *maximum* extent possible.

It would be a formidable task to determine the margins existing for each part type from each manufacturer for each specification value. It is also unnecessary, since considerable experience with successful derating practices is available to serve as a guide. *Using this experience to establish a minimum derating policy, and advocating further derating where feasible, is the approach taken herein.* Derating practices utilized by the following agencies or programs are reviewed:

- 1) Ames Research Center (Pioneer)
- 2) TRW (Pioneer, 777, Vela)
- 3) Philco-Ford (ATS)
- 4) Philco-Ford (Skynet)
- 5) Martin Marietta (Skylab)
- 6) Motorola (SGLS Transponder)
- 7) Jet Propulsion Laboratory (Mariner)
- 8) George C. Marshall Space Flight Center (Shuttle)

- 9) Manned Spacecraft Center (Skylab)
- 10) Grumman (Spacecraft Policy)
- 11) Goddard Space Flight Center (PPL 11)
- 12) Hughes (Intelsat)

Summaries of these practices are shown for the various part types in Tables 1 through 6. The values shown for Hughes Aircraft Company are typical for their spacecraft usage and an ambient temperature of 0°C. Their general practice is to derate in accordance with the reliability prediction models of Reference 3. The required failure rate to meet a reliability goal in the usage environment determines the various quality and stress factors (as required by the model) that must be utilized for each part. The stresses thus identified are maximum permissible values and do not preclude further derating. For example, higher ambient temperatures would require further derating of low power and switching transistors; the power dissipation typically following a curve to zero at 55°C.

The information in Tables 1 through 6 is presented in scatter diagram form in Figures 1 through 6 for critical parameters of each part type. It is obvious from these figures that the most stringent approach to derating was generally taken by Philco-Ford on ATS and SKYNET. However, their approach has since been relaxed somewhat in more recent proposals, which shifts their values closer to the center of gravity of the scatter diagrams.

The derating guidelines included in Reference 4 are a composite of the derating policies employed by the Jet Propulsion Laboratory, Grumman Aircraft Corporation, Manned Spacecraft Center, Goddard Space Flight Center, and Marshall Space Flight Center. From Figures 1 through 6, it is seen that these composite values are close to the average or on the conservative side of the scatter. It is recommended that these values be used as guidelines for minimum derating of parts and that further derating be used whenever possible. These guidelines, for the parts included in this study, are included in Section C of this report.

Table 1 Capacitor Operating

	Ames	TRW	Philco ATS	Philco Skynet	Martin	Motorola	JPL	MSFC	MSC	Grumman	GSFC	Hughes
Ceramic					50% V	50% V		50% V, 70% I	70% V, 70% I	50% V	50% V, T _A (Max) = 85°C	40% V T _A = 0°C 0% V T _A = 42°C
Ceramic Disc (~1000 Volts)	70% V						70% V					
Ceramic (Low Voltage)				10% V								
Ceramic Disc (~1000 Volts)	50% V						50% V					
Ceramic (High Voltage)				60% V								
Low Voltage Cer- amic (<0.1uf)	70% V						70% V					
Low Voltage Cer- amic (<0.1uf)	60% V						60% V					
Glass	60% V				75% V	50% V	CYFR10 & 15, 70% V CYFR20 & 30, 60% V	50% V, 70% I	90% V, 70% I	50% V	50% V, T _A (Max) = 85°C	
Porcelain	70% V						70% V	50% V, 70% I			50% V, T _A (Max) = 85°C	
Mica (Low Voltage)				10% V								
Mica (<1.0 kv.)	70% V						70% V					
Mica (High Voltage)				60% V								
Mica (>1.0 kv.)	50% V						50% V					
Mica, Dipped						50% V		60% V, 70% I			60% V, T _A (Max) = 85°C	
Mica, Molded						35% V					40% V, T _A (Max) = 85°C	
Mica									90% V, 70% I	70% V		
Tantalum Solid				30% V	75% V	3 Ω/V = 60% V 0.1 Ω/V = 40% V		50% V, 70% I T _A (Max.) = 50°C Use 3 Ω/V Res.	0-35 V, 70% V, 70% I 35-50 V, 65% V, 70% I 50-75 V, 60% V, 70% I	0-15 V, 80% V 15-35 V, 70% V 35-50 V, 65% V 50-75 V, 60% V	3 Ω/V, 60% V, T _A (Max) = 85°C 0.1 Ω/V, 40% V, T _A (Max) = 50°C	34% V, T _A = 0°C 30% V, T _A = 60°C 0% V, T _A = 90°C
Tantalum, Solid 18 & 22uf, 50V 39 & 47uf, 35V 82 & 100uf, 20V All Others	50% V 70% V						50% V					
Tantalum, Wet Slug	75% V				75% V	70% V, T _A (Max) = 70°C	70% V	50% V, 70% I T _A (Max.) = 70°C		70% V	70% V, T _A (Max) = 70°C	
Tantalum, Foil			50% V	40% V	50% V	70% V, T _A (Max) = 70°C	70% V	50% V, 70% I T _A (Max.) = 70°C	70% V, 70% I		70% V T _A (Max) 70°C	
Variable, Air				10% V				30% V, 70% I	30% V, 70% I	30% V		
Variable, Glass									50% V, 70% I	50% V		
Variable, Ceramic									50% V, 70% I	50% V		
Paper					50% V	50% V	80% V	50% V, 70% I			50% V, T _A (Max) = 85°C	
Mylar				60% V		45% V					60% V, T _A (Max) = 85°C	

Table 1 Capacitor Derating (concl.)

	Ames	TRW	Philco ATS	Philco Skynet	Martin	Motorola	JPL	MSFC	MSC	Grumman	GSFC	Hughes
Plastic Film								50% V, 70% I	90% V, 70% I	50% V		
Plastic Film ($<1.0\mu\text{f}$)							70% V					
Plastic Film ($>1.0\mu\text{f}$)							50% V					
Metallized Film ($<1.0\text{ f}$)							60% V					
Metallized Film ($>1.0\text{ f}$)							50% V					
Film Types					50% V							
All Others			50% V		75% Surge Volt. 200% Leak- age I							

Table 2. Measurement Matrix

	Ames	IRW	Philco ATS	Philco Skynet	Martin	Motorola	JPL	MSFC	NSC	Grumman	CSFC	Hughes	
Digital Integrated Circuits		80% Fanout	90% Fanout		1. 70% Fanout 2. T_j Max = 130°C	1. AC Fanout 60% 2. DC Fanout 60% 3. AC & DC Fanout, 60% AC Load, 40% DC Load, Series Con- nection of Logic Gates 80% Max.		1. 80% Out 2. 75% Oper- ating Fre- quency 3. T_j Max. = 85°C	1. V_{pk} = 60% 2. V_{pk} = 75% 3. V_{surge} = 90% 4. I_{pk} = 75%	75% Fanout I	1. 60% Fanout AC & DC Fan- out, 60% AC Load, 40% DC Load		
Linear Integrated Circuits			100% Supply V; Input, Differen- tial, & Common Mode 80% Max; Input V = 80% Input/Output, in-out Differen- tial = 110%.		1. Gain = 20% 2. Offset Volt. = 0.5mV 3. Output I = 70% Max. 4. P = 90%	Turn on or Off Volt. Tran- sients 95%		70% Bias volt., 70% Input Sig- nal volt., 75% Oper., Freq., I Max = 85°C	1. V_{pk} = 60% 2. V_{pk} = 75% 3. V_{surge} = 90% 4. I_{pk} = 75%	output Volt. Swing 75%			
All Inte- grated Circuits							1. Reduce Supply Volt. to Ef- fect Lower Power at Price of Speed and Narrower Noise Immunity Mar- gins. 2. 75% Fanout 3. Operate over Narrow Temp. Range 4. 60% Power						

Table 4 Relay and Switch Denating

	Ames	TRW	Philco ATS	Philco Skynet	Martin	Motorola	JPL	MSFC	MSC	Grumman	GSFC	Hughes
Resistive Load						50% Rated Current	80% Rated Current	75% Rated Resistive Current		80% Rated Current	50% Rated Current	
Capacitive Load						50% Rated Current	80% Rated Current	75% Rated Resistive Current		80% Rated Current	50% Rated Current	
Inovltive Load						50% Rated Current	80% Rated Current	40% Rated Resistive Current		80% Rated Current	50% Rated Current	
Motor Load						50% Rated Current	80% Rated Current	20% Rated Resistive Current		80% Rated Current	50% Rated Current	
Lamp Load						50% Rated Current	80% Rated Current	10% Rated Resistive Current		80% Rated Current	50% Rated Current	
Notes							<ol style="list-style-type: none"> 1. Applies to Load Current at Rated Load Voltage. 2. Coil Voltage and Current should be Rated Values 					

Table 6 Resistor Summary

Ames Power	IRW	Philco ATS Per. Volt.	Philco Skynet Power	Martin Per. Volt.	Motorola Power	JPL Power	ISFC Per Volt	ISC P V i	Crucial Per Volt.	GSFC Per. Volt.	Hughes Power
70%				50% 80%	50%	50% $T_A > 50^\circ C$ 70% $T_A < 50^\circ C$	50%	50% 80% 75%	30% 80%	50%	70% ($T_A = 0^\circ C$)
40%				50% 80%	50%	50% $T_A > 70^\circ C$ 100% $T_A > 70^\circ C$	50%	50% 80% 75%	C. P. 30% 80% 1% Tol. 30% 80% 3% Tol. 35% 80% 4% Tol. 20% 80%	50%	70% ($T_A = 15^\circ C$) 7% ($T_A = 120^\circ C$)
50%			5%	50% 80%	50%		50%	50% 80% 75%		90% (Chassis Mount) 50% (RoR)	
40%				50% 80%	15%	50%		50% 80% 75%		25%	
					25%						
					25%					25%	
					25%						
					33%				20% 80%		
					50%					35% 80% 35% 80%	
					50%					50%	
								80% 75%	Current = 70%	50%	
		25% 50%	20%	70%							
Notes											

1. Max. Volt. = 80%
2. Derate Stacked Resistors Further
3. Vertical, 80%
4. Horizontal, 60%
5. Nickel Leaded Composition Res. Derate Add'l 50%

Table 2. Transistor Ratings

Ames	TRK V	Gain	Philco ATS P V I	Philco Skyvet P	Martin	Motorola	JPL P V I	MSFC P V I	MSC V _{Max} V _p V _{Surge} I	Graham P V I	GNFC P	Busnes P V
Small Signal General Purpose Low Power and Switching	75%	75%		10%				90% 75% 75% 50% 75% 75%	60% 75% 90% 75% 60% 75% 90% 75%		20% 20%	35-70% (T _A = 0°C) 0% 30% (T _A = 55°C)
High Power NPN Power	65%	80%		25%				30% 75% 75%	60% 75% 90% 75% 60% 75% 90% 75%		15%	
R.F. Power Unijunction All Others			25% 25% 25%		1. 70% Voltage 2. 80% Current 3. 50% Power 4. 200% Leakage 5. 15% Min. BC Gain 6. 120% Switch 7. T _j Max. = 130°C	1. T _j Max = 110°C 2. 75% Voltage	50% 75% 50%		60% 75% 90% 75% 60% 75% 90% 75%	90% 75% 75%	20%	
Notes		T _j Max = 125°C					1. T _j Max = 110°C Except for Power Transistor 2. I _{Max} = 300mA For 1 mil Alum Wire	T _j Max = 110°C	T _j Max = 110°C		1. T _j Max = 110°C 2. 75% Voltage	

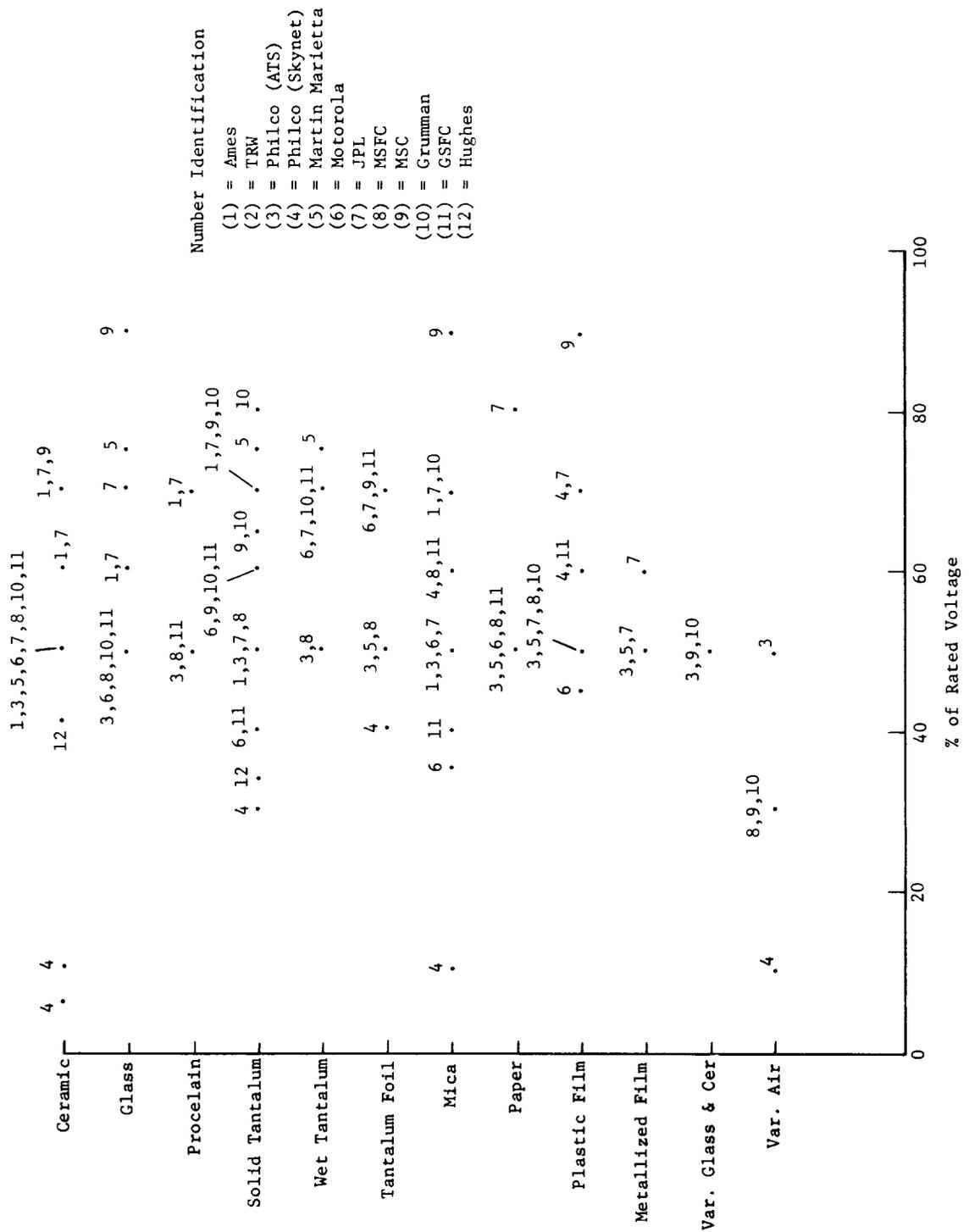
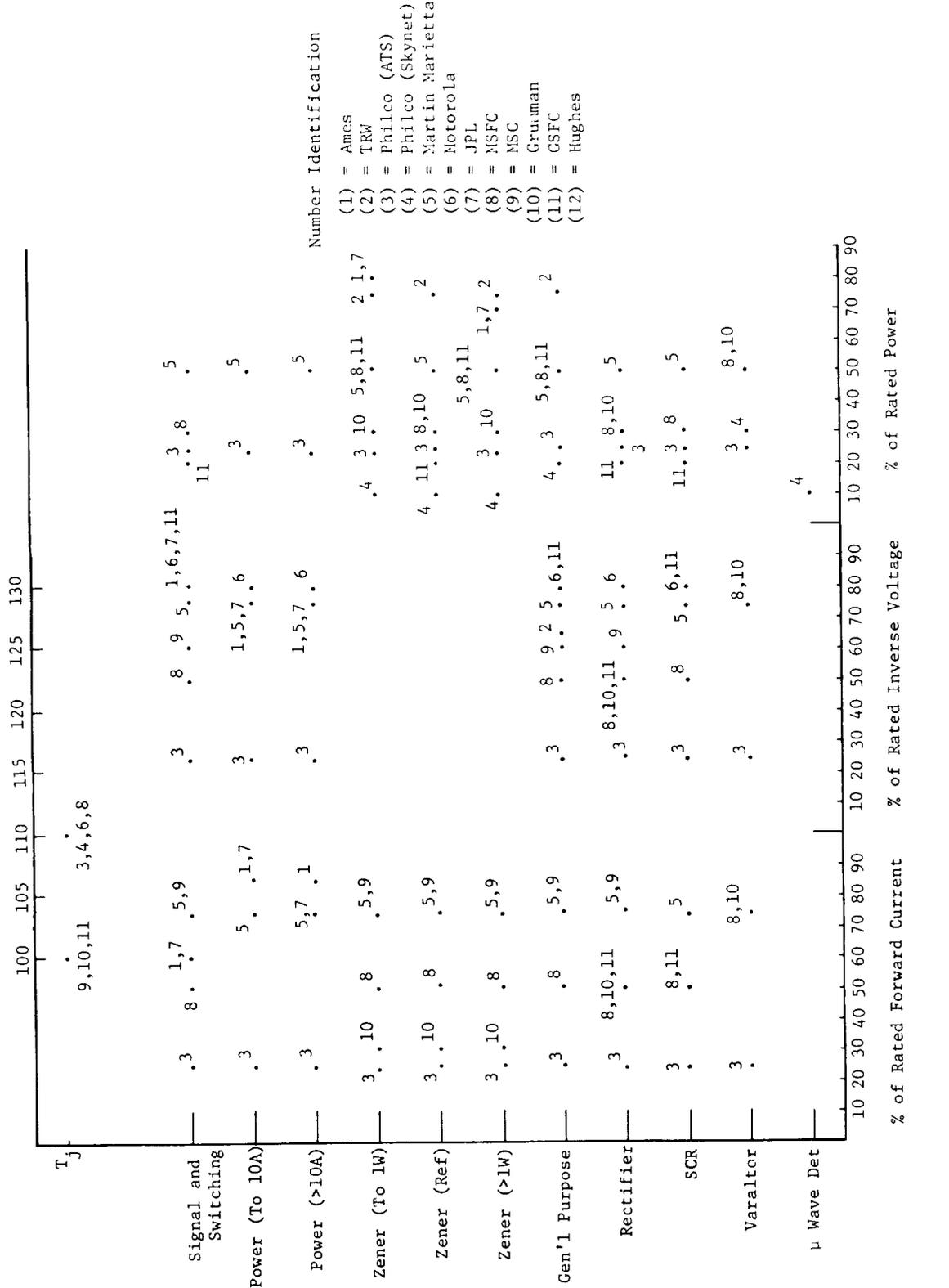


Figure 1 Capacitor Denatation



Number Identification
 (1) = Ames
 (2) = TRW
 (3) = Philco (ATS)
 (4) = Philco (Skynet)
 (5) = Martin Marietta
 (6) = Motorola
 (7) = JPL
 (8) = NSFC
 (9) = MSC
 (10) = Gruman
 (11) = GSFC
 (12) = Hughes

Figure 2 Diode Derating

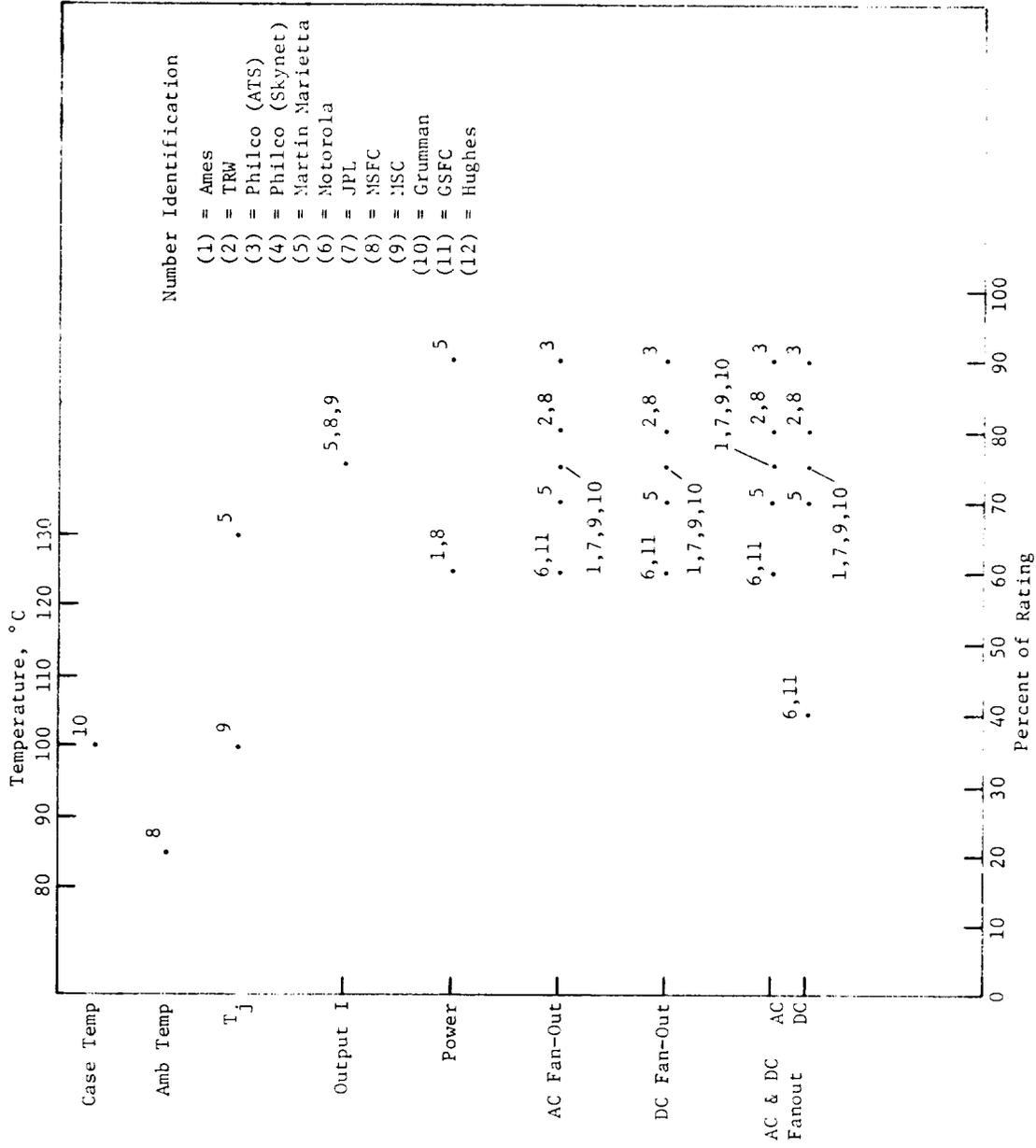


Figure 2 Microcircuit Derating

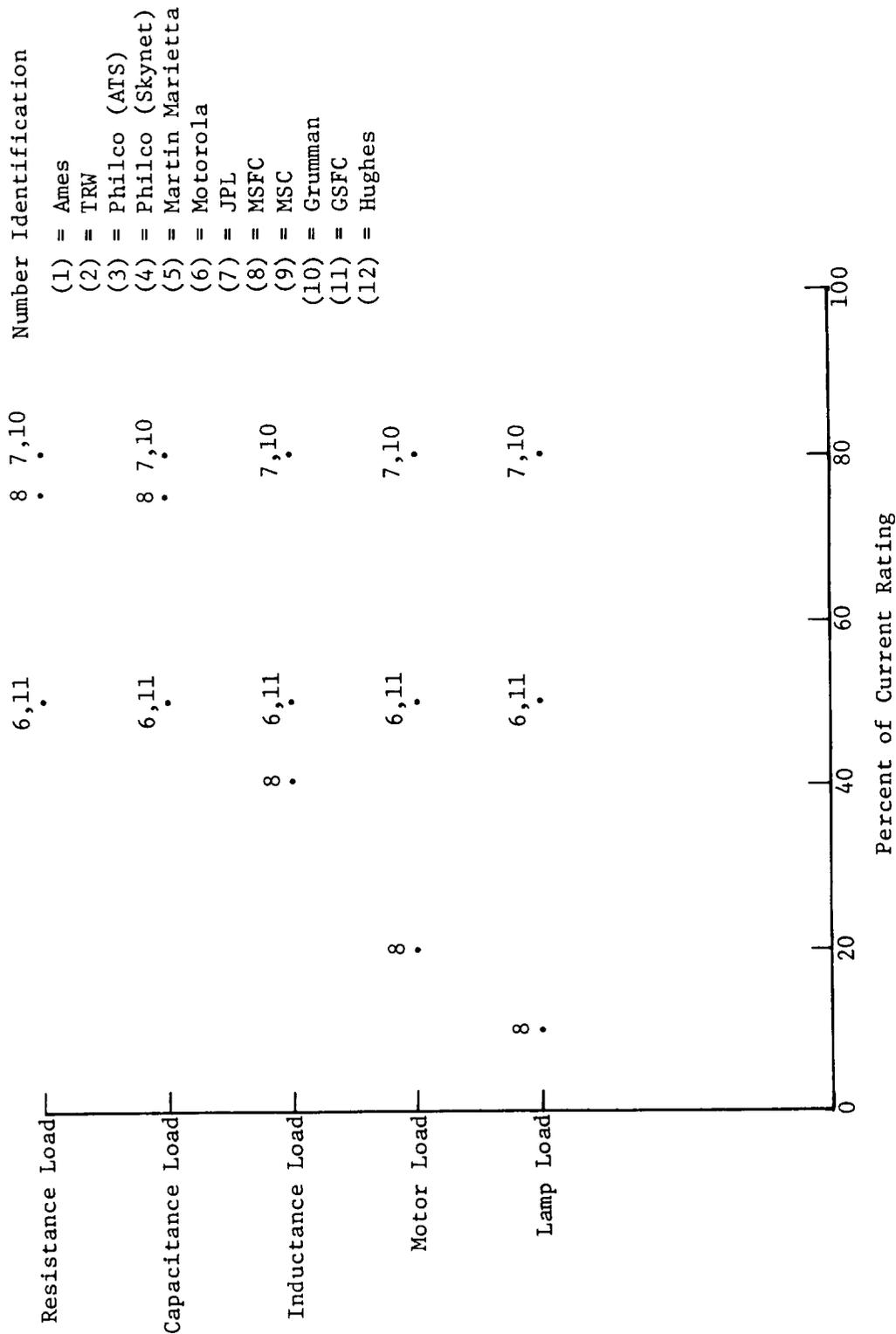


Figure 4 Relay and Switch Derating

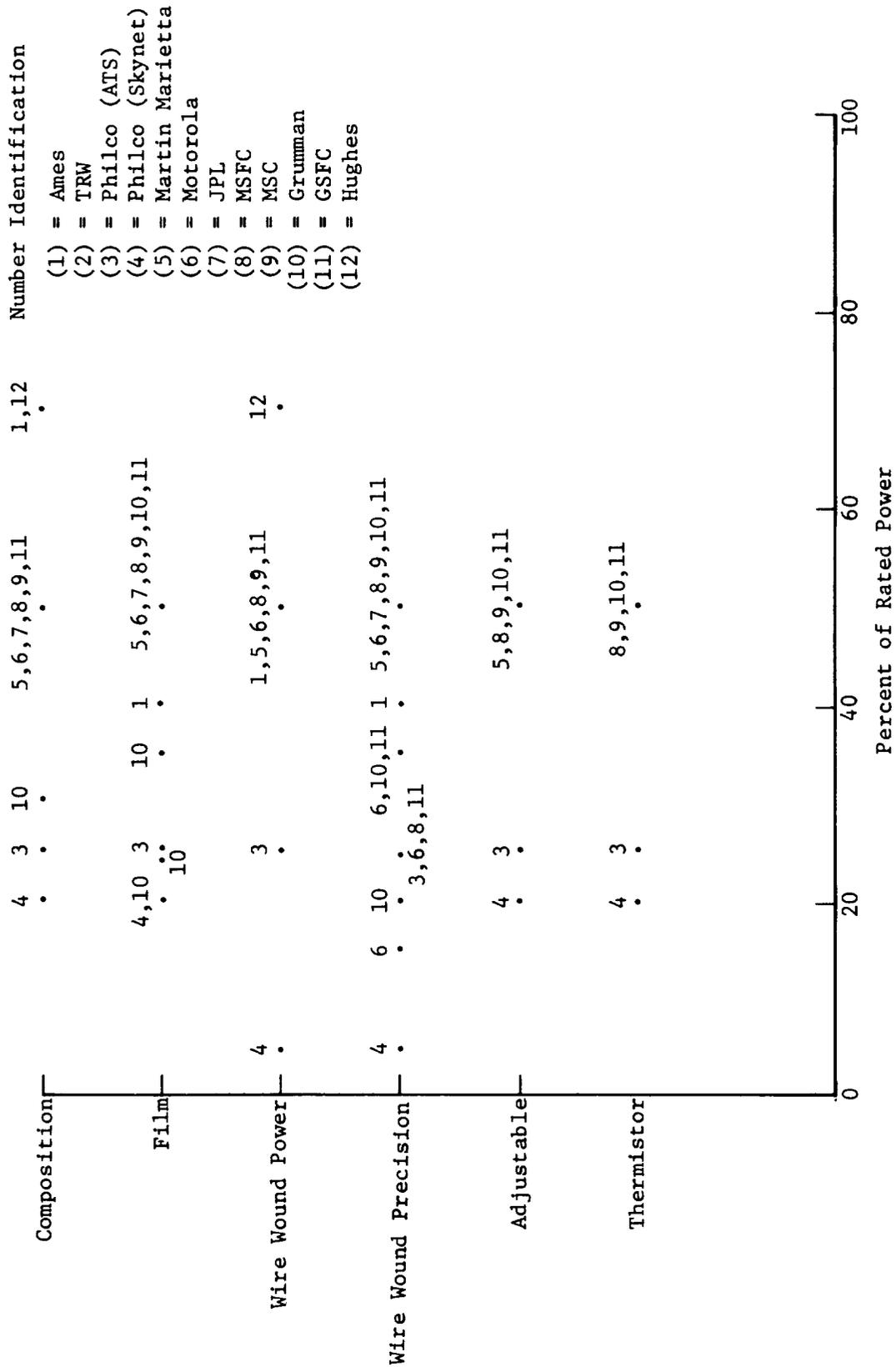


Figure 5 Resistor Derating

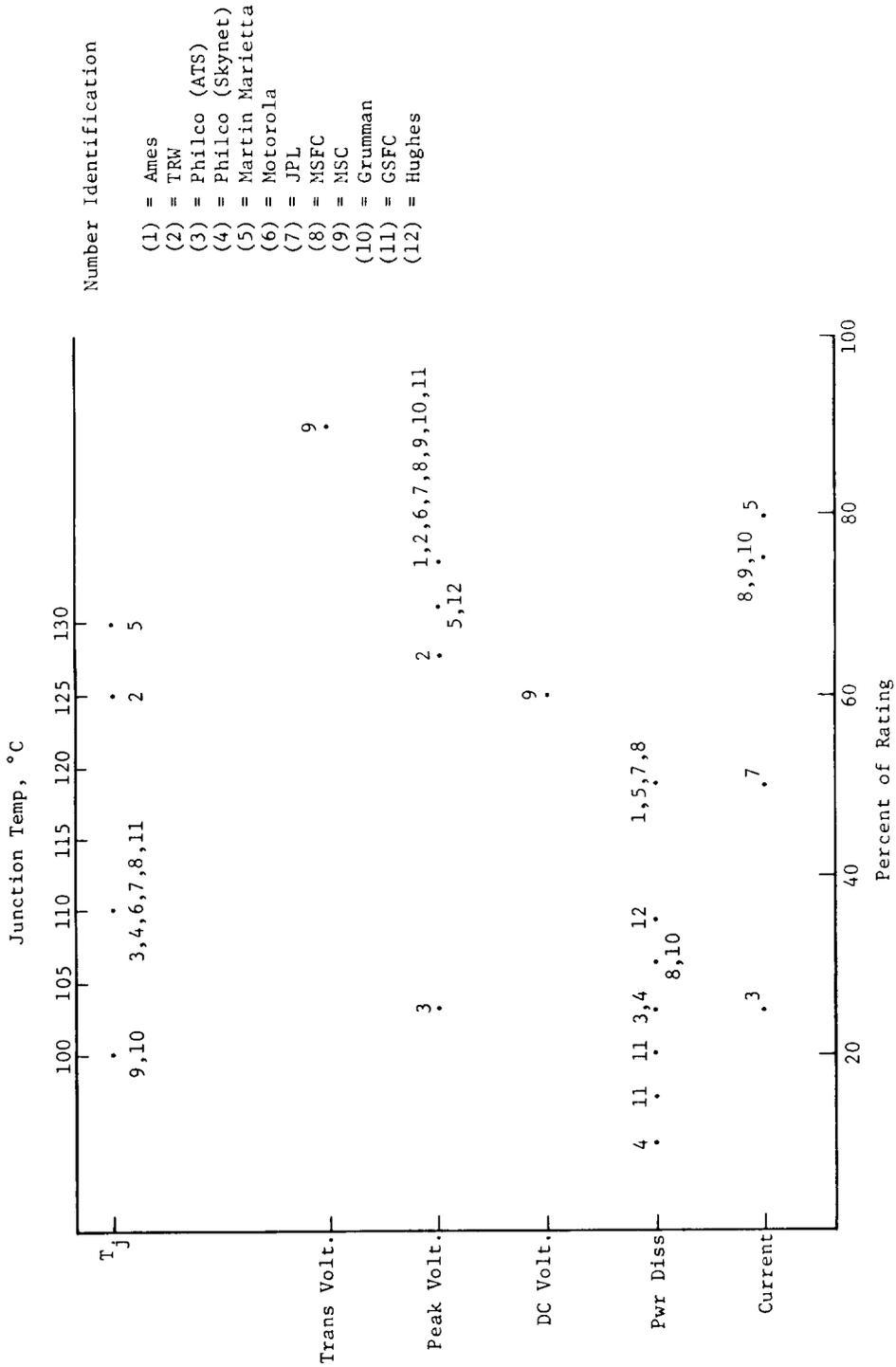


Figure 6 Transistor Denaturation

C. DERATING GUIDELINES, ELECTRONIC PARTS

1. Introduction

The following guidelines give basic information for the derating of parts. The guidelines are a composite of the derating policies employed by the Jet Propulsion Laboratory, Grumman Aircraft Corporation, Manned Spacecraft Center, Goddard Space Flight Center, and Marshall Space Flight Center as presented in Reference 4. The specified derating percentages and applicable notes will assist the designer in obtaining reliable operation of parts. It must be emphasized that the user should evaluate all parts to the requirements of his applications, since he is responsible for assuring that adequate deratings are accomplished. The recommended derating factors are based on the best information currently available.

2. Purpose

Derating is the reduction of electrical, thermal, and mechanical stresses on a part to decrease the degradation rate and prolong the expected life of the part. By derating, the margin of safety between the operating stress level and the actual failure level for the part is increased, providing added protection from system anomalies unforeseen by the designer.

3. Derating Guideline Factors

The following derating factors indicate the maximum recommended stress values and do not preclude further derating. When derating, the designer must (1) take into account the specification environmental and operating condition rating factors, (2) consider the actual environmental and operating conditions of the application, and then (3) apply the recommended derating factor contained herein. Parts not appearing in these guidelines are lacking in empirical data and failure history. Since the operating characteristics for such parts cannot be guaranteed, it is a good policy to derate generously to provide an additional margin of safety. Where parts are listed, but are not given a specific derating value, a good general practice should also be to derate generously.

a. *Capacitors* - Derating guideline factors for capacitors are tabulated below.

<u>Type</u>	<u>Derating Factor</u>	<u>Parameter</u>	<u>Applicable Notes</u>
<u>Fixed</u>			
Ceramic	.50	voltage	1, 2
Mica Dipped	.60	voltage	1, 2
Glass	.50	voltage	1, 2
Porcelain	.50	voltage	1, 2
Paper	.50	voltage	1, 2
Plastic	.50	voltage	1, 2
Tantalum			
Foil	.50	voltage	1, 2, 4
Wet Slug (Hermetic)	.50	voltage	1, 2, 4
Solid (3 ohms/volt limiting resistor)	.50	voltage	1, 2, 3
<u>Adjustable</u>			
Air	.30	voltage	1, 2
Ceramic	.50	voltage	1, 2
Glass	.50	voltage	1, 2

NOTES:

1. The current derating factor is 70 percent of manufacturer's specified limit.
2. Manufacturer's derating factors shall be applied before using the factors of this document.
3. Ambient temperature shall not exceed 50°C.
4. Ambient temperature shall not exceed 70°C.

b. *Diodes* - Derating guideline factors for diodes are tabulated below.

<u>Type</u>	<u>Derating Factor</u>	<u>Parameter</u>	<u>Applicable Notes</u>
General purpose	.50	Power	1
	.50	PIV	
	.50	Surge current	
	.50	Forward current	
Rectifier	.30	Power	1
	.50	PIV	
	.50	Surge current	
	.50	Forward current	
Switching	.30	Power	1
	.50	PIV	
	.50	Surge current	
	.50	Forward current	
SCR	.30	Power	1
	.50	PIV	
	.50	Surge current	
	.50	Forward current	
Varactor	.50	Power	1
	.75	PIV	
	.75	Forward current	
Zener	.50	Power	1, 2
	.50	Forward current	
	(2)	Zener current	
Reference	.30	Power	1, 2
	.50	Forward current	
	(2)	Zener current	

NOTES:

1. Junction temperatures for all diodes shall not exceed 110°C.
2. Zener current should be limited to no more than

$$I_Z = .5 \left(I_{Z_{\max}} + I_{Z_{\text{nom}}} \right)$$

c. *Microcircuits* - Derating guideline factors for microcircuits are tabulated below.

<u>Type</u>	<u>Derating Factor</u>	<u>Parameter</u>	<u>Applicable Notes</u>
Digital	.80	Output current Operating frequency	1, 2
	.75		
Linear	.70	Bias voltage	1
	.70	Input signal voltage	
	.75	Output current	
	.75	Operating frequency	
Voltage	.80	Input voltage (rated maximum)	1
	.75	Output current (rated maximum)	
	.60	Power dissipation (rated maximum)	

NOTES:

1. All microcircuits shall be used at ambient temperatures less than 85°C.
2. This derating factor is not to be used when fan out would be reduced to less than one.

d. *Relays and Switches* - Derating guideline factors for relays and switches are tabulated below.

<u>Type of Load</u>	<u>Derating Factor</u>	<u>Parameter</u>	<u>Applicable Notes</u>
Capacitive	.75	Contact current	1
Resistive	.75	Contact current	
Inductive	.40	Contact current	
Motor	.20	Contact current	
Filament	.10	Contact current	

Note:

1. Capacitive peak in rush current should not exceed the derated limit.

e. *Resistors* - Derating guideline factors for resistors are tabulated below:

<u>Type</u>	<u>Derating Factor</u>	<u>Parameter</u>	<u>Applicable Notes</u>
<u>Fixed</u>			
Carbon Composition	.50	Power	1, 2
Insulated Film	.50	Power	1, 2
Wirewound, Precision			
1.0%	.50	Power	1, 2
0.1%	.25	Power	1, 2
Wire wound, Power	.50	Power	1, 2
Thermistor	.50	Power	1, 2, 3
<u>Adjustable</u>			
Wirewound	.70	Rated Current	1, 2, 4
Nonwirewound	.70	Rated Current	1, 2, 4

NOTES:

1. The maximum voltage for all resistors shall be no more than 80% of the MIL-ratings.
2. High density packaging may require further derating if ambient temperatures are increased.
3. Thermistors used in other than zero power applications should also have minimum wattage specified for the application.
4. Rated current is defined as:

$$I_R = \sqrt{\frac{P_{\max}}{R_{\max}}}$$

and by limiting the current to .70 rated current, power is limited to .5 maximum power.

f. *Transistors* - Derating guideline factors for transistors are tabulated below:

<u>Type</u>	<u>Derating Factor</u>	<u>Parameter</u>	<u>Applicable Notes</u>
General Purpose	.50	power	1, 2
	.75	current	
	.75	voltage	
Power	.30	power	1, 2
	.75	current	
	.75	voltage	
Switching	.50	power	1, 2
	.75	current	
	.75	voltage	

NOTES:

1. Junction temperatures for all transistors shall not exceed 110°C for any combination of parameters.
2. Worst-case combination of dc, ac, and transient voltages shall be no greater than the derated limit.

D. DESIGN PRACTICE GUIDELINES

Part derating is one aspect of a conservative design approach to improve reliability. Although it provides increased safety margins, reduces the probability of catastrophic failure, and increases the time to achieve degradation levels, each particular circuit will have a different tolerance to part drift which is a function of lifetime, complexity, application, and failure criticality. The user must consider all aspects of his application and utilize all additional practices which will tolerate degradation and enhance success. Included in this section are some design practice guidelines which are recommended for use in conjunction with derating guidelines to achieve reliable circuit design.

1. Worst Case Analysis

A worst case analysis should be performed concurrently with the design, beginning in the early stages of development. The analysis should consist of a circuit description with schematic, a summary, a functional analysis, a stress analysis, and test results. The summary should include both a tabulation of all functional requirements versus the functional capabilities, and a tabulation of part applied stress levels versus the derated stress limits. No deviations from requirements or deratings should be allowed without justification, review, and approval. The functional analysis is performed to assure the circuit has the capability to satisfy all functional requirements within the required performance and safety margins, under the most unfavorable combination of realizable conditions. Included are input, output, environmental, and packaging conditions, as well as part parameter dispersions including aging and life tolerances. Suitable computer programs (ECAP, SCEPTRE, TRAC) should be used to the maximum extent for efficiency and reliability of design. The input program and output data should be included in the report. The worst case stress analysis should verify proper application of parts such that the applied stresses do not exceed the derated values of voltages, currents, power dissipation, etc. under worst case conditions. Worst-case conditions include power-up and power-down under all phases of circuit operation including manufacturing and system/subsystem test. The results of tests performed to insure satisfaction of performance requirements and existence of required margins should be included in support of the analysis.

2. Test Points

A sufficient number of protected test points should be provided to facilitate checkout and troubleshooting. As a minimum, redundant circuits require unambiguous checkout provisions to verify full operation at the component acceptance test level. Protection of test points should be provided to insure: (1) system operation will not be impaired by normal functioning test equipment, and (2) degradation will not result from short circuits between the test point and ground, power, or adjacent test points. This may be accomplished by use of either protective parts within the assembly or by protective circuitry within external test equipment.

3. Transient and Power Sequence Protection

Turn-on and turn-off transient protection should be provided to prevent damage from inductive kick-back or high capacitive charging currents. The circuit should be designed or otherwise protected so as not to be damaged from any sequence of power application or removal. In addition, no erroneous output conditions should be created in critical functions from power application or removal.

4. Grounding

The single point ground approach should be used to the maximum extent possible to minimize common impedances between circuits. This is accomplished by selective grouping of individual circuit returns prior to returning to the component grounds. Typical groupings are: AC power returns, DC power returns, returns for signals below 50 KHz, and returns for signals above 50 KHz. All ground conductors should be chosen for minimum length and maximum practical cross sectional area to minimize inductance and resistance. This also applies to printed wiring, especially when the interconnected circuits have rise and fall times of less than 10 microseconds. Ground planes are to be considered where minimum ground return inductance is necessary.

5. Shielding and Isolation

Shielding and isolation should be used within the assembly to control signal environments and thereby minimize cross-coupling. Separable noise generating functions within the assembly such as DC/DC converters and switching type pre-regulators should be in electrostatic enclosures wherever possible.

6. Analog Circuit Design

Amplifiers and any combination of feedback loops and function generators should individually and collectively conform to the following paragraphs.

a. Operating Point - Operating or bias point should be selected such that the following functional requirements are satisfied:

Full scale input and output range;

Input impedance;

Output impedance;

Common mode range and rejection level;

Noise level;

Gain and phase limits;

Linearity and/or distortion;

Offset limits.

b. Feedback - In addition to providing the required closed loop transfer function and the required closed loop parameter control, open loop characteristics should also be determined to insure stability. Open loop gain and phase determination should include the effects of input source impedance, output load impedance, and any significant interconnecting cable or wiring reactance.

c. Negative Feedback - The gain and phase margins of the loop should be such that transient overshoot and ringing requirements are met. In no case, however, should the phase margin at unit gain crossover be less than 30° nor should the gain margin at 180° phase shift be less than 10 dB.

d. Non-saturating Positive Feedback - This type of feedback loop is most commonly used in sine wave oscillator circuits and requires adequate phase shift control in the positive feedback loop to meet the required frequency tolerance. Gain control should be provided to maintain loop gain of unity over the oscillation period. The subsidiary loop maintaining unity gain around

the positive feedback loop should comply with the gain and phase margins of paragraph 6c. Greater than unity gain should be provided in the positive feedback loop following power-up to insure self starting.

e. Relaxation Feedback - This type of feedback loop incorporates reactive components and is typified by the astable multivibrator. The circuit should be biased for a non-oscillating positive loop gain greater than unity to guarantee self starting. The minimum value of oscillating loop gain selected should be sufficient to meet the rise and/or fall time requirements of the output waveform. The total positive feedback loop should be demonstrated to meet the accuracy requirements for output frequency control.

f. Stable (D.C. Regenerative) Feedback - This type of positive feedback should be used in analog comparator and power switching to improve a known hysteresis level. The loop gain in the switching or transition region should be sufficient to meet the threshold and speed requirements. Hysteresis level should be a minimum of 1% as referred to the signal threshold level in order to reduce the susceptibility to high frequency oscillations and noise when operated at the critical input threshold point. Wherever system requirements permit, larger percentages of hysteresis should be used.

g. Decoupling - Decoupling should be provided to eliminate unwanted feedback loops and to prevent conducted noise from being transferred to sensitive areas.

h. Decoupling of Discrete Circuits - Cascaded circuit stages should have power line decoupling by sections having gains no higher than 200 per section. The decoupling must be effective from the lowest frequency of concern to at least two octaves above the open loop unity gain crossing of the circuit being decoupled. Determination of network effectivity at high frequencies must include the reactive effects of the applied parts and interconnections.

i. Decoupling of Integrated Circuits - Integrated circuits normally contain inter-stage isolation and are insensitive to low and mid frequency power supply noise. For high frequencies, external decoupling must be provided for each integrated circuit package. As a minimum, decoupling with 0.1 μ f ceramic capacitors from the B+ and B- terminals to signal ground is required.

The effective lead length from the capacitor to the B+ and B- of the integrated circuit terminals and the ground terminal must be kept to a minimum.

j. Bandwidth Limitation Requirement - Bandwidth, rise time, and slew rates should be no greater than that value required to meet input-output performance requirements. Excessive bandwidths and rise times should be limited to reduce noise susceptibility and sensitivity to parasitic oscillations. Excluded from this requirement are integrated circuits where limiting the bandwidth would void the guarantee for required phase margin.

7. Pulse, Logic, and Low Level Switching Circuit Design

Low level bi-level circuits and/or groups of such circuits should conform to the following paragraphs.

a. Functional Verification - All logic systems should be broken into functional blocks, small enough in size, such that a logical verification can be made by using analytical techniques (truth tables, Karnaugh maps, state tables, computer programs, etc.).

b. Fanout Verification - Fanout should never exceed the derated maximum (current or normalized fanout) for the logic part and must be reduced from that level where greater noise immunity or corrections for higher than specified circuit differential temperatures are needed. Fanout utilization for each logic part must be tabulated.

c. Timing Verification - Timing studies must be made for every logic component. All circuits should operate within the specified minimum and maximum propagation delay limits. Factors which should be used in determining timing margins are the specified logic part delay including capacitive loading effects, through delay of counter gating, the effect of clock skew, and the effect of time delay.

d. Time and Data Correlation - All systems requiring time correlation for the logic operation such as flip-flop gating or sequential data handling should be implemented as a synchronous (clocked) system. Any signal received into a synchronous system should have a single point of clocking to prevent logic ambiguities due to skewing effects. The preferred methods for achieving delay or time correlation are clocked counters or delay lines. No race conditions should exist which can cause

an undetermined or erroneous output. In general, multivibrators ("one shots") and capacitors (placed on gate outputs) should not be used for delays or time correlation of logic.

Multivibrators may be used if the following conditions are met: (1) no spurious signals or noise can cause false triggering which would be detrimental to the logic component operation, and (2) detailed timing studies associated with the "one shot" should include the effects of derated external components (R and C), plus a 25% margin on minimum and maximum pulse width and retriggering capability.

Capacitors may be used on gate outputs when the following conditions are met: (1) a current limiting resistor is added to limit the discharge and charge rate of the capacitor, (2) system noise immunity is not degraded, and (3) detailed timing studies show the maximum and minimum pulse delay caused by the capacitor.

e. Counters and Shift Registers - Counters and shift registers should be analyzed to determine the effects on the logic system when an unused state is entered. Provisions should be made to insure that such a logic function cannot either lock up in an unused state or generate a catastrophic function when an unused state is entered. The selection of the counter type should be scrutinized to minimize the total logic required to provide proper decoding and minimum unwanted states.

f. Flip-Flops - The worst case setup and release time for data inputs must be determined for a worst case timing analysis. In general, all data lines must remain stable during the enable portion of the clock, including the rise period and the fall period, to insure against logic ambiguities. In cases where data lines are not stable during the enable portion of the clock, the logic component should be analyzed to determine the overall effect when an ambiguous state is entered. To insure against logic ambiguities, the clock of a flip-flop must be inhibited before the trailing edge of a direct preset or clear pulse. To reduce the coupling of reflected signals into logic circuitry, flip-flops should never be used as line drivers. Unused inputs should be terminated as defined in the part control package. The following flip-flops require special precautions:

- 1) RS flip-flops should be arranged so that both data inputs (R and S) are never high at the same time during an enabled clock thus causing a logically indeterminate condition.

- 2) JK master-slave flip-flops should be arranged so that no transient on an input can cause the "master" portion of the flip-flop to be "set" such that it may be subsequently transferred to the "slave." To avoid this problem the enable duty cycle of the clock should be minimized.

g. Gates - Unused gates or unused inputs of gates should be terminated as specified in the part control package. Increased fan-out capability may be obtained by paralleling gates/buffers of the same package. "Wired-Or" connections impose loading on the output in addition to the normal fanout load. This loading should be included in the loading analysis. "Wired-Or" conditions are not permitted with circuits having a push-pull output stage.

h. Clock Signal Generation and Distribution - The inhibit time duty cycle of the clock should be maximized in order to (1) contain all of the clock triggered switching transients which may cause ambiguous states during decommutating/decoding, and (2) minimize noise susceptibility. The rise and fall times of clocks should be minimized to keep from degrading noise immunity. Shielded or physically separated wiring should be used to distribute clock signals in order to minimize noise coupling into critical signal paths. Clock lines should have protection against negative overshoot. Oscillators should be gate buffered before using as clock signals for flip-flops.

i. Power Up and Power Down Transients - During loss of power at power transfer, circuits which have a memory requirement should be able to maintain the memory capability for a period of 1.25 times the maximum transient specified. Analysis should show that no catastrophic outputs are generated during power up or power down conditions. Logic circuits with separate power supplies or "dormant modes" should be analyzed to determine the effects of power down conditions on logic interface circuits.

j. Logic Compatibility - All logic levels should be compatible. All interfaces of discrete to discrete circuitry, discrete to I.C. circuitry, and I.C.'s of a different family should have both a margin of 10% or .5 volts (whichever is greater) in the high state and 6 dB in the low state when both are referenced to ground and to the receiver logic levels. Logic circuitry must be insensitive to spurious signals, particularly to those generated outside the component. To facilitate this requirement, interface circuits which do not receive information from controlled

impedance transmission lines (i.e., coax, twinax, twisted pair, etc.) should provide means for rejecting or filtering transients. When signals are transmitted over controlled impedance lines, line characteristics such as RC distortion, attenuation, and propagation delays should be determined and their effects used in the worst case analysis.

k. Internal Component Interfaces - When using a common ground for internal interfaces, the following receiver logic level margins are acceptable: either 5% or .3 v (whichever is greater) in the high state and 3 dB in the low state where both states are referenced to ground. A ground plane is mandatory for single wire interconnections greater than 10 inches but not to exceed 20 inches. Twisted pair or coax (with or without ground planes) must be used on interconnections exceeding 20 inches, and they may be used in lieu of ground planes on interconnections less than 20 inches.

l. Component to Component Interfaces - Arrange logic such that interface signals between components use that state (high or low level) which offers the greatest noise immunity for the safe or unarmed condition of that function.

m. Packaging and Decoupling - Self-induced switching transients should be suppressed by adding capacitance to each printed wiring board or module. The total amount of capacitance required is to be calculated to keep B+ and ground line voltage changes at a safe level, cutting into the specified noise margin by no more than 6 dB. It is necessary to use capacitors that are effective at the relatively high frequency present in the switching current spikes. For integrated circuit boards, 0.1 μ f ceramic capacitors should be used for this purpose to optimize both high capacitance per size and good RF properties. Capacitor leads should be held to a minimum length and the required capacitance should be distributed over the PC board or module. The number of capacitors required should be based on the printed-wiring-board-lead inductance existing between the capacitor and the switching elements. This inductance must be determined and minimized to realize the benefit provided by the added capacitors. Additional decoupling capacitors should be provided for any driving/receiving devices and multivibrators. Multilayer printed wiring boards, with B+ and ground planes as internal layers, closely spaced, should be considered for minimum inductance when using TTL logic or any other logic element with an active pull-up. In all other cases make the ground bus or ribbon as wide as possible.

8. Power Switching Circuit Design

Switching of power, control, and signal functions should preferably be accomplished with solid state devices. Where the subsystem requirements cannot be met with solid state devices, electromechanical devices may be used. A detailed justification should be provided for the electromechanical devices chosen. Items to be considered in determining the optimum switching circuit are:

Circuit isolation;

Load characteristics;

Switch voltage drop and power dissipation;

Cycle requirements;

Response time;

Transients (generation and susceptibility);

Operating environments;

Volume and weight.

a. Power to Signal Ground Isolation - Isolation should be sufficiently high in impedance such that DC and AC ground loop currents are minimal.

b. Solid State Switching - The secondary breakdown limits of transistors should be met under the actual imposed reactive switching loadlines. Regenerative feedback techniques and decoupling should conform to the applicable requirements of section 6. Input interface requirements should conform to the applicable requirements of section 6.

c. Electro-Mechanical Switching - No single contact or driving function failure should cause loss or erroneous actuation of a critical function. Redundancy may be used to meet this requirement. Where redundancy is utilized, techniques must be provided for circuit checkout. Contacts may not be paralleled to provide total load current needs. It should be verified that the driven circuitry will tolerate the specified discontinuities due to contact bounce and resultant noise generation. Where magnetic latching type relays are used, the minimum coil energizing or

de-energizing pulse periods should exceed the maximum relay pull in or pull out requirement by a factor of 2.5. Transients or stimulus applied to the individual energizing or de-energizing coil should neither exceed 10% of the voltage-time product of the minimum transfer pulse specified, nor 5% where applied simultaneously to both coils.

9. Power Supplies

Power supply systems should have over-voltage limiting set to levels safe for the circuits being supplied. Power supply failure must not cause damage to the loads. It should also accommodate capacitive loads which may be imposed and which may affect the gain phase margin of negative feedback regulation. The gain and phase margins of section 6 should be met by the power supply under all load conditions. Overload protection should be provided, and the power supply must be able to withstand continuous short circuits. Under worst case conditions, the power supply should provide less than 90% of allowable ripple voltage and less than 90% of allowable regulation limits. The dynamic response should meet all load requirements.

10. Capacitors

Capacitors have an equivalent circuit that contains an ideal capacitor, inductor, leakage resistance, and equivalent series resistance. These effects should be determined and included in analysis of the circuit design. In addition to guideline deratings and as a minimum, surge and ripple current should be derated to 70% of rating and leakage current to twice rated. Circuits should operate properly over the complete voltage range with the variation in capacitance due to age and temperature. The effect of maximum temperature excursions should be added algebraically to life tolerances of capacitance. The drift capacitance changes to be utilized for five year (or less) life applications are as follows:

<u>Type Capacitor</u>	<u>Capacitance Change</u>
Glass	$\pm 0.5\%$ or ± 0.5 pf, whichever is larger.
Tantalum foil	$\pm 10\%$
Solid tantalum	$\pm 3\%$
Ceramic	$\pm 15\%$
Plastic	$\pm 0.05\%$ to $+0.5\%$, depending on MIL-C-5 letter designation
Silver mica	$+3\%$ under controlled environment

Capacitance values cannot be guaranteed for back biased polarized capacitors. The most suitable type material and capacitor construction should be chosen for each circuit use. Electrolytic capacitors, when used for bypassing and filtering, should be applied with a minimum of RF current flowing. The peak voltage should be lower than the derated dc working voltage. *Foil tantalum capacitors* may be safely charged from low impedance sources, other types of electrolytic capacitors should have at least three ohms per volt source impedance to limit surge current to a safe value. *Paper capacitors* are good for low frequency current applications. The current rating depends on the temperature rise produced by the dissipation factor and by the current flowing through the ohmic resistance. The low dissipation factor and high insulation resistance makes *plastic film capacitors* suitable for use up to 1 MHz for Mylar and up to 1 GHz for Teflon, Polystyrene and Polycarbonate capacitors in coupling and bypass applications. Plastic film capacitors have low dielectric absorption. Their use is almost mandatory in operational amplifiers used as integrators. The only other dielectric that competes with plastics in this area is *mica*. The characteristics of *ceramics* can be tailored to many applications, with the temperature coefficient of Temperature Compensation Ceramics capable of close control. Stable ceramics and glass compete strongly with mica in high frequency applications. *Micas* are often used as plate bypass capacitors for transmitters. Silver-micas may be subject to silver ion migration which is accentuated by humidity, high temperature, and constant dc potentials. For long term applications, this migration effect through the dielectric will reduce dielectric strength, insulation resistance, and capacitance. Consequently, silver-mica capacitors should not be used where these environmental conditions exist.

11. Resistors

Resistors have an equivalent circuit that contains an ideal resistor, inductance, and capacitance. These effects should be determined and included in analysis of the circuit design. In addition to guideline deratings, designs should provide for all tolerances and resistance changes caused by processing, environments, and life drift.

Metal film resistors used in a humidity controlled environment require a +0.37% and a -0.17% delta design tolerance if never operated in an ambient temperature in excess of 70°C and a wattage

dissipation more than 50% rated. For uncontrolled humidity applications, the delta design tolerance should be +0.46% and -0.26%. The effects of temperature and the initial tolerance should be added to these values, including the effects of self-heating.

Design tolerances for *carbon composition resistors* should be $\pm 19\%$. For 1% RW10 to RW69 *wire wound resistors*, the design tolerance should be $\pm 12.2\%$. For 0.1% RW10 to RW69 resistors, the design tolerance should be $\pm 11.3\%$. For 1% RW70 to RW80 wire wound resistors, the design tolerance should be $\pm 2.4\%$. For 0.1% RW70 to RW80 resistors, the design tolerance should be $\pm 1.5\%$. *Carbon composition resistors* have the least inductance. Carbon and metal film resistors, still relatively useful at high frequencies, have slightly more inductance, but not as much as non-inductive wire wound. *Inductive wire wound resistors* should be avoided except for dc and very low frequency circuits.

12. Transistors

In addition to guideline deratings, bipolar transistor minimum current gain should be derated 10% for aging and the leakage current derated to 200%. When applying devices below the gain temperature coefficient crossover point, the gain should also be decreased 7% for each 10°C below the specification temperature. For circuits sensitive to high gain, assure that maximum gain is specified, that it will not allow thermal runaway, and that closed loop margins are met. When operating the device below the gain temperature coefficient crossover point, the maximum gain should be increased for temperature at the rate of 7% for each 10°C rise above the specified temperature. Also, correction of gain for collector to emitter voltages above the value used in gain specifications should be made. Circuits should be designed to accommodate an open ended f_t specification (use of minimum f_t as specified but allowing for infinite f_t). Field effect transistor transmittance should be derated 15% for aging and -4% for each 10°C above the specification temperature. The transmittance should be increased 4% for each 10°C below the specification temperature. The effects of a positive temperature coefficient of R_{DSS} and a corresponding negative temperature coefficient of I_{DSS} should be included. The temperature coefficient varies slightly with the semiconductor doping level. However, at a chip temperature of 100°C , R_{DSS} and I_{DSS} will be no more than 1.7

times the 25°C values. Linear proportions may be assumed for other temperatures. The effect of the actual gate to source voltage on R_{DSS} should be included. The substrate potential and its effect on R_{DSS} for MOSFETS must also be considered. The effects of secondary breakdown in all switching circuits with inductive or capacitive loads should be determined and devices specified accordingly. No general rule, such as constant I^2t , will hold for transient capability of all devices. I^2t allowable is a strong function of voltage. Under no condition should the voltage rating be exceeded.

13. Diodes

In addition to guideline deratings, leakage currents should be derated to 200% of specification value to compensate for aging effects. No additional deratings above the guideline values are required for life stability of V_f , V_R , or V_z for diodes and zener diodes.

14. Transformers

For linear applications, either the combined effects of applied voltage at minimum operating frequency, hysteresis offset due to DC currents and operating temperature should cause flux excursions less than 75% of total saturation level, or examination of the hysteresis curve should be made to show acceptable performance at this operating point. Environmental requirements of shock, vibration, and temperature must be considered with regard to magnet wire type, core construction, winding type, and encapsulation requirements. Rise time and overshoot are affected by leakage inductance and interwinding capacitance. Leakage inductance may be reduced by using a small number of turns, toroid construction, interleaved primary and secondary, short average turn length, and bifilar windings. The interwinding capacitance may be reduced with thick wire insulation, small number of turns, interlayer insulation, winding of primary and secondary in separate sections, and by electrostatic shielding. Center tapped windings should be wound bifilar to reduce resistive and reactive unbalance. In the selection of core material for audio and power transformers, consideration should be given to core loss in watts per pound over the frequency range of interest to obtain maximum core efficiency and appropriate hysteresis loop shape. For maximum efficiency, losses should be distributed equally between core and copper.

The wire size should allow at least 850 circular mils per RMS ampere. If these requirements are in conflict, the wire size should govern. The insulation breakdown should be derated to 50% at maximum internal temperature. The stray inductive and capacitive effects should be negligible throughout the required passband. The design should provide less than 50% of the required circuit regulation limits. With open-circuited secondaries, a sufficient number of primary turns should be assured by designing for a primary impedance at least 10 times the reflected load impedance, for the lowest frequency of interest. For pulse transformers, the open circuit primary inductance should be specified to assure a pulse droop margin of 10% of the allowable droop. The interwinding capacitance should be low enough to allow the required rise time in the circuit under consideration. A maximum DC winding resistance should be specified to provide the proper L/R time constant. A 50% margin should be obtained of required peak pulse voltage and a voltage-time product obtained to provide a 25% margin on magnetic saturation. A 50% margin on voltage breakdown requirements should be obtained for winding to winding, winding to core, and winding to case voltages.

15. Relays

Switching of power, control, and signal functions should be accomplished preferably by the use of solid state devices. Where electromechanical devices must be used, justification should be provided for the electromechanical devices chosen. The areas to be considered in determining optimum switching devices are requirements of circuit isolation, switch voltage drop and power dissipation, cycle requirements, qualification and operating environments, generation and susceptibility to transients, response time, load characteristics, volume and weight.

Where relays are used as the switching element, no single relay contact failure should cause loss of a critical function. Redundancy may be used to meet this requirement, but techniques should be provided for circuit checkout. In addition to guideline deratings, a 20% margin should be provided for worst case operate voltage and current. Residual voltage or leakage current applied to the coil should not exceed 20% of the minimum drop out value. Relay coil suppression should be provided with consideration of suppression circuit failure modes, change in relay response time, voltage capability of driving circuitry, and EMI requirements.

Where magnetic latching type relays are used, the minimum coil energizing or de-energizing pulse periods should exceed the maximum relay pull-in or pull-out requirement by a factor of 2.5. Relay contacts should not be paralleled to provide total load current capability. Minimum current should be provided to all contacts which is at least 10% above the specified minimum ratings. The driven circuit should be designed to tolerate the specified discontinuities due to contact bounce and the resultant noise generation. Where relay contacts switch non-suppressed inductive loads, contact voltage ratings and life cycling capability should be adequate. Arc suppression may be provided for contact protection.

E. REFERENCES

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VI. VIBRATION LIFE EXTENSION OF PRINTED CIRCUIT BOARD
ASSEMBLIES

by R. W. Burrows

CONTENTS

VI.	VIBRATION LIFE EXTENSION OF PRINTED CIRCUIT BOARD ASSEMBLIES	VI-1
A.	INTRODUCTION	VI-1
B.	GUIDELINES	VI-2
C.	VIBRATION TESTS	VI-3
1.	Test Program	VI-3
2.	Test Results	VI-5
3.	Comparisons	VI-8
4.	Conclusions	VI-10
D.	CONTROL OF PC BOARD FLEXURE	VI-11
E.	STUDY OF REMOVABLE ENCAPSULANTS	VI-12
1.	Sandia Corporation's Microballoon Approach	VI-13
2.	Survey and Preliminary Evaluation of Other Removable Encapsulants	VI-14
F.	REFERENCES	VI-17
<u>Figure</u>		
1	Mounting Configuration No. 1	VI-6
2	Mounting Configuration No. 2	VI-7
<u>Table</u>		
1	Summary of Test Configurations	VI-4

VI. VIBRATION LIFE EXTENSION OF PRINTED CIRCUIT BOARD ASSEMBLIES

A. INTRODUCTION

With future reuseable space vehicles, such as the Space Shuttle, the equipment must be designed and qualified to vibration of long duration, as compared to the usual single launch situation. For example, the Shuttle Orbiter experiences 50 seconds of significant vibration per flight. If a time safety factor of four is applied, the duration of a vibration test to qualify the equipment for 100 missions is about 6 hours, and 28 hours for 500 missions. An alternate approach would be to utilize an accelerated test approach by increasing the level and shortening the time, but the trade-off between level and time has not been sufficiently established to define an acceptable accelerated test approach.

In future programs involving reusable hardware, it is always advantageous to utilize developed, off-the-shelf, hardware. In the case of electronic equipment, the typical method of packaging is conventional PC boards.

When conventional PC board construction is considered, in the light of anticipated Space Shuttle requirements, the following questions arise:

- 1) Will conventional PC board assemblies withstand 28 hours of vibration, and at what levels?
- 2) What can be done in the packaging design to increase the vibration capability, short of permanently encapsulating the entire assembly which is extremely undesirable from the standpoints of failure analysis, maintenance, and repair?
- 3) For accelerated test purposes, what is the trade-off between vibration time and level?
- 4) What minimum modifications can be applied to existing, off-the-shelf, hardware to significantly increase the vibration capability?

This study was conducted to gain preliminary answers to these questions. To answer Questions 1, 2 and 3, a brief vibration test program was conducted on PC boards. To answer Question 4, a preliminary study was conducted to determine what materials might be employed as an encapsulant that is easily removable, to facilitate repair and maintenance. The work of Sandia Corporation which has successfully used loose phenolic microballoons is summarized.

B. GUIDELINES

In the Space Shuttle Program, which will require Vibration Qualification Tests of very long duration, possibly 28 hours, the principal problem with most electronic equipment is failure of the electronic part leads due to flexure of the PC boards at their resonant frequency.

The tests summarized herein indicate that well-designed PC board assemblies adequately damped, can survive 28 hours vibration at levels under 15 or 20 g rms at the spectrum chosen to be representative of the Shuttle Orbiter.

The tests show that edge clamping, the use of damping strips, and conformal coating reduced the amplification from 80 to 15 and very significantly extend vibration life. Two boards of different design, but not edge clamped, damped or conformally coated, were vibrated at 17 g rms. The amplification was 80 and lead breakage began at 26.5 hours and 13 hours. When the vibration level was increased to 34 g rms to accelerate the test, lead breakage began at 28 minutes and 20 minutes. However, when a board was conformally coated, and damping strips applied, the amplification was reduced to 35; the first failure at 34 g's was delayed to 2.5 hours. When this configuration was also rigidly clamped at the edges, the amplification was further reduced to 15; and no failures had yet occurred when the test was terminated at 5 hours, 40 minutes.

The vibration time acceleration factors obtained by increasing the vibration level 6 db were highly variable, varying from 1.5 to greater than 79. The mean of nine data points was 23.6. Although the scope of this test program was not sufficient to substantiate an accurate acceleration factor, the approach used could yield more valid acceleration factors by applying the approach to a greater number of hardware items. If the resulting acceleration factor was, for example 20, then a 28-hour test could be conducted in 1.4 hours by increasing the qualification test level by 6 db.

Due to the uncertainties involved in any accelerated vibration test approach, it would be judicious to avoid excessive accelerations. A 3 db increase, rather than 6 db, would introduce much less uncertainty, but still provide a sufficient test acceleration to effectively shorten a 28-hour test.

For high vibration levels, exceeding 15 or 20 g rms, encapsulation of boards is desirable, but conventional encapsulents, such as the polyurethanes and epoxies, render the electronic package unrepairable. The Sandia Corporation has extended vibration life by filling the entire cavity of an electronic package with loose phenolic microballoons, reducing their PC board amplification from 28 to 6. For manned missions, the use of microballoons would create crew safety and contamination concerns. Further evaluation and development testing is recommended to identify and select other easily removable encapsulants which could be used in off-the-shelf hardware to allow the utilization of such hardware in future programs involving reusable vehicles and long vibration exposures. The study described herein recommends four candidates.

C. VIBRATION TESTS

1. Test Program

The primary failure mechanism of an assembled PC board under vibration is the flexing of the board at its resonant frequency which loosens, fatigues and breaks the leads of the mounted parts. In a prior test program, it was found that the electronic parts, which were broken from the PC boards, had not themselves failed. Accordingly, in the test program described herein, the data was evaluated on the basis of the time required to break the part leads and connections. Electrical functional tests were not conducted in order to maximize the test data with the limited resources allotted to the test program.

The test specimens consisted of six printed circuit boards, four of one configuration and two of a second configuration. The first, identified as Configuration A in Table 1, held one resistor, seven capacitors, and 36 dual in-line (DIP) integrated circuits (ICs). The second board, identified as Configuration B in Table 1, held one resistor, four capacitors, 11 DIP ICs, and 18 ICs in TO-5 cans. Both types of boards measured 5.75 x 6.20 inches.

Table 1 Summary of Test Configurations

SPECIMEN NUMBER	PCB CONFIG.	MOUNTING CONFIG.	DAMPING	CONFORMAL COATING	TEST LEVEL
1	A	1	No	No	17 Grms
2	B	1	No	No	17 Grms
3	A	1	No	No	34 Grms
4	B	1	No	No	34 Grms
5	A	2	Yes	Yes	34 Grms
6	A	1	Yes	Yes	34 Grms

Table 1 presents a summary of the configurations and parameters tested. A sketch of mounting Configuration 1 is shown in Fig. 1. This mounting consisted of two one-half inch standoffs at two corners, and clamped along the opposite, rear, edge of the board (where the board normally is plugged into an electrical connector). Mounting Configuration 2, as shown in Fig. 2, consisted of clamped supports along all four edges of the board. As indicated in the table, boards five and six were damped on the bottom with four strips each of a damping material planned for use on the Viking program, and identified as SMRD, a General Electric product. Also, as noted, some of the boards were conformally coated and some were not.

The basic random vibration level was as follows:

20 - 100 Hz at +3 dB/Octave

100 - 1000 Hz at $0.8 \text{ g}^2/\text{Hz}$

1000 - 2000 Hz at -6 dB/Octave

Overall = 34.0 g rms

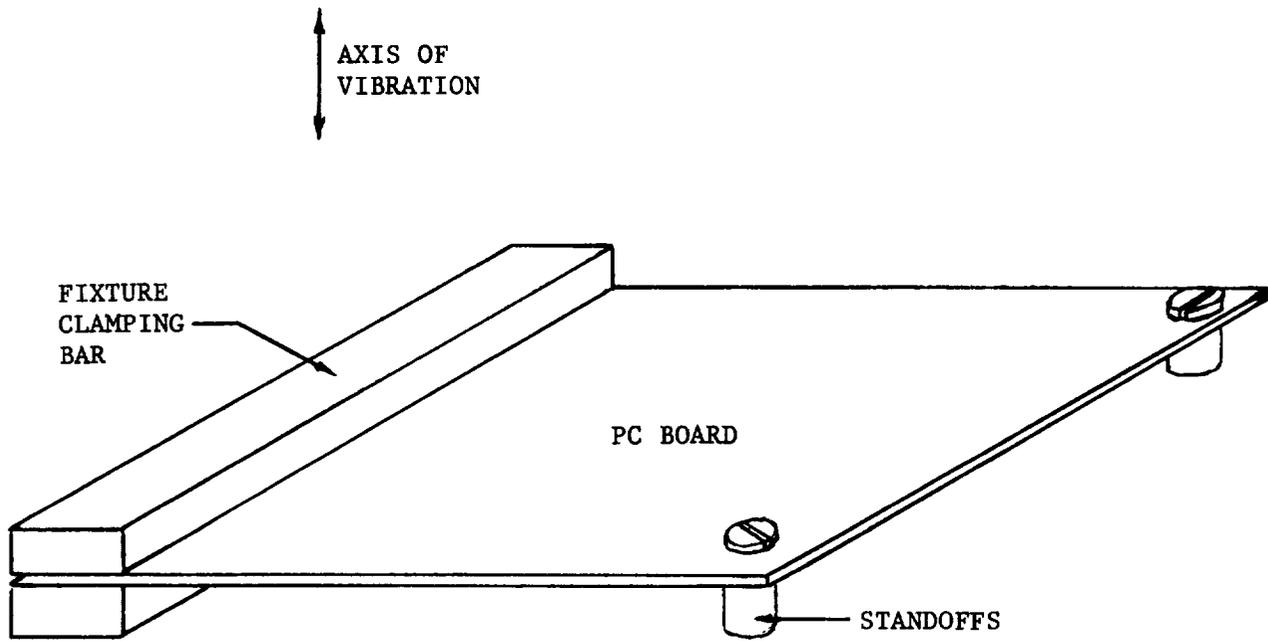
Some testing was performed at 17 g rms, but all testing was to the same spectral shape. The maximum test duration scheduled was 28 hours.

2. Test Results

The following listing presents the physical failures noted and the approximate times of occurrence. Refer to Table 1 for description of the particular specimen and test configuration. Also included are the dominant resonance frequencies and amplifications observed.

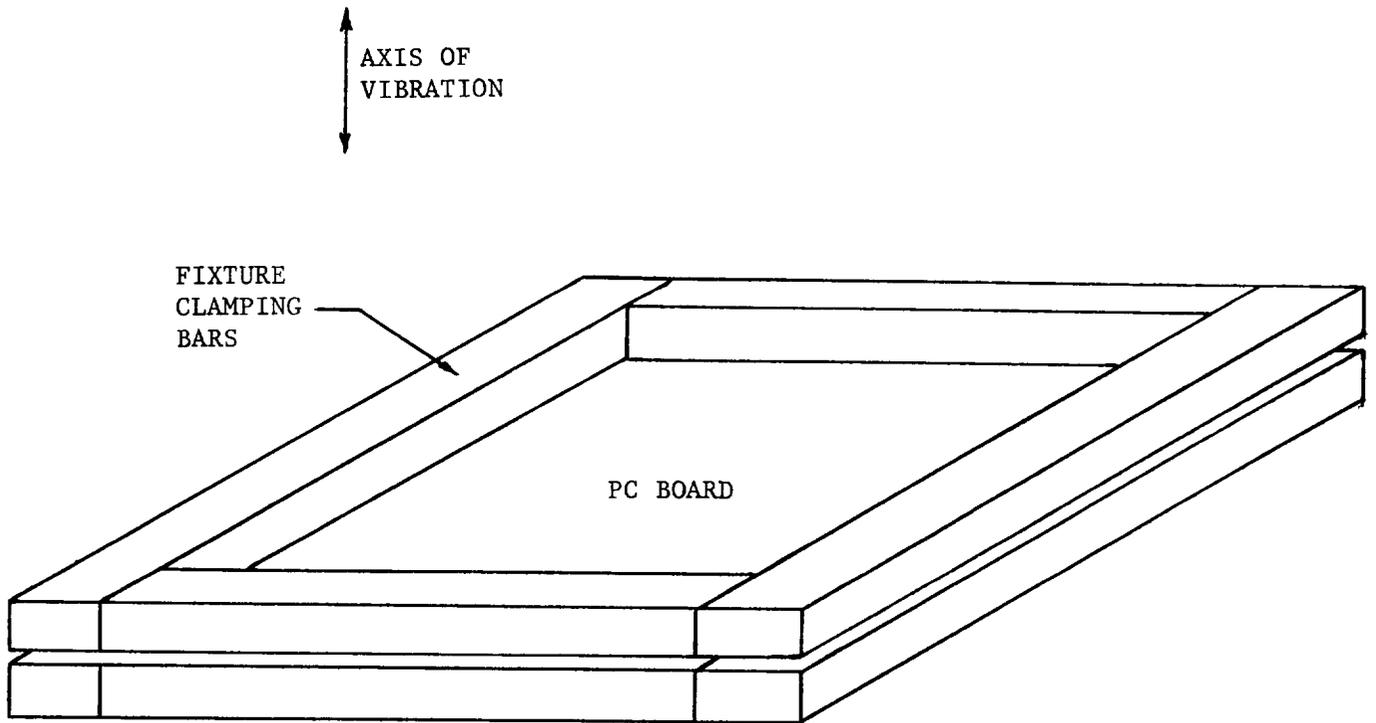
a. Specimen No. 1 - An amplification of 80 was observed at 160 Hz. Note that testing was at 17 g rms, 6 dB below the reference level. At 26.5 hours, loss of capacitor C-7 was observed due to failure of the leads at the solder joint.

b. Specimen No. 2 - An amplification of 80 was observed at 170 Hz. Note that testing of this PCB was also at 17 g rms. At approximately 13 hours, individual TO-5 IC leads started breaking and continued to accumulate until 26.5 hours, at which time IC A19 completely separated from the board. At this time there were 14 additional leads broken on seven other IC's.



NOT TO SCALE

Figure 1 Mounting Configuration No. 1



NOT TO SCALE

Figure 2 Mounting Configuration No. 2

c. *Specimen No. 3* - Specimen and mounting configurations were the same as Specimen No. 1, so no resonance search was performed. Testing was at the reference level, 34 g rms. At 28 minutes, failure of capacitor C-7 was observed, due to lead failure at the bends in the leads. At 30 minutes, capacitor C-5 was lost by the same failure mechanism. At 3 hours, 45 minutes, capacitor C-6 was lost; one lead failed at the solder joint and the other lead failed at the bend. Between approximately 14 hours and 17.8 hours, six leads broke on the DIP ICs. Testing was stopped at 17.8 hours.

d. *Specimen No. 4* - Specimen and mounting configurations were the same as Specimen No. 2, so no resonance search was performed. Test level was the reference level of 34 g rms. At 20 minutes, resistor R-1 broke off due to failure of the leads at the solder joints. At approximately five hours, capacitors C-2 and C-3 broke off at the solder joints. Commencing at approximately six hours, individual TO-5 IC leads started breaking, with 29 broken at 13.8 hours and 63 broken at 17.8 hours. Physical separation of IC number A-3 occurred at 15.8 hours, A-4 at 16.4 hours, and A-19 at 17.1 hours. Testing was stopped at 17.8 hours.

e. *Specimen No. 5* - An amplification of 15 was observed at 400 Hz. The test level was 34 g rms. At the end of testing, 5 hours, 40 minutes, no failures were observed.

f. *Specimen No. 6* - An amplification of 35 was observed at 170 Hz. At 2.5 hours, capacitor C-5 was lost due to broken leads at the bends. At 3 hours, 10 minutes, capacitor C-6 was lost, and at 3 hours, 20 minutes, capacitor C-7 was lost. No further failures were noted when testing was stopped at 5 hours, 40 minutes.

3. Comparisons

Specimens No. 1 and No. 3 were identical except No. 3 was tested at twice the rms level, 6 dB higher. Capacitor C-7, which failed on PCB No. 3 at 28 minutes, failed on PCB No. 1 at 26.5 hours. Thus, a 6 dB decrease in level resulted in an increase of time before failure by a factor of 57. The same capacitor on PCB No. 6, which had a thin conformal coating and damping strips added, lasted for 2 hours, 20 minutes, an increase of a factor of 7. Capacitor C-5 which lasted 30 minutes on PCB No. 3, had not failed at end of 26.5 hours during low level test, but failed at 2.5 hours on PCB No. 6, an increase of a factor of 5. Capacitor C-6, which failed at 3 hours, 46 minutes on PCB No. 3, did not fail on PCB No. 1, but failed at 3 hours, 10 minutes on PCB No. 6, an increase of a factor of only 1.2. However, the same printed circuit

board configuration, when clamped on four sides, conformally coated, and damped, did not experience any failures at 34 g rms for 5 hours, 40 minutes. This indicates a minimum life increase of 12X for C-7, 11X for C-5, and 1.5X for C-6. In summary, consider PCB No. 3 as the reference board. Decreasing the level by 6 dB extended the lives as follows:

57X for C-7

53X (minimum) for C-5: Did not fail at -6 dB

7X (minimum) for C-6

Adding conformal coating and damping strips extended the lives as follows:

7X for C-7

5X for C-5

1.2X for C-6

Adding conformal coating, damping strips, and clamping all for sides increases the lives a minimum as follows (parts did not fail in this configuration):

12X (minimum) for C-7

11X (minimum) for C-5

1.5 X (minimum) for C-6

For the "B" configuration board, consider PCB No. 4 as the reference board. Decreasing the level by 6 dB increases the lives as follows:

79X (minimum) for R-1

5.3X (minimum) for C-2

5.3X (minimum) for C-3

2.2X (approximate) for initiation of T0-5 IC lead breakage

1.7X for loss of first IC

1.5X for loss of IC No. A-19

4. Conclusions

Based on the limited data from this test, only general conclusions can be drawn. A 6 dB reduction in test level (one-half the g rms level) resulted in an increased part life. That increase varied for individual parts from a factor of 1.5X to in excess of 79X. The mean of nine data points was 23.6X minimum. The addition of conformal coating and damping strips also increased the part life; this increase varied from 1.2X to 7X.

A further change to clamped on four sides (from clamped on one side and standoffs on other two corners), with conformal coating and damping, extended the part life even further; this increase varied from "in excess of 1.5X" to "in excess of 12X."

The addition of conformal coating and damping strips reduced the amplification by a factor of 2.3 (from 80 to 35). A further change to clamped four sides provided an additional reduction by a factor of 2.3 (from 35 to 15).

The most significant conclusion that can be drawn from these test data is that test levels less than 15 or 20 g rms and long durations (28 hours for example) do not appear to present insurmountable problems using existing PCB design if proper precautions are taken in board design, component layout, and mounting techniques. The tests have indicated that damping material may significantly reduce the amplifications at resonance, with inherent longer life. Also noted was the fact that going to a more rigid mounting configuration (clamped on four sides as compared to clamped one side and two standoffs) not only increased the resonant frequency, as expected, but also resulted in a significant decrease in the amplification at resonance. This decrease in Q apparently results from a change to a "more complex" mode shape, one with more inflection points and more antinodes. Generalizing on this result, the Q of a board may be reduced by any mounting change which results in excitation of a higher mode, or results in exciting a different fundamental mode with a more complex shape. For example, the addition of a center support will restrain the first mode and force any resonance occurring to be at a higher mode with a lower amplification. The data acquired does not permit a quantitative evaluation of the reduction gained for any particular mode change.

At vibration levels higher than 15 or 20 g rms, or for off-the-shelf hardware not currently designed to withstand long duration exposure to 15 or 20 g rms, the use of encapsulation should be considered. Removable encapsulents which provide a much greater degree of maintainability than solid potting, are discussed in the next section.

D. CONTROL OF PC BOARD FLEXURE

The following information, directly abstracted from a paper by D. E. Longmire (Ref 1), confirms the benefits of edge clamping and board dampening. It also presents other data.

"In PC boards it is mainly the displacement which caused the failures, not the actual g loads. The repeated flexure destroys the solder joints, the adhesion of the circuit lines to the boards, and fatigues component leads until they break. So it can be said that most printed circuit boards can stand high g's if flexure is not allowed.

"To control flexure these things need to be done: size and weight reduced, the board made thicker, board supports added or the edge supports improved, damping added, or the board isolated. In any event, the control must move the board natural frequency to one which is well separated from the mounting structure natural frequency. When isolators are used, the isolation frequency should be less than half that of the structural f_n . If stiffness is the route taken, then the f_n of the board assembly should be twice the structural resonant frequency. In this approach it is desirable to place the f_n of the board higher than any expected range of input frequencies.

"Individual component g levels may be very high using the last method, but unless these components are large, or heavy, or definitely delicate, no failures should occur. Individual PC components in modern electronics are very rugged and can generally withstand 100 to 200 g's or more with ease.

"There are several schemes for damping PC boards. Visco-elastic materials for this purpose are made by the Lord Manufacturing Corporation. A layer of the visco-elastic material is bonded to a thin glass laminate which is approximately 0.03" thick. This assembly is sandwiched to the soldered side of a single-sided PC board and the sandwich then consists of PC board, visco-elastic layer, and finally the fiberglass skin. The results of this damping are dramatic. Reduction of the Q or amplification by a factor of 4 or 5 may be expected. In addition, the f_n of the board and damping assembly will rise by almost a factor of two, which is usually in the right direction.

"The Korfund Corporation has developed several interesting damping compounds which can be applied putty-like to the PC board. Again damping is very effective. Both of the above materials share the common disadvantage of making board repair difficult. For this reason, isolation techniques are the most popular and successful method of protecting PC boards.

"The Barry Corporation makes PC board edge guides which incorporate flexibility and therefore isolation at the very input to the PC board. Edge guides which have a medium hardness of approximately 50 to 60 durometer set up an isolation f_n of about 70 cps in a 4x6" moderately loaded digital type PC board. We have made these guides using polyurethanes and modified epoxies. Both of these materials have good damping characteristics; however, at this time it is too early to give complete results of vibration testing. Vinyls are fine at room temperature, but these do not exhibit particularly satisfactory thermal or long term dimensional properties.

"The amount of damping which an electronic cabinet can have is a function of the thought and detail put into the factor by the designer. Riveted structures can be advantageous in self-dampening as assembly. Damping materials similar to those described earlier can also be used. Think in terms of damping and isolation rather than rigidity and integrity and much less of the hostile outside world of vibration will reach the inner sanctum of the PC board."

Reference 2 also presents empirical design data derived from vibration tests, for calculating the PC board resonant frequency as a function of board shape, size, thickness, material, and mounting technique.

E. STUDY OF REMOVABLE ENCAPSULANTS

This survey was accomplished to determine what minimum modification, in the form of an easily removable encapsulant, could be applied to existing off-the-shelf hardware to significantly increase the vibration capability. The work of Sandia Corporation is summarized together with a discussion of other possible approaches.

1. Sandia Corporation's Microballoon Approach

Sandia has developed a system employing loose phenolic microballoons and silicone rubber to improve vibration and shock capability of electronic equipment. This work, reported by E. C. Neidel (Ref 2), is described: An electronic package with PC boards instrumented with accelerometers was vibrated and a peak response (Q) of 28 was measured at 84 cycles. Filling the unit with glass microballoons reduced the peak response to 12, at 300 cps. It was observed that the glass microballoons had a tendency to break into small pieces, tended to act as an adhesive, and could constitute a health hazard if they became airborne and were inhaled. Phenolic microballoons were then tested. These reduced the peak response from 28 to 6.2, and did not break up. With a size range of 0.0002 to 0.0050 inches in diameter, and an average particle diameter of 0.0017 inches, no health problems were anticipated by either the Sandia medical or safety departments. Consequently, loose phenolic microballoons were chosen as the packing material to fill the free volume of the unit.

During the vibration tests some component and lead wire failures occurred, so silicone rubber was applied to provide additional support. First, a viscous mixture with 2% silicon dioxide was applied with a spatula to form large fillets between the larger and heavier components and the circuit board. Then, silicone rubber, without the additive, was poured in the assembly and allowed to run off freely. The result was a cocoon-like conformal coating about 1/16 inch thick. The silicone rubber used was formulated to cure at room temperature in 24 hours. Both the conformal coating and the thicker fillet mixture are readily peelable after curing. The surface adhesion is low enough to allow easy removal from all surfaces. As a result, the dynamic characteristics of the unit have been improved with the only compromise on the ease of repair being the addition of a readily peelable material. Areas exposed during repair can be recoated with no difficulty.

In a microballoon system, all components must be sealed including those which penetrate the container. Also, the container itself must be sealed to keep the microballoons in, and to keep moisture out.

2. Survey and Preliminary Evaluation of Other Removal Encapsulants

Several prerequisites exist for the "Ideal" potting material. The material should be easily applied and easily removed to facilitate maintenance and repair. The material should be nonflammable and not hazardous to the crew. The material should not impose stresses on the parts. Heat conduction properties of the material must be considered.

A survey, conducted to acquire suggestions, resulted in 12 suggestions, four of which merit further consideration. These suggestions, and their evaluation, are presented below:

- 1) Suggestion No. 1 - Process General Electric's SMRD (used as damping strips in the previously described test program) into small blocks, pellets, or granules, and pack them into the assembly.

Reviewers Comments - A good suggestion worthy of further evaluation by a test program.

- 2) Suggestion No. 2 - Fill the cavity with powdered alumina.

Reviewers Comments - No advantage over Sandia's phenolic microballoons and has the disadvantage of being heavier. Recommend no further consideration.

- 3) Suggestion No. 3 - Fill the cavity with a mixture of 3M Fluorocarbon Fluid and Emerson and Cummings "Eccospheres."

Reviewers Comments - This combination provides fluid dampening, and heat transfer better than natural convection. It is an inert fluid, is nonflammable, and has excellent dielectric strength. However, since it is a liquid, a leak in the package would create a messy situation.

- 4) Suggestion No. 4 - Use a wax with a melting point high enough to present a phase change at the highest required temperature. This is usually 160°F.

Reviewers Comments - Waxes have reasonably good dielectric strength and wide range of melting points. However, waxes contract upon solidification rendering the filling operation more difficult. They are heavier than the Sandia approach and they may impose stress on parts at low temperatures, although data on this facet has not been located. Also, waxes are flammable and impose a potential crew safety hazard.

- 5) Suggestion No. 5 - Use General Electric RTV 602, which is friable and thus easily removed. Thermal conductivity can be maximized using large granules of alumina (Al_2O_3) in the potting. Microballoons could be added to the base resin to lower the specific gravity.

Reviewers Comments - This material may not be as easily removable as the above indicates. This should be determined before the material is considered a good candidate.

- 6) Suggestion No. 6 - Treat the printed circuit boards and the package interior with a silicone mold release compound. Fill the package with a very soft foamed silicone room-temperature-curing material. The poor tensile strength would allow the PCB's to be pulled out of their mounts.

Reviewers Comments - Believe the components on the PCB boards would lock in the PCB boards so they could not be *easily* removed, but the approach may be feasible with the components having small vertical dimensions, like flat packs. This approach is worthy of further evaluation.

- 7) Suggestion No. 7 - Fill the package with petrolatum.

Reviewers Comments - Inflammable, fairly heavy, and messy in event of a leak in the package.

- 8) Suggestion No. 8 - Use resilient vibration-energy dampening blocks of silicone rubber molded to closely fit parts. Place blocks (1-2 in.² area) at points of maximum vibration, cemented to one surface, and in compression between adjacent PCB's. Minimizes stressing of parts, low weight, easy repair (may be sliced free), won't trap gas, and minimizes blocking of heat flow.

Reviewers Comments - Worthy of further evaluation. General Electric's SMRD is superior to silicone rubber.

- 9) Suggestion No. 9 - Use Thiokol Chemical Company's Solithane 113/300 polyurethane, either unfilled as a clear, low viscosity potting resin, or filled with Cab-O-Sil for a thixotropic, clear, encapsulation coating. Is visco-elastic and has good damping properties. Is relatively easy to remove by attack from chlorinated solvent and mechanical means. The filled version is recommended for weight savings.

Reviewers Comments - This material may not be as easily removable as the above indicates. This should be determined before the material is considered a good candidate.

- 10) Suggestion No. 10 - Use low density polyurethane foam, such as MMC-L721A, or CPR 1021. May be softened with alcohol, followed by mechanical removal for repair. Excellent for fabrication, weight and repair. Adequate heat transfer must be accomplished through wide copper traces conducting to a heat sink.

Reviewers Comments - This material is used on the Titan program, where it has been found that the packages are essentially unrepairable. The removal process is unwieldy, time consuming, and has a significant potential for damaging the electronic parts.

- 11) Suggestion No. 11 - Fill the cavity with a mixture of phenolic microballoons and SMRD granules.

Reviewers Comments - This combination could provide more, or possibly less dampening, than Sandia's phenolic microballoon approach. A test program would be required to establish this.

- 12) Suggestion No. 12 - Pack the cavity with moist brown sugar and harden the material by vacuum exposure at a slightly elevated temperature. The potting can be removed by dissolving in water. This approach is used by Sandia during prototype development testing, where a removal potting material is needed.

Reviewers Comments - An ingenious approach, useful in development testing, but not desirable for production hardware since the high modulus of the dried material would severely stress the internal parts during temperature changes.

It is concluded that suggestions, numbers 1, 6, 8 and 11, have merit. It is recommended that a test program be initiated to establish the comparative feasibility and effectiveness of these suggestions, as well as further search for additional candidate solutions for extending the vibration endurance of off-the-shelf electronic hardware with minimum modification.

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VII. TOLERANCE FUNNELING AND TEST REQUIREMENTS STUDY

by R. A. Homan

CONTENTS

	<u>Page</u>
VII. TOLERANCE FUNNELING AND TEST REQUIREMENTS STUDY	VII-1
A. INTRODUCTION	VII-1
B. TOLERANCE FUNNELING TEST GUIDELINES	VII-1
1. End of Life Tolerance	VII-1
2. Test Equipment Uncertainties	VII-1
3. Test Limit Margins	VII-2
4. Analysis	VII-2
5. Module Pre- and Post-Encapsulation Limits	VII-3
6. Component Design Development and Qualification Limits	VII-3
7. Component Acceptance Limits	VII-3
8. Subsystem Limits	VII-3
9. Module Test Loads	VII-3
10. Component and Subsystem Test Loads	VII-3
11. Module Stimuli	VII-5
12. Component and Subsystem Stimuli	VII-5
13. Test Equipment Accuracy	VII-5
C. DISCUSSION	VII-5
1. General	VII-5
2. Test Limit Consideration	VII-6
3. Test Limit Restraints	VII-7
4. Test Limit Selection	VII-9 and VII-10

Figure

1 Dual-Valued Test Limits	VII-6
-------------------------------------	-------

Table

1 Test Type and Test Limits - Component DD/Qual Tests and Subsystem Tests	VII-4
2 Limits as a Function of n Variables - Equally Weight	VII-10

VII. TOLERANCE FUNNELING AND TEST REQUIREMENTS STUDY

A. INTRODUCTION

To reduce the incidence of extremely costly failures at the launch complex, and at all other high levels of assembly, it is essential that the functional test requirements for a given hardware item be most stringent during the earliest stages of fabrication, and progressively less stringent as the hardware is moved through successive testing to the final countdown. This philosophy, referred to as Tolerance Funnelling, or Triangular Tolerances, insures that marginal hardware is detected early in the life cycle where corrective action is least costly and most readily applied. It is extremely costly and bad practice to employ the same functional requirements throughout the life cycle, since small shifts or drift in either the hardware or in the test instruments will cause equipment to be rejected late in the life cycle. Where the philosophy of tolerance funnelling is recognized and accepted, the problem that then exists is that each different designer has his own approach to establishing the tolerance funnel. The purpose of this study is to present a tolerance funnelling approach that can produce a more consistent and uniform approach within a given program.

B. TOLERANCE FUNNELING TEST GUIDELINES

1. End of Life Tolerances

End of life degradation tolerances of tested parameters as identified by worst case analysis should be excluded from the test limits during all levels of test. A possible exception is that during EMI susceptibility and voltage transient margin testing, end of life limits can be included due to severity of the tests.

2. Test Equipment Uncertainties

Test equipment uncertainties must be defined and should fall inside of the test limits. It should not allow the acceptance of a flight component with a tested parameter that exceeds the realizable worst case limit in that test configuration.

3. Test Limit Margins

Test limit margins should be relaxed with each level of test (module to component to subsystem). This decreases the risk of having a test failure as the impact of having a test failure increases. For example, a test failure at the subsystem level represents a greater impact than at the component or module level test.

4. Analysis

Test limits should be based primarily upon the worst case analysis to identify the worst case limits in the different hardware configurations. These iterations are:

- 1) Manufacturing Acceptance test worst case limits at the module level during pre-encapsulation tests. These worst case limits should consider initial part tolerances plus self heating caused by part application.
- 2) Manufacturing Acceptance test worst case limits at the module level during post-encapsulation tests. These worst case limits should consider initial part tolerances plus self heating caused by part application and should consider effects of the encapsulation techniques employed.
- 3) Acceptance, design development, and qualification test worst case limits at the component level where tests are conducted under bench conditions. These worst case limits should consider initial part tolerances plus self heating caused by part application and should consider effects of component case internal temperatures.
- 4) Acceptance test worst case limits at the component-level where tests are conducted under temperature extremes. These worst case limits should be as determined in 3) plus any worst case deltas due to temperature extremes.
- 5) Design development and Qualification test worst case limits at the component levels under temperature extremes. These worst case limits should be as determined in 4), plus any worst case deltas resulting from the wider temperature range.
- 6) Component limits based on controlling interface requirements. These limits should be total worst case variations, including all environments and "end of life" degradation.

5. Module Pre- and Post-Encapsulation Limits

Test limits for acceptable units should be 50% or Root Sum Square (RSS) of worst case limits, whichever is greater during pre and post encapsulation tests. Test limits for unacceptable units during pre and post encapsulation tests should be the worst case limits. Units with test values between the acceptable and unacceptable limits should be analyzed individually for disposition as to rework, retest, acceptable as is, or reject.

6. Component Design Development and Qualification Limits

Test limits for component design development and qualification tests should be in accordance with Table 1.

7. Component Acceptance Limits

Test limits for acceptable components should be 60% or Root Sum Square (RSS) of worst case limits, whichever is greater for bench operating conditions, dynamic environments (i.e., shock, vibration), and before and after heat compatibility. During temperature tests, the acceptable limits should be 60% or Root Sum Square (RSS) of worst case limits, whichever is greater. Test limits for unacceptable components should be worst case limits for bench operating conditions, dynamic environments (i.e., shock, vibration), and before and after heat compatibility. During temperature tests, the unacceptable limits shall be the worst case limits. Components with test values between the acceptable and unacceptable limits should be analyzed individually for disposition as to rework, retest, acceptable as is, or reject.

8. Subsystem Limits

Test limits for subsystem mock-up tests, ETC, PTC, etc. should be in accordance with Table 1.

9. Module Test Loads

Test loads for modules should be "end of Life" as identified in the worst case analysis and should include margin verification. The test loads should encompass all interface limits.

10. Component and Subsystem Test Loads

Component and subsystem test loads should encompass all controlling interface requirements.

Table 1 Test Type and Test Limits - Component DD/Qual Tests and Subsystem Tests

<u>Test</u>	<u>Oper.</u>	<u>Non Oper.</u>	<u>Opr/Non Op.</u>	<u>* Limits</u>
Proof Pressure			X	1)
Burst Pressure		X		1)
Seal		X		1)
Static Load		X		1)
Operating Life	X			1)
Heat Compat.		X		1)
Non Op. Pyro		X		1)
EMC	X			2)
Temp Humidity		X		1)
Prop. Comp.		X		1)
Asc. Pressure			X	1)
Launch Accel.		X		1)
Launch Acous.			X	1)
Launch Vibr.			X	1)
Cruise T/V			X	3)
Corona/Arcing	X			1)
Entry Thermal			X	3)
Entry Accel.	X			1)
Entry Acous.			X	1)
Entry Vib.			X	1)
Oper. Pyro	X			1)
Landing Shock			X	1)
Surface Thermal	X			3)
Sand/Dust			X	1)
Extended Level				
Voltage	X			2)
Transients			X	2)
Vibration			X	1)
Temperature			X	3)
Extended Cycle				
Longer duration	X			4)
Extended Life	X			1)
Specials				
Nuc. Rad.	X			1)
Windbl. Dust	X			1)
Prelaunch Thermal	X			3)
Mag. Field	X			1)
Static Discharge	X			1)

- * 1) Test limits should be 70% or Root Sum Square (RSS) of worst case limits, whichever is greater, per paragraph 4(3) before, during and after test as applicable.
- 2) Test limits should be 70% or Root Sum Square (RSS) of worst case limits, whichever is greater, per paragraph 4(3) before, during and after test, except worst case limits of paragraph 4(6) should apply during all susceptibility testing (i.e., radiated, conducted, transients).
- * 3) Test limits should be 70% or Root Sum Square (RSS) of worst case limits, whichever is greater, per paragraph 4(3) before and after test. Test limit should be 70% or Root Sum Square (RSS) of worst case limits, whichever is greater, per paragraph 4(5) during test as applicable.
- 4) Test limits should be 70% or Root Sum Square (RSS) of worst case limits, whichever is greater, per paragraph 4(2) before and after test. During test, use 70% or Root Sum Square (RSS) or worst case limits, whichever is greater, per paragraph 4(3) for vibration; or 70% or Root Sum Square (RSS) of worst case limits, whichever is greater, per paragraph 4(5) for temperature, as applicable.

11. Module Stimuli

Electrical stimulus for modules should be "end of life" as identified in the worst case analysis. The test conditions should encompass controlling interface limits.

12. Component and Subsystem Stimuli

Component and subsystem external stimulus should encompass controlling interface requirements.

13. Test Equipment Accuracy

Test equipment accuracy, by order of preference, should be as follows:

- 1) An accuracy of at least an order of magnitude better than the allowable tolerance of the measurement to be made.
- 2) Calibration of the test equipment by using standard signals which simulate the expected range of signals in three or more steps. The standard signal accuracy shall be at least three times greater than the measurement tolerance.
- 3) Within state of the art limitations, the inaccuracy of the test equipment shall be no greater than 25% of the allowable tolerance of the measurement to be made.

C. DISCUSSION

1. General

The worst case analysis determines if component/subsystem performance requirements will be met under worst case electrical and environmental conditions including end of life mission degradation. A direct extension of this discipline is the total test program which among other things establishes confidence, by environmental and functional tests, that each flight system is free of defects and capable of performing the mission. As discussed in the following paragraphs, various test limits (tolerance funneling) should be considered for all levels of test. Considerations have been given to the effects of environments, loads, stimulus and measurement uncertainties on test limit selection.

2. Test Limit Considerations

If a module is a worst case design, it is generally accepted that a worst case unit will never be built. In other words, a test parameter close to the worst case limit may be an indication of a faulty unit, i.e., wrong part, damaged part, bad solder joint, faulty test equipment, etc. In these situations, an evaluation or disposition of the unit should be made.

This approach requires dual-valued test limits as shown in Figure 1.

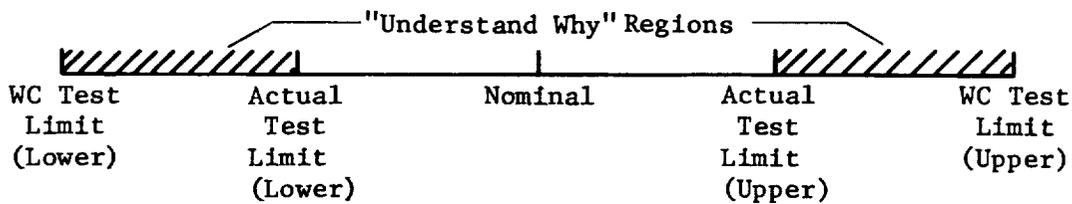


Figure 1 Dual-Valued Test Limits

The worst case test limit is the realizable test limit in the test configuration and test environment and is determined by worst case analysis. When the test parameters exceed these WC limits, the module is rejected.

The actual test limit is a limit more representative of the actual hardware considering the normalizing tendency of a test parameter that is a function of several variables.

The "understand why" region is bounded by these two limits. Test parameters falling into this region require evaluation and disposition. The evaluation might include the following:

- 1) Check part numbers for correct values;
- 2) Check PC board/module layout, solder joints, etc. Perform continuity measurements;*
- 3) Measure the actual part values;*
- 4) Observe waveforms, currents and voltages;*
- 5) Verify supporting test equipment.

*These measurements would be done to the extent possible without lifting any part leads. Extreme care would be required during these measurements to prevent part damage or degradation. Test equipment must be suitable for the parts used in the circuits being evaluated from the standpoint of applied voltage, current and loading effect (transient and dc).

3. Test Limit Restraints

The selection of the actual test limit is difficult because of the many restraints, some of which are identified as follows:

Items forcing the test limits to nominal are:

- 1) Nominal units allow maximum degradation for the mission;
- 2) All incorrect (wrong) parts should be identified;
- 3) All damaged parts should be identified;
- 4) All manufacturing defects (solder joints, etc.) should be identified.
- 5) Proper test equipment implementation.

Items forcing the test limit to worst case are:

- 1) Good units should not be rejected;
- 2) Understand process is not cost effective;
- 3) "Understand" process can impair reliability if troubleshooting becomes excessive or is done carelessly;
- 4) Reject of good hardware at the subsystem/system level is a serious program impact;
- 5) Test parameter distribution is difficult to predict.

The impact of different test limits is illustrated by the following example which considers two variables:

The parameter to be measured is a time constant, $\tau = RC$. The test level is a PC board acceptance test at room temperature.

The worst case tolerance on "R" is

initial = $\pm 1\%$
Temperature = $\pm 1\%$ = $\pm 3\%$ total
aging = $\pm 1\%$

The worst case tolerance on "C" is

initial = $\pm 9\%$
Temperature = $\pm 9\%$ = $\pm 27\%$ total
aging = $\pm 9\%$

The worst case limit, as a result of initial tolerances would be $\pm 10\%$.

Case 1. Assume a test limit = $\pm 10\%$

Then, the units falling in the "understand why" region = 0. "R" could be any value from nominal $\pm 10 \pm 9 = \pm 19\%$ assuming "C" is in specification.

"C" could be any value from nominal $\pm 10 \pm 1 = \pm 11\%$ assuming "R" is in specification.

Case 2. Assume a test limit = $\pm 5\%$

"R" could be any value from nominal $\pm 5 \pm 9 = \pm 14\%$

"C" could be any value from nominal $\pm 5 \pm 1 = \pm 6\%$

Case 3. Assume a test limit = $0\% = \text{nominal}$

Then, every unit would fall into the "understand why" region and "R" could be any value from nominal $\pm 9\%$.

"C" could be any value from nominal $\pm 1\%$

The three different cases indicate the following:

Case 1 is the most cost effective

Case 2 is a compromise and the most desirable

Case 3 allow maximum margin for end of life degradation but is not cost effective.

In no case, can a limit be selected that will guarantee that all parts are within specified limits.

4. Test Limit Selection

The selection of the recommended test limits given in this report is based upon the following:

Case 1. Test limits are 50 % of worst case limits.

These limits would apply when the parameter to be measured is the composite or result of several variables (n) that are equally weighted. Table 2 gives the worst case limit, 50% worst case limit and the RSS limit for n = 1 to 10. The table indicates that for n > 4, the RSS limit is < the 50% worst case limit.

For n greater than 4, the margin of 50% worst case limit over the RSS limit should result in a minimum number of "understand why" conditions even though it is recognized that the distributions of the individual variables are not normal distributions.

The 50% limit also provides a generous margin over the worst case design limit.

Case 2. Test limits are RSS limits.

These limits would apply when n is small and/or when the individual variables are unequally weighted. The example given in Attachment 1 illustrates the predominant effect of the largest variable in the RSS limit which tends to minimize the significance of the initial distribution of the individual variables. Although the margin over the worst case limit is not as great as for Case 1, the RSS margin should be more representative of real life and result in a minimum number of "understand why" conditions.

The test limits at higher levels of test (component, subsystem) are increased to provide funneling, thereby tending to reduce the risk as the level of the test increases.

Although test equipment uncertainties have not been considered in this, they would naturally be included inside the test limits selected. Care must be taken when using the RSS test limits such that inverse funneling does not result from increasing test equipment uncertainties as the level of the test increases.

Table 2 Limits as a Function of n Variables - Equally Weighted

<u>n</u>	<u>Worst Case</u>	<u>RSS</u>	<u>50% WC</u>
1	1%	1%	.5%
2	2%	1.4%	1.0%
3	3%	1.73%	1.5%
4	4%	2%	<u>2.0%</u>
5	5%	2.23%	2.5%
6	6%	2.45%	3.0%
7	7%	2.64%	3.5%
8	8%	2.82%	4.0%
9	9%	3%	4.5%
10	10%	3.16%	5.0%

