

**DESIGN, FABRICATION, TESTING AND DELIVERY OF A FEASIBILITY MODEL
LAMINATED FERRITE MEMORY**

by

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FINAL SUMMARY REPORT

**Contract No. NAS8-27594
DRL No. 271,
Line Item No. 2**

27 April 1973

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Prepared for

**NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GEORGE C. MARSHALL SPACE FLIGHT CENTER
MARSHALL SPACE FLIGHT CENTER, ALABAMA 35812**

**NASA-CR-124372) DESIGN, FABRICATION,
TESTING AND DELIVERY OF A FEASIBILITY
MODEL LAMINATED FERRITE MEMORY Final
Summary Report, 24 Jun. 1971 - 30 Mar.
(Ampex Corp.) 33 p HC \$3.75 CSCI 09B G3/08 17807**

**N73-30149
Unclas**

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RR 73-06

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ABSTRACT

A study on the effect of using multi word addressing with laminated ferrite arrays was made. This study showed that both a reduction in the number of components and a reduction in power consumption is obtained for memory capacities between 10^6 bits and 10^6 words.

An investigation into the effect of variations in the processing steps resulted in a number of process modifications that improved the quality of the arrays. Two problems for which the investigation did not result in a solution are the development of an improved method for fabricating the $17 \mu\text{m}$ (.0007 in.) center lamina and the isolation of the factors which produce an anomalous high sense signal output observed in some arrays.

A feasibility model laminated ferrite memory system was constructed by modifying a commercial plated wire memory system to operate with laminated ferrite arrays. To provide flexibility for the testing of the laminated ferrite memory, an exerciser has been constructed to automatically control the loading and recirculation of arbitrary size checkerboard patterns of ONE's and ZERO's and to display the patterns of stored information on a CRT screen.

During the final check out of the memory system, an accidental burnout occurred which caused major damage to both the exerciser and the feasibility model memory and prevented completion of the work.

A proposal for the repair of the feasibility model memory system and the memory exerciser, and completion of the contract work was submitted.

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1.0 INTRODUCTION

The goal of the program was to improve the yield and reproducibility of the processes involved in the fabrication of laminated ferrite arrays so that production of the approximately 2000 arrays required for a 10^7 bit memory would be feasible.

The work on the laminated ferrite memory project was divided into two major areas: (1) process improvement, and (2) fabrication of the feasibility model memory. A number of processes are involved in the fabrication of laminated ferrite memory arrays. To insure that arrays can be fabricated with a high yield and with reproducible mechanical and electrical characteristics, the individual processes must be understood. Also, the interaction effects produced by a variation in one process on the product of other processes must be determined to establish the controls required to obtain reproducible arrays. As an illustration of this interaction, when the binder-to-powder volume ratio is increased, the shrinkage of the ferrite will also increase. This requires that the shrinkage of the conductors be increased to prevent mechanical distortion and cracking of fired arrays.

A purchased plated wire memory was modified to allow the use of laminated ferrite arrays in place of the plated wire storage elements, to form a feasibility model memory to demonstrate the operating characteristics of a laminated ferrite array memory.

The work on process improvements concentrated on investigating basic interactions between process steps and the characteristics of the ferrite components of the arrays. This work has included investigation of

the factors influencing (1) the flow characteristics of the ferrite sheets, (2) the shrinkage of the ferrite when fired, (3) the distortion of arrays when fired, and (4) the quality of the bond between laminae.

To provide flexibility for the testing of the laminated ferrite memory, an exerciser has been constructed to automatically control the loading and recirculation of arbitrary size checkerboard patterns of ONE's and ZERO's and to display the patterns of stored information on a CRT screen.

2.0 WORK REQUIREMENTS

Work Requirements

The work called for under this contract was divided into three areas:

- (1) A system study to identify the functional characteristics of a mass storage system using laminated ferrite arrays,
- (2) Further development of the processing technology involved in fabricating laminated ferrite arrays including lamination, embossing, insulation, thickness control and process control, and
- (3) Fabrication of a feasibility model laminated ferrite memory consisting of address register, diodes, array drivers, and two laminated ferrite arrays having a combined capacity of 512 words of 32 bit length. The major effort was to be concentrated on the last two areas.

3.0 SUMMARY

A study of the effect of multi-word addressing, under the restrictions imposed by laminated ferrite arrays, on the number of components and the power consumption showed that both could be reduced by accessing more than one word per address selection for memories having capacities between 10^6 bits and 16 words. The optimum number of words per address was found to be dependent upon the memory size, circuit design of the current drivers and sense amplifiers, and the relative weighting of reliability (number of components) and power consumption.

The processes involved in the fabrication of the laminated ferrite arrays were investigated to determine the factors which affect the quality of the arrays. The effects of process variations were determined by fabricating arrays incorporating these process variations and evaluating the results. During this project 78 arrays were fabricated. As a result of these investigations a number of the processes were modified to improve the array quality. It was noted during these investigations, that the undisturbed and disturbed sense signal amplitude of some arrays was more than double that normally obtained. An investigation into the cause of this increased signal amplitude failed to isolate the cause of this anomalous behavior.

A feasibility model memory was constructed by modifying a purchased plated wire memory system to operate using the laminated ferrite arrays as the storage medium. In addition, a memory exerciser was designed and built to control the operation of the memory under three basic program modes, and

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to display the memory contents on a CRT screen. The combination of the memory exerciser and the feasibility model memory was also intended to be used as a test instrument to completely test individual arrays.

During the final check out of the memory an accident occurred which applied 110V AC to the +5V supply bus of the exerciser and memory, and caused extensive damage in both units. An assessment of the damage and an estimate of the cost to repair and retest the units was made. The units could not be repaired and the contract work completed within the authorize contract funds, therefore a proposal for repairing the units and completing the contract work was prepared and submitted.

4.0 LAMINATED FERRITE MEMORY DEVELOPMENT

4.1 System Study

4.1.1 Functional Characteristics of Laminated Memory System

The laminated ferrite memory arrays have been designed for use in 2-conductor word organized (linear select) random access memory systems operated in a 2 crossover per bit mode. Previous work^[1] indicated that an array size of 260 x 70 conductors was the preferred size for space memory system applications and that a maximum length of 2040 words be used for the digit/sense conductors. This size array allows for 256 32-bit words per array with 14 spare word lines and four spare bits per word.

The minimization of power dissipation and the number of components are important considerations in space applications where power conservation and high reliability are prime requirements. The laminated ferrite arrays are ideally suited for low power systems because of their low drive current requirements which are under 150 mA for the read and write currents and 25 mA for the digit currents. These low currents are easily obtained from commercially available integrated circuits which minimizes the number of components, and are easily steered by low current IC switches which is in the direction of reducing power. The power consumption of the associated logic and decoding circuits can be negligibly low with available MOS IC's, especially COS/MOS. Therefore, the major sources of power consumption are the drivers/current steering switches and the sense amplifiers. The use of

[1] "Laminated Ferrite Memory System," Aug. 1968, Contract No. NAS1-7084. Also available as NASA CR-666636.

a modified 2-1/2 D memory organization can be used to minimize both the power consumption and the number of components. In this modified 2-1/2 D organization multiple words are accessed by each address selection. Since the laminated arrays use destructive read out, the unselected words are rewritten unchanged. The word in the selected address is read and either rewritten or a new word is written according to whether a restore or write command is to be executed. The reduction in power and number of components is shown in Figs. 1 and 2 for a 10^6 bit memory and a 10^6 word memory respectively. For the 10^6 bit memory it is seen that minimum power occurs for two words per address and the number of components is decreased to one fourth and reduction in total power is still half of the reduction obtained for two words per address. For the 10^6 word memory both total power and number of components continue to decrease past 16 words per address. One other significant fact that can be deduced from a comparison of these data is that forming the large capacity memory by combining 32 modules of 10^6 bit size, would result in more than a factor of 4 increase in both the power consumption and the number of components as can be seen by a comparison of the last two columns in Table I.

In practice, the choice of the number of words per address to be used in a specific design will be determined by the memory size, power dissipation of the drivers/switches and sense amplifiers, and the relative importance between power conservation and reliability.

4.2 Array Processing Technology Development

In a previous contract [2] the feasibility of fabricating laminated ferrite arrays which operate using low read, write and digit currents was demonstrated. The technology development work conducted under this con-

[2] "Development of a Monolithic Ferrite Memory Array," Heckler, C.H. and Bhiwandker, N.C., Contract No. NAS1-8170. Also available as NASA CR-2152.

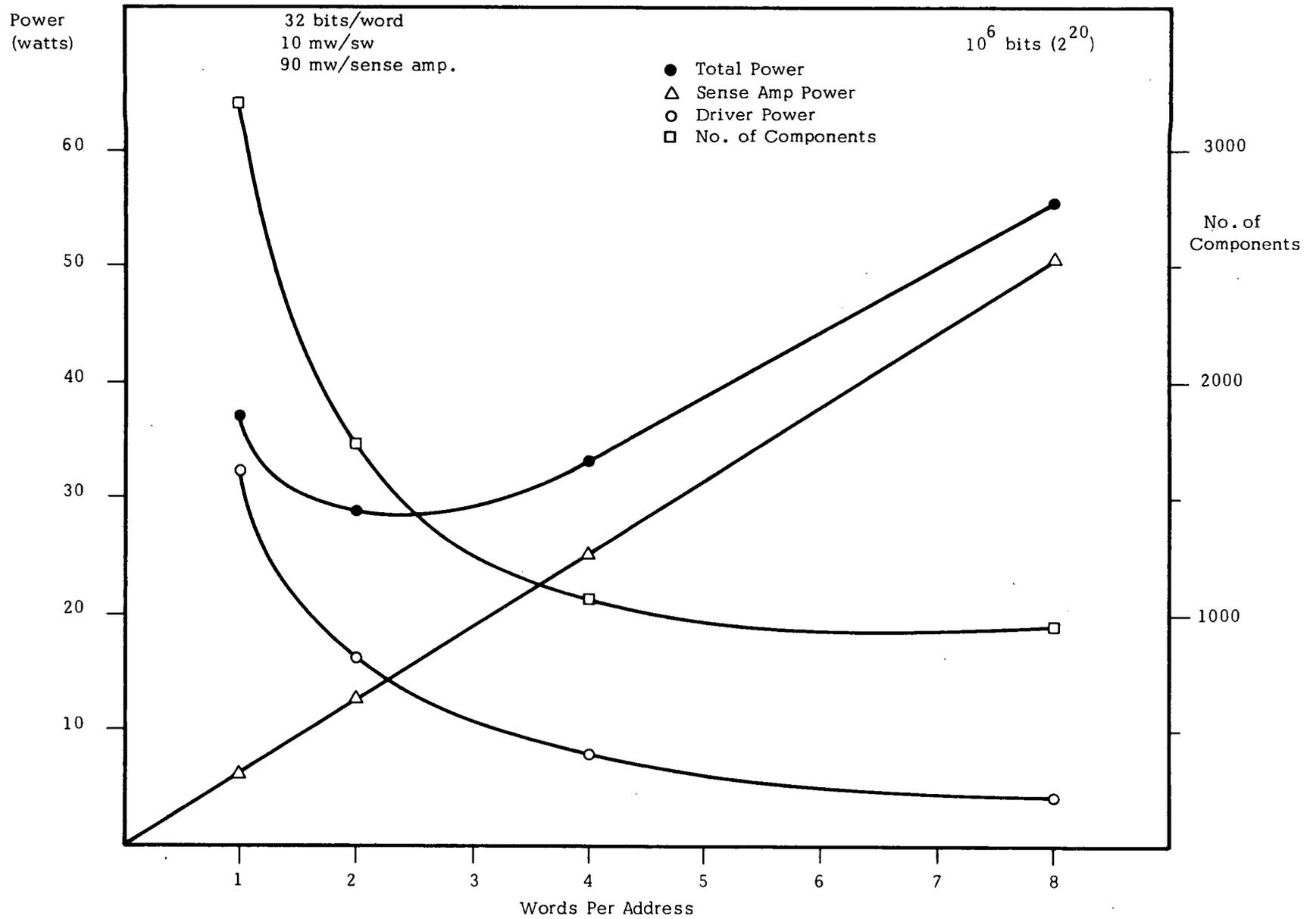


Fig. 1 Power Dissipation vs. No. of Words Per Address: 10⁶ Bits

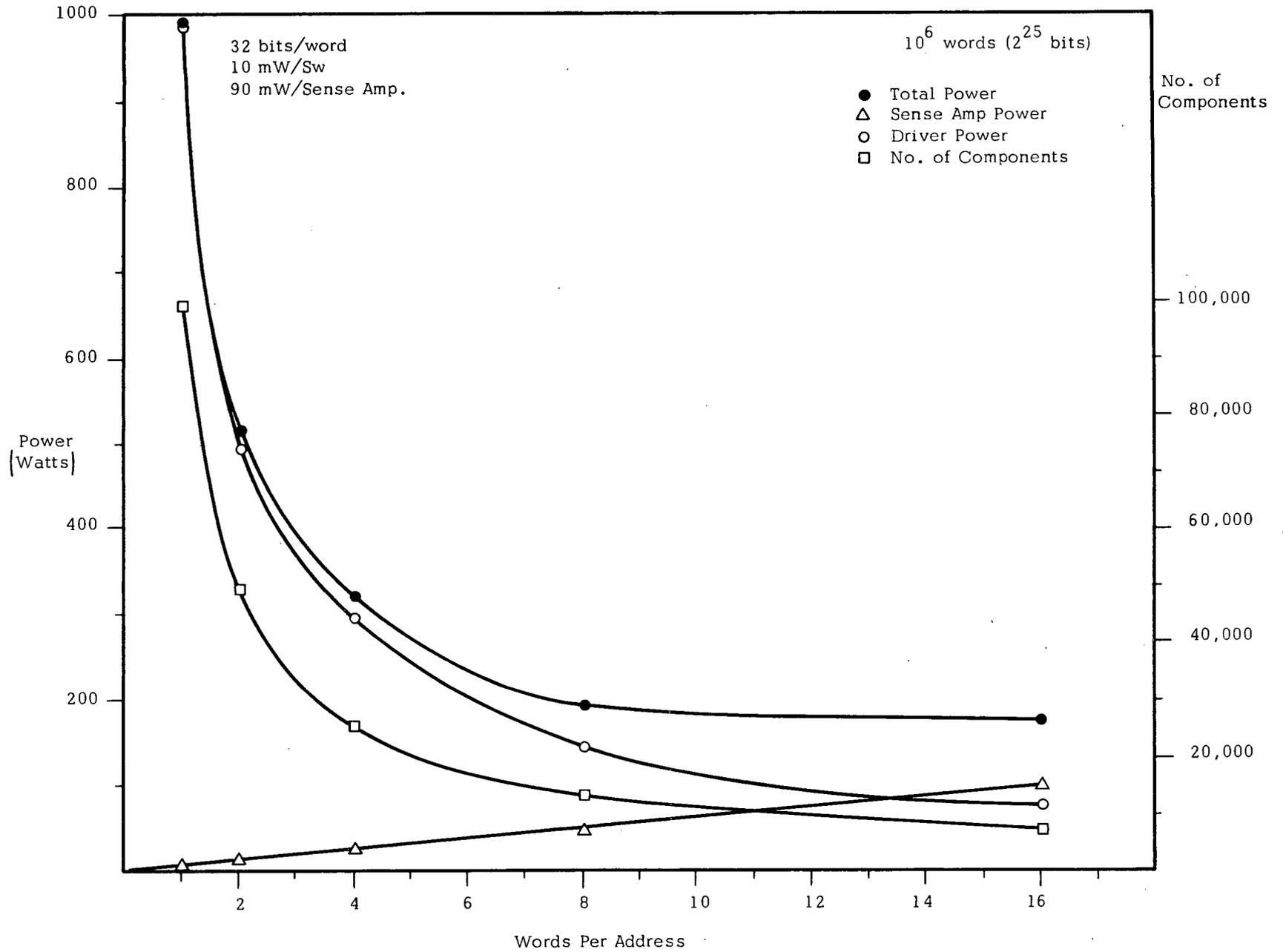


Fig. 2 Power Dissipation vs. No. of Words Per Address: 10^6 Bits

tract was directed toward determination and control of those variables in the process which alter the array characteristics, and toward improvement of the process to increase yield and/or improve characteristics. This work was carried out by investigating the individual process steps involved in the fabrication of the laminated ferrite arrays. In the course of these investigations, 78 partially populated and full populated arrays were fabricated to evaluate the effects of changes made in the process.

Table I Summary of Power Requirements and Number of Components

	10^6 bits (2 Words/Address)	10^6 Words (8 Words/Address)	10^6 Words (32 10^6 Modules)
Total Power Consumption	29 W	200 W	935 W
Number of Components	1690	12,970	54,080

4.2.1 Embossing

In the fabrication of arrays the word and digit/sense laminae are embossed to form channels 152.4 mm (0.006 in.) wide^[3], which are on 381.0 mm (0.015 in.) centers and 63.5 mm (0.0025 in.) deep preparatory to inserting the conductors. The quality of the embossed pattern affects the positioning of the conductors and the quality of the bond in the subsequent laminating step and 63.5 mm (0.0025 in) deep preparatory to inserting the conductors. The quality of the embossed pattern affects the positioning of the conductors and the quality of the bond in the subsequent laminating step.

A number of factors have been determined to affect the quality of the embossing of the green state laminae. These are: calcining temperature, binder content, embossing temperature, pressure and number of cycles of application of the pressure. The sensitivity of embossing quality to calcining temperature and to binder content was determined in the previous contract. However, since these two parameters also affect other array properties, in these experiments, they were treated as dependent variables. The experiments, which were related to the embossing process, were restricted to those involving variations of temperature, pressure and the number of pressure cycles.

The process as originally developed resulted in a variability in the shape of the embossed channel pattern. The ranges of temperature and pressure, over which embossing may be accomplished, is narrow. At the higher temperatures and pressures, the laminae sticks to the embossing mold and/or backing sheet of 25.4 mm (0.001 in) thick teflon. At the lower temperatures and/or pressures, the material does not flow sufficiently

[3] English units were used in all dimensional measurements during this project.

to give acceptable quality embossing. The use of release agents was attempted to eliminate the sticking at the higher temperatures and pressures. The characteristics required of the release agent are very restrictive in order to not affect either the subsequent laminating process and/or the magnetic characteristics of the arrays. These problems occur due to the unavoidable transfer of release agent from the mold and the teflon backing sheet to the laminae during embossing. A release agent with the necessary properties was not found, therefore alternate methods of improving the quality of embossing were investigated. The method developed to eliminate the variability in embossing quality was to apply a number of pressure cycles. It was determined that four cycles were required to obtain good reproducible quality embossed channel patterns. The embossing process as modified consists of placing the mold with lamina and teflon backing sheet between heated platens of a Carver hydraulic laboratory press. A 20 minute temperature stabilization period is used to bring the mold to the temperature of the platens, 46°C. A force of 2270 kg (5000 lbs) is then applied for three minutes, after which the pressure is released and the mold rotated 90 degrees. The pressure is reapplied for three additional cycles with a 90 degree rotation of the mold between each cycle. This procedure allows a slightly lower temperature to be used for the embossing.

4.2.2 Lamina Thickness Control

The work on improving the process for preparing the laminae was divided into two areas: (1) improvement of the uniformity of laminae thickness, and (2) improvement in the process for forming the thin center lamina.

The process for preparation of the word and digit/sense laminae developed previously consisted of first mixing the polyvinyl chloride binder with the ferrite powder on a calender material. This material was cut into strips and pressed to the desired thickness on a Carver hydraulic press using precision spacers to control the thickness of the ferrite sheets. The major

problem associated with this process was the uniformity of the thickness over a sheet. The original tolerance, that the sheets were made to, was $\pm 5 \mu\text{m}$ (± 0.0002 in.). This resulted in a bonding problem during lamination as, in a worst case where the peaks and valleys of the word and digit/sense laminae align, the separation of laminae as measured between the valleys, is of the same order of magnitude as the thickness of the center lamina. The process for preparing ferrite sheets has been refined to control the thickness of both the word and digit/sense laminae to $\pm 2.5 \mu\text{m}$ (± 0.0001 in.). This has been accomplished by controlling the thickness of the calendered sheets, control of the lateral separation between the precision spacers, and a programmed application of pressure.

The thickness of the calendered sheets is controlled to $275 \mu\text{m}$ $\pm 25 \mu\text{m}$ (0.011 in. ± 0.001 in.) to limit the amount of flow in the final pressing. Strips 25 mm x 200 mm (1 in. x 4 in.) are cut from the calendered sheets and centered on the bottom platen between two precision spacers. The separation between the spacers is maintained at $200 \mu\text{m}$ (4 in.) and the platen temperature is controlled at 148°C . Teflon sheets $25 \mu\text{m}$ (0.001 in.) thick are placed between the platen and the ferrite strip to prevent sticking during the pressing.

The pressure is applied in a 4-step program to reduce the thickness to $107.5 \mu\text{m}$ (0.0043 in.) for digit/sense sheets and $157.5 \mu\text{m}$ (0.0063 in.) for word sheets. Initially 1370 kg (3000 lb) of force is applied for one minute. This is followed by 2740 kg (6000 lb) for one minute and then 3650 kg (8000 lb) for three minutes. In the final step a force of 4540 kg (10,000 lb) is applied for five minutes.

The process for preparation of the thin center sheet developed previously was to form a casting slurry of the ferrite powder and binder by diluting with toluene and doctor-blade sheets on a glass substrate. After drying, the sheets were removed by scraping with a microtome blade.

A number of experiments were conducted to find an alternate process. The approach attempted was to initially cast a thin film of a water soluble material and then doctor-blade the thin ferrite sheet on top. After drying, the ferrite sheet was dissolved by soaking the soluble film in water. This process was attempted using polyvinyl alcohol (PVA) to form the water soluble film with only partial success. One problem with this process was that the solubility of PVA in water was too low so that soaking times in excess of 16 hours were required to obtain release. Attempts to modify the process to decrease the time required to obtain release of the thin ferrite sheets were unsuccessful.

Other problems were that the thin ferrite sheets wrinkled after soaking in water for 16 hours, and there was a greater tendency to form pin holes in the ferrite sheets probably because the surface of the PVA film was not as smooth as the glass substrate.

The number of materials available for use with this process was severely restricted by the dual requirements that the solvent used in the ferrite casting slurry not dissolve the release material, and the solvent used to dissolve the release material not dissolve the ferrite sheet. PVA was the best of the materials found to be a candidate for this process but it was not usable, therefore the previously developed process was retained for the preparation of the thin center sheets.

4.2.3 Lamination

The process of thermobonding the three laminae to form the arrays is a central process requiring a proper balance between temperature and pressure. With too low a temperature, or too low a pressure, an effective bond will not be obtained. Too high a temperature or too high a pressure will cause shorting between word and digit/sense conductors and will produce distortion in the array as a result of excessive flow. The bonding obtained with the process developed in the previous contract was good everywhere

except around the edges. This factor was attributed to the tolerance to which the thickness of the sheets was held and the manner in which the thickness varied. These pressed sheets were thickest in the center and thinnest along the edges. The major improvement in the laminating process implemented under this contract has been the decreasing of the tolerance on the uniformity of thickness in the laminae from $\pm 5 \mu\text{m}$ (± 0.0002 in.) to $\pm 2.5 \mu\text{m}$ (± 0.0001 in.). The process previously developed consisted of assembling the three laminae in an alignment jig between teflon release sheets. A pressure of 548 g/cm^2 (8 lb/in^2) was applied and the array was heated for 1 hr. at 160°C , the first 10 minutes in vacuum and the remainder in air.

With the availability of laminae having a more uniform thickness, the pressure has been lowered to 440 g/cm^2 (6.25 lb/in^2) and the heating cycle was modified.

An initial heating to 120°C at a pressure of 9.5 g/cm^2 ($.134 \text{ lb/in}^2$) is used to form a partial bond between the three laminae. The array is then removed from the alignment fixture, weights are placed on top of the array to exert a pressure of 440 g/cm^2 (6.25 lb/in^2) and the assembly is placed in a vacuum oven and heated. At 80°C the chamber is evacuated for 5 minutes after which air is admitted and the temperature is raised to 150°C for 1 hour. The array is oven cooled to room temperature and removed.

Physical inspection of the bonds obtained using this process indicate a good bond throughout the arrays. However, the final criteria of the quality of the bond is the uniformity of the magnetic characteristics at each of the 18,900 crossovers. A memory exerciser was designed and built to test the arrays under operating conditions. Unfortunately, a major burn-out of the tester and memory occurred before this data could be obtained.

4.2.4 Processing Control

During the course of the work on this program to improve the processes used in the fabrication of laminated ferrite arrays it was found that the amplitude of the undisturbed and disturbed sense signals in some arrays was more than twice the normal signal and was not correlatable with variations in the fabrication process. This finding focused on the firing cycle as the probable source of signal variations. Toroidal samples were co-fired with the arrays and tested in an attempt to find a correlation between the increased signal output and the measured toroid characteristics. An apparent correlation between the B-H loop characteristics of the control toroids and the high sense signal output of the arrays was observed which indicated a possible variation in the firing atmosphere. A series of tests were initiated to determine (1) that the arrays and the control toroids were receiving the same atmosphere during firing and (2) that the firing atmosphere determines the magnitude of the sense signal output.

The question of the array and toroids receiving different atmospheres was raised by the fact that the arrays are fired between two alumina setter plates spaced $500 \pm 25 \mu\text{m}$ (0.020 ± 0.001 in) apart to prevent their warping and the control toroids are placed on top of the top setter plate.

Because the magnetic characterization of interest could not be determined from testing the arrays special toroids were prepared which were the same thickness as the array. So that the environment for these toroids would be the same as that for the arrays, ferrite sheets the same dimensions as the arrays were prepared and 4.6 mm (0.185 in.) diameter holes were punched in the sheets. Toroids, 2.8 mm (0.115 in.) OD were placed in these holes for the series of experimental firings. Analysis of the magnetic characteristics of fired toroids established that there was a significant difference between the atmosphere environment of the arrays and test toroids placed on top of the top setter plate. The analysis also showed that the

effect on the magnetic characteristics due to variations of flow rate and of changes in the atmosphere during cooling from N_2 to O_2 was less pronounced in toroid samples fired between the setter plates than those fired on top.

This low sensitivity to changes in the cooling atmosphere for units fired between setter plates eliminated the possibility that the variation in the atmosphere that normally occurs from firing to firing, caused the increased amplitude of the sense signal observed in some of the arrays.

The reason for this anomalous behavior of some laminated ferrite arrays is not presently known. Understanding the origin of this effect has been hampered by the lack of a model that adequately describes the switching around the intersections of the arrays. This switching differs from that in the more conventional toroid in that it involves a rotation of the magnetization vector rather than 180° reversal. NO effort was expended toward developing a model of switching in arrays under this contract.

4.2.5 Conductor Resistance

The resistance of the pt-pd-Au alloy conductors embedded in the arrays is 1.18 ohms per cm. The resistance of these conductors would be reduced to less than 20% of this value if their density could be increased to 100% theoretical density. One benefit from such a reduction in resistance of the digit/sense conductors would be a reduction of the signal attenuation. This would increase the number of words that could be connected to the sense amplifiers and therefore decrease the required number of sense amplifiers. Another benefit would be a reduction in power dissipation and a reduction in joule heating.

One method of achieving a higher conductor density is to alter the alloy composition to obtain a melting temperature closer to the firing temperature used to sinter the arrays. Since the alloy, DP8283, is proprietary with E.I. duPont the percentages of pt, pd and gold used are not known. However, the melting point of this alloy is greater than $1500^\circ C$, which is the maximum firing temperature specified by duPont.

The melting points of binary alloys of Au-Pt and Au-Pd, as compiled by Hansen^[4], are shown in Fig. 3. These mixtures do not have definite melting points, therefore the liquids and solidus are given. It is seen from these curves that if the platinum-metal-group constituent of the alloy is palladium, 80 weight percent of gold is required to reach the solidus at the array firing temperature. This compares to 40 weight percent of Au if the platinum-metal-group constituent is platinum. For the ternary alloy, an intermediate weight percent of gold would be required. From these curves and the known maximum firing temperature of the alloy it is seen that the maximum amount of gold is between 40% - 60% depending on the pt/pd ratio.

The method used to vary the composition was to gold plate the conductors which were prepared by the normal method, viz. doctor blading sheets from the DP 8283 conductor paste, bisque firing to 855°C and die punching conductors 0.055 mm x 0.125 mm x 100 mm (0.0022 in x 0.005 in x 4.0 in.).

Using this method, conductors were prepared having from 24% to 70% by weight of gold added. The results are summarized in Table 2. For 60% greater additions of Au the melting point was below 1350°C and the conductors melted. Between additions of 47% and 58% the resistance was reduced by 36%. However, the reduced value of resistance obtainable was about 4 times the resistance calculated for pt or pd conductors of 100% density. It was concluded that increasing the gold content of this alloy will not result in the desired reduction in conductor resistance.

[4] "Constitution of Binary Alloys," Max Hansen, 2nd ed. McGraw-Hill Book Co. Inc. N. Y., 1958, p. 224 and p. 227.

4.3 Feasibility Model

The feasibility model memory was built to demonstrate the operation of the laminated ferrite memory arrays in an operating memory system. As the major purpose of the feasibility model was the demonstration of operation of laminated ferrite arrays rather than the optimization of the design of a memory system, a commercial memory was purchased and modified to operate with the laminated ferrite arrays fabricated under this program. In addition to the demonstration function of this model, it was desired to use the memory to test all bit locations of the arrays. An automatic memory exerciser was designed and built to operate in conjunction with the memory to permit testing of the arrays under actual operating conditions.

Table 2 Conductor Resistance Vs. Wt. % Au

Wt. % Au Added	Conductor Cross-Section ($\mu\text{m} \times \mu\text{m}$)	Conductor Resistance per Unit Length Ω/cm
0	55 x 125	1.22
24	"	1.29
47	"	0.76
58	"	0.85
60	"	Melted

The memory that was purchased to fulfill these objectives was a Nemonic Data Systems, Inc. model 1K x 32 NM-5132 plated wire memory system. This memory contained most of the logic required for operation of the laminated ferrite arrays. In addition, most of the circuits exceeded

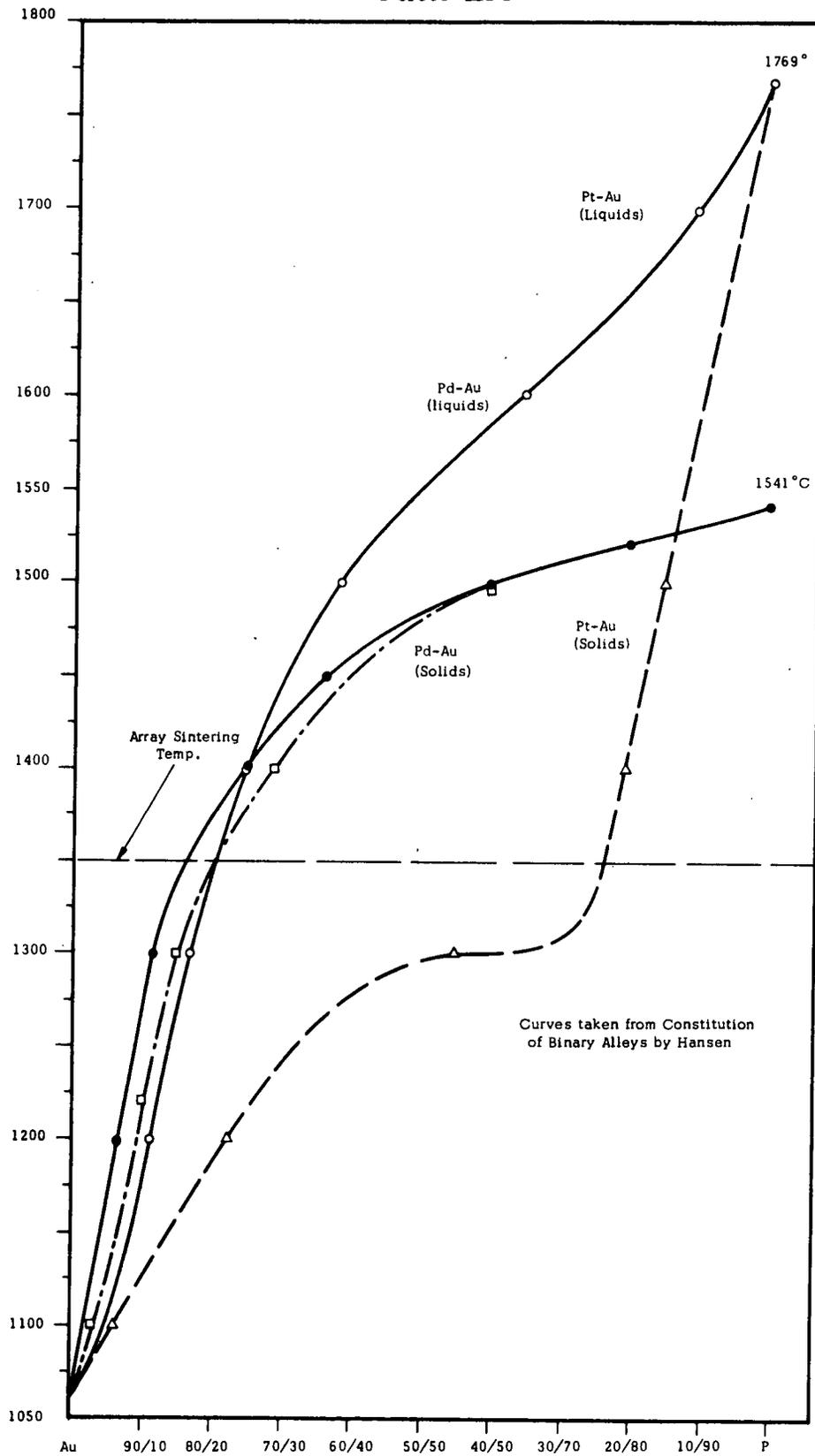


Fig. 3 Transition Temperatures of Pt-Au and Pd-Au Alloys

the requirements for interfacing with the laminated ferrite arrays. The logic changes that were required involved the combining of the data read and data write phases into a single memory cycle, and modification of the data path logic to provide rewriting after read since a destructive read-out is used with the laminated ferrite arrays. The major circuit changes required involved the addition of a second word selection matrix and associated drivers for the write phase of the memory cycle since operation of the plated wire required only a single polarity word current which was used for both the read and write operations. To accomplish the logic modifications and the circuit additions, the memory system was expanded from 6 to 11 plug in cards. Three of the additional cards, for the expanded selection matrix, were purchased from Nemonic Data Systems, the other two cards were specially fabricated to affect the timing and control logic changes.

A block diagram of the modified feasibility model memory is shown in Fig. 4. The modification of the data path to control, via the data gates, the transfer of either the contents of the output register or input data into the input register is shown in this figure. A block diagram of the modified address selection logic for a read/write cycle is shown in Fig. 5. This logic took maximum use of the available Nemonic Data Systems circuits to accomplish the modification. In Fig. 6, the modified read/write circuits are shown for accessing 1 of 512 memory addresses.

The read and write currents were set at 130 mA and 100 mA respectively by changing the current limiting resistor in the current generator circuit from 16 Ω to 75 Ω for read and 110 Ω for write.

The digit driver circuits were modified to extend the pulse width of the digit current pulses and to decrease the digit current to 20 mA. The modified digit circuits are shown in Fig. 7. The original logic which provided

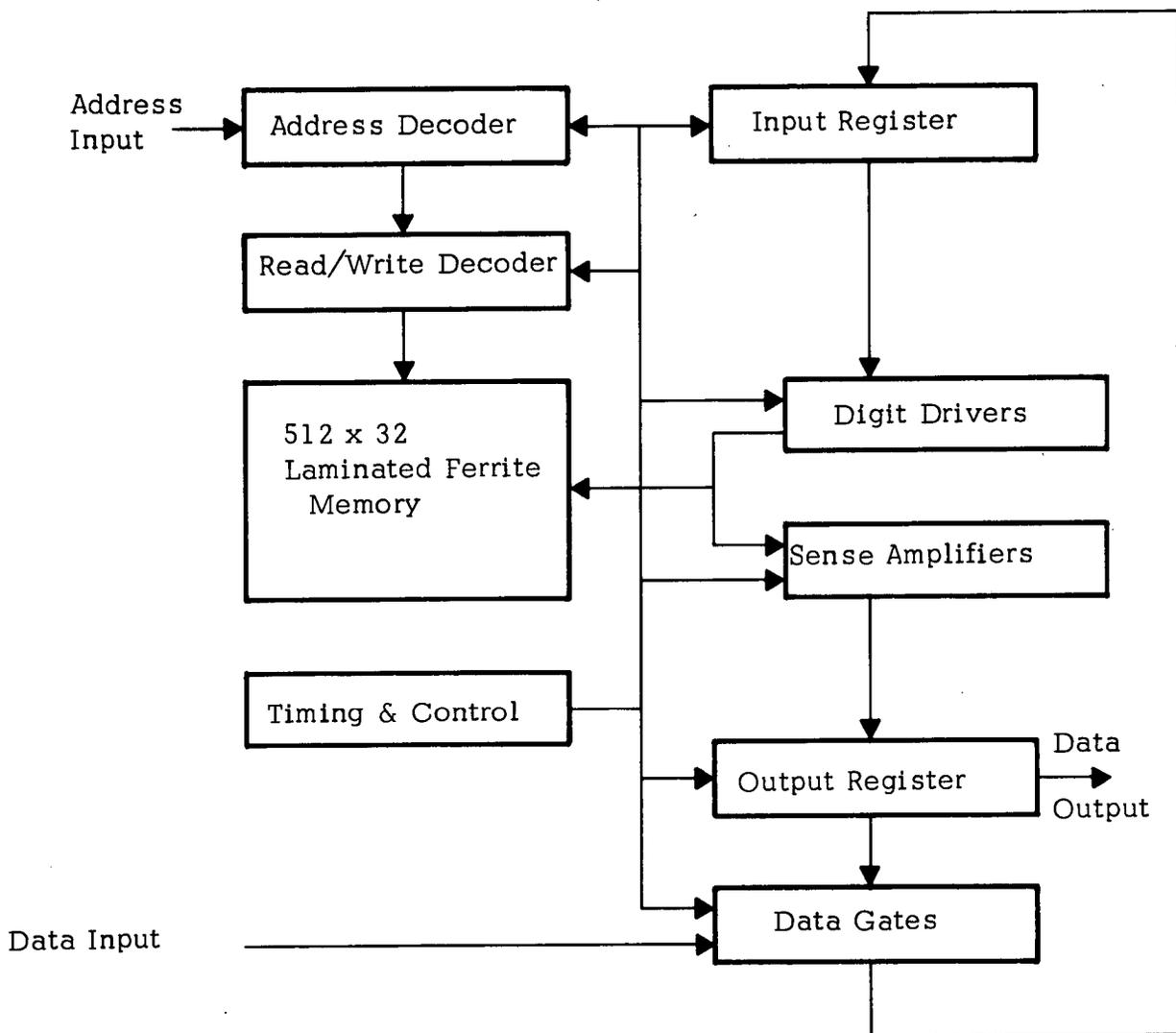


Fig. 4 Block Diagram - Laminated Ferrite Feasibility Model Memory System

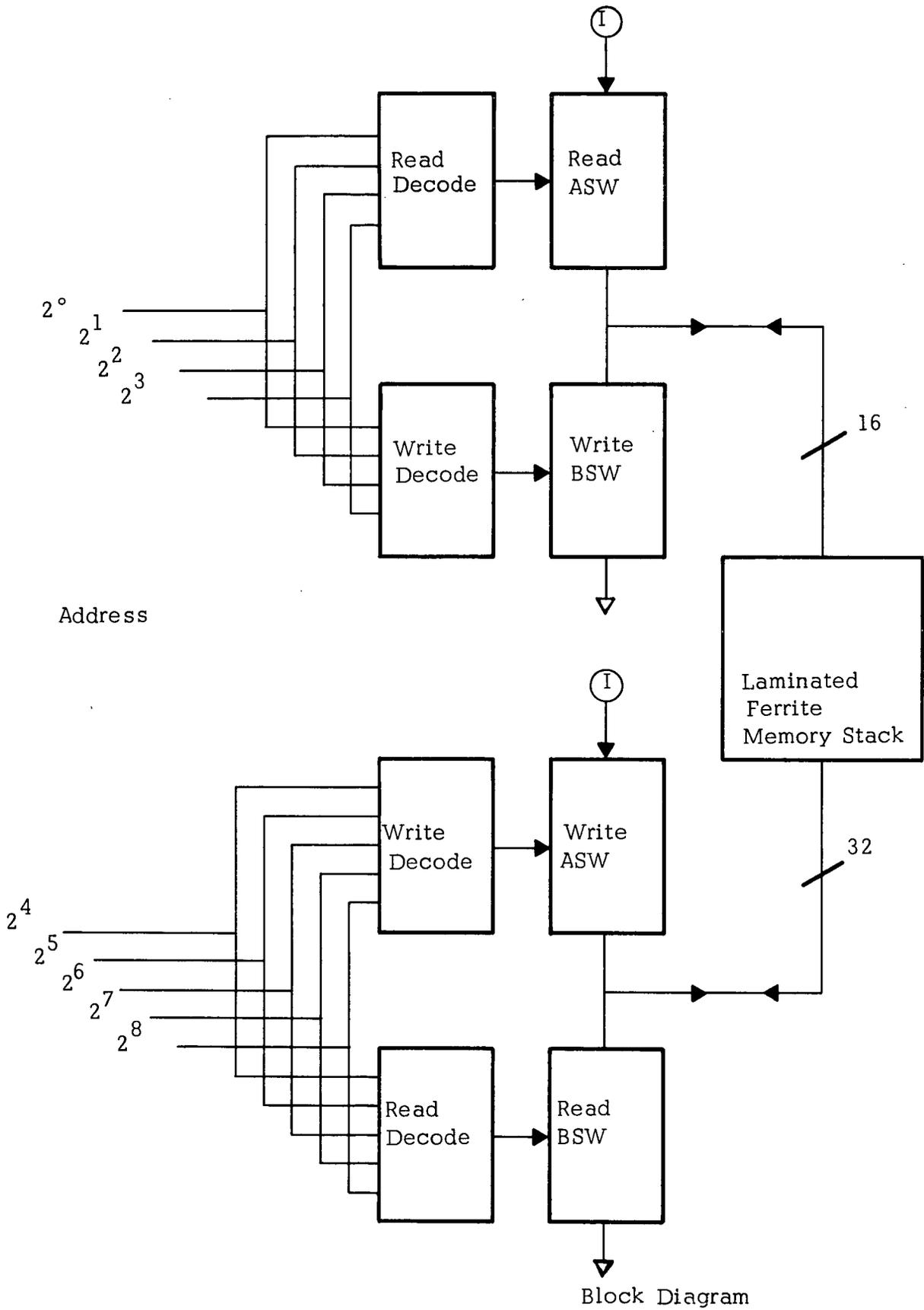


Fig. 5 Modified Address Selection for Read/Write Cycle

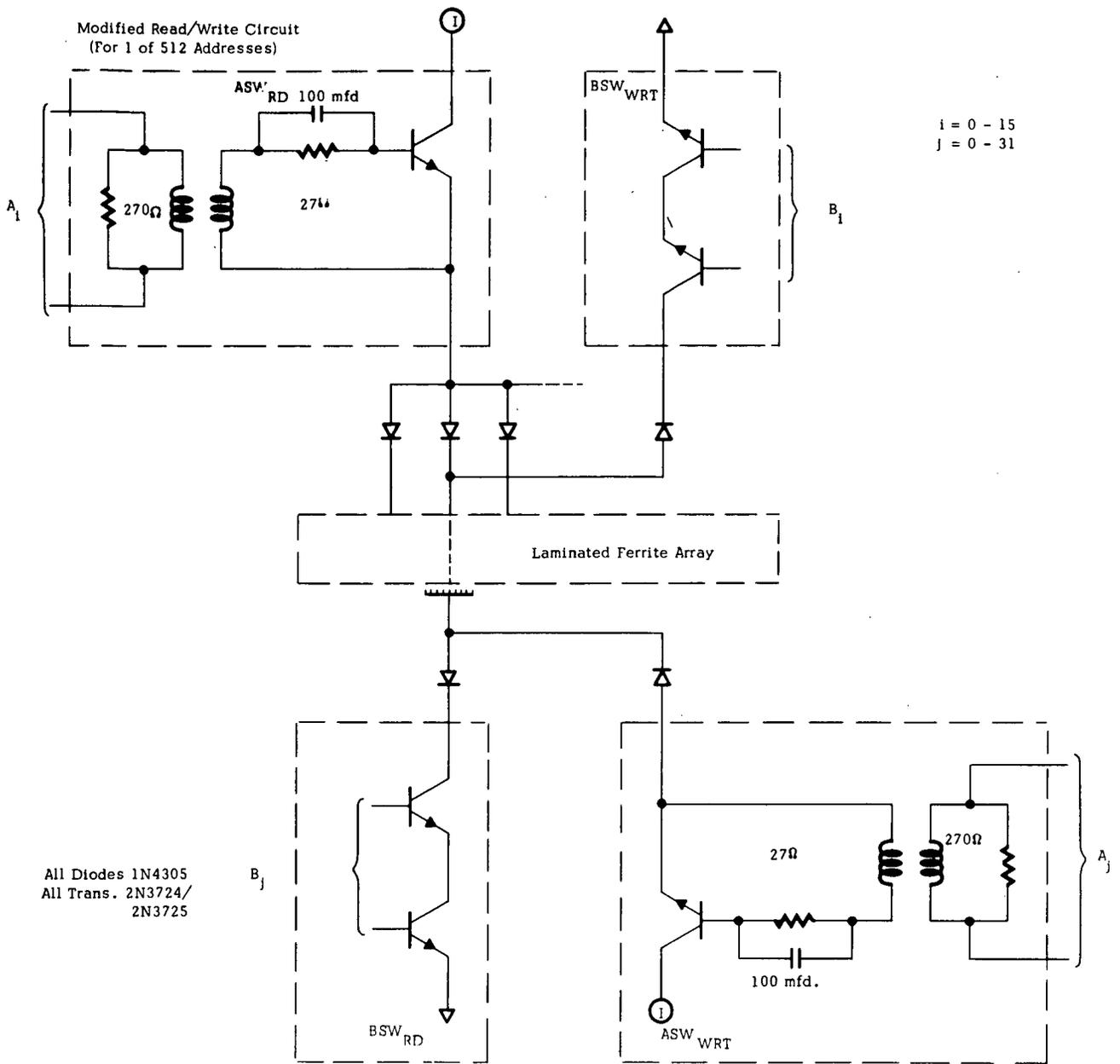


Fig. 6 Modified Read/Write Circuit

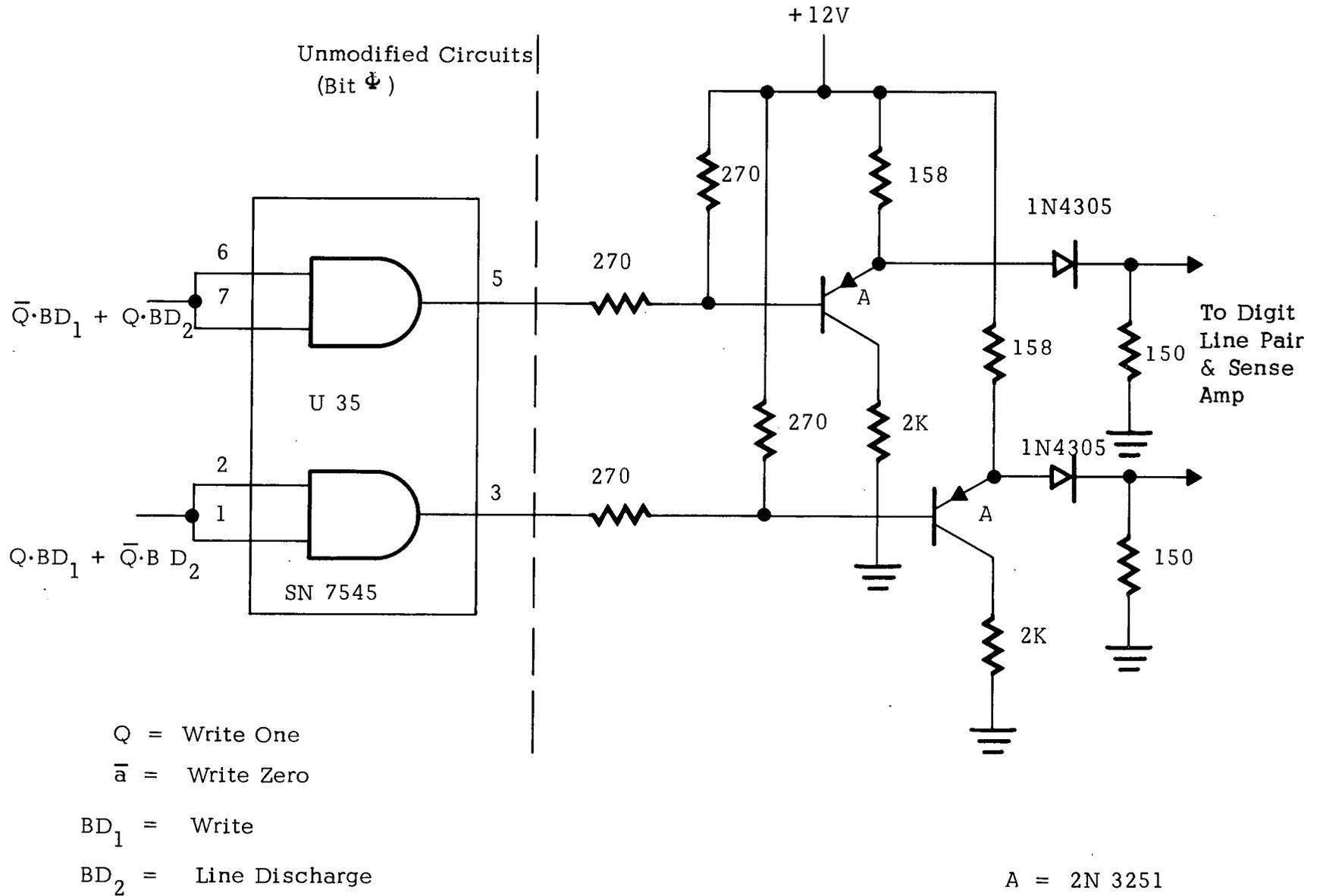


Fig. 7 Digit Driver Circuits

a line discharging pulse following the digit write operation was retained. This is controlled by complementing the Q function following digit write.

The block diagram for the exerciser is shown in Fig. 8. The logic functions provided by the exerciser are: (1) the address counter which steps the address sequentially from 1 through 512, (2) the bit counter used to initially set information into the memory and to control the shifting of the shift register for the display output to a CRT, (3) the pattern counter used to control the size of the checkerboard pattern, (4) the shift register used for display of stored data and the horizontal shifting of the checkerboard pattern and (5) the control logic used for control of the operating modes. The memory exerciser provides three basic modes of operation: a read/restore mode, a horizontal pattern shift and a vertical pattern shift. In the read/restore mode, the pattern stored in the memory is continuously read and displayed on a CRT screen. In the horizontal and vertical pattern scan modes, the pattern is continuously shifted in the indicated direction and displayed on the CRT screen. The speed of shifting of the pattern is selectable so that the pattern changes can be followed. In all three modes, the memory can be operated at full speed, i.e., without a time interval between memory cycles, or at reduced speed by triggering from an external clock.

To load the memory, the pattern size is selected and the pattern for the first word is sequentially loaded into the shift register. The full memory is then loaded by depressing the memory initiate button. After loading, the operation mode is selected and initiated by again depressing the memory initiate button.

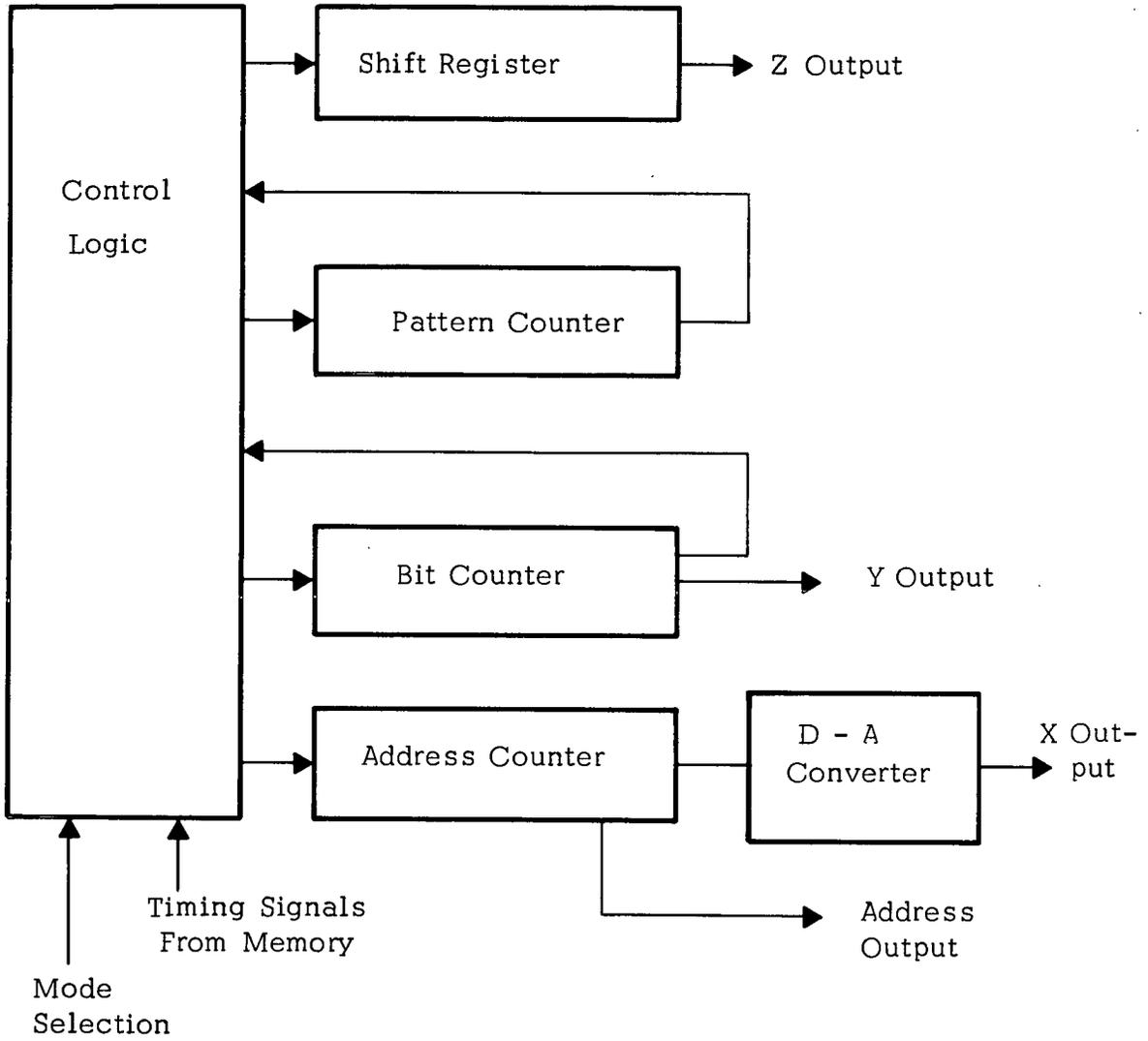


Fig. 8 Block Diagram - Memory Exerciser

5.0 CONCLUSIONS AND RECOMMENDATIONS

The study on the effect of using multi word addressing with laminated ferrite arrays showed that both a reduction in the number of components and a reduction in power consumption is obtained for memory capacities between 10^6 bits and 10^6 words. The optimum number of words per address for a given system design depends on memory size, circuit design of drivers and sense amplifiers and the relative weighting of reliability (number of components) and power consumption.

The investigation into the effect of variations in the processing steps have resulted in a number of process modifications that have improved the quality of the arrays. Two problems for which the investigation did not result in a solution are the development of an improved method for fabricating the $17 \mu\text{m}$ (.0007 in.) center lamina and the isolation of the factors which produce the anomalous high sense signal output observed in some arrays. The characteristics of the thin center lamina are important in that the range of conditions for obtaining acceptable laminating is determined in a large degree by the characteristics of the center lamina and the present range is narrow. The desirability of obtaining a larger output signal is self evident in that detection would be easier or lower drive currents could be used to obtain the same output signal level.

A feasibility model laminated ferrite memory system was constructed by modifying a commercial plated wire memory system to operate with laminated ferrite arrays. In addition a memory exerciser was designed and built to control the operation of the feasibility model memory and provide a con-

tinuous display of the memory contents on a CRT screen. This unit was designed to also be used for the testing of individual arrays.

During the final check out of the memory system, an accidental burnout occurred which caused major damage to both the exerciser and the feasibility model memory. The cost for repair of the damage and the completion of the contract work was determined. The damage could not be repaired and the contract work completed within the authorized contract funds. A proposal for the repair of the feasibility model memory system and the memory exerciser, and completion of the contract work was submitted.

It is recommended that the feasibility model memory system and exerciser be repaired and the contract work completed. It is also recommended that additional investigation of the array fabrication process be conducted, specifically the process for fabricating the center laminae to improve the range of temperature and pressure for laminating the arrays. An understanding of the origin of the anomolous large output signal should be obtained so that the output of all arrays could be made uniformly large. Finally, the problem of connections between the arrays and the memory system should be studied in order to reduce their cost and increase their reliability.