FINAL REPORT

for

PLATED WIRE MEMORY SUBSYSTEM

October 1972 - February 1974

Contract No.: NAS5-23163

PRICES SUBJECT TO CHANGE

Prepared by

Motorola Inc.

Government Electronics Div.

Scottsdale, Arizona

for

Goddard Space Flight Center

Greenbelt, Maryland
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October 1972 - February 1974

Contract No.: NAS5-23163

Goddard Space Flight Center

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Motorola Inc. Government Electronics Division

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for

Goddard Space Flight Center

Greenbelt, Maryland

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SECTION 1

INTRODUCTION AND OVERALL PROGRAM SUMMARY

1. INTRODUCTION

This Final Engineering Report documents the overall activity and history of the work performed by Motorola, Inc., Government Electronics Division, Scottsdale, Arizona for the Goddard Space Flight Center, Greenbelt, Maryland, under NASA Contract No. NAS5-23163. The report is submitted in accordance with the requirements of Specifications S-562-P-24 (Rev. 2) and covers the period from October 1972 to February 1974.

1.1 PROGRAM SUMMARY

The work performed under the subject contract entailed the construction and testing of a 4096 word by 18 bit random access, NDRO Plated Wire Memory for use in conjunction with a Spacecraft Input/Output Unit and Central Processing Unit.

The primary design parameters, in order of importance, were high reliability, low power, volume and weight. Two memory units, Serial No. 101 and 102, were delivered.

1.2 RESULTS ATTAINED

The memory units were subjected to comprehensive functional and environmental testing at the end-item level to verify conformance with the specified requirements. Contract modifications were necessary in some areas, either to relax the requirements or to redefine noncritical parameters. All such modifications were relatively insignificant, with the possible exception of system weight and operating power consumption.

A comparison of the memory units most significant physical and performance characteristics versus the specified requirements is shown in Table I.
<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Contract Reference</th>
<th>Specified</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volume</td>
<td>S-562-P-24 (Rev. 2)</td>
<td>160 in$^3$</td>
<td>159.45 in$^3$</td>
</tr>
<tr>
<td>Weight</td>
<td>S-562-P-24 (Rev. 2)</td>
<td>6 lbs</td>
<td>6.25 lbs.</td>
</tr>
<tr>
<td></td>
<td>Mod. 3 (7-24-73)</td>
<td>6.5 lbs</td>
<td></td>
</tr>
<tr>
<td>Power (Operate)</td>
<td>S-562-P-24 (Rev. 2)</td>
<td>6 watts</td>
<td>6.68 watts (102)</td>
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<tr>
<td></td>
<td>Mod. 3 (7-24-73)</td>
<td>7 watts</td>
<td>6.29 watts (101)</td>
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<tr>
<td>Power (Standby)</td>
<td>S-562-P-24 (Rev. 2)</td>
<td>170 milliwatts</td>
<td>130.8 mW (102)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>127.6 mW (101)</td>
</tr>
<tr>
<td>Voltage Tolerance</td>
<td>S-562-P-24 (Rev. 2)</td>
<td>±5% on all</td>
<td>±5% on all</td>
</tr>
<tr>
<td>Operating Rate</td>
<td>S-562-P-24 (Rev. 2)</td>
<td>500 kHz</td>
<td>&gt;600 kHz</td>
</tr>
<tr>
<td></td>
<td>Mod. 2 (3-16-73)</td>
<td>600 kHz</td>
<td></td>
</tr>
<tr>
<td>Access Time</td>
<td>S-562-P-24 (Rev. 2)</td>
<td>500 nanoseconds</td>
<td>&lt;500 nanoseconds</td>
</tr>
<tr>
<td>Operating Temp.</td>
<td>S-562-P-24 (Rev. 2)</td>
<td>-40°C to +85°C</td>
<td>Tested from -40°C to +85°C</td>
</tr>
<tr>
<td>Operating Vacuum</td>
<td>S-562-P-24 (Rev. 2)</td>
<td>One Atm. to 10$^{-6}$ mm Hg.</td>
<td>Tested from one Atm. to 10$^{-5}$ mm Hg. (Modified for test purposes)</td>
</tr>
<tr>
<td></td>
<td>Mod. 3 (7-24-73)</td>
<td>One Atm. to 10$^{-5}$ mm Hg.</td>
<td></td>
</tr>
<tr>
<td>Operating Vibration</td>
<td>S-562-P-24 (Rev. 2)</td>
<td>Sinusoidal: 5-25 Hz, 0.5 in DA 25-110 Hz, 15 g Peak 110-2000 Hz, 7.5g Peak Two Octaves/Minute Random: 15 Hz, 0.01g$^2$/Hz 15-70 Hz, Linear Increase 70-100 Hz,</td>
<td></td>
</tr>
<tr>
<td>Characteristic</td>
<td>Contract Reference</td>
<td>Specified</td>
<td>Measured</td>
</tr>
<tr>
<td>--------------------------------------------</td>
<td>--------------------</td>
<td>-------------------------------------------------------------------------------------------------</td>
<td>---------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Operating Vibration (Contd)</td>
<td></td>
<td>0.31g^2/Hz, 100-400 Hz, Linear Decrease, 400-2000 Hz, 0.02g^2/Hz Two Min./Axis</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Mod. 4(7-24-73)</td>
<td>Sinusoidal: 5-25 Hz, 0.33 in DA 25-110 Hz, 10g Peak 110-2000 Hz, 5g Peak Two Octaves/Minute Random: 15 Hz, 0.004g^2/Hz 15-70 Hz, Linear Increase 70-100 Hz, 0.138g^2/Hz 100-400 Hz, Linear Decrease 400-2000 Hz, 0.0089g^2/Hz</td>
<td>Tested at Mod. 4 levels</td>
</tr>
<tr>
<td>Operating Shock</td>
<td>S-562-P-24 (Rev. 2)</td>
<td>Two Shock Pulses of 30g for 6 and 12 milliseconds in three directions.</td>
<td>Tested at specified levels.</td>
</tr>
</tbody>
</table>
SECTION 2

HISTORICAL PROGRAM SUMMARY

2. PROGRAM HISTORY

The design, construction and test history, as related to the hardware requirements of this contract, is summarized in this section. The summarization is in chronological order from date of contract award to date of final delivery of the memory units. Design activity began on both units on 5 October 1972.

2.1 SERIAL NUMBER 101

Assembly was completed and testing began in April 1973. An analysis of the test results indicated that design problems were limited to the performance of the memory at voltage and temperature extremes. The unit worked over much of the design range and it was jointly decided (GSFC TWX 4 June 1973) to deliver the unit to GSFC for temporary use while the problems were analyzed and corrected in S/N 102. The unit was shipped to GSFC in June after temperature tests only. After GSFC received S/N 102, S/N 101 was returned to Motorola in August 1973 for modification and test. S/N 101 was modified with all design changes made as a result of S/N 102 testing. The unit was acceptance tested and shipped to GSFC on 7 November 1973.

The memory was again returned to Motorola on January 16, 1974, to be modified to correct the very low repetition rate problem discovered in S/N 102. Modification to correct the problem was completed, and the memory was tested and shipped on February 15, 1974.

2.2 SERIAL NUMBER 102

Assembly was completed and testing began in May 1973. During the Y-axis sine vibration test, on 6/21/73, bit errors were noted at 20 Hz, 130 Hz and 408 Hz. The unit was removed from the housing and inspected, thereby revealing broken pins on the word drive interconnect. Analysis indicated that the interconnect was too rigid to allow for deflection at the center of the electronics and plane boards.

Rigidity in the horizontal direction was reduced by cutting the printed circuit board and completing the connections with stranded, teflon insulated wire. Relative motion between the horizontal connectors is accommodated through the flexible wiring. (See Figure 2.) The unit was then retested at 8.4 G rms with no problems.
As a result of the design analysis and testing results, several design changes and performance modifications were requested and approved by GSFC (TWX dated 26 July 1973). These included the addition of Mu-metal shielding, change of interconnect board design as described, decrease of negative supply voltage from -6.9 Vdc to -6.1 Vdc, increase in allowable operating power to 7 watts and allowable weight to 6.5 pounds, and reduction of vacuum specification from $10^{-6}$ mmHg to $10^{-5}$ mmHg.

S/N 102 passed the acceptance tests and was shipped on 7/30/73.

At GSFC it was discovered that S/N 102 exhibited repeatable bit errors when operated with a low repetition rate initiate pulse. The unit was returned to Motorola on 8/21/73 where the problem was verified. It was determined that during final checkout this problem was not adequately tested. Checkout procedures were modified to fully exercise the memory.

Several design changes were made to correct the low repetition rate problem and provide more consistent memory operation. These changes included word selection circuitry bias and restore timing changes, addition of power supply decoupling capacitors on the digit drivers, and grounding methods in the memory stack. On 10/15/73, S/N 102 completed an abbreviated AT (per GSFC TWX dated 9/14/73) and was shipped to GSFC.

GSFC discovered a very low repetition rate problem (about 0.3 Hz) and returned the memory to Motorola on December 4, 1973. Analysis indicated that the voltage at the collectors of the Level 1 select transistors when both the Level 1 and Level 2 select transistors had been off for several hundred milliseconds, tended to rise to the +5 volt supply voltage due to leakage currents through the reversed biased base-emitter junctions of the Level 2 select transistors (see Figure 13).

Upon selection of particular Level 1 and Level 2 select transistor, the base-emitter capacitance couples a negative voltage pulse onto the Level 2 select lines. This negative pulse turns on unwanted Level 2 select transistors, robbing current from the addressed word line and allowing current to flow down unselected word lines. This causes a net differential signal at the sense amplifier inputs which can be of the wrong polarity, resulting in an error.

The problem was solved by providing a leakage path to ground from the Level 1 collector point to prevent that point from rising above ground potential. This was accomplished by adding sixty-four 10k ohm, 1/8 watt, carbon composition resistors; four on each side of each of eight memory planes; three by lap soldering one end of each resistor to a word select flat pack pin or PC board track and the other end of each resistor to a plated - through hole in the memory plane ground layer; one by soldering one end as above and lap soldering the other end to a ground pad. (See Memory Plane Assembly 01-P13720D included as an insert at the back of this report.) All resistors were bonded to the PC board. A modified acceptance test was performed and the memory was returned to GSFC on January 18, 1974.
SECTION 3

TECHNICAL DESCRIPTION

3. DESCRIPTION

The memory unit is shown in Figures 1 and 2. They are identified as Motorola Part Number 01-P13701D001. Serial Numbers 101 and 102.

3.1 SYSTEM CONFIGURATION

Motorola Drawing Numbers 01-P13701D, 15-P13703D, and 15-13702D (included in the engineering drawing package submitted to GSFC) completely define the end-item package in terms of size, mounting pattern, finish, etc. Drawing 69-P13705D, Interconnection Diagram, is included as an insert at the back of this report. The weight of the delivered unit was 6.25 pounds.

3.2 ELECTRICAL INTERFACE

Connectors J1 and J2 are Deutsch, Type 75020-442P, as modified and supplied by GSFC. The total memory interface is comprised of the following (Refer to Figure 3 Memory System Electrical Interface).

1. 18 Input Data Lines (to memory)
2. 16 Input Address Lines (to memory)
3. 18 Output Data Lines (from memory)
4. 1 Initiate Line (to memory)
5. 1 Read/Write Select Line (to memory)
6. 1 Read Complete Line (from memory)
7. 2 Thermistor Sensor Lines (from memory)
8. 7 Lines for -6.1V (to memory - all lines common internally)
9. 5 Lines for +5.0V (to memory - all lines common internally)
10. 12 Lines for Power and Signal Return (all lines common internally)
Figure 1. 4K x 18 Bit Plated Wire Memory System
Figure 3. Memory System Electrical Interface
The connector pin designations are as given in Table II.

All signal inputs and outputs are to, or from, TTL Series 54 Standard logic devices. All inputs present one unit load. There is no internal loading on any of the output signal lines. The 18 data output lines and the read complete line are driven from open collector logic elements whose output transistor is normally in the OFF state.

The electrical interface characteristics of the delivered unit are as follows. On all signal inputs, a logic ONE is defined as the most positive voltage level, with respect to the return. On all signal outputs, a logic ONE is defined as the high impedance state. All time relationships are defined from the 50 percent points of the respective signals. Transition times (where applicable) are as specified for TTL Series 54 Standard logic with loading as applied. Stability is defined as being above the minimum logic ONE level or below the maximum logic ZERO level.

**Memory Capacity:** 4096 words of 18 bits each (73,728 bits total).

**Access:** Random by word via 12-bit input address. Also provides for addressing by memory unit via four-bit bank address. All bank address bits must be at a logic ONE for access.

**Access Time:** 350 nanoseconds, maximum, from leading edge of Initiate signal.

**Read Cycle Time:** 1.20 microseconds, maximum, from leading edge of Initiate signal.

**Write Cycle Time:** 1.00 microseconds, maximum, from leading edge of Initiate signal.

**Operate Rate:** 0 to 600k operations per second, minimum, with any read/write ratio.

**Initiate Signal:** Active level = logic ONE. Minimum pulse width = 50 nanoseconds. Maximum pulse width = 550 nanoseconds.

**Read/Write Select:** Read = logic ONE. Write = logic ZERO. Must be stable from leading edge of Initiate signal to end of read or write cycle.

**Bank Address Lines:** Must be stable from leading edge of Initiate pulse to end of Read or Write cycle.

**Word Address Lines:** Must be stable from leading edge of Initiate to end of cycle time.
<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Function</th>
<th>Pin No.</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>J1-1A</td>
<td>Address Bit 0</td>
<td>J2-1A</td>
<td>Data Input Bit 0</td>
</tr>
<tr>
<td>-1B</td>
<td>Address Bit 1</td>
<td>-1B</td>
<td>Data Input Bit 1</td>
</tr>
<tr>
<td>-1C</td>
<td>Address Bit 2</td>
<td>-1C</td>
<td>Data Input Bit 2</td>
</tr>
<tr>
<td>-1D</td>
<td>Address Bit 3</td>
<td>-1D</td>
<td>Data Input Bit 3</td>
</tr>
<tr>
<td>-1E</td>
<td>Address Bit 4</td>
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<td>Data Input Bit 4</td>
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<td>-1F</td>
<td>Address Bit 5</td>
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<td>Return</td>
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<td>-1M</td>
<td>Return</td>
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<td>-1N</td>
<td>Initiate Command</td>
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<td>-2D</td>
<td>Address Bit 10</td>
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<td>Data Input Bit 17</td>
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<td>-2E</td>
<td>Address Bit 11</td>
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<td>Data Output Bit 0</td>
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<td>-2F</td>
<td>Bank Address Bit 0</td>
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<td>-2G</td>
<td>Bank Address Bit 1</td>
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<td>-6.1V</td>
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<td>-6.1V</td>
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<td>Data Output Bit 8</td>
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Table II. External Connector Pin Assignments (Contd)

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<th>Pin No.</th>
<th>Function</th>
<th>Pin No.</th>
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<td>J2-2P</td>
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<td>Bank Address Bit 2</td>
<td>-3A</td>
<td>Data Output Bit 2</td>
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<td>-3B</td>
<td>Bank Address Bit 3</td>
<td>-3B</td>
<td>Data Output Bit 2</td>
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<tr>
<td>-3C</td>
<td>+5.0V</td>
<td>-3C</td>
<td>Data Output Bit 2</td>
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<tr>
<td>-3D</td>
<td>+5.0V</td>
<td>-3D</td>
<td>Data Output Bit 2</td>
</tr>
<tr>
<td>-3E</td>
<td>+5.0V</td>
<td>-3E</td>
<td>Data Output Bit 2</td>
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<td>-3F</td>
<td>+5.0V</td>
<td>-3F</td>
<td>Data Output Bit 2</td>
</tr>
<tr>
<td>-3G</td>
<td>+5.0V</td>
<td>-3G</td>
<td>Data Output Bit 2</td>
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<tr>
<td>-3H</td>
<td>Thermistor</td>
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<td>Data Output Bit 2</td>
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<td>Thermistor</td>
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<td>Return</td>
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<tr>
<td>-3K</td>
<td>Read Complete</td>
<td>-3K</td>
<td>Return</td>
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<tr>
<td>-3L</td>
<td>Return</td>
<td>-3L</td>
<td>Return</td>
</tr>
<tr>
<td>-3M</td>
<td>Return</td>
<td>-3M</td>
<td>Return</td>
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<td>Not Assigned</td>
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</tr>
<tr>
<td>-3P</td>
<td>Not Assigned</td>
<td>-3P</td>
<td>Return</td>
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</table>

**Input Data Lines:** For write operations, must be stable from leading edge of Initiate to end of cycle time. For read operations, may be any level within TTL logic limits.

**Read Complete Line:** Presents high impedance (20k minimum) in quiescent state. Goes active (i.e. low impedance) at end of access time (maximum of 350 nanoseconds following leading edge of Initiate signal). Remains at active level for minimum of 250 nanoseconds and maximum of 450 nanoseconds. Will sink minimum of 10 mA at 0.3V in active state.

**Data Output Lines:** Presents high impedance state (20k minimum) in quiescent state. Goes active (i.e. low impedance) maximum of 30 nanoseconds following leading edge of Read Complete signal and remains active for minimum of 150 nanoseconds following trailing edge of Read Complete signal and maximum of 750 nanoseconds. Will sink minimum of 10 mA at 0.3 V in active state.
3.2.1 Power Source Requirements

The memory unit operates from power sources of +5.0V and -6.1V. Requirements imposed on these power sources by the memory are as follow (all measurements made at connector terminals):

+5.0V:

Regulation: ±5%

Average Standby Current: 13.1 mA, worst-case.

Average Operate Current: 840 mA, worst-case at operate rate of 500k operations per second and read/write ratio of one.

Transient Demands: 50 mA, maximum, during cycle time.

Standby Power: 68.8 milliwatts maximum at +5.25V.

Operate Power: 4.41 watts, maximum, at +5.25V and at operate rate of 500 kHz with a read/write ratio of one.

-6.1V:

Regulation: ±5%

Average Standby Current: 10.9 mA, worst-case.

Average Operate Current: 355 mA, worst-case at operate rate of 500k operations per second and read/write ratio of one.

Transient Demands: 60 mA, maximum, during cycle time.

Standby Power: 69.8 milliwatts, maximum, at -6.40 volts.

Operate Power: 2.27 watts, maximum, at -6.40 volts and at operate rate of 500 kHz with read/write ratio of one.

3.2.2 Thermistor Characteristics

The thermistor is mounted at the approximate center of the unit. It is a YSI Type 44006 precision element with a nominal impedance of 10k ohms at +25°C. The resistance versus temperature characteristic is given in Table III.
## Table III. Thermistor Resistance Versus Temperature

### RESISTANCE VERSUS TEMPERATURE \(-80^\circ C\) to \(+150^\circ C\)

<table>
<thead>
<tr>
<th>TEMPERATURE (°C)</th>
<th>RESISTANCE (Ω)</th>
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</table>
3.3 FUNCTIONAL DESCRIPTION

3.3.1 Memory Organization

The memory is organized into 1024 memory words of 72 bits each (expandable to 96 bits). Each memory word therefore comprises four 18-bit external data words. Figure 4 is a block diagram of the memory organization. The memory stack itself is packaged on eight identical printed wiring, glass-epoxy substrates, with 128 two-turn word lines on each board, for a total of 1024.

Each word line wraps twice around 144 plated wires, with the corresponding wires in each of the eight boards connected in series. At the far end, each pair of adjacent wires is shorted together, forming seventy-two pairs, with each pair traversing between all 1024 word lines. The opposite ends of each pair terminate at the input of a differential sense amplifier. The outputs of a bi-directional digit driver current source is also connected to each pair of wires at the same end as the sense terminations. A specific bit storage location is formed at the crossover points of a particular word line and a pair of plated wires.

Using two wires for each bit storage (i.e., two crossovers) allows a differential implementation for information sensing, virtually eliminating common-mode noise problems and increasing the signal outputs at any given word current level, thus permitting operation at lower word currents than would have been required with a single crossover-per-bit implementation.

A memory word consists of the 72 bits under a single word line on a particular memory stack board. A particular data word address uniquely locates an 18-bit data word by identifying a word line and a group of 18 sense amplifier channels or 18 digit driver current sources.

The only electronics packaged as part of the memory stack is associated with word line selection. The rest of the electronics is packaged on three similar board assemblies.

3.3.2 Word-Line Selection and Drive

Figures 5 and 6 show the word current selection and drive method. Word line addressing is accomplished through a two-level tree of transistor switches. The first level steers the word current to one of 64 unique areas of the stack. The second level steers the word current into one of 16 word lines in the particular word group addressed through the first level. Both levels are packaged on the memory stack boards.
Figure 4. Overall Functional Block Diagram
Figure 5. Simplified Memory Drive and Sense Diagram
Figure 6. Word-Line Selection Matrix
The data word address is decoded in the sequencer, using SNC 5445 Binary-to-Decimal Decoders. Address bits $2^2$, $2^3$ and $2^6$ through $2^9$ are decoded into 1-of-64 and identify the word group. Bits $2^0$, $2^1$, $2^4$ and $2^5$ are decoded into 1-of-16 and identify the word line within a group. Bits $2^{10}$ and $2^{11}$ identify a particular data word location (1-of-4) along the addressed word line. The apparent anomaly in sequence of the bits allocated for identification of word group and word line is a result of test considerations. With the switching matrix implementation used in the system, the address bit allocation defined above will identify adjacent word lines across a plane when the address sequences in a straight binary code.

Since only one end of each word line is actively switched (with the opposite end returned to ground) only the addressed word-line has any voltage applied to it (with reference to the quiescent level). Thus, current flow in the stack resulting from charge transfer to/from stray capacitance is minimized and stack charge "restoration" is not necessary. The resulting design is significantly less complex, faster and more noise-free.

A transformer is used for coupling between the word current generator and the word line selection matrix to negate the need for a third, high-voltage power input. The transformer also provides some additional measure of noise reduction.

3.3.3 Control and Sequencing

The memory design does not use a discrete internal clock. Instead, memory sequences are generated from a series of programmable delays. A diagram of the sequencer logic is shown in Figure 7. Each delay is programmable, independent of any other delay. (The actual programming is accomplished by selection of discrete component values). Thus, timing sequences can be optimized for performance and power consumption.

Power to all but a minimum of control logic is switched off between memory cycles. The delay circuit is designed to come up in a normalized state when power is applied.

When an Initiate signal occurs, the power switch is turned on. If the signal is of longer duration than delay $\tau_A$ (approximately 35 nanoseconds), then the Initiate Override signal is actuated, locking the memory in the operate mode until the read or write cycle is completed.

Power to the digit drivers, sense amplifiers and associated logic is also controlled through the sequencer. The corresponding power switches are physically located on the digit electronics board assemblies.

Delays $\tau_B$ through $\tau_E$ are activated for a write cycle. Delays $\tau_B$ and $\tau_D$ set the width of the two phases of digit current and $\tau_C$ sets the separation between the two phases. Delay $\tau_E$ controls the duration of the word current. The $\phi_1$ and $\phi_2$ digit current controls for one of the four possible data words are activated, depending on the states of address bits $2^{10}$ and $2^{11}$.
Figure 7. Sequencer, Logic Diagram
Delays $\tau_F$ through $\tau_I$ are activated during a read cycle. Delay $\tau_F$ starts the word current after power start-up transients have had an opportunity to dissipate. A pick-off from the word current level is delayed by $\tau_C$ and used as the read strobe, which clocks the sense amplifier outputs into the output data buffer register. Delays $\tau_H$ and $\tau_I$ set the duration of the read complete and the post-read data hold periods, respectively.

3.3.4 Write Operation

The memory timing for a write cycle is shown in Figure 8. For proper operation, the address, data and read/write control signals must be stable prior to the leading edge of the initiate command and must remain stable until the write cycle has been completed.

When an initiate command pulse occurs in the presence of a low (or ground) level on the read/write control line, power to the sequencer and to the write electronics is turned on. A low impedance path is connected from the word current generator to a particular word line (through the word line selection matrix) as identified by address bits $2^0$ through $2^9$. A group of 18 digit driver current sources is then energized for $\phi_1$ current. The particular current sources are identified by address bits $2^{10}$ and $2^{11}$. The polarity of current (i.e. direction along the plated wire element) from any current source is controlled by the logic level of the data input to that current source. The $\phi_1$ digit current is then terminated and $\phi_2$ current enabled. The two phases are of equal amplitude and duration. This balanced current implementation precludes any hysteresis build-up due to an unequal history of data "one" and "zero" writes.

![Figure 8. System Timing, Write Operation](image-url)
The word current generator is energized early enough that the terminating transition of the word current can be made to occur during the time when \( \phi_2 \) digit current is at full amplitude. Data is "written into" the wire when the word current terminates in the presence of digit current.

At the end of the \( \phi_2 \) digit current, the write cycle is complete and internal system power is turned off. A write cycle, from the leading edge of the initiate command to turn-off of system power, requires approximately 750 nanoseconds.

3.3.5 Read Operation

The memory timing for a read cycle is shown in Figure 9. For proper operation, the address and read/write control lines must be stable prior to the leading edge of the initiate command and must remain stable until completion of the read cycle.

When the initiate command pulse occurs in coincidence with a high level on the read/write control line, power to the sequencer and the read electronics is turned on. A low impedance path is again connected to the addressed word line through the word line selection matrix. A group of 18 sense amplifier channels are selected, as identified by address bits 2\(^{10}\) and 2\(^{11}\).

After any transients generated in the sense amplifiers have had a chance to settle out, the word current generator is energized. Signals are induced in the plated wires during the word current transients and are amplified by the sense amplifiers. The leading edge transient of the word current is controlled to effect the widest useable "window" in the sense amplifier output. The amplifier outputs are used as steering inputs to buffer storage registers. The polarity depends on the state of the information previously "written into" the plated wire.

The information "read out" during the turn-on transient of the word current is clocked into the the buffer register by the strobe. The strobe is generated by a level detector in the current generator. This minimizes possible uncertainties in strobe position.

The read-complete signal is initiated when the data is clocked into the buffer register. It is maintained for a minimum of 250 nanoseconds and a maximum of 450 nanoseconds. Output data is maintained in the buffer register for at least 150 nanoseconds after termination of the read complete signal. At the end of this time the read cycle is complete and internal power is switched off.

The data and read complete sources are Series 54 open collector logic elements. A low impedance (i.e., output transistor on) denotes the active level for the read complete line and a logic zero on the data lines. The only time the low impedance condition will exist on a data line is during the actual read-out (per Figure 2-9) of a bit 0.

3.4 ELECTRICAL PARTS

High-Rel, screened parts were used in construction of the memory.
3.4.1 Logic Circuits

Series 54 TTL integrated circuit logic elements were used throughout the memory. These were procured per vendor High-Rel specification SNC which is MIL-STD-883, Class B.

3.4.2 Discrete Parts

Two types of established reliability resistors were used in the memory; the RCRXXG Composition and the RNR55C metal film. Both types were procured to S failure-rate levels.

Three types of capacitors were used; the CSR13 style, established reliability tantalum with failure rate of R or lower, the CKRO5 and 06 style, established reliability ceramic with failure rate of R or lower, and the CM series mica per MIL-C-5/18 with additional screening for DWV and IR. Only JANTX transistors and diodes were used in construction of the memory.
3.4.3 Transformer

A single rf transformer was used in the memory for coupling the word current from the generator to the memory stack. The transformer was fabricated in-house to the requirements of MIL-C-15305, Type LT6K, with temperature cycling per MIL-STD-202, Method 102, Condition C, except 10 cycles at -55°C.

3.4.4 Hybrid Circuits

Six different hybrids are used in the memory. These are custom circuits manufactured in-house and screened to meet the requirements of this program. Each of these circuits is described briefly in the following paragraphs.

3.4.4.1 Delay Circuit

The delay circuit is shown, functionally, in Figure 10. Only the high-to-low transition at the input is delayed at the output, with both the true and complement outputs available. The delay is adjustable from a minimum of approximately 25 nanoseconds to a maximum of several microseconds.

3.4.4.2 Word Current Generator

The word current generator is shown in Figure 11. It consists, basically, of a controlled current source for which the turn-on slope and the amplitude are programmable by selection of external, discrete components. The current is gated on and off by an external enable signal. Input voltages are monitored and the word current is inhibited if voltage(s) is below a level at which the memory will operate properly.

There is also a level detector on the current output from which a trigger is developed for sampling the sense amplifier outputs during a read operation.

3.4.4.3 Word-Line Selection Circuits

The word line selection circuits are shown in Figures 12 and 13. A particular switch is closed by grounding the corresponding selection input. The first and second level switches are packaged together. A particular package contains one first level switch and two banks of four second level switches each. Each of four second level selection inputs controls one switch in each bank. A single selection input controls the first level switch. The pin-outs are configured so that a first level switch can be connected to a second level bank in a different package, as well as to a bank in its own package.

3.4.4.4 Sense Amplifier

The four-channel sense amplifier (MC 1544) is shown in Figure 14. The input terminating resistors are external to the package.
Figure 10. Delay Circuit, Functional Diagram

Figure 11. Word Current Generator, Functional Diagram
Figure 12. Custom Package and Layout
Figure 13. Word Line Selection Matrix, Functional Diagram
Figure 14. Four-Channel Sense Amplifier, Functional Diagram
3.4.4.5 Digit Driver

The digit driver is shown in Figure 15. Basically, it consists of two current sources with steering such that, depending on the logic inputs, one of the sources may be enabled to conduct current through the load in a particular direction. The T1 and T2 inputs denote successive time periods for the two opposite phases of digit current. The D and D inputs denote the true and complement levels of an input data bit. If D is true, then current will flow in the direction indicated during T1 and in the opposite direction during T2. The current flow would be opposite if D were true.

3.4.4.6 Power Switches

Two types of power switches are used in the memory. One type provides two independently controlled logic level (i.e., +5.0 V) outputs from the primary +5 V input. The other type provides two sets of +5.0 V and -6.1 V outputs from the corresponding inputs. Each set is controlled independently. The switches themselves consume no power when in the OFF state. The switches perform no regulation. They are shown functionally in Figures 16 and 17.

3.5 MECHANICAL DESIGN

3.5.1 Stack Design

The plated wire memory stack used in the LP RASM used a standard Motorola plane design for spaceborne memories developed to high reliability, quality assurance, and workmanship standards. The primary design goal of the stack was simplicity of fabrication combined with high reliability. The number of solder joints and plated through holes are minimized to accomplish this end. The stack consists of eight planes arranged and interconnected to meet the specific requirements of the LP RASM. Specific details of stack construction are described below.

The tunnel structure, the heart of the memory plane, contains the word lines and the plated wire which stores the bits of data. The plated wires are installed in 0.007 diameter tunnels on 0.025 centers in a polymide-FEP tunnel matt. The tunnel matt is constructed by forming the FEP (between the polyimide film) around dummy wires at controlled temperature, pressure and wire tension. After complete assembly processing the dummy wires are removed and the plated wire is installed in the tunnel.

Word lines of etched copper on glass epoxy board are laminated to each side of the tunnel matt so that they are perpendicular to the tunnels (plated wire). The word lines are double turn (twice around the wires per line). Their mechanical configuration is 0.010 wide conductor, an intervening 0.005 space and another 0.010 conductor, all on repetitive 0.050 centers. Plated-thru holes at each end of the tunnel matt creates the double turn word lines.
Figure 15. Digit Driver, Functional Diagram
Figure 16. Power Switch +5V/-6V

Figure 17. Power Switch +5V/+5V
Each carrier structure contains 64 word lines and 100 bit lines (Plated wire tunnel pairs). To provide the desired storage capacity for the LP RASM only 72 tunnel pairs are populated (plated wire installed).

Keepers, of high magnetic permeability and processed with extreme care, are bonded to the outer surface of the glass epoxy board which support the word lines to contain the word line field and shield against external magnetic fields. The tunnel matt and word lines are carefully fabricated and then laminated into a subassembly using multilayer printed wiring board techniques. The keepers are then laminated using similar techniques. A cross section of the tunnel structure is shown in Figure 18.

The memory plane is fabricated by laminating two tunnel structures to each side of a motherboard. The motherboard is a two-sided printed wiring board which has a ground plane laminated in the center. The input and return for the matrix is tracked to the edge of the board where pc board interconnect is used to interface with the plane. Two tunnel structures per plane provide 128 word x 72 bit capacity. Installation of the 8 word-drive flat packs per side, by lap soldering, completes the memory plane subassembly. Memory plane construction is shown in Figure 19.

The memory stack consists of eight memory planes electrically and mechanically integrated into one unit to provide 1024 words x 72 bits of storage. The digit lines of each plane are interconnected with flat flexible circuitry bonded to the motherboard which permits the stack to be opened as necessary during assembly and rework. The plated wire is formed like a "hairpin" and installed into the top and bottom carrier structure (similar to a trombone slide). The two ends of the plated wire are lap soldered directly to the conductor of the interconnecting flex cable. This approach for installing the plated wire minimizes the number of solder joints required while providing the required stress relief.

PC board interconnect with miniature connectors (see Figure 2) is used to interconnect common word drive signals from plane to plane and carry all digit and word signals to the electronics. The use of printed circuitry interconnect provides controlled impedance and line characteristics. The connectors allow the stack to be connected/disconnected from the electronics with minimum effort.
During assembly, spacers are installed at each tie-down location on the planes to precisely position the planes relative to each other in the stack. The tie-downs are located to provide maximum stability under dynamic conditions.

### 3.5.2 System Packaging

The 4k x 18 bit Low Power Random Access Spacecraft Memory developed by Motorola consisted of a 1k by 72 plated wire stack, two digit drive/sense electronics boards and a timing/control/word drive board, all contained in an aluminum housing.

The concept of stacking the electronics boards in the same manner as the planes was used in the complete memory package. The timing/control/word drive board is located on top of the plated wire stack while the two digit drive/sense boards are located below the plated wire stack. This arrangement eliminates interference between signals as the digit line interconnects leave the plated wire stack in one direction while the word lines go the other direction.
The size of the memory plane (i.e., number of word lines, digit lines, required structural mounting and word drive matrix area) determine the "plan view" size of the system package. The basic plane size is 8.05" long x 4.38" wide and contains 6 tie-down screws. The electronics boards have the same mounting tie-down locations and length as the plane but are 5.0" wide.

Mechanically, each of the electronic boards are essentially identical. Each consists of a printed wiring board to which flat pack integrated circuits (Motorola plated wire hybrids or conventional logic) are lap soldered and a few discrete components are mounted. The digit boards contain the digit drivers, sense amplifiers, data input buffers and data output registers. The third board contains the timing and control logic and the transistor word drive select electronics.

After the boards are assembled, a thin conformal coating is applied to the board assembly. This coating provides protection in a high humidity environment, protection against shorting across components and a vibration damping effect on the boards. This provides an encapsulated assembly that is easily disassembled for servicing or repair.

Flat flexible cable is used for interconnecting between board assemblies. The flex interconnect is arranged so the plated wire stack and printed wiring boards can be assembled in the system stack (described previously) or opened out to provide access for testing or troubleshooting of the boards, the stack or the system. The connection to the external connector is a conventional hard wire harness.

The plated wire stack and electronics boards are assembled by stacking them into a single unit and installing them in a housing. Spacers are provided between the boards and the stack at the tie down locations to position them with respect to each other. Six special high strength screws pass through the spacers and secure the system in the housing.

The system assembly is contained in a single protective housing which was machined from aluminum. The memory housing is 8.6" long x 6.3" wide x 2.9" high (exclusive of mounting flanges and connectors) establishing a volume of 157 cubic inches. The system has a total weight of 6.25 pounds.

3.5.3 Materials

Motorola's basic memory system design uses materials that meet the requirements of high reliability spaceborne hardware, particularly in the area of environment, outgassing and compatibility with other materials in the spacecraft. Materials are used that were approved on the Mariner '71 subsystems which Motorola designed and fabricated and have since been proven by the success of the mission. The use of any material is dependent not only on the material but also on its receiving the proper processing and cure. This factor was considered in the assembly procedures and processes used to fabricate the memory system.
All of the material used in the LP RASM were submitted to the Chemistry and Physics Section of the Engineering Physics Division at GSFC for review and approval. From the preliminary design, some alternate materials were recommended and some changes in cure cycles were suggested. If data was not readily available on a material it was tested by the C&P Section to insure it met all requirements.
SECTION 4
TESTING

4. GENERAL

Comprehensive testing was performed on the memory and its components at the piece part level and at each level of assembly. The formal test documents for tests performed at the stack and system levels are included as appendices.

4.1 SYSTEM LEVEL TESTING

Acceptance tests were conducted at the system level. Acceptance testing included complete functional tests at temperature extremes of +85°C and -40°C. The Acceptance Test Procedure and Test Data Records are included as Appendix I. Acceptance Tests (except at high and low temperatures) were repeated after environmental testing.

Environmental testing consisted of both sine and random vibration, shock and altitude (to \(10^{-5}\) mm Hg). The memory unit was continuously exercised during all environmental testing.

4.2 MEMORY STACK TESTING

A 100 percent on-line test was performed on the plated-wire during manufacture under relatively severe test patterns and word/digit current variations.

In addition to the on-line wire test, the memory stack was subjected to comprehensive, worst-case tests, over temperature, at the stack level using an EH8500 computer controlled stack tester. These tests were performed in accordance with a formal stack test procedure, which is included as Appendix II. The procedure is quite definitive, however, and some explanation is probably in order relative to the test pattern shown in Figure 8 (page 13 of the test procedure).

The first three horizontal rows relate to word current in the word line corresponding to the particular bit under test and word currents in the two word lines immediately adjacent (i.e., left adjacent bit and right adjacent bit). The fourth row relates to digit current in the plated-wire corresponding to the particular bit under test.

The vertical columns relate to successive time slots, left-to-right except that, as indicated in the row labeled NO. OF CYCLES, the first group of three time slots is cycled through \(10^3\) times before stepping to the fourth time slot.
IWD identifies a maximum, or disturb, word current level. IWW and IWR identify a minimum word current level, which is worst-case for writing and reading in the bit-under-test. IDD1 and IDD2 identify maximum, or disturb, bipolar digit current levels. IDW1 and IDW2 identify minimum levels of the bipolar digit currents. These are worst-case for writing in the word-under-test.

During the first three time slots, information of a particular polarity is "hard-written" (i.e., under maximum word and digit current levels) into the bit-under-test and its two adjacent bits along the same plated-wire. This is done 1000 times and constitutes adverse history.

The opposite polarity information is then "soft-written" one time in the bit-under-test and then immediately read out, again with minimum word current. The resulting wire output represents an "undisturbed" condition (i.e., with no intervening activity at adjacent bit locations).

The next four program steps are cycled through a total of 10,000 times. During the first time slot, information opposite to that stored in the bit-under-test is written into one of the adjacent bits under conditions of worst-case maximum word and digit current levels. In the second time slot, maximum-level word current is pulsed through the word line corresponding to the bit-under-test. The same two steps are then repeated, only with reference to the other adjacent bit.

During the final time period, the bit-under-test is again read and compared to preset limits, using worst-case minimum word current.

Any wire which did not meet a minimum output level requirement of 4.5 millivolts, over temperature, was replaced. This amounted to a total of 56 wire pairs. There is a total of 576 wire pairs (72 pairs per plane times 8 planes) in the stack. The replacement incidence therefore represented less than 10 percent, which is well within normal expectations.

4.3 HYBRID CIRCUIT SCREENING

All hybrid microcircuits used in the memory were subjected to extensive, 100 percent screening to criteria based on MIL-STD-883 criteria. In addition to comprehensive electrical tests at temperature extremes, these tests included precap visual inspection, centrifuge, operational vibration, stabilization bake, thermal cycling, power aging and leak testing.
APPENDIX I

ACCEPTANCE TEST PROCEDURES
<table>
<thead>
<tr>
<th>LTR</th>
<th>DESCRIPTION</th>
<th>DATE</th>
<th>APPROVED</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1</td>
<td>Initial Release</td>
<td>5-21-73</td>
<td></td>
</tr>
<tr>
<td>X2</td>
<td>Incorporated changes prior to first usage.</td>
<td>5-21-73</td>
<td></td>
</tr>
<tr>
<td>X3</td>
<td>Change -6.9V to -6.1V</td>
<td>6-18-73</td>
<td></td>
</tr>
<tr>
<td>X4</td>
<td>Change $10^{-6}$ mmHg to $10^{-5}$ mmHg, Change sine sweep levels, page 28. Change random vibration levels, page 29.</td>
<td>7-24-73</td>
<td></td>
</tr>
</tbody>
</table>

**ASTERISK INDICATES DATA WHICH IS NONMANDATORY FOR INFORMATION ONLY.**

**FOR ASSOCIATED LISTS SEE**

**INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY**

**MOTOROLA INC.**

Government Electronics Division

8201 EAST McDOWELL ROAD

SCOTTSDALE, ARIZONA 85252

**ACCEPTANCE TEST PROCEDURE, LOW POWER RANDOM ACCESS SPACECRAFT MEMORY, PART NO. 01-P13701D**

**SIZE** | **CODE IDENT NO.** | **DWG. NO.** |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>94990</td>
<td>12-P13722D</td>
</tr>
</tbody>
</table>

**SCALE**

**SHEET 1 OF 35**

-100A-7/70 DWG FORMAT
<table>
<thead>
<tr>
<th>SECTION</th>
<th>TITLE</th>
<th>PAGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>SCOPE</td>
<td>3</td>
</tr>
<tr>
<td>2.</td>
<td>REFERENCE INFORMATION</td>
<td>3</td>
</tr>
<tr>
<td>3.</td>
<td>TEST EQUIPMENT AND ENVIRONMENTAL REQUIREMENTS</td>
<td>4</td>
</tr>
<tr>
<td>4.</td>
<td>TEST SCHEDULE</td>
<td>6</td>
</tr>
<tr>
<td>5.</td>
<td>TEST RECORDS</td>
<td>7</td>
</tr>
<tr>
<td>6.</td>
<td>PHYSICAL CHARACTERISTICS</td>
<td>7</td>
</tr>
<tr>
<td>7.</td>
<td>INITIAL FUNCTIONAL TESTS</td>
<td>7</td>
</tr>
<tr>
<td>8.</td>
<td>TEMPERATURE TEST</td>
<td>20</td>
</tr>
<tr>
<td>9.</td>
<td>VACUUM TEST</td>
<td>24</td>
</tr>
<tr>
<td>10.</td>
<td>VIBRATION TEST</td>
<td>27</td>
</tr>
<tr>
<td>11.</td>
<td>SHOCK TEST</td>
<td>29</td>
</tr>
<tr>
<td>12.</td>
<td>FINAL FUNCTIONAL TESTS</td>
<td>30</td>
</tr>
</tbody>
</table>
1. **SCOPE**

This procedure and the test data sheet (12-P11216B) define the unit acceptance requirements for the Low Power Random Access Spacecraft Memory, Motorola Part No. 01-P13701D, manufactured under Contract No. NAS 5-23163.

2. **REFERENCE INFORMATION**

2.1 **SPECIFICATIONS APPLICABLE**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>S-562-P-24</td>
<td>Low Power Random Access Spacecraft Memory.</td>
</tr>
<tr>
<td>12-P13721D</td>
<td>Test Data Record</td>
</tr>
<tr>
<td>12-P11173B</td>
<td>Motorola Plated Wire Memory Tester Operating Manual.</td>
</tr>
</tbody>
</table>

2.2 **DEFINITIONS**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>UP position on DATA and ADDRESS switches. DATA and ADDRESS lamps ON</td>
</tr>
<tr>
<td>0</td>
<td>DOWN position on DATA and ADDRESS switches. DATA and ADDRESS lamps OFF</td>
</tr>
<tr>
<td>Tester</td>
<td>Motorola Plated Wire Memory Tester</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit</td>
</tr>
<tr>
<td>Error Lamps</td>
<td>Lamp ON indicates ERROR present.</td>
</tr>
</tbody>
</table>
3. TEST EQUIPMENT AND ENVIRONMENTAL REQUIREMENTS

3.1 TEST EQUIPMENT

The calibrated test equipment listed below, or its equivalent, will be required to perform this test procedure. Any equipment used as an equivalent to that listed below shall be recorded in the data sheet.

STANDARD TEST EQUIPMENT

<table>
<thead>
<tr>
<th>ITEM</th>
<th>MANUFACTURER</th>
<th>MANUFACTURER'S RANGE &amp; MODEL OR TYPE</th>
<th>ACCURACY</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Milliammeter</td>
<td>Hewlett Packard</td>
<td>428B</td>
<td>0-10 Amp.</td>
</tr>
<tr>
<td>Oscilloscope</td>
<td>Tektronix</td>
<td>585</td>
<td>50ns/cm</td>
</tr>
<tr>
<td>Scope Plug-In</td>
<td>Tektronix</td>
<td>82</td>
<td>Tr 1.5ns</td>
</tr>
<tr>
<td>Digital Voltmeter</td>
<td>Hewlett-Packard</td>
<td>3440A</td>
<td>Accuracy ± .05% of reading</td>
</tr>
<tr>
<td>Counter</td>
<td>CMC</td>
<td>727BN</td>
<td>0.1% ± 1/2 LSB</td>
</tr>
<tr>
<td>DC Multifunction Unit</td>
<td>Hewlett-Packard</td>
<td>3444A</td>
<td>0-999.9 ma.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0-9,999 megohms</td>
</tr>
<tr>
<td>Oven</td>
<td>Wyle</td>
<td>CO-106-1800</td>
<td>-100°F to +500°F</td>
</tr>
<tr>
<td>Power Supplies</td>
<td>Precision Design Inc</td>
<td>5015-A</td>
<td>0-50V, 1.5 Amp.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5015-S</td>
<td>0-50V, 1.5 Amp.</td>
</tr>
<tr>
<td>Pulse Generator</td>
<td>EH</td>
<td>139B</td>
<td>10Hz to 50MHz</td>
</tr>
</tbody>
</table>
NON-STANDARD TEST EQUIPMENT
(NO CALIBRATION REQUIRED)

Motorola Plated Wire Memory Tester 01-P11170B001

NOTE: The Motorola Plated Wire Memory Tester supplies inputs to the memory under test from SN5400 series logic and presents a single unit load of SN5400 logic on the memory output lines.

Motorola Tester Interface Box T-5909

NOTE: The Interface Box puts a 51 ohm resistor in series with all of the signals going to the memory and provides a 1K pull-up resistor to signals coming back from the memory.

ENVIRONMENTAL TEST EQUIPMENT

<table>
<thead>
<tr>
<th>ITEM</th>
<th>MANUFACTURER</th>
<th>MODEL NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vibration Tester</td>
<td>LING</td>
<td>275</td>
</tr>
<tr>
<td>Vacuum Chamber</td>
<td>NRC</td>
<td>2707</td>
</tr>
<tr>
<td>Shock Tester</td>
<td>MRL</td>
<td>2424</td>
</tr>
<tr>
<td>Vibration Test Fixture</td>
<td>MOT</td>
<td></td>
</tr>
</tbody>
</table>

3.2 TEST CONDITIONS

Unless otherwise specified all tests shall be performed under the following conditions.

3.2.1 Power Supply Voltage

The unit specified to be tested shall operate from the following DC source voltages:

\[ +5.0V \pm 5\% \]
\[ -6.1V \pm 5\% \]
3.2.2 **Ambient Temperature**

The unit shall be tested in a laboratory area having a temperature of $+25 \pm 10^\circ C (77 \pm 18^\circ F)$.

3.2.3 **Ambient Humidity**

Normal laboratory ambient, not to exceed 90%.

3.2.4 **Ambient Atmospheric Pressure**

Normal laboratory ambient.

3.2.5 **Stabilization Period**

The test equipment shall not be used to conduct tests until after a minimum warm-up period of 15 minutes.

4. **TEST SCHEDULE**

The testing to be performed on each memory unit is as follows:

1. Physical Characteristics (Weight and Dimensions).
3. Operational Tests at Temperature Extremes.
4. Operational Vacuum Tests
5. Operational Vibration Tests
6. Operational Shock Tests
7. Final Functional Tests

Tests 3 through 6 may be performed in any sequence.
TEST RECORDS

5.1 TEST LOG

The Test Log shall be used to record the history of the memory, starting from the first system test. The log shall reference all testing, rework and idle time for the particular memory unit.

5.2 DATA RECORD

All test results shall be recorded in the Test Data Record, Motorola Document No. 12-P13721D.

6. PHYSICAL CHARACTERISTICS

6.1 WEIGHT

Place the LP RASM on the scale and read and record, in the data sheet, the weight of the memory, in pounds.

6.2 DIMENSIONS

Measure and record, in the data sheet, the outside dimensions as shown in Figure 1. Compute and record, in the data sheet, the memory volume by multiplying dimension W by dimension H by dimension D. \( V = W \times H \times D \).

7. INITIAL FUNCTIONAL TESTS

7.1 INTERCONNECTION

At the Interface Box, set memory power to OFF. Connect the unit under test as shown in Figure 2, except that the Interface Box will not be connected to the Plated Wire Memory Tester. The
connections are all labeled on the Interface Box.

Turn the coarse voltage controls fully counterclockwise and turn on power to all electrical test equipment.

Using the scope, adjust the Pulse Generator for $+3 \pm 0.1V$ positive pulses of $450 \pm 10$ nanosecond duration (at the 50 percent points) at a $500 \pm 1.0$ KHz rep rate. (Use the counter to adjust the rep rate). The pulse generator output must be terminated in 50 ohms and connected to the tester when making these adjustments.

Normal precaution shall be taken to ensure that the equipment is not dropped or damaged in any way while it is being handled, or while the connectors are being engaged.

### 7.2 PRELIMINARY CONTROL SETTINGS

Set the Tester and Interface Box controls as follows and maintain these control settings unless otherwise directed in the individual tests.

<table>
<thead>
<tr>
<th>CONTROL</th>
<th>SETTING</th>
</tr>
</thead>
<tbody>
<tr>
<td>TESTER</td>
<td></td>
</tr>
<tr>
<td>BD1-BD4 (24 Switches)</td>
<td>No. 0 Down</td>
</tr>
<tr>
<td></td>
<td>all Other Up</td>
</tr>
<tr>
<td>Tape Reader Power</td>
<td>Light Off</td>
</tr>
<tr>
<td>Run-Off-Rewind Switch</td>
<td>OFF</td>
</tr>
<tr>
<td>Tester Power</td>
<td>Light On</td>
</tr>
<tr>
<td>Address Switches</td>
<td>Down</td>
</tr>
</tbody>
</table>
CONTROL
TESTER (Cont.)

<table>
<thead>
<tr>
<th>Setting</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Down</td>
<td>WRITE</td>
</tr>
<tr>
<td>24</td>
<td>SEQ.</td>
</tr>
<tr>
<td>MAN</td>
<td>EXT.</td>
</tr>
</tbody>
</table>

INTERFACE BOX

<table>
<thead>
<tr>
<th>Setting</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>All 2.4V</td>
<td>GND</td>
</tr>
<tr>
<td>GND</td>
<td>OFF</td>
</tr>
<tr>
<td>OFF</td>
<td>OFF</td>
</tr>
</tbody>
</table>

7.3 INITIAL POWER SUPPLY CONDITIONS

Using the DVM, adjust the three supplies as follows:

+5V to Interface Box: +5.0V ± 0.1V
+5V to Memory: +5.0 ± 0.1V
-6.1V to Memory: -6.1 ± 0.1V
Set the meter selection switches to measure current and leave them in this position. Disconnect the output side of all three power supplies from the Interface Box.

All subsequent mention of +5V in the procedure refers to memory power unless otherwise specified.

7.4 CHASSIS ISOLATION

Using the digital ohmmeter verify that the impedance between the memory chassis and ground test point on the interface box is \( \geq 9 \) megohms. Record the results in the Data Sheet.

7.5 INPUT SIGNAL LOADING

7.5.1 Connect the two +5V supplies to the Interface Box. (If the Interface Box supply overloads, reset it by turning its power off and back on).

7.5.2 Remove the jumper wire from the INT PULSE test point. Connect the digital ammeter between the INT PULSE and INT PULSE SW test points. Momentarily turn the MEMORY POWER switch to ON and measure and record the current. Set the INT PULSE switch to the +2.4V position. Momentarily set the memory power switch to ON and again measure and record the current. Disconnect the ammeter and connect the jumper wire between the INT PULSE and INT PULSE SW test points.

7.5.3 Replace the jumper from the MEMORY SELECT 1 test point to the MEMORY SELECT 1 SWITCH test point with the digital ammeter. Momentarily set MEMORY POWER to ON and measure and record the current. Set the MEMORY SELECT 1 SWITCH to the GND position.
Momentarily set MEMORY POWER to ON and measure and record the current.

Disconnect the ammeter and replace the jumper wire. Set the MEMORY SELECT 1 SWITCH back to the +2.4V position.

7.5.4 Repeat paragraph 7.5.3 for MEMORY SELECT 2, MEMORY SELECT 3, and MEMORY SELECT 4.

7.5.5 Connect the ammeter from the READ/WRITE test point to the INPUT CURRENT SWITCH test point. Set the Initiate Pulse Switch to 2.4V. Momentarily set the memory power switch to ON. Measure and record the current. Move the INPUT CURRENT SWITCH to the +2.4V position. Momentarily set the MEMORY POWER switch to ON and measure and record the current. Return the INPUT CURRENT SWITCH to the GND position.

7.5.6 Connect the ammeter between the ADDRESS BIT 2^o and the INPUT CURRENT test points. Momentarily set the MEMORY POWER switch to the ON position and measure and record the current. Set the INPUT CURRENT SWITCH to the +2.4V position. Momentarily set the MEMORY POWER switch to the ON position and measure and record the current. Set the INPUT CURRENT SWITCH back to the GND position.

Repeat the above two measurements at each of the 12 address bit test points. Connect a jumper between the R/W and GND test points. Repeat the above two measurements at each of the 18 DI test points (i.e. with the ammeter conn. between a DI test point and the INPUT CURRENT test point).
Verify that the MEMORY POWER switch is OFF. Remove the jumper from the R/W test point and install the jumper from the INT PULSE test point back in its original position.

7.6 VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS.

7.6.1 Connect the Interface Box to the tester. Connect the -6.1V power supply to the Interface Box. At the tester, depress the STOP and RESET pushbuttons.

7.6.2 Turn the MEMORY POWER switch ON and push the START button on the tester. The tester will write a "0" in all data bits in all 4096 addresses one time and stop.

7.6.3 Set the READ/WRITE switch on the tester to the READ position. Push the tester START button. Using the Dual Trace of the oscilloscope, measure and record in the data sheet the voltage at the READ COMPLETE test point 150 ns after the leading edge of the pulse at the INITIATE PULSE test point. The voltage shall be ≤100 mv.

(The read complete output for this test and the data outputs for the next test are terminated with a 1K resistor to GND).

7.6.4 Measure and record in the data sheet the voltage at each of the 18 data output lines that occurs 500 ns after the leading edge of the Initiate Pulse. The voltage shall be ≤100 mv. Push the tester stop button. Set the OUTPUT PULLUP RESISTOR switch to the +5V position.
7.7 POWER CONSUMPTION

7.7.1 Using the DVM, adjust the +5V and -6.1V memory power supplies to +5.0 ± 0.1V and -6.1 ± 0.1V, respectively. Record the voltages.

Using the 428B milliammeter, measure and record the current from the +5V memory supply. Compute and record the +5V power.

7.7.2 Using the milliammeter, measure and record the current to the -6.1V supply. Compute and record the -6.1V power.

7.7.3 Compute and record the total Memory Idle Power.

7.7.4 Set the ADDRESS PATTERN switch to SEQ. and momentarily depress the RESET and START buttons. The tester should be cycling through memory addresses.

7.7.5 Repeat 7.7.1.

7.7.6 Repeat 7.7.2.

7.7.7 Compute and Record the Total Active Power.

7.8 READ COMPLETE TIMING

7.8.1 Connect the oscilloscope as follows; trigger input jack to the INITIATE PULSE test point, channel A voltage probe to the INITIATE PULSE test point and the channel B voltage probe to the READ COMPLETE test point.

7.8.2 Set the DATA PATTERN switch to MAN and the READ/WRITE switch to READ.

7.8.3 Depress and release the RESET button, then the START button.

7.8.4 Synchronize the oscilloscope on the leading edge of the initiate pulse.
7.8.5 The read complete pulse shall be a negative pulse and shall be generated 500 nanoseconds maximum after the leading edge of the initiate pulse and the duration shall be 250 ns minimum and 450 ns maximum. (All timing relationships shall be measured at the 50% points). Record the pulse delay and duration in the data sheet.

7.8.6 Momentarily depress the STOP button and set the READ/WRITE switch to WRITE. Depress and release the RESET button, then the START button. Set the READ/WRITE switch to READ and momentarily depress the START switch.

7.8.7 Connect the scope channel A voltage probe to the first data output line test point (DO-0). The high-to-low transition on the data output line shall occur prior to (or in coincidence with) the leading edge of the read complete pulse. The low-to-high transition of the data output line shall occur no earlier than 150 nanoseconds following the trailing edge of the read complete pulse. (All timing relationships shall be measured at the 50 percent points). Record the results.

7.8.8 Repeat the measurements of 7.8.7 at each of the remaining 17 data output line test points. Record the results.

7.9 SYSTEM FUNCTIONAL TESTS

7.9.1 Depress and release the RESET button. Set the ADDRESS PATTERN switch to SEQ. Adjust the pulse generator frequency to 600 ± 1.0 KHz. Set the DATA PATTERN switch to SEQ.
7.9.2 Depress and release the START button. The tester will then begin cycling through all memory locations. It steps to the first address, writes a "0", reads a "0", writes a "1" and reads a "1" in all bits in that address word, then steps to the next address, etc. The tester continues this cycle unless an error occurs. Test for 10 seconds and record any errors. Use the counter to measure the elapsed test time. Depress the STOP button.

7.9.3 Set the READ 1/READ 7 Switch to the READ 7 position. The READ 7 mode causes the tester to write a "0", read a "0" seven times, write a "1", and read a "1" seven times in each memory location.

7.9.4 Depress and release the START button. The Tester will continue to cycle unless an error occurs. Test for 10 seconds and record any errors.

7.9.5 Depress and release the STOP button. Set the DATA PATTERN switch to MAN and the READ/WRITE switch to WRITE. Set all DATA switches to the DOWN position.

7.9.6 Depress and release the RESET button and then the START button.

7.9.7 Set all DATA switches to the UP position.

7.9.8 Depress and release the RESET button and then the START button.

7.9.9 Set the READ/WRITE switch to READ. Depress and release the RESET button.
7.9.10 Depress and release the START button. Test for one minute. Record any errors.

7.9.11 Depress and release the STOP button.

7.9.12 Set the READ/WRITE switch to WRITE.

7.9.13 Set all DATA switches to the DOWN position. Depress and release the RESET button.

7.9.14 Depress and release the START button. The memory will cycle thru all 4096 addresses one time and stop.

7.9.15 Set the READ/WRITE switch to READ. Depress and release the RESET button.

7.9.16 Depress and release the START button. Run for one minute. Record any errors.

7.9.17 Depress and release the STOP button.
7.10 RANDOM ACCESS CAPABILITY

7.10.1 Set the READ/WRITE switch to WRITE and the ADDRESS PATTERN switch to MAN.

7.10.2 Select an address at random with the ADDRESS switches.

7.10.3 Set the DATA switches in a random pattern. Depress and release the RESET button.

7.10.4 Depress and release the START button. The selected data will be written into the selected address.

7.10.5 Depress and release the Stop button. Set the READ/WRITE switch to READ.

7.10.6 Depress and release the START button. The data in this address location will be read out. If an error occurs, note this in the data sheet.

7.10.7 The operator should select 3 other addresses at random, repeating steps 7.10.2 through 7.10.6 to verify the random access capability.

7.11 NON-VOLATILITY TEST

7.11.1 Set the ADDRESS PATTERN switch to SEQ and the DATA PATTERN switch to MAN.

7.11.2 Set the DATA switches to a random pattern. Depress and release the RESET button. Set the READ/WRITE switch to WRITE.

7.11.3 Depress and release the START button. The tester will run through all 4096 addresses one time and then stop. Set the READ/WRITE switch to READ.

7.11.4 Turn memory power to OFF.
7.11.5 Depress and release the RESET button.

7.11.6 Turn memory power to ON.

7.11.7 Depress and release the START button. If any errors occur, record them on the data sheet. If no errors occur, no words were disturbed when the power was interrupted.

7.11.8 Depress and release the STOP button.

7.11.9 Repeat 7.11.4 through 7.11.8 four times. Record any errors.

7.12 MEMORY SELECT TEST

7.12.1 Set the ADDRESS PATTERN switch to SEQ and the DATA PATTERN switch to SEQ.

7.12.2 Set the MEMORY SELECT switches to 0000.

7.12.3 Depress and release the RESET button, then the START button. The tester should indicate an error at the first address. Record this address on the data sheet.

7.12.4 Repeat 7.12.3 with the memory select switches set to 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, and 1110.

7.12.5 Set the MEMORY SELECT switches to 1111.

7.12.6 Set the No. 0 switch on BD1 to the UP position. Depress and release the RESET button, then the START button. Allow the tester to run for 10 seconds. Record any errors. Depress and release the STOP button.
7.13 WORST CASE PATTERN TEST

7.13.1 Set the DATA PATTERN switch and the ADDRESS PATTERN switch to WC1. Turn the WC switch ON. Depress and release the STOP and RESET buttons.

7.13.2 Depress and release the START button. The tester will execute the following sequence:

A. Write a "1" in every bit of every word 2^{10} times.
B. Write a "0" once in every bit of every word under an even numbered word line in the stack.
C. Write a "1" in every bit of every word under an odd numbered word line and read the previously written "0" in every bit of every word under an even numbered word line until the operator sequences to the next group or until an error is detected. The READ light is lit during this cycle.

NOTE: If any error lights are ON when cycle C starts, disregard them and depress RESET one time prior to starting the one minute count. This applies to all worst-case pattern tests.

Run in cycle C for one minute. Record any errors on the data sheet.

7.13.3 Press and release the WC1 SEQ button. The tester will execute the preceding sequence, except "even" and "odd" are interchanged. The WC2^0 and WC2^1 lights will indicate the second WC1 group is under test. Record any errors.
7.13.4 Repeat 7.13.3 for WC1 groups 3 and 4 in which "1" and "0" are interchanged. Record any errors on the data sheet. Depress and release the STOP button. Turn the MEMORY POWER to OFF.

8. TEMPERATURE TEST

The temperature tests shall be conducted under normal laboratory conditions, with the exception of temperature.

8.1 TEST SETUP

Place the unit in the temperature chamber and establish the test setup as shown in Figure 3.

8.2 HIGH TEMPERATURE

Increase the chamber ambient temperature to \(+85^\circ C \pm 3^\circ C\). When the chamber has reached this temperature, note the time and set the DATA PATTERN and ADDRESS PATTERN switches to WC1. Turn the WC switch to ON. Turn MEMORY POWER to ON and depress the START button. Using the DVM, adjust the memory power supplies to \(+5.25 \pm 0.02V\) and \(-6.40 \pm 0.02V\). Depress the STOP button.

8.2.1 Repeat paragraphs 7.13.1 through 7.13.4. Record the results.

8.2.2 Set the MEMORY POWER switch to ON. Depress and release the START button. Using the DVM, adjust the memory power supplies to \(+4.75 \pm 0.02V\) and \(-5.80 \pm 0.02V\). Depress the STOP button.

8.2.3 Repeat paragraphs 7.13.1 through 7.13.4. Record the results.

8.2.4 Beginning 50 minutes after the temperature chamber has reached \(85^\circ C\) measure and record, on the data sheet, the thermistor resistance at 10 minute intervals. Do this by connecting the...
digital ohmmeter across the THERMISTOR terminals on the interface box. At each measurement, except the first one, calculate the percent change from the previous reading. When the change is less than 5 percent, proceed to paragraph 8.2.5.

8.2.5
Set the ADDRESS PATTERN and DATA PATTERN switches to SEQ. Turn the MEMORY POWER to ON. Using the DVM, adjust the memory power supplies to $+5.25 \pm 0.02V$ and $-6.40 \pm 0.02V$.

Measure and record the power supply voltage, current and standby (idle) power (paragraphs 7.7.1 through 7.7.3, except do not readjust the voltages).

8.2.6
Depress the START button. The memory shall run without error for 10 seconds. Record the results.

8.2.7
Adjust the pulse generator frequency to $500 \pm 1.0 \text{ KHz}$. Measure and record the operating power (paragraphs 7.7.5 through 7.7.7, except adjust the voltages to $+5.25 \pm 0.02V$ and $-6.40 \pm 0.02V$).

Depress the STOP button. Adjust the pulse generator frequency to $600 \pm 1.0 \text{ KHz}$.

8.2.8
Repeat paragraphs 7.13.1 through 7.13.4.

8.2.9
Set the MEMORY POWER switch to ON. Depress and release the START button. Using the DVM, adjust the memory power supplies to $+4.75 \pm 0.02V$ and $-5.80 \pm 0.02V$. Depress the STOP button.

8.2.10 Repeat paragraphs 7.13.1 through 7.13.4.
8.2.11 Set the MEMORY POWER switch to ON.
Set the +5V supply to 5.0V ± 0.02 and the -6.1V and to -6.1 ± 0.02V. Set the DATA PATTERN switch to MAN and the ADDRESS PATTERN switch to SEQ. Set the READ/WRITE switch to WRITE. Select a random pattern and push the START pushbutton. The tester will write the data once in each of the 4096 addresses and stop. Set the READ/WRITE switch to READ and push the START pushbutton. The memory shall run without error. After 10 seconds, push the STOP button. Record the results. Set MEMORY POWER to OFF.

8.3 LOW TEMPERATURE
Remove the oven door and let the memory unit cool to approximately room temperature. Place the memory unit in a plastic bag and again seal the chamber.

8.3.1 Decrease the chamber ambient temperature to -40° ± 3°C. When the chamber has reached this temperature, note the time. Monitor the thermistor resistance by connecting the digital ohmmeter across the THERMISTOR terminals on the interface box. When the termistor resistance has reached 29 Kohms, proceed to paragraph 8.3.2.

8.3.2 Set the DATA PATTERN and ADDRESS PATTERN switches to WC1. Turn the WC switch to ON. Turn MEMORY POWER to ON and depress the START button. Using the DVM, adjust the memory power supplies to +5.25 ± 0.02V and -6.40 ± 0.02V. Depress the STOP button.
8.3.3 Repeat paragraphs 7.13.1 through 7.13.4. Record the results.

8.3.4 Set the MEMORY POWER switch to ON. Depress the START button. Using the DVM, adjust the memory power supplies to \( +4.75 \pm 0.02V \) and \( -5.80 \pm 0.02V \). Depress the STOP button.

8.3.5 Repeat paragraphs 7.13.1 through 7.13.4. Record the results.

8.3.6 Beginning 150 minutes after the chamber temperature has reached \(-40^\circ C\), measure and record, in the data sheet, the thermistor resistance at 10 minute intervals. At each measurement, except the first one, calculate the percent change from the previous reading. When the change is less than 5 percent proceed to paragraph 8.3.7.

8.3.7 Depress the START button. The memory shall run without error for 10 seconds. Depress the STOP button and record the results.

8.3.8 Set the +5V supply to \( 5.25V \pm .02V \) and the -6.1V supply to \( -6.40 \pm .02V \). Measure and record the power supply volt & the standby power (paragraphs 7.7.1 through 7.7.3, except do not readjust the voltages).

8.3.9 Adjust the pulse generator frequency to \( 500 \pm 1.0 \) KHz. Set the DATA PATTERN and ADDRESS PATTERN switches to SEQ. Push the START pushbutton. Measure and record, in the data sheet, the operating power (paragraphs 7.7.5 through 7.7.7, except adjust the voltages to \( +5.25 \pm 0.02V \) and \( -6.40 \pm 0.02V \)).

Adjust the pulse generator frequency to \( 600 \pm 1.0 \) KHz.
8.3.10  Set the +5V supply to +4.75 ± 0.02V and the -6.1V supply to -5.80 ± 0.02V. Push the RESET button. The memory shall run without error for one minute. Depress the STOP button. Record the results in the data sheet.

8.3.11  Repeat paragraphs 7.13.1 through 7.13.4.

8.3.12  Set the MEMORY POWER switch to ON. Depress and release the START button. Using the DVM, adjust the memory power supplies to +5.25 ± 0.02V and -6.40 ± 0.02V. Depress the STOP button.

8.3.13  Repeat paragraphs 7.13.1 through 7.13.4.

8.3.14  Turn the memory power OFF.

9.  VACUUM TEST

9.1  SETUP

9.1.1  Verify that the MEMORY POWER switch on the Interface Box is in the OFF position. Turn the coarse voltage controls fully counterclockwise on all three power supplies. Connect the equipment as shown in Figure 3. Turn on power to all memory associated test equipment.
9.1.2 Set the Tester and Interface Box controls as follows and maintain these control settings unless otherwise directed in the individual tests.

<table>
<thead>
<tr>
<th>CONTROL</th>
<th>SETTING</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TESTER</strong></td>
<td></td>
</tr>
<tr>
<td>BD1-BD4 (24 Switches)</td>
<td>UP</td>
</tr>
<tr>
<td>Tape Reader Power</td>
<td>Light Off</td>
</tr>
<tr>
<td>Run-OFF-Rewind Switch</td>
<td>OFF</td>
</tr>
<tr>
<td>Tester Power</td>
<td>Light ON</td>
</tr>
<tr>
<td>ADDRESS Switches</td>
<td>DOWN</td>
</tr>
<tr>
<td>DATA Switches</td>
<td>DOWN</td>
</tr>
<tr>
<td>READ/WRITE</td>
<td>READ</td>
</tr>
<tr>
<td>WORD LENGTH</td>
<td>24</td>
</tr>
<tr>
<td>READ 1/READ 7 Switch</td>
<td>READ 7</td>
</tr>
<tr>
<td>ADDRESS PATTERN</td>
<td>SEQ</td>
</tr>
<tr>
<td>DATA PATTERN</td>
<td>SEQ</td>
</tr>
<tr>
<td>FREQUENCY</td>
<td>EXT</td>
</tr>
<tr>
<td><strong>INTERFACE BOX</strong></td>
<td></td>
</tr>
<tr>
<td>MEMORY SELECT SWITCHES</td>
<td>All 2.4V</td>
</tr>
<tr>
<td>INPUT CURRENT SWITCH</td>
<td>GND</td>
</tr>
<tr>
<td>OUTPUT PULLUP RESISTOR</td>
<td>4.5V</td>
</tr>
<tr>
<td>INITIATE PULSE SWITCH</td>
<td>PULSE</td>
</tr>
<tr>
<td>WC2 SWITCH</td>
<td>OFF</td>
</tr>
<tr>
<td>WC SWITCH</td>
<td>OFF</td>
</tr>
<tr>
<td>MEMORY POWER</td>
<td>OFF</td>
</tr>
</tbody>
</table>
9.1.3 Push the STOP button. Turn on all three power supplies. Using the DVM, adjust the Interface Box supply to \(+5.0 \pm 0.1V\). Set the memory supplies to approximately \(+5V\) and \(-6V\). Set the MEMORY POWER switch to ON. Using the DVM, adjust the memory supplies to \(+5.0 \pm 0.1V\) and \(-6.1 \pm 0.1V\). Set the memory power switch to OFF.

9.1.4 Using the scope, adjust the Pulse Generator for \(+3.0 \pm 0.1V\) positive pulses of \(450 \pm 10\) nanoseconds duration (measured at the 50% points). Using the counter, adjust the rep rate to \(600 \pm 1.0\) KHz. The pulse generator must be terminated in 50 ohms and connected to the tester when making these adjustments. Just prior to starting the environmental test, proceed to the next applicable paragraph.

9.2 TEST

Push the tester STOP and RESET pushbuttons. Turn the MEMORY POWER ON and push the START pushbutton on the tester. The tester will write a "0", read a "0" seven times in all data bits, write a "1", read a "1" seven times in all bits, step to the next address and repeat the same sequence. The tester will keep cycling until an error occurs. Record any bit errors. Proceed immediately to paragraph 9.2.1.
9.2.1 While monitoring the tester for errors, start the vacuum chamber pump and pump the air out of the vacuum chamber at a rate such that the pressure inside the chamber drops to 7 mmHg in less than five minutes. Record any errors.

9.2.2 Continue pumping the chamber until the pressure $10^{-5}$ mmHg. In order to reach this pressure, the test may last several hours. Therefore, one hour after the test has started, the memory and tester may be turned off by pushing the STOP pushbutton on the tester, turning the MEMORY POWER OFF and turning the TESTER POWER OFF. After the chamber has reached $10^{-5}$ mmHg, test the memory as outlined in paragraph 7.13. Record any errors. Push the memory STOP pushbutton, turn the MEMORY POWER OFF, turn the TESTER POWER OFF and return the memory to one atmosphere pressure.

10. VIBRATION TEST

The following vibration tests are to be performed in three mutually perpendicular axes. The tests include sine sweep and random vibration, and the levels to be used are described below in the individual tests. These levels are inputs to the base or mounting bracket of the unit under test. The unit shall be functionally tested during the vibration testing to insure correct operation. Prior to performing the random vibration a spectral analysis of the tester input shall be performed to insure that the random vibration input is within the specified limits. The analysis
shall be plotted and the data sheet kept as part of the test data. For information only, an accelerometer shall be mounted on the top surface of the housing while testing the X and Z axes. Plot the output from this accelerometer and file as part of the test data.

10.1 SINE SWEEP TEST

10.1.1 Verify that the MEMORY POWER switch is in the OFF position. Turn the coarse voltage controls fully counterclockwise on all three power supplies.

Connect the equipment as shown in Figure 3 and turn on power to all memory associated test equipment.


Mount the memory unit on the shake table so as to be vibrated in the vertical (Y) axis as shown in Figure 4. (The axis order may be varied for convenience).

10.1.2 Push the STOP and RESET buttons. Turn the MEMORY POWER ON.

Perform a sine sweep over the frequency range of 5-2000 Hz at the levels listed below:

<table>
<thead>
<tr>
<th>FREQUENCY RANGE</th>
<th>TEST LEVEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>5-25 Hz</td>
<td>0.33 in DA</td>
</tr>
<tr>
<td>24-110 Hz</td>
<td>10G PEAK</td>
</tr>
<tr>
<td>110-2000 Hz</td>
<td>5g PEAK</td>
</tr>
</tbody>
</table>

The sweep rate is to be 2 octaves per minute. During the sweep, repeatedly perform the tests of paragraph 7.13. Record any bit errors in the Qual Test Data Sheet. Push the STOP button.
10.2 RANDOM VIBRATION

10.2.1 Perform the spectral analysis specified in paragraph 10. While applying the following random vibration input, repeatedly perform the tests of paragraph 7.13.

<table>
<thead>
<tr>
<th>FREQUENCY RANGE</th>
<th>TEST LEVEL</th>
<th>TOLERANCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 Hz</td>
<td>.0044g²/Hz</td>
<td>± 3db</td>
</tr>
<tr>
<td>15-70 Hz</td>
<td>LINEAR INCREASE</td>
<td>Log-Log Plot</td>
</tr>
<tr>
<td>70-1000 Hz</td>
<td>.138 g²/Hz</td>
<td>± 3db</td>
</tr>
<tr>
<td>100-400 Hz</td>
<td>LINEAR DECREASE</td>
<td>Log-Log Plot</td>
</tr>
<tr>
<td>400-2000 Hz</td>
<td>.0089 g²/Hz</td>
<td>± 3db</td>
</tr>
</tbody>
</table>

The test time is to be 2 minutes per axis. Record any errors in the Data Record.

10.22 Repeat paragraph 10.1.2 and 10.2, in the two other mutually perpendicular axes as shown in Figure 4. Push the STOP button. Turn the MEMORY POWER OFF and then turn the TESTER POWER OFF.

11. SHOCK TEST

Two shocks in each direction shall be applied along the three mutually perpendicular axes of the LP RASM (total of 6 shocks).

11.1 SETUP

Verify that the MEMORY POWER switch is in the OFF position. Turn the coarse voltage controls fully counterclockwise on all three power supplies. Connect the equipment as shown in Figure 3 and apply power to all memory associated test equipment. Set the controls as shown in para. 9.1.2 and perform para. 9.1.3 and 9.1.4. Mount the LP RASM on the shock table so as to apply...
the shock in the vertical (Y) axis as shown in Figure 5. (The axes order may be varied for convenience).

11.2 TEST

11.2.1 Push the STOP and RESET buttons. Turn the MEMORY POWER ON and push the START button. The tester is now testing the LP RASM for bit errors. Apply a half sine shock pulse of 30 g's for a duration of 6 milliseconds. Record any bit errors. Push the STOP button.

11.2.2 Push the RESET and START buttons. Apply a half sine shock pulse of 30 g's for a duration of 12 milliseconds. Record any bit errors.

11.2.3 Repeat para. 11.2.1 and 11.2.2 for each of the other two directions as shown in Figure 5. Push the STOP button. Turn the MEMORY POWER OFF and then turn the TESTER POWER OFF.

12. FINAL FUNCTIONAL TESTS

To insure that the memory is still operating properly, perform all the tests of paragraph 7. Record the data.
FIGURE 1. LP RASM OUTLINE DIMENSIONS

MOTOROLA INC.
Government Electronics Division
8201 E. McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

SIZE  CODE IDENT NO.  DWG NO.
A    94990        12-P13722D

SCALE NONE  REVISION  SHEET  31

V.3.B.19811-IV4.2-69 DWG FORMAT
FIGURE 2. TEST SET UP
FIGURE 3. TEST SET UP
FIGURE 4. VIBRATION AXES
NOTE: ARROWS INDICATE DIRECTION OF SHOCK APPLIED TO THE LP RASM

FIGURE 5. SHOCK DIRECTIONS
<table>
<thead>
<tr>
<th>APPLICATION</th>
<th>REVISIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTR</td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>X1</td>
<td>Initial Release</td>
</tr>
<tr>
<td>X2</td>
<td>Incorporated changes prior to First Usage</td>
</tr>
<tr>
<td>X3</td>
<td>Change -6.9V to -6.1V</td>
</tr>
<tr>
<td>X4</td>
<td>Change 6000mw to 7000mw, pages 10, 17, 19, 30. Change weight from 6.0 to 6.5 pounds, page 2.</td>
</tr>
</tbody>
</table>

Asterisk indicates data which is nonmandatory—For information only.

This document cleared through QA Records Center.
SCOPE

This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

REFERENCE INFORMATION

3.1 SPECIFICATIONS APPLICABLE

S-562-P-24 Low Power Random Access Spacecraft Memory

12-P13722D Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. TEST DATA

Unit S/N 101 Start Date of Tests 10-25-73

Tested by

3.2 EQUVALENT TEST EQUIPMENT

COUNTER TS1 361-R
PULSE GEN. CH 138
MP 3442 PLUG-IN
DIGITEC 269 MULTIMETER
Oven Wyle 3600

4. PHYSICAL CHARACTERISTICS

6.1 WEIGHT

Weight of LP-RASM = 6.25 Pounds 6.5 pounds

MOTOROLA INC.

Government Electronics Division

SIZE CODE IDENT NO. DWG NO.
A 94990 12-P13722D

SCALE REVISION SHEET
Date of Test 10-25-7?
Tested By

6.2 DIMENSIONS

\[ V = 2.919 \text{ inches} \]
\[ W = 8.632 \text{ inches} \]
\[ L = 9.971 \text{ inches} \]
\[ D = 6.328 \text{ inches} \]
\[ MB = 7.180 \text{ inches} \]

\[ V = H \times W \times X \times D = 159.45 \text{ inches}^3 \]

\[ \leq 160 \text{ inches}^3 \]
7.4 CHASSIS ISOLATION

Impedance \( > 10 \text{ ma} \)

Limit
\( \geq 9 \text{ megohms} \)

7.5 INPUT SIGNAL LOADING

7.5.2 Current from INITIATE PULSE to Gnd \(109 \text{ ma} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to INITIATE PULSE \(11 \mu\text{a} \) \( \leq 20 \mu\text{a} \)

7.5.3 Current from MEM SEL 1 to Gnd \(629 \text{ ma} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to MEM SEL 1 \(1.09 \mu\text{a} \) \( \leq 20 \mu\text{a} \)

7.5.4 Current from MEM SEL 2 to Gnd \(671 \text{ ma} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to MEM SEL 2 \(1.58 \mu\text{a} \) \( \leq 20 \mu\text{a} \)

Current from MEM SEL 3 to Gnd \(676 \text{ ma} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to MEM SEL 3 \(1.62 \mu\text{a} \) \( \leq 20 \mu\text{a} \)

Current from MEM SEL 4 to Gnd \(633 \text{ ma} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to MEM SEL 4 \(112 \mu\text{a} \) \( \leq 20 \mu\text{a} \)

7.5.5 Current from READ/WRITE to Gnd \(761 \text{ ma} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to READ/WRITE \(206 \mu\text{a} \) \( \leq 20 \mu\text{a} \)

7.5.6 Current from ADDRESS 2° to Gnd \(921 \text{ ma} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to ADDRESS 2° \(66 \mu\text{a} \) \( \leq 20 \mu\text{a} \)
Current from ADDRESS 2\textsuperscript{1} to Gnd \(923\) mA
Current from 2.4V to ADDRESS 2\textsuperscript{1} \(70\) \(\mu\)A
Current from ADDRESS 2\textsuperscript{2} to Gnd \(931\) mA
Current from 2.4V to ADDRESS 2\textsuperscript{2} \(68\) \(\mu\)A
Current from ADDRESS 2\textsuperscript{3} to Gnd \(931\) mA
Current from 2.4V to ADDRESS 2\textsuperscript{3} \(64\) \(\mu\)A
Current from ADDRESS 2\textsuperscript{4} to Gnd \(927\) mA
Current from 2.4V to ADDRESS 2\textsuperscript{4} \(63\) \(\mu\)A

Limits
\(\leq 2\) mA
\(\leq 20\) \(\mu\)A
\(\leq 2\) mA
\(\leq 20\) \(\mu\)A
\(\leq 2\) mA
\(\leq 20\) \(\mu\)A
\(\leq 2\) mA
\(\leq 20\) \(\mu\)A
Current from ADDRESS 2\textsuperscript{6} to Gnd \(-0.7\) ma
Current from 2.4V to ADDRESS 2\textsuperscript{6} \(-0.86\) \(\mu\)a

Current from ADDRESS 2\textsuperscript{7} to Gnd \(-0.1\) ma
Current from 2.4V to ADDRESS 2\textsuperscript{7} \(-0.86\) \(\mu\)a

Current from ADDRESS 2\textsuperscript{8} to Gnd \(-0.937\) ma
Current from 2.4V to ADDRESS 2\textsuperscript{8} \(-0.50\) \(\mu\)a

Current from ADDRESS 2\textsuperscript{9} to Gnd \(-0.897\) ma
Current from 2.4V to ADDRESS 2\textsuperscript{9} \(-0.51\) \(\mu\)a

Current from ADDRESS 2\textsuperscript{10} to Gnd \(-0.917\) ma
Current from 2.4V to ADDRESS 2\textsuperscript{10} \(-2.02\) \(\mu\)a

Current from ADDRESS 2\textsuperscript{11} to Gnd \(-0.896\) ma
Current from 2.4V to ADDRESS 2\textsuperscript{11} \(-2.03\) \(\mu\)a

Current from DATA IN BIT 0 to Gnd \(-0.972\) ma
Current from 2.4V to DATA IN BIT 0 \(-0.21\) \(\mu\)a

\(\checkmark\)
Current from DATA IN BIT 1 to Gnd  9.72 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 1  23 µa  ≤ 20 µa
Current from DATA IN BIT 2 to Gnd  9.84 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 2  21 µa  ≤ 20 µa
Current from DATA IN BIT 3 to Gnd  8.54 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 3  9.3 µa  ≤ 20 µa
Current from DATA IN BIT 4 to Gnd  8.58 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 4  1.01 µa  ≤ 20 µa
Current from DATA IN BIT 5 to Gnd  8.41 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 5  1.01 µa  ≤ 20 µa
Current from DATA IN BIT 6 to Gnd  1.182 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 6  1.01 µa  ≤ 20 µa
Current from DATA IN BIT 7 to Gnd  1.122 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 7  9.9 µa  ≤ 20 µa
Current from DATA IN BIT 8 to Gnd  1.193 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 8  1.03 µa  ≤ 20 µa
Current from DATA IN BIT 9 to Gnd  8.433 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 9  8.0 µa  ≤ 20 µa
Current from DATA IN BIT 10 to Gnd: 834 ma
Current from 2.4V to DATA IN BIT 10: 70 μA

Current from DATA IN BIT 11 to Gnd: 826 ma
Current from 2.4V to DATA IN BIT 11: 68 μA

Current from DATA IN BIT 12 to Gnd: 839 ma
Current from 2.4V to DATA IN BIT 12: 92 μA

Current from DATA IN BIT 13 to Gnd: 832 ma
Current from 2.4V to DATA IN BIT 13: 80 μA

Current from DATA IN BIT 14 to Gnd: 839 ma
Current from 2.4V to DATA IN BIT 14: 80 μA

Current from DATA IN BIT 15 to Gnd: 835 ma
Current from 2.4V to DATA IN BIT 15: 90 μA

Current from DATA IN BIT 16 to Gnd: 832 ma
Current from 2.4V to DATA IN BIT 16: 59 μA

Current from DATA IN BIT 17 to Gnd: 832 ma
Current from 2.4V to DATA IN BIT 17: 104 μA

Limits:

- 2 ma
- 20 μA
7.6  VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS

7.6.3 READ COMPLETE voltage = 80 mv ≤ 100 mv

7.6.4 DATA OUT BIT 0 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 1 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 2 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 3 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 4 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 5 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 6 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 7 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 8 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 9 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 10 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 11 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 12 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 13 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 14 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 15 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 16 voltage ≤ 80 mv ≤ 100 mv
DATA OUT BIT 17 voltage ≤ 80 mv ≤ 100 mv
S/N 101

Date of Test 10-25-73
Tested By

limits

7.7 POWER CONSUMPTION (25°C)

7.7.1 Memory +5V Voltage 5.003 Volts
Memory -6.1V voltage -6.104 Volts
+5V Current 10.5 ma
+5V Power 52.5 mw

7.7.2 Memory -6.1V Current 3.2 ma
Memory -6.1V Power 19.5 mw

7.7.3 Total Memory Idle Power 72.0 mw

7.7.5 Memory +5V Voltage 5.00 Volts
Memory -6.1V Voltage -6.10 Volts
+5V Current 675 ma
+5V Power 2375 mw

7.7.6 Memory -6.1V Current 165 ma
Memory -6.1V Power 1606.5 mw

7.7.7 Total Active Power 4381.5 mw

7.8 READ COMPLETE TIMING

7.8.5 Delay 360 ns
Duration 300 ns

500 ns max.

250 ns min

450 ns max.
Date of Test 10-25-28
Tested by [Signature]

7.8.7 & 7.8.8
READ COMPLETE/DATA OUTPUT TIMING

<table>
<thead>
<tr>
<th>DO</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>1</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>2</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>3</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>4</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>5</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>6</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>7</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>8</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>9</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>10</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>11</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>12</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>13</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>14</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>15</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>16</td>
<td>OK X REJECT</td>
</tr>
<tr>
<td>17</td>
<td>OK X REJECT</td>
</tr>
</tbody>
</table>

LIMITS

REJECT

REFER TO TEST PROC.
7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?
No [X]  
Yes ___ Address ___ Bits ___  0 errors

7.9.4 Did an error occur?
No [X]  
Yes ___ Address ___ Bits ___  0 errors

7.9.10 Did an error occur?
No [X]  
Yes ___ Address ___ Bits ___  0 errors

7.9.16 Did an error occur?
No [X]  
Yes ___ Address ___ Bits ___  0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?
No [X]  
Yes ___ Address ___ Bits ___  0 errors

7.10.7 Did an error occur?
  a) No [X]  
    Yes ___ Address ___ Bits ___  0 errors
b) No  
Yes Address  Bits  0 errors

c) No  
Yes Address  Bits  0 errors

7.11  NON-VOLATILITY TEST

7.11.7  Did an error occur?
&  No  
7.11.9  Yes Address  Bits  0 errors

7.12  MEMORY SELECT TEST

7.12.3  Address 0000  (Octal)  0000

7.12.4  Address 0001 0000  (Octal)  0000
        0010 0000  (Octal)  0000
        0011 0000  (Octal)  0000
        0100 0000  (Octal)  0000
        0101 0000  (Octal)  0000
        0110 0000  (Octal)  0000
        0111 0000  (Octal)  0000
        1000 0000  (Octal)  0000
        1001 0000  (Octal)  0000
        1010 0000  (Octal)  0000
S/N 101

Date of Test 10-25-??
Tested By

Address 1011 0000 (Octal)
1100 0000 (Octal)
1101 0000 (Octal)
1110 0000 (Octal)

7.12.6 Did an error occur?
No  
Yes  Address  Bits  0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?
No  
Yes  Address  Bits  0 errors

7.13.3 Did an error occur?
No  
Yes  Address  Bits  0 errors

MOTOROLA INC.
Government Electronics Division

8201 E. McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

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S/N 101

Date of Test 10-25-73
Tested By MVE

7.23.4
a) Did an error occur?
   No X
   Yes _____ Address _____ Bit _____ 0 errors

b) Did an error occur?
   No X
   Yes _____ Address _____ Bit _____ 0 errors
S/N 101  Date of Test 10-25-73

Tested by AMR

8. TEMPERATURE TEST +85°C at 10:45 A

8.2.1 Did any errors occur?
   No  X
   Yes Address  0 Errors
   Bits

8.2.3 Did any errors occur?
   No  X
   Yes Address  0 Errors
   Bits

8.2.4 HIGH TEMPERATURE
Thermal Resistance
   50 minutes  1,950 K ohms
   60 minutes  1,809 K ohms % change 7.2
   70 minutes  1,722 K ohms % change 4.8
   80 minutes  ___ K ohms % change
   90 minutes  ___ K ohms % change

8.2.5 -6.1V Voltage -6.40 Volts +5V Voltage 5.25 Volts
   -6.1V Current  5.0 ma +5V Current 11.6 ma
   -6.1V Power  32 mw +5V Power 60.9 mv

   Total Memory Idle Power  92.9 mw

   170 mw max.
3.3.6 Did an error occur?
No  
Yes  Address  Bit  0 errors

3.2.7 -6.1V Voltage 6.40 Volts +5V Voltage 5.25 Volts
-6.1V Current 306 ma +5V Current 8.25 ma
-6.1V Power 1958.4 mw +5V Power 4334.3 mw

Total Memory Operate Power 6289.7 mw 7000 mw max.

8.2.8 WC a) Did an error occur?
No 
Yes  Address  Bits  0 Errors

WC b) Did an error occur?
No  
Yes  Address  Bits  0 Errors

WC c) Did an error occur?
No 
Yes  Address  Bits  0 Errors

WC d) Did an error occur?
No  
Yes  Address  Bits  0 Errors
S/N 101

DATE of TEST 10-25-78
Tested by

8.2.10 Did any errors occur?
No
Yes Address

Limits
0 Errors

8.2.11 Did an error occur?
No
Yes Address

0 Errors

8.3 Low Temperature -40°C at 1:35 P

8.3.3 Did any errors occur?
No
Yes Address

0 Errors

8.3.5 Did any errors occur?
No
Yes Address

0 Errors

MOTOROLA INC.
Government Electronics Division

8201 E. McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

AV-2-B-199H-100A-3 69 DFG FORMAT
8.3.6 LOW TEMPERATURE

Thermal Resistance

<table>
<thead>
<tr>
<th>Time</th>
<th>Resistance (K ohms)</th>
<th>% Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>150 min</td>
<td>144.0</td>
<td></td>
</tr>
<tr>
<td>160 min</td>
<td>146.4</td>
<td>3.1</td>
</tr>
<tr>
<td>170 min</td>
<td></td>
<td></td>
</tr>
<tr>
<td>180 min</td>
<td></td>
<td></td>
</tr>
<tr>
<td>190 min</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

8.3.7 Did an error occur?

No [X]

Yes [ ]

Address [ ]

Bits [ ]

0 Errors

8.3.8 -6.1V Voltage 6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 10.9 ma +5V Current 11.0 ma

-6.1V Power 69.8 mw +5V Power 57.8 mw

Total Memory Idle Power 127.6 mw

170 mw max.

8.3.9 -6.1V Voltage 6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 285 ma +5V Current 743 ma

-6.1V Power 1824 mw +5V Power 39008 mw

Total Memory Operate Power 5724.8 mw

7000 mw max.
S/N 101

Date of Test 10-25-73
Tested By

8.3.10 Did an error occur?
No 
Yes _____ Address _____ Bits _____ 0 Errors

8.3.11 WC a) Did an error occur?
No 
Yes _____ Address _____ Bits _____ 0 Errors

WC b) Did an error occur?
No 
Yes _____ Address _____ Bits _____ 0 Errors

WC c) Did an error occur?
No 
Yes _____ Address _____ Bits _____ 0 Errors

WC d) Did an error occur?
No 
Yes _____ Address _____ Bits _____ 0 Errors

8.3.13 Did any errors occur?
No 
Yes _____ Address _____ Bits _____ 0 Errors
<table>
<thead>
<tr>
<th>TIME</th>
<th>PRESSURE (mm Hg A)</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0930</td>
<td>0.14</td>
<td></td>
</tr>
<tr>
<td>0935</td>
<td>1.00</td>
<td></td>
</tr>
<tr>
<td>1030</td>
<td>1.25x10^-5</td>
<td></td>
</tr>
<tr>
<td>1120</td>
<td>1.3x10^-5</td>
<td></td>
</tr>
<tr>
<td>1215</td>
<td>1.2x10^-6</td>
<td></td>
</tr>
<tr>
<td>1300</td>
<td>2.3x10^-6</td>
<td>Go To Hi Vac</td>
</tr>
<tr>
<td>1330</td>
<td>1.5x10^-6</td>
<td></td>
</tr>
<tr>
<td>1400</td>
<td>6x10^-7</td>
<td></td>
</tr>
<tr>
<td>1430</td>
<td>5.3x10^-7</td>
<td></td>
</tr>
<tr>
<td>1520</td>
<td>5x10^-7</td>
<td></td>
</tr>
<tr>
<td>1535</td>
<td>4.6x10^-7</td>
<td></td>
</tr>
<tr>
<td>1620</td>
<td>4.3x10^-7</td>
<td></td>
</tr>
<tr>
<td>0345</td>
<td>1.3x10^-5</td>
<td>Go To Hi Vac</td>
</tr>
<tr>
<td>0400</td>
<td>6.3x10^-6</td>
<td></td>
</tr>
<tr>
<td>0430</td>
<td>4.3x10^-7</td>
<td></td>
</tr>
<tr>
<td>0535</td>
<td>3.5x10^-7</td>
<td></td>
</tr>
<tr>
<td>0615</td>
<td>3.5x10^-7</td>
<td></td>
</tr>
<tr>
<td>0720</td>
<td>2.1x10^-6</td>
<td></td>
</tr>
<tr>
<td>0815</td>
<td>2.1x10^-6</td>
<td>VENT To Atm.</td>
</tr>
</tbody>
</table>
9. VACUUM TEST

9.2 Did Any Bit Errors Occur?

No X
Yes Address _______ Bits _______ 0 Errors

9.2.1 Fast Decompression

Date 10-26-73 Tested by MHE

Did Any Bit Errors Occur?

No X
Yes Address _______ Bits _______ 0 Errors

9.2.2 Hard Vacuum

Date 10-29-73 Tested by MHE

Did Any Bit Errors Occur?

No X
Yes Address _______ Bits _______ 0 Errors

10. VIBRATION TEST

Date 10-29-73 Tested by MHE

SINE SWEEP

Axis X - Did Any Bit Errors Occur?

No X
Yes _______ Freq _____ Address _____ Bits _____ 0 Errors
<table>
<thead>
<tr>
<th>Axis</th>
<th>Time Start</th>
<th>Time Stop</th>
<th>Total Time</th>
<th>E.P</th>
<th>G rms</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>15:35</td>
<td>15:36</td>
<td>20 sec</td>
<td></td>
<td>5.64g</td>
<td>shaped random</td>
</tr>
<tr>
<td>X</td>
<td>15:40</td>
<td>15:41</td>
<td>20 sec</td>
<td></td>
<td>5.64g</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>15:49</td>
<td>15:50</td>
<td>20 sec</td>
<td></td>
<td>5.64g</td>
<td>plot accel curve</td>
</tr>
<tr>
<td>X</td>
<td>16:23</td>
<td>16:25</td>
<td>2 min</td>
<td></td>
<td>5.64g</td>
<td>shaped random</td>
</tr>
<tr>
<td>X</td>
<td>1630</td>
<td>1634</td>
<td>4 sec</td>
<td>.33</td>
<td>10 F 5.0</td>
<td>5-2 KHZ</td>
</tr>
<tr>
<td>Z</td>
<td>1650</td>
<td>1654</td>
<td>4 sec</td>
<td>.33</td>
<td>10 F 5.0</td>
<td></td>
</tr>
<tr>
<td>Z</td>
<td>1705</td>
<td>1707</td>
<td>2 min</td>
<td></td>
<td>5.64 RMS</td>
<td>shaped random noise</td>
</tr>
<tr>
<td>Y</td>
<td>1917</td>
<td>1919</td>
<td>2 min</td>
<td></td>
<td>5.64 RMS</td>
<td></td>
</tr>
<tr>
<td>Y</td>
<td>1923</td>
<td>1927</td>
<td>4 sec</td>
<td>.33</td>
<td>10 F 5.0</td>
<td>5-2 KHZ</td>
</tr>
</tbody>
</table>

Remarks:
- Shaped Random Noise
FILTER B.W. 1. 5Hz SCAN RATE 1.125Hz AVG. TIME: 10 SECONDS
2.10Hz SCAN RATE 2.25Hz AVG. TIME 10 SECONDS
3.20Hz SCAN RATE 3.50Hz AVG TIME: 10 SECONDS
4.50Hz SCAN RATE 4.25Hz AVG TIME: 10 SECONDS

FREQ. RANGE 1. 15-20Hz MOTOROLA SIMULATION
20-40
10-100
100-2K

MEDIAN TIMES 10/29/73
10/29/73
10/29/73
10/29/73

Response acceler (in axis) top of unit

97
FILTER B.W. 1.5 HZ SCAN RATE 1.125 HZ AVG. TIME 10 SECONDS
2.0 HZ SCAN RATE 2.25 HZ AVG. TIME 10 SECONDS
3.20 HZ SCAN RATE 3.5 HZ AVG. TIME 10 SECONDS
4.50 HZ SCAN RATE 1.25 HZ AVG. TIME 10 SECONDS

FREQ. RANGE 1.5-20 HZ MOTOROLA 5000
PROJECT 7195 UNIT 01-P13701D001 SER. NO. 101

X & Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 Hz SCAN RATE 1:125 Hz AVG. TIME 1.10 SECONDS
2. 10 Hz SCAN RATE 2:25 Hz AVG. TIME 2.10 SECONDS
3. 20 Hz SCAN RATE 3:5 Hz AVG. TIME 3.10 SECONDS
4. 50 Hz SCAN RATE 4:2 Hz AVG. TIME 4.10 SECONDS

FREQ. RANGE 1. 15-20 Hz MOTOROLA SPECIFICATION NO.
2. 20-10 Hz CUSTOMER SPECIFICATION NO.
3. 100-20 Hz
4. 100-2K Hz

VIBRATION DATE 10/29/73
DATE ANALYZED 10/23/73 L. Pat. Norton

VIBRATION TOLERANCE LEVEL ±36B

REMARKS

100
SHOCK TEST
(DROP)

Date 11-2-73

Sheet 1 of 19/2

Project 7195

Unit PW 41

Operator Earl

Observer Ken C. Wood

Vibration Mounts None

No. of drops on each axis 2 Total of 6

Acceleration 302 \frac{3}{2} \text{ ipm}

Duration 6 Milliseconds ±10%.

| Axis | Face | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|------|------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|
| A    | 1    | 1 |   |   |   |   |   |   |   |   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
|      | 2    |   |   |   |   |   |   |   |   |   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   | 1   |
| B    | 1    |   |   |   |   |   | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
|      | 2    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| C    | 1    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|      | 2    |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

Notes:
- 10.5 mm ±0.01
- 1 in 3rd phase 25° ±3°
- 25° out of phase
- 25° out of phase
- 101
- 4300 Hz
Date of Test: 10-29-73
Tested by: [signature]

Axis Z - Did Any Bit Error Occur?

No

Yes

Freq

Address

Bits

0 Errors

Axis Z - Did Any Bit Errors Occur?

No

Yes

Freq

Address

Bits

0 Errors

RANDOM VIBRATION

Axis X - Did Any Bit Errors Occur?

No

Yes

Freq

Address

Bits

0 Errors

Axis Y - Did Any Bit Errors Occur?

No

Yes

Freq

Address

Bits

0 Errors

Axis Z - Did Any Bit Errors Occur?

No

Yes

Freq

Address

Bits

0 Errors

11. SHOCK TEST

Date: 11-2-73
Tested by: [signature]

6 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No

Yes

Freq

Address

Bits

0 Errors
Z Direction - Did Any Bit Errors Occur?
No  
Yes   Address  Bits  0 Errors

X Direction - Did Any Bit Errors Occur?
No  
Yes   Address  Bits  0 Errors

12 MILLISECOND DURATION SHOCK
Y Direction - Did Any Bit Errors Occur?
No  
Yes   Address  Bits  0 Errors

Z Direction - Did Any Bit Errors Occur?
No  
Yes   Address  Bits  0 Errors

X Direction - Did Any Bit Errors Occur?
No  
Yes   Address  Bits  0 Errors
7.4 CHASSIS ISOLATION

Impedance \( \geq 10\,\text{megohms} \)

Limit \( \leq 9\,\text{megohms} \)

7.5 INPUT SIGNAL LOADING

7.5.2 Current from INITIATE PULSE to Gnd \( 0.92\,\text{ma} \)
Current from 2.4V to INITIATE PULSE \( 1.19\,\text{µa} \)

7.5.3 Current from MEM SEL 1 to Gnd \( 1.088\,\text{ma} \)
Current from 2.4V to MEM SEL 1 \( 0.66\,\text{µa} \)

7.5.4 Current from MEM SEL 2 to Gnd \( 1.092\,\text{ma} \)
Current from 2.4V to MEM SEL 2 \( 1.16\,\text{µa} \)
Current from MEM SEL 3 to Gnd \( 1.092\,\text{ma} \)
Current from 2.4V to MEM SEL 3 \( 1.22\,\text{µa} \)

7.5.5 Current from READ/WRITE to Gnd \( 1.43\,\text{ma} \)
Current from 2.4V to READ/WRITE \( 2.11\,\text{µa} \)

7.5.6 Current from ADDRESS \( 0 \) to Gnd \( 9.23\,\text{ma} \)
Current from 2.4V to ADDRESS \( 0 \) \( 7.2\,\text{µa} \)
Current from ADDRESS 2\(^1\) to Gnd \(0.928\) ma
Current from 2.4V to ADDRESS 2\(^1\) \(0.75\) \(\mu\)a

Current from ADDRESS 2\(^2\) to Gnd \(0.932\) ma
Current from 2.4V to ADDRESS 2\(^2\) \(0.73\) \(\mu\)a

Current from ADDRESS 2\(^3\) to Gnd \(0.934\) ma
Current from 2.4V to ADDRESS 2\(^3\) \(0.68\) \(\mu\)a

Current from ADDRESS 2\(^4\) to Gnd \(0.921\) ma
Current from 2.4V to ADDRESS 2\(^4\) \(0.68\) \(\mu\)a

Limits
\(\leq 2\) ma
\(\leq 20\ \mu\)a
S/N 101

Date of Test 11-2-72

Tested By

Current from ADDRESS 2\(^5\) to Gnd \(0.825\) ma
Current from 2.4V to ADDRESS 2\(^5\) \(1.05\) \(\mu\)a

Limits
\(\leq 2\) ma
\(\leq 20\mu\)a

Current from ADDRESS 2\(^6\) to Gnd \(0.938\) ma
Current from 2.4V to ADDRESS 2\(^5\) \(0.67\) \(\mu\)a

\(\leq 2\) ma
\(\leq 20\mu\)a

Current from ADDRESS 2\(^7\) to Gnd \(0.818\) ma
Current from 2.4V to ADDRESS 2\(^7\) \(0.91\) \(\mu\)a

\(\leq 2\) ma
\(\leq 20\mu\)a

Current from ADDRESS 2\(^8\) to Gnd \(0.942\) ma
Current from 2.4V to ADDRESS 2\(^8\) \(0.54\) \(\mu\)a

\(\leq 2\) ma
\(\leq 20\mu\)a

Current from ADDRESS 2\(^9\) to Gnd \(0.919\) ma
Current from 2.4V to ADDRESS 2\(^9\) \(0.55\) \(\mu\)a

\(\leq 2\) ma
\(\leq 20\mu\)a

Current from ADDRESS 2\(^{10}\) to Gnd \(0.920\) ma
Current from 2.4V to ADDRESS 2\(^{10}\) \(0.15\) \(\mu\)a

\(\leq 2\) ma
\(\leq 20\mu\)a

Current from ADDRESS 2\(^{11}\) to Gnd \(0.922\) ma
Current from 2.4V to ADDRESS 2\(^{11}\) \(0.11\) \(\mu\)a

\(\leq 2\) ma
\(\leq 20\mu\)a

Current from DATA IN BIT 0 to Gnd \(0.976\) ma
Current from 2.4V to DATA IN BIT 0 \(0.24\) \(\mu\)a

\(\leq 2\) ma
\(\leq 20\mu\)a
Current from DATA IN BIT 1 to Gnd 998 ma  \leq 2 ma
Current from 2.4V to DATA IN BIT 1 26 \mu a  \leq 20 \mu a
Current from DATA IN BIT 2 to Gnd 995 ma  \leq 2 ma
Current from 2.4V to DATA IN BIT 2 25 \mu a  \leq 20 \mu a
Current from DATA IN BIT 3 to Gnd 866 ma  \leq 2 ma
Current from 2.4V to DATA IN BIT 3 99 \mu a  \leq 20 \mu a
Current from DATA IN BIT 4 to Gnd 862 ma  \leq 2 ma
Current from 2.4V to DATA IN BIT 4 108 \mu a  \leq 20 \mu a
Current from DATA IN BIT 5 to Gnd 550 ma  \leq 2 ma
Current from 2.4V to DATA IN BIT 5 107 \mu a  \leq 20 \mu a
Current from DATA IN BIT 6 to Gnd 192 ma  \leq 2 ma
Current from 2.4V to DATA IN BIT 6 107 \mu a  \leq 20 \mu a
Current from DATA IN BIT 7 to Gnd 230 ma  \leq 2 ma
Current from 2.4V to DATA IN BIT 7 105 \mu a  \leq 20 \mu a
Current from DATA IN BIT 8 to Gnd 219 ma  \leq 2 ma
Current from 2.4V to DATA IN BIT 8 110 \mu a  \leq 20 \mu a
Current from DATA IN BIT 9 to Gnd 847 ma  \leq 2 ma
Current from 2.4V to DATA IN BIT 9 85 \mu a  \leq 20 \mu a
Current from DATA IN BIT 10 to Gnd \(842\) ma \(\leq\) 2 ma
Current from 2.4V to DATA IN BIT 10 \(75\) \(\mu\)a \(\leq\) 20\(\mu\)a

Current from DATA IN BIT 11 to Gnd \(830\) ma \(\leq\) 2 ma
Current from 2.4V to DATA IN BIT 11 \(72\) \(\mu\)a \(\leq\) 20\(\mu\)a

Current from DATA IN BIT 12 to Gnd \(852\) ma \(\leq\) 2 ma
Current from 2.4V to DATA IN BIT 12 \(97\) \(\mu\)a \(\leq\) 20\(\mu\)a

Current from DATA IN BIT 13 to Gnd \(838\) ma \(\leq\) 2 ma
Current from 2.4V to DATA IN BIT 14 \(84\) \(\mu\)a \(\leq\) 20\(\mu\)a

Current from DATA IN BIT 14 to Gnd \(843\) ma \(\leq\) 2 ma
Current from 2.4V to DATA IN BIT 14 \(85\) \(\mu\)a \(\leq\) 20\(\mu\)a

Current from DATA IN BIT 15 to Gnd \(838\) ma \(\leq\) 2 ma
Current from 2.4V to DATA IN BIT 15 \(84\) \(\mu\)a \(\leq\) 20\(\mu\)a

Current from DATA IN BIT 16 to Gnd \(841\) ma \(\leq\) 2 ma
Current from 2.4V to DATA IN BIT 17 \(95\) \(\mu\)a \(\leq\) 20\(\mu\)a

Current from DATA IN BIT 17 to Gnd \(834\) ma \(\leq\) 2 ma
Current from 2.4V to DATA IN BIT 17 \(1010\) \(\mu\)a \(\leq\) 20\(\mu\)a
7.6 VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS

7.6.3 READ COMPLETE voltage 50 mv

<table>
<thead>
<tr>
<th>DATA OUT BIT</th>
<th>Voltage</th>
<th>Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>60 mv</td>
<td>100 mv</td>
</tr>
<tr>
<td>1</td>
<td>60 mv</td>
<td>100 mv</td>
</tr>
<tr>
<td>2</td>
<td>90 mv</td>
<td>100 mv</td>
</tr>
<tr>
<td>3</td>
<td>100 mv</td>
<td>100 mv</td>
</tr>
<tr>
<td>4</td>
<td>90 mv</td>
<td>100 mv</td>
</tr>
<tr>
<td>5</td>
<td>90 mv</td>
<td>100 mv</td>
</tr>
<tr>
<td>6</td>
<td>90 mv</td>
<td>100 mv</td>
</tr>
<tr>
<td>7</td>
<td>95 mv</td>
<td>100 mv</td>
</tr>
<tr>
<td>8</td>
<td>90 mv</td>
<td>100 mv</td>
</tr>
<tr>
<td>9</td>
<td>90 mv</td>
<td>100 mv</td>
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<tr>
<td>10</td>
<td>90 mv</td>
<td>100 mv</td>
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<tr>
<td>11</td>
<td>90 mv</td>
<td>100 mv</td>
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<tr>
<td>12</td>
<td>80 mv</td>
<td>100 mv</td>
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<tr>
<td>13</td>
<td>90 mv</td>
<td>100 mv</td>
</tr>
<tr>
<td>14</td>
<td>92 mv</td>
<td>100 mv</td>
</tr>
<tr>
<td>15</td>
<td>95 mv</td>
<td>100 mv</td>
</tr>
<tr>
<td>16</td>
<td>95 mv</td>
<td>100 mv</td>
</tr>
<tr>
<td>17</td>
<td>100 mv</td>
<td>100 mv</td>
</tr>
</tbody>
</table>
7.7 POWER CONSUMPTION (25°C)

7.7.1 Memory +5V Voltage  5.00 Volts
Memory -6.1V voltage -6.10 Volts
+5V Current  9.8 ma
+5V Power  49.0 mw

7.7.2 Memory -6.1V Current  3.0 ma
Memory -6.1V Power  18.3 mw

7.7.3 Total Memory Idle Power 67.3 mw

7.7.5 Memory +5V Voltage  5.00 Volts
Memory -6.1V Voltage -6.10 Volts
+5V Current  8/11 ma
+5V Power  4055 mw

7.7.6 Memory -6.1V Current  300 ma
Memory -6.1V Power  1830 mw

7.7.7 Total Active Power  5885 mw

7.8 READ COMPLETE TIMING

7.8.5 Delay  350 ns
Duration  275 ns

Date of Test  11-2-2
Tested By  WAC

MOTOROLA INC.
Government Electronics Division
8201 E. MCDOUGALL ROAD
SCOTTSDALE, ARIZONA 85262

SIZE CODE IDENT NO. DWG NO. SCALE REVISION SHEET
A 94990 12-P13721D 30
<table>
<thead>
<tr>
<th>DO</th>
<th>Status</th>
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</thead>
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</tr>
<tr>
<td>DO-1</td>
<td>OK</td>
</tr>
<tr>
<td>DO-2</td>
<td>OK</td>
</tr>
<tr>
<td>DO-3</td>
<td>OK</td>
</tr>
<tr>
<td>DO-4</td>
<td>OK</td>
</tr>
<tr>
<td>DO-5</td>
<td>OK</td>
</tr>
<tr>
<td>DO-6</td>
<td>OK</td>
</tr>
<tr>
<td>DO-7</td>
<td>OK</td>
</tr>
<tr>
<td>DO-8</td>
<td>OK</td>
</tr>
<tr>
<td>DO-9</td>
<td>OK</td>
</tr>
<tr>
<td>DO-10</td>
<td>OK</td>
</tr>
<tr>
<td>DO-11</td>
<td>OK</td>
</tr>
<tr>
<td>DO-12</td>
<td>OK</td>
</tr>
<tr>
<td>DO-13</td>
<td>OK</td>
</tr>
<tr>
<td>DO-14</td>
<td>OK</td>
</tr>
<tr>
<td>DO-15</td>
<td>OK</td>
</tr>
<tr>
<td>DO-16</td>
<td>OK</td>
</tr>
<tr>
<td>DO-17</td>
<td>OK</td>
</tr>
</tbody>
</table>

**Limits**

Refer to test proc.
7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?
No X
Yes Address Bits 0 errors

7.9.4 Did an error occur?
No X
Yes Address Bits 0 errors

7.9.10 Did an error occur?
No X
Yes Address Bits 0 errors

7.9.16 Did an error occur?
No X
Yes Address Bits 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?
No X
Yes Address Bits 0 errors

7.10.7 Did an error occur?
a) No X
Yes Address Bits 0 errors
7.11 NON-VOLATILITY TEST

7.11.7 Did an error occur?

7.11.9 No X

Yes Address Bits 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal) 0000

7.12.4 Address 0001 0000 (Octal) 0000
0010 0000 (Octal) 0000
0011 0000 (Octal) 0000
0100 0000 (Octal) 0000
0101 0000 (Octal) 0000
0110 0000 (Octal) 0000
0111 0000 (Octal) 0000
1000 0000 (Octal) 0000
1001 0000 (Octal) 0000
1010 0000 (Octal) 0000
S/N 101

Date of Test 11-2-73
Tested By __________

Address

1011 0000 (Octal)
1100 0000 (Octal)
1101 0000 (Octal)
1110 0000 (Octal)

7.12.6 Did an error occur?
No  
Yes ___ Address ___ Bits ___ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?
No  
Yes ___ Address ___ Bits ___ 0 errors

7.13.3 Did an error occur?
No  
Yes ___ Address ___ Bits ___ 0 errors
7.13.4 a) Did an error occur?
    No [X]
    Yes [ ] Address [ ] Bit [ ]
    0 errors

b) Did an error occur?
    No [X]
    Yes [ ] Address [ ] Bit [ ]
    0 errors
<table>
<thead>
<tr>
<th>LTR</th>
<th>DESCRIPTION</th>
<th>DATE</th>
<th>APPROVED</th>
</tr>
</thead>
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<tr>
<td>X1</td>
<td>Initial Release</td>
<td></td>
<td></td>
</tr>
<tr>
<td>X2</td>
<td>Incorporated changes prior to First Usage</td>
<td>3-12-73</td>
<td></td>
</tr>
<tr>
<td>X3</td>
<td>Change -6.9V to -6.1V</td>
<td>6-18-73</td>
<td></td>
</tr>
<tr>
<td>X4</td>
<td>Change 6000mw to 7000mw, pages 10, 17, 19, 30. Change weight from 6.0 to 6.5 pounds, page 2.</td>
<td>7-24-73</td>
<td></td>
</tr>
</tbody>
</table>

**Note:**
- Sterisk indicates data which is not mandatory for information only.

**THIS DOCUMENT CLEARED THROUGH QA RECORDS CENTER**

**MOTOROLA INC.**
Government Electronics Division
8241 East McDowell Road
Scottsdale, Arizona 85252

**ACCEPTANCE TEST DATA SHEET,**
LOW POWER RANDOM ACCESS SPACE-CHT-3401, PAGE NO. 01-P13721D

**SIZE**
94990
**CONFIDENTIAL**

**SCALE**
SHEET 1 OF 33
1. **SCOPE**
   This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

2. **REFERENCE INFORMATION**

2.1 **SPECIFICATIONS APPLICABLE**

- **S-562-P-24**
  Low Power Random Access Spacecraft Memory

- **12-P13722D**
  Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. **TEST DATA**

   Unit S/N 101
   Start Date of Tests 2-13-74
   Tested by [Signature]

4. **PHYSICAL CHARACTERISTICS**

4.1 **WEIGHT**

   Weight of LP-RASM - N/A
   Pounds 6.5

---

[Signature]

[Stamp]
6.2 DIMENSIONS

H = _________ inches

W = _________ inches

MW = _________ inches

D = _________ inches

MD = _________ inches

V = H x W x D = _________ inches³
    ≤ 160 inches³
S/N 121  

Date of Test: 2-13-74
Tested By: [Signature]

7.4 CHASSIS ISOLATION
Impedance: \( \geq 10 \, \text{M} \Omega \)

Limit
\( \geq 9 \, \text{megohms} \)

7.5 INPUT SIGNAL LOADING

7.5.2 Current from INITIATE PULSE to Gnd \( \leq 2 \, \text{ma} \)
Current from 2.4V to INITIATE PULSE \( \leq 20 \, \mu \text{A} \)

7.5.3 Current from MEM SEL 1 to Gnd \( \leq 2 \, \text{ma} \)
Current from 2.4V to MEM SEL 1 \( \leq 20 \, \mu \text{A} \)

7.5.4 Current from MEM SEL 2 to Gnd \( \leq 2 \, \text{ma} \)
Current from 2.4V to MEM SEL 2 \( \leq 20 \, \mu \text{A} \)

7.5.5 Current from MEM SEL 3 to Gnd \( \leq 2 \, \text{ma} \)
Current from 2.4V to MEM SEL 3 \( \leq 20 \, \mu \text{A} \)

7.5.6 Current from MEM SEL 4 to Gnd \( \leq 2 \, \text{ma} \)
Current from 2.4V to MEM SEL 4 \( \leq 20 \, \mu \text{A} \)

7.5.5 Current from READ/WRITE to Gnd \( \leq 2 \, \text{ma} \)
Current from 2.4V to READ/WRITE \( \leq 20 \, \mu \text{A} \)

7.5.6 Current from ADDRESS \( 2^0 \) to Gnd \( \leq 2 \, \text{ma} \)
Current from 2.4V to ADDRESS \( 2^0 \) \( \leq 20 \, \mu \text{A} \)
S/N 101

Date of Test 2-13-74

Tested By ___

Current from ADDRESS 2<sup>1</sup> to Gnd _____ ma

Current from 2.4V to ADDRESS 2<sup>1</sup> _____ µa

Current from ADDRESS 2<sup>2</sup> to Gnd _____ ma

Current from 2.4V to ADDRESS 2<sup>2</sup> _____ µa

Current from ADDRESS 2<sup>3</sup> to Gnd _____ ma

Current from 2.4V to ADDRESS 2<sup>3</sup> _____ µa

Current from ADDRESS 2<sup>4</sup> to Gnd _____ ma

Current from 2.4V to ADDRESS 2<sup>4</sup> _____ µa

Limits

N/A ≤ 2 ma

N/A ≤ 20 µa

N/A ≤ 2 ma

N/A ≤ 20 µa

N/A ≤ 2 ma

N/A ≤ 20 µa
<table>
<thead>
<tr>
<th>Address</th>
<th>Current Flow</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>$2^5$</td>
<td>N/A ma</td>
<td>$\leq 2$ ma</td>
</tr>
<tr>
<td>$2^7$</td>
<td>N/A $\mu$A</td>
<td>$\leq 20 \mu$A</td>
</tr>
<tr>
<td>$2^8$</td>
<td>N/A ma</td>
<td>$\leq 2$ ma</td>
</tr>
<tr>
<td>$2^9$</td>
<td>N/A $\mu$A</td>
<td>$\leq 20 \mu$A</td>
</tr>
<tr>
<td>$2^{10}$</td>
<td>N/A ma</td>
<td>$\leq 2$ ma</td>
</tr>
<tr>
<td>$2^{11}$</td>
<td>N/A $\mu$A</td>
<td>$\leq 20 \mu$A</td>
</tr>
</tbody>
</table>

MOTOROLA INC.
Government Electronics Division

SIZE | CODE IDENT NO. | DWG NO.
--- | -------------- | --------
A    | 94990          | 12-M721D

AV-2-8-1973-1001-3/69 DWG FORMAT
<table>
<thead>
<tr>
<th>Current from</th>
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</tr>
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<tbody>
<tr>
<td>DATA IN BIT 1 to Gnd</td>
<td>N/A ma ≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 1</td>
<td>μa ≤ 20 μa</td>
</tr>
<tr>
<td>DATA IN BIT 2 to Gnd</td>
<td>ma ≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 2</td>
<td>μa ≤ 20 μa</td>
</tr>
<tr>
<td>DATA IN BIT 3 to Gnd</td>
<td>ma ≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 3</td>
<td>μa ≤ 20 μa</td>
</tr>
<tr>
<td>DATA IN BIT 4 to Gnd</td>
<td>ma ≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 4</td>
<td>μa ≤ 20 μa</td>
</tr>
<tr>
<td>DATA IN BIT 5 to Gnd</td>
<td>ma ≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 5</td>
<td>μa ≤ 20 μa</td>
</tr>
<tr>
<td>DATA IN BIT 6 to Gnd</td>
<td>ma ≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 6</td>
<td>μa ≤ 20 μa</td>
</tr>
<tr>
<td>DATA IN BIT 7 to Gnd</td>
<td>ma ≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 7</td>
<td>μa ≤ 20 μa</td>
</tr>
<tr>
<td>DATA IN BIT 8 to Gnd</td>
<td>ma ≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 8</td>
<td>μa ≤ 20 μa</td>
</tr>
<tr>
<td>DATA IN BIT 9 to Gnd</td>
<td>ma ≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 9</td>
<td>N/A μa ≤ 20 μa</td>
</tr>
<tr>
<td>Current</td>
<td>Limits</td>
</tr>
<tr>
<td>---------</td>
<td>----------</td>
</tr>
<tr>
<td>to Gnd</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>N/A</td>
<td>( \leq 20\mu \text{ a} )</td>
</tr>
<tr>
<td>2.4V</td>
<td>( \leq 20\mu \text{ a} )</td>
</tr>
<tr>
<td>( \mu \text{ a} )</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>( \mu \text{ a} )</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>( \mu \text{ a} )</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>( \mu \text{ a} )</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>( \mu \text{ a} )</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>( \mu \text{ a} )</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>( \mu \text{ a} )</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
</tbody>
</table>

**Notes:**
- Current from Data IN BIT 10 to Gnd: N/A
- Current from 2.4V to DATA IN BIT 10: \( \mu \text{ a} \)
- Current from 2.4V to DATA IN BIT 11: \( \mu \text{ a} \)
- Current from 2.4V to DATA IN BIT 12: \( \mu \text{ a} \)
- Current from 2.4V to DATA IN BIT 13: \( \mu \text{ a} \)
- Current from 2.4V to DATA IN BIT 14: \( \mu \text{ a} \)
- Current from 2.4V to DATA IN BIT 15: \( \mu \text{ a} \)
- Current from 2.4V to DATA IN BIT 16: \( \mu \text{ a} \)
- Current from 2.4V to DATA IN BIT 17: \( \mu \text{ a} \)

**Date of Test:** 2-13-74

**Tested By:**

---

**MOTOROLA INC.**

**Government Electronics Division**

**Address:**
8201 E. McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

**Sheet 8**
7.6 VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS

7.6.3 READ COMPLETE voltage N/A mv 

7.6.4 DATA OUT BIT 0 voltage mv 
DATA OUT BIT 1 voltage mv 
DATA OUT BIT 2 voltage mv 
DATA OUT BIT 3 voltage mv 
DATA OUT BIT 4 voltage mv 
DATA OUT BIT 5 voltage mv 
DATA OUT BIT 6 voltage mv 
DATA OUT BIT 7 voltage mv 
DATA OUT BIT 8 voltage mv 
DATA OUT BIT 9 voltage mv 
DATA OUT BIT 10 voltage mv 
DATA OUT BIT 11 voltage mv 
DATA OUT BIT 12 voltage mv 
DATA OUT BIT 13 voltage mv 
DATA OUT BIT 14 voltage mv 
DATA OUT BIT 15 voltage mv 
DATA OUT BIT 16 voltage mv 
DATA OUT BIT 17 voltage N/A mv 

Limit

≤ 100 mv
7.7 POWER CONSUMPTION (25°C)

7.7.1 Memory +5V Voltage 5.00 Volts
Memory -6.1V Voltage -6.10 Volts
+5V Current 8.9 ma
+5V Power 3.5 3.6 mw 44.5 mw

7.7.2 Memory -6.1V Current 3.6 ma
Memory -6.1V Power 21.9 mw

7.7.3 Total Memory Idle Power 66.4 mw 170 mw max

7.7.5 Memory +5V Voltage 5.00 Volts
Memory -6.1V Voltage -6.10 Volts
+5V Current 670 ma
+5V Power 3350 250 mw

7.7.6 Memory -6.1V Current 250 ma
Memory -6.1V Power 1525 mw

7.7.7 Total Active Power 4875 mw 7000 mw max.

7.8 READ COMPLETE TIMING

7.8.5 Delay N/A ns
Duration N/A ns

500 ns max.
250 ns min
450 ns max.
**S/N** 101  
**Date of Test** 2-13-74  
**Tested by** [signature]

<table>
<thead>
<tr>
<th>DO-0</th>
<th>OK</th>
<th>N/A</th>
<th>REJECT</th>
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<td></td>
</tr>
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<td>DO-2</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
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<tr>
<td>DO-3</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
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<td>DO-4</td>
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<td>OK</td>
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<td>DO-16</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-17</td>
<td>OK</td>
<td>N/A</td>
<td>REJECT</td>
</tr>
</tbody>
</table>

**LIMITS**

**REFER TO TEST PROC.**
7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?
No X
Yes __ Address ___ Bits ___ 0 errors

7.9.4 Did an error occur?
No X
Yes __ Address ___ Bits ___ 0 errors

7.9.10 Did an error occur?
No X
Yes __ Address ___ Bits ___ 0 errors

7.9.16 Did an error occur?
No X
Yes __ Address ___ Bits ___ 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?
No X
Yes __ Address ___ Bits ___ 0 errors

7.10.7 Did an error occur?
a) No X
Yes __ Address ___ Bits ___ 0 errors
7.11 NON-VOLATILITY TEST

7.11.7 Did an error occur?
&
7.11.9 No

Yes Address Bits 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal)

7.12.4 Address 0001 0000 (Octal)
0010 0000 (Octal)
0011 0000 (Octal)
0100 0000 (Octal)
0101 0000 (Octal)
0110 0000 (Octal)
0111 0000 (Octal)
1000 0000 (Octal)
1001 0000 (Octal)
1010 0000 (Octal)

0000
0000
0000
0000
0000
0000
0000
0000
0000
0000
S/N 101

Date of Test 2-13-74
Tested By

Address 1011 0000 (Octal)
1100 0000 (Octal)
1101 0000 (Octal)
1110 0000 (Octal)

7.12.6 Did an error occur?
No
Yes Address ___ Bits ___ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?
No
Yes Address ___ Bits ___ 0 errors

7.13.3 Did an error occur?
No
Yes Address ___ Bits ___ 0 errors

MOTOROLA INC.
Government Electronics Division
8281 E. Mcdowell Road
Scottsdale, Arizona 85252

SIZE CODE IDENT NO. DRAW NO.
A 94990 12-P13721D

SCALE REVISION SHEET

14
a) Did an error occur?

No \(\times\)
Yes ___ Address ___ Bit ___

0 errors

b) Did an error occur?

No \(\times\)
Yes ___ Address ___ Bit ___

0 errors
S/N 101

Date of Test 2-13-74

Tested by

8. TEMPERATURE TEST +85°C at 9:05 A

8.2.1 Did any errors occur?

No

Yes Address

0 Errors

8.2.3 Did any errors occur?

No

Yes Address

0 Errors

8.2.4 HIGH TEMPERATURE

Thermal Resistance

50 minutes 1.755 K ohms

60 minutes 1.615 K ohms % change 7.9

70 minutes 1.512 K ohms % change 6.3

80 minutes 1.454 K ohms % change 3.8

90 minutes K ohms % change

8.2.5 -6.1V Voltage -6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 5.2 ma +5V Current 10 ma

-6.1V Power 33.3 mw +5V Power 52.5 mv

Total Memory Idle Power 85.8 mw 170 mw max.

MOTOROLA INC.
Government Electronics Division

SIZE CODE IDENT NO. DWG NO.
A 94990 12-P13721D

SCALE REVISION SHEET
8.2.6  Did an error occur?

No  
Yes  Address  Bit  0 errors

8.2.7  
-6.1V Voltage 6.40 Volts  
+5V Voltage 5.25 Volts  
-6.1V Current 300 ma  
+5V Current 770 ma  
-6.1V Power 1920 mw  
+5V Power 4043 mwv

Total Memory Operate Power 5963 mw  
7000 mw max.

8.2.8  
WC a)  Did an error occur?

No  
Yes  Address  Bits  0 Errors

WC b)  Did an error occur?

No  
Yes  Address  Bits  0 Errors

WC c)  Did an error occur?

No  
Yes  Address  Bits  0 Errors

WC d)  Did an error occur?

No  
Yes  Address  Bits  0 Errors
8.2.10 Did any errors occur?

No  X

Yes Address

Bits

8.2.11 Did an error occur?

No  X

Yes Address

Bits

8.3 Low Temperature -40°C at 12:25.

8.3.3 Did any errors occur?

No  X

Yes Address

Bits

8.3.5 Did any errors occur?

No  X

Yes Address

Bits

Limits

0 Errors

0 Errors

0 Errors
8.3.6 LOW TEMPERATURE

Thermal Resistance

150 minutes 4.70 K ohms
160 minutes 150.1 K ohms % change 2.1
170 minutes ______ K ohms % change _______
180 minutes ______ K ohms % change _______
190 minutes ______ K ohms % change _______

8.3.7 Did an error occur? Limits
No X
Yes _____ Address _____ Bits _____ 0 Errors

8.3.8 -6.1V Voltage 6.40 Volts +5V Voltage 5.25 Volts
-6.1V Current 10.5 ma +5V Current 9.3 ma
-6.1V Power 67.2 mv +5V Power 46.6 mv

Total Memory Idle Power 116 mv 170 mv max.

8.3.9 -6.1V Voltage 6.40 Volts +5V Voltage 5.25 Volts
-6.1V Current 220 ma +5V Current 685 ma
-6.1V Power 1228 mw +5V Power 3596 mv

Total Memory Operate Power 5324 mw 7000 mw max.
8.3.10 Did an error occur?
No ☒
Yes _____ Address _____ Bits _____ 0 Errors

8.3.11 WC a) Did an error occur?
No ☒
Yes _____ Address _____ Bits _____ 0 Errors

WC b) Did an error occur?
No ☒
Yes _____ Address _____ Bits _____ 0 Errors

WC c) Did an error occur?
No ☒
Yes _____ Address _____ Bits _____ 0 Errors

WC d) Did an error occur?
No ☒
Yes _____ Address _____ Bits _____ 0 Errors

8.3.13 Did any errors occur?
No ☒
Yes _____ Address _____ Bits _____ 0 Errors
S/N  N/A  Date of Test    
Tested by            

9.  VACUUM TEST

9.2  Did Any Bit Errors Occur?
No       
Yes     Address _____   Bits _____   0 Errors

9.2.1  Fast Decompression
Date ______  Tested by ______

Did Any Bit Errors Occur?
No       
Yes     Address _____   Bits _____   0 Errors

9.2.2  Hard Vacuum
Date ______  Tested by ______

Did Any Bit Errors Occur?
No       
Yes     Address _____   Bits _____   0 Errors

10.  VIBRATION TEST

Date ______  Tested by ______

SINE SWEEP
Axis X - Did Any Bit Errors Occur?
No       
Yes     Freq _____  Address _____   Bits _____   0 Errors
Axis Y - Did Any Bit Error Occur?

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Axis Z - Did Any Bit Errors Occur?

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**RANDOM VIBRATION**

Axis X - Did Any Bit Errors Occur?

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Axis Y - Did Any Bit Errors Occur?

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Axis Z - Did Any Bit Errors Occur?

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**SHOCK TEST**

Date | Tested By
---|---

6 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

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<td>Address</td>
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</table>
S/N N/A

Date of Test

Tested by

Limits

Z Direction - Did Any Bit Errors Occur?

No

Yes Address Bits 0 Errors

X Direction - Did Any Bit Errors Occur?

No

Yes Address Bits 0 Errors

12 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No

Yes Address Bits 0 Errors

Z Direction - Did Any Bit Errors Occur?

No

Yes Address Bits 0 Errors

X Direction - Did Any Bit Errors Occur?

No

Yes Address Bits 0 Errors
S/N: N/A          Date of Test: __________  
Tested By: __________

7.4  CHASSIS ISOLATION

Impedance: __________

Limit: ≥ 9 megohms

7.5  INPUT SIGNAL LOADING

7.5.2  Current from INITIATE PULSE to Gnd: ___ ma  ≤ 2 ma

Current from 2.4V to INITIATE PULSE: ___ μa  ≤ 20 μa

7.5.3  Current from MEM SEL 1 to Gnd: ___ ma  ≤ 2 ma

Current from 2.4V to MEM SEL 1: ___ μa  ≤ 20 μa

7.5.4  Current from MEM SEL 2 to Gnd: ___ ma  ≤ 2 ma

Current from 2.4V to MEM SEL 2: ___ μa  ≤ 20 μa

Current from MEM SEL 3 to Gnd: ___ ma  ≤ 2 ma

Current from 2.4V to MEM SEL 3: ___ μa  ≤ 20 μa

Current from MEM SEL 4 to Gnd: ___ ma  ≤ 2 ma

Current from 2.4V to MEM SEL 4: ___ μa  ≤ 20 μa

7.5.5  Current from READ/WRITE to Gnd: ___ ma  ≤ 2 ma

Current from 2.4V to READ/WRITE: ___ μa  ≤ 20 μa

7.5.6  Current from ADDRESS 2⁰ to Gnd: ___ ma  ≤ 2 ma

Current from 2.4V to ADDRESS 2⁰: ___ μa  ≤ 20 μa
Current from ADDRESS 2₁ to Gnd ______ ma  
Current from 2.4V to ADDRESS 2₁ ______ μa  
Current from ADDRESS 2₂ to Gnd ______ ma  
Current from 2.4V to ADDRESS 2₂ ______ μa  
Current from ADDRESS 2₃ to Gnd ______ ma  
Current from 2.4V to ADDRESS 2₃ ______ μa  
Current from ADDRESS 2₄ to Gnd ______ ma  
Current from 2.4V to ADDRESS 2₄ ______ μa

Limits

≤ 2 ma
≤ 20 μa
≤ 2 ma
≤ 20 μa
≤ 2 ma
≤ 20 μa
≤ 2 ma
≤ 20 μa
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<th>Current from 2.4V to Address</th>
<th>Limits</th>
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<td>$\leq 2 \text{ ma}$</td>
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<td>$\mu A$</td>
<td>$\leq 20 \mu A$</td>
</tr>
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<td>$2^6$ to Gnd</td>
<td>$\mu A$</td>
<td>$\leq 2 \text{ ma}$</td>
</tr>
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<td>$\mu A$</td>
<td>$\leq 2 \text{ ma}$</td>
</tr>
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<td>$2^7$ to Gnd</td>
<td>$\mu A$</td>
<td>$\leq 20 \mu A$</td>
</tr>
<tr>
<td>$2^8$ to Gnd</td>
<td>$\mu A$</td>
<td>$\leq 2 \text{ ma}$</td>
</tr>
<tr>
<td>$2^8$ to Gnd</td>
<td>$\mu A$</td>
<td>$\leq 20 \mu A$</td>
</tr>
<tr>
<td>$2^9$ to Gnd</td>
<td>$\mu A$</td>
<td>$\leq 2 \text{ ma}$</td>
</tr>
<tr>
<td>$2^9$ to Gnd</td>
<td>$\mu A$</td>
<td>$\leq 20 \mu A$</td>
</tr>
<tr>
<td>$2^{10}$ to Gnd</td>
<td>$\mu A$</td>
<td>$\leq 2 \text{ ma}$</td>
</tr>
<tr>
<td>$2^{10}$ to Gnd</td>
<td>$\mu A$</td>
<td>$\leq 20 \mu A$</td>
</tr>
<tr>
<td>$2^{11}$ to Gnd</td>
<td>$\mu A$</td>
<td>$\leq 2 \text{ ma}$</td>
</tr>
<tr>
<td>$2^{11}$ to Gnd</td>
<td>$\mu A$</td>
<td>$\leq 20 \mu A$</td>
</tr>
<tr>
<td>Data IN Bit 0</td>
<td>$\mu A$</td>
<td>$\leq 2 \text{ ma}$</td>
</tr>
<tr>
<td>Data IN Bit 0</td>
<td>$\mu A$</td>
<td>$\leq 20 \mu A$</td>
</tr>
</tbody>
</table>
S/N: N/A

Current from DATA IN BIT 1 to Gnd: __________ ma
Current from 2.4V to DATA IN BIT 1: _______ μa

Current from DATA IN BIT 2 to Gnd: __________ ma
Current from 2.4V to DATA IN BIT 2: _______ μa

Current from DATA IN BIT 3 to Gnd: __________ ma
Current from 2.4V to DATA IN BIT 3: _______ μa

Current from DATA IN BIT 4 to Gnd: __________ ma
Current from 2.4V to DATA IN BIT 4: _______ μa

Current from DATA IN BIT 5 to Gnd: __________ ma
Current from 2.4V to DATA IN BIT 5: _______ μa

Current from DATA IN BIT 6 to Gnd: __________ ma
Current from 2.4V to DATA IN BIT 6: _______ μa

Current from DATA IN BIT 7 to Gnd: __________ ma
Current from 2.4V to DATA IN BIT 7: _______ μa

Current from DATA IN BIT 8 to Gnd: __________ ma
Current from 2.4V to DATA IN BIT 8: _______ μa

Current from DATA IN BIT 9 to Gnd: __________ ma
Current from 2.4V to DATA IN BIT 9: _______ μa

Limit:
- Current from DATA IN BIT 1 to Gnd: ≤ 2 ma
- Current from DATA IN BIT 1 to Gnd: ≤ 20 μa
- Current from 2.4V to DATA IN BIT 1: ≤ 2 ma
- Current from 2.4V to DATA IN BIT 1: ≤ 20 μa
- Current from DATA IN BIT 2 to Gnd: ≤ 2 ma
- Current from DATA IN BIT 2 to Gnd: ≤ 20 μa
- Current from 2.4V to DATA IN BIT 2: ≤ 2 ma
- Current from 2.4V to DATA IN BIT 2: ≤ 20 μa
- Current from DATA IN BIT 3 to Gnd: ≤ 2 ma
- Current from DATA IN BIT 3 to Gnd: ≤ 20 μa
- Current from 2.4V to DATA IN BIT 3: ≤ 2 ma
- Current from 2.4V to DATA IN BIT 3: ≤ 20 μa
- Current from DATA IN BIT 4 to Gnd: ≤ 2 ma
- Current from DATA IN BIT 4 to Gnd: ≤ 20 μa
- Current from 2.4V to DATA IN BIT 4: ≤ 2 ma
- Current from 2.4V to DATA IN BIT 4: ≤ 20 μa
- Current from DATA IN BIT 5 to Gnd: ≤ 2 ma
- Current from DATA IN BIT 5 to Gnd: ≤ 20 μa
- Current from 2.4V to DATA IN BIT 5: ≤ 2 ma
- Current from 2.4V to DATA IN BIT 5: ≤ 20 μa
- Current from DATA IN BIT 6 to Gnd: ≤ 2 ma
- Current from DATA IN BIT 6 to Gnd: ≤ 20 μa
- Current from 2.4V to DATA IN BIT 6: ≤ 2 ma
- Current from 2.4V to DATA IN BIT 6: ≤ 20 μa
- Current from DATA IN BIT 7 to Gnd: ≤ 2 ma
- Current from DATA IN BIT 7 to Gnd: ≤ 20 μa
- Current from 2.4V to DATA IN BIT 7: ≤ 2 ma
- Current from 2.4V to DATA IN BIT 7: ≤ 20 μa
- Current from DATA IN BIT 8 to Gnd: ≤ 2 ma
- Current from DATA IN BIT 8 to Gnd: ≤ 20 μa
- Current from 2.4V to DATA IN BIT 8: ≤ 2 ma
- Current from 2.4V to DATA IN BIT 8: ≤ 20 μa
- Current from DATA IN BIT 9 to Gnd: ≤ 2 ma
- Current from DATA IN BIT 9 to Gnd: ≤ 20 μa
- Current from 2.4V to DATA IN BIT 9: ≤ 2 ma
- Current from 2.4V to DATA IN BIT 9: ≤ 20 μa
S/N N/A

Date of Test __________
Tested By __________

Current from DATA IN BIT 10 to Gnd __________ ma
Current from 2.4V to DATA IN BIT 10 __________ μA

Current from DATA IN BIT 11 to Gnd __________ ma
Current from 2.4V to DATA IN BIT 11 __________ μA

Current from DATA IN BIT 12 to Gnd __________ ma
Current from 2.4V to DATA IN BIT 12 __________ μA

Current from DATA IN BIT 13 to Gnd __________ ma
Current from 2.4V to DATA IN BIT 14 __________ μA

Current from DATA IN BIT 14 to Gnd __________ ma
Current from 2.4V to DATA IN BIT 14 __________ μA

Current from DATA IN BIT 15 to Gnd __________ ma
Current from 2.4V to DATA IN BIT 15 __________ μA

Current from DATA IN BIT 16 to Gnd __________ ma
Current from 2.4V to DATA IN BIT 17 __________ μA

Current from DATA IN BIT 17 to Gnd __________ ma
Current from 2.4V to DATA IN BIT 17 __________ μA

Limits

- Current from DATA IN BIT 10 to Gnd: \( \leq 2 \text{ ma} \)
- Current from 2.4V to DATA IN BIT 10: \( \leq 20 \mu\text{A} \)
- Current from DATA IN BIT 11 to Gnd: \( \leq 2 \text{ ma} \)
- Current from 2.4V to DATA IN BIT 11: \( \leq 20 \mu\text{A} \)
- Current from DATA IN BIT 12 to Gnd: \( \leq 2 \text{ ma} \)
- Current from 2.4V to DATA IN BIT 12: \( \leq 20 \mu\text{A} \)
- Current from DATA IN BIT 13 to Gnd: \( \leq 2 \text{ ma} \)
- Current from 2.4V to DATA IN BIT 14: \( \leq 20 \mu\text{A} \)
- Current from DATA IN BIT 14 to Gnd: \( \leq 2 \text{ ma} \)
- Current from 2.4V to DATA IN BIT 14: \( \leq 20 \mu\text{A} \)
- Current from DATA IN BIT 15 to Gnd: \( \leq 2 \text{ ma} \)
- Current from 2.4V to DATA IN BIT 15: \( \leq 20 \mu\text{A} \)
- Current from DATA IN BIT 16 to Gnd: \( \leq 2 \text{ ma} \)
- Current from 2.4V to DATA IN BIT 17: \( \leq 20 \mu\text{A} \)
- Current from DATA IN BIT 17 to Gnd: \( \leq 2 \text{ ma} \)
- Current from 2.4V to DATA IN BIT 17: \( \leq 20 \mu\text{A} \)
7.6  VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS

7.6.3  READ COMPLETE voltage _______  mv  ≤ 100  mv

7.6.4  DATA OUT BIT 0 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 1 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 2 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 3 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 4 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 5 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 6 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 7 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 8 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 9 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 10 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 11 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 12 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 13 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 14 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 15 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 16 voltage _______  mv  ≤ 100  mv
 DATA OUT BIT 17 voltage _______  mv  ≤ 100  mv
7.7 POWER CONSUMPTION (25°C)

7.7.1 Memory +5V Voltage ________ Volts
Memory -6.1V voltage ________ Volts
+5V Current ________ ma
+5V Power ________ mw

7.7.2 Memory -6.1V Current ________ ma
Memory -6.1V Power ________ mw

7.7.3 Total Memory Idle Power ________ mw 170 mw max

7.7.5 Memory +5V Voltage ________ Volts
Memory -6.1V Voltage ________ Volts
+5V Current ________ ma
+5V Power ________ mw

7.7.6 Memory -6.1V Current ________ ma
Memory -6.1V Power ________ mw

7.7.7 Total Active Power ________ mw 7000 mw max.

7.8 READ COMPLETE TIMING

7.8.5 Delay ________ ns 500 ns max.
Duration ________ ns 250 ns min
450 ns max.
<table>
<thead>
<tr>
<th>S/N</th>
<th>Date of Test</th>
<th>Tested by</th>
</tr>
</thead>
</table>

**LIMITS**

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<th>READ COMPLETE/DATA OUTPUT TIMING</th>
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<td>OK __________ REJECT __________</td>
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<tr>
<td>DO-1</td>
<td>OK __________ REJECT __________</td>
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<tr>
<td>DO-2</td>
<td>OK __________ REJECT __________</td>
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<td>DO-6</td>
<td>OK __________ REJECT __________</td>
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<td>DO-15</td>
<td>OK __________ REJECT __________</td>
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<tr>
<td>DO-16</td>
<td>OK __________ REJECT __________</td>
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<tr>
<td>DO-17</td>
<td>OK __________ REJECT __________</td>
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REFER TO TEST PROC.
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<th>Description</th>
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<th>Address</th>
<th>Bits</th>
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<td>Address</td>
<td>Bits</td>
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<td>Bits</td>
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<td>Bits</td>
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<td>Bits</td>
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<td>Address</td>
<td>Bits</td>
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<td></td>
<td></td>
<td>b) Yes</td>
<td>Address</td>
<td>Bits</td>
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<tr>
<td></td>
<td></td>
<td>c) No</td>
<td>Address</td>
<td>Bits</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>d) Yes</td>
<td>Address</td>
<td>Bits</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

S/N: N/A
Date of Test: 
Tested By: 
Limits:
**Non-Volatility Test**

7.11.7 Did an error occur?

<table>
<thead>
<tr>
<th>Address (Octal)</th>
<th>Bits</th>
<th>Errors</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>0001</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>0010</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>0011</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>0100</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>0101</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>0110</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>0111</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>1000</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>1001</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>1010</td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

**Memory Select Test**

7.12.3 Address (Octal)

<table>
<thead>
<tr>
<th>Address (Octal)</th>
<th>Bits</th>
<th>Errors</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

**S/N N/A**

**Date of Test**

**Tested By**

**Limits**

- 0 errors
S/N N/A

Date of Test

Tested By

Limits

Address 1011 (Octal) 0000
1100 (Octal) 0000
1101 (Octal) 0000
1110 (Octal) 0000

7.12.6 Did an error occur?
No _____
Yes _____ Address _____ Bits ______ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?
No _____
Yes _____ Address _____ Bits ______ 0 errors

7.13.3 Did an error occur?
No _____
Yes _____ Address _____ Bits ______ 0 errors
Date of Test 2-12-74
Tested By _

S/N _ N/A

7.13.4 a) Did an error occur?

No ___
Yes ___ Address ____ Bit ____ 0 errors

b) Did an error occur?

No ___
Yes ___ Address ____ Bit ____ 0 errors

L150

LIMITS
<table>
<thead>
<tr>
<th>REV</th>
<th>X1</th>
<th>X4</th>
<th>X3</th>
<th>X1</th>
<th>X1</th>
<th>X1</th>
<th>X1</th>
<th>X1</th>
<th>X1</th>
<th>X1</th>
<th>X1</th>
<th>X1</th>
</tr>
</thead>
<tbody>
<tr>
<td>SHEET</td>
<td>27</td>
<td>28</td>
<td>29</td>
<td>30</td>
<td>31</td>
<td>32</td>
<td>33</td>
<td>34</td>
<td>35</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>REV STATUS</th>
<th>REV</th>
<th>OF SHEETS</th>
<th>SHEET</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1</td>
<td>X4</td>
<td>1</td>
<td>2</td>
</tr>
</tbody>
</table>

<table>
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<tr>
<th>LTR</th>
<th>DESCRIPTION</th>
<th>DATE</th>
<th>APPROVED</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1</td>
<td>Initial Release</td>
<td></td>
<td></td>
</tr>
<tr>
<td>X2</td>
<td>Incorporated changes prior to First Usage</td>
<td>3-16-73</td>
<td></td>
</tr>
<tr>
<td>X3</td>
<td>Change -6.9V to -6.1V</td>
<td>6-16-73</td>
<td></td>
</tr>
<tr>
<td>X4</td>
<td>Change 6000mw to 7000mw, pages 10, 17, 19, 30. Change weight from 6.0 to 6.5 pounds, page 2.</td>
<td>7-24-73</td>
<td></td>
</tr>
</tbody>
</table>

ASTERISK INDICATES DATA WHICH IS NOMANDATORY - FOR INFORMATION ONLY.

THIS DOCUMENT CLEARED THROUGH QA RECORDS CENTER.

MOTOROLA INC. 8201 EAST MCDOWELL ROAD SCOTTSDALE, ARIZONA 852.
1. **SCOPE**

   This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

2. **REFERENCE INFORMATION**

2.1 **SPECIFICATIONS APPLICABLE**

   - **S-562-P-24**
     - Low Power Random Access Spacecraft Memory
   - **12-P13722D**
     - Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. **TEST DATA**

   Unit S/N 102  
   Start Date of Tests 7-25-73  
   Tested by R.C. Reed

4. **PHYSICAL CHARACTERISTICS**

   **6.1 WEIGHT**

   Weight of LP-RASM = 6.145 Pounds  
   Limit 6.5 pounds

---

**MOTOROLA INC.**

Government Electronics Division

A 94990 12-P13721D
S/N 102 Date of Test 7-25-78
Tested By

6.2 DIMENSIONS

<table>
<thead>
<tr>
<th>Letter</th>
<th>Value</th>
<th>Units</th>
<th>Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>2.890</td>
<td>inches</td>
<td></td>
</tr>
<tr>
<td>W</td>
<td>8.630</td>
<td>inches</td>
<td></td>
</tr>
<tr>
<td>MW</td>
<td>8.961</td>
<td>inches</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>6.318</td>
<td>inches</td>
<td></td>
</tr>
<tr>
<td>MD</td>
<td>7.174</td>
<td>inches</td>
<td></td>
</tr>
</tbody>
</table>

V = H x W x D = 57.57 inches³ ≤ 160 inches³
7.4 CHASSIS ISOLATION

Impedance \( \geq 10 \) megohms

Limit \( \geq 9 \) megohms

7.5 INPUT SIGNAL LOADING

7.5.2 Current from INITIATE PULSE to Gnd \( 1.086 \) ma \( \leq 2 \) ma
Current from 2.4V to INITIATE PULSE \( 12.4 \) \( \mu \)a \( \leq 20 \) \( \mu \)a

7.5.3 Current from MEM SEL 1 to Gnd \( 1.108 \) ma \( \leq 2 \) ma
Current from 2.4V to MEM SEL 1 \( 1.65 \) \( \mu \)a \( \leq 20 \) \( \mu \)a

7.5.4 Current from MEM SEL 2 to Gnd \( 1.114 \) ma \( \leq 2 \) ma
Current from 2.4V to MEM SEL 2 \( 0.96 \) \( \mu \)a \( \leq 20 \) \( \mu \)a
Current from MEM SEL 3 to Gnd \( 1.114 \) ma \( \leq 2 \) ma
Current from 2.4V to MEM SEL 3 \( 1.00 \) \( \mu \)a \( \leq 20 \) \( \mu \)a

7.5.5 Current from MEM SEL 4 to Gnd \( 1.11 \) ma \( \leq 2 \) ma
Current from 2.4V to MEM SEL 4 \( 0.69 \) \( \mu \)a \( \leq 20 \) \( \mu \)a

7.5.6 Current from READ/WRITE to Gnd \( 0.757 \) ma \( \leq 2 \) ma
Current from 2.4V to READ/WRITE \( 1.43 \) \( \mu \)a \( \leq 20 \) \( \mu \)a

Current from ADDRESS 2\(^0\) to Gnd \( 1.06 \) ma \( \leq 2 \) ma
Current from 2.4V to ADDRESS 2\(^0\) \( 0.66 \) \( \mu \)a \( \leq 20 \) \( \mu \)a

VOID - See Sheet 24

THIS SHEET N/A

REVISED BY: DWH
<table>
<thead>
<tr>
<th>Address</th>
<th>Current from</th>
<th>Current to</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADDRESS 2(^1)</td>
<td>2.4V</td>
<td>Gnd</td>
<td>1.04 ma</td>
</tr>
<tr>
<td>ADDRESS 2(^2)</td>
<td>2.4V</td>
<td>Address</td>
<td>0.65 (\mu)a</td>
</tr>
<tr>
<td>ADDRESS 2(^2)</td>
<td>ADDRESS</td>
<td>Gnd</td>
<td>1.07 ma</td>
</tr>
<tr>
<td>ADDRESS 2(^3)</td>
<td>2.4V</td>
<td>Address</td>
<td>0.68 (\mu)a</td>
</tr>
<tr>
<td>ADDRESS 2(^3)</td>
<td>ADDRESS</td>
<td>Gnd</td>
<td>1.05 ma</td>
</tr>
<tr>
<td>ADDRESS 2(^4)</td>
<td>2.4V</td>
<td>Address</td>
<td>0.64 (\mu)a</td>
</tr>
<tr>
<td>ADDRESS 2(^4)</td>
<td>ADDRESS</td>
<td>Gnd</td>
<td>1.03 ma</td>
</tr>
<tr>
<td>ADDRESS 2(^4)</td>
<td>ADDRESS</td>
<td>Gnd</td>
<td>0.62 (\mu)a</td>
</tr>
</tbody>
</table>

**Void - See Sheet 24**

This sheet N/A R02
<table>
<thead>
<tr>
<th><strong>Limits</strong></th>
<th><strong>Current from ADDRESS 2⁵ to Gnd</strong></th>
<th><strong>Current from 2.4V to ADDRESS 2⁵</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>≤ 2 ma</td>
<td>1.79 ma</td>
<td>0.60 μA</td>
</tr>
<tr>
<td>≤ 20 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>≤ 2 ma</td>
<td>1.06 ma</td>
<td>0.66 μA</td>
</tr>
<tr>
<td>≤ 20 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>≤ 2 ma</td>
<td>0.785 ma</td>
<td>0.56 μA</td>
</tr>
<tr>
<td>≤ 20 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>≤ 2 ma</td>
<td>1.034 ma</td>
<td>0.51 μA</td>
</tr>
<tr>
<td>≤ 20 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>≤ 2 ma</td>
<td>0.999 ma</td>
<td>0.46 μA</td>
</tr>
<tr>
<td>≤ 20 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>≤ 2 ma</td>
<td>0.864 ma</td>
<td>0.31 μA</td>
</tr>
<tr>
<td>≤ 20 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>≤ 2 ma</td>
<td>0.865 ma</td>
<td>0.33 μA</td>
</tr>
<tr>
<td>≤ 20 μA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>≤ 2 ma</td>
<td>0.84 ma</td>
<td>0.52 μA</td>
</tr>
<tr>
<td>≤ 20 μA</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**VO10 - SEE SHEET 26**

**THIS SHEET NIP**

**ROZ 156**
<table>
<thead>
<tr>
<th>S/N</th>
<th>Date of Test</th>
<th>Tested By</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current from DATA IN BIT 1 to Gnd</td>
<td>837 ma</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 1</td>
<td>62 μa</td>
<td>≤ 20 μa</td>
<td></td>
</tr>
<tr>
<td>Current from DATA IN BIT 2 to Gnd</td>
<td>83 ma</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 2</td>
<td>62 μa</td>
<td>≤ 20 μa</td>
<td></td>
</tr>
<tr>
<td>Current from DATA IN BIT 3 to Gnd</td>
<td>886 ma</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 3</td>
<td>52 μa</td>
<td>≤ 20 μa</td>
<td></td>
</tr>
<tr>
<td>Current from DATA IN BIT 4 to Gnd</td>
<td>809 ma</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 4</td>
<td>54 μa</td>
<td>≤ 20 μa</td>
<td></td>
</tr>
<tr>
<td>Current from DATA IN BIT 5 to Gnd</td>
<td>887 ma</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 5</td>
<td>56 μa</td>
<td>≤ 20 μa</td>
<td></td>
</tr>
<tr>
<td>Current from DATA IN BIT 6 to Gnd</td>
<td>958 ma</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 6</td>
<td>38 μa</td>
<td>≤ 20 μa</td>
<td></td>
</tr>
<tr>
<td>Current from DATA IN BIT 7 to Gnd</td>
<td>969 ma</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 7</td>
<td>38 μa</td>
<td>≤ 20 μa</td>
<td></td>
</tr>
<tr>
<td>Current from DATA IN BIT 8 to Gnd</td>
<td>930 ma</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 8</td>
<td>39 μa</td>
<td>≤ 20 μa</td>
<td></td>
</tr>
<tr>
<td>Current from DATA IN BIT 9 to Gnd</td>
<td>974 ma</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 9</td>
<td>86 μa</td>
<td>≤ 20 μa</td>
<td></td>
</tr>
</tbody>
</table>

VOID - SEE SHEET 2

THIS SHEET MARKED 57
Current from DATA IN BIT 10 to Gnd: 969 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 10: 98 μA ≤ 20 μA
Current from DATA IN BIT 11 to Gnd: 963 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 11: 20 μA ≤ 20 μA
Current from DATA IN BIT 12 to Gnd: 834 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 12: 39 μA ≤ 20 μA
Current from DATA IN BIT 13 to Gnd: 827 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 13: 75 μA ≤ 20 μA
Current from DATA IN BIT 14 to Gnd: 817 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 14: 70 μA ≤ 20 μA
Current from DATA IN BIT 15 to Gnd: 890 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 15: 55 μA ≤ 20 μA
Current from DATA IN BIT 16 to Gnd: 885 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 16: 55 μA ≤ 20 μA
Current from DATA IN BIT 17 to Gnd: 890 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 17: 52 μA ≤ 20 μA

V010 - SEE SHEET 28
THIS SHEET SIGNED

158
7.6 VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS

7.6.3 READ COMPLETE voltage \(\leq 30 \text{ mv}\) \(\leq 100 \text{ mv}\)

7.6.4 DATA OUT BIT 0 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 1 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 2 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 3 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 4 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 5 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 6 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 7 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 8 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 9 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 10 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 11 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 12 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 13 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 14 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 15 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 16 voltage \(\leq 100 \text{ mv}\)
DATA OUT BIT 17 voltage \(\leq 100 \text{ mv}\)
7.7 POWER CONSUMPTION (25°C)

7.7.1 Memory +5V Voltage 5.00 Volts
Memory -6.1V voltage 6.10 Volts
+5V Current 10.3 ma
+5V Power 5.15 mw

7.7.2 Memory -6.1V Current 3.25 ma
Memory -6.1V Power 19.8 mw

7.7.3 Total Memory Idle Power 713 mw 170 mw max

7.7.5 Memory +5V Voltage 5.05 Volts
Memory -6.1V Voltage 6.10 Volts
+5V Current 38.3 38.3 ma
+5V Power 30.8 mw

7.7.6 Memory -6.1V Current 100.05 ma 159 160
Memory -6.1V Power 97.2 mw 97.2

7.7.7 Total Active Power 100.5 mw 7000 mw max.

7.8 READ COMPLETE TIMING

7.8.5 Delay 340 ns 500 ns max.
Duration 260 ns 250 ns min 450 ns max.

VOID - SEE SHEET 36
THIS SHEET REV A 160
<table>
<thead>
<tr>
<th>DO</th>
<th>Status</th>
</tr>
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<tbody>
<tr>
<td>0</td>
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</tr>
<tr>
<td>1</td>
<td>OK</td>
</tr>
<tr>
<td>2</td>
<td>OK</td>
</tr>
<tr>
<td>3</td>
<td>OK</td>
</tr>
<tr>
<td>4</td>
<td>OK</td>
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<td>5</td>
<td>OK</td>
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<td>OK</td>
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<td>OK</td>
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<tr>
<td>16</td>
<td>OK</td>
</tr>
<tr>
<td>17</td>
<td>OK</td>
</tr>
</tbody>
</table>

**LIMITS**

Refer to test proc.

**READ COMPLETE/DATA OUTPUT TIMING**

**S/N 102**

**Date of Test 7-30-73**

**Tested by**

**MOTOROLA INC.**

**Government Electronics Division**

**SIZE** A

**CODE IDENT NO.** 94990

**DWG NO.** 12-P13721D

**SCALE**

**REVISION**

**SHEET** 11
7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?
No
Yes   Address  Bits   0 errors

7.9.4 Did an error occur?
No
Yes   Address  Bits   0 errors

7.9.10 Did an error occur?
No
Yes   Address  Bits   0 errors

7.9.16 Did an error occur?
No
Yes   Address  Bits   0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?
No
Yes   Address  Bits   0 errors

7.10.7 Did an error occur?
a) No
Yes   Address  Bits   0 errors
b) No [√] 
   Yes    Address _____ Bits _____ 0 errors

c) No [ ] 
   Yes    Address _____ Bits _____ 0 errors

7.11 NON-VOLATILITY TEST

7.11.7 Did an error occur? 
   & No [√] 
   Yes    Address _____ Bits _____ 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal) 0000

7.12.4 Address 0001 0000 (Octal) 0000
   0010 0000 (Octal) 0000
   0011 0000 (Octal) 0000
   0100 0000 (Octal) 0000
   0101 0000 (Octal) 0000
   0110 0000 (Octal) 0000
   0111 0000 (Octal) 0000
   1000 0000 (Octal) 0000
   1001 0000 (Octal) 0000
   1010 0000 (Octal) 0000
S/N 102

Date of Test 7-30-73
Tested By RIT

Address 1011 0000 (Octal)
1100 0000 (Octal)
1101 0000 (Octal)
1110 0000 (Octal)

7.12.6 Did an error occur?
No

Yes Address Bits 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?
No

Yes Address Bits 0 errors

7.13.3 Did an error occur?
No

Yes Address Bits 0 errors
7.13.4  

a) Did an error occur?
   No ✓
   Yes Address ___ Bit ___  0 errors

b) Did an error occur?
   No ✓
   Yes Address ___ Bit ___  0 errors
8. TEMPERATURE TEST

8.2.1 Did any errors occur?  
No □  Yes □

Address □  Bits □

Limits

8.2.3 Did any errors occur?
No □  Yes □

Address □  Bits □

8.2.4 HIGH TEMPERATURE

Thermal Resistance

- 50 minutes 1.874 K ohms
- 60 minutes 1.730 K ohms  % change 7.7
- 70 minutes 1.626 K ohms  % change 6.0
- 80 minutes 1.556 K ohms  % change 4.92
- 90 minutes K ohms  % change

8.2.5 -6.1V Voltage +6.02 Volts  +5V Voltage 5.25 Volts
-6.1V Current 3.95 ma  +5V Current 11.7 ma
-6.1V Power 30.8 mw  +5V Power 61.4 mv

Total Memory Idle Power 92.2 mw  170 mw max.
S/N 102

Date of Test 7-27-73
Tested by

3.2.6 Did an error occur?

No [ ] Yes [✓] Address ____ Bit ____

Limits

0 errors

8.2.7 -6.1V Voltage -6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 300 ma +5V Current 784 ma

-6.1V Power 1920 mw +5V Power 4116 mw

Total Memory Operate Power 6034 mw 7000 mw max.

8.2.8 WC a) Did an error occur?

No [✓] Yes ____ Address ____ Bits ____

0 Errors

WC b) Did an error occur?

No [✓] Yes ____ Address ____ Bits ____

0 Errors

WC c) Did an error occur?

No [✓] Yes ____ Address ____ Bits ____

0 Errors

WC d) Did an error occur?

No [✓] Yes ____ Address ____ Bits ____

0 Errors

167
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<th>8.2.10</th>
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S/N 102  Date of Test 7-27-79
Tested By D

6.3.6 LOW TEMPERATURE
Thermal Resistance
150 minutes 194.0 K ohms
160 minutes 218.0 K ohms % change 12.4
170 minutes 225.6 K ohms % change 3.5
180 minutes ———— K ohms % change
190 minutes ———— K ohms % change

6.3.7 Did an error occur? No
Yes Address _______ Bits _______ 0 Errors

8.3.8 -6.1V Voltage 6.40 Volts +5V Voltage 5.25 Volts
-6.1V Current 9.8 ma +5V Current 11.0 ma
-6.1V Power 62.72 mv +5V Power 57.75 mv

Total Memory Idle Power 180.47 mv 170 mv max.

8.3.9 -6.1V Voltage 6.40 Volts +5V Voltage 5.25 Volts
-6.1V Current 262 ma +5V Current 683 ma
-6.1V Power 1677 mw +5V Power 9585 mv

Total Memory Operate Power 5262 mw 7000 mw max.
S/N 102

Date of Test 7-27-73
Tested By K.G.

8.3.10 Did an error occur? 
No

Yes Address Bits 0 Errors

8.3.11 WC a) Did an error occur? 
No

Yes Address Bits 0 Errors

WC b) Did an error occur? 
No

Yes Address Bits 0 Errors

WC c) Did an error occur? 
No

Yes Address Bits 0 Errors

WC d) Did an error occur? 
No

Yes Address Bits 0 Errors

8.3.13 Did any errors occur? 
No

Yes Address Bits 0 Errors
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REMARKS: Start Pumping
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<td>4.5x10^-2</td>
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**Remarks:**

* Victor L. Hollen *
9. VACUUM TEST
9.2 Did Any Bit Errors Occur?
   No □
   Yes Address _______ Bits _______ 0 Errors

9.2.1 Fast Decompression
   Date 7-25-73
   Tested by R0Z
   Did Any Bit Errors Occur?
   Yes □
   No Address _______ Bits _______ 0 Errors

9.2.2 Hard Vacuum
   Date 7-26-73
   Tested by R0Z
   Did Any Bit Errors Occur?
   No □
   Yes Address _______ Bits _______ 0 Errors

10. VIBRATION TEST
    Date 7-26-73
    Tested by R0Z
    SINE SWEEP
    Axis X - Did Any Bit Errors Occur?
    No
    Yes Freq _______ Address _______ Bits _______ 0 Errors

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**Vibration Test**

Sheet 1 of 1  Date: July 26, 1973

Project: 4339 Unit: PW Memory

Serial No.: 102

Operator: Pete Martin

Observer: Bob Lott

Cycle Time: Freq. to cps.

Reason for test: 

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<th>Total</th>
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<th>G'</th>
<th>Remarks</th>
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<tr>
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<td>15:38</td>
<td>15:42</td>
<td>4.3min</td>
<td>0.3</td>
<td>10g+5g</td>
<td>sine sweep 500-2000 Hz</td>
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<tr>
<td>A</td>
<td>15:45</td>
<td>15:47</td>
<td>2min</td>
<td>564g/μs</td>
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<td>shaped random</td>
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Drive Monitor Sig. Gen: Accel 9
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<th>Freq</th>
<th>Address</th>
<th>Bits</th>
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**RANDOM VIBRATION**

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**SHOCK TEST**

Date tested by RPD

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<th>Y Direction - Did Any Bit Errors Occur?</th>
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<tr>
<td></td>
<td>Bits</td>
</tr>
<tr>
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<td>0 Errors</td>
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</table>

**MOTOROLA INC.**

Government Electronics Division

E. I. MCDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

SIZE  CODE IDENT NO. DWG NO.
A   94990  12-P13721D
Z Direction - Did Any Bit Errors Occur?

No

Yes _____ Address ________ Bits _______ 0 Errors

X Direction - Did Any Bit Errors Occur?

No

Yes _____ Address ________ Bits _______ 0 Errors

12 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No

Yes _____ Address ________ Bits _______ 0 Errors

Z Direction - Did Any Bit Errors Occur?

No

Yes _____ Address ________ Bits _______ 0 Errors

X Direction - Did Any Bit Errors Occur?

No

Yes _____ Address ________ Bits _______ 0 Errors
7.4 CHASSIS ISOLATION
Impedance > 10

7.5 INPUT SIGNAL LOADING

7.5.2 Current from INITIATE PULSE to Gnd 1.086 ma ≤ 2 ma
Current from 2.4V to INITIATE PULSE 1.25 μa ≤ 20 μa

7.5.3 Current from MEM SEL 1 to Gnd 1.108 ma ≤ 2 ma
Current from 2.4V to MEM SEL 1 0.65 μa ≤ 20 μa

7.5.4 Current from MEM SEL 2 to Gnd 1.111 ma ≤ 2 ma
Current from 2.4V to MEM SEL 2 0.76 μa ≤ 20 μa
Current from MEM SEL 3 to Gnd 1.111 ma ≤ 2 ma
Current from 2.4V to MEM SEL 3 1.00 μa ≤ 20 μa
Current from MEM SEL 4 to Gnd 1.111 ma ≤ 2 ma
Current from 2.4V to MEM SEL 4 0.69 μa ≤ 20 μa

7.5.5 Current from READ/WRITE to Gnd 0.757 ma ≤ 2 ma
Current from 2.4V to READ/WRITE 0.43 μa ≤ 20 μa

7.5.6 Current from ADDRESS 2^0 to Gnd 1.06 ma ≤ 2 ma
Current from 2.4V to ADDRESS 2^0 0.66 μa ≤ 20 μa
S/N 102

Date of Test 7-30-73

Tested By EEC

Limits

Current from ADDRESS 2^1 to Gnd 1.07 mA ≤ 2 mA
Current from 2.4V to ADDRESS 2^1 0.65 μA ≤ 20 μA
Current from ADDRESS 2^2 to Gnd 1.07 mA ≤ 2 mA
Current from 2.4V to ADDRESS 2^2 0.68 μA ≤ 20 μA
Current from ADDRESS 2^3 to Gnd 1.05 mA ≤ 2 mA
Current from 2.4V to ADDRESS 2^3 0.67 μA ≤ 20 μA
Current from ADDRESS 2^4 to Gnd 1.03 mA ≤ 2 mA
Current from 2.4V to ADDRESS 2^4 0.62 μA ≤ 20 μA
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<th>Values</th>
<th>Limits</th>
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<td>79 ma</td>
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<tr>
<td>Current from 2.4V to ADDR 2^5</td>
<td>60 μa</td>
<td>≤ 20 μa</td>
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<td>Current from ADDR 2^6 to Gnd</td>
<td>106 ma</td>
<td>≤ 2 ma</td>
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<tr>
<td>Current from 2.4V to ADDR 2^6</td>
<td>66 μa</td>
<td>≤ 20 μa</td>
</tr>
<tr>
<td>Current from ADDR 2^7 to Gnd</td>
<td>785 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to ADDR 2^7</td>
<td>56 μa</td>
<td>≤ 20 μa</td>
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<td>1034 ma</td>
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<tr>
<td>Current from 2.4V to ADDR 2^8</td>
<td>51 μa</td>
<td>≤ 20 μa</td>
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<tr>
<td>Current from ADDR 2^9 to Gnd</td>
<td>999 ma</td>
<td>≤ 2 ma</td>
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<td>Current from 2.4V to ADDR 2^9</td>
<td>46 μa</td>
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<td>Current from ADDR 2^10 to Gnd</td>
<td>864 ma</td>
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<td>Current from 2.4V to ADDR 2^10</td>
<td>31 μa</td>
<td>≤ 20 μa</td>
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<tr>
<td>Current from ADDR 2^11 to Gnd</td>
<td>865 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to ADDR 2^11</td>
<td>33 μa</td>
<td>≤ 20 μa</td>
</tr>
<tr>
<td>Current from DATA IN BIT 0 to Gnd</td>
<td>840 ma</td>
<td>≤ 2 ma</td>
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<tr>
<td>Current from 2.4V to DATA IN BIT 0</td>
<td>54 μa</td>
<td>≤ 20 μa</td>
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Current from DATA IN BIT 1 to Gnd  837 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 1  62 μa  ≤ 20 μa
Current from DATA IN BIT 2 to Gnd  830 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 2  62 μa  ≤ 20 μa
Current from DATA IN BIT 3 to Gnd  886 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 3  52 μa  ≤ 20 μa
Current from DATA IN BIT 4 to Gnd  809 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 4  54 μa  ≤ 20 μa
Current from DATA IN BIT 5 to Gnd  887 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 5  56 μa  ≤ 20 μa
Current from DATA IN BIT 6 to Gnd  958 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 6  38 μa  ≤ 20 μa
Current from DATA IN BIT 7 to Gnd  969 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 7  38 μa  ≤ 20 μa
Current from DATA IN BIT 8 to Gnd  930 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 8  39 μa  ≤ 20 μa
Current from DATA IN BIT 9 to Gnd  974 ma  ≤ 2 ma
Current from 2.4V to DATA IN BIT 9  86 μa  ≤ 20 μa
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<th>969 μA</th>
<th>≤ 2 ma</th>
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<td>78 μA</td>
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<td>Current from DATA IN BIT 11 to Gnd</td>
<td>963 μA</td>
<td>≤ 2 ma</td>
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<tr>
<td>Current from 2.4V to DATA IN BIT 11</td>
<td>79 μA</td>
<td>≤ 20 μA</td>
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<td>Current from DATA IN BIT 12 to Gnd</td>
<td>834 μA</td>
<td>≤ 2 ma</td>
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<td>Current from 2.4V to DATA IN BIT 12</td>
<td>59 μA</td>
<td>≤ 20 μA</td>
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<td>Current from DATA IN BIT 13 to Gnd</td>
<td>827 μA</td>
<td>≤ 2 ma</td>
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<td>Current from 2.4V to DATA IN BIT 13</td>
<td>75 μA</td>
<td>≤ 20 μA</td>
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<td>812 μA</td>
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<td>Current from 2.4V to DATA IN BIT 14</td>
<td>70 μA</td>
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<td>Current from DATA IN BIT 15 to Gnd</td>
<td>890 μA</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 15</td>
<td>55 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Current from DATA IN BIT 16 to Gnd</td>
<td>885 μA</td>
<td>≤ 2 ma</td>
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<tr>
<td>Current from 2.4V to DATA IN BIT 16</td>
<td>55 μA</td>
<td>≤ 20 μA</td>
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<tr>
<td>Current from DATA IN BIT 17 to Gnd</td>
<td>890 μA</td>
<td>≤ 2 ma</td>
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<tr>
<td>Current from 2.4V to DATA IN BIT 17</td>
<td>52 μA</td>
<td>≤ 20 μA</td>
</tr>
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</table>
### 7.6 Verification of Open Collector on Output Signals

#### 7.6.3 Read Complete Voltage
- **Data OUT BIT 0 Voltage**: 105.480 mv, ≤ 100 mv
- **Data OUT BIT 1 Voltage**: 105.480 mv, ≤ 100 mv
- **Data OUT BIT 2 Voltage**: 105.400 mv, ≤ 100 mv
- **Data OUT BIT 3 Voltage**: 105.400 mv, ≤ 100 mv
- **Data OUT BIT 4 Voltage**: 105.400 mv, ≤ 100 mv
- **Data OUT BIT 5 Voltage**: 105.400 mv, ≤ 100 mv
- **Data OUT BIT 6 Voltage**: 105.400 mv, ≤ 100 mv
- **Data OUT BIT 7 Voltage**: 105.400 mv, ≤ 100 mv
- **Data OUT BIT 8 Voltage**: 10.0 mv, ≤ 100 mv
- **Data OUT BIT 9 Voltage**: 95.0 mv, ≤ 100 mv
- **Data OUT BIT 10 Voltage**: 90.0 mv, ≤ 100 mv
- **Data OUT BIT 11 Voltage**: 90.0 mv, ≤ 100 mv
- **Data OUT BIT 12 Voltage**: 80.0 mv, ≤ 100 mv
- **Data OUT BIT 13 Voltage**: 75.0 mv, ≤ 100 mv
- **Data OUT BIT 14 Voltage**: 70.0 mv, ≤ 100 mv
- **Data OUT BIT 15 Voltage**: 80.0 mv, ≤ 100 mv
- **Data OUT BIT 16 Voltage**: 90.0 mv, ≤ 100 mv
- **Data OUT BIT 17 Voltage**: 95.0 mv, ≤ 100 mv
7.7 POWER CONSUMPTION (25°C)

7.7.1 Memory +5V Voltage 5.00 Volts
Memory -6.1V Voltage 6.10 Volts
+5V Current 10.3 ma
+5V Power 51.5 mw

7.7.2 Memory -6.1V Current 3.25 ma
Memory -6.1V Power 19.8 mw

7.7.3 Total Memory Idle Power 71.3 mw 170 mw max

7.7.5 Memory +5V Voltage 5.00 Volts
Memory -6.1V Voltage 6.10 Volts
+5V Current 6.38 ma
+5V Power 3.5 mw

7.7.6 Memory -6.1V Current 159 ma
Memory -6.1V Power 97 mw

7.7.7 Total Active Power 100.5 mw 7000 mw max.

7.8 READ COMPLETE TIMING

7.8.5 Delay 340 ns 500 ns max.
Duration 260 ns 250 ns min 450 ns max.
**READ COMPLETE/DATA OUTPUT TIMING**

<table>
<thead>
<tr>
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<th>Status</th>
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</thead>
<tbody>
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</tr>
<tr>
<td>17</td>
<td>OK REJECT</td>
</tr>
</tbody>
</table>

REFER TO TEST PROC.
7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?
No
Yes Address Bits 0 errors

7.9.4 Did an error occur?
No
Yes Address Bits 0 errors

7.9.10 Did an error occur?
No
Yes Address Bits 0 errors

7.9.16 Did an error occur?
No
Yes Address Bits 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?
No
Yes Address Bits 0 errors

7.10.7 Did an error occur?
a) No
Yes Address Bits 0 errors

S/N 102
Date of Test 7-30-73
Tested By [Signature]

MOTOROLA INC.
Government Electronics Division

SIZE A CODE IDENT NO. 94990
DRAW NO. 12-P13721D

888 E. MINNEAPOLIS ROAD
SCOTTSDALE, ARIZONA 85251
7.11 NON-VOLATILITY TEST

7.11.7 Did an error occur?

&

7.11.9 No

Yes __ Address _____ Bits ____ 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal) 0000

7.12.4 Address 0001 0000 (Octal) 0000

0010 0000 (Octal) 0000

0011 0000 (Octal) 0000

0100 0000 (Octal) 0000

0101 0000 (Octal) 0000

0110 0000 (Octal) 0000

0111 0000 (Octal) 0000

1000 0000 (Octal) 0000

1001 0000 (Octal) 0000

1010 0000 (Octal) 0000

S/N 101

Date of Test 7-30-73
Tested By NEC

b) No

Yes Address Bits 0 errors

No

Yes Address Bits 0 errors

186
<table>
<thead>
<tr>
<th>Address</th>
<th>Bits (Octal)</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
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<td>0000</td>
<td>0000</td>
<td></td>
</tr>
</tbody>
</table>

7.12.6 Did an error occur?
No [ ]
Yes [X] Address [ ] Bits [ ] 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?
No [ ]
Yes [X] Address [ ] Bits [ ] 0 errors

7.13.3 Did an error occur?
No [ ]
Yes [X] Address [ ] Bits [ ] 0 errors

187
S/N 102

Date of Test 2-30-73
Tested By __________

7.13.4

a) Did an error occur?
   No __________
   Yes ______ Address ______ Bit _______ 0 errors

b) Did an error occur?
   No __________
   Yes ______ Address ______ Bit _______ 0 errors
<table>
<thead>
<tr>
<th>REV</th>
<th>X1</th>
<th>X2</th>
<th>X3</th>
<th>X4</th>
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<tr>
<td>X1</td>
<td>Initial Release</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>X2</td>
<td>Incorporated changes prior to First Usage</td>
<td>3-16-73</td>
<td></td>
<td></td>
</tr>
<tr>
<td>X3</td>
<td>Change -6.9V to -6.1V</td>
<td>6-18-73</td>
<td></td>
<td></td>
</tr>
<tr>
<td>X4</td>
<td>Change 6000mW to 7000mW, pages 10, 17, 19, 30. Change weight from 6.0 to 6.5 pounds, page 2.</td>
<td>7-24-73</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**APPROVAL**

- **DATE**: 3-16-73
- **APPROVER**: [Signature]

**LATISSIMPLY USED ON**

- **DESCRIPTION**: Initial Release
- **DATE**: 3-16-73
- **APPROVER**: [Signature]
- **DESCRIPTION**: Incorporated changes prior to First Usage
- **DATE**: 3-16-73
- **APPROVER**: [Signature]
- **DESCRIPTION**: Change -6.9V to -6.1V
- **DATE**: 6-18-73
- **APPROVER**: [Signature]
- **DESCRIPTION**: Change 6000mW to 7000mW, pages 10, 17, 19, 30. Change weight from 6.0 to 6.5 pounds, page 2.
- **DATE**: 7-24-73
- **APPROVER**: [Signature]
1. SCOPE
This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

2. REFERENCE INFORMATION
2.1 SPECIFICATIONS APPLICABLE
   S-562-P-24  Low Power Random Access Spacecraft Memory
   12-P13722D  Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. TEST DATA
   Unit S/N 102  Start Date of Tests 1-7-74
   Tested by [Signature]

   ATP PARA. NO.

3.1 EQUIVALENT TEST EQUIPMENT
   DIGITEC 260 MULTIMETER
   EH 138 PULSE GEN.
   TSI 361-2 COUNTER

4. PHYSICAL CHARACTERISTICS
   Limit

6.1 WEIGHT
   Weight of LP-RASM = 6.5 pounds
S/N ______________________  Date of Test __________
Tested By _______________

6.2 DIMENSIONS

H = ___________ inches
W = ___________ inches
MW= ___________ inches
D = ___________ inches
MD= ___________ inches

V = H x W x D = __________ inches³  ≤ 160 inches³
### 7.4 CHASSIS ISOLATION

Impedance \( > 10 \text{ M\Omega} \)

### 7.5 INPUT SIGNAL LOADING

<table>
<thead>
<tr>
<th>Current Source</th>
<th>Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current from INITIATE PULSE to Gnd</td>
<td>( \leq 2 \text{ mA} )</td>
</tr>
<tr>
<td>Current from 2.4V to INITIATE PULSE</td>
<td>( \leq 20 \text{ \mu A} )</td>
</tr>
<tr>
<td>Current from MEM SEL 1 to Gnd</td>
<td>( \leq 2 \text{ mA} )</td>
</tr>
<tr>
<td>Current from 2.4V to MEM SEL 1</td>
<td>( \leq 20 \text{ \mu A} )</td>
</tr>
<tr>
<td>Current from MEM SEL 2 to Gnd</td>
<td>( \leq 2 \text{ mA} )</td>
</tr>
<tr>
<td>Current from 2.4V to MEM SEL 2</td>
<td>( \leq 20 \text{ \mu A} )</td>
</tr>
<tr>
<td>Current from MEM SEL 3 to Gnd</td>
<td>( \leq 2 \text{ mA} )</td>
</tr>
<tr>
<td>Current from 2.4V to MEM SEL 3</td>
<td>( \leq 20 \text{ \mu A} )</td>
</tr>
<tr>
<td>Current from MEM SEL 4 to Gnd</td>
<td>( \leq 2 \text{ mA} )</td>
</tr>
<tr>
<td>Current from 2.4V to MEM SEL 4</td>
<td>( \leq 20 \text{ \mu A} )</td>
</tr>
<tr>
<td>Current from READ/WRITE to Gnd</td>
<td>( \leq 2 \text{ mA} )</td>
</tr>
<tr>
<td>Current from 2.4V to READ/WRITE</td>
<td>( \leq 20 \text{ \mu A} )</td>
</tr>
<tr>
<td>Current from ADDRESS 2(^0) to Gnd</td>
<td>( \leq 2 \text{ mA} )</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2(^0)</td>
<td>( \leq 20 \text{ \mu A} )</td>
</tr>
</tbody>
</table>
S/N ___________________________ Date of Test ________________
Tested By _______________________

Limits

Current from ADDRESS 2¹ to Gnd _____ ma ≤ 2 ma
Current from 2.4V to ADDRESS 2¹ _____ µa ≤ 20 µa

Current from ADDRESS 2² to Gnd _____ ma ≤ 2 ma
Current from 2.4V to ADDRESS 2² _____ µa ≤ 20 µa

Current from ADDRESS 2³ to Gnd _____ ma ≤ 2 ma
Current from 2.4V to ADDRESS 2³ _____ µa ≤ 20 µa

Current from ADDRESS 2⁴ to Gnd _____ ma ≤ 2 ma
Current from 2.4V to ADDRESS 2⁴ _____ µa ≤ 20 µa
<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
<th>Limit</th>
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</thead>
<tbody>
<tr>
<td>Current from ADDRESS 2^5 to Gnd</td>
<td>____ma</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2^5</td>
<td>____(\mu \text{a} )</td>
<td>( \leq 20\mu \text{a} )</td>
</tr>
<tr>
<td>Current from ADDRESS 2^6 to Gnd</td>
<td>____ma</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2^6</td>
<td>____(\mu \text{a} )</td>
<td>( \leq 20\mu \text{a} )</td>
</tr>
<tr>
<td>Current from ADDRESS 2^7 to Gnd</td>
<td>____ma</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2^7</td>
<td>____(\mu \text{a} )</td>
<td>( \leq 20\mu \text{a} )</td>
</tr>
<tr>
<td>Current from ADDRESS 2^8 to Gnd</td>
<td>____ma</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2^8</td>
<td>____(\mu \text{a} )</td>
<td>( \leq 20\mu \text{a} )</td>
</tr>
<tr>
<td>Current from ADDRESS 2^9 to Gnd</td>
<td>____ma</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2^9</td>
<td>____(\mu \text{a} )</td>
<td>( \leq 20\mu \text{a} )</td>
</tr>
<tr>
<td>Current from ADDRESS 2^10 to Gnd</td>
<td>____ma</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2^10</td>
<td>____(\mu \text{a} )</td>
<td>( \leq 20\mu \text{a} )</td>
</tr>
<tr>
<td>Current from ADDRESS 2^11 to Gnd</td>
<td>____ma</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2^11</td>
<td>____(\mu \text{a} )</td>
<td>( \leq 20\mu \text{a} )</td>
</tr>
<tr>
<td>Current from DATA IN BIT 0 to Gnd</td>
<td>____ma</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 0</td>
<td>____(\mu \text{a} )</td>
<td>( \leq 20\mu \text{a} )</td>
</tr>
</tbody>
</table>
S/N __________________________

Date of Test __________________
Tested By ____________________

Limits

Current from DATA IN BIT 1 to Gnd _____ ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 1 _____ μa ≤ 20 μa

Current from DATA IN BIT 2 to Gnd _____ ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 2 _____ μa ≤ 20 μa

Current from DATA IN BIT 3 to Gnd _____ ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 3 _____ μa ≤ 20 μa

Current from DATA IN BIT 4 to Gnd _____ ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 4 _____ μa ≤ 20 μa

Current from DATA IN BIT 5 to Gnd _____ ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 5 _____ μa ≤ 20 μa

Current from DATA IN BIT 6 to Gnd _____ ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 6 _____ μa ≤ 20 μa

Current from DATA IN BIT 7 to Gnd _____ ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 7 _____ μa ≤ 20 μa

Current from DATA IN BIT 8 to Gnd _____ ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 8 _____ μa ≤ 20 μa

Current from DATA IN BIT 9 to Gnd _____ ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 9 _____ μa ≤ 20 μa

MOTOROLA INC.
Government Electronics Division

8201 E. McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

SIZE  CODE IDENT NO.  DRAW NO.
A  94900  12-PI3721D

SCALE  REVISION  SHEET 7
<table>
<thead>
<tr>
<th>Current from DATA IN BIT</th>
<th>Current from 2.4V to DATA IN BIT</th>
<th>Limits</th>
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<tbody>
<tr>
<td>10 to Gnd</td>
<td>10</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>11 to Gnd</td>
<td>11</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>12 to Gnd</td>
<td>12</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>13 to Gnd</td>
<td>13</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>14 to Gnd</td>
<td>14</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>15 to Gnd</td>
<td>15</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>16 to Gnd</td>
<td>16</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
<tr>
<td>17 to Gnd</td>
<td>17</td>
<td>( \leq 2 \text{ ma} )</td>
</tr>
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</table>
7.6 VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS

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<tr>
<th>Section</th>
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<th>Limit</th>
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<td>7.6.3</td>
<td>READ COMPLETE voltage</td>
<td>( \leq 100 \text{ mv} )</td>
</tr>
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<td>7.6.4</td>
<td>DATA OUT BIT 0 voltage</td>
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<td>DATA OUT BIT 1 voltage</td>
<td>( \leq 100 \text{ mv} )</td>
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<td></td>
<td>DATA OUT BIT 2 voltage</td>
<td>( \leq 100 \text{ mv} )</td>
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<td></td>
<td>DATA OUT BIT 3 voltage</td>
<td>( \leq 100 \text{ mv} )</td>
</tr>
<tr>
<td></td>
<td>DATA OUT BIT 4 voltage</td>
<td>( \leq 100 \text{ mv} )</td>
</tr>
<tr>
<td></td>
<td>DATA OUT BIT 5 voltage</td>
<td>( \leq 100 \text{ mv} )</td>
</tr>
<tr>
<td></td>
<td>DATA OUT BIT 6 voltage</td>
<td>( \leq 100 \text{ mv} )</td>
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<td></td>
<td>DATA OUT BIT 7 voltage</td>
<td>( \leq 100 \text{ mv} )</td>
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<td>DATA OUT BIT 8 voltage</td>
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<td>DATA OUT BIT 9 voltage</td>
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<td>DATA OUT BIT 10 voltage</td>
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<td>DATA OUT BIT 11 voltage</td>
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<td>DATA OUT BIT 12 voltage</td>
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<td>DATA OUT BIT 14 voltage</td>
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<td>DATA OUT BIT 16 voltage</td>
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<tr>
<td></td>
<td>DATA OUT BIT 17 voltage</td>
<td>( \leq 100 \text{ mv} )</td>
</tr>
</tbody>
</table>
7.7 POWER CONSUMPTION (25°C)

7.7.1 Memory +5V Voltage 5.00 Volts
Memory -6.1V voltage -6.10 Volts
+5V Current 10.4 ma
+5V Power 52 mw

7.7.2 Memory -6.1V Current 3.3 ma
Memory -6.1V Power 20.1 mw

7.7.3 Total Memory Idle Power 72.1 mw

7.7.5 Memory +5V Voltage 5.00 Volts
Memory -6.1V Voltage -6.10 Volts
+5V Current 709 ma
+5V Power 354.5 mw

7.7.6 Memory -6.1V Current 268 ma
Memory -6.1V Power 163.5 mw

7.7.7 Total Active Power 5180 mw

7.8 READ COMPLETE TIMING

7.8.5 Delay __________ ns
Duration __________ ns

Date of Test 1-7-74
Tested By MHC

Limits

7000 mw max.
500 ns max.
250 ns min
450 ns max.

S/N 102
<table>
<thead>
<tr>
<th>DO</th>
<th>Status</th>
<th>Reason</th>
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</thead>
<tbody>
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<td>REJECT</td>
</tr>
<tr>
<td>DO-1</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-2</td>
<td>OK</td>
<td>REJECT</td>
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<td>DO-3</td>
<td>OK</td>
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<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-17</td>
<td>OK</td>
<td>REJECT</td>
</tr>
</tbody>
</table>

**LIMITS**

**REFER TO TEST PROC.**
7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?
No [X]
Yes [ ] Address [ ] Bits [ ]

0 errors

7.9.4 Did an error occur?
No [X]
Yes [ ] Address [ ] Bits [ ]

0 errors

7.9.10 Did an error occur?
No [X]
Yes [ ] Address [ ] Bits [ ]

0 errors

7.9.16 Did an error occur?
No [X]
Yes [ ] Address [ ] Bits [ ]

0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?
No [X]
Yes [ ] Address [ ] Bits [ ]

0 errors

7.10.7 Did an error occur?
a) No [X]
Yes [ ] Address [ ] Bits [ ]

0 errors
S/N 102

Date of Test 1-7-74
Tested By WEC

Limits

b) No X
   Yes Address _____ Bits _____ 0 errors

c) No X
   Yes Address _____ Bits _____ 0 errors

7.11 NON-VOLATILITY TEST

7.11.7 Did an error occur?
   & No X
   Yes Address _____ Bits _____ 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal) 0000

7.12.4 Address 0001 0000 (Octal) 0000
   0010 0000 (Octal) 0000
   0011 0000 (Octal) 0000
   0100 0000 (Octal) 0000
   0101 0000 (Octal) 0000
   0110 0000 (Octal) 0000
   0111 0000 (Octal) 0000
   1000 0000 (Octal) 0000
   1001 0000 (Octal) 0000
   1010 0000 (Octal) 0000

7.201
S/N 107

Date of Test 1-7-74
Tested By [Blank]

Address 1011 0000 (Octal)
1100 0000 (Octal)
1101 0000 (Octal)
1110 0000 (Octal)

7.12.6 Did an error occur?
No [X]
Yes [ ] Address [Blank] Bits [Blank] 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?
No [X]
Yes [ ] Address [Blank] Bits [Blank] 0 errors

7.13.3 Did an error occur?
No [X]
Yes [ ] Address [Blank] Bits [Blank] 0 errors

[Signature] 202
7.13.4  a) Did an error occur?
    No       x
    Yes ______ Address ______  Bit ______
    0 errors

b) Did an error occur?
    No       x
    Yes ______ Address ______  Bit ______
    0 errors
8. TEMPERATURE TEST

8.2.1 Did any errors occur?
Yes ________ Address ________ Bits ________
No XXXX ________

8.2.3 Did any errors occur?
No XXXX ________
Yes ________ Address ________ Bits ________
No XXXX ________

8.2.4 HIGH TEMPERATURE

Thermal Resistance

50 minutes 1.707 K ohms
60 minutes 1.595 K ohms % change 6.6
70 minutes 1.575 K ohms % change 5.0
80 minutes 1.454 K ohms % change 4.0
90 minutes ___ K ohms % change ___

8.2.5 -6.1V Voltage 6.40 Volts +5V Voltage 5.25 Volts
-6.1V Current 5.0 ma +5V Current 11.7 ma
-6.1V Power 32 mw +5V Power 61.4 mv

Total Memory Idle Power 93.4 mw 170 mw max.

MOTOROLA INC.

S/N 102 Date of Test 1-7-74
Tested by

8.2.1 Did any errors occur?
Yes Address Bits
No XXXX

8.2.3 Did any errors occur?
Yes Address Bits
No XXXX

8.2.4 HIGH TEMPERATURE

Thermal Resistance

50 minutes 1.707 K ohms
60 minutes 1.595 K ohms % change 6.6
70 minutes 1.575 K ohms % change 5.0
80 minutes 1.454 K ohms % change 4.0
90 minutes ___ K ohms % change ___

8.2.5 -6.1V Voltage 6.40 Volts +5V Voltage 5.25 Volts
-6.1V Current 5.0 ma +5V Current 11.7 ma
-6.1V Power 32 mw +5V Power 61.4 mv

Total Memory Idle Power 93.4 mw 170 mw max.

MOTOROLA INC.
8.2.6 Did an error occur?

No  

Yes Address Bit 0 Errors

Limits

8.2.7 -6.1V Voltage 6.40 Volts +5V Voltage 5.25 Volts

-6.1V Current 340 ma +5V Current 840 ma

-6.1V Power 2176 mw +5V Power 4410 mw

Total Memory Operate Power 6586 mw 7000 mw max.

8.2.8 WC a) Did an error occur?

No  

Yes Address Bits 0 Errors

WC b) Did an error occur?

No  

Yes Address Bits 0 Errors

WC c) Did an error occur?

No  

Yes Address Bits 0 Errors

WC d) Did an error occur?

No  

Yes Address Bits 0 Errors
S/N 102

8.2.10 Did any errors occur?
No
Yes Address
Bits

8.2.11 Did an error occur?
No
Yes Address
Bits

8.3 Low Temperature

8.3.3 Did any errors occur?
No
Yes Address
Bits

8.3.5 Did any errors occur?
No
Yes Address
Bits

Limits
0 Errors

Address

0 Errors

Address

0 Errors

Address

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8.3.6 **LOW TEMPERATURE**

Thermal Resistance

<table>
<thead>
<tr>
<th>Time</th>
<th>K ohms</th>
<th>% change</th>
</tr>
</thead>
<tbody>
<tr>
<td>150 min</td>
<td>145.2</td>
<td></td>
</tr>
<tr>
<td>160 min</td>
<td>147.3</td>
<td>1.4</td>
</tr>
<tr>
<td>170 min</td>
<td></td>
<td></td>
</tr>
<tr>
<td>180 min</td>
<td></td>
<td></td>
</tr>
<tr>
<td>190 min</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

8.3.7 **Did an error occur?**

- **Yes**
- **No**

**Limits**

<table>
<thead>
<tr>
<th>Address Bits</th>
<th>Errors</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

8.3.8

- **-6.1V Voltage**: 6.4 Volts
- **+5V Voltage**: 5.25 Volts
- **-6.1V Current**: 9.3 ma
- **+5V Current**: 11.2 ma
- **-6.1V Power**: 59.5 mv
- **+5V Power**: 58.8 mv

**Total Memory Idle Power**: 118.3 mv

8.3.9

- **-6.1V Voltage**: 6.9 Volts
- **+5V Voltage**: 5.25 Volts
- **-6.1V Current**: 300 ma
- **+5V Current**: 748 ma
- **-6.1V Power**: 1920 mw
- **+5V Power**: 3.927 mw

**Total Memory Operate Power**: 5847 mw

---

**MOTOROLA INC.**

**Government Electronics Division**

**SIZE** A  **CODE IDENT NO.** 94990  **DRAW NO.** 12-PL3721D

**SCALE**  **REVISION**  **SHET** 19
S/N 102

Date of Test 1-8-74
Tested By, [Signature]

8.3.10 Did an error occur?
No X
Yes ___ Address _____ Bits _____

Limits

8.3.11 WC a) Did an error occur?
No X
Yes ___ Address _____ Bits _____ 0 Errors

8.3.11 WC b) Did an error occur?
No X
Yes ___ Address _____ Bits _____ 0 Errors

8.3.11 WC c) Did an error occur?
No X
Yes ___ Address _____ Bits _____ 0 Errors

8.3.11 WC d) Did an error occur?
No X
Yes ___ Address _____ Bits _____ 0 Errors

8.3.13 Did any errors occur?
No X
Yes ___ Address _____ Bits _____ 0 Errors

MOTOROLA INC.
Governments and Defense Division

620 E. McDOWELL ROAD
SCOTTSDALE, ARIZONA 85251

AV-2-8-199J-109A-3 69 DWG FORMAT

AV-2-8-199J-109A-3 69 DWG FORMAT
9. VACUUM TEST
9.2 Did Any Bit Errors Occur?
No______
Yes______ Address _____ Bits ______ 0 Errors

9.2.1 Fast Decompression
Date______ Tested by ________

Did Any Bit Errors Occur?
No______
Yes______ Address _____ Bits ______ 0 Errors

9.2.2 Hard Vacuum
Date______ Tested by ________

Did Any Bit Errors Occur?
No______
Yes______ Address _____ Bits ______ 0 Errors

10. VIBRATION TEST
Date______ Tested by ________

SINE SWEEP
Axis X - Did Any Bit Errors Occur?

No______
Yes______ Freq_____ Address_____ Bits _____ 0 Errors
Axis Y - Did Any Bit Error Occur? Limits
No ______
Yes ____ Freq _____ Address _____ Bits ______ 0 Errors

Axis Z - Did Any Bit Errors Occur? No ______
Yes ____ Freq _____ Address _____ Bits ______ 0 Errors

RANDOM VIBRATION
Axis X - Did Any Bit Errors Occur? No ______
Yes ____ Freq _____ Address _____ Bits ______ 0 Errors

Axis Y - Did Any Bit Errors Occur? No ______
Yes ____ Freq _____ Address _____ Bits ______ 0 Errors

Axis Z - Did Any Bit Errors Occur? No ______
Yes ____ Freq _____ Address _____ Bits ______ 0 Errors

11. SHOCK TEST
Date ______ Tested By _______________________

6 MILLISECOND DURATION SHOCK
Y Direction - Did Any Bit Errors Occur? No ______
Yes ____ Address ________ Bits ________ 0 Errors
Z Direction - Did Any Bit Errors Occur?
No _____
Yes ____ Address _______ Bits _______ 0 Errors

X Direction - Did Any Bit Errors Occur?
No _____
Yes ____ Address _______ Bits _______ 0 Errors

12 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?
No _____
Yes ____ Address _______ Bits _______ 0 Errors

Z Direction - Did Any Bit Errors Occur?
No _____
Yes ____ Address _______ Bits _______ 0 Errors

X Direction - Did Any Bit Errors Occur?
No _____
Yes ____ Address _______ Bits _______ 0 Errors
<table>
<thead>
<tr>
<th>Section</th>
<th>Description</th>
<th>Current (mA)</th>
<th>Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.4</td>
<td>Chassis Isolation Impedance</td>
<td></td>
<td>9 megohms</td>
</tr>
<tr>
<td>7.5</td>
<td>Input Signal Loading</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7.5.2</td>
<td>Current from INITIATE PULSE to Gnd</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Current from 2.4V to INITIATE PULSE</td>
<td>≤ 20 μA</td>
<td></td>
</tr>
<tr>
<td>7.5.3</td>
<td>Current from MEM SEL 1 to Gnd</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Current from 2.4V to MEM SEL 1</td>
<td>≤ 20 μA</td>
<td></td>
</tr>
<tr>
<td>7.5.4</td>
<td>Current from MEM SEL 2 to Gnd</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Current from 2.4V to MEM SEL 2</td>
<td>≤ 20 μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Current from MEM SEL 3 to Gnd</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Current from 2.4V to MEM SEL 3</td>
<td>≤ 20 μA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Current from MEM SEL 4 to Gnd</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Current from 2.4V to MEM SEL 4</td>
<td>≤ 20 μA</td>
<td></td>
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<tr>
<td>7.5.5</td>
<td>Current from READ/WRITE to Gnd</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Current from 2.4V to READ/WRITE</td>
<td>≤ 20 μA</td>
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<tr>
<td>7.5.6</td>
<td>Current from ADDRESS 2^0 to Gnd</td>
<td>≤ 2 ma</td>
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</tr>
<tr>
<td></td>
<td>Current from 2.4V to ADDRESS 2^0</td>
<td>≤ 20 μA</td>
<td></td>
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</tbody>
</table>
Date of Test 
Tested By 

Current from ADDRESS 2¹ to Gnd ____ ma  \( \leq 2 \text{ ma} \)
Current from 2.4V to ADDRESS 2¹ ____ \( \mu \text{a} \)
\( \leq 20 \mu \text{a} \)
Current from ADDRESS 2² to Gnd ____ ma  \( \leq 2 \text{ ma} \)
Current from 2.4V to ADDRESS 2² ____ \( \mu \text{a} \)
\( \leq 20 \mu \text{a} \)
Current from ADDRESS 2³ to Gnd ____ ma  \( \leq 2 \text{ ma} \)
Current from 2.4V to ADDRESS 2³ ____ \( \mu \text{a} \)
\( \leq 20 \mu \text{a} \)
Current from ADDRESS 2⁴ to Gnd ____ ma  \( \leq 2 \text{ ma} \)
Current from 2.4V to ADDRESS 2⁴ ____ \( \mu \text{a} \)
\( \leq 20 \mu \text{a} \)
<table>
<thead>
<tr>
<th>S/N</th>
<th>Date of Test</th>
<th>Tested By</th>
<th>Limits</th>
</tr>
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<tr>
<td>Description</td>
<td>Current (mA)</td>
<td>Limit (mA)</td>
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<tr>
<td>Current from DATA IN BIT 1 to Gnd</td>
<td>≤ 2 ma</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 1</td>
<td>≤ 20 μA</td>
<td>≤ 20 μA</td>
<td></td>
</tr>
<tr>
<td>Current from DATA IN BIT 2 to Gnd</td>
<td>≤ 2 ma</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 2</td>
<td>≤ 20 μA</td>
<td>≤ 20 μA</td>
<td></td>
</tr>
<tr>
<td>Current from DATA IN BIT 3 to Gnd</td>
<td>≤ 2 ma</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 3</td>
<td>≤ 20 μA</td>
<td>≤ 20 μA</td>
<td></td>
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<tr>
<td>Current from DATA IN BIT 4 to Gnd</td>
<td>≤ 2 ma</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 4</td>
<td>≤ 20 μA</td>
<td>≤ 20 μA</td>
<td></td>
</tr>
<tr>
<td>Current from DATA IN BIT 5 to Gnd</td>
<td>≤ 2 ma</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 5</td>
<td>≤ 20 μA</td>
<td>≤ 20 μA</td>
<td></td>
</tr>
<tr>
<td>Current from DATA IN BIT 6 to Gnd</td>
<td>≤ 2 ma</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 6</td>
<td>≤ 20 μA</td>
<td>≤ 20 μA</td>
<td></td>
</tr>
<tr>
<td>Current from DATA IN BIT 7 to Gnd</td>
<td>≤ 2 ma</td>
<td>≤ 2 ma</td>
<td></td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 7</td>
<td>≤ 20 μA</td>
<td>≤ 20 μA</td>
<td></td>
</tr>
<tr>
<td>Current from DATA IN BIT 8 to Gnd</td>
<td>≤ 2 ma</td>
<td>≤ 2 ma</td>
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<td>≤ 20 μA</td>
<td>≤ 20 μA</td>
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<tr>
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</tr>
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Current from DATA IN BIT 10 to Gnd _______ ma
Current from 2.4V to DATA IN BIT 10 _______ /a

Current from DATA IN BIT 11 to Gnd _______ ma
Current from 2.4V to DATA IN BIT 11 _______ /a

Current from DATA IN BIT 12 to Gnd _______ ma
Current from 2.4V to DATA IN BIT 12 _______ /a

Current from DATA IN BIT 13 to Gnd _______ ma
Current from 2.4V to DATA IN BIT 14 _______ /a

Current from DATA IN BIT 14 to Gnd _______ ma
Current from 2.4V to DATA IN BIT 14 _______ /a

Current from DATA IN BIT 15 to Gnd _______ ma
Current from 2.4V to DATA IN BIT 15 _______ /a

Current from DATA IN BIT 16 to Gnd _______ ma
Current from 2.4V to DATA IN BIT 17 _______ /a

Current from DATA IN BIT 17 to Gnd _______ ma
Current from 2.4V to DATA IN BIT 17 _______ /a
## VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS

### 7.6.3 READ COMPLETE voltage

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### 7.6.4 DATA OUT BIT 0 voltage

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<td>Memory +5V Voltage</td>
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<td>Memory -6.1V voltage</td>
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<td></td>
<td>+5V Current</td>
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<tr>
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<td>+5V Power</td>
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<td>Memory -6.1V Voltage</td>
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<td>DO-17</td>
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Refer to test proc.
7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?
No _____
Yes _____ Address _____ Bits _____ 0 errors

7.9.4 Did an error occur?
No _____
Yes _____ Address _____ Bits _____ 0 errors

7.9.10 Did an error occur?
No _____
Yes _____ Address _____ Bits _____ 0 errors

7.9.16 Did an error occur?
No _____
Yes _____ Address _____ Bits _____ 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?
No _____
Yes _____ Address _____ Bits _____ 0 errors

7.10.7 Did an error occur?
a) No _____
Yes _____ Address _____ Bits _____ 0 errors

220
7.11 NON-VOLATILITY TEST

7.11.7 Did an error occur?

7.11.9 No

Yes Address Bits

7.12 MEMORY SELECT TEST

7.12.3 Address (Octal)

7.12.4 Address 0001 (Octal)

0000

0010 (Octal)

0000

0011 (Octal)

0000

0100 (Octal)

0000

0101 (Octal)

0000

0110 (Octal)

0000

0111 (Octal)

0010 (Octal)

0000

1000 (Octal)

0000

1001 (Octal)

0000

1010 (Octal)

0000
S/N ________

Date of Test ________
Tested By ________

Address 1011 ________ (Octal) 0000
1100 ________ (Octal) 0000
1101 ________ (Octal) 0000
1110 ________ (Octal) 0000

7.12.6 Did an error occur?
No ______
Yes ______ Address ______ Bits ______ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?
No ______
Yes ______ Address ______ Bits ______ 0 errors

7.13.3 Did an error occur?
No ______
Yes ______ Address ______ Bits ______ 0 errors
S/N __________

Date of Test __________

Tested By __________

Limits

7.13.4 a) Did an error occur?

No ______

Yes ______ Address ______ Bit ______ 0 errors

b) Did an error occur?

No ______

Yes ______ Address ______ Bit ______ 0 errors
APPENDIX II

STACK TEST PROCEDURE
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<td>CT-0179</td>
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</tr>
<tr>
<td>REV 1</td>
</tr>
<tr>
<td>OF SHEETS</td>
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1. SCope

1.1 This test procedure specifies the electrical tests to be performed on all 01-P13707D plated wire memory stacks.

2. Applicable Documents

2.1 Drawing No. 69-P07708E, Interconnect Drawing
2.2 Drawing No. 69-P13705D, Interconnect Diagram, Memory
2.3 Drawing No. 01-P13707D, Memory Stack Assembly
2.4 Drawing No. 69-P10930D, Diagram of the Word Drive Test Adapter Boxes.
2.5 Drawing N. 99-P07707E, Restore Timing.

3. Special Requirements

3.1 Test cables as shown in Figures 1, 2, & 3.
3.2 Stack & Timing Interface Adapters 69-P10930D.
3.3 Four 52 pin to 64 pin adapters, 84-P04070D001.

4. Stack Tester/Adapter Box/Stack Interconnect

4.1 The interconnections between the EH8500 Stack Tester, the Word Drive Test Adapter Box and the Word Line Interface Boards are shown in Interconnect Drawing No. 69-P07708E. Switches 1-5 are to be set to 4278, switches 6 & 7 to ON. The Sense & Word Line Interconnections are shown in Figures 4 & 5.
5. TEST CONDITIONS

5.1 SENSE TERMINATION
The sense lines are to be terminated by 100 ohm (± 1%) resistors to ground. The terminating resistors may be mounted at the input to the sense amplifier.

5.2 STACK RESTORE
The Restore Timing is shown in the Restore Timing Drawing No. 99-P07707E. The restore pulse width is adjusted, along with the restore voltage, to recharge the previously selected first and second level word select lines to +5V at the beginning of the following cycle.

5.3 CURRENT PULSE WAVEFORMS
The current pulse waveforms (as shown in Figure 6) are to be set up initially using a current probe (calibrated to ± 1% @ 40 and 500 ma) to monitor the word and digit currents at the locations shown in Figure 7. The amplitudes of all currents are given in Section 5.4.

5.3.1 The overshoot on any current shall be less than 2% of the specified current amplitude.

5.3.2 The droop on any current shall be less than 2% of the specified current amplitude.

5.3.3 The overlap and steering for the word and digit currents is specified in Figure 6.

5.3.4 All times specified are ± 2%, or one nanosecond, whichever is greater.
5.4 CURRENT AMPLITUDES
Current amplitudes are milliamperes, ± 1%, as measured at mid-point of the flat top.

5.4.1 Read Current
Read Current = I_{WR} = 475 ma.

5.4.2 Write Currents
Word Current = I_{WW} = 475 ma.

<table>
<thead>
<tr>
<th>Digit Current I_{DW1}</th>
<th>+25°C ±5</th>
<th>95°C -5</th>
<th>+5</th>
<th>0°C -0</th>
<th>-40°C -5</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>41.0</td>
<td>35.0</td>
<td>48.0</td>
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<table>
<thead>
<tr>
<th>Digit Current I_{DW2}</th>
<th>+5</th>
<th>0°C -0</th>
<th>-40°C -5</th>
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<tbody>
<tr>
<td></td>
<td>39.0</td>
<td>33.0</td>
<td>46.0</td>
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</tbody>
</table>

5.4.3 Disturb Currents
Word Current = I_{WD} = 525 ma.

<table>
<thead>
<tr>
<th>Digit Current I_{DD1}</th>
<th>+25°C ±5</th>
<th>95°C -5</th>
<th>+5</th>
<th>0°C -0</th>
<th>-40°C -5</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>45.5</td>
<td>40.0</td>
<td>53.5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Digit Current I_{DD2}</th>
<th>+5</th>
<th>0°C -0</th>
<th>-40°C -5</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>48.0</td>
<td>42.0</td>
<td>57.0</td>
</tr>
</tbody>
</table>

5.5 TEMPERATURE TESTING
All electrical tests shall be performed at the three temperatures. The tests shall be run in the following order.

5.5.1 Test all outputs at 25 ± 5°C. Peak amplitude of output shall be 4.5 millivolts minimum.
5.5.2 Interchange connectors on J12 & J1 of the Word Drive Adapter Box.

5.5.3 Repeat paragraph 5.5.1.

5.5.4 Test all outputs at 95° ±5°C. Peak amplitude of all outputs shall be 4.5 millivolts minimum.

5.5.5 Interchange connectors on J12 & J1 of the Word Drive Adapter Box.

5.5.6 Repeat paragraph 5.5.4.

5.5.7 Test all outputs at -40° ±0°C. Peak amplitude of all outputs shall be 4.5 millivolts minimum.

5.5.8 Interchange connectors on J12 & J1 of the Word Drive Adapter Box.

5.5.9 Repeat paragraph 5.5.7.

5.6 TEST PATTERN

The test pattern shall be as shown in Figure 8.
ALL DIODES ARE IN 3600
+5, 1/4 WATT BOARD, BD-1

INTERFACE BOARD, BD-1

TO BNC CONNECTOR J2

TO CANNON CONNECTOR J1

FIGURE 1: STACK TEST CABLE
TO CANNON CONNECTOR J1

FIGURE 2: STACK TEST CABLE
FIGURE 3: STACK TEST CABLE

ALL DIODES ARE 1N3600
ALL RESISTORS 2.2K OHMS
±5%, 1/4 WATTS

INTERFACE BOARD BD-3

TWISTED PAIR

FRONT TOP

J12-28
27 26 25 24 23 22 21 18 12 11 10 9 4 3 2

J12-32
31 30 29 24 22 21 16 15 14 13 8 7 6 5

MOTOROLA INC.
Government Electronics Division
8301 E. McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

SIZE CODE IDENT NO. DWG NO.
A 94990 12-P13729D

SCALE REVISION SHEET
DIGIT DRIVE TEST FIXTURE INTERCONNECT

FIGURE 4

FLAT PACKS  STACK

XP3  XP4  XP5  XP6

84-P04070D001 ADAPTER BOARD

1 PINS 64 1 PINS 64 1 PINS 64 1 PINS 64

J1  J7  J2  J8

TEST CABLE TEST CABLE TEST CABLE TEST CABLE
PLATED WIRE MEMORY STACK

TO J12 ON THE WORD DRIVE ADAPTER BOX & J5 ON THE WADE TRON.

INTERFACE BOARD BD-3

INTERFACE BOARD BD-2

INTERFACE BOARD BD-1

TO J2 ON THE WORD DRIVE ADAPTER BOX

FIGURE 5 WORD LINE INTERCONNECT
FIGURE 6  Current Waveforms

\[ DS = 40 \text{ nanoseconds between } I_W 10\% \text{ & } I_D 90\% \text{ points.} \]

\[ D_r = D_f = 80 \text{ nanoseconds, 10\% to 90\%.} \]

\[ D_w = 220 \text{ nanoseconds, between 50\% points.} \]

\[ D_D = 150 \text{ nanoseconds, between 50\% points.} \]

\[ W_r = 75 + 5 \text{ nanoseconds, 10\% to 90\%.} \]

\[ W_W = 200 \pm 10 \text{ nanoseconds, between 50\% points.} \]

\[ W_D = 60 \text{ nanoseconds, between 90\% points.} \]

\[ W_f = 40 \text{ nanoseconds 10\% to 90\%.} \]
Indicates points at which currents are to be monitored on word and digit inputs and point at which sense output signal is specified.

FIGURE 7
Current Monitoring Points
## ADJACENT BIT DISTURB WITH INTERLEAVED READ/WRITE (NDRO)

<table>
<thead>
<tr>
<th>BIT UNDER TEST</th>
<th>HISTORY</th>
<th>WRITE</th>
<th>UV READ</th>
<th>WRITE</th>
<th>READ</th>
<th>WRITE</th>
<th>READ</th>
<th>DV READ</th>
</tr>
</thead>
<tbody>
<tr>
<td>LAB</td>
<td>IWD</td>
<td>IWD</td>
<td>IWD</td>
<td>IWD</td>
<td>IWD</td>
<td></td>
<td>IWD</td>
<td>IWD</td>
</tr>
<tr>
<td>RAB</td>
<td>IWD</td>
<td></td>
<td></td>
<td>IWD</td>
<td>IWD</td>
<td></td>
<td>IWD</td>
<td>IWD</td>
</tr>
<tr>
<td>DIGIT</td>
<td>IDD1</td>
<td>IDD1</td>
<td>IDD1</td>
<td>IDA2</td>
<td>IDD1</td>
<td>IDD1</td>
<td>IDD1</td>
<td>IDD1</td>
</tr>
</tbody>
</table>

- **NO. OF CYCLES**: 10³, 1, 1, 10³, Minimum

**Entire Program Repeated with Opposite Polarity Digit Currents**

**Figure 8: Test Pattern**