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(NASA-CR-134310) CODED SPREAD SPECTRUM DIGITAL TRANSMISSION SYSTEM DESIGN STUDY Final Report (Linkabit Corp.) 126 p HC $9.50 CSCL 17B

N74-27624

Unclas

G3/07 43170

LINKABIT CORPORATION

10453 ROSELLE STREET
UNIVERSITY INDUSTRIAL PARK
SAN DIEGO, CALIFORNIA 92121

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CODED SPREAD SPECTRUM DIGITAL TRANSMISSION SYSTEM DESIGN STUDY

By: J.A. Heller
J.P. Odenwalder
A.J. Viterbi

LINKABIT CORPORATION
10453 Roselle Street
San Diego, CA 92121

May 1974

Final Report on Contract No. NAS9-13733

for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
Lyndon B. Johnson Space Center
Houston, Texas 77058

Abstract

This report presents the results of a comprehensive study of the performance of Viterbi-decoded convolutional codes in the presence of nonideal carrier tracking and bit synchronization. A constraint length 7, rate 1/3 convolutional code and parameters suitable for the Space Shuttle coded communications links are used. Mathematical models are developed and theoretical and simulation results are obtained to determine the tracking and acquisition performance of the system. Pseudorandom sequence spread spectrum techniques are also considered to minimize potential degradation caused by multipath.

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1.0 Introduction

The Coded Spread Spectrum Digital Transmission System Design Study represents a comprehensive investigation of the system whose functional block diagram is given in Figure 1.1. This system was initially defined in Ref. 1.1 based on the Space Shuttle mission configuration.

The emphasis of this study has been on determining the impact of practical bit synchronizer and carrier tracking loops on the performance of the coded transmission system. Mathematical models have been developed for each loop and programmed to obtain extensive performance simulation for both the tracking and acquisition modes.

This report, just as the study whose results it presents, is organized from the user outward. Section 2 briefly summarizes the existing implementation of a convolutional encoder-Viterbi decoder for a K = 7, rate 1/3 code and considers its error performance with ideal demodulation and tracking. Section 3 treats the design, implementation, and impact on decoder performance of a practical bit synchronizer for the BIϕ-L binary PSK modulation used. In addition to tracking simulations to determine the degradation in decoded bit error probability,

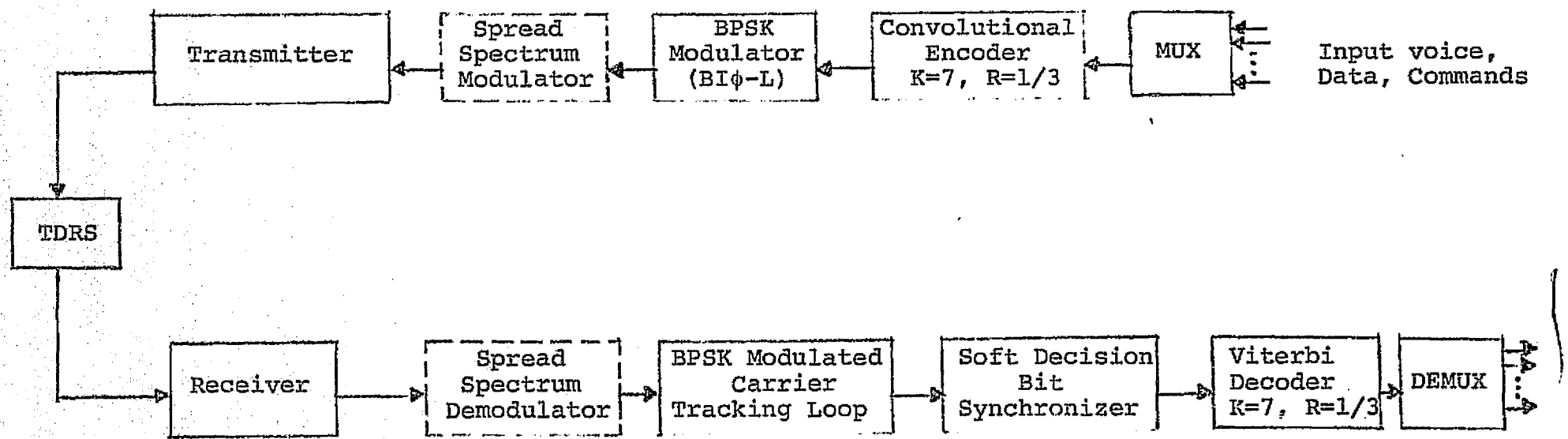

Figure 1.1 Overall Communication System Block Diagram

considerable attention and simulations are devoted to synchronizer loop acquisition performance. Section 4 incorporates the effects of the carrier tracking loop. Both Costas and decision-directed loops are considered, with considerable performance improvement demonstrated by the latter. Simulation results are obtained for decoder performance degradation due to the combination of bit synchronizer and carrier tracking loops, as well as for the joint acquisition behavior of both loops.

Spread spectrum modulation and demodulation is treated in Section 5. The original emphasis on spread spectrum modulation was reduced early in the performance of this study on the basis of a relaxation in the CCIR guidelines on maximum power density at the earth's surface caused by space communication transmission. As a result, extensive design and evaluation of performance impact of this subsystem was not undertaken, and these efforts were partially redirected to a more extensive study of the other loops. However, pseudorandom sequence spread spectrum modulation provides an effective technique for greatly reducing the detrimental effects of multipath. Hence, consideration of spread spectrum techniques was maintained as part of the study, but specifically to assess the reduction of multipath susceptibility rather than the reduction in energy density at the earth's surface. Coded

system performance simulation was carried out with spread spectrum modulation in the presence of multipath, and the results are treated in Section 5.

Section 6 summarizes the results of this comprehensive study, which is the first to thoroughly investigate the effect of both carrier tracking and bit synchronization loops on convolutionally coded system performance. Conclusions are drawn and recommendations made for further investigation.

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1.1 B. H. Batson and R. W. Moorehead, "A Digital Communications System for Manned Spaceflight Applications," in Proceedings of the 1973 International Conference on Communications, Seattle, Washington, pp. 37-1 - 37-9.

2.0 Review of Viterbi Decoding Theory, Implementation, and Performance

Since numerous Viterbi decoders for constraint length 7 codes have been implemented by LINKABIT Corporation since early in 1971 and they have been tested and operated on space links since early in 1972, no effort was devoted on this study to Viterbi decoder implementation and performance evaluation per se.

However, for completeness, a summary of theory and implementation is included in this section. The performance curve given in Figure 2.4 was obtained using a channel simulator with an actual K = 7, rate 1/3, Viterbi decoder, the LINKABIT LV7015LR, which was developed under a company-sponsored IR & D program. Its implementation complexity is summarized in Section 2.3.

2.1 Convolutional Coding-Viterbi Decoding

A binary convolutional coder consists of a K stage binary shift register and v mod-2 adders. Each of the mod-2 adders is connected to certain of the shift register stages. The pattern of connections specifies the code. Information bits are shifted into the encoder shift register one bit at a time. After each shift, the outputs of the mod-2 adders are sampled sequentially yielding the code symbols. These code symbols are then used by the modulator to specify the waveforms to be sent over the channel. Since v code symbols are generated for each information bit, the code rate R_n is 1/v information bits per code symbol. The constraint length of the code is K, since that is the number of shifts over which a single information bit can influence the encoder output. The state of the convolutional encoder is the contents of the first (K - 1) shift register stages. The encoder state together with the next input bit uniquely specify the v output symbols.

As an example, a K = 3, v = 2 encoder is shown in Figure 2.1. The first two coder stages specify the state of the encoder; thus, there are 4 possible states. The code words, or sequences of code symbols, generated by the encoder for various input information bit sequences is shown in the code "trellis" of Figure 2.2. The code trellis is really just a state diagram for the encoder of Figure 2.1. The four

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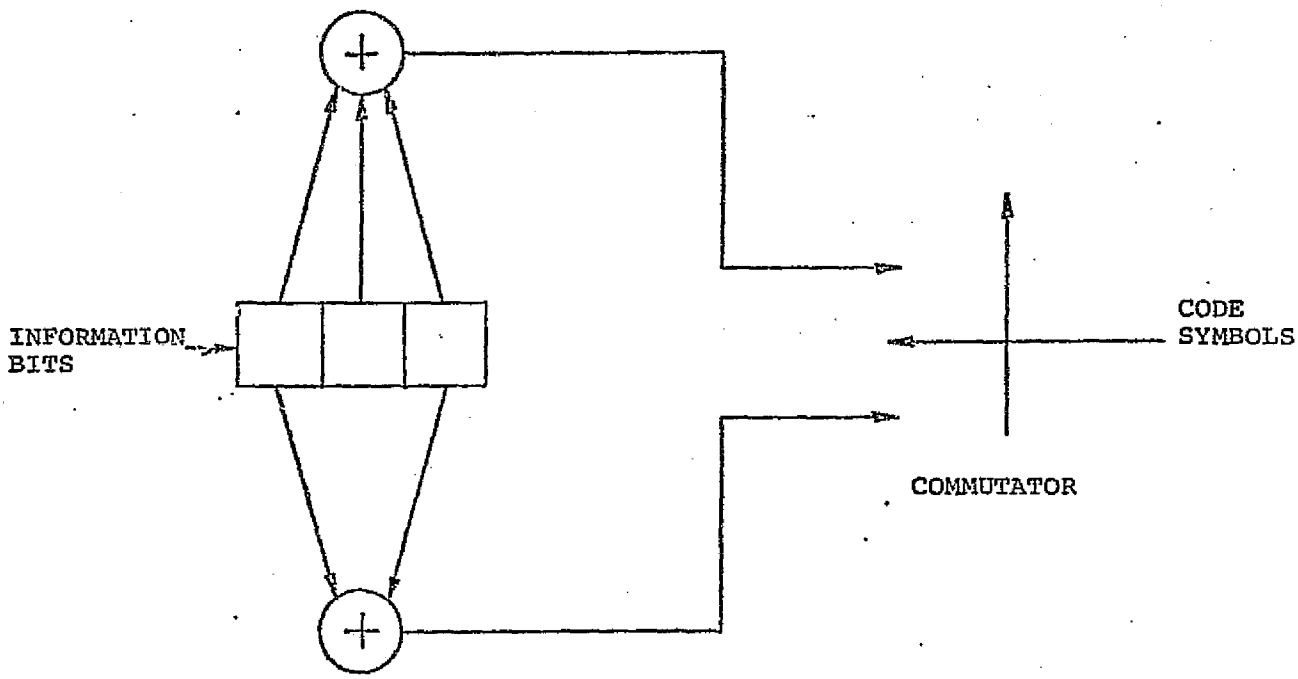

Figure 2.1. A K=3, R_n = 1/2 Convolutional Encoder

states are represented by circled binary numbers corresponding to the contents of the first two stages of the encoder. The lines or "branches" joining states indicate state transitions due to the input of single information bits. Dashed and solid lines correspond to "1" and "0" input information bits, respectively. The trellis is drawn under the assumption that the encoder is in state 00 at time 0. If the first information bit were a 1, the encoder would go to state 10 and would output the code symbols 11. Code symbols generated are shown adjacent to the trellis branches. As an example, the input data sequence 101 ... generates the code symbol sequence 111000 ... . Further interpretations of the encoder state diagram and a discussion of "good" convolutional codes is presented in Reference 2.1.

The binary symbols output by the encoder are used to modulate a carrier. In the case of binary PSK modulation, each code symbol results in the transmission of a pulse of carrier at either of two 180° separated phases depending on whether the symbol is a zero or one.

A coherent PSK demodulator consists of a filter matched to the pulse modulating waveform. The output of the matched filter sampled at the end of each pulse will tend to be positive if a zero was sent and negative if a one was sent. The sampled filter output may be hard quantized (where only the sign is saved), or quantized to many levels prior to

input to the decoder. Hard quantization results in about a 2 dB degradation in decoder performance compared to infinitely fine quantization; whereas 8 levels of quantization is fine enough to cause a loss of only .25 dB.

A thorough discussion of the Viterbi decoding algorithm is presented by Viterbi, (Reference 2.1). Here, it will suffice to review the algorithm and elaborate on those features and parameters which bear on decoder performance, complexity, and power dissipation.

Referring to the code trellis diagram of Figure 2.2, a brute-force maximum likelihood decoder would calculate the likelihood of the received data for code symbol sequences on all paths through the trellis. The path with the largest likelihood would then be selected, and the information bits corresponding to that path would form the decoder output. Unfortunately, the number of paths for an L bit information sequence is 2^L; thus, this brute force decoding quickly becomes impractical as L increases.

With Viterbi decoding, it is possible to greatly reduce the effort required for maximum likelihood decoding by taking advantage of the special structure of the code trellis. Referring to Figure 2.2, it is clear that the trellis assumes a fixed periodic structure after trellis depth 3 (in general, K) is reached. After this point, each of the 4 states can be entered from either of two preceding states. At depth 3, for instance, there are 8 code paths, 2 entering each state.

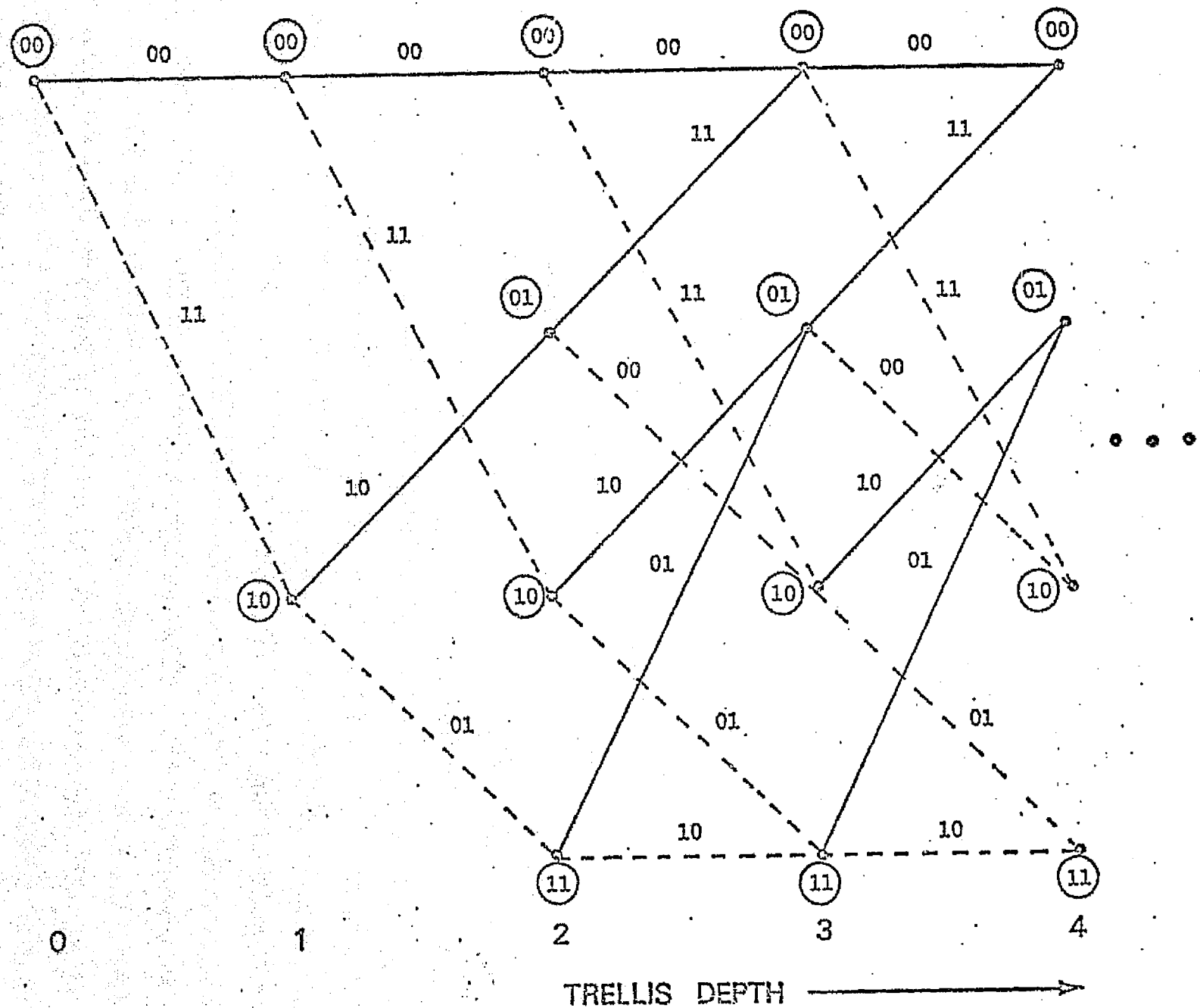

Figure 2.2. Code Trellis Diagram

For example, state 00 at level 3 has the two paths entering it corresponding to the information sequences 000 and 100. These paths are said to have diverged at state 00, depth 0 and remerged at state 00, depth 3. Paths remerge after 2 [in general (K-1)] consecutive identical information bits. A Viterbi decoder calculates the likelihood of each of the 2 paths entering a given state and eliminates from further consideration the less likely path that leads to the state. This is done for each of the $2^{(K-1)}$ states at a given trellis depth; after each decoding operation only one path remains leading to each state. The decoder then proceeds one level deeper into the trellis and repeats the process.

For the K = 3 code trellis of Figure 2.2, there are 8 paths at depth 3. Decoding at depth 3 eliminates 1 path entering each state. The result is that 4 paths are left. Going on to depth 4, the decoder is again faced with 8 paths. Decoding again eliminates 4 of these paths, and so on. Note that in eliminating the less likely paths entering each state, the Viterbi decoder will not reject any path which would have been selected by the brute force maximum likelihood decoder.

The decoder as described thus far never actually decides upon one most likely path. It always retains a set of $2^{(K-1)}$ paths after each decoding step. Each retained path is the most likely path to have entered a given encoder state. However, it can be shown that, with high probability, the $2^{(K-1)}$ decoder selected paths will not be mutually disjoint very far

back from the present decoding depth. All of the $2^{(K-1)}$ paths tend to have a common stem which eventually branches off to the various states. Thus, if the decoder stores enough of the past information bit history of each of the $2^{(K-1)}$ paths, then the oldest bits on <u>any</u> path may be used as the decoder output. A better strategy is to output the oldest bit on the path leading to the state that currently has the highest likelihood.

The great advantage of the Viterbi maximum likelihood decoding algorithm is that the number of decoding operations performed in decoding L bits is only $L2^{(K-1)}$ which is linear in L. Of course, Viterbi decoding as a practical technique is limited to relatively short constraint length codes due to the exponential dependence of decoder operations per bit decoded on K. Fortunately, excellent decoder performance is possible with good short constraint length codes.

2.2 Decoding Partitioning - Block Diagram

Figure 2.3 shows a block diagram of a Viterbi decoder. The decoder blocks will be described with reference to the constraint length 7, rate 1/3 Viterbi decoder under consideration.

Each code bit time, a 3-bit (soft) or a 1-bit (hard) quantized matched filter output is input to the decoder. The input processor correlates sets of 3 contiguous quantized matched filter outputs with each of the 8 possible code symbols, 000, 001, ..., 111, which can appear on a rate 1/3 trellis branch. Quantized values of these 8 correlations are inversely proportional to branch log likelihoods. These quantized values are called branch metrics. We take the convention that the lower the branch metric, the better the correlation between the branch code symbols and the quantized received data. The input processor generates 8 branch metrics during each information bit or branch time.

The arithmetic processor selects the most likely of the 2 ways of entering each of the $2^{(K-1)} = 64$ states at a given level in the code trellis. At each code trellis level, the decoder stores in the state metric memory a state metric or measure of the likelihood of the best path entering each of the 64 states. During each bit time, for each of the $2^{(K-1)}$ next states, the arithmetic processor adds 2 branch metrics to 2 predecessor state metrics, chooses the smallest sum (best correlation) and stores that sum as the new state metric of the next state.

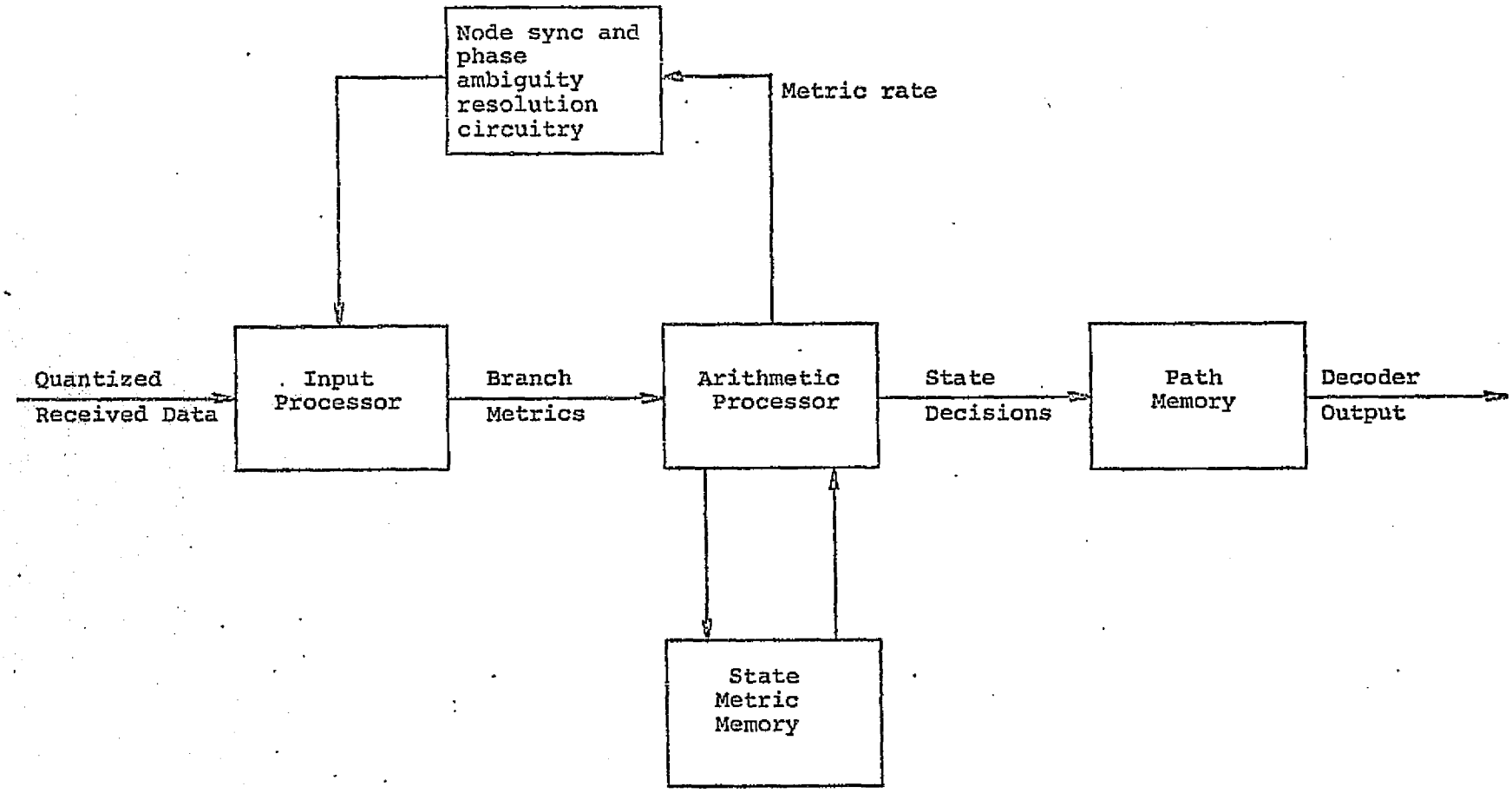

Figure 2.3. Viterbi Decoder Functional Block Diagram

In addition to storing a state metric for each state, the decoder path memory stores the past 32 information bits on the best path leading to each state. It has been determined, through computer simulation and direct testing of the LINKABIT rate 1/3, K=7 LV7015LR Viterbi decoder, that a decoder path storage of 32 bits per state path results in negligible performance degradation (<.05 dB) compared to infinite path lengths. After the arithmetic processor performs its 2^{K-1} state operations each information bit time, the 32nd or last bit on the path corresponding to the lowest (best) metric state is output by the decoder.

The function of the node sync and phase ambiguity resolution circuitry is to resolve input processor node sync and modem 180° phase ambiguity by observing the rate of state metric increase. If the rate of metric increase is too rapid, the assumed node sync position is changed or the received data is inverted to compensate for a possible 180° phase inversion. The input processor cycles through 6 possible node sync - phase ambiguity states (3 node sync states for rate 1/3 and a 2 way phase ambiguity).

Since the number of decoder arithmetic operations per bit time is 2^{K-1} and the metric and path memory is proportional to 2^{K-1}, the decoder complexity grows exponentially with constraint length K. Even for short constraint lengths (i.e., K=7) the complexity of a brute force decoder implementation can be very large. During the past several years, LINKABIT

has modified and simplified the Viterbi decoding algorithm to allow an implementation many times less complex (in number and cost of integrated circuits) than more obvious brute force approaches. These developments have culminated in the LV7015 series of Viterbi decoders in the 100 Kbps range, and other high speed Viterbi decoders.

2.3 Viterbi Decoder Performance and Complexity

Figure 2.4 shows the bit error rate versus energy per bit to noise ratio, E_b/N_o, for the LINKABIT LV7015LR rate 1/3, K = 7 Viterbi decoder using 3-bit soft quantized received data. The LV7015LR uses the code whose three generators are 1011011, 1111001, 1100101. The decoder employs a 32 bit path memory. The performance curve of Figure 2.4 has been confirmed by extensive simulation and testing.

The LV7015LR utilizes 60 standard TTL integrated circuits and has a power requirement of 5.6 watts, exclusive of power supply.

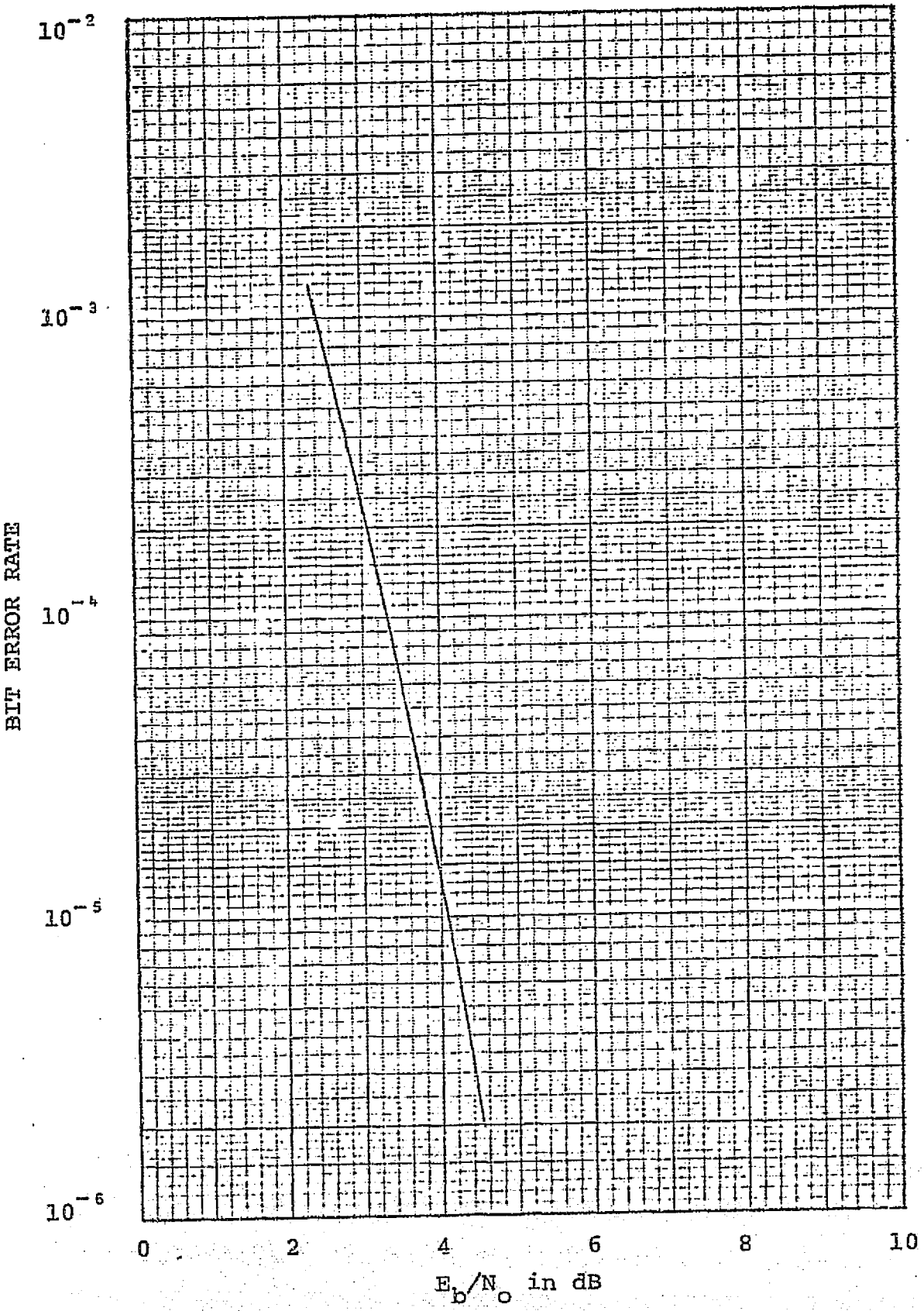

Figure 2.4. Performance of LINKABIT LV7015LR Rate 1/3 Convolutional Encoder-Viterbi Decoder with 3-bit Quantized Received Data

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SECTION 2. REFERENCES

2.1. Viterbi, A.J. "Convolutional Codes and Their Performance in Communication Systems," IEEE Transactions on Communication Technology, Vol. COM-19, No. 5, Part II, October, 1971.

2.2 Heller, J. A. and I. M. Jacobs, "Viterbi Decoding for Satellite and Space Communication," IEEE Transactions on Communication Technology, Vol. COM-19, No. 5, Part II, October, 1971.

3.0 Bit Synchronizer Theory, Implementation and Effect on Coded Performance

The extensive literature available on the subject of bit synchronizers (Ref. 3.1 - 3.4 among many) deals almost exclusively with the problem of synchronization of a bit stream which employs NRZ-L modulation. Practically none of the references have addressed in any significant detail the problem for BIØ-L modulation. This form of modulation offers both advantages and disadvantages for acquiring and tracking the bit or symbol timing.

The obvious advantage is that since a transition is provided with certainty during each bit period, a greater effective signal-to-noise ratio is guaranteed in the tracking loop. This is particularly useful during acquisition. In fact, with random data, the average number of transitions is tripled. Furthermore, it avoids the problem of maintaining synchronization when a long sequence of zeros or ones occurs in the random data*.

There are, however, some potential disadvantages of BIϕ-L modulation. These are, in order of importance:

a) A given fixed timing error will degrade BIϕ-L somewhat more than it degrades NRZ-L modulation; this will be

*With rate 1/3 convolutional coding, however, a minimum average of two transitions in 9 bits can be guaranteed by proper code selection (see Appendix II).

partially or completely offset by the reduction in timing error achieved by the BIϕ-L loop.

b) A bit synchronization loop for BIϕ-L exhibits a two-way ambiguity, with the possibility of locking with a half-bit timing error. (Sec. 3.3). This condition can be detected and corrected. (Sec. 3.6).

c) The bandwidth occupancy is approximately double that of NRZ-L.

The spectral densities of the two modulations, are respectively (Ref. 3.2) for a bit time T,

$$S(f) = [\sin(\Pi fT)]^2/(\Pi fT)^2 \text{ for NRZ-L}$$

$$S(f) = [\sin(\Pi fT/2)]^4/(\Pi fT/2)^2 \text{ for BI}\phi\text{-L}$$

so that the main lobe extends over double the bandwidth in the latter case.

Bandwidth occupancy is not likely to be particularly significant in this application, other than that for a fixed predetection filter, signals with wider bandwidth will be more susceptible to intersymbol interference effects. The other two difficulties with BIØ-L modulation, (a) and (b), will be evaluated quantitatively in Section 3.3.

Bit synchronizers are members of the class of tracking and synchronization systems whose performance may be generally evaluated by the classical phase-locked loop analysis (Refs. 3.1, 3.5). Key performance parameters are

a) timing error variance and its dependence on loop gain, bandwidth, and filter (order) parameters;

b) steady-state timing errors due to doppler and doppler rates;

c) acquisition time and range.

In addition, bit synchronizer performance is measured by the degradation suffered due to timing errors in the bit error detector, whose timing is derived by the synchronizer. This, in fact, is the most important parameter in the present application.

While it is possible to treat this problem fairly generally, though approximately, by making enough simplifying assumptions (Refs. 3.2, 3.4) a precise analysis (or simulation) requires first of all the specification of the form of the bit synchronizer timing-error detector, which is the counterpart to the phase detector in carrier phase locked loop tracking systems. Numerous error detectors have been proposed, analyzed, and implemented for bit synchronizers operating on NRZ-L data. These include the early-late gate, the data-transition tracking loop, the absolute value type sychronizer, and the difference of squares loop. (Refs. 3.1, 3.2, 3.3, 3.4, 3.10). To our knowledge no such studies or developments have appeared for BIϕ-L modulation bit synchronizers. It

is possible, of course, to construct parallels of each' of the above type of error detector for BIØ-L. However, the guaranteed transition in the middle of the bit reduces the importance of several of the techniques and provides the opportunity for simplification. In particular, determination of the existence of a transition between bits is less critical.

3.1 Bit Synchronizer Timing-Error Detectors for BIØ-L Modulation: Techniques and Performance Analysis

A general bit synchronizer block diagram is illustrated in Figure 3.1. The loop filter may be either analog or digital. A digital mechanization of the VCO would employ an accumulator, a crystal oscillator clock and a timing (phase) shifter, possibly implemented by a variable modulus divider.

Functional block diagrams of four types of error detectors, denoted A, B, C, and D, are presented in Figures 3.2 and 3.3. Types A and B differ only according to whether or not the hard limiter is included and similarly for types C and D. In each case the upper (X) channel of the detector incorporates the bit detector and its output is fed to the A/D converter. If the bit-to-bit transitions were ignored, and only the guaranteed center transition were used for synchronization, then the Y gate in Figure 3.2 would include only the interval $\frac{T}{2} - \Delta < t < \frac{T}{2} + \Delta$. Similarly in Figure 3.3 the lowest gate, Y_2, could be omitted. The choice of gate width* 2Δ is governed by the values of input and desired loop SNR and dynamic range. The narrower the gate, the higher the loop SNR for a given input noise level; however a narrow gate produces an error detector characteristic which

*In some of the bit synchronizer literature (Refs. 3.4, 3.8), this is called the window and denoted $W = 2\Delta/T$.

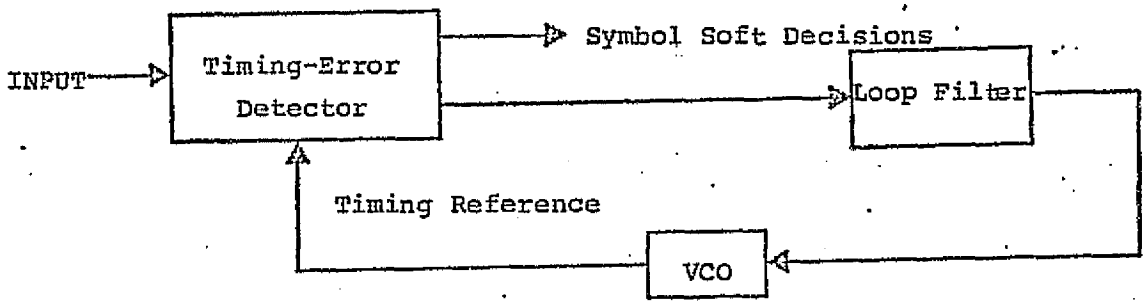

Figure 3.1 Bit Synchronizer Block Diagram

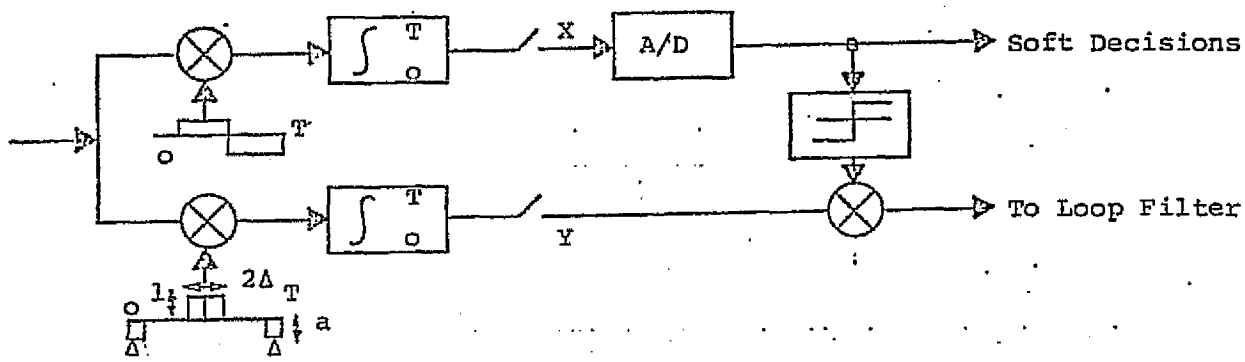

Figure 3.2 Functional Block Diagram of Type A (with hard limiter) and Type B (without limiter) Detectors

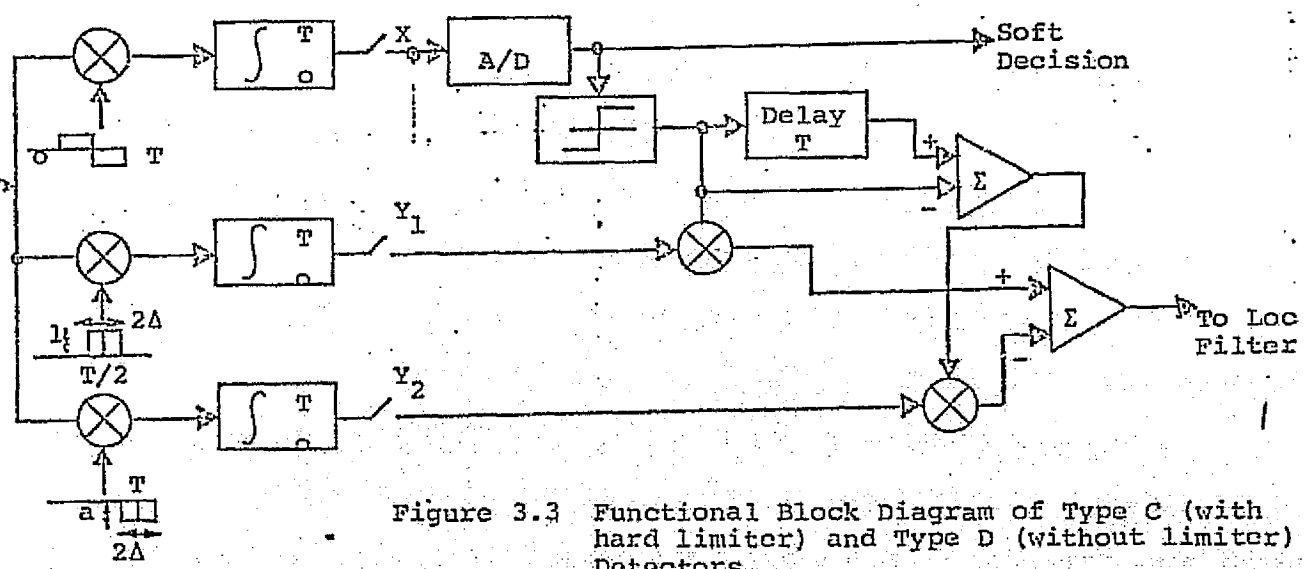

Figure 3.3 Functional Block Diagram of Type C (with hard limiter) and Type D (without limiter) Detectors

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saturates beyond small timing errors. These observations will presently be substantiated quantitatively.

Gates at the bit edges will contribute constructively to the timing error measurement only half the time on the average. In the type A error detector, the edge gate outputs are used during each bit period; thus noise alone is introduced half the time. In the type C detector, the Y_2 gate output is used only when a bit transition is detected (by comparing two successive bit decisions out of the X channel). Hence type C should operate better than type A at high input SNR where the bit decisions are reliable. On the other hand, at SNR below 0dB the unreliable bit decisions may render the advantage negligible. In any case, since the edge gate detector outputs may be less reliable than the mid-bit gate outputs, it is reasonable to weigh the former less heavily than the latter. This is shown in Figures 3.2 and 3.3 by scaling the edge gate reference waveforms by a constant a ($0 \leq a < 1$).

Since the bit detector X is soft quantized to 8 levels (for decoding purposes), it is reasonable to consider using soft quantized rather than hard quantized outputs of the X channel in combining with the Y channel gates. An argument for this might be that if the magnitude of the X channel output is small, there is less confidence in its reliability. Hence it may be reasonable to weigh the Y

gate outputs less in this situation. This can be done by simply eliminating the hard limiters in both configurations. Thus types B and D error detectors are the same as types A and C, respectively, with soft decisions at the Y outputs substituted for hard. It is also worth noting that when soft decisions are used, the advantage of type C over type A may not carry over to the comparison of types D and B. It appears, however, that the performance difference between hard and soft quantization is sufficiently small in this application that the additional complexity may not be warranted.

Bit synchronizers employing type A and B timing-error detectors can be analyzed exactly for first-order loops and with a slight approximation (Ref. 3.5), the results apply also to second-order loops. This analysis is carried out in Appendix I. (For type B the quantization of the X channel is taken to be infinitely fine). The result in both cases can be summarized as follows. For a bit time T, loop bandwidth B_L, bit (or symbol) energy-to-noise density, E/N_o, gate half-width* $\Delta = \delta T$ and bit-edge gate amplitude a (see Figure 3.2), the steady-state timing-error probability density function is

* In some of the NRZ-L bit synchronizer literature (Refs. 3.4, 3.8) the term window is used, with $W = 2\delta$, at the bit edge only.

$$\pi(\tau) = \frac{\exp\,[-f(\tau)]/h(\tau)}{\int_{-1/2}^{1/2} \{\exp\,[-f(x)]/h(x)\}dx} \qquad -1/2 \leq \tau \leq 1/2 \tag{3.1}$$

where τ is the relative timing error (as a fraction of a bit),

$$f(\tau) = \frac{\gamma\, E/N_o}{2B_L T\delta(1+a^2)} \int_o^{\tau} \frac{g(y)}{h(y)}\, dy \tag{3.2}$$

where :

$$\gamma = \begin{cases} 1 \text{ for Type A} \\ 2E/N_o \text{ for Type B} \end{cases}$$

and $g(\tau)$ and $h(\tau)$ are respectively the normalized mean and variance of the timing-error detector output. These differ, of course, depending on the type of detector* and the parameters δ, a, and E/N_o. The function $g(\tau)$ is plotted in Figure 3.4 for Type A detectors for E/N_o = -5 dB, 0 dB and -5 dB and δ = 1/8. $g(\tau)$ is sometimes called the error (or phase) detector characteristic or S-curve. The smaller δ, the larger its slope at τ = 0, and hence the loop gain in this region; however, the detection characteristic saturates beyond δ.

*This analysis shows that the Type B loop modelled without quantization is inferior to Type A loops at low SNR; this somewhat surprising conclusion is explained by recognizing that, while a linear measure is better for small values of X, some saturation should be provided for high values. Thus a soft limiter (or A/D converter) appears to be the optimum nonlinearity for the X channel, while the analysis assumed a perfectly linear measurement of X.

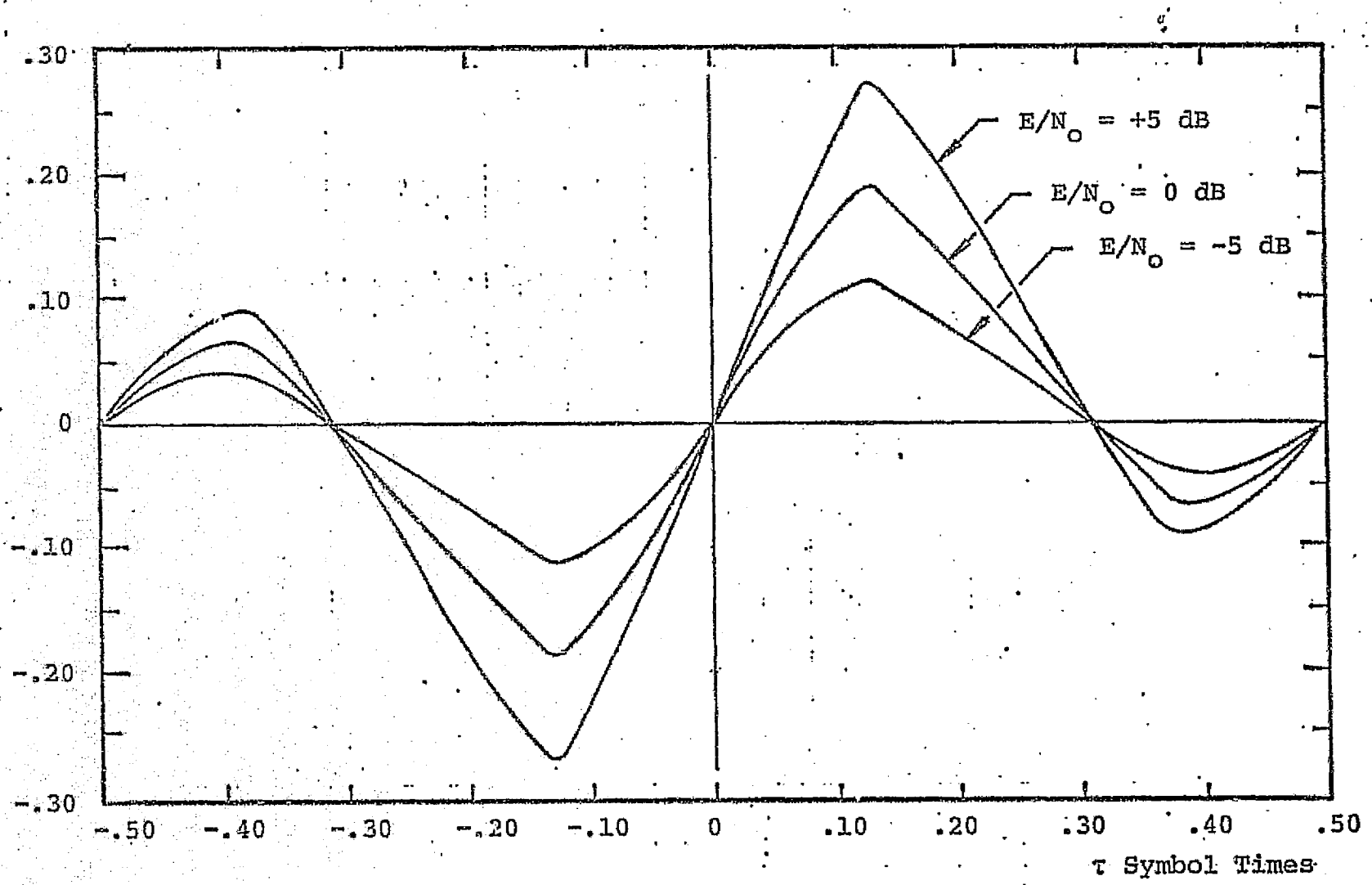

Figure 3.4 - g(τ), Detector Characteristics (S-curves) for Type A Detector (δ=1/8, a=1/2)

Also of considerable importance in bit synchronizer operation is the possible ambiguity at timing errors equal to half a bit time ($\tau = \pm 1/2$). As can be seen in Figure 3.4 - $g(\tau)$ has a positive slope at $\tau = \pm 1/2$ as well as at $\tau = 0$. Thus there is a stable (ambiguous) lock-point at a half-bit error. Resolution of this two-way ambiguity, and implementation of a half-bit shift when the wrong lock point has been achieved, requires separate detection (using the bit detector, X output or possibly the decoder metric) and will be discussed in Section 3.6. The shape of the normalized variance $h(\tau)$ will depend less strongly on τ, especially at low E/N_o ratios.

The probability density function of the relative timing error $\pi(\tau)$, as given by eq. (3.1) is plotted in Figure 3.5 for Type A loops at $E/N_o = -5$ dB, 0 dB, and +5 dB, $\delta = 1/8$, and $a = 1/2$. The most important result is, of course, the resulting bit error probability with the bit synchronizer loops used. For uncoded operation, this is shown in Appendix I to be

$$\overline{P_B}\,(E/N_o) = \int_0^{\frac{1}{2}} \left\{ Q\,[\sqrt{2E/N_o}\,(1-2\tau] + Q\,[\sqrt{2E/N_o}\,(1-4\tau)] \right\} \pi(\tau)\,d\tau \tag{3.3}$$

where $\Pi(\tau)$ is given by eq. 3.1 and plotted in Figure 3.5. The result of this integration is given in Figure 3.6 for various choices of $B_L T$ and compared with the ideal bit error probability for uncoded operation.

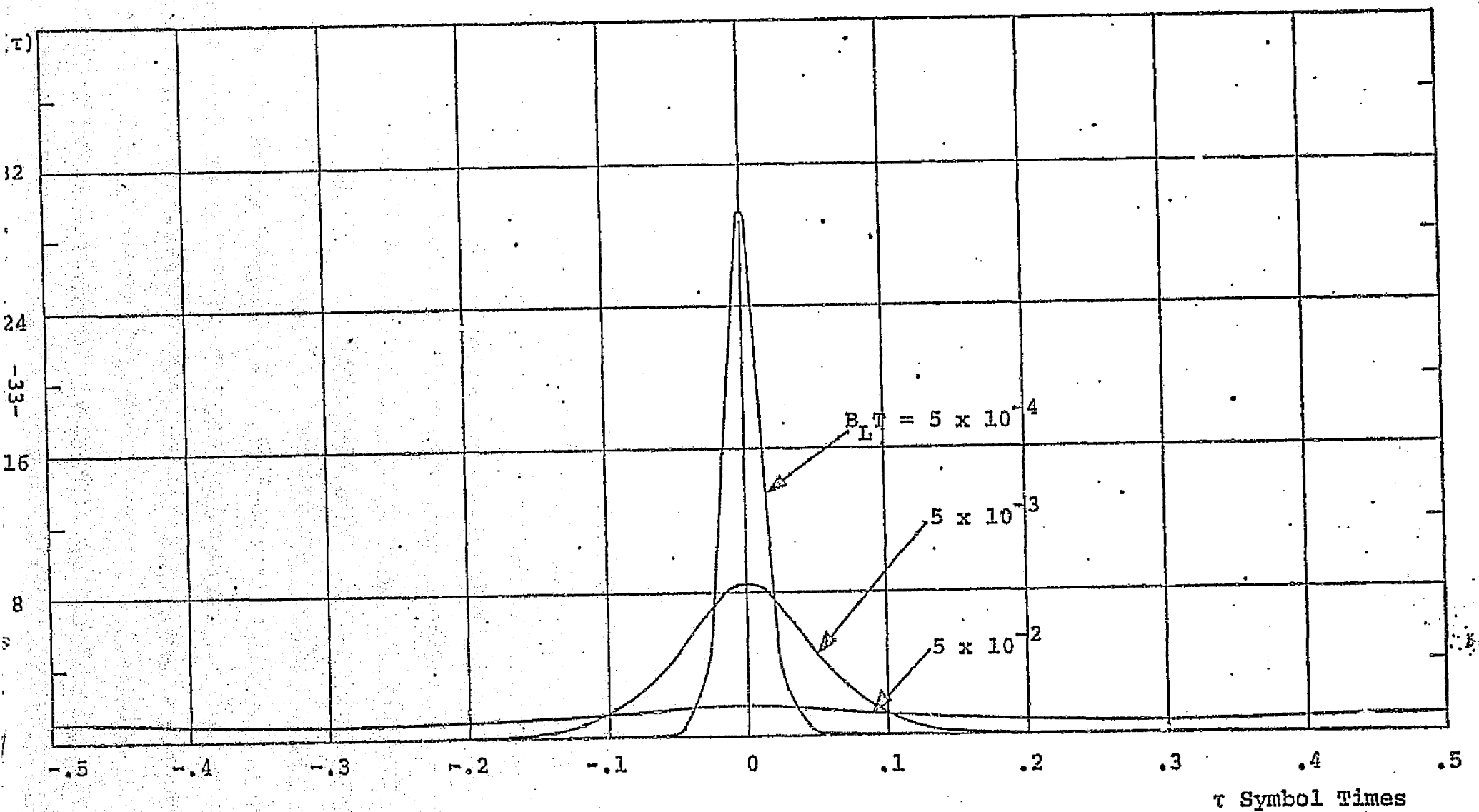

Figure 3.5 Probability Density for Type A - Detector Loop
(δ=1/8, a=1/2, E/N_o=-5 dB)

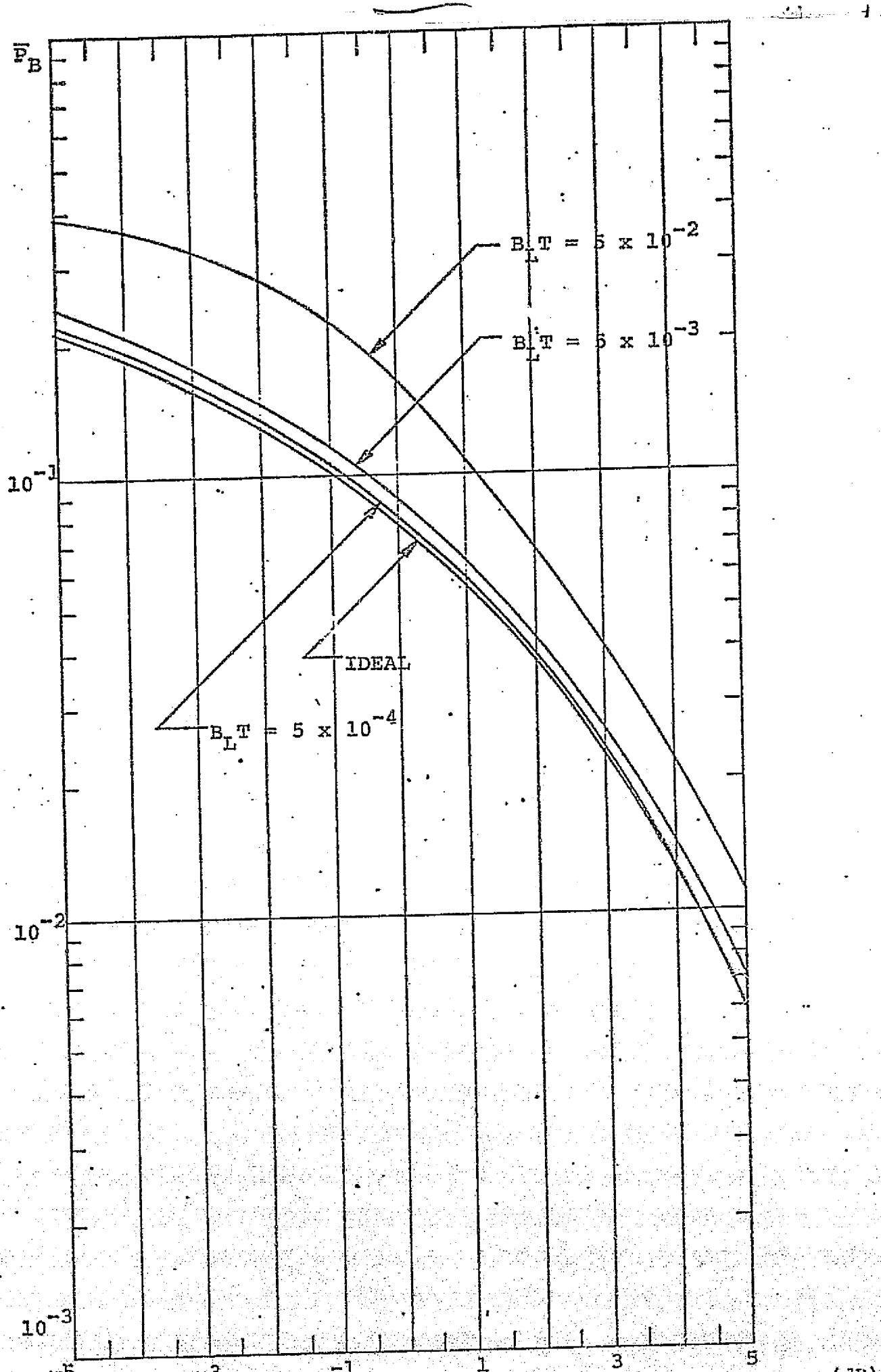

Figure 3.6. $\overline{P}_B$ for Type A Loop (δ=1/8, a=1/2) - Uncoded

It appears from the results of Figure 3.6 that a loop bandwidth* of $B_L = 108$ Hz ($B_L T = 5 \times 10^{-4}$) will maintain the tracking error due to noise sufficiently small that the bit error probability curve is within 0.2 dB of ideal. Thus there appears to be no reason to use a loop bandwidth which is much smaller than 100 Hz. This is encouraging because it enhances the loop's capability to acquire and track doppler rates, as will be discussed in Section 3.5. Of course, these conclusions are based on uncoded operation only. Coded operation is treated in Section 3.6.

Types C and D loops could be analyzed using techniques similar to those employed by Simon (Ref. 3.3) who analyzed a NRZ-L synchronizer employing an edge gate similar to Y_2 of Figure 3.3. However, it appears that dependancies among successive bits may require some minor simplifying assumption to obtain analytical results.

Further confidence in these results was obtained by simulation of loops with both Type A and Type B loops. In addition, the simulations afford the capability to assess the effects of

(a) quantization by the input A/D converter,

*Loop bandwidth values are based on a bit rate of 216 Kbps.

(b) performance of a convolutionally coded system employing rate 1/3, K = 7, Viterbi decoding*,

(c) acquisition performance with a fixed doppler offset.

The results of the simulations are discussed in Section 3.4.

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*Successive timing errors are statistically dependent because of the "sluggishness" of a narrow-band loop. This does not effect the uncoded error probability exact analysis, but it precludes the analysis of coded error probability, without questionable simplifying (independence) assumptions. Thus simulation in conjunction with a bit synchronizer loop is essential for assessing the degradation of timing-errors on coded operation.

3.2 Functional Design of a Bit Synchronizer

The various timing-error detectors and the corresponding bit synchronizer loops, discussed and analyzed in the last section, suggest the possibility of a flexible functional design which can accomodate essentially all the types of BIØ-L timing-error detectors considered, and even timing-error detectors for NRZ-L modulation. Figure 3.7 gives the functional block diagram of such a flexible or multi-mode bit synchronizer.

The key to a flexible, yet cost-effective, design is to recognize that the basic building block of all bit synchronizers under consideration is the gate pulse half-width Δ (Figure 3.2 and 3.3). This suggests an integrate-and-dump (I & D) circuit with integration time Δ. If, in addition, Δ is made equal to 1/n-th of the bit time, where n is an even integer, then the bit detector output consists merely of the sum of the first n/2 I & D outputs minus the sum of the last n/2 outputs over one bit time. All gate options (Y, Y_1, and Y_2) of all 4 types of error detectors of Figure 3.2 and 3.3 can be obtained as the sum and difference of some subset of the I & D samples. In addition, even an NRZ-L mechanization is possible with appropriate combinations of the I & D samples.

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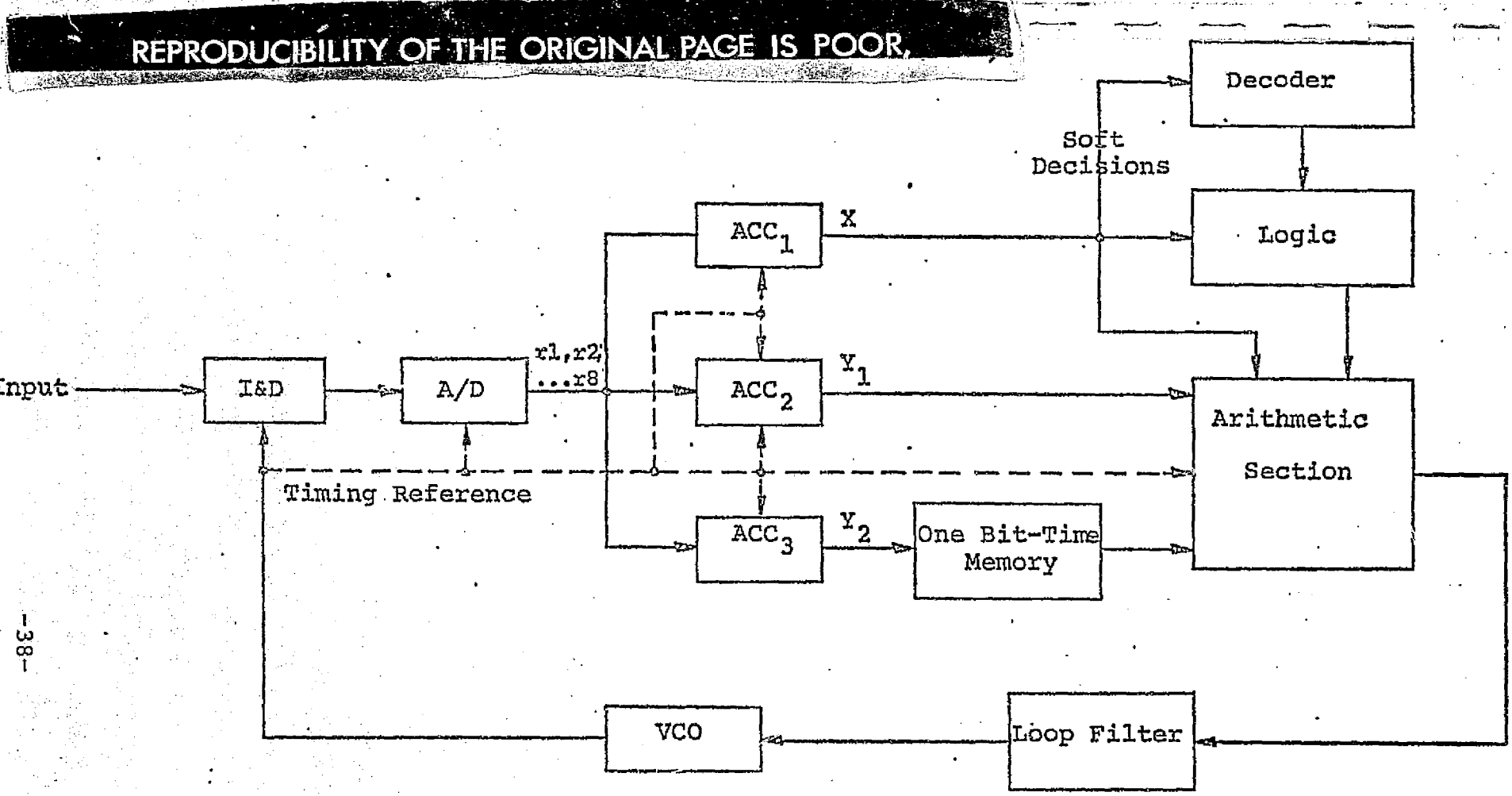

Error Detector Characteristics ($\Delta/T = 1/8$)

	BIϕ-L Types A, B	BIϕ-L Types C, D	NRZ-L Data Transition Loop
X	$\sum_{i=1}^{4} r_i - \sum_{i=5}^{8} r_i$	$\sum_{i=1}^{4} r_i + \sum_{i=5}^{8} r_i$	$\sum_{i=1}^{8} r_i$
Y_1	$r_4 + r_5 - a(r_1 + r_8)$	$r_4 + r_5$	——
Y_2	——	$-a(r_8' + r_1)$	$r_8' + r_1$
ARITHMETIC SECTION	(sgn X) · Y or X · Y	(sgn X) · ($Y_1 + Y_2'$) or X($Y_1 + Y_2'$)	sgn X · Y_2' or X · Y_2'

Note: Prime indicates a one symbol delay.

Figure 3.7 Functional Block Diagram of Multi-Mode Bit Synchronization Loop

The functional block diagram of Figure 3.7 demonstrates these capabilities. For the sake of a specific example, Δ is taken to be one-eighth of a bit time.* After the A/D converter up to three accumulators will be employed (Types A and B require only 2). The first accumulator ACC_1 is the bit detector in each case. The second accumulator ACC_2 implements the mid-bit gate and the edge gate in types A and B. The third accumulator ACC_3 implements the edge gate in types C and D error detectors and requires a membory over one bit time, which can be implemented using a single 5-bit register. The arithmetic section then combines the outputs of the accumulators under the control of logic controlled by ACC_1 and a possible mode-select switch which can select among the various types of bit synchronizers. The table in the left corner of Figure 3.7 indicates the operations of each accumulator and the arithmetic section for $T/\Delta = 8$. Modification for other even integer values of T/Δ is obvious. Multiplication (for types B and D) can best be performed using a read-only memory ROM. The loop filter can be either digital, employing an accumulator and a scaler, for a second order loop, or analog. The VCO can also be either digital, employing an accumulator and a crystal-controlled clock, or analog.

*This appears to be the best choice from the viewpoint of predetection bandwidth and flexibility.

One interesting possibility merits consideration, given that the bit synchronizer will be employed with a decoder. Especially at very low input SNR the symbol error probability will be very high and the resulting error detector outputs will tend to be very noisy. It is then possible to utilize a more reliable decision by using the decoder output. To assess the value of this appraoch, note that at $E/N_o = -2dB$, the uncoded bit error rate is .13 while with coding this reduces to 3×10^{-4}. Even at the extremely low value of $E/N_o = -5$ dB, coding improves the error probability slightly. To use the bit decisions out of the decoder in place of the output of ACC_1 is relatively straightforward. All that is required is a rate 1/3 convolutional encoder which converts the bit decisions back into symbols, which are input to the logic section in place of the output of ACC_1. However, the decoder introduces a delay of about 30 bit times or 90 symbol times. This delay of itself may hamper the loop acquisition. More serious is the fact that the outputs of the accumulators (ACC_2 and ACC_3) would have to be delayed by an equivalent time; this would require a memory of 90 symbols (which, assuming 5 bits of quantization per symbol) would require storage of 450 bits for each accumulator. An alternative, which avoids both delay and storage, is to use the state corresponding to the largest metric at the given time as an input to the encoder. This will be more likely to be in error than the delayed bit decision, but it

will still be far better than the noisy symbol decision out of ACC_1. The metric itself can also be used in a soft decision mode (as in types B and D error detectors). The problem of possible burst errors out of the decoder is not expected to be more serious than the potential delay with decoded bit decisions. This approach was not pursued in detail because of the positive simulation results (Section 3.4) without this decoder-aided feature.

3.3 Loop Parameters and Tracking and Acquisition Analysis

In this section, the degradation due to doppler offsets and rates is analyzed. These effects require, of course, the use of a second order loop. Thus, it is necessary first to establish the appropriate parameters of the loop filter in terms of the loop gain and bandwidth. This filter may be assumed to employ a nearly perfect integrator; if a digital mechanization is used, the integrator is replaced by an accumulator which is indeed perfect. Without the loop filter the bandwidth (of a first order loop) is (Ref. 3.5)

$$B_L = (AK)/4 \text{ Hz}$$

where A is the input signal voltage (in the absence of noise) and K is the product of all the loop gains normalized to a symbol period. Thus, if T is the bit period, KT has the dimensions of sec/volt.

If the (analog) loop filter for the second order loop has transfer function $1 + \alpha/s$ (proportional plus integral scaled by α), then the loop bandwidth becomes (Ref. 3.5)

$$B_L = (AK+\alpha)/4$$

In terms of damping factor ζ, the ratio of second order integrator scale factor to the loop gain is

$$\alpha/(AK) = 1/(4\zeta^2)$$

As a reasonable compromise between stability and speed of response let $\zeta = 1/\sqrt{2} = .707$. Then the scale factor is

$$\alpha = AK/2$$

As a result, for a second order loop,

$$B_L = (3/8)\ AK$$

Potentially, the most detrimental effect is that of doppler rate. Based on linear loop theory, the steady-state error due to a doppler rate R is given by (Ref. 3.5).

$$\phi_{ss} = \frac{R}{\alpha AK} = \frac{9}{32}\ \frac{R}{B_L^{\ 2}}$$

If R is given in Hz/sec and B_L in Hz, then the dimensions of ϕ_{ss} are in fractions of a bit time (or $\phi_{ss}T$ is in seconds).

According to one study (Ref. 3.4), the worst expected doppler rate is 4.1 KHz/sec and the doppler offset is 55 KHz at the carrier frequency of 2.2 GHz. At a bit rate of 216 Kbps, these reduce to 0.4 Hz/sec rate and 5.5 Hz offset (Ref. 3.4). Then the steady state error for a second order loop is

$$\phi_{ss} = 0.11/B_L^{\ 2} \text{ symbol times}$$

For loop bandwidth $B_L \geq 100$ Hz this is entirely negligible. Even nonlinear effects are not expected to modify this conclusion substantially.

Doppler offset causes no bias in a second order loop with an ideal integrator in the loop filter. On the other hand, the acquisition time depends on the square of the initial offset. It has been shown (Ref.3.5) that in the absence of noise for a second order phase-locked loop, the acquisition time for any initial offset of Δf Hz is approximately*

$$T_{acq} \simeq \frac{(2\pi\Delta f)^2}{\alpha(AK)^2} = \frac{(2\pi)^2 27}{256} \frac{(\Delta f)^2}{B_L^3} \simeq 4 \frac{(\Delta f)^2}{B_L^3} \text{ sec.}$$

While the above mentioned study indicates an expected doppler offset of 5.5 Hz, other oscillator uncertainties may produce a larger frequency offset. With a maximum frequency offset of 5×10^{-4} bits/bit time which corresponds to 108 Hz at a bit rate of 216 Kbps and a loop bandwidth of the same order of magnitude, acquisition would seem to be only on the order of a few hundredths of a second. This holds only at very high SNR.

For low SNR, no analysis is available and the problem does not appear to be tractable by analysis, although some simulations have been described for NRZ-L loops (Ref. 3.8) Simulations were carried out with the Type A loop de-

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*For nonsinusoidal loops the constant may change somewhat but the basic dependence on $(\Delta f)^2/B_L^3$ will not.

scribed in Sections 3.3 and 3.4. The results of these simulations are described in Section 3.6.

3.4 Uncoded and Coded Bit Error Probability Performance Simulation

The system described in Section 3.3 was simulated on the LINKABIT computer facility. Most of the simulations were carried out with a Type A timing-error detector with mid-bit gate half-width $\Delta = 1/8$ and no edge detector. A second order loop was used throughout with several choices of loop bandwidth.

The bit error probabilities were measured for both uncoded and coded operation. The latter utilizes previously developed software for the rate 1/3, K = 7, Viterbi decoder. Each simulation run was sufficiently long to record at least a thousand errors for uncoded operation and on the order of one hundred error events (several hundred bit errors) for coded operation. Results for uncoded operation indicate that the simulation results are nearly the same as the theoretical results. Thus it appears from Figure 3.8 that a choice of $B_L T = 5 \times 10^{-4}$ is sufficient to achieve a performance within 0.5 dB of that of the ideal time reference case.

As already noted in Section 3.3, the only reliable method of evaluating the degradation due to bit synchronizer inaccuracy in coded operation is by simulation. The results shown in Figure 3.9 indicate that synchronizer tracking inaccuracies, resulting from use of wider loop bandwidths, cause much more significant degradation in coded that in uncoded operation particularly at the lower error probabilities.

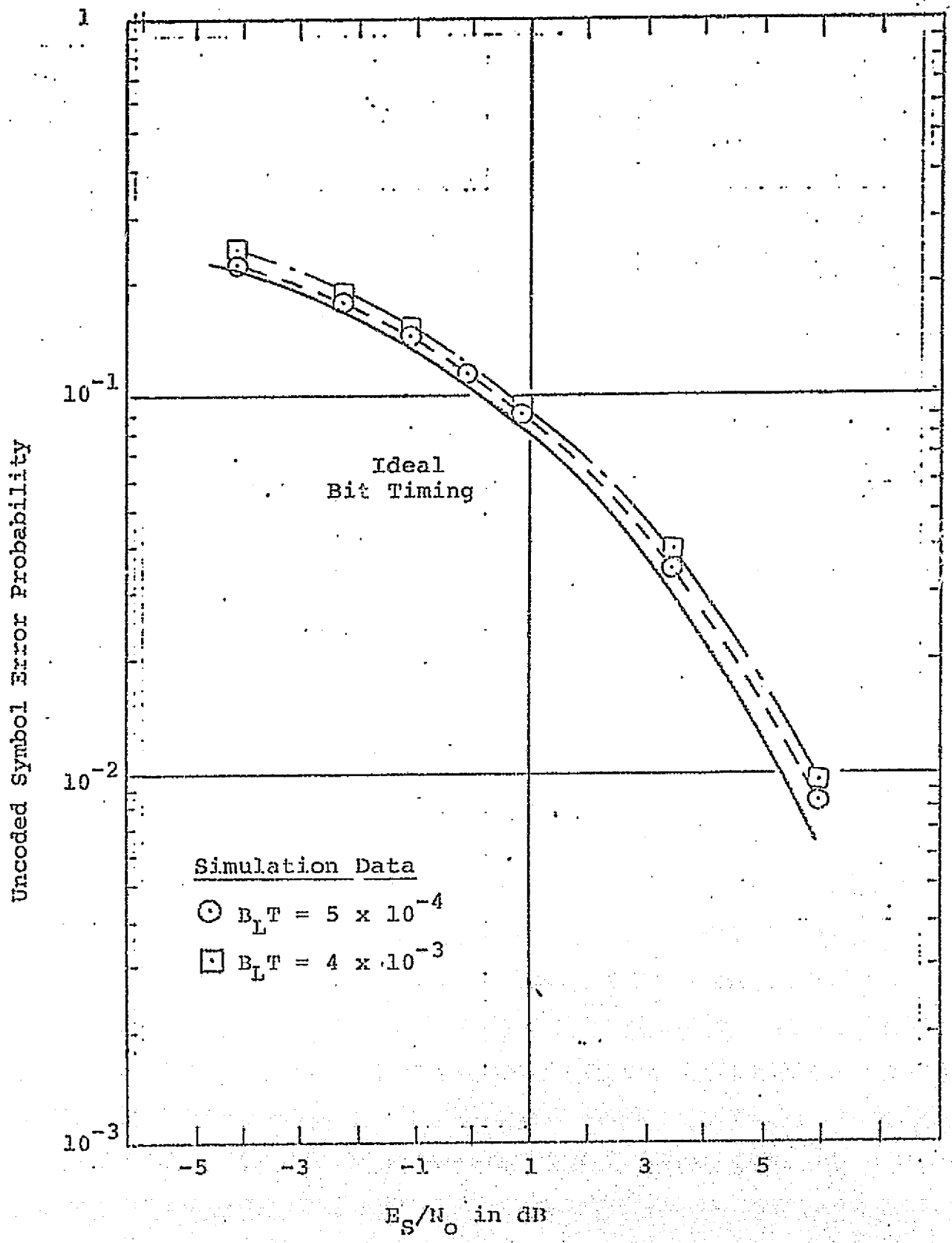

Figure 3.8 Uncoded Bit Tracking Simulation Data

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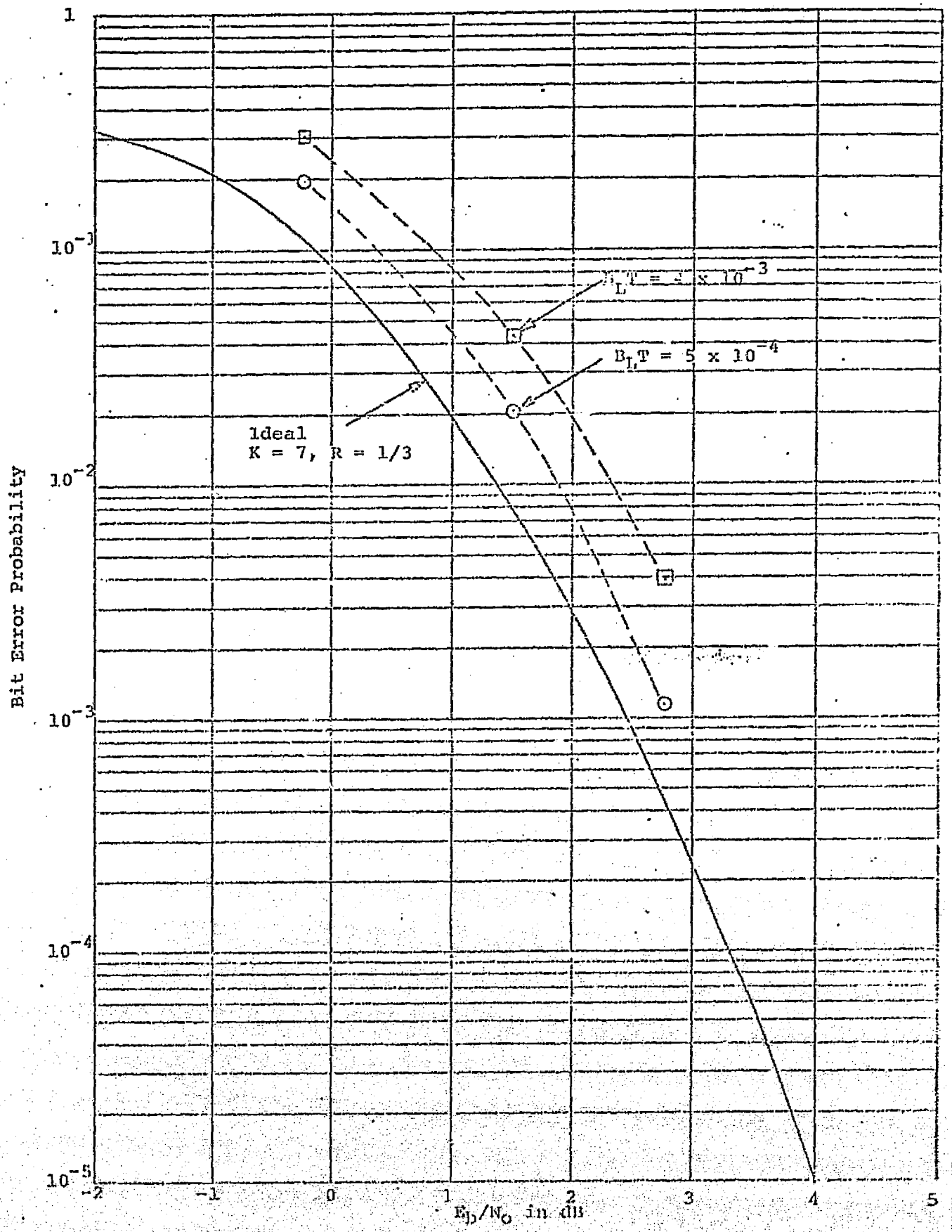

Figure 3.9 Coded Bit Tracking Simulation Data

3.5 Acquisition Simulation

As noted in Section 3.3, there are no theoretical results available for predicting acquisition time at very low SNR's. Thus, the basic simulation program for determining bit error rates was modified to introduce a frequency offset (timing-error ramp) in the noisy incoming signal. Results are shown in Table 3.1. These results indicate that at the threshold value of symbol $E/N_o = -5$ dB acquisition times became excessively long for offsets equal to or greater than the loop bandwidth. However, it was found that by using a wider loop bandwidth during acquisition (about an order of magnitude above the tracking bandwidth) the situation was markedly improved. As can be seen for the first entry in Table 3.1, with a loop bandwidth equal to 8 times the expected maximum frequency offset; i.e. $B_L T = 4 \times 10^{-3}$ for $(\Delta f)T = 5 \times 10^{-4}$ ($B_L = 864$ Hz for $\Delta f = 108$ Hz, with symbol rate 216 Kbps) the loop locks in a mean time of about 0.08 sec.

The second entry in Table 3.1 deals with a strategy of stepping the VCO over the region of uncertainty in 8 equal steps, using the same loop bandwidth as for a single step. Thus the maximum frequency uncertainty per step is 13.5 Hz. The total acquisition time with this strategy is about 8 times the single step time of Table 3.1, i.e., about 0.06 seconds.

Symbol E/N in dB	Δf in Hz	$(\Delta f)T$	B_L in Hz	$B_L T$	No. of Steps Required in Search	T_{ACQ} Mean in Seconds	T_{ACQ} Standard Deviation in Seconds	Number of Runs
-5	108	5×10^{-4}	864	4×10^{-3}	1	.0793	.0688	12
-5	13.5	6.25×10^{-5}	864	4×10^{-3}	8	.00784	.00206	8
7	216	10^{-3}	864	4×10^{-3}	1	.00634	———	1
30	216	10^{-3}	864	4×10^{-3}	1	.00218	———	1

Acquisition time (in symbol times) = number of symbol times from the start of acquisition until the first of $2^{12} = 4096$ consecutive symbol times during which the magnitude of the error is less than 1/8 symbol time.

Table 3.1 Bit Timing Acquisition Simulation Data for a 216 kbps Channel Data Rate.

In Section 4.3 it is shown that the carrier tracking loop VCO must be stepped over the region of carrier frequency uncertainty to acquire lock within a reasonable amount of time. Since Table 3.1 shows that the total bit timing acquisition time is approximately the same for the single or 8 step acquisition strategies, the problem of simultaneously stepping the carrier tracking and the bit timing VCO's is avoided by using the single step bit timing acquisition strategy in the combined carrier tracking and bit timing acquisition strategies.

3.6 Ambiguity, Lock Detection, False Lock, and Bit Slipping Rate

As is graphically evident from the timing-error gate characteristic curve of Figure 3.4, a BIϕ-L bit synchronizer has a stable lock point at the half-bit error point. This follows from the fact that the characteristic curve has a positive slope at timing errors of ± 0.5 of a bit time. This positive slope, smaller than that at zero-error, nevertheless will tend to force the loop to a stable lock at this point, whenever the timing error magnitude is greater than about 0.3 of one bit time. Of course, noise may easily force the loop out of this point and onto a stable lock at a bit period. But to guarantee that this two-way ambiguity will be avoided, an auxiliary device must be employed to detect the half-bit lock condition.

Fortunately, the same device which detects this condition can also be used to determine the correct locked condition. This can be accomplished by accumulating magnitudes (with sign deleted) of the bit detector outputs over a long enough period. This can best be done by accumulating the 3-bit soft decision outputs in an accumulator.

When the loop is locked at the bit period the accumulated value is proportional to the symbol energy-to-noise ratio times the number of symbol times accumulated.

When the loop is out of lock it will be much smaller. It is shown in Appendix III that the difference between the mean accumulated value over N symbols, when the loop is in lock and when it is out of lock is approximately

$$m_L - m_o \approx \sqrt{\frac{2}{\pi}} \left(\frac{2E_s}{N_o}\right) N \text{ for } E_s/N_o << 1$$

while the variance in either case is approximately

$$V_L \approx V_o = \left(1 - \frac{2}{\pi}\right) N$$

where the variance of the additive Gaussian noise is normalized to unity. With a threshold test to decide between the lock and out-of-lock conditions, the detectability is approximately

$$D = \frac{(m_L - m_o)^2}{V_o} \approx \frac{2/\pi}{1-2/\pi} \left(2\frac{E_s}{N_o}\right)^2 N$$

Thus at $E_s/N_o \approx -5$ dB with $N = 10{,}000$ (.05 sec. at the coded data rate), we have

$$10 \log_{10} D \approx 38 \text{ dB}$$

The false alarm and detection probabilities depend, of course, on the location of thresholds and the acquisition strategy. However, with such a high detectability, there appears to be no difficulty.

When the loop is locked to the mid-bit point and random data is being received, then the average value accumulated will be measurably less than that accumulated at the correct lock point, for the magnitude of the detector output will be proportional to the symbol energy whenever a transition occurs, but it will contain no signal energy (and respond only to noise) when a transition does not occur. For random data only half the inter-bit transitions occur. If only one-tenth the bits are ones (or zeros), then nine-tenths of the transitions occur.

Lock detection and ambiguity elimination can be accomplished by accumulating the difference between two bit detectors (displaced by a half-bit from each other) and comparing this difference with sufficiently high positive and negative thresholds. If, during acquisition, either threshold is crossed, a lock condition is declared (and the VCO stops searching). Depending on which threshold is crossed, one or the other bit detector is chosen for the correct position.

During tracking, the accumulator continues to be updated; however, it is prevented from overflowing. As long as the bit synchronizer remains locked, the accumulator will stay near this boundary most of the time. If the accumulator should decrease to zero, loss of lock is declared and search resumed.

When the bit synchronizer is operating on convolutionally coded data, the decoder can perform these functions more effectively than the bit synchronizer components. First of all, proper design of the code (Appendix II) can guarantee that the relative frequency of either ones or zeros is at least equal to 2/9. More important, the rate 1/3 Viterbi decoder normally must resolve a three-way ambiguity for bit (or branch) synchronization. Adding to this the two-way half-bit ambiguity will require the decoder to resolve a six-way rather than a three-way ambiguity. However, exactly the same technique can be used, which is based on frequency of metric normalization. Thus, both the lock indication and the half-bit indication can be taken over almost routinely by the decoder, and the time to establish these indications reliably is much shorter than when the synchronizer bit detector output magnitudes are used.

A related issue is the question of false lock to a sideband of the symbol period fundamental caused by a particular low frequency periodic symbol pattern. This is not expected to be a problem because the VCO crystal tuned at 216 KHz typically cannot be pulled over by more than 0.1% of its center frequency.

Finally, correct lock can be lost occasionally due to bit slippage. Again here, as can be seen from Fig. 3.4, if noise causes the loop to slip to a timing error above 0.3 symbol times, it may very well reach the stable half-bit

error point, or even slip a full bit. This event is exceedingly rare for loop parameter values of interest. For a phase-locked loop it can be shown (Reference 3.5) that the inverse mean cycle slip time (or average number of cycles slipped per unit time) is

$$\frac{1}{\overline{\tau}_{s\text{-}l}} = \frac{2B_L}{\pi^2 \alpha \, I_o^{\,2}(\alpha)} \simeq \frac{4B_L}{\pi} e^{-2\alpha}$$

Where

$$\alpha = \frac{1}{(2\pi\sigma)^2}$$ and σ is the standard deviation in

bit times. For the analytical results and simulations* obtained in Sections 3.3 and 3.4 where $\sigma < .01$, $\alpha > 250$ and $e^{-2\alpha}$ becomes absurdly small. While the timing error characteristic is certainly not sinusoidal here, the result is within the right order of magnitude. Note, in fact that even if α were reduced by an order of magnitude, the slip frequency would still be negligible. Notwithstanding this, some form of bit slip detector must be implemented in conjunction with the lock detector.

*Simulation results were based on several hundred thousand bit times during which time the bit slippage condition was never even approached.

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4.0 Carrier Tracking Loop Design, Interface, and Effects on Coded Performance

This section presents the investigation of the effects of the carrier tracking loop on overall system performance. Acquisition and coded error rate performance with nonideal bit synchronization are considered for Costas and decision-directed carrier tracking loops.

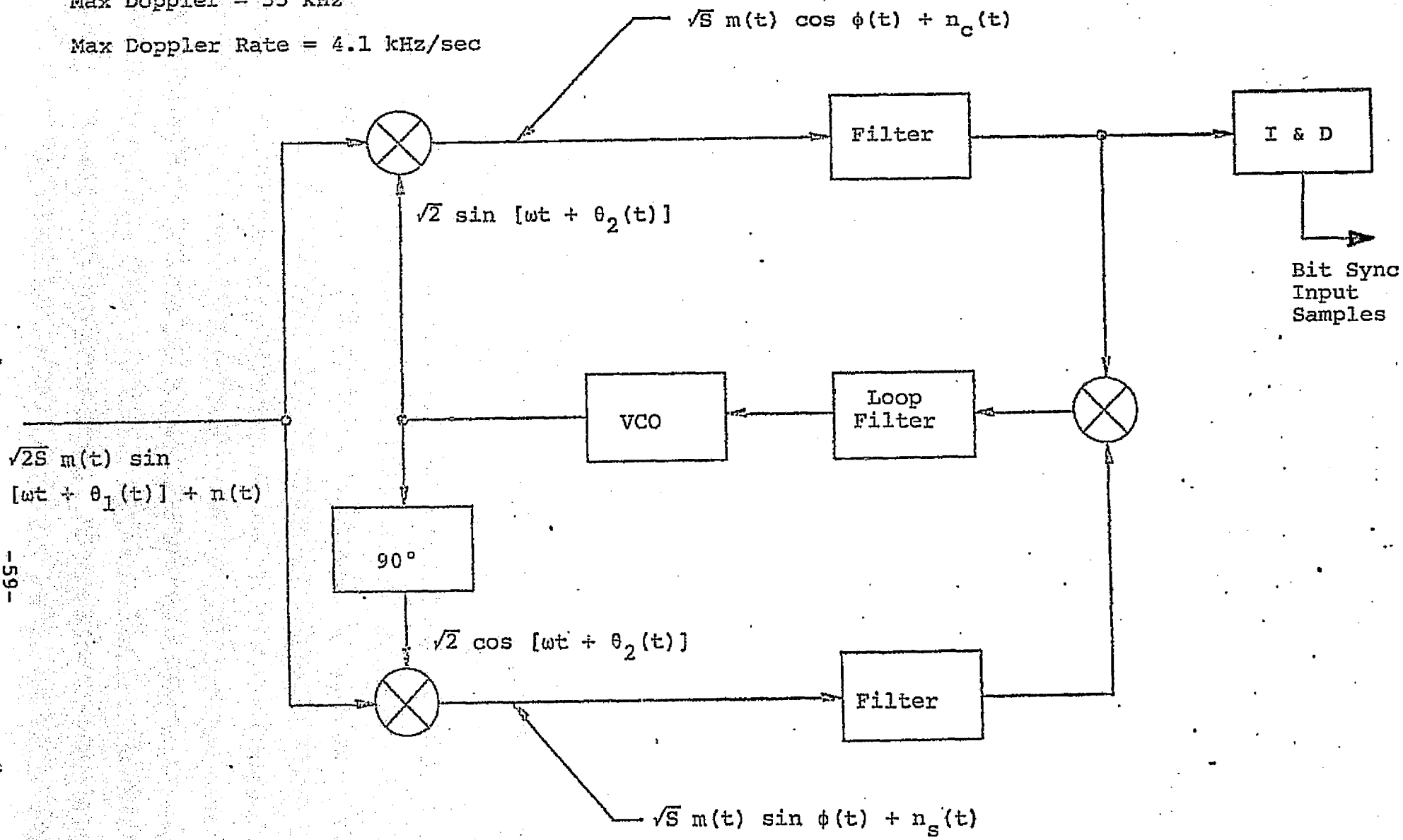
4.1 Loop Modeling

Figure 4.1 is the block diagram of a Costas tracking loop. m(t) represents the antipodal modulation, S is the signal power and n(t) is wideband Gaussian noise of one-sided power spectral density of N_o. $n_c(t)$ and $n_s(t)$ represent independent in-phase and quadrature noise components of one-sided spectral density N_o. The in-phase and quadrature channel filters have a bandwidth, W, as narrow as possible without significantly attenuating the signal. The output integrate-and-dump (I & D) is part of the bit synchronization system. For the system of Section 3, this integrates over 1/8 of a channel symbol time.

A mathematical model of the Costas loop of Figure 4.1 is given in Figure 4.2. The I & D circuit following the cosine channel filter suggests the possibility of combining the two. For example, the in-phase and quadrature

Max Doppler = 55 kHz

Max Doppler Rate = 4.1 kHz/sec



$\phi(t) = \theta_1(t) - \theta_2(t)$

Figure 4.1 Costas Loop Block Diagram

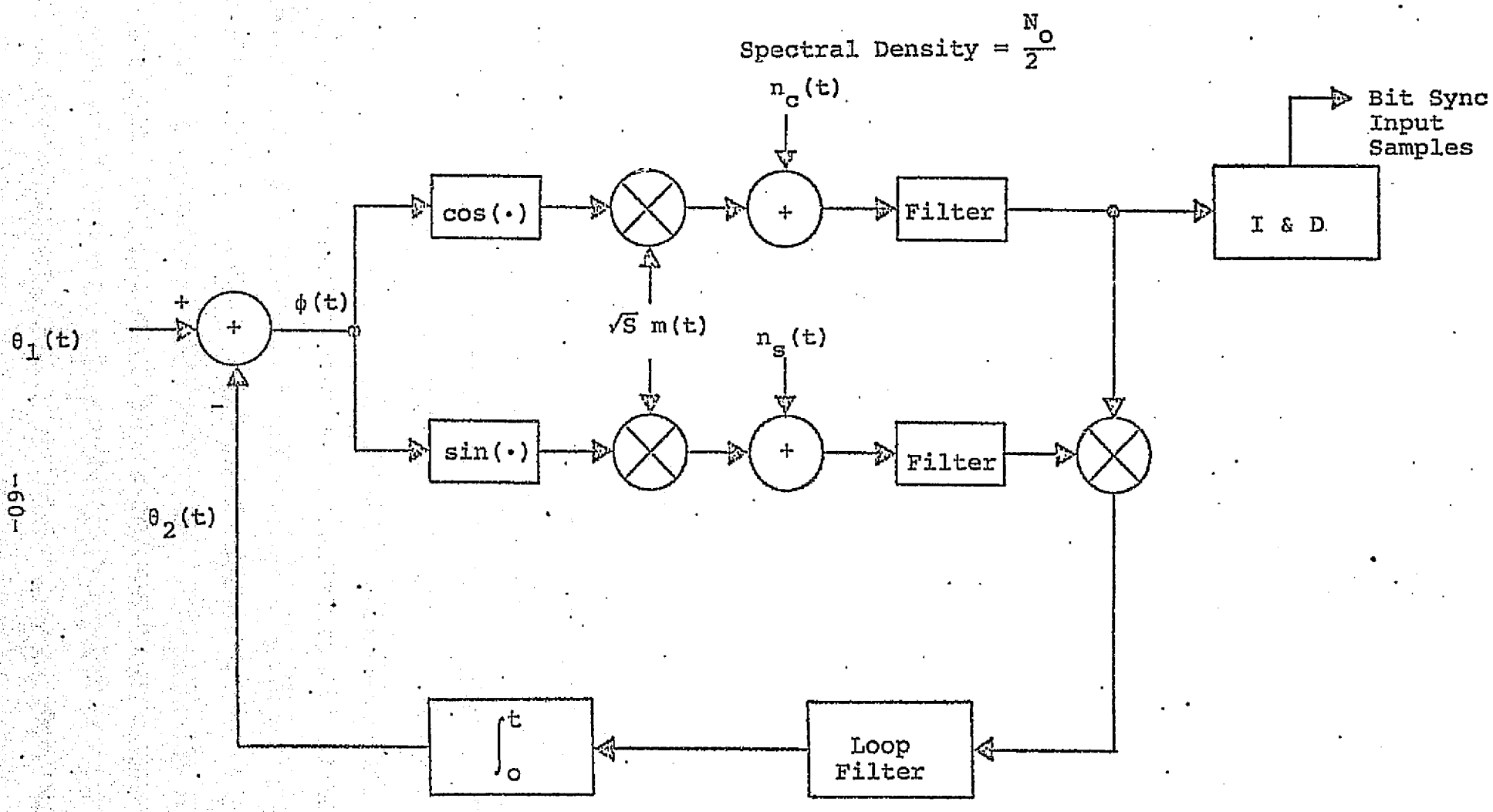


Figure 4.2 Costas Loop Model

channel filters could be replaced by I & D circuits like that used at the input to the bit synchronization system. However, the bit synchronizer input I & D only integrates over 1/8 of a channel symbol time. Thus its noise bandwidth is $4/T_s$ where T_s is the channel symbol time. This is a much wider bandwidth than is required. Narrower bandwidth filters can be simulated by replacing these filters by I & D circuits over 1/8 of a channel symbol time followed by digital filters as shown in Figure 4.3a. This is a fairly accurate approximation to the case of analog passive filters. Alternately, by combining the 8 I & D outputs per channel symbol, a filter matched to the BIϕ-L input signal may be realized as shown in Figure 4.3b. Simulation data has been obtained using both of these approaches.

To track a doppler rate with a small steady state error, a second-order loop with a large loop gain is needed. Let the loop filter transfer function be

$$F(S) = K(1 + \frac{a}{S}) \tag{4.1}$$

The digital equivalent of the second-order Costas loop with in-phase and quadrature channel matched filters is given in Figure 4.4.

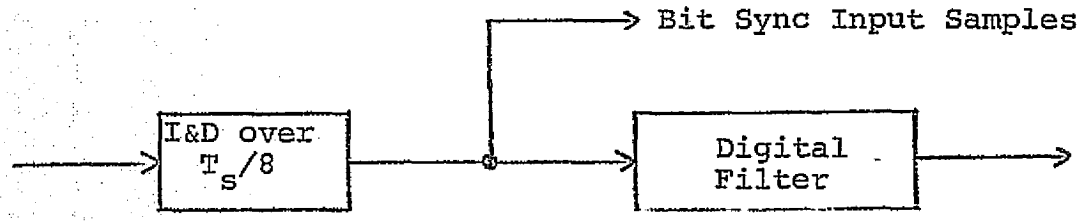


Figure 4.3a Digital Filter Model for I Channel Filter (Passive Filter Approximation)

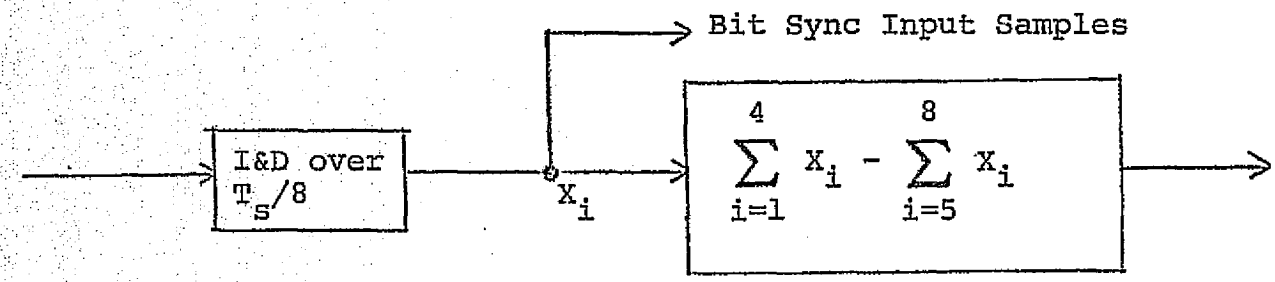
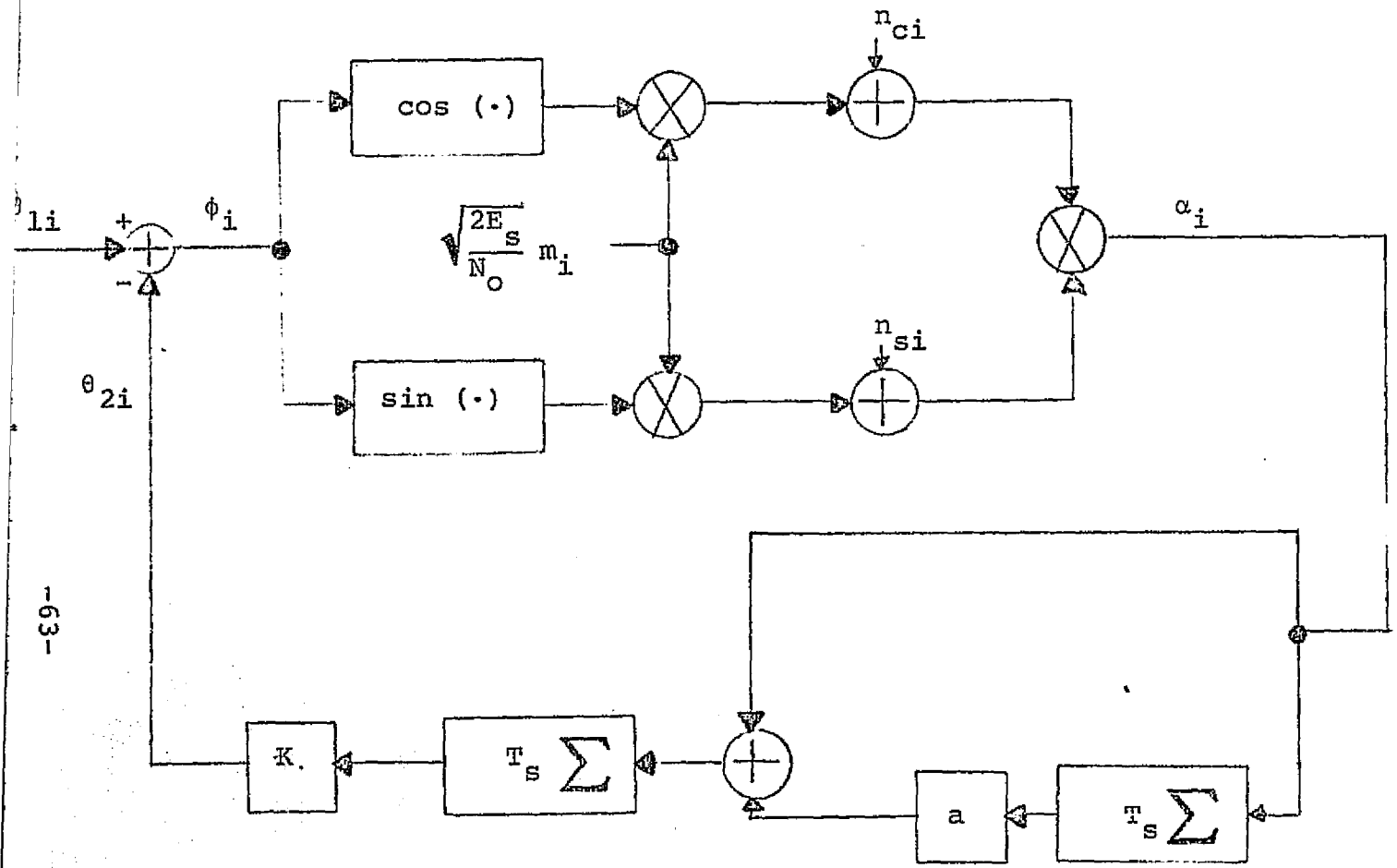


Figure 4.3b Matched Filter Model for I Channel Filter



n_{ci} and n_{si} are independent zero mean, variance = 1 Gaussian random variables.

Figure 4.4 Digital Model of a Second Order Costas Loop with In-Phase and Quadrature Channel Matched Filters

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR.

Before proceeding to simulation results of this nonlinear system, it is helpful to consider the linearized model of this loop. This model can be used to obtain coarse estimates of some of the loop parameters. To obtain the linearized model, first replace the in-phase and quadrature channels and the multiplier portion of the loop by the equivalent form of Figure 4.5 where N

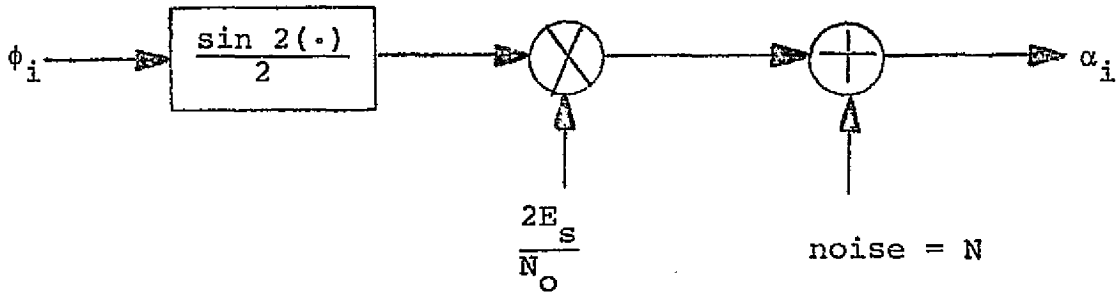
$$N = \sqrt{\frac{2E_s}{N_o}}\ m_i\ [n_{ci} \sin \phi_i + n_{si} \cos \phi_i] + n_{ci} n_{si} \qquad (4.2)$$

is a noise term with zero mean and variance

$$\sigma_N^2 = \frac{2E_s}{N_o} + 1 \qquad (4.3)$$

Assuming small phase errors and a small loop bandwidth, produces the linearized model of Figure 4.6. This model is now in the form of a linear digital phase-locked loop. A linear analysis of such a system is given in Appendix IV. In this appendix the inverse of the phase error variance is shown to be

$$\alpha = \frac{1}{\sigma_\phi^2} = \frac{E_s/N_o}{B_L T_s} \quad \frac{1}{1 + \frac{N_o}{2E_s}} \qquad (4.4)$$



$$N = \sqrt{\frac{2E_s}{N_o}}\, m_i \, [n_{ci} \sin \phi_i + n_{si} \cos \phi_i] + n_{ci}\, m_{si}$$

Figure 4.5 Model for the Error Detector Part of the Costas Loop

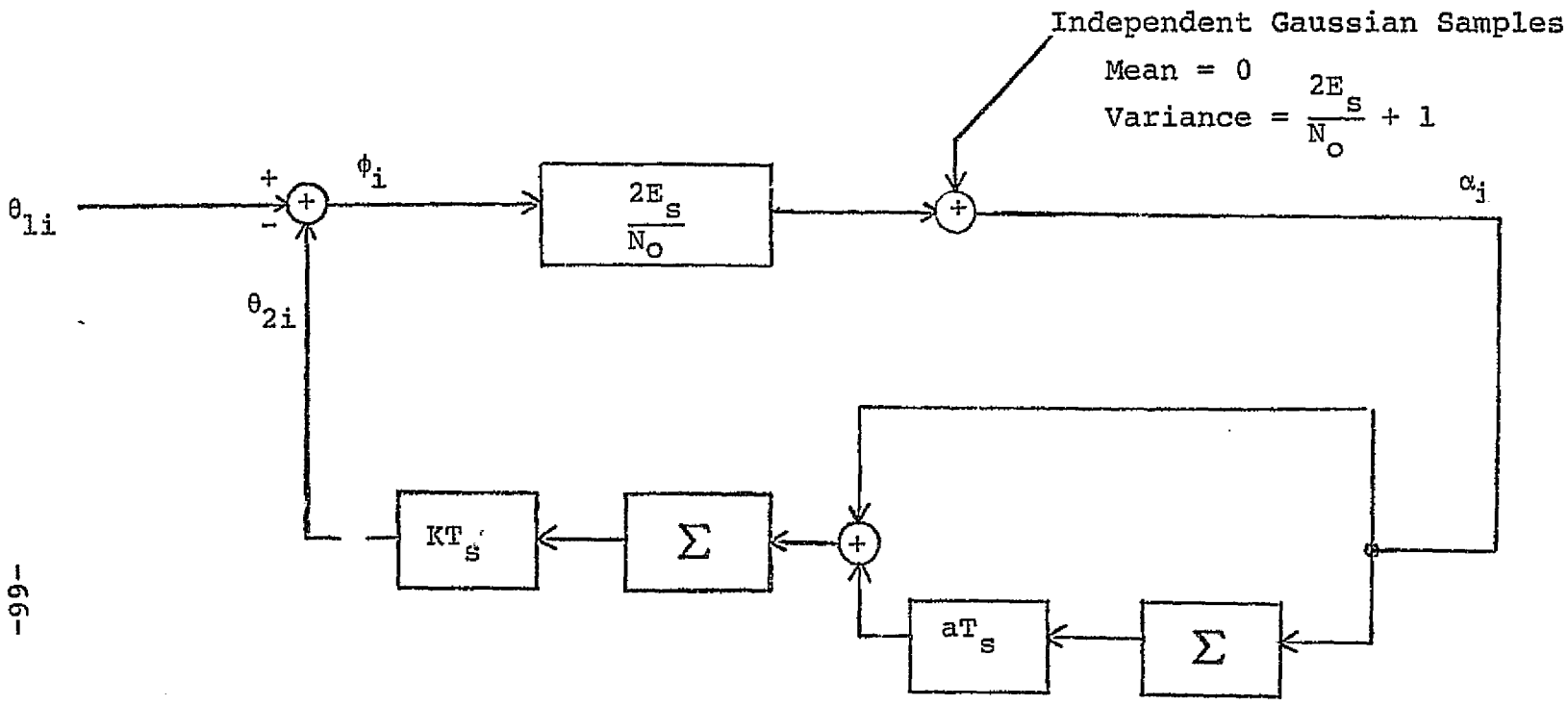


Figure 4.6 Linearized Model of Costas Loop

where

$$B_L = \frac{1}{4} \left\{ \left(\frac{2E_s}{N_o} \right) K + a \right\} \tag{4.5}$$

The decision-directed tracking loop considered is similar to the Costas loop, the only difference being that a limiter is added at the cosine channel multiplier input (see Figure 4.7). In the absence of noise this multiplier input now just removes the signal modulation. The error detector can be modelled as shown in Figure 4.8 where

$$N = \gamma_i \, n_{si} \tag{4.6}$$

is a noise term, γ_i is a random variable

$$\gamma_i = \begin{cases} +1 & \text{if modulation removed correctly} \\ -1 & \text{otherwise} \end{cases} \tag{4.7}$$

and

$$P_{+i} = \Pr \{\gamma_i = 1\} \tag{4.8}$$

$$P_{-i} = \Pr \{\gamma_i = -1\} \tag{4.9}$$

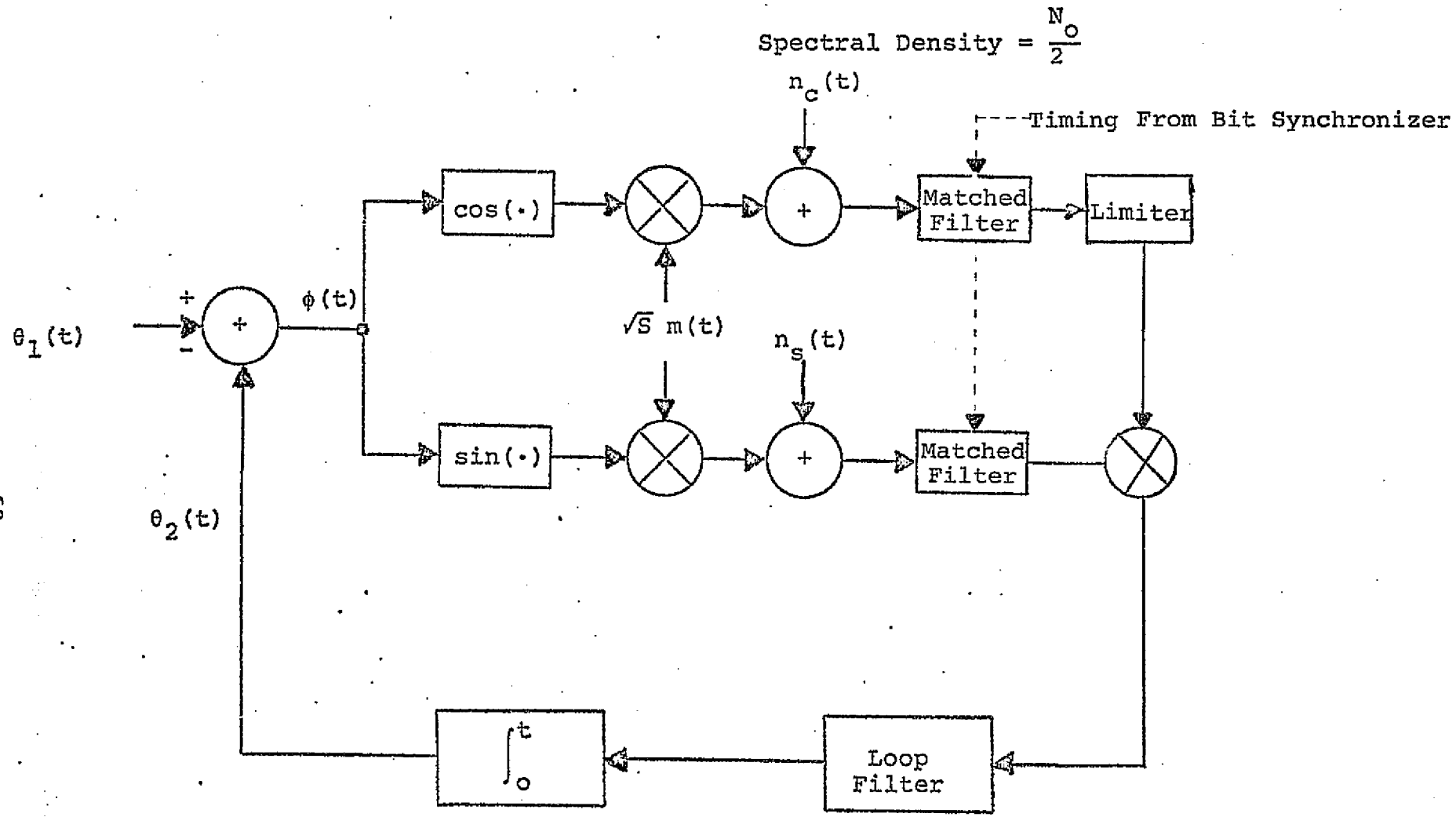
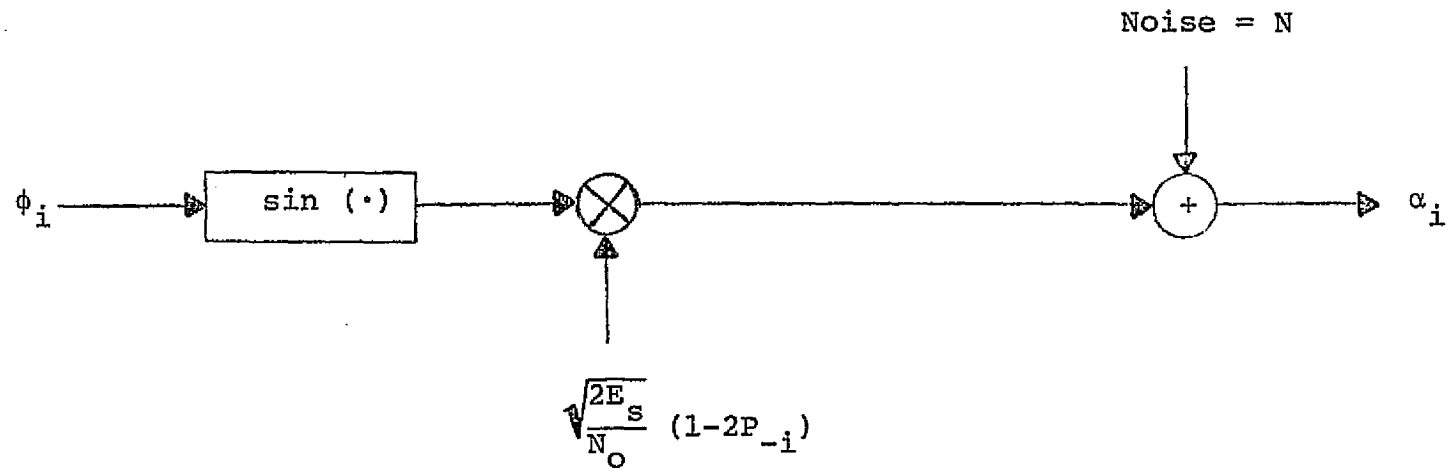


Figure 4.7 Decision-Directed Loop Model



$N = \gamma_i\, n_{si}$, Var $N = 1$

$$\gamma_i = \begin{cases} +1 & \text{if modulation removed correctly} \\ -1 & \text{otherwise} \end{cases}$$

$P_{-i} = \Pr\{\gamma_i = -1\}$

Figure 4.8 Model for the Error Detector Part of the Decision-Directed Loop

The noise term has zero mean and its variance is equal to the variance of n_{si}.

For small phase errors and narrow loop bandwidths

$$P_{-i} = Q\left\{\sqrt{\frac{2E_s}{N_o}} \cos \phi_i\right\} \approx Q\left(\sqrt{\frac{2E_s}{N_o}}\right) \tag{4.10}$$

where

$$Q(x) = \int_x^\infty \frac{1}{\sqrt{2\pi}} \exp\left(-\frac{\alpha^2}{2}\right) d\alpha \tag{4.11}$$

and the linear model of Figure 4.9 results. The phase error variance can be obtained using the results of Appendix IV.

Table 4.1 summarizes the linearized performance of the Costas and decision-directed loops. This table also gives the corresponding quantities for all analog loops. These quantities can be obtained by arguments similar to those just given for the loops with the matched filters. The bandwidth W of analog loop filters are assumed not to significantly attenuate the signal. The table entries for the digital filter model of the in-phase and quadrature channel filters can be obtained from the analog loop entries with W equal to the noise bandwidth of the digital filters.

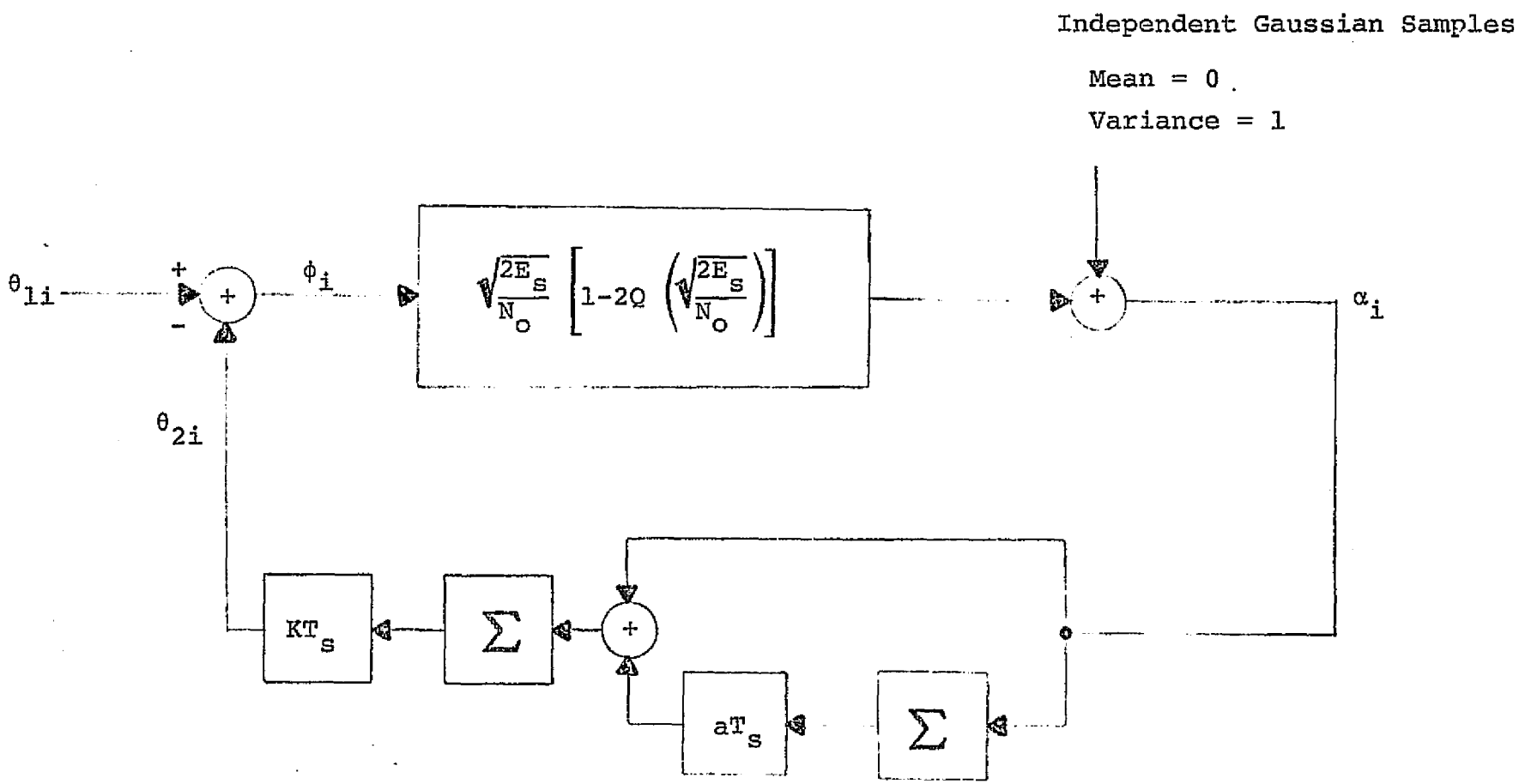


Figure 4.9 Linearized Model of Decision-Directed Loop

Type of Loop	$\alpha = \frac{1}{\sigma_\phi^2}$	P
Costas With Matched Filters	$\frac{E_s/N_o}{B_L T_s} \frac{1}{1 + \frac{N_o}{2E_s}}$	$\frac{2E_s}{N_o}$
Analog Costas	$\frac{E_s/N_o}{B_L T_s} \frac{1}{1 + WT_s\left(\frac{N_o}{E_s}\right)}$	$\frac{2E_s}{N_o}$
Decision-Directed With Matched Filters	$\frac{E_s/N_o}{B_L T_s} \left\{1-2Q\left(\sqrt{\frac{2E_s}{N_o}}\right)\right\}^2$	$\sqrt{\frac{2E_s}{N_o}} \left\{1-2Q\left(\sqrt{\frac{2E_s}{N_o}}\right)\right\}$
Analog Decision-Directed	$\frac{E_s/N_o}{B_L T_s} \left\{1-2Q\left(\sqrt{\frac{E_s}{N_o} \frac{1}{WT_s}}\right)\right\}^2$	$\sqrt{\frac{2E_s}{N_o}} \left\{1-2Q\left(\sqrt{\frac{2E_s}{N_o}}\right)\right\}$

$$B_L = \frac{PK + a}{4}$$

$$\zeta = \sqrt{\frac{PK}{4a}}$$

Table 4.1 Summary of Linearized Carrier Loop Performance

For all of the types of loops summarized in Table 4.1, the damping coefficient, loop bandwidth, and steady state phase error due to a doppler rate of R_{dop} Hz/sec are

$$\zeta = \sqrt{\frac{PK}{4a}} \tag{4.12}$$

$$B_L = \frac{PK + a}{4} \tag{4.13}$$

and

$$E_{ss} = \frac{2\pi\ R_{dop}}{aKP} = 2\pi \left(\frac{4\zeta^2 + 1}{8\zeta}\right)^2 \frac{R_{dop}}{B_L^2} \text{ radians} \tag{4.14}$$

respectively. In all of the simulations which follow, the damping coefficient was set at $1/\sqrt{2}$. For this damping coefficient and a doppler rate of 4.1 kHz/sec the steady state phase error is

$$E_{ss} = \frac{7240}{B_L^2} \text{ radians} \tag{4.15}$$

4.2 Carrier Tracking Performance

4.2.1 Phase Ambiguity Resolution

The carrier tracking loops described in the previous section all have stable operating points every 180 degrees. So the bit synchronizer input samples could have the wrong polarity. This phase ambiguity can be resolved by using differential encoding with a transparent convolutional code or by using a nontransparent code and changing the polarity of the input samples when the Viterbi decoder metrics sense that the polarity is wrong. Both of these techniques have been employed in LINKABIT decoder implementations.

With the first method, differential encoding is employed before encoding with a transparent convolutional code. Transparent convolutional codes have the property that the bit-by-bit complement of a code word is also a code word. Such a code must have an odd number of taps on each of its mod-2 adders. Then if a data sequence generates a certain code word, its complement will generate the complementary code word. Five of the 17 different non-catastrophic $K = 7$, $R = 1/3$ convolutional codes with the maximum free distance of 15 are transparent (Ref. 4.11). The polarity inversion is finally corrected by only considering bit transitions out of the Viterbi decoder. Differential

encoding does cause a small degradation in the bit error probability performance. For example, an isolated bit error would cause two differential encoding bit errors. However, since Viterbi-decoding errors usually occur in bursts, differential encoding increases the bit error probability by considerably less than a factor of two.

With the second method, a nontransparent convolutional code is used. Then if the polarity is wrong, the resulting word does not correspond to a valid code word. Thus the Viterbi decoder metrics will not increase as fast as when the polarity is correct. The metrics can easily be monitored to detect this condition. This method avoids the small differential encoding degradation of the other method. The encoder/decoder which is described in Section 2 and which was used to obtain the simulation data of this report uses this method.

4.2.2 Theoretical Carrier Tracking Performance

A constant phase error of ϕ will degrade the received energy-to-noise ratio by $\cos^2 \phi$ (Ref. 4.2). Since the phase error is being tracked in the presence of noise, the phase error will be a function of time. However, when the data rate is much larger than the carrier loop bandwidth, which is the case for this application, the phase error will not vary

significantly over many bit times. The Viterbi decoder output errors will occur in bursts, but at bit error probabilities in the range of interest, the bursts are very rarely longer than a few constraint lengths. So assume that the phase error is constant over the length of most error bursts. Then the mean error probability is

$$\overline{P_E} = \int_{-\pi}^{\pi} p(\phi) P_E \left(\frac{E_b}{N_o} \cos^2 \phi\right) d\phi \tag{4.16}$$

where $p(\phi)$ is the probability density function of the phase error and $P_E(E_b/N_o)$ is an expression for the zero phase error, bit error probability curve. For a first-order and to a good approximation also for a second-order loop the phase error density function is (Ref. 4.3).

$$p(\phi) = \frac{e^{\alpha \cos \phi}}{2\pi I_o(\alpha)}, \qquad \alpha >> 1 \tag{4.17}$$

where α is the loop signal-to-noise ratio of Table 4.1. Substituting (4.17) into (4.16) and performing the integration yields the average error probability. The results are shown in Figure 4.10 for a K = 7, R = 1/3 system with ideal bit timing.

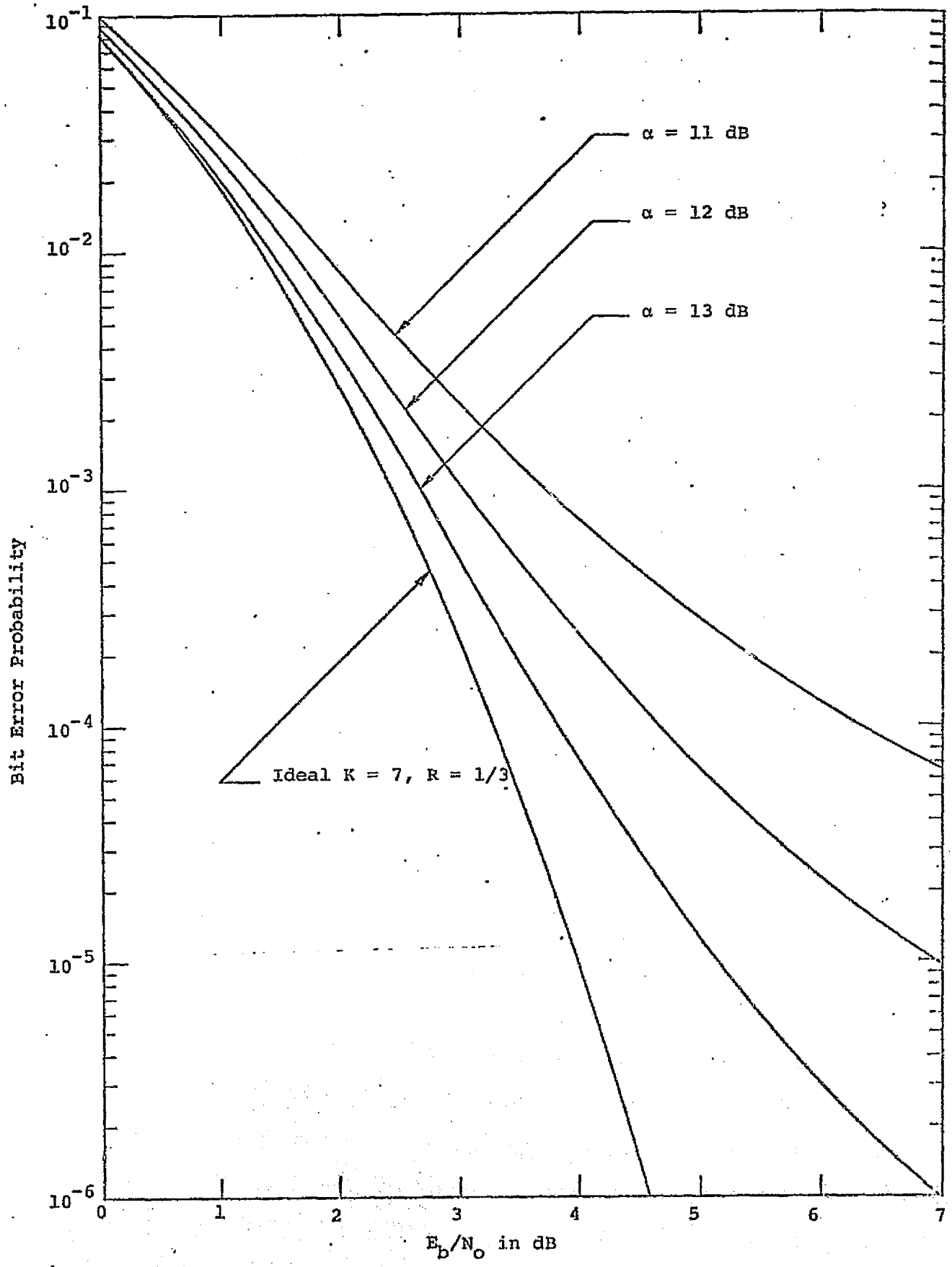


Figure 4.10. Theoretical Carrier Tracking Performance with Ideal Bit Sync

One might conjecture that the bit error probability curve with nonideal bit synchronization of Figure 3.9 could be used to obtain the performance of the system with non-ideal carrier tracking as in Figure 4.10. Such a set of curves were obtained. However, they proved to be better than the simulation results indicated. This discrepancy can be explained by noting that the bit timing and carrier tracking degradations are not the results of independent events. A bit timing error will cause the I & D circuits to integrate over the wrong time intervals and thus reduce the effective E_b/N_o available to the carrier tracking loop. Similarly a phase error will degrade the performance of the bit synchronization loop.

4.2.3 Carrier Tracking Performance Simulation

Figure 4.11 shows the simulated performance of the coded system with both carrier tracking and bit synchronization loops implemented. A 160 Hz loop bandwidth bit synchronizer was used. The carrier tracking loop used the decision-directed technique with either matched filters or digital filter models for the in-phase and quadrature channel filters and a loop bandwidth of 640 Hz. This carrier loop bandwidth was selected large enough to obtain a small steady state phase error but small enough

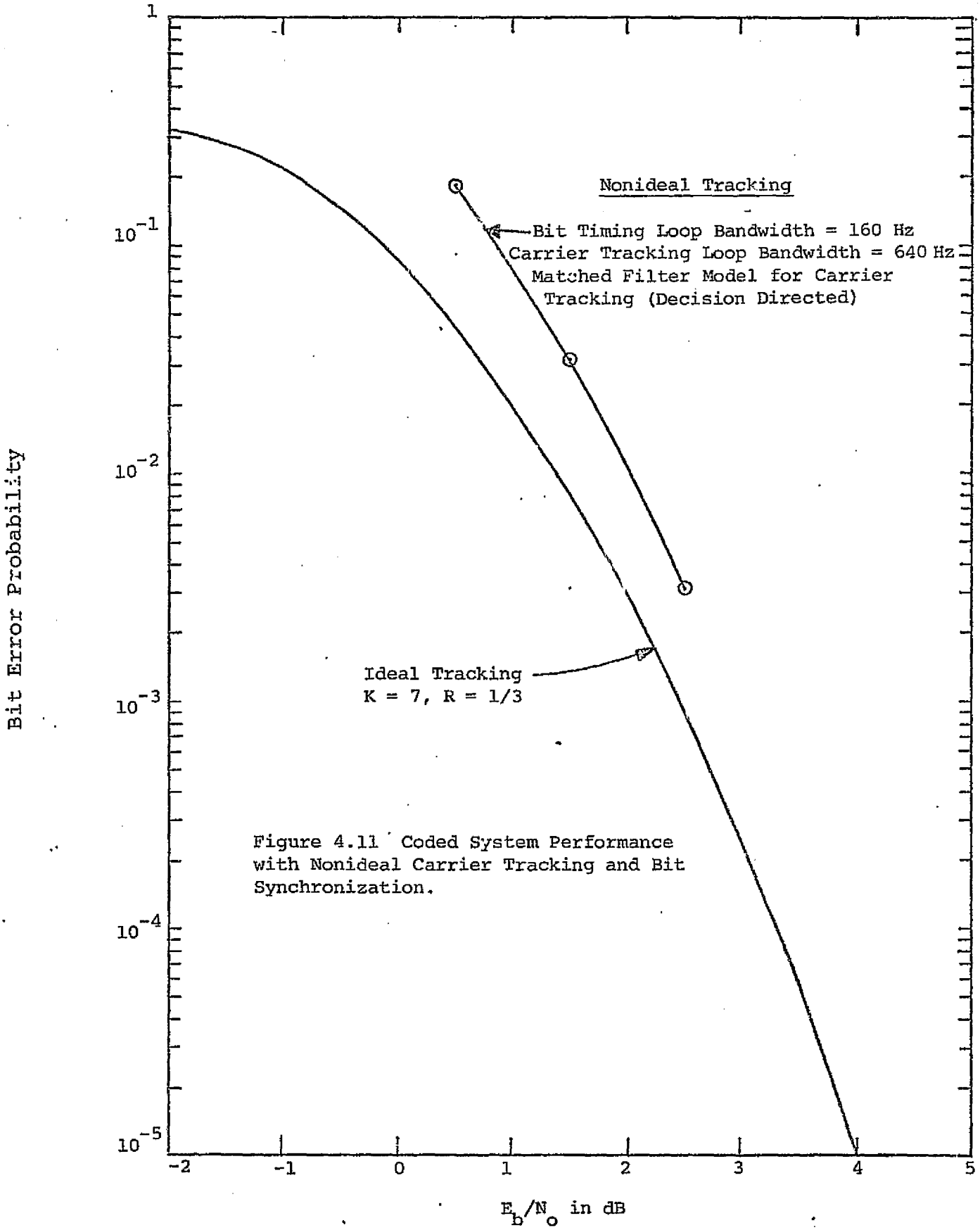


Figure 4.11 Coded System Performance with Nonideal Carrier Tracking and Bit Synchronization.

to make the probability of loss of lock very small. From Section 4.1 the steady state phase error due to the maximum expected doppler rate of 4.1 KHz/sec was shown to be $7240/B_L^2$ radians. The 640 Hz bandwidth makes this error insignificant. Simulations also showed that the probability of loss of lock with this bandwidth is very small. In all of the simulations at this bandwidth the loop never lost lock.

The curves of Figure 4.11 show that the combined carrier and bit timing tracking degradation from that of the ideal tracking case can be maintained at reasonable values. For the set of loop bandwidths used here, the total degradation varies from 0.6 to 1.3 dB for E_b/N_o ratios from 2.5 to 0.5 dB, respectively, for the matched filter model case.

The single delay digital filter in the I and Q channels, which closely approximate RC analog filters, were simulated with an optimum noise bandwidth of $1.6/T_a$. This model produces a somewhat larger degradation than the matched filter model. In fact, to obtain the same error probability performance as with the decision-directed matched filter, the loop bandwidth had to be reduced to 160 Hz, from the 640 Hz used in the latter case.

4.3 Combined Carrier and Bit Timing Acquisition

Acquiring carrier tracking within a reasonable amount of time with a doppler offset of 55 kHz requires either a large loop bandwidth or that the loop be stepped or swept through the frequency range of uncertainty. Simulations have shown that the carrier loop bandwidth cannot be increased very much above 640 Hz without occasionally losing lock. So in the acquisition simulations reported here the loop bandwidth was fixed at 640 Hz.

Before proceeding to the moderate-to-low E_b/N_o simulation results, it is helpful to examine the performance of the system at high signal-to-noise ratios. Figure 4.12 shows a typical time plot of the bit timing and phase errors for large signal-to-noise ratios. The data for this figure was obtained with an initial bit timing error of 1/4 of a channel symbol time and the maximum expected data frequency error of 108 Hz and a carrier frequency offset of 860 Hz. This assumes that the VCO would be swept through up to 64 steps of 860 Hz each in order to acquire a carrier whose initial uncertainty is 55 kHz. Carrier and bit timing loop bandwidths of 640 and 864 Hz, respectively, were used. The data for this figure and for all of the acquisition simulations reported here were obtained with the decision-directed loop and the matched filter type of in-phase and quadrature channel filters.

Figure 4.12 shows that the bit timing loop pulls in very fast even though the carrier loop is still slipping cycles. This can be explained by noting that a fixed phase error ϕ reduces the bit synchronizer effective E_b/N_o ratio by the factor $\cos^2 \phi$. Since the carrier loop is still slipping cycles the phase error sweeps through the complete 2π radian range producing an average degradation of 1/2 in the effective E_b/N_o ratio. At large signal-to-noise ratios this degradation is not enough to seriously increase the acquisiton time of the bit timing loop. However, it should be considered at small signal-to-noise ratios. With the exceptions that more cycles and bit times are slipped and a longer acquisition time is necessary, the general behavior shown in Figure 4.12 also occurs at lower signal-to-noise ratios.

Table 4.2 gives the combined carrier and bit timing acquisition of this system for several E_b/N_o ratios and for carrier acquisition methods in which the 55 kHz uncertainty is searched in either 64 or 512 steps. The data shows that for E_b/N_o ratios of 2.5 dB or more, which corresponds to a coded tracking bit error probability of 2×10^{-3} or less, acquisition can be achieved in a few seconds.

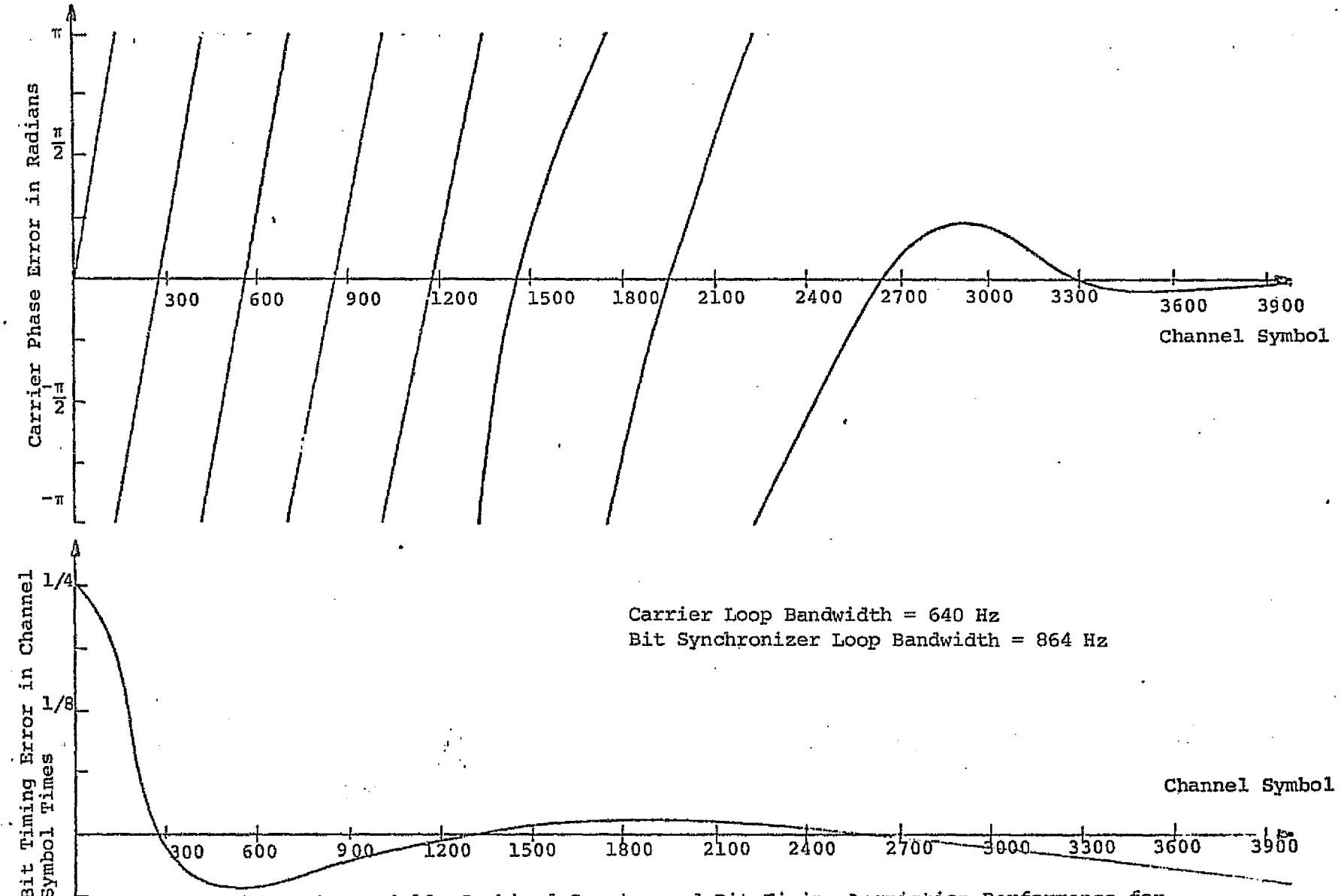


Figure 4.12 Combined Carrier and Bit Timing Acquistion Performance for E_b/N_o = 30 dB

E_b/N_0 in dB	Carrier Frequency Offset in Hz	Mean Aquisition Time in Seconds	Number of Search Steps Necessary For a ± 55 kHz Uncertainty	Total Acquisition Time for a ± 55 kHz Uncertainty in Seconds
30	860	.0167	64	.107
5.5	860	.0487	64	.312
2.5	860	.0562	64	.359
30	108	.00261	512	.1335
5.5	108	.00340	512	.174
2.5	108	.00556	512	.285

Carrier Loop Bandwidth = 640 Hz
Bit Synchronizer Loop Bandwidth = 864 Hz

Table 4.2 Summary of Combined Carrier and Bit Timing Acquisition Performance

References

4.1 J. P. Odenwalder, Unpublished Ph.D dissertation results. School of Engineering and Applied Science, University of California, Los Angeles, March, 1970.

4.2 J. A. Heller and I. M. Jacobs, "Viterbi Decoding for Satellite and Space Communication," IEEE Transactions on Communication Technology, Vol. COM-19, October 1971, pp. 835-848.

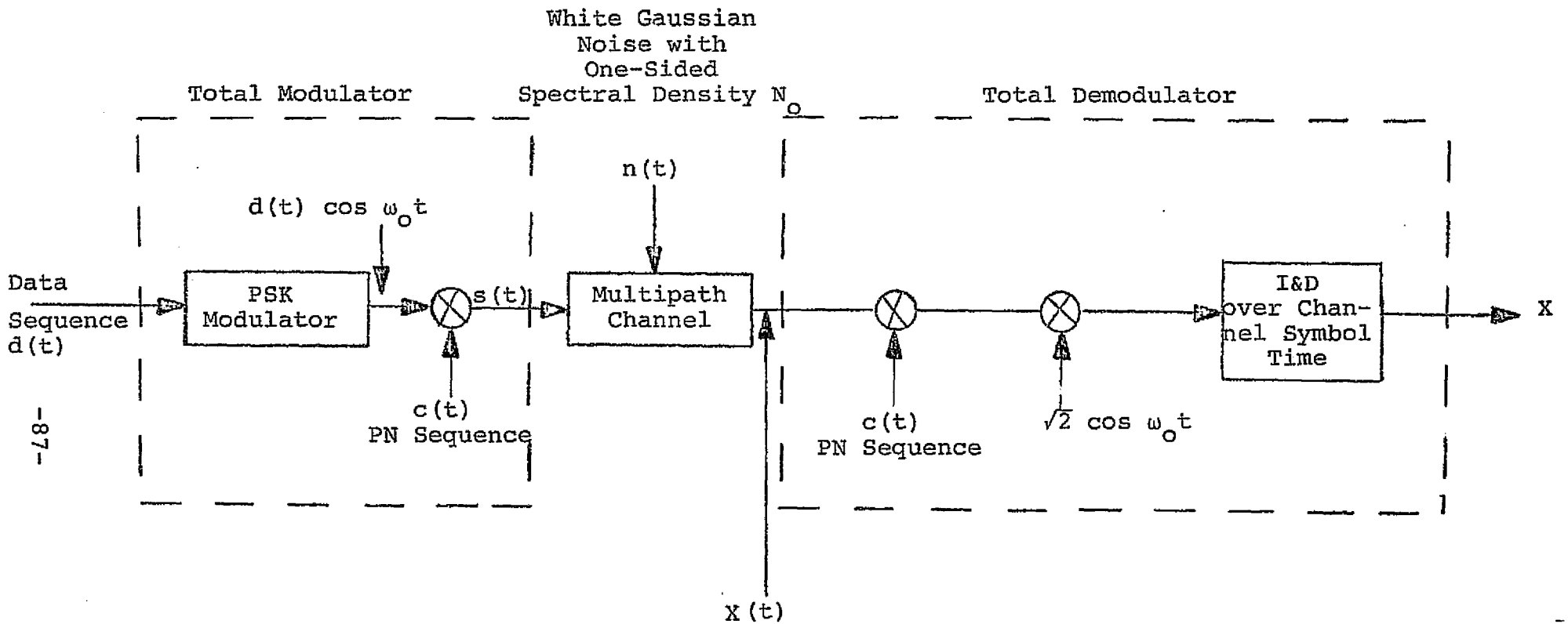
4.3 A. J. Viterbi, Principles of Coherent Communication. New York: McGraw-Hill, 1966.

5.0 Spread Spectrum Modulation and Its Effects

Originally the TDRS-to-ground (forward) link included a PN spread spectrum modulator/demodulator (see Figure 5.1) to reduce the energy density per unit bandwidth impinging on the earths surface (Ref. 5.1). This energy density reduction is no longer required. So this study effort has been redirected to examine the performance of the PN spread spectrum system in a multipath environment.

For a large number of PN chips per channel symbol, the multipath channel performance can be estimated as follows. Assume that the PN sequence is synchronous with the data sequence and that the number of PN chips per channel symbol, m, and the indirect path delays are integer multiples of the PN chip time. This assumption simplifies the analysis and for large m has negligible effect on the result. Then from Figure 5.1 the demodulator output for a positive transmitted channel symbol after demodulation, correlation with the local replica of the PN sequence and matched filtering is

$$X = \sqrt{S}\, T_s \left[1 + \frac{1}{m} \sum_i a_i \gamma_i \cos \omega_o \tau_i\right] + n \qquad (5.1)$$



$$X(t) = \underbrace{s(t)}_{\substack{\text{Direct}\\ \text{Path}\\ \text{Received}\\ \text{Signal}\\ \text{of Power}\\ S}} + \underbrace{\sum_i a_i\, s(t - \tau_i)}_{\substack{\text{Indirect}\\ \text{Path}\\ \text{Received}\\ \text{Signals}}} + n(t)$$

Figure 5.1 Spread Spectrum System Block Diagram

where n is a Gaussian random variable with mean zero and variance

$$\sigma_n^2 = \frac{N_o T_s}{2} \tag{5.2}$$

and the γ_i are random variables equal to the number of agreements minus the number of disagreements in comparing the polarities of the delayed received sequence and the demodulator PN sequence, over the m components corresponding to the given symbol integration time. For a large number of PN chips per channel symbol and different indirect path delays the γ_i are approximately independent random variables with zero means and variances m. Thus the mean and variance of X are

$$\overline{X} = \sqrt{S}\ T_s \tag{5.3}$$

and

$$\sigma_X^2 = \frac{ST_s^2}{m} \left(\sum_i a_i \cos \omega_o \tau_i\right)^2 + \frac{N_o T_s}{2} \tag{5.4}$$

The ratio is

$$\frac{\overline{X}^2}{\sigma_X^2} = \frac{2E_s}{N_o}\left\{\frac{1}{1 + \frac{2E_s}{N_o}\frac{(\sum_i a_i \cos \omega_o \tau_i)^2}{m}}\right\} \tag{5.5}$$

Comparing (5.5) with the corresponding ratio without multipath (i.e., $a_i = 0\ \forall i$), shows that the multipath signals cause an effective degradation of

$$\text{loss} = 10 \log \left\{1 + \frac{2E_b}{N_o}\frac{(\sum_i a_i \cos \omega_o \tau_i)^2}{N}\right\} \quad \text{dB} \tag{5.6}$$

where E_b/N_o is the information bit energy-to-noise ratio and $N = m/R_N = 3m$ is the number of PN chips per information bit. Equation 5.6 is valid for coded or uncoded operation. However, for a fixed bit error probability coded operation requires a smaller E_b/N_o ratio and thus has a smaller degradation due to multipath signals.

To obtain a more accurate estimate of the performance of this spread spectrum system, especially when there are only a few PN chips per information bit, a simulation program was written. Figure 5.2 shows the results of these simulations with one indirect path with $(a \cos \omega_o \tau) = 1$ and a delay of two PN chips. It is apparent that with a bandwidth expansion of 16 over that required with rate 1/3 channel coding, the E_b/N_o loss due to the indirect path can be reduced to about 0.6 dB at the moderate-to-high error

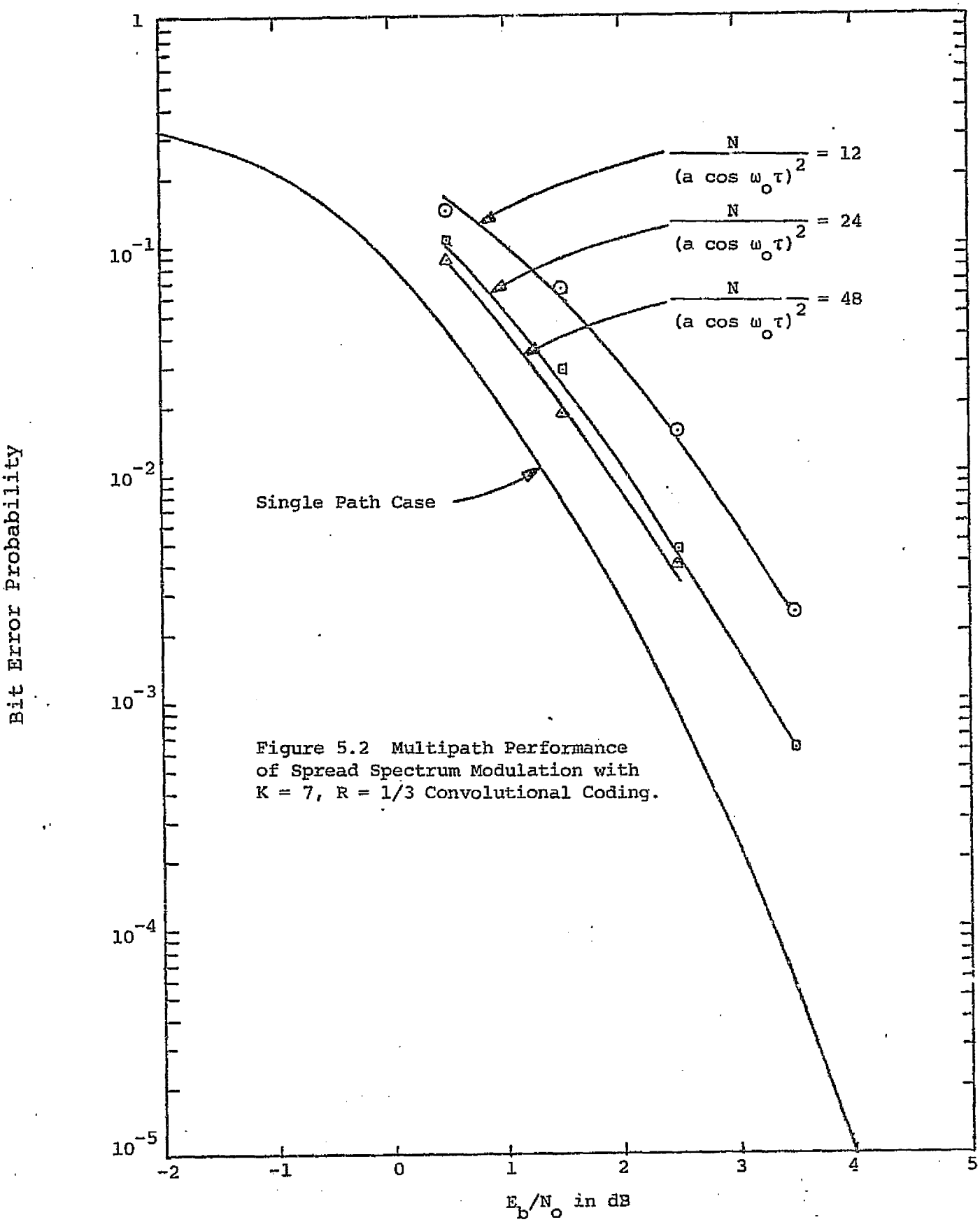


Figure 5.2 Multipath Performance of Spread Spectrum Modulation with K = 7, R = 1/3 Convolutional Coding.

rates where simulation data was obtained. Based on (5.6), even smaller losses are expected at smaller bit error probabilities.

C-2

REFERENCES

5.1 B. H. Batson and R. W. Moorehead, "A Digital Communications System for Manned Spaceflight Applications," in Proceedings of the 1973 International Conference on Communications, Seattle, Washington, pp. 37-1 - 37-9.

6.0 Conclusions

This design study of a coded digital transmission system has established the tracking loop parameters required to maintain error probability performance curves within approximately 1 dB of the ideal achievable by a K=7 R=1/3 convolutional encoder-Viterbi decoder with perfect bit and carrier tracking. It has been established, partly theoretically but mostly by simulation, that this performance can be achieved by using a bit synchronizer for BIϕ-L modulation and a decision-directed carrier tracking loop utilizing matched filters, which derive symbol timing from the bit synchronizer; the required loop bandwidth for the bit synchronizer and the carrier loop are respectively 160 Hz and 640 Hz. The degradation introduced by either loop is less than 0.5 dB. To achieve the same performance with a Costas carrier tracking loop, the loop bandwidth had to be reduced by a factor of 4.

Acquisition for both loops can be achieved within .06 sec. even at E_b/N_o ratios as low as 2.5 dB ($E_s/N_o \simeq$ -2.3 dB). For the acquisition simulation, the bit synchronizer loop bandwidth was widened by a factor of 8, while the carrier loop VCO was swept across the frequency uncertainty band. Attention was also devoted to a pseudonoise spread spectrum modulation technique to reduce the detrimental effects of multipath.

In the course of this study, it was found that proper design of interfaces between modules can significantly improve performance; in particular, the bit synchronizer

timing can be used to implement decision-directed matched filters in the carrier loop, and the channel quality (metric increase) indicator in the decoder can be used to resolve bit synchronizer and carrier loop tracking ambiguities.

This study has of necessity been limited to consideration of only a limited range of parameters, loop bandwidths, and acquisition strategies. However, a simulation capability has been developed which is available for investigation of other ranges of parameters and variations in tracking and acquisition techniques, and thus can be utilized for further study of any proposed communication techniques for this or similar missions.

APPENDIX I

PERFORMANCE ANALYSIS OF TYPE A AND B TIMING-ERROR LETECTORS

The analysis of the error detector shown in Figure 3.2 is based on observing that the two reference waveforms (bit detector and gate) are orthogonal to one another. Consequently, the Gaussian variables at the integrator outputs, X and Y, are independent. Thus the first and second moments of their products are just the products of the individual moments. That is, letting $R_B = XY$, we have

$$E(R_B^k) = E(X^k)\ E(Y^k) \tag{I.1}$$

and similarly if $R_A = (\text{sgn } X)Y$

$$E(R_A^k) = E[(\text{sgn } X)^k]\ E(Y^k) \tag{I.2}$$

(I.1) is used for the Type B soft decision bit detector, while (I.2) is used for the Type A hard decision case. Figure I.1 shows the input and reference waveforms both when no inter-bit transition occurs and when it does occur, for a timing error of a fraction τ of a symbol period. From this it can be seen that when no transition occurs, the X and Y outputs have normalized means, respectively.

$$(AT)^{-1}E(X|\text{no trans}) = (1-2\tau), \quad 0 \leq \tau \leq 1/2 \tag{I.3}$$

$$(AT)^{-1}E(Y|\text{no trans}) = \begin{cases} 2\tau \text{ for } 0 \leq \tau \leq \delta \\ 2\delta \text{ for } \delta \leq \tau \leq 1/2 - \delta \\ 2[\delta(1-a) + a(1/2-\tau)] \text{ for } 1/2-\delta \leq \tau \leq 1/2 \end{cases} \tag{I.4}$$

$$\stackrel{\Delta}{=} \alpha(\tau)$$

where $\delta = \Delta/T$ is the half-width of the gate normalized by the symbol time. When a transition occurs at the leading edge,

$$(AT)^{-1}E(X|\text{trans}) = (1-4\tau), \quad 0 \leq \tau \leq 1/2 \tag{I.5}$$

$$(AT)^{-1}E(Y|\text{trans}) = \begin{cases} 2\tau(1+a) \text{ for } 0 \leq \tau \leq \delta \\ 2\delta(1+a) \text{ for } \delta \leq \tau \leq 1/2-\delta \\ 2(1/2-\tau)(1+a) \text{ for } 1/2-\delta \leq \tau \leq 1/2 \end{cases} \tag{I.6}$$

$$\stackrel{\Delta}{=} \beta(\tau)$$

The variances of X and Y under either condition, due only to the input white noise, are

$$\text{Var}(X|\text{trans}) = \text{Var}(X|\text{no trans}) = N_oT/2$$

$$\text{Var}(Y|\text{trans}) = \text{Var}(Y|\text{no trans}) = N_oT\delta(1+a^2) \tag{I.7}$$

Also since $\text{sgn } X = \begin{cases} 1 \text{ if } X \geq 0 \\ -1 \text{ if } X < 0 \end{cases}$, then it follows from (I.3), (I.4) and (I.5)

$$E(\text{sgn } X) = \Pr(X \geq 0) - \Pr(X < 0) = 1-2Q[E(X)/\sqrt{\text{Var } X}]$$

where

$$Q(y) = \int_y^\infty \frac{e^{-z^2/2}}{\sqrt{2\pi}}\, dz$$

Thus

$$E(\text{sgn } X|\text{no trans}) = 1-2Q\left[\sqrt{2A^2T/N_o}(1-2\tau)\right]$$

$$E(\text{sgn } X|\text{trans}) = 1-2Q\left[\sqrt{2A^2T/N_o}(1-4\tau)\right] \tag{I.8}$$

From (I.2), (I.4), (I.6) and (I.8) if follows that for the Type A detector the mean output (error detector characteristic) is

$$\begin{aligned} ATg_A(\tau) &\overset{\Delta}{=} E[R_A(\tau)] = 1/2[E(\text{sgn } X|\text{no trans})\ E(Y|\text{no trans}) \\ &\quad + E(\text{sgn } X|\text{trans})\ E(Y|\text{trans})] \\ &= AT \begin{cases} \tau[(1-2Q[\sqrt{2E/N_o}(1-2\tau)])+(1+a)(1-2Q[\sqrt{2E/N_o}(1-4\tau)])] \\ \qquad\qquad \text{for } 0 \leq \tau \leq \delta \\ \delta[(1-2Q[\sqrt{2E/N_o}(1-2\tau)])+(1+a)(1-2Q[\sqrt{2E/N_o}(1-4\tau)])] \\ \qquad\qquad \text{for } \delta \leq \tau \leq 1/2-\delta \\ [\delta(1-a)+a(1/2-\tau)](1-2Q[\sqrt{2E/N_o}(1-2\tau)]) \\ \quad +(1/2-\tau)(1+a)(1-2Q[\sqrt{2E/N_o}(1-4\tau)]) \text{ for } 1/2-\delta \leq \tau \leq 1/2 \end{cases} \end{aligned} \tag{I.9}$$

where $E = A^2T$ is the symbol energy. Since $(\text{sgn } X)^2 = 1$, it follows that the normalized second moment is

$$E[R_A^2(\tau)] = N_oT\delta(1+a^2) + 1/2[E(Y|\text{No trans})]^2 + 1/2[E(Y|\text{trans})]^2$$

Thus the variance is

$$\begin{aligned}
\text{Var } R_A(\tau) &= E[R_A^2(\tau)] - E[R_A(\tau)]^2 \\
&= N_oT\delta(1+a^2) + A^2T^2[\ell_A(\tau)-g_A^2(\tau)] \\
&= N_oT\delta(1+a^2)\left\{1+\frac{E/N_o}{\delta(1+a^2)}[\ell_A(\tau)-g_A^2(\tau)]\right\} \\
&\stackrel{\Delta}{=} N_oT\delta(1+a^2)h_A(\tau) \qquad \text{(I.10)}
\end{aligned}$$

where

$$\ell_A(\tau) = \begin{cases} 2\tau^2[1+(1+a)^2] & \text{for } 0 \le \tau \le \delta \\ 2\delta^2[1+(1+a)^2] & \text{for } \delta \le \tau \le 1/2-\delta \\ 2[\delta(1-a)+a(1/2-\tau)]^2 + 2(1/2-\tau)^2(1+a)^2 & \\ \qquad\qquad \text{for } 1/2-\delta \le \tau \le 1/2 & \end{cases} \qquad \text{(I.11)}$$

For the Type B detector, similarly,

$$(AT)^2 g_B = E[R_B(\tau)] = 1/2[E(X|\text{trans})\ E(Y|\text{trans}) + E(X|\text{no trans})\ E(Y|\text{no trans})]$$

$$= (AT)^2 \begin{cases} \tau[(1-2\tau)+(1+a)(1-4\tau)] & \text{for } 0 \le \tau \le \delta \\ \delta[(1-2\tau)+(1+a)(1-4\tau)] & \text{for } \delta \le \tau \le 1/2-\delta \\ [\delta(1-a)+a(1/2-\tau)](1-2\tau)+(1/2-\tau)(1+a)(1-4\tau) & \\ \qquad\qquad \text{for } 1/2-\delta \le \tau \le 1/2 \end{cases} \qquad (I.12)$$

$$\text{Var}\ [R_B(\tau)] = E[R_B^2(\tau)] - E[R_B(\tau)]^2$$

$$= 1/2\left\{ \left[A^2T^2(1-2\tau)^2+\frac{N_oT}{2}\right]\left[A^2T^2\alpha^2(\tau)+N_oT\delta(1+a^2)\right] + \left[A^2T^2(1-4\tau)^2+\frac{N_oT}{2}\right]\left[A^2T^2\beta^2(\tau)+N_oT\delta(1+a^2)\right] \right\}$$

$$-A^4T^4g_B^2(\tau) \qquad (I.13)$$

where $\alpha(\tau)$ and $\beta(\tau)$ are defined in (I.4) and (I.6). This can be written as

$$\text{Var}\ [R_B(\tau)] = \frac{(N_oT)^2\delta(1+a^2)}{2}\ h_B(\tau)$$

where

$$h_B(\tau) \triangleq \frac{1}{2}\left\{ \left[1+\frac{2E}{N_o}(1-2\tau)^2\right]\left[1+\frac{E}{N_o}\ \frac{\alpha^2(\tau)}{\delta(1+a^2)}\right] + \left[1+\frac{2E}{N_o}\ (1-4\tau)^2\right]\left[1+\frac{E}{N_o}\ \frac{\beta^2(\tau)}{\delta(1+a^2)}\right] - 4\left(\frac{E}{N_o}\right)^2 \frac{g_B^2(\tau)}{\delta(1+a^2)} \right\} \qquad (I.14)$$

Now since the successive detector outputs are independent, either loop may be modelled as shown in Figure I.2 where the noise source is white with variance given by (I.10) or (I.13). Based on the techniques developed in Ref 3.5 and 3.6 it follows that the steady-state probability density of the timing error τ is given by

$$\pi(\tau) = \frac{\exp\,[-f(\tau)]/h(\tau)}{\int_{-1/2}^{1/2} \exp\,[-f(x)]/h(x)\;dx} \tag{I.15}$$

where

$$f(\tau) = \frac{2}{K}\int_0^{\tau} \frac{E[R(x)]}{Var[R(x)]}\,dx = C\int_0^{\tau} \frac{g(x)}{h(x)}\,dx$$

where $g(\tau)$ and $h(\tau)$ are defined by (I.9) and (I.10) for Type A and by (I.12) and (I.14) for Type B. Thus for a Type A loop

$$C_A = \frac{2AT}{KN_oT\delta(1+a^2)} = \frac{E/N_o}{2(B_LT)\delta(1+a^2)} \tag{I.16}$$

where*

$$B_LT = \frac{KAT}{4}$$

while for a Type B loop

$$C_B = \frac{(2AT)^2}{K(N_oT)^2\delta(1+a^2)} = \frac{(E/N_o)^2}{(B_LT)\delta(1+a^2)}$$

where*

$$B_LT = \frac{K(AT)^2}{4}$$

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*B_L is the loop bandwidth which is proportional to the loop gain. Note that this proportionality depends on A for Type A loops and $(AT)^2$ for Type B.

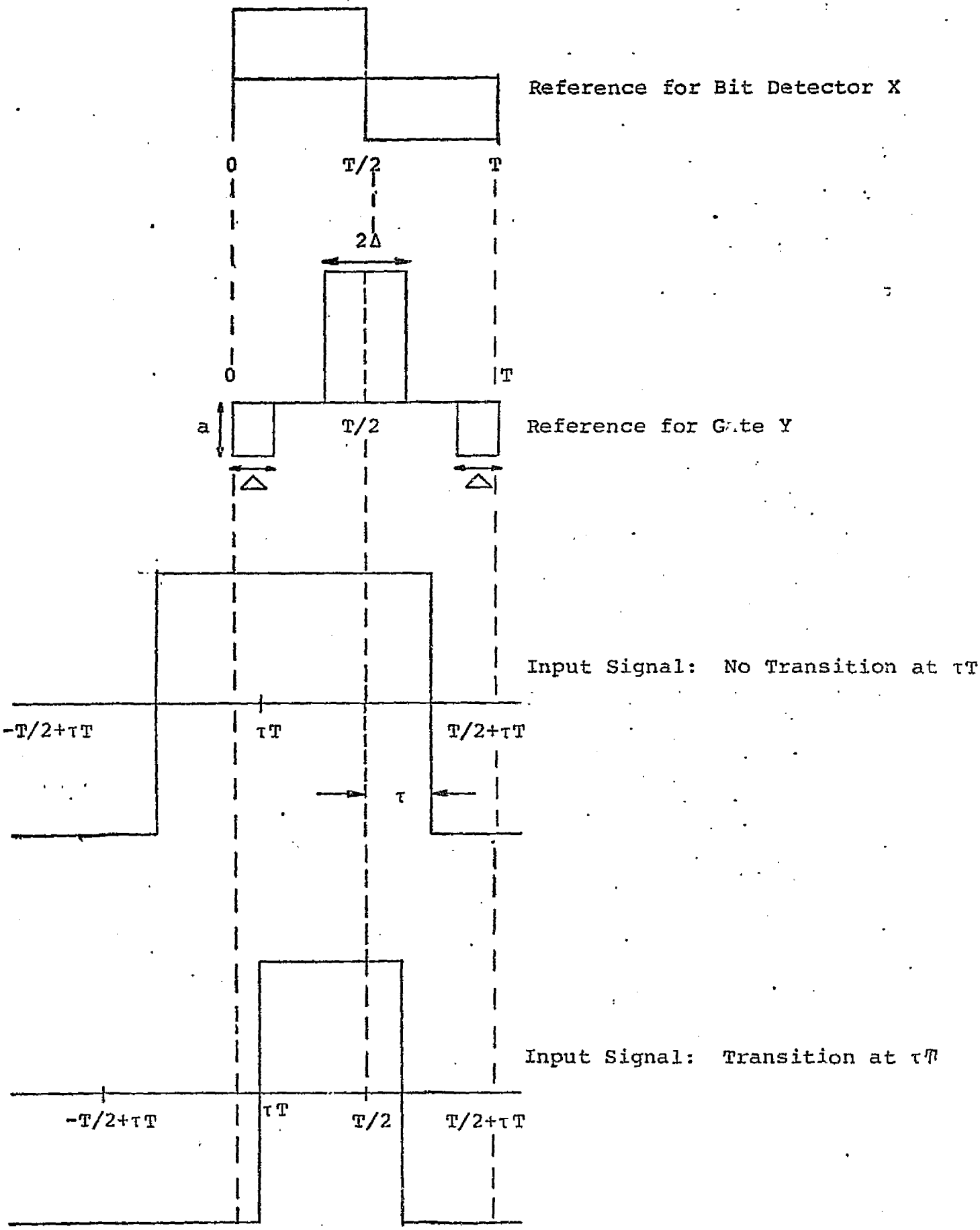

Figure I.1. Reference Waveforms for Types A and B Loops

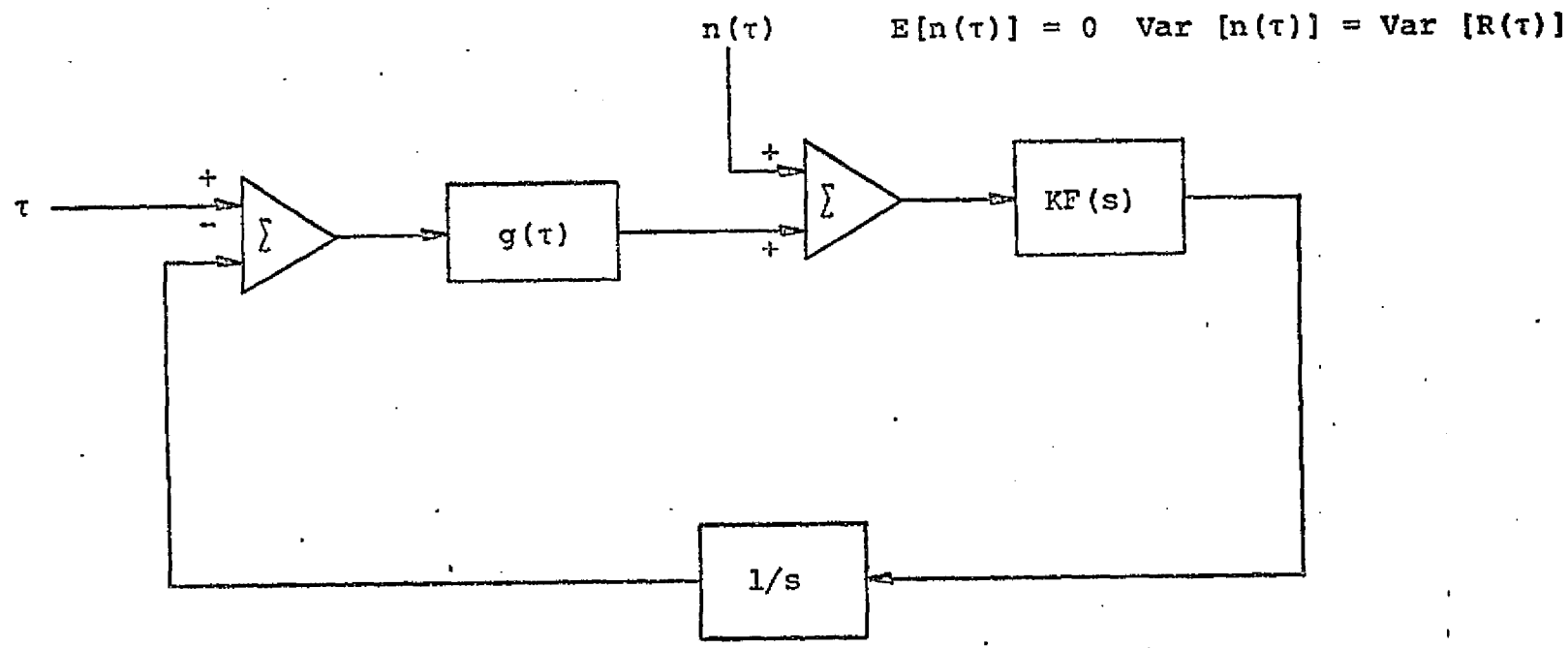

Figure I.2. Exact Model of Type A and B Loops

Note that in the linear region (where $g(x)/h(x) \simeq x$) the exponent becomes approximately $C\tau^2/2$ so that C^{-1} is the approximate variance. Thus for high signal-to-noise ratios

$$\sigma_A^2 \simeq C_A^{-1} = \frac{N_o B_L}{A^2} [2\delta(1+a^2)]$$

$$\sigma_B^2 \simeq C_B^{-1} = \frac{N_o B_L}{A^2} \frac{[2\delta(1+a^2)]}{2E/N_o}$$

Plots of $g(\tau)$ and $\pi(\tau)$ are given in Figures 3.4 and 3.5 for some specific values of the parameters.

The average bit error probability is obtained by averaging the conditional $P_B(\tau)$ by the density $\pi(\tau)$. Thus

$$\overline{P_B} = \int_{-1/2}^{1/2} P_B(\tau)\pi(\tau)\, d\tau$$

$$= 1/2 \int_{-1/2}^{1/2} \{Q[\sqrt{2E/N_o}\,(1-2\tau)] + Q[\sqrt{2E/N_o}(1-4\tau)]\}\, \pi(\tau)\, d\tau \tag{I.17}$$

The conditional $P_B(\tau)$ expression follows from the fact that the signal energy is $E(1-2\tau)$ when no transition occurs and $E(1-4\tau)$ when it does occur. Plots of $\overline{P_B}$ are given in Figure 3.6.

APPENDIX II

Binary convolutional codes with a guaranteed minimum density of code symbol transitions.

Assuming random zeros and ones from a data source, the average density of zero-one or one-zero transitions in the data stream will be .5 transitions per bit. If one is interested in worst case transition densities however, the all zeros or all ones sequence yields no transitions at all. In communications systems which derive bit timing by observing transitions in the received baseband modulated data, a decrease in the density of transitions results in an increase in bit timing jitter.

The use of linear binary convolutional or block codes does not solve the problem either. The all zeros data sequence always results in an all zeros code sequence with contains no transitions. In addition, for so called "transparent" codes, the all ones data sequence produces an all ones code sequence - again no transitions.

Fortunately, in most cases transitions can be guaranteed by simple bit-by-bit inversion of one or more of the parity symbol outputs of the encoder, and reinversion at the receiving end prior to decoding. For example, with a rate 1/3 code, one of the three parity generator outputs may be inverted.

Inversion of one or more of the code symbols makes the code nonlinear, but the code distance properties - hence the coding performance - does not change.

A convolutional encoder, being a finite state machine, has an input-output relationship which can be described by a state diagram. For example, the state of a rate 1/n code is the contents of the first K-1 encoder shift register stages, where the code constraint length is K. Sets of n code symbols are assigned to each state transition corresponding to the n encoder outputs produced for the given state transition.

The density of code symbol transitions produced by L information bits is the <u>number</u> of code symbol transitions in a given L state path in the state diagram, divided by nL. The <u>minimum density</u> L state path is that path containing the minimum number of symbol transitions. For a given code it is possible to determine the symbol transition density of the minimum density L state path as L approaches infinity. As long as this transition density is non-zero, we can guarantee a minimum density of code symbol transitions regardless of the data source output sequence. Furthermore, the minimum transition density code sequence is periodic with period less than $n2^K$. The periodicity guarantees that it is impossible to have a long span of code symbols with transition densities less than the minimum average density.

As an example, for the K = 7, rate 1/3 code given by Odenwalder (Ref. 3.7) and one parity generator output complemented, the minimum density of code symbol transitions is .22, or two transitions per 9 code symbols.

APPENDIX III

Lock Detector Statistics

III.1 Detectability of Lock Indication

The lock detector described in Section 3.6 forms the magnitude of the bit detector output and accumulates it over N symbol times. In additive white Gaussian noise, when perfect lock is achieved, the mean value of the magnitude of the bit detector output is

$$E\left|x_1\right| = \frac{1}{\sqrt{2\pi}}\int_{-\infty}^{\infty}\left|x\right| e^{-(x-\sqrt{2E/N_o})^2/2}dx$$

$$= \sqrt{\frac{2}{\pi}}\, e^{-E/N_o} + \sqrt{\frac{2E}{N_o}}\left[1-2Q\left(\sqrt{\frac{2E}{N_o}}\right)\right]$$

where Q is as defined in Appendix I and the noise variance is normalized to unity, without loss of generality. Now for small E/N_o, this becomes approximately

$$E\left|x_1\right| \simeq \sqrt{\frac{2}{\pi}}\left(1 + 2\frac{E}{N_o}\right)$$

In the out of lock condition, the bit detector responds essentially only to noise. Then its magnitude per symbol has mean

$$E\left|x_o\right| = \sqrt{\frac{2}{\pi}}$$

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The second moments in the two cases are

$$E\left|x_1\right|^2 = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\infty} |x|^2 \, e^{-\left[\left(x-\sqrt{2E/N_o}\right)^2/2\right]} dx$$

$$= 1 + \frac{2E}{N_o}$$

and

$$E\left|x_o\right|^2 = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{\infty} |x|^2 \, e^{-x^2/2} \, dx = 1$$

Thus the respective variances are

$$VAR(|x_1|) = E(|x_1|^2) - (E|x_1|)^2 \simeq \left(1 - \frac{2}{\pi}\right) + \frac{2E}{N_o}\left(1 - \frac{4}{\pi}\right)$$

$$\simeq 1 - \frac{2}{\pi} \text{ for } \frac{E}{N_o} << 1$$

and

$$Var(|x_o|) = E(|x_o|^2) - (E|x_o|)^2 = 1 - \frac{2}{\pi}$$

For the false alarm and detection probabilities, based on the accumulated sum over N symbol times, classical radar techniques (Ref. 3.11) The key parameter is the detectability, defined as

$$D = \frac{\left(N\,E\,|x_1| - N\,E\,|x_o|\right)^2}{N \text{ Var } |x_o|}$$

$$\simeq \frac{\frac{2}{\pi}(2E/N_o)^2 \, N}{1 - \frac{2}{\pi}} \qquad E/N_o << 1$$

III.2 Ambigious Lock

For ambigious lock determination, as described in Section 3.4, we compare two bit detectors displaced by 1/2 bit from one another. The correct position will have mean as before

$$E|X_1| \simeq \sqrt{\frac{2}{\pi}}\,(1 + 2E/N_o)$$

while the incorrect (ambigious) lock position will have mean

$$E|X_a| \simeq \sqrt{\frac{2}{\pi}}\,(1 + E/N_o)$$

since its effective energy will be only half as large (since with random data it responds to signals only half as often). Then the probability that the accumulated incorrect (ambigious) lock detector output will be greater than the correct accumulated output is

$$P_a = Pr\left(\sum_{i=1}^{N} X_{1i} < \sum_{i=1}^{N} X_{ai}\right)$$

$$= Q\left(\sqrt{N(E|X_1| - E|X_a|)^2 / [2-(4/\pi)]}\right)$$

where $E|X_1| - E|X_a| \simeq \sqrt{2/\pi}\ (E/N_o)$

And approximating $Q(X) \lesssim \frac{1}{2} e^{-X^2/2}$

we have

$$Pa \lesssim \frac{1}{2} e^{-\frac{N}{2(\pi-2)}\left(\frac{E}{N_o}\right)^2} \qquad \text{(random data)}$$

If the data has only 10% transisions (worst case to be assumed), then

$$E|X_a| \simeq \sqrt{\frac{2}{\pi}}\left(1 + \frac{9E}{10\ N_o}\right) \qquad \text{(worst case)}$$

which results in choosing the incorrect lock position with probability

$$P_a \lesssim \frac{1}{2}\, e^{-\frac{N}{2(\pi-2)}\left(\frac{11}{10}\frac{E}{N_o}\right)^2} \qquad \text{(worst case)}$$

At $E/N_o = -5dB$, this means that the number of symbols accumulated must be made at least

$$N \geq 246 \qquad \text{(worst case)}$$

in order to keep $P_a < 10^{-5}$.

In contrast with random data, at the same SNR and for the same P_a, we need only

$$N \geq 203 \qquad \text{(random data)}$$

The probability of ambigious lock is actually smaller than P_a, because not only must $|X_a|$ be greater than $|X_1|$, but in addition $|X_a| - |X_1|$ must be greater than some threshold, as described in Section 6.

APPENDIX IV

LINEARIZED MODEL ANALYSIS OF A DIGITAL PHASE-LOCKED LOOP

This appendix contains an analysis of the linearized digital phase-locked loop of Figure IV.1. Stability criteria, the phase error due to deterministic inputs, and the phase error variance due to noise are determined.

IV.1 Stability Analysis

Figure IV.2 gives the Z-transform model of the tracking loop of Figure IV.1. The closed-loop transfer function of the linearized model is

$$H(Z) = \frac{PF(Z)}{1+PF(Z)}$$

$$= \frac{K'PZ^{-1}[1-(1-a')Z^{-1}]}{1-AZ^{-1} + BZ^{-2}} \qquad \text{(IV.1)}$$

where

$$A = 2 - K'P \qquad \text{(IV.2)}$$

$$B = 1 - (1-a')K'P \qquad \text{(IV.3)}$$

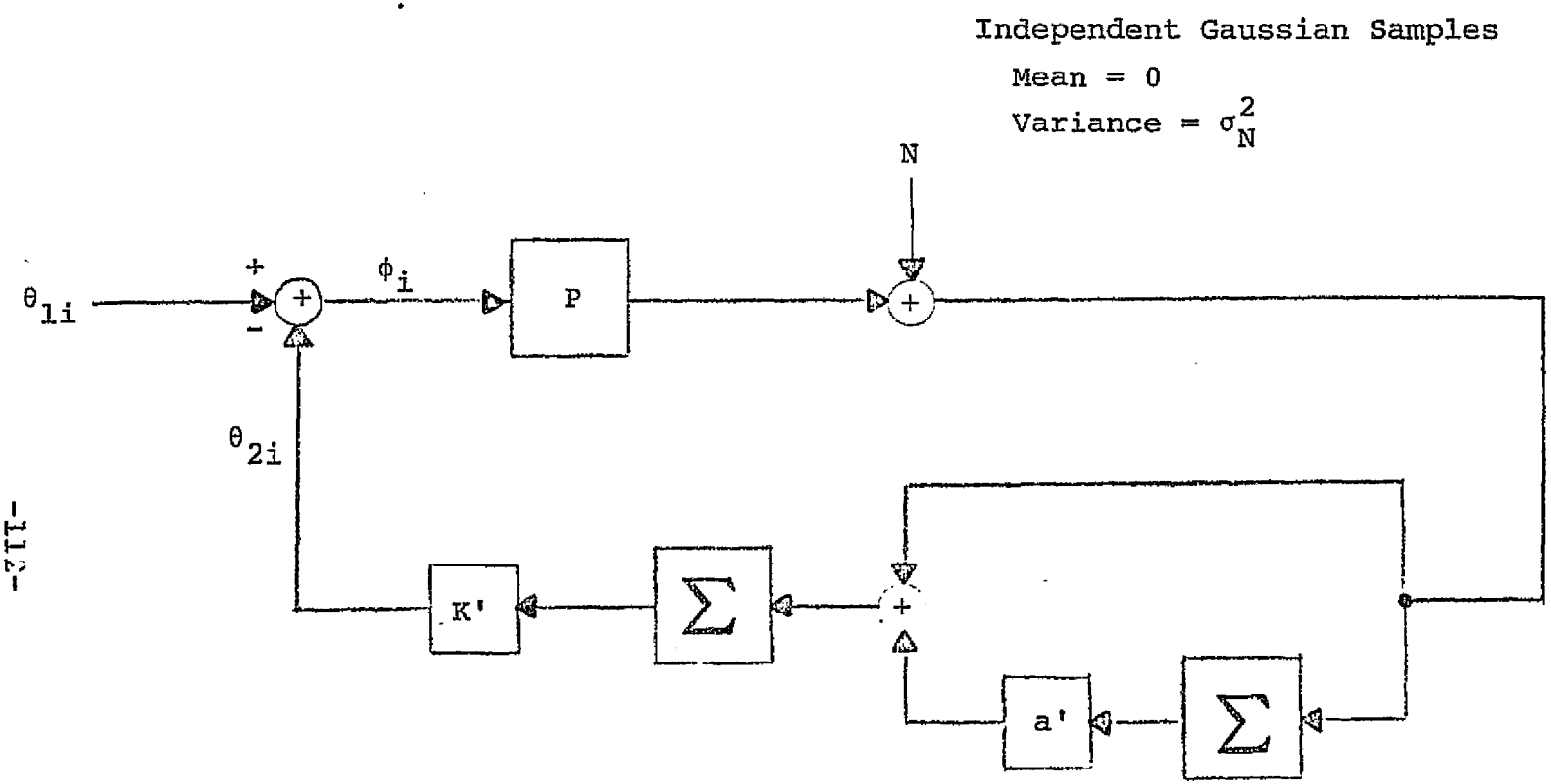

Figure IV.1 Linearized Digital Second Order Phase-Locked Loop Model

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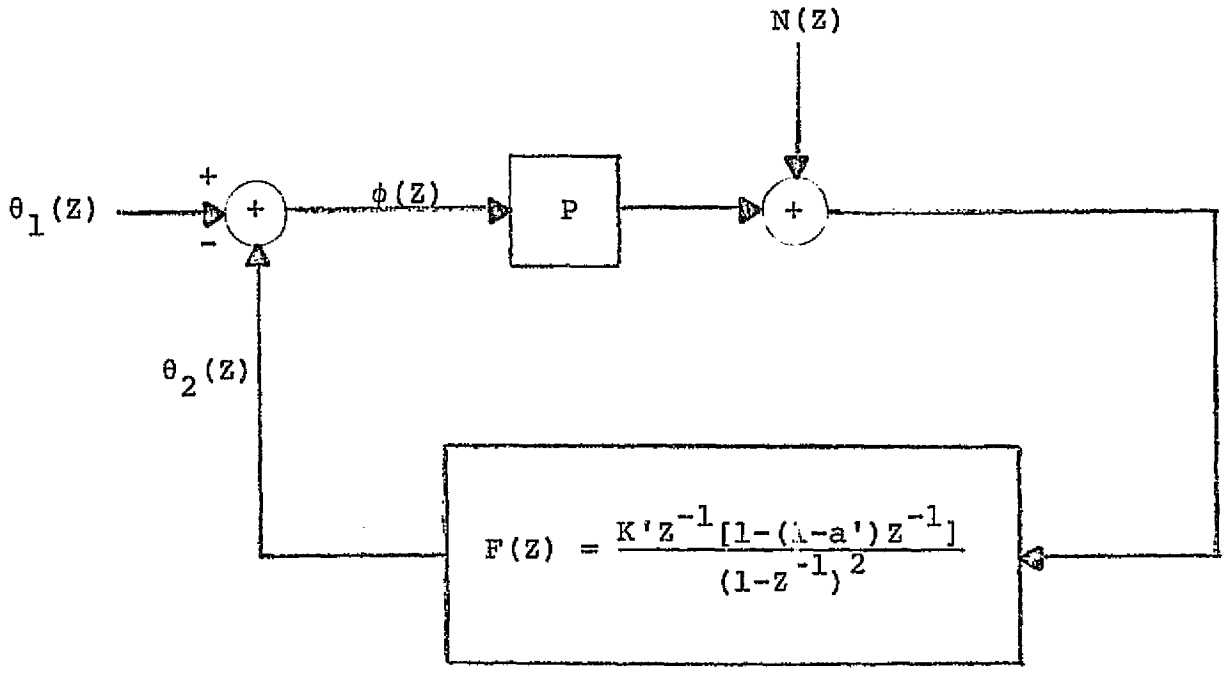

Figure IV.2 Z-Transform Model of a Digital Phase-Locked Loop

For stability, the poles of the closed-loop transfer function must be within the unit circle. Figure IV.3 shows the loci of these poles as the loop gain K'P is varied. This figure is drawn for $0 \leq a' < 1$ which can be shown to be necessary for stability. Both poles are at +1 when K'P = 0. As K'P increases they split and follow the circle shown. At K'P = 4a', the poles remerge and with further increases in K'P one approaches +1 and the other approaches $-\infty$. Thus, the system is stable if and only if

$$0 \leq a' < 1 \tag{IV.4}$$

$$0 < K'P < \frac{4}{2-a'} \tag{IV.5}$$

We assume that these equations are satisfied throughout this appendix.

The stability criterion of a first-order loop (a' = 0) can be obtained from Figure IV.3 or Equation IV.5 with a' = 0. In this case the system is stable when $0 < K'P < 2$.

IV.2 Deterministic System Response

Since this is a linearized system we can treat the effects of the signal and noise inputs separately. Thus, the phase error response to an arbitrary phase and frequency input $\phi_k = \alpha + k\beta$ is

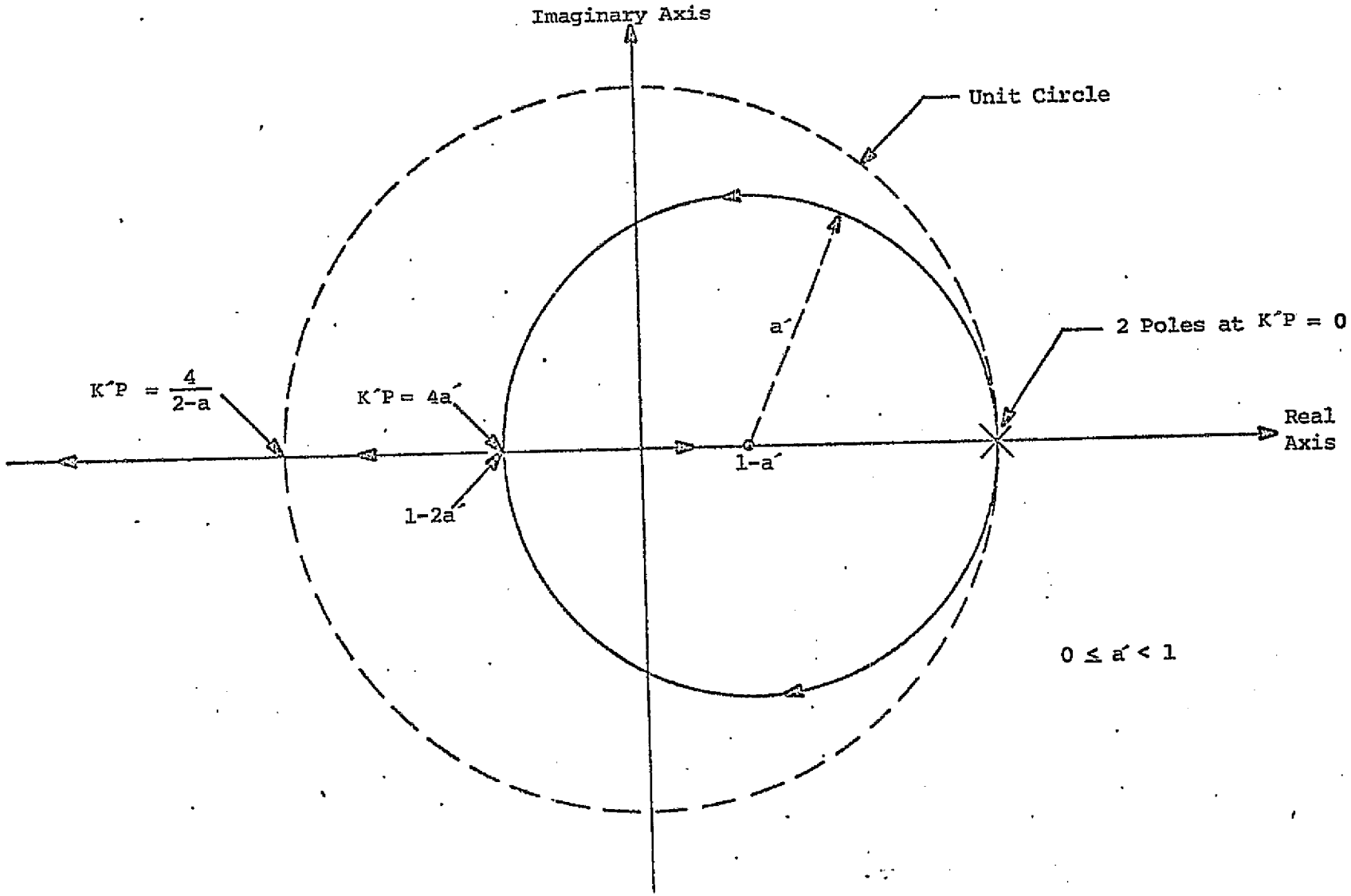

Figure IV.3 Root Loci of a Second-Order Digital Phase-Locked Loop.

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$$\phi_s(Z) = [1 - H(Z)]\ \theta(Z)$$

$$= \frac{(1-Z^{-1})^2}{1-AZ^{-1} + BZ^{-2}} \left[\frac{\alpha}{1-Z^{-1}} + \frac{\beta Z^{-1}}{(1-Z^{-1})^2}\right]$$

$$= \frac{\alpha + (\beta-\alpha)Z^{-1}}{1-AZ^{-1} + BZ^{-2}} \tag{IV.6}$$

The sequence of outputs corresponding to (IV.6) can be obtained, but it depends on the location of the closed-loop poles and the general expression is uninformative. However, the final value can be obtained as

$$\lim_{k\to\infty} \phi_s(k) = \lim_{Z\to 1} (1-Z^{-1})\ \phi_s(Z) = 0 \quad \text{if } a'K'P \neq 0$$

So, as expected, this second-order loop can track phase and frequency inputs with zero steady-state phase error.

For a first-order loop ($a' = 0$) $H(Z)$ reduces to

$$H(Z) = \frac{K'PZ^{-1}}{1+(K'P-1)Z^{-1}} \tag{IV.7}$$

and the response to a phase and frequency input is

$$\phi_s(Z) = \frac{1}{1+(K'P-1)Z^{-1}} \left[\alpha + \frac{\beta Z^{-1}}{1-Z^{-1}}\right] \tag{IV.8}$$

Solving (IV.8) for the sequence of phase errors gives

$$\phi_s(k) = \begin{cases} \alpha & , k = 0 \\ (\alpha - \frac{\beta}{K'P})\ (1-K'P)^k + \frac{\beta}{K'P} & , k \geq 1 \end{cases} \qquad \text{(IV.9)}$$

Since

$$\lim_{k\to\infty} \phi_s(k) = \frac{\beta}{K'P}$$

a second-order loop is needed to track frequency inputs.

IV.3 Phase Error Variance

The transfer function from the noise input to the phase error signal is $-H(Z)/P$. So the effect of noise alone is to produce a random phase error ϕ_n with variance

$$\text{Var}\ (\phi_n) = \frac{\sigma_N^2}{P^2} \oint H(Z)H(Z^{-1})\ \frac{Z^{-1}}{2\pi i}\ dZ$$

$$= \sigma_N^2 (K')^2 \oint \frac{Z^{-1}[1-(1-a')Z^{-1}][1-(1-a')Z]}{(1-AZ^{-1}+BZ^{-2})(1-AZ+BZ^2)}\ \frac{dZ}{2\pi i}$$

Performing the contour integration around the unit circle yields

$$\mathrm{Var}\ (\phi_n) = \sigma_N^2 (K')^2 \left\{ \frac{(1+B)\,[1+(1-a')^2]-2(1-a')A}{(1-B)\,[(1+B)^2-A^2]} \right\}$$

$$= \frac{\sigma_N^2}{P^2} \left\{ \frac{2a'+K'P(1-a')(2-a')}{(1-a')\,[4-K'P(2-a')]} \right\} \qquad \text{(IV.10)}$$

By comparison with the corresponding quantity for an analog loop, the quantity in the large brackets of (IV.10) is equal to two times the loop bandwidth times the time between samples.

In Section 4 the time between samples is T_s, the channel symbol time, and

$$a' = T_s\ a$$

$$K' = T_s\ K$$

Thus

$$B_L = \frac{2a+KP(1-T_s a)(2-T_s a)}{2(1-T_s a)\,[4-T_s KP(2-T_s a)]}$$

$$\approx \frac{a + KP}{4} \qquad \text{(IV.11)}$$

From (IV.10) and (IV.11) the inverse variance is

$$\alpha = \frac{P^2}{\sigma_N^2}\ \frac{1}{2B_L T_s} \qquad \text{(IV.12)}$$