FINAL REPORT

HIGH BIT RATE MASS DATA STORAGE DEVICE

SUBMITTED UNDER

CONTRACT NAS 8-28959

TO

NATIONAL AERONAUTICS & SPACE ADMINISTRATION
GEORGE C. MARSHALL SPACE FLIGHT CENTER
HUNTSVILLE, ALABAMA

DOCUMENT TM-329-165

FEBRUARY 23, 1973

LEACH CORPORATION
CONTROLS DIVISION
717 N. CONEY AVENUE
AZUSA, CALIFORNIA 91702

PREFACE

This report has been prepared in accordance with data requirement description MA-061 of Contract NAS8-28959 for a High Bit Rate Mass Data Storage Device manufactured for GMSFC by Leach Corporation.

R. E. Crowe
Program Manager

Jack Hodson
Director of Engineering

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SECTION I CONTRACTURAL WORK REQUIREMENTS

1.1 Scope of Work

The scope of work is defined in exhibit "A" of Contract NAS8-28959. (See Appendix A of this report).

Exhibit "A" of Contract NAS8-28959 consists of three basic parts:

(a) Technical Requirements

(b) Delivery Requirements

(c) Data Requirements

1.2 Technical Requirements

The technical requirements are per GMSFC specification GC110467 as modified by Leach Proposal 732639 and Leach letter dated 6/27/72. (See Appendix B of this report)

The technical requirements are, briefly: A device which can record and reproduce a 10 Mbs BI-Ø-L signal for 30 minutes continuously with an error rate of less than 10^{-6} in a laboratory environment.

1.3 Delivery Requirements

The delivery of the device is required within six months after award of contract (December 29, 1972) and the final report due thirty (3) days later (January 29, 1973).

1.4 Data Requirements

The data requirements are per DRL 308, Contract NAS8-28959 and consists of monthly letter progress reports, this final report (TM 329-165) and the operation and maintenance manual to be submitted with the end item.

SECTION II SUMMARY OF THE ACCOMPLISHMENTS AND ASSESSMENT AGAINST THE SCOPE OF WORK

2.1 Technical Performance

The High Bit Rate Mass Storage Device as tested per Leach ATP 204411 exceeds the contractural technical performance requirements as described in Section 1.2 of this report.

2.2 Delivery Requirements

The hardware was shipped on February 19, 1973, Way Bill No. 075405362, approximately 30 days behind schedule.

SECTION III DETAILED TECHNICAL INFORMATION

3.1 Design Principles

The basic design principles which led to the Leach "HD 103 Feasibility Model" (the forerunner of this device) are explained in Appendix C, "Technical Discussion and Double Density Codes".

The High Bit Rate Mass Storage Device was based on the Leach developed "HD 103 Feasibility Model". The logic implementation was changed for reduced IC package count.

3.1.1 Design and Functional Description

The following is a detailed discussion describing the design and function of the High Bit Rate Mass Storage Device. The applicable schematics are attached to this report. The Leach supplied instruction manual also contains this material. The functional description of the MTR-7114 tape recorder is contained in a standard manual concerning the recorder only.

3.1.1.1 DESCRIPTION

The HDDR-II Mass Data Storage System consists of a Leach MTR 7114 Recorder/Reproducer a wire-wrapped, integrated circuit flat plane and necessary power supplies for the flat plane. These units, with interconnecting cables and control panel are enclosed in a common housing mounted on casters. Refer to Figure 1, Figure 2, Figure 3 and Figure 4. The description of the MTR 7114 Recorder/Reproducer can be found in the manual for that unit. The purpose of this discussion is to describe the electronics used in the HDDR-II double density decoding and encoding techniques.

3.1.1.2 THEORY OF OPERATION

The following paragraph is a discussion of the double density recording and reproducing techniques. Shown in Figure 5 is a binary representation of a SØM signal. This SØM signal may be toggled off either the positive or negative toggle. In Figure 5, it is shown coming off the positive toggle; divided by 2. This is the double density wave form. After it has been toggled off the SØM signal, all of the binary information is still maintained in the double density wave form. The code is listed under the double density wave form as being either a 2, 3, or 4. If there is one full bit width between the transitions of the double density wave form this is called a 2. If there is 1-1/2 bit widths between transitions, it is called a 3. If there are 2 bit widths between transitions, it is called a 4. This code has one characteristic which allows a parity detection and is also used to generate a sync word for purposes of deskewing. This characteristic is the fact that the data can never generate an odd number of 3's between 4's. Thus, the sync word used in the HDDR-II Mass Data Storage System is a pattern 4, 3, 4, 3. This pattern cannot be generated

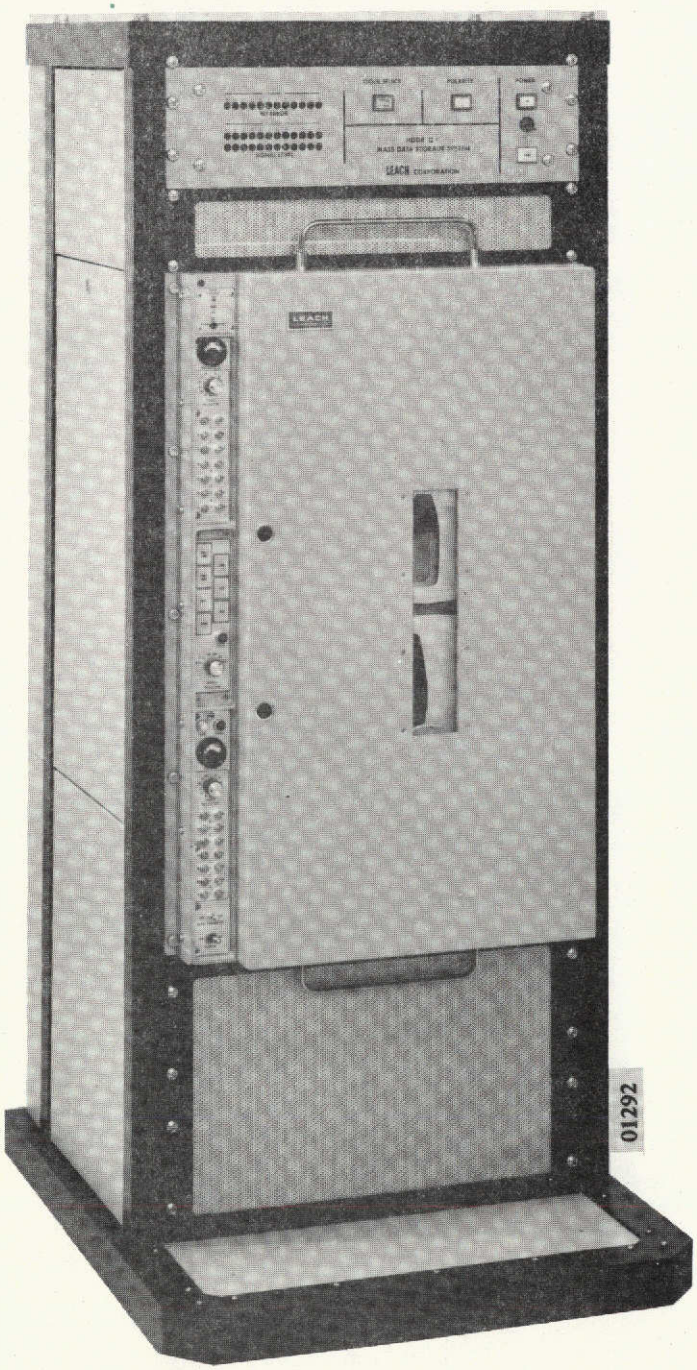


FIGURE 1. HDDR - II MASS DATA STORAGE SYSTEM

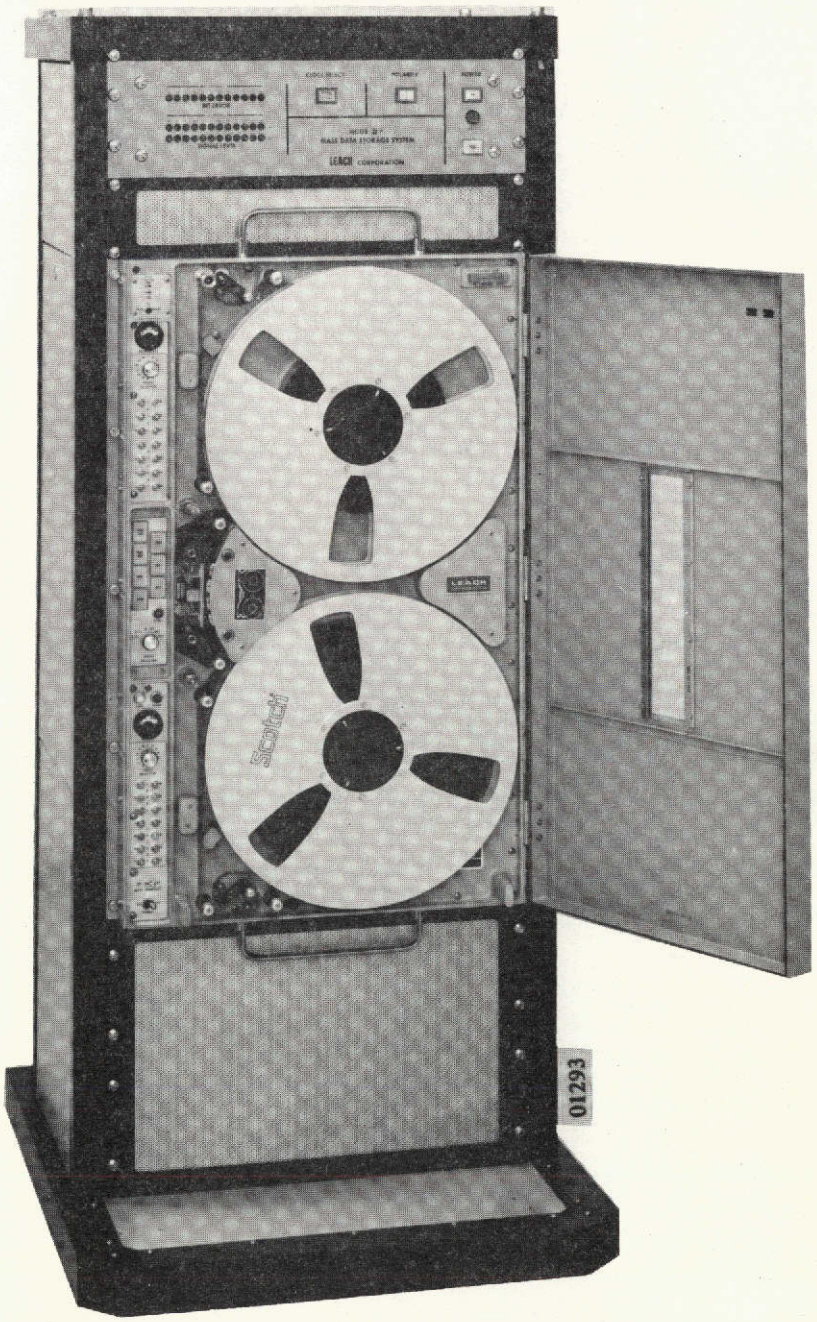


FIGURE 2. HDDR-II MASS DATA STORAGE SYSTEM, RECORDER COVER OPEN

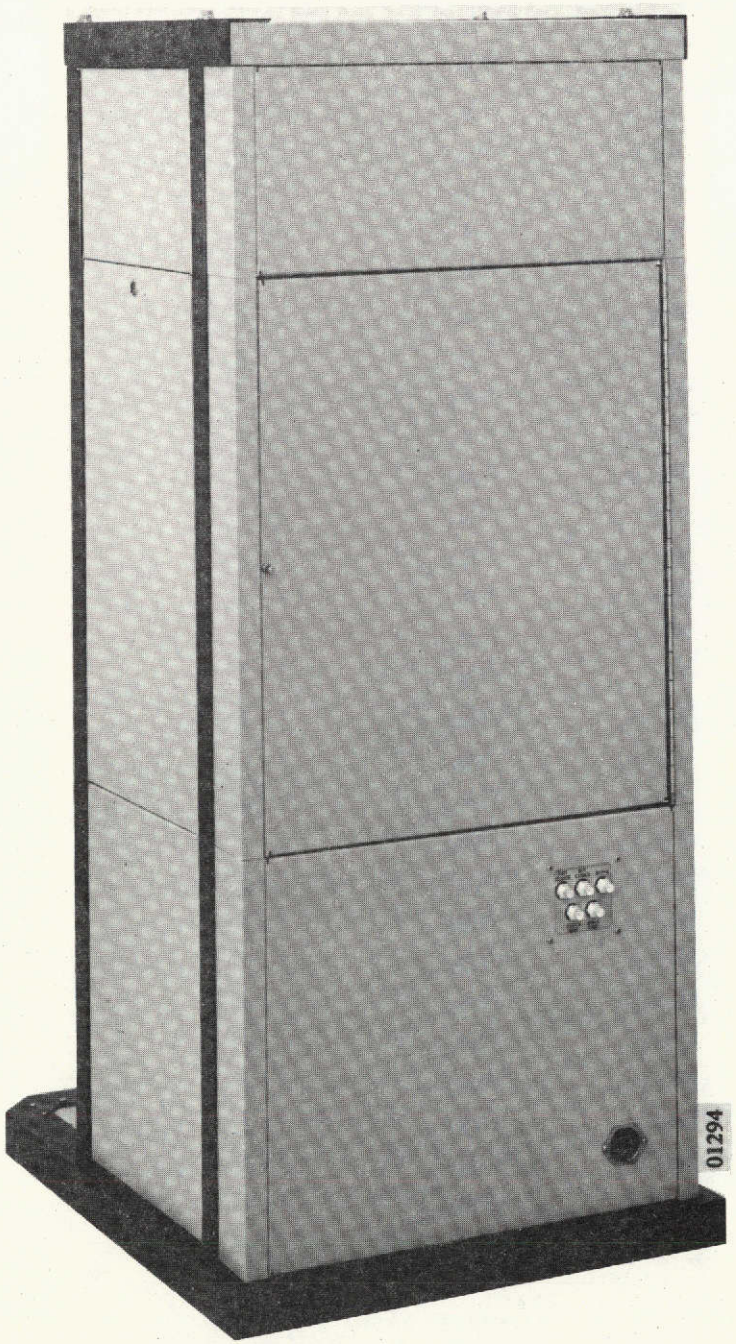


FIGURE 3. HDDR-II MASS DATA STORAGE SYSTEM, REAR VIEW

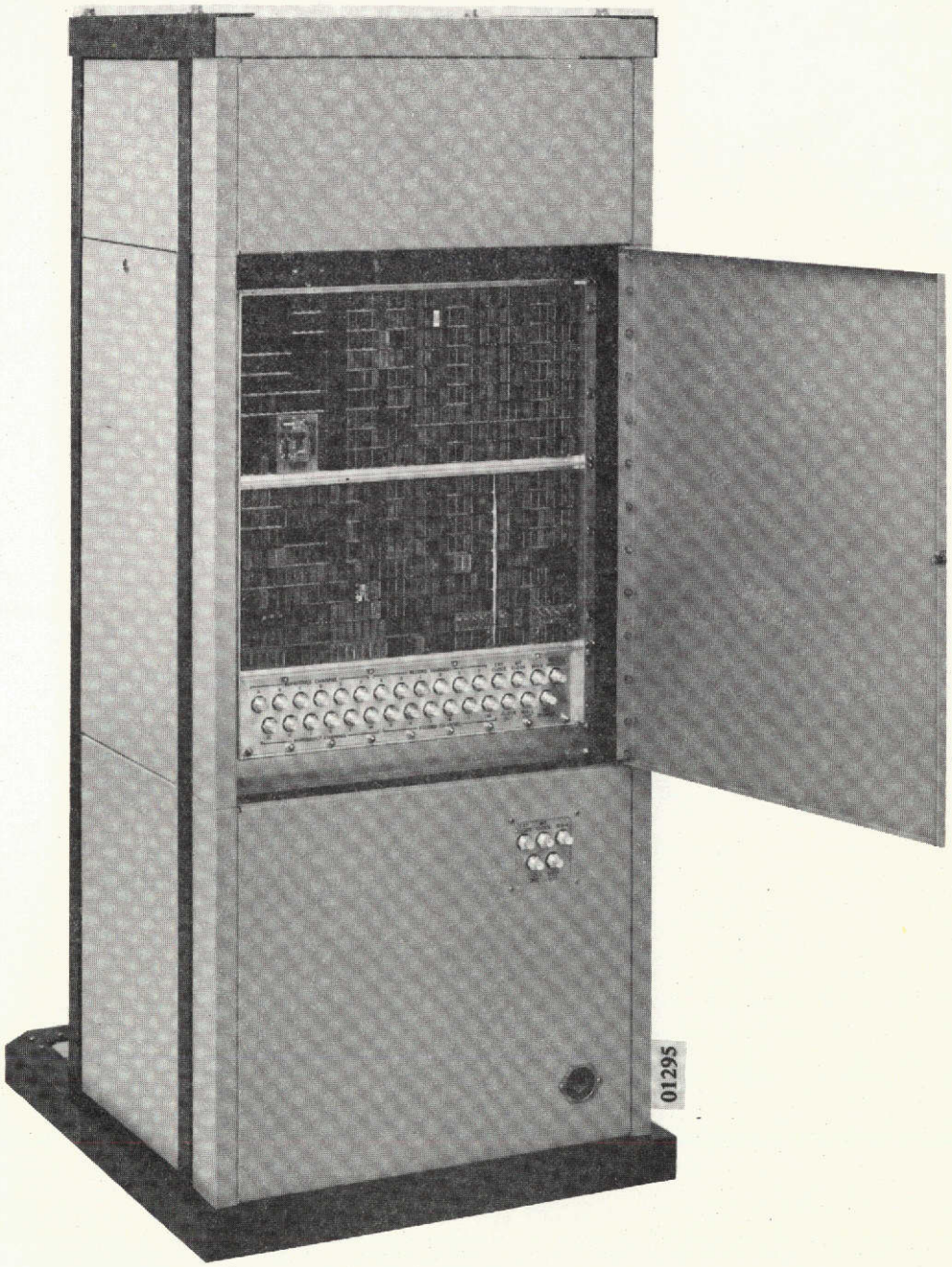


FIGURE 4. HDDR-II MASS DATA STORAGE SYSTEM, REAR COVER OPEN

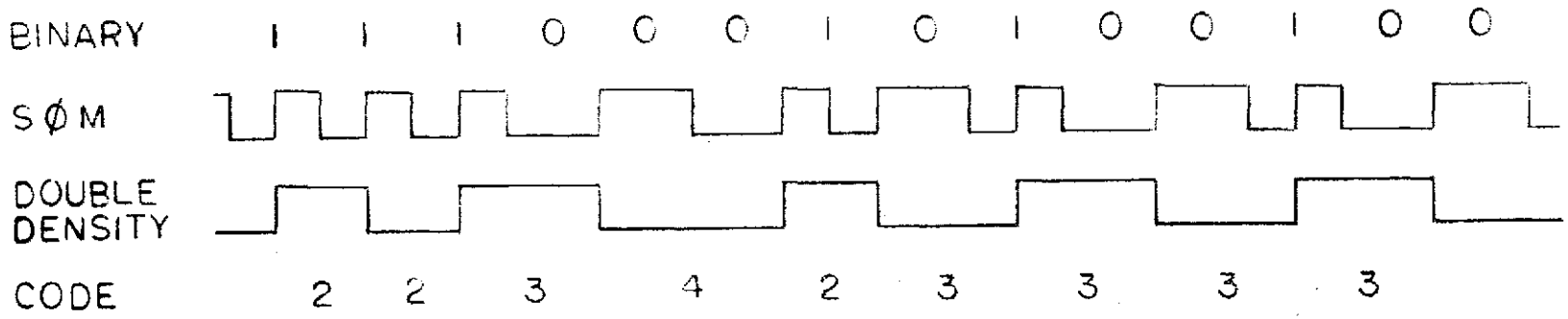


FIGURE 5
DOUBLE DENSITY WAVEFORMS

by the data, therefore the data can never generate a false sync. The sync word is discussed further in the text.

3.1.1.3 ENCODER

The block diagram for the HDDR-II Mass Data Storage System is on Dwg. 204448 located in Appendix "D". Refer to it during this discussion, and also to the schematics on Dwg. 204257. Referring to the block diagram on the HDDR-II twelve-channel recorder encoder, there are clock and data selection gates. These are used first to determine whether the recorder is in the record mode or in the playback mode. This is determined by means of the record indicate signal from the MTR 7114 recorder. If it is in the record mode, the only clock that can be selected is the bit clock along with the BI-Ø-L data. If in the playback mode, the clock that is selected is either the external clock or the 10MHz internal clock as determined by the clock select switch. In the record mode, the clock select switch has no effect. The data polarity switch simply inverts the incoming BI-Ø-L data. The output of these clock and data selection gates form a signal which is the ANBC clock, which is the incoming 10MHz clock and the NRZL 10MHz data. This is the data after it has been converted from BI-Ø-L. These circuits are shown on page 2 of the schematic 204257.

Continuing to refer to the block diagram and page 2 of the schematic, the ANBC clock is divided by 50 and outputted as a servo reference. This servo reference is fed to one of the tracks of the recorder to servo the recorder and to provide an initial dejittering of the data coming off tape. Also, it will keep the packing density constant for various incoming clock frequencies. The ANBC signal is divided by 12 and this output is called "enable strobe", referred to on the block diagram and schematic as ES. This term, ES, is used on page 3 of the schematic in the 12-bit serial-to-parallel converter. It is also used again on page 17 of the schematic in the parallel-to-serial converter of the output data after it has been played back. The ES term is further divided by 128. Several

of the terms from the 128 divider are used in the buffer address control, and on the decoder buffer read address.

After the term has been divided by 128, it is fed to the phase-lock voltage controlled oscillator. This VCO generates the system bit clock, called SBC, and this clock is approximately 14.2 MHz. SBC is divided by 16 and shown on the schematic and block diagram as VCO 16. This is the record frequency before it is divided by 2 for the double density wave form. The VCO 16 term is divided by 8 and divided by 17 and fed back to the VCO input. The two inputs to the voltage controlled oscillator are phase locked at the same frequency. The VCO 16 signal is 17/16 times greater than the ES signal. This 17/16 ratio allows the insertion of the 8-bit sync after the 128 bits of data.

Refer to page 3 of the schematic. Found here is the 12-bit parallel-to-serial converter in the 16 x 12 encoder buffer. The 16 x 12 encoder buffer is achieved by using three random access memories, each of which is a 4 x 16 encoder buffer. The buffer address control provides the control of the incoming data address and it also controls the address of the outgoing data from the encoder buffer. The purpose of the encoder buffer is to allow the insertion of the sync word. Refer to Figure 6. The sync word, referred to as the sync toggle, is generated on page 2 of the schematic and is designated by the term ST. This sync toggle goes to page 4 of the schematic

After every 128 bits of data, the data coming out of the encoder buffer is disabled for 8 bits. However, the data going into the buffer, at a slower rate, continues into the buffer uninterrupted. The output of the data, being disabled, allows the sync generator to generate its sync word; on the double density code the sync word is 4, 3, 4, 3. Also in the sync word is another bit of information which is a superfluous bit added to get the ratio of 136 to 128, which is the same as 17/16. The NRZL data is converted to SØM and then mixed with the sync toggle. After this, it is passed through a divide-by-2 D-type flip-flop which

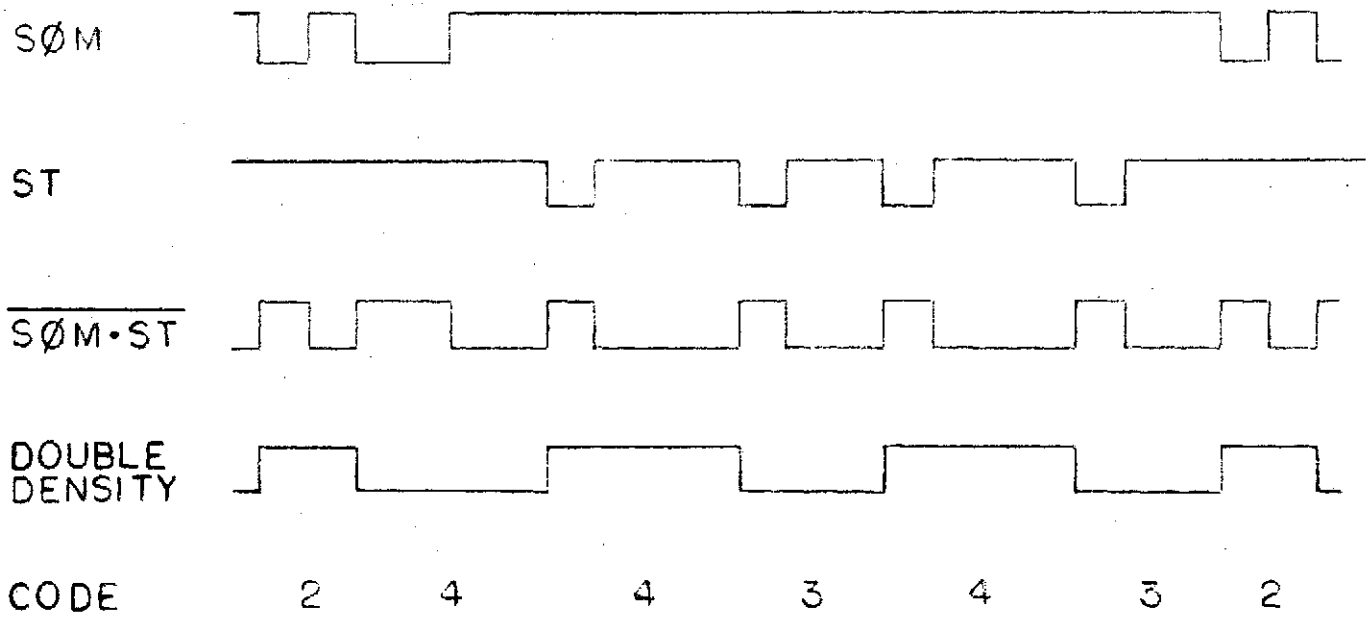


FIGURE 6

GENERATION OF SYNC WORD
REFERENCE: PAGES 2 AND 4 OF 204257

converts it to double density. It is then phase equalized and sent to one of the twelve record tracks.

3.1.1.4 DECODER

The playback signal is capacitively coupled to a zero crossing detector. Refer to pages 18, 19 and 20 of the schematic. The zero crossing detector drives the high/low level detector which drives a lamp, indicating the playback signal is too high or too low. These lamps are self explanatory and are found on the front panel. The zero crossing detector is passed to a transition detector that outputs a pulse for every transition, whether it is positive or negative. The output pulse of the transition detector is referred to on the schematics as FT3. This pulse is synchronized with the SBC clock and is exactly one SBC clock wide. The transition detector is used to reset a counter which drives the aperture detector. The transition detector and counter are found on pages 5 through 16 inclusive of the schematic. The aperture detector and the aperture- to- NRZL converter and deskew/dejitter buffer are also found on pages 5 through 16 of the schematic. The counter is used to drive the aperture detector. The aperture detector outputs the 2, 3, or 4 as used in the double density symbolic language. These 2's, 3's and 4's are sent to what may be called an aperture- to- NRZL converter. This is actually the heart of the decoding process.

The aperture- to- NRZL converter has four basic outputs. (1) The 3's parity output. This output detects whenever there are an odd number of 3's between 4's, which are not part of the sync word. In the event of a 3's parity error, the bit error lamp on the front panel will illuminate for approximately 1/10 of a second. (2) The playback data output. This output is NRZL data and still contains the sync word as part of it. (3) The playback clock output. This playback clock inherently has a lot of jitter. Even without flutter in the recorder, the playback clock will have jitter due to decoding from a 2, 3 or 4 to NRZL data. (4) The sync detector output. The sync detector zeros the deskew/dejitter

buffer write address. Thus, all 12 channels will have the same read addresses, because the decoder buffer read address is the same for all 12 channels. Thus, the sync detector by zeroing the write address control, facilitates a deskew operation. Since the information is clocked out of the buffer at the ANBC clock rate, it is also a dejitter buffer. The output of the random access memory (which is the 256 x 1 buffer) inherently has many slivers. These slivers, or spikes, come at predictable times and thus can be eliminated by proper clocking through a D-type flip-flop. This is the desliver circuit found on page 17. All twelve channels come to page 17 where they are deslivered and sent to a parallel-to-serial converter. The parallel-to-serial twelve-channel converter accepts NRZL data from all twelve tracks and converts it to NRZL serial data. It is then converted to BI-Ø-L data with a clock output. It can be seen that this system allows a high density recording. The outputs are deskewed/dejittered Bi-Ø-L information at 10 MHz. It should be kept in mind that during playback only, the same clock may be entered into the system that was used in recording. Normally, this will be 10 MHz, crystal controlled, internal clock. However, if another frequency is used, then an external clock must be used and that external clock must be the same clock that was used as the bit clock during record.

3.1.1.5 Calculations

Not applicable

3.1.1.6 Unique Procedures or Techniques Developed For the Contract

Unique techniques were previously developed on the Leach HD 103 feasibility model and applied during the construction of the device. These are described in Appendix C.

3.1.1.7 Operation Instructions

Operation instructions are contained in the instruction manuals furnished with the equipment. Additional copies may be made available on request.

3.2 Design Evaluation

3.2.1 Summary of Test Results

The error rate test summarizes a digital system's performance. Using a repeatative pattern, the measured error rate was 7.9 in 10^8 compared to the 10^{-6} error rate specified.

3.2.2 Description of Tests

Tests were run on the equipment per Leach LTP 204411 which describes the purpose, procedures, and gives the detailed test data. This procedure is Appendix D.

3.2.2.1 Evaluation of Test Data

The test data consisted of three basic sets of measurements:

1) Compliance to data and clock timing relationships.

2) Jitter between output data and clock measurements

3) Error rate data

3.2.2.1.1 Data and Clock Timing Relationships

These relationships were verified by paragraphs 3.1 and 3.2 of the ATP to be within the Figure 2 tolerances (ATP)

3.2.2.1.2 Jitter Measurements

This measurement showed no discernable jitter on the 2ns scale of the 7704A scope.

This was to be expected because of the following:

1) The measuring equipment contributed negligible "apparent" jitter.

2) The data was being clocked out of the output dejitter/deskew buffer by the same clock being compared to the data.

3) The data was further buffered by a SN 74S74 very high speed flip-flop before the output line driver.

4) The clock jitter was negligible.

3.2.2.1.3 Error Rate

The error rate data using the 16 bit repetative pattern specified in the ATP was 7.9×10^{-8}.

Much testing during the pre-ATP was done with a 1 megabit random code. The equipment performance was not as good with this pattern, but was still within the 10^{-6} requirement.

During the pre-ATP phase, two important items were apparent:

1) The heads should be cleaned every time the tape is changed.

2) 3M type 971 tape provided better performance. The MTR-7114 was set up to use this tape, and the roll used for the ATP was sent with the device.

Analysis of the test data shows that the device exceeds all performance requirements.

3.2.2.2 Problem Areas

During the course of development of this equipment, three general problem areas were apparent. These were: (1) The phase locked VCO and (2) High speed operation of conventional counter IC's and (3) Timing problems.

The first two problems were inter-related because the counters were used around the loop, such that when the counter began to miss counts the VCO was driven to a higher frequency causing the counter tostop entirely.

A change in counter types and a faster method of decoding the count was used to circumvent the problem.

A limitation to the VCO to prevent very high oscillation frequencies was also implemented.

The timing problems were numerous, but were generally solved using Schottky high speed logic rather than a complete redesign of the circuit.

During the pre-ATP phase when all external panels were in place, a heat problem which resulted in the recorder equalizer changing characteristics was apparent. This, of course, caused the error rate to increase as a function of time.

This problem was solved by adding a blower to the bottom of the cabinet, and by removing a rear panel from the recorder.

Because the recorder is completely enclosed by the device's cabinet, the removal of this panel does not jeopardize operation of the equipment, and is not noticeable.

These problem areas, plus the required extensive debug of the logic plane caused delivery to be extended approximately 45 days.

3.3 Conclusions and Recommendations

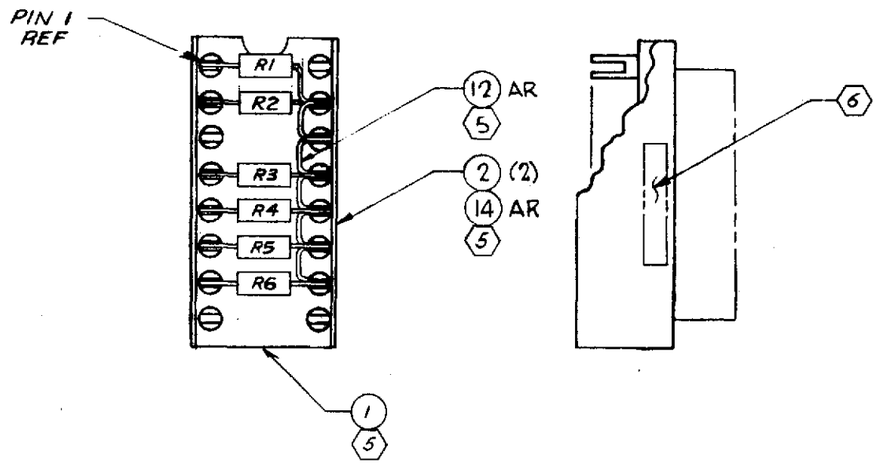
This contract proved the feasibility of a high data rate mass storage device in a compact package for use in a laboratory environment.

More development work will be required to reduce the size, weight and power for spacecraft applications.

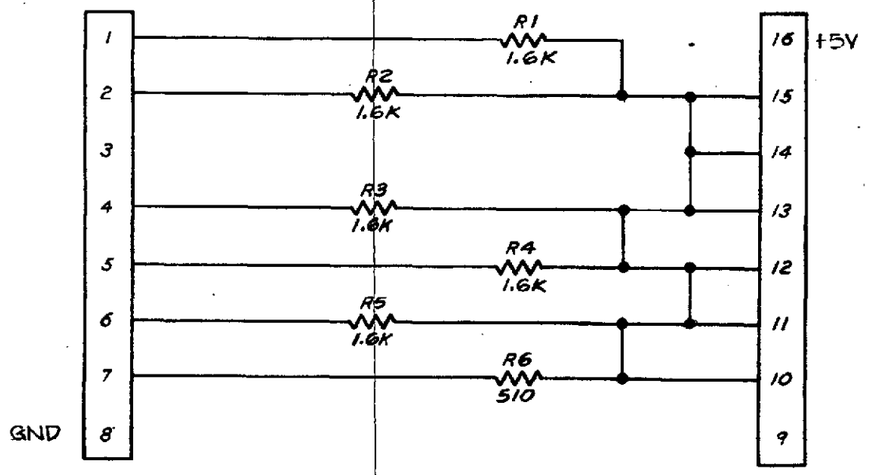
FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



-001 SHOWN



SCHEMATIC DIAGRAM

FOR PARTS LIST SEE PL204250-001

6 MARK PER LEACH STD 201179-006 WITH 204250-001 APPROX WHERE SHOWN.

5 AFTER ASSEMBLY OF ITEM NO.'S 5,& 6 TO ITEM NO. 1, BOND ITEM NO. 2 TO ITEM NO. 1 2 PLACES AS SHOWN, USING ITEM NO. 14.

4 ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/8W.

3 REFERENCE DESIGNATIONS ARE ABBREVIATED: PREFIX WITH UNIT NO. AND APPLICABLE SUBASSEMBLY DESIGNATION.

2 FOR NEXT ASSEMBLY SEE APPLICATION BLOCK.

1 DO NOT SCALE DRAWING.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PARTS LIST

QTY N/A	QTY U/O	NEXT ASSEMBLY	USED ON
12	12	204274	HD-103

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCE

FRACTIONS ± .XX ±

ANGLES ± .XXX ±

MATERIAL

FINISH

SURFACE ROUGHNESS

CONTRACT NO.

DRAWN B. GODIKER

CHECKED

DESIGN

ENGINEER

PROJECT

RELEASE

DESIGN APPROVAL

DESIGN APPROVAL

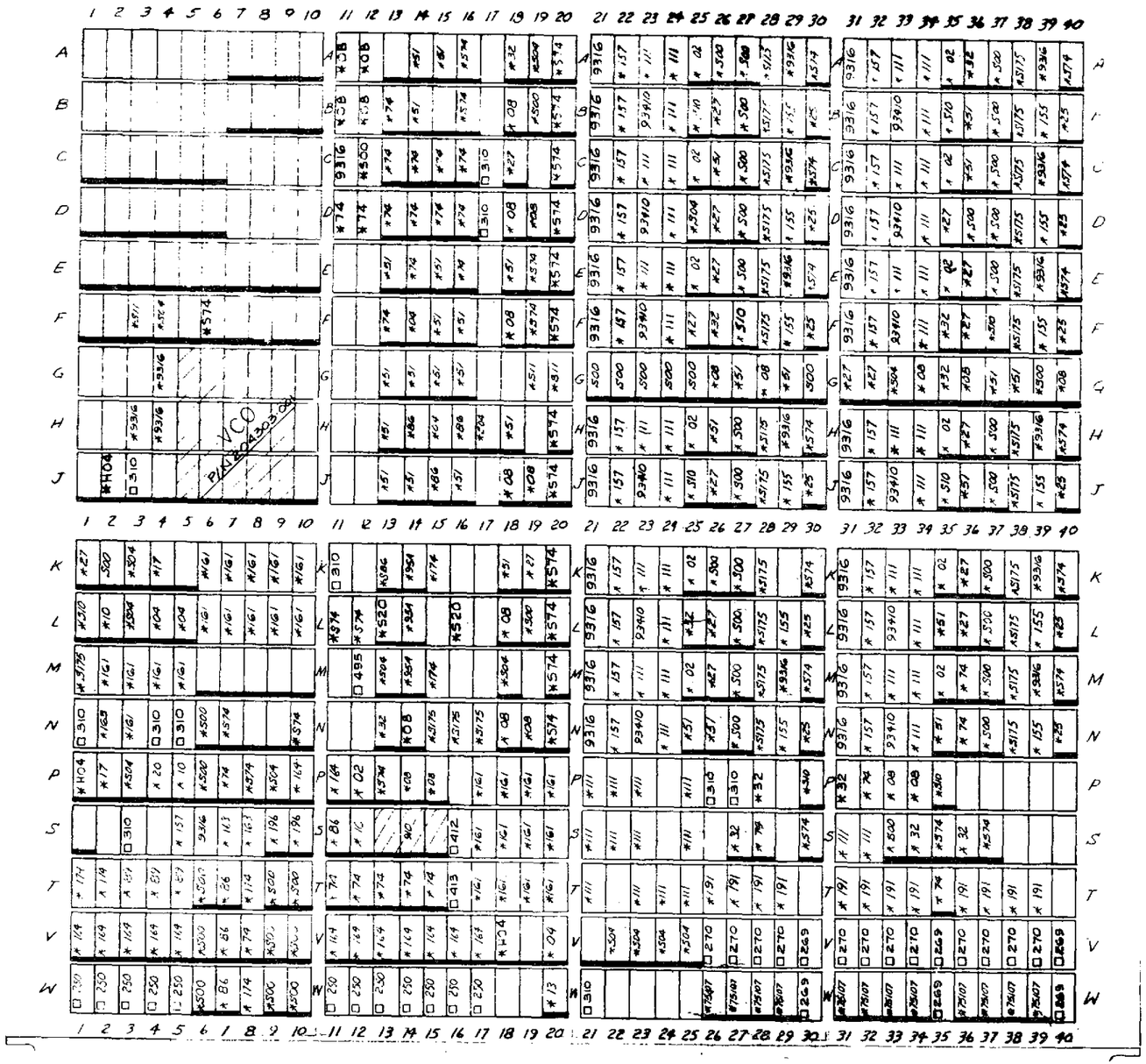
LEACH CORPORATION
717 NORTH CONEY AVE.
CONTROLS DIVISION
AZUSA, CALIFORNIA

DISCRETE PLATFORM, PHASE EQUALIZER

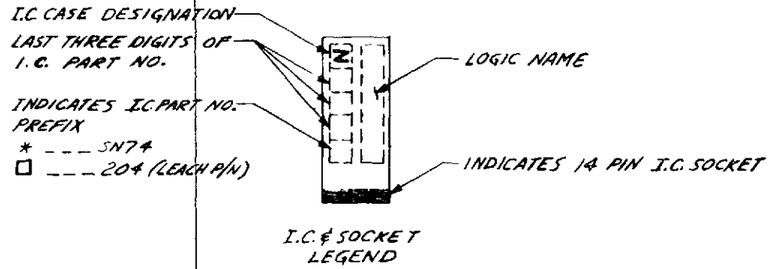
SIZE	CODE IDENT NO.	DWG NO.
C	96261	204250

SCALE 4/1 LEVEL: 0 SHEET 1 OF 1

FOLDOUT FRAME



FOLDOUT FRAME

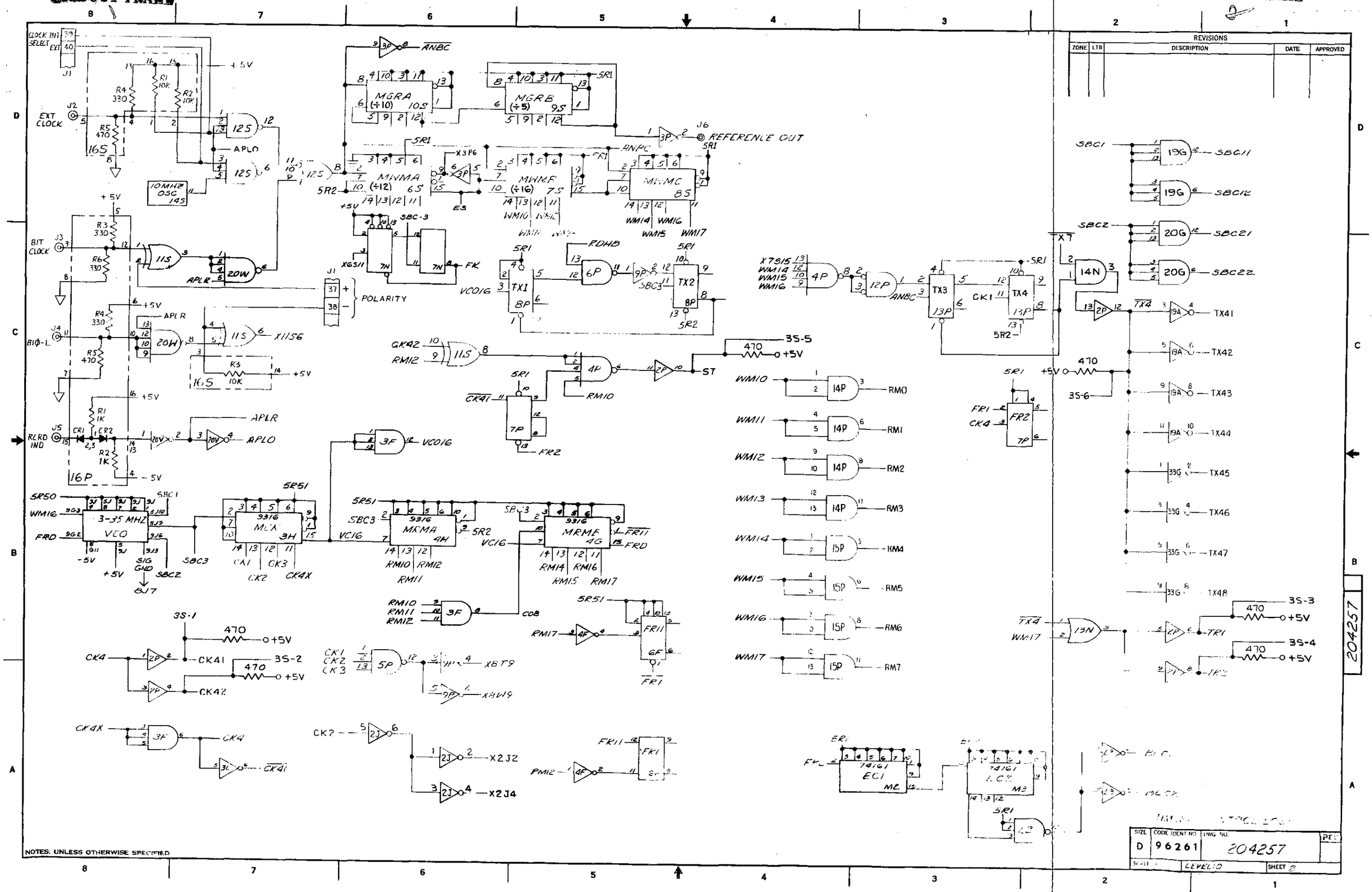


FOR I C IDENTIFICATION
SEE PL204274
LOGIC SCHEMATIC
DWG NO. 204257

SHT 1 OF 20

FOLDOUT FRAME

FOLDOUT FRAME



NOTES: UNLESS OTHERWISE SPECIFIED

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

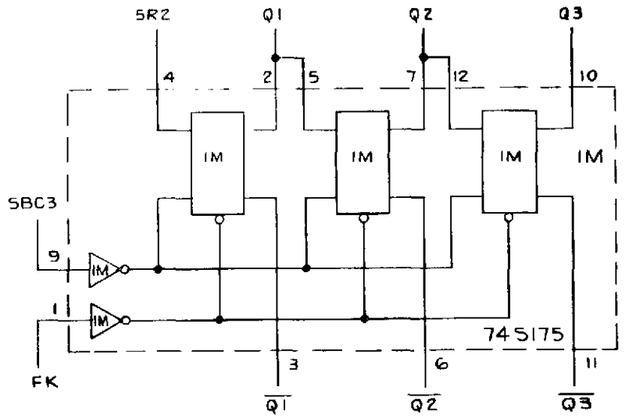
SIZE	CODE IDENT NO	DWG NO.	REV
D	96261	204257	
SCALE	LEVEL 0	SHEET 2	

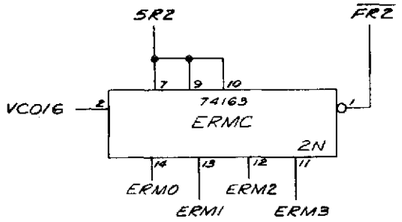
204257

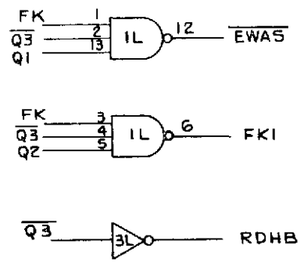
FOLDOUT FRAME

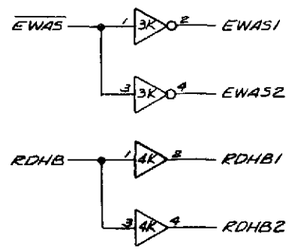
FOLDOUT FRAME

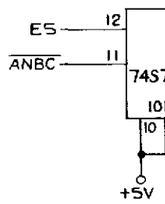
REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

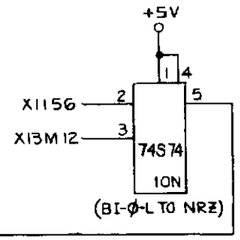


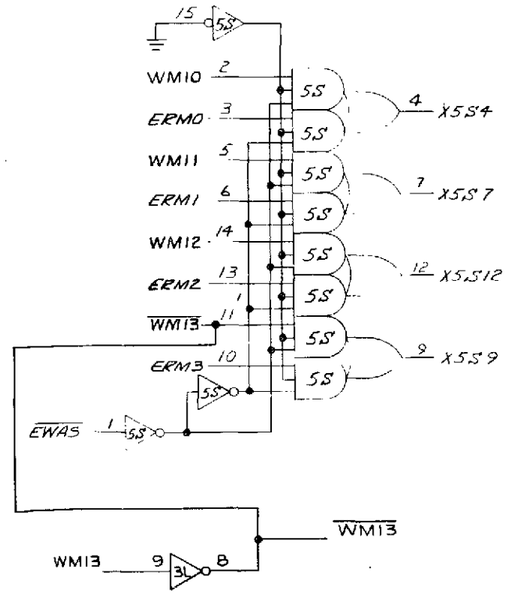


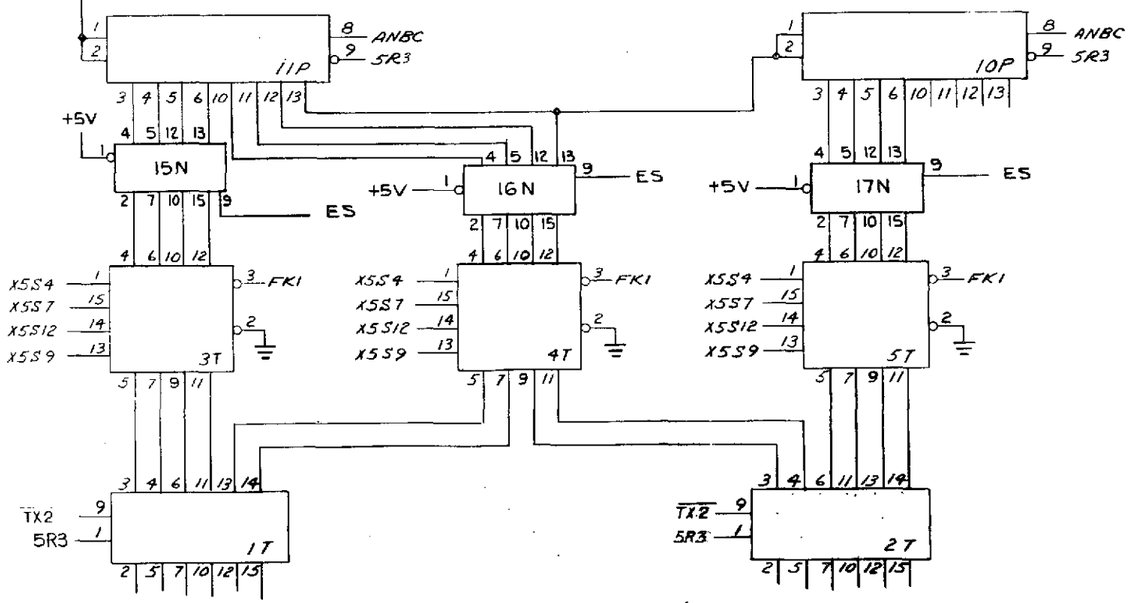


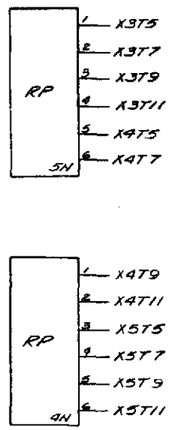












SERIAL TO PARALLEL CONVERTER

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204257	
SCALE	LEVEL:0	SHEET 3	

204257

FOLDOUT FRAME

FOLDOUT FRAME

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

CK41

XIT2 (NRZ)

XIT5 (NRZ)

XIT7 (NRZ)

XIT10 (NRZ)

XIT12 (NRZ)

XIT15 (NRZ)

2X BIT CLK XBT9

FRIA2

FR1

FR2

6N

(SYNC TOGGLE) ST

(4X BIT CLK) X2J2

DBL DENS

74164 1V

204250 1W

74164 2V

204250 2W

74164 3V

204250 3W

74164 4V

204250 4W

74164 5V

204250 5W

74164 11V

204250 11W

SR4

+5

J7 CH A OUT

J8 CH B OUT

J9 CH C OUT

J10 CH D OUT

J11 CH E OUT

J12 CH F OUT

CK42

X2T2 (NRZ)

X2T5 (NRZ)

X2T7 (NRZ)

X2T10 (NRZ)

X2T12 (NRZ)

X2T15 (NRZ)

2X BIT CLK X8W9

FRIA2

(SYNC TOGGLE) ST

(4X BIT CLK) X2J4

74164 12V

204250 12W

74164 13V

204250 13W

74164 14V

204250 14W

74164 15V

204250 15W

74164 16V

204250 16W

74164 17V

204250 17W

18V

J13 CH G OUT

J14 CH H OUT

J15 CH J OUT

J16 CH K OUT

J17 CH L OUT

J18 CH M OUT

204257

DOUBLE DENSITY ENCODER

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204257	
SCALE —	LEVEL: 0	SHEET 4	

FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

SR5 X26W4 PB DBL.DENS FT1A FT2A FT3A

PB DBL.DENS X22V2

SBC1 SBC2 21G TC2A TC1A

74S175 FT3A FT4A 28A A1Y0 A1Y1 A1Y2 FA1A FA2A FA3A

SR5 FT4A 19F TC2.1 SR6

FA3A FA5A FB3A FB2A 27A 26A 7451 18E

FA6A FA4A FB3A 26B FA7A 27A X27A11 FB1A 24A TC2A THREE'S PARITY

FA3A FB3A 26A FA4A 18A FA7A FB2A 25B TC2A FA5A

FA4A FB2A FA3A 26B FB3A 24B TC2A

FA3A FA5A FA6A 26B FB3A 25A A2Y0 SYNC. DET.

FA5A FB1A FA1A FB1A 7451 14A

X27A11 FA2A FB1A 25A 18A FB4A 24B TC2A NRZ P/B DATA

SR5 FA1A FA3A FA6A FA7A 30B FA4A FA4A 7451 14A FB5A 23A TC2A X14A6 P/B CLK

FA2A FA5A FA7A 26D SR6

BEC1 74161 4M 4L

SR5 TC1A 9316 21A X14A6 AM0 AM1 AM2 AM3 SYNCA

ADM5 ADM7 ADM4 ADM6 9316 21B TC1A X25A13 LOAD SR5 CARRY X21B15

SYNC A 25D

FB4A SR5 AM0 RM0 AM1 RM1 AM2 RM2 AM3 RM3 74157 22A AM4 RM4 AM5 RM5 AM6 RM6 AM7 RM7 71457 22B 93410 23B X23B11 DATA OUTPUT

X23B11 470Ω +5V 26 P1

EWASI WEA

SR5 FT3A FT4A BC5A 23A TC2A 9316 29A SR6 BC1A BC2A BC3A BC4A SR5

74155 29B BC4A BC5A FT3A BC1A BC2A BC3A 27F A1Y0 A1Y1 A1Y2 A1Y3 A2Y0 A2Y1 A2Y2 A2Y3

TFRR SR5 28P 34G X34G3 19E X21B15 SYNC A TX41

FBIA 74S175 FA4A 28B A2Y1 FA5A 28B A2Y2 FA6A 28B A2Y3 FA7A 28B TC2A SR5 TWO THREE FOUR

FA6A FB1A FB2A FB3A 30B SYNC A

X34G3 SYNCA 25A X25A13 LOAD

AM4 TX41 AM5 AM6 18B ADM4 ADM5 ADM6

TR1 SYNCA AM7 26A ADM7

FB5A FB3A 19B

SR5 74S14 20A RDHB1 19D 74S74 TC1A WEA

DECODER, CHANNEL A

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204257	
SCALE		LEVEL: 0	SHEET 5

204257

FOLDOUT FRAME

FOLDOUT FRAME

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE	APPROVED

74S175

SYNC. DET.

THREE'S PARITY

TWO

THREE

FOUR

SYNC B

LOAD

DATA OUTPUT

DECODER, CHANNEL B

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204257	
SCALE		LEVEL: 0	SHEET 6

204257

FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

Reproduced from best available copy.

5R9 X28W4 PB DBL.DENS $\overline{\text{PB DBL.DENS}}$ X22V10 $\overline{\text{FT3C}}$ FT1C FT2C 30E 27C

74S175 FT3C 28E FA1C 28E FA2C 28E FA3C 28E C1Y0 C1Y1 C1Y2 28E

5R9 FT4C 16A 5R10 TC2C

SBC1 SBC2 22G TC2C TC1C 28E 5R9 28E

5R9 TC2C 9316 29E SR10 BC1C BC2C BC3C BC4C 5R9 FT4C FT3C BC5C 23E 5R9

74155 29F BC4C BC5C $\overline{\text{FT3C}}$ BC1C BC2C BC3C 27F C1Y0 C1Y1 C1Y2 C1Y3 C2Y0 C2Y1 C2Y2 C2Y3

5R9 TFRR 28P 34G X34G8 X21F15 TX42 3CM $\overline{\text{SYNC C}}$

74S175 FB1C FA4C 28F C2Y1 FA5C 28F C2Y2 FA6C 28F C2Y3 FA7C 28F TC2C 28F 5R9 28F TWO THREE FOUR

FA5C FB1C FA6C 27E FB2C 25E FA6C FA4C 27E FB3C 25F FA7C FA3C 27E X27E11 FA3C FB3C 27D FA4C FB3C 26F FA6C 27D FA5C FB2C 25B FA7C TC2C FB2C 24E 5R9 FA4C FB2C FA3C 25F FB3C TC2C 24F FB3C FA3 FA5C FA6C 25F FB3C 25E C240 5R9 THREE'S PARITY SYNC. DET.

FA5C FB1C FA1C FB1C 7451 26C 5R9 FA2C FB1C X27E11 25E 26F NRZ P/B DATA FB4C TC2C 24F 5R10 5R9 FA1C FA3C FA6C FA7C 30F FA4C FA4C 7451 26C X26C6 5R9 FA2C FA5C FA7C 18C FB5C TC2C 23E P/B CLK 5R10

CM4 TX42 CM5 CM6 18F CDM4 18F CDM5 18F CDM6

TR1 27D CDM7 SYNCC CM7 27J

5R9 BECI 74161 6L 4L J1 RRC

5R9 TC1C 74163 21E CM0 CM1 CM2 CM3 CDM4 CDM5 CDM6 CDM7 TC1C 74163 21F CM4 CM5 CM6 CM7 X25E13 LOAD 5R9 CARRY X21F15 SYNC C 25D $\overline{\text{SYNC C}}$

FB4C 5R9 CM0 RM0 CM1 RM1 CM2 RM2 CM3 RM3 74157 22E 93410 X23F11 DATA OUTPUT CM4 RM4 CM5 RM5 CM6 RM6 CM7 RM7 74157 22F 23F X23F 11 470Ω +5V 26P3 E WAS1 10 $\overline{\text{WEC}}$

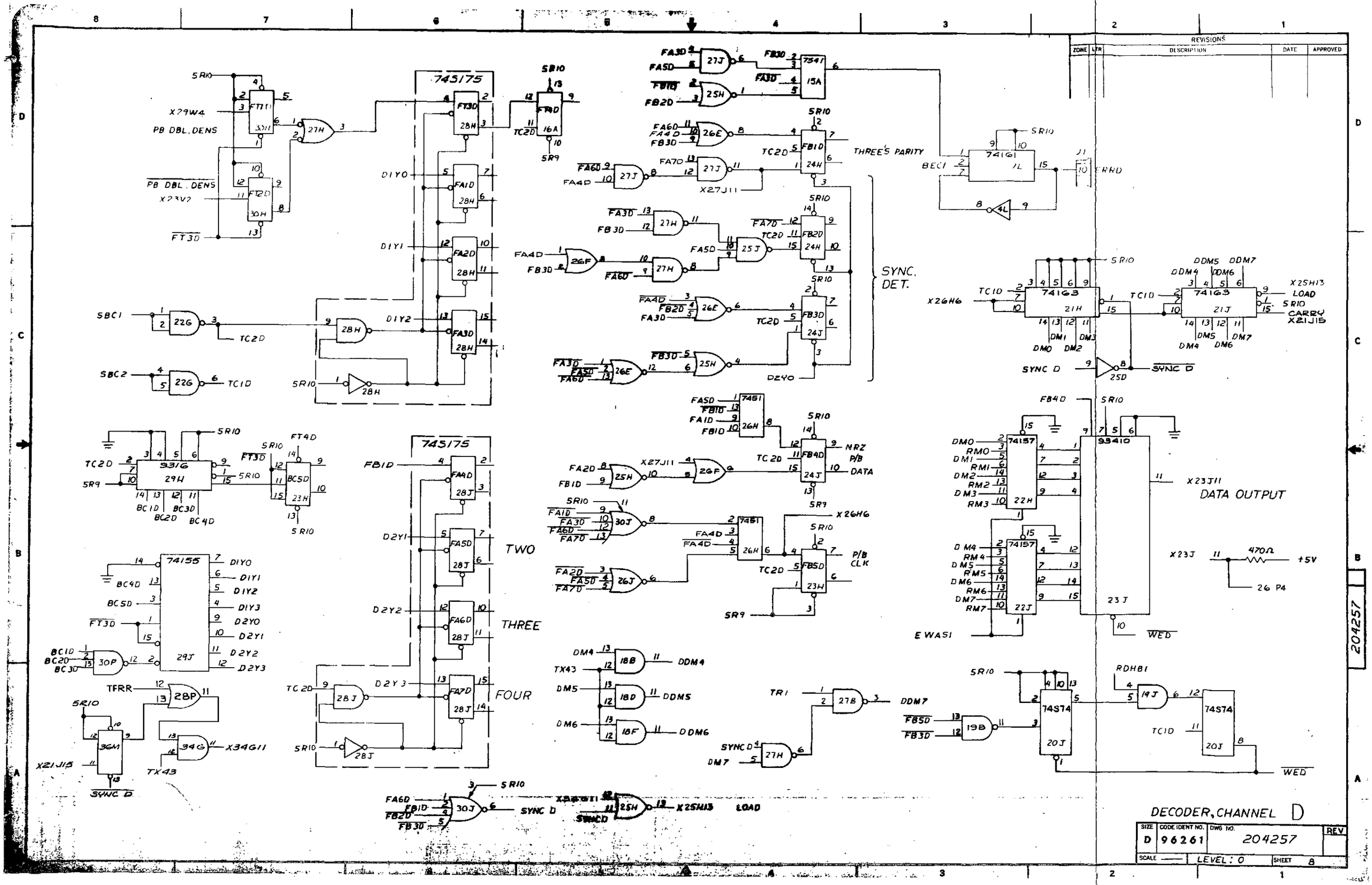
5R9 FB5C FB3C 19B 74S74 20E RDHB1 19J TC1C 74S74 20E $\overline{\text{WEC}}$

FA6C FB1C FB2C FB3C 30F SYNC C X34G8 X25E13 LOAD SYNC C 25E

DECODER, CHANNEL C

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204257	
SCALE —	LEVEL: 0	SHEET 7	

204257

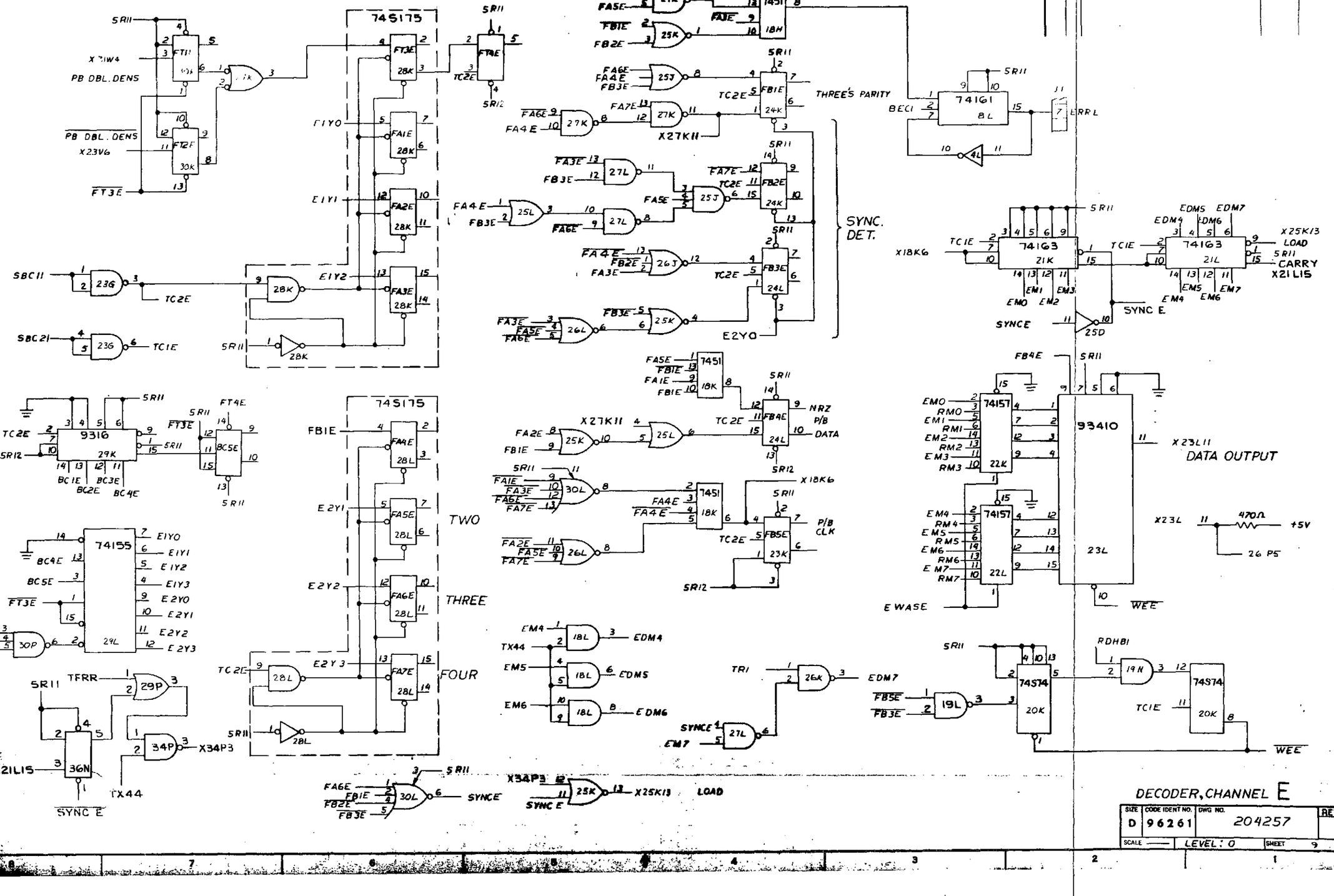


REVISIONS
ZONE
LTR
DESCRIPTION
DATE
APPROVED
74S175
74S175
THREE'S PARITY
SYNC. DET.
TWO
THREE
FOUR
DATA OUTPUT
PB DBL. DENS
SYNC D
LOAD
+5V
26 P4
DECODER, CHANNEL D
SIZE
D
CODE IDENT NO.
96261
DWG NO.
204257
REV
SCALE
LEVEL: 0
SHEET 8
204257

FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



DECODER, CHANNEL E

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204257	
SCALE		LEVEL: 0	SHEET 9

204257

FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

DECODER, CHANNEL F

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204257	
SCALE		LEVEL: 0	SHEET 16

204257

FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

SYNC. DET.

THREE'S PARITY

TWO

THREE

FOUR

DATA OUTPUT

LOAD

DECODER, CHANNEL G

SIZE	CODE IDENT NO	DWG NO.	REV
D	96261	204257	
SCALE	LEVEL: 0	SHEET 11	

204257

FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS			
ZONE	DESCRIPTION	DATE	APPROVED

SYNC. DET.

THREE'S PARITY

TWO

THREE

FOUR

DATA OUTPUT

LOAD

DECODER, CHANNEL H

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204257	
SCALE		LEVEL: 0	SHEET 12

204257

FOLDOUT FRAME

FOLDOUT FRAME

REVISIONS			
ZONE	DESCRIPTION	DATE	APPROVED

SR
X 15W4
PB DBL. DENS
PB DBL. DENS
X 24V10
FT3J
SBC12
SBC22
TC2J
TC1J
SR15
74S175
FT1
FT2
FT3J
FT4J
J1Y0
J1Y1
J1Y2
J1Y3
FA1J
FA2J
FA3J
FA4J
J2Y0
J2Y1
J2Y2
J2Y3
74155
BC4J
BC5J
BC1J
BC2J
BC3J
TFRR
SYNC J
X31F15
TX46
X33P3
X35E13
LOAD
SYNC J
FA3J
FA5J
FB1J
FB2J
FB3J
FA6J
FA4J
FA7J
X37E11
THREE'S PARITY
SYNC. DET.
J2Y0
FA5J
FB1J
FA1J
FB1J
NRZ P/B DATA
FA2J
FB1J
X37E11
FA6J
FA4J
FB3J
FA7J
FA2J
FA5J
FA7J
X2766
FA4J
FA4J
FB5J
TC2J
P/B CLK
SR16
TWO
THREE
FOUR
FA6J
FB1J
FB2J
FB3J
SYNC J
JM4
TX46
JM5
JM6
JDM4
JDM5
JDM6
TR 2
SYNC J
JM7
JDM7
FB5J
FB3J
74161
7K
BEC2
SL
J1
SR15
74163
TC1J
X2766
JDM4
JDM5
JDM6
JDM7
JM0
JM1
JM2
JM3
JM4
JM5
JM6
JM7
SYNC H
SYNC J
X35E13
LOAD
SR15
CARRY
X31F15
FB4J
93410
74157
RM0
RM1
RM2
RM3
RM4
RM5
RM6
RM7
EWAS2
X33F11
DATA OUTPUT
X33F
470Ω
+5V
27 P3
WEJ
RDHB2
74S74
TC2J
WEJ

DECODER, CHANNEL J

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204257	
SCALE ——	LEVEL: 0	SHEET 13	

204257

FOLDOUT FRAME

FOLDOUT FRAME 2

REVISIONS			
ZONE LTR	DESCRIPTION	DATE	APPROVED

SBC12 256 TC2K

SBC22 256 TC1K

PB DBL.DENS

PB DBL.DENS

X25V2

FT3K

5R16

74S175

FT1K FT2K FT3K FT4K

K1Y0 K1Y1 K1Y2 K1Y3 K2Y0 K2Y1 K2Y2 K2Y3

5R15 9316 BC1K BC2K BC3K BC4K BC5K

74155

TFRR 31P 28S 33P X33P6 TX47 X31J15 SYNC K

TWO THREE FOUR

FA3K FA5K FB1K FB2K 37H 35H 296

FA6K FA4K FB3K 36E FA7K 37H X37H11

FA3K FB3K 37B FA5K 35J FA4K FB3K 35F FA6K 37J

FA4K FB2K FA3K 36E FB3K 34J TC2K FA3K FA5K FA6K 36E FB3K 35H K2Y0

FA5K FB1K FA1K FB1K 74S51 36J FA2K FB1K 35H X37H11 35F FB4K 34J NRZ P/B DATA

FA1K FA3K FA6K FA7K 40J FA4K FA4K 74S51 36J FB5K 33H P/B CLK

FA2K FA5K FA7K 36H

KM4 TX47 KM5 KM6 366 KDM4 KDM5 KDM6

TR2 370 KDM7 SYNC K 37J KM7

FB5K FB3K 39G

FA6K FB1K FB2K FB3K 40J SYNC K

X33P6 35H X35H13 LOAD SYNC K

THREE'S PARITY

BEC2 74161 8K SL RRK

SYNC. DET.

TC1K X36J6 74163 31H KM0 KM1 KM2 KM3

KDM4 KDM5 KDM6 KDM7 74163 31J KM4 KM5 KM6 KM7 X35H13 LOAD 5R16 CARRY X31J15

SYNC K 18M SYNC C

FB4K 5R16 93410 74157 32H 32J 33J KM0 RM0 KM1 RM1 KM2 RM2 KM3 RM3 KM4 RM4 KM5 RM5 KM6 RM6 KM7 RM7 E WAS 2

X33J11 DATA OUTPUT

X33J 470Ω +5V 27 P4

WEK

5R16 74S74 20H RDHB2 19J TC2K WEK

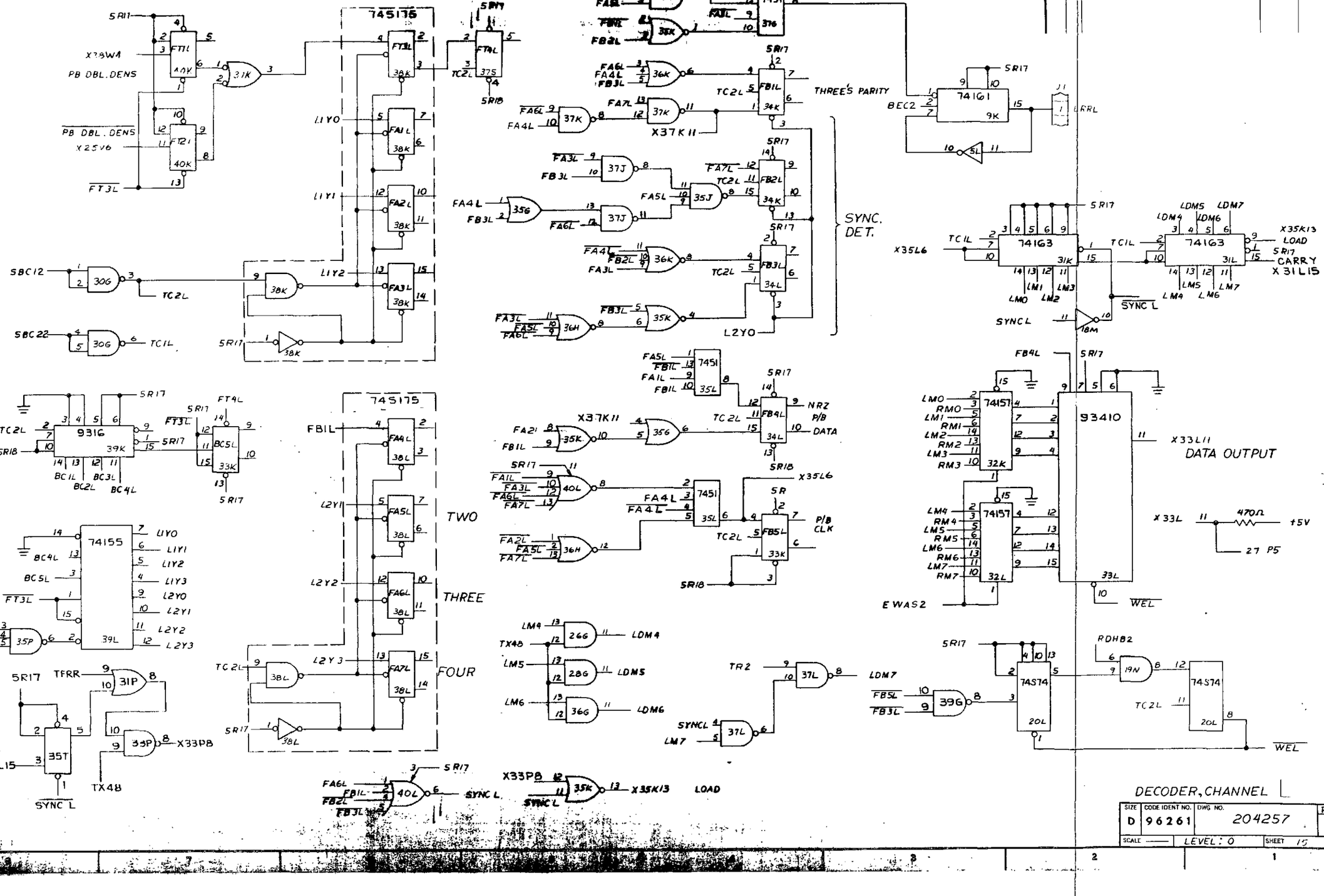
DECODER, CHANNEL K

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204257	
SCALE ——	LEVEL: 0	SHEET 14	

204257

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



DECODER, CHANNEL

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204257	
SCALE		LEVEL: 0	SHEET 15

204257

FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

745175

SR18 FT1M PB DBL. DENS X25V10A

PB DBL. DENS X25V10 FT2M 40M FT3M

FT3M FT4M 38M FT4M 37S TC2M SR17

M1Y0 M1Y1 M1Y2 FA1M FA2M FA3M 38M

SBC12 30G TC2M SBC22 30G TC1

SR18 38M

SR18 FT3M 9316 39M SR17 BC1M BC2M BC3M BC4M BC5M 33M

74155 39N M1Y0 M1Y1 M1Y2 M1Y3 M2Y0 M2Y1 M2Y2 M2Y3 BC1M BC2M BC3M 35P

SR18 TFRR 33P 33P X33P11 X31N15 SYNC M 1X48

745175

FB1M FA4M 38N M2Y1 FA5M 38N M2Y2 FA6M 38N M2Y3 FA7M 38N TC2M 38N SR18 38M

TWO THREE FOUR

FA6M FB1M FB2M FB3M 40N SYNCM

FA3M FA5M FA6M 36L FB3M 35M X33P11 SYNCM X35M13 LOAD

FA3M FA5M 37M FB3M FB2M 7451 FA3M 37G

FB1M FB2M 37M

FA6M FA4M FB3M 36L FA7M 37M X37M11 FB1M 34M TC2M THREE'S PARITY

FA3M FB3M 37N FA4M FB3M 35G FA6M 37N FA5M FA7M TC2M FB2M 34M

FA4M FB2M FA3M 36L FB3M 34N TC2M M2Y0 SYNC. DET.

FA5M FB1M FA1M FB1M 7451 38G

FA2M FB1M 35M X37M11 356 TC2M FB4M 34N NRZ P/B DATA SR17

SR18 FA1M FA3M FA6M FA7M 40N FA4M FA4M 7451 38G FB5M 33M P/B CLK SR17 X38G6 SR

FA2M FA5M FA7M 36K

SR18 74161 10F BEC2 5L J1 LRRM

SR18 MDM4 MDM6 MDM5 MDM7 74163 3M TC1M TC1M X35M13 LOAD SR18 CARRY X31N15 X38G6 MM0 MM1 MM2 MM3 MM4 MM5 MM6 MM7 SYNC M 18M SYNC M

FB4M SR18 74157 32M 74157 32N 93410 33N MM0 RM0 MM1 RM1 MM2 RM2 MM3 RM3 MM4 RM4 MM5 RM5 MM6 RM6 MM7 RM7 X33N11 DATA OUTPUT EWAS2 WEM

X33N 470Ω +5V 27 P6

MM4 TX48 406 406 406 MDM4 MDM5 MDM6

TR2 37L MDM7 SYNCM MM7 37N

SR18 FB5M FB3M 39G 74S74 20M RDHB2 19N 74S74 20M TC2M WEM

DECODER, CHANNEL M

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204257	

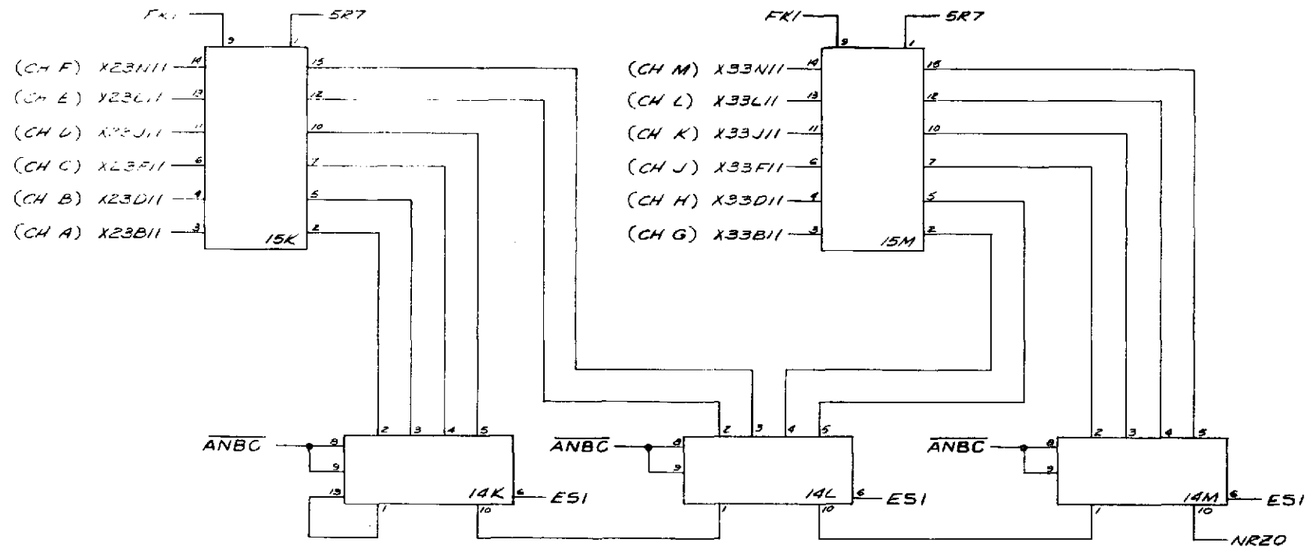
SCALE — LEVEL: 0 SHEET 16

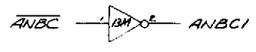
204257

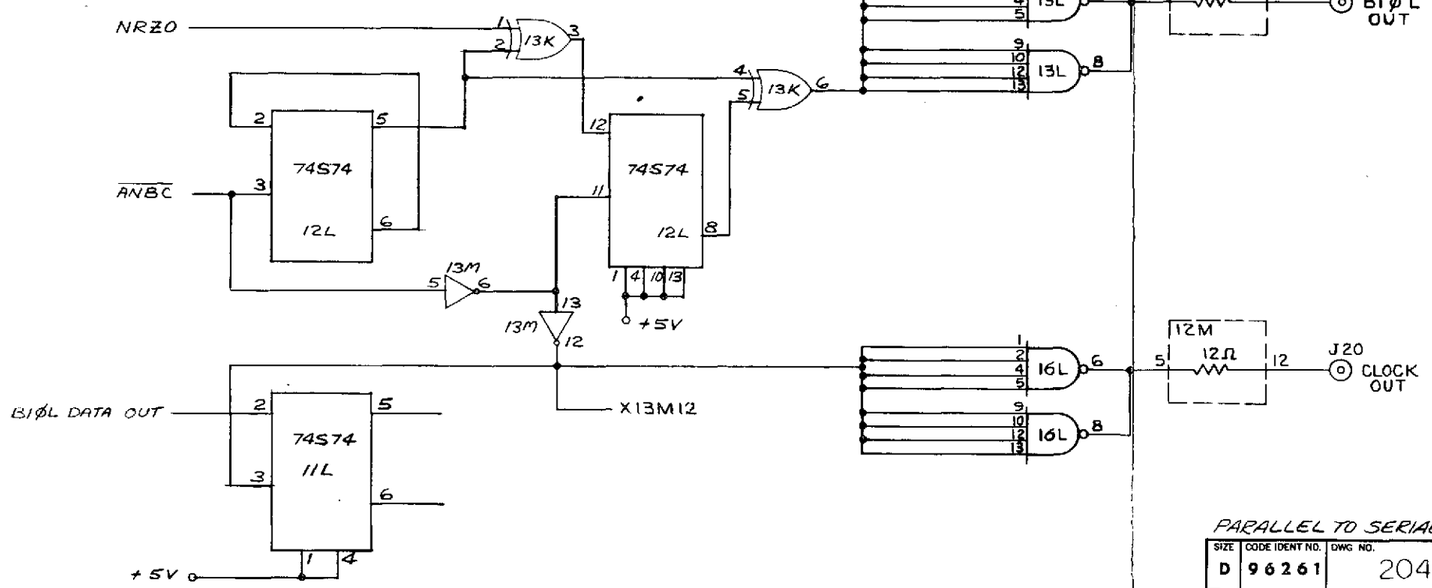
FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED







204257

PARALLEL TO SERIAL CONVERTER

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204257	
SCALE —	LEVEL:0	SHEET 17	

FOLDOUT FRAME

FOLDOUT FRAME

REVISIONS			
ZONE	DESCRIPTION	DATE	APPROVED

PLAYBACK CHAN A (PBA) J21 C1 10UF,6V

PLAYBACK CHAN B (PBB) J22 C2 10UF,6V

PLAYBACK CHAN C (PBC) J23 C3 10UF,6V

PLAYBACK CHAN D (PBD) J24 C4 10UF,6V

INPUT BUFFER CHANNEL A,B,C,D

SIZE	CODE IDENT NO.	DWG NO	REV
D	96261	204257	

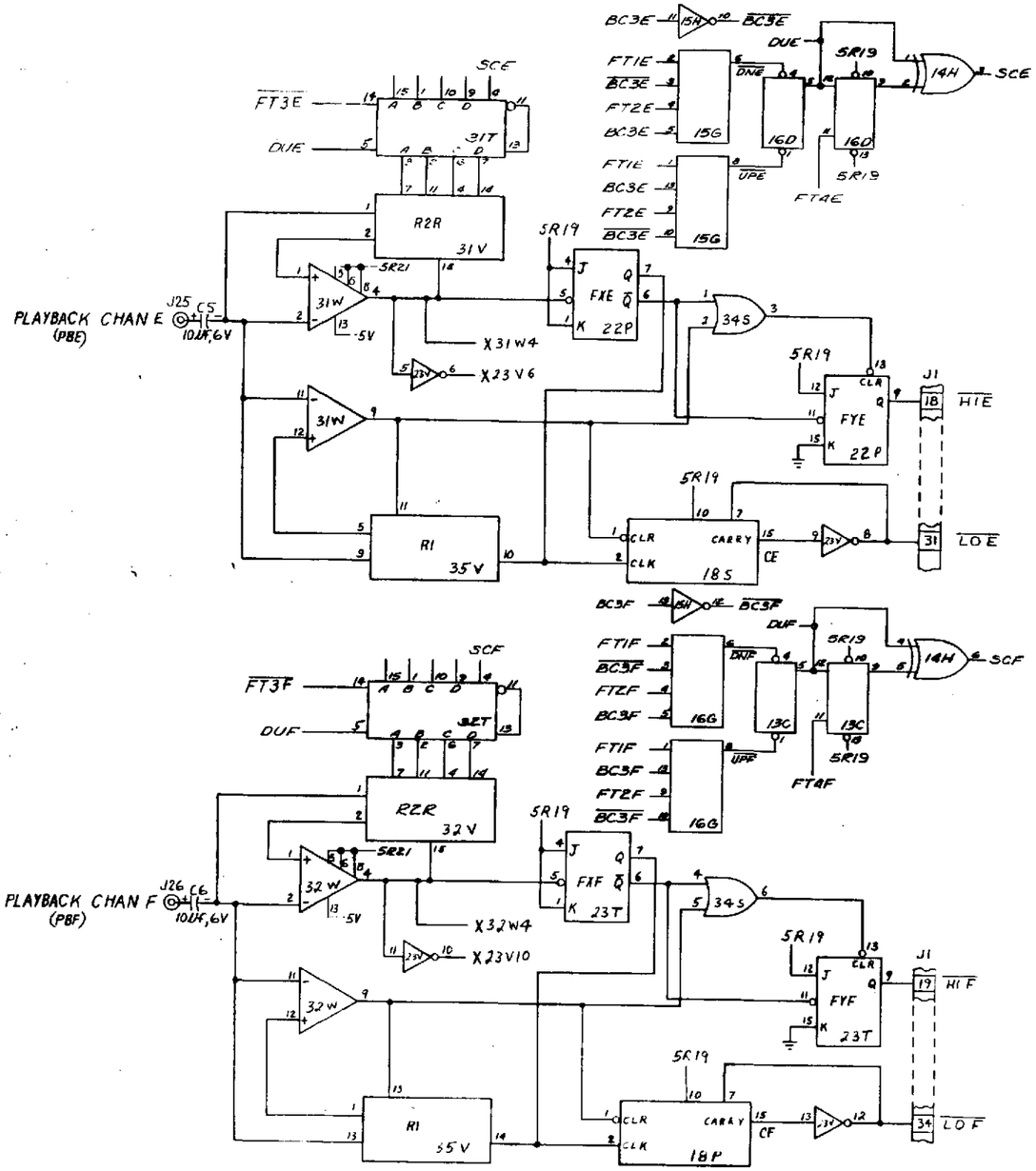
SCALE — LEVEL: 0 SHEET 18

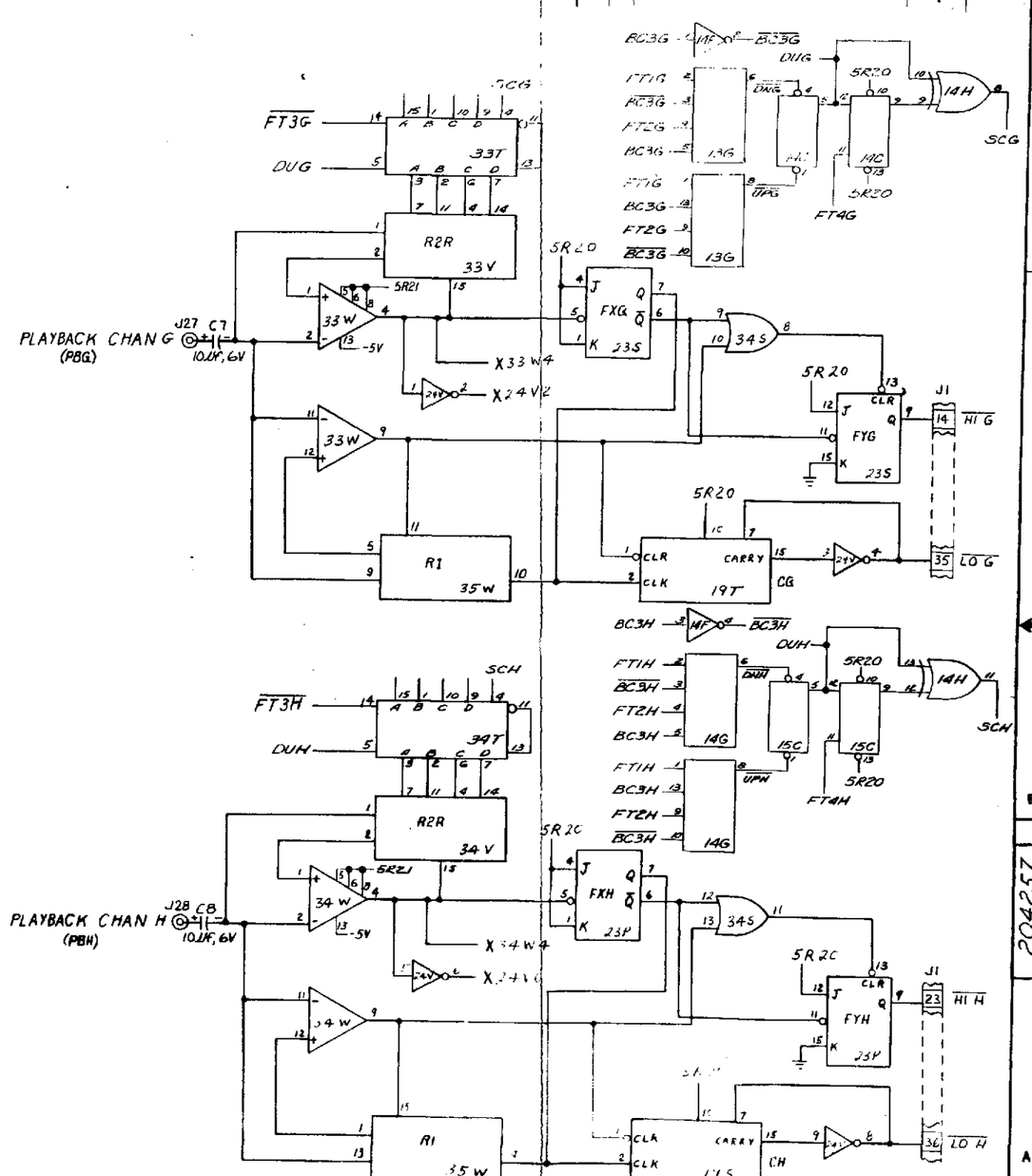
204257

FOLDOUT FRAME

FOLDOUT FRAME

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED





INPUT BUFFER CHANNEL :E,F,G,H;

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204257	
SCALE		LEVEL:0	SHEET 19

204257

FOLDOUT FRAME

FOLDOUT FRAME

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED

PLAYBACK CHAN J (PBJ)

PLAYBACK CHAN K (PBK)

PLAYBACK CHAN L (PBL)

PLAYBACK CHAN M (PBM)

INPUT BUFFER CHANNEL J,K,L,M

SIZE	CODE IDENT NO	DWG NO	REV
D	96261	204257	
SCALE —	LEVEL:0	SHEET 20	

204257

FOLDOUT FRAME

FOLDOUT FRAME

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

AM7
BM7
CM7
DM7
EM7
FM7
GM7
HM7
JM7
KM7
LM7
MM7
11A
11B
12A
12B
$\overline{CLRX}$

+5V
AM6
TX6 7474 12D
TX7 7474 12D
CK-1
11B
+5V
$\overline{TX4}$
TX5 7474 11D
12B
TFRR

+5V
WM11
$\overline{CLRX}$
9316 11C
12B
+5V
D Q 7474 12C
+5V
D Q 7474 12C
12B

$\overline{CLRX}$ WAVEFORM WHEN ALL 12 CHANNELS IN SYNC:

30-50% DUTY CYCLE

204257

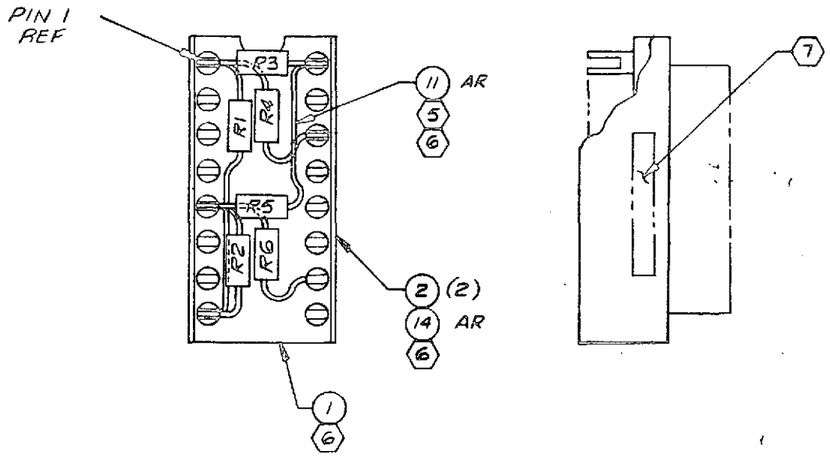
SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204257	
SCALE ----	LEVEL: 0	SHEET 21	

FOLDOUT FRAME

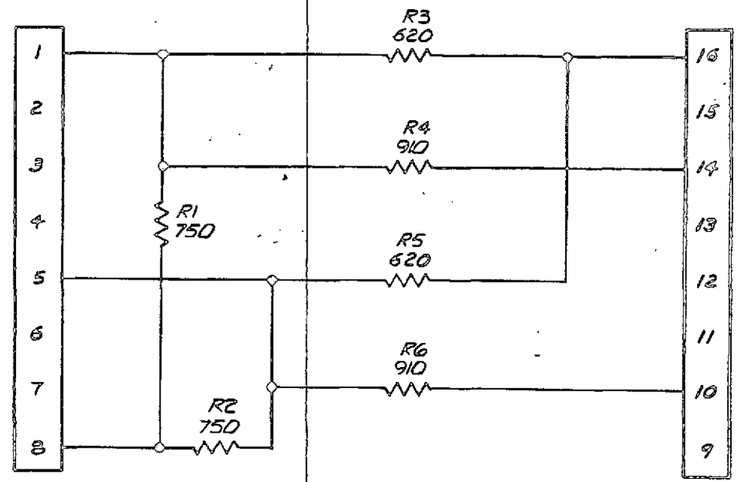
FOLDOUT FRAME

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



-001 SHOWN



SCHEMATIC DIAGRAM

FOR PARTS LIST SEE PL 204269-001

(7) MARK PER LEACH STD 201179-006 WITH 204269-001 APPROX WHERE SHOWN.

(6) AFTER ASSEMBLY OF ITEM NO.'S 4, 5, 6, & 11 TO ITEM NO. 1, BOND ITEM NO. 2 TO ITEM NO. 1 2 PLACES AS SHOWN, USING ITEM NO. 14.

(5) SLEEVE RESISTOR LEADS AND BUSS WIRE WITH ITEM NO. 11 WHERE APPLICABLE.

4 ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/8W.

3 REFERENCE DESIGNATIONS ARE ABBREVIATED: PREFIX WITH UNIT NO. AND APPLICABLE SUBASSEMBLY DESIGNATION.

2 FOR NEXT ASSEMBLY SEE APPLICATION BLOCK.

1 DO NOT SCALE DRAWING.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PARTS LIST

QTY N/A	QTY U/O	NEXT ASSEMBLY	USED ON
6	6	204274	HD-103
		APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCE

FRACTIONS ± | XX ± | ANGLES ± | XXX ±

MATERIAL

FINISH

SURFACE ROUGHNESS

CONTRACT NO:

DRAWN	H. Smith	12-26-78
CHECKED		
DESIGN		
ENGINEER		
PROJECT		
RELEASE		
DESIGN APPROVAL		
DESIGN APPROVAL		

LEACH CORPORATION
717 NORTH CONEY AVE. CONTROLS DIVISION AZUSA, CALIFORNIA

DISCRETE PLATFORM INPUT BIAS

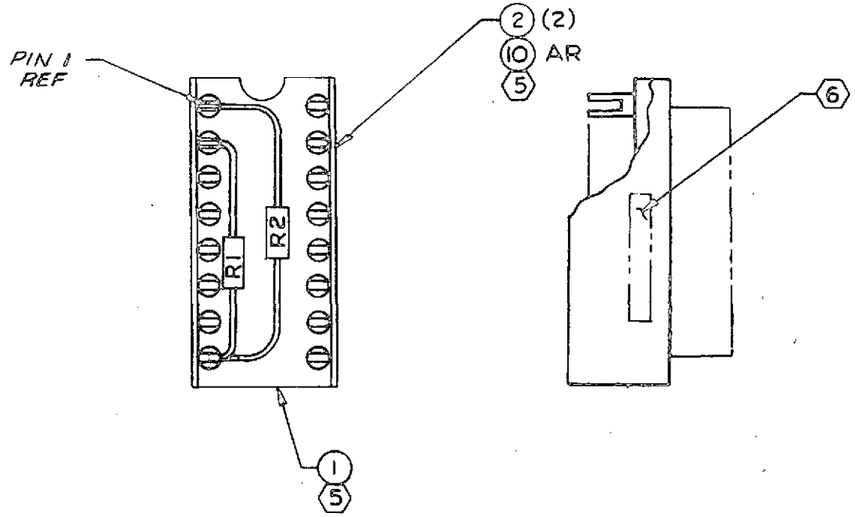
SIZE	CODE IDENT NO.	DWG NO.
C	96261	204269

SCALE 4/1 SHEET 1

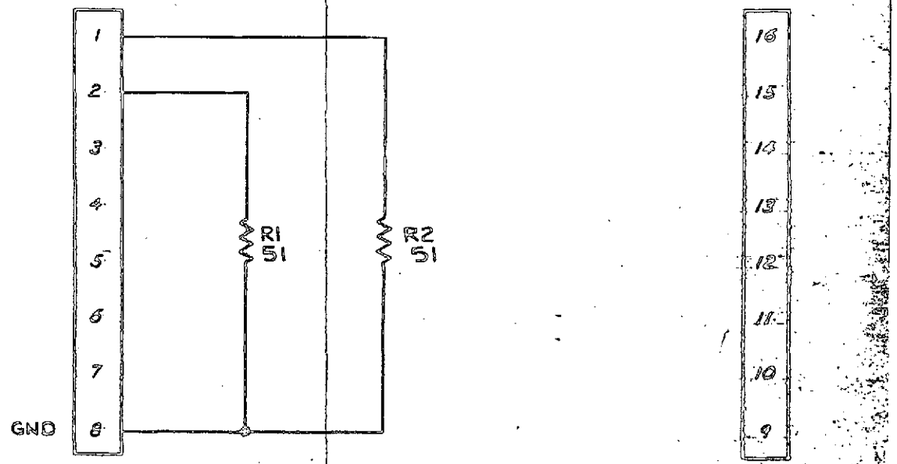
FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



-001 SHOWN



SCHEMATIC DIAGRAM

FOR PARTS LIST SEE PL 204270-001

6. MARK PER LEACH STD 201179-006 WITH 204270-001 APPROX WHERE SHOWN.
5. AFTER ASSEMBLY OF ITEM NO. 4 TO ITEM NO. 1 BOND ITEM NO. 2 TO ITEM NO. 1 2 PLACES AS SHOWN, USING ITEM NO. 10.
4. ALL RESISTOR VALUES ARE IN OHMS, ± 5%, 1/8 W
3. REFERENCE DESIGNATIONS ARE ABBREVIATED: PREFIX WITH UNIT NO. AND APPLICABLE SUBASSEMBLY DESIGNATION.
2. FOR NEXT ASSEMBLY SEE APPLICATION BLOCK.
1. DO NOT SCALE DRAWING.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PARTS LIST

QTY N/A	QTY U/O	NEXT ASSEMBLY	USED ON
12	12	204274	HD-108
APPLICATION			

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ± .XX ±
ANGLES ± .XXX ±
MATERIAL
FINISH
SURFACE ROUGHNESS √

CONTRACT NO.
DRAWN 7-25-75
CHECKED
DESIGN
ENGINEER
PROJECT
RELEASE
DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
717 NORTH COney AVE. CONTROLS DIVISION AZUSA, CALIFORNIA

DISCRETE PLATFORM, R-2R LADDER

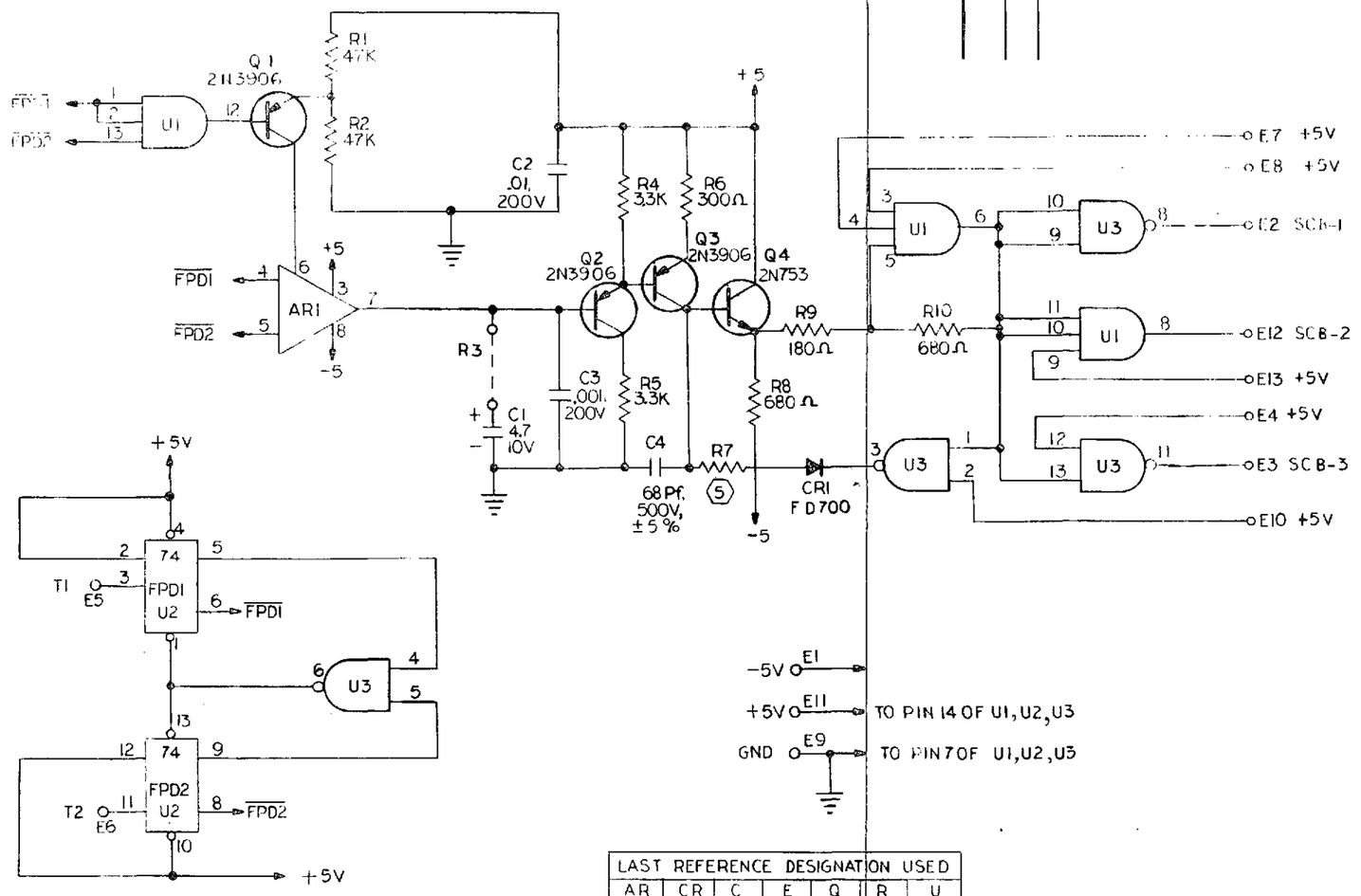
SIZE	CODE IDENT NO.	DWG NO.
C	96261	204270

SCALE 4/1 LEVEL 10 SHEET 1 OF 2

FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS			
ZONE	LTR	DESCRIPTION	DATE



LAST REFERENCE DESIGNATION USED						
AR	CR	C	E	Q	R	U
1	1	4	13	4	10	3

6. INTEGRATED CIRCUIT NO. / PART NO. / VENDOR CODE IDENT

U1	SN74S11N	01295
U2	MC7474L	04713
U3	9S0059/74S00	07263
AR1	CA3060 E	86684

5. COMPONENT IS SELECT IN TEST, APPROX VALUE 33Ω.
4. ALL CAPACITOR VALUES ARE IN MICROFARADS, ± 10%.
3. ALL RESISTOR VALUES ARE IN OHMS, ± 5%, 1/4W.
2. REFERENCE DESIGNATIONS ARE ABBREVIATED: PREFIX WITH UNIT NO. AND APPLICABLE SUBASSEMBLY DESIGNATION.
1. FOR ASSEMBLY SEE APPLICATION BLOCK.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATI
			LIST OF MATERIALS OR PARTS LIST		

QTY N/A	QTY U/O	NEXT ASSEMBLY	USED ON
REF	REF	204303	HD-103
		APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ± XX ±
ANGLES ± XXX ±
MATERIAL
FINISH
SURFACE ROUGHNESS

CONTRACT NO.

DRAWN	R. ALVERSON	NOV 16 '72
CHECKED		
DESIGN		
ENGINEER		
PROJECT		
RELEASE		

DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
717 NORTH CONEY AVE. AZUSA, CA
CONTROLS DIV

PHASE LOCKED VCO SCHEMATIC

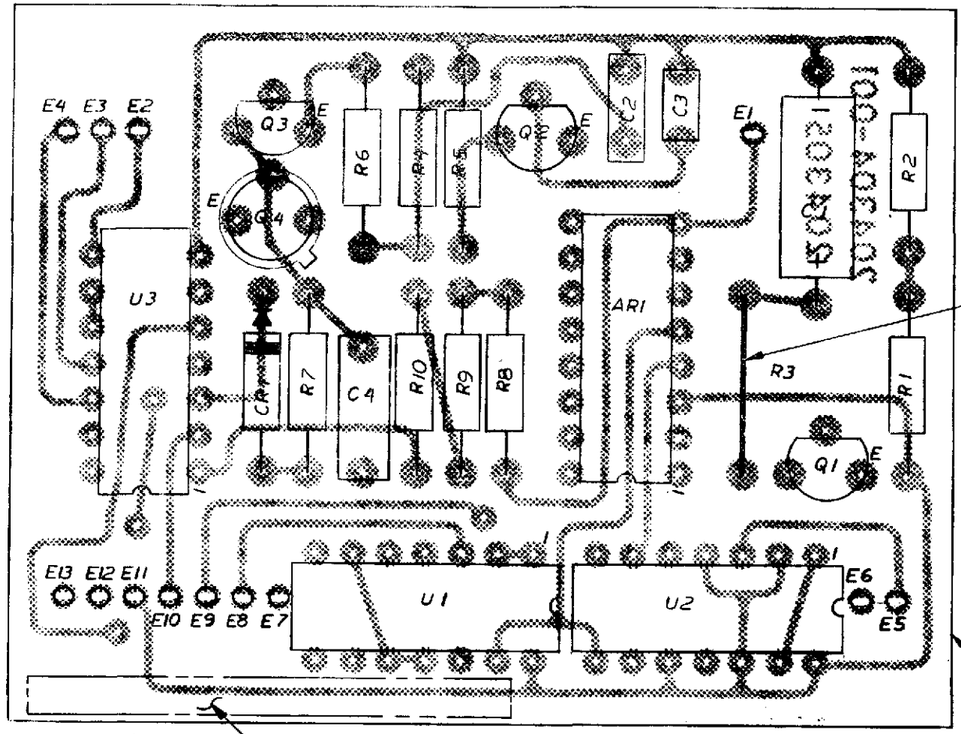
SIZE	CODE IDENT NO.	DWG NO.
C	96261	204302

SCALE NONE | LEVEL: 0 | SHEET 1

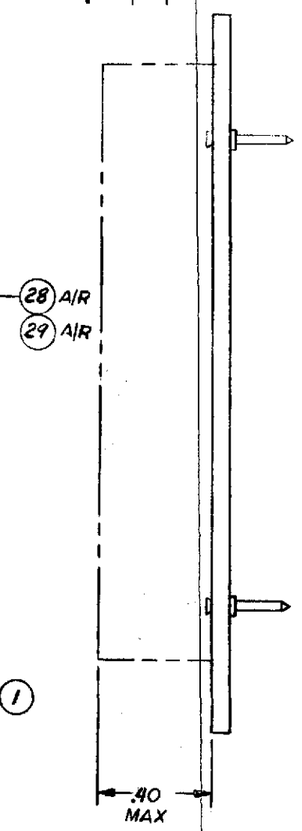
FOLDOUT FRAME 1

FOLDOUT FRAME 2

ZONE	LTR	REVISIONS DESCRIPTION	DATE	APPROVED



-001 SHOWN



7. MARK PER LEACH STD 201179-006 WITH 204303-001 AND SERIAL NO. USING NONCONDUCTIVE WHITE INK, APPROX WHERE SHOWN.
6. SOLDER 360° AROUND ALL TERMINALS WHERE TERMINAL CONTACTS PRINTED WIRING.
5. MINIMUM .005 SOLDER WETTING REQUIRED OUTWARD FROM HOLE DIAMETER WHERE TWO SIDED CIRCUITRY EXISTS.
4. FABRICATION AND ASSEMBLY SHALL CONFORM TO MIL-STD-275.
3. FOR NEXT ASSEMBLY SEE APPLICATION BLOCK. FOR SCHEMATIC SEE DWG NO. 204302.
2. REFERENCE DESIGNATIONS ARE ABBREVIATED: PREFIX WITH APPLICABLE UNIT NO. AND SUBASSEMBLY DESIGNATION.
1. DO NOT SCALE DRAWING.

NOTES: UNLESS OTHERWISE SPECIFIED

FOR PARTS LIST SEE PL 204303-001

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PARTS LIST

QTY N/A	QTY U/O	NEXT ASSEMBLY	USED ON
1	1	204274	HD-103
		APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ± .XX ±
ANGLES ± .XXX ±
MATERIAL
FINISH
SURFACE ROUGHNESS √

CONTRACT NO.
DRAWN 1-3-73
CHECKED
DESIGN
ENGINEER
PROJECT
RELEASE
DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
717 NORTH CONEY AVE
CONTROLS DIVISION
AZUSA, CALIFORNIA

CIRCUIT CARD ASSEMBLY, PHASE LOCKED VCO

SIZE	CODE IDENT NO.	DWG NO.	REV
C	96261	204303	

SCALE 4-1 | LEVEL: 0 | SHEET 1 OF 1

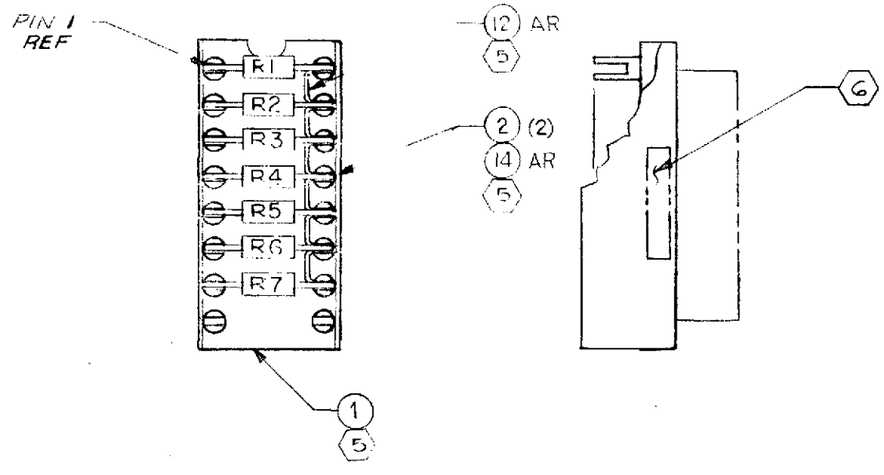
204303

FOLDOUT FRAME

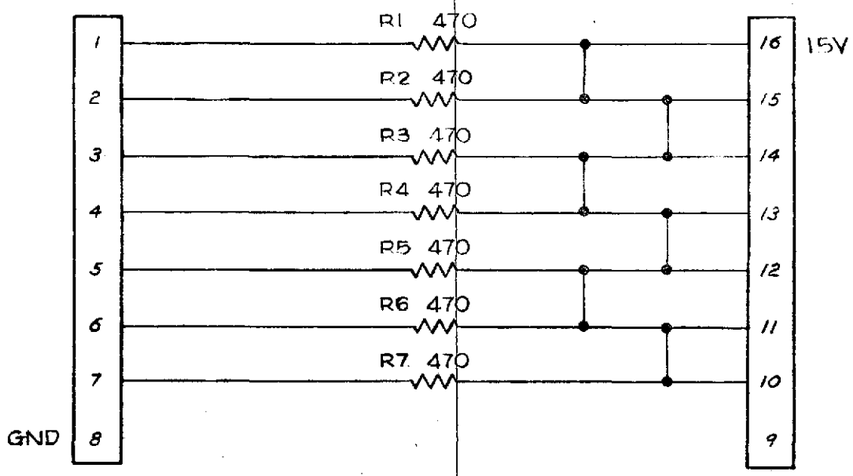
FOLDOUT FRAME

REVISIONS				
LTR	DESCRIPTION	DATE	APPROVED	

Reproduced from best available copy.



-001 SHOWN



SCHEMATIC DIAGRAM

FOR PARTS LIST SEE PL 204310-001

(6) MARK PER LEACH STD 201179-006 WITH 204310-001 APPROX WHERE SHOWN.

(5) AFTER ASSEMBLY OF ITEM NO.'S 4 & 12 TO ITEM NO. 1, BOND ITEM NO. 2 TO ITEM NO. 1 2 PLACES AS SHOWN, USING ITEM NO. 14.

4.- ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/8W

3.- REFERENCE DESIGNATIONS ARE ABBREVIATED: PREFIX WITH UNIT NO. AND APPLICABLE SUBASSEMBLY DESIGNATION.

2.- FOR NEXT ASSEMBLY SEE APPLICATION BLOCK.

1.- DO NOT SCALE DRAWING.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PART LIST

QTY N/A	QTY U/A	NEXT ASSEMBLY	USED ON
6	6		HD-103
		APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ± XX ±
ANGLES ± XXX °
MATERIAL
FINISH
SURFACE ROUGHNESS

CONTRACT NO.
DRAWN R. Iverson 11/16/72
CHECKED
DESIGN
ENGINEER
PROJECT
RELEASE
DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
717 NORTH CONEY AVE. CONTROLS DIVISION AZUSA, CALIFORNIA

DISCRETE PLATFORM
PULL-UP RESISTORS

SIZE	CODE IDENT NO.	DWG NO.	REV
C	96261	204310	

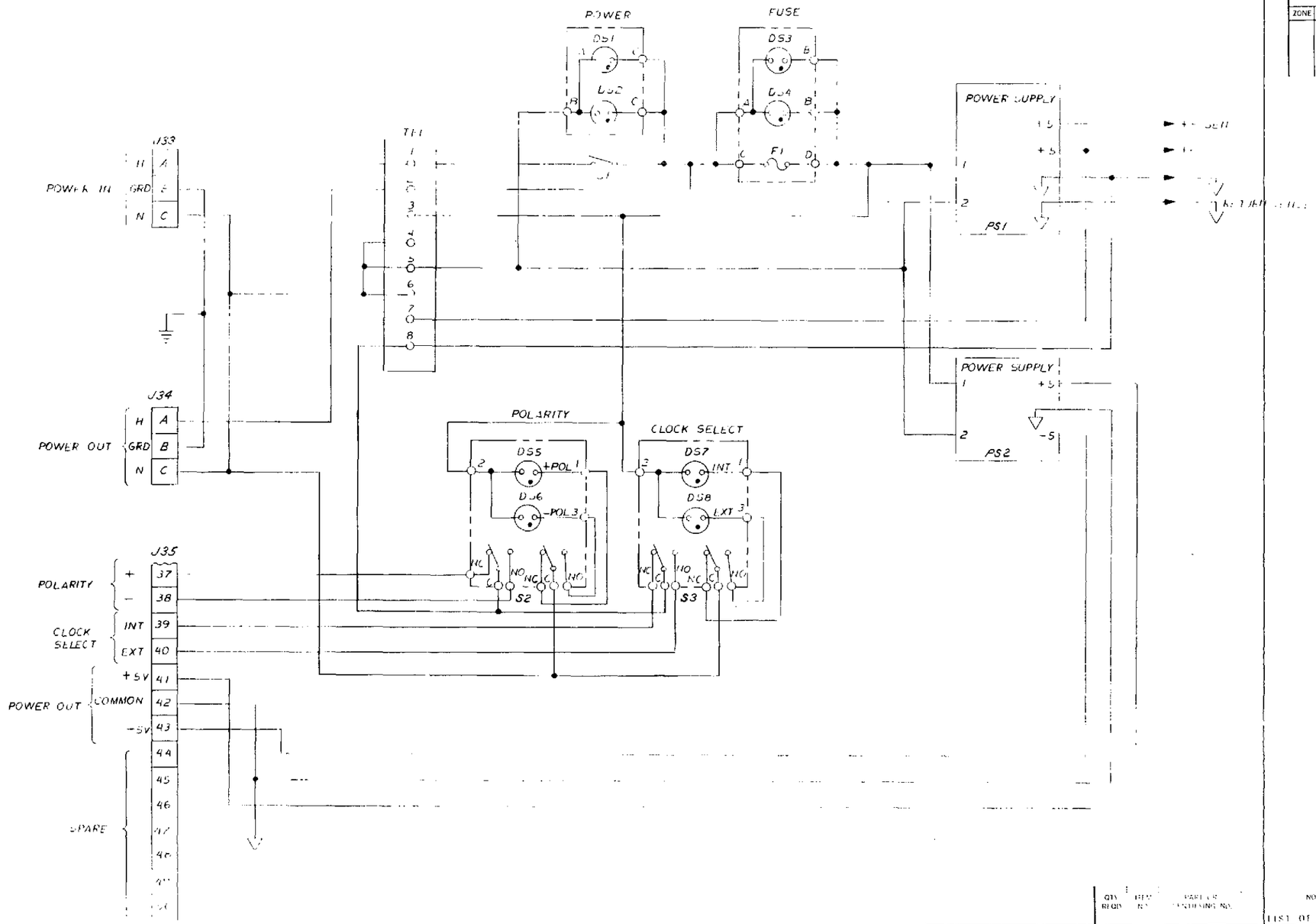
SCALE 4/1 LEVEL: 0 SHEET 1 OF 1

204310

FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PARTS LIST

QTY N/A	QTY U/A	NEXT ASSEMBLY	USED ON APPLICATION
1	1		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS
ANGLES
MATERIAL
FINISH
SURFACE ROUGHNESS

CONTRACT NO.
DRAWN
CHECKED
DESIGN ENGINEER
PROJECT ENGINEER
RELEASE
DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
57 NORTH CONEY AVE
CONTROLS DIVISION
AZUSA, CALIFORNIA

SCHEMATIC DIAGRAM,
POWER SUPPLY

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204317	

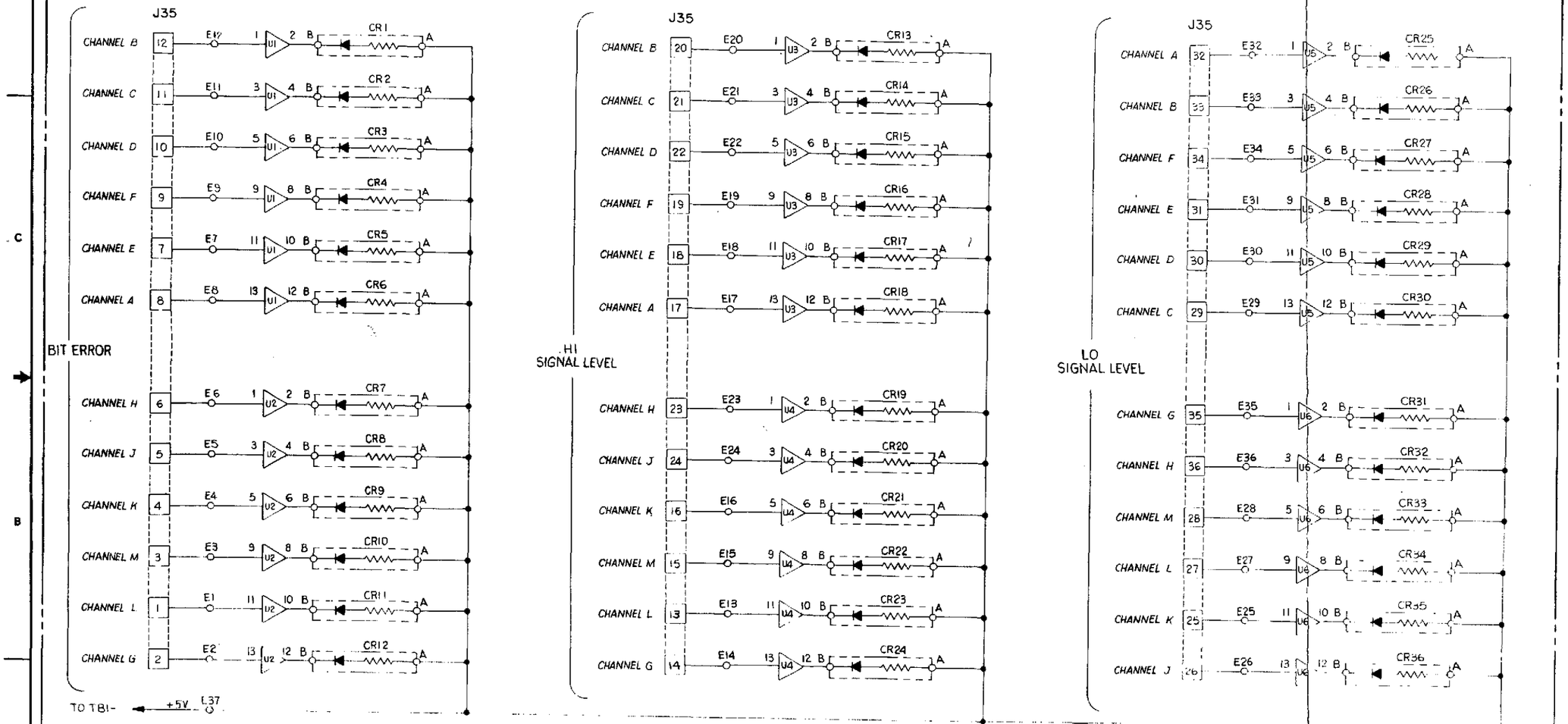
SCALE — LEVEL 0 SHEET 1 OF 2

204317

FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



LED CIRCUIT BOARD PART NO.

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ± XX ±
ANGLES ± XXX
MATERIAL
FINISH
SURFACE ROUGHNESS

CONTRACT NO.
DRAWN
CHECKED
DESIGN
ENGINEER
PROJECT
RELEASE
DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
317 NORTH CONEY AVE.
CONTROLS DIVISION
AZUSA, CALIFORNIA

SCHEMATIC DIAGRAM, POWER SUPPLY

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204317	
SCALE NONE	LEVEL: 0	SHEET 2 OF 2	

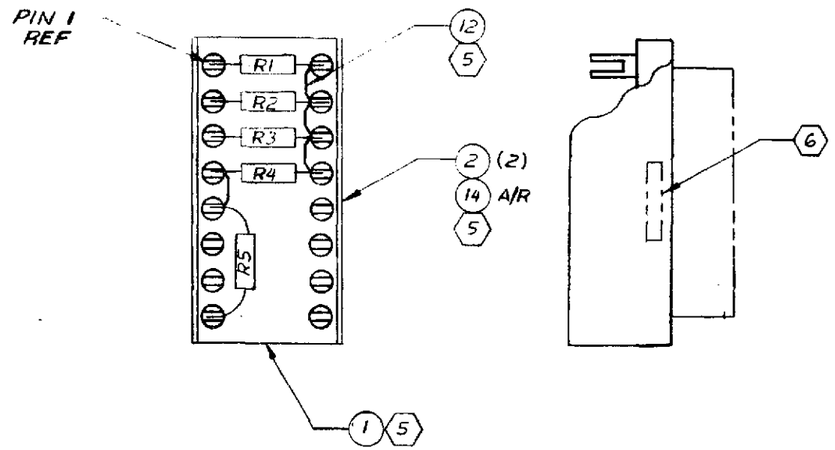
204317

NOTES: UNLESS OTHERWISE SPECIFIED

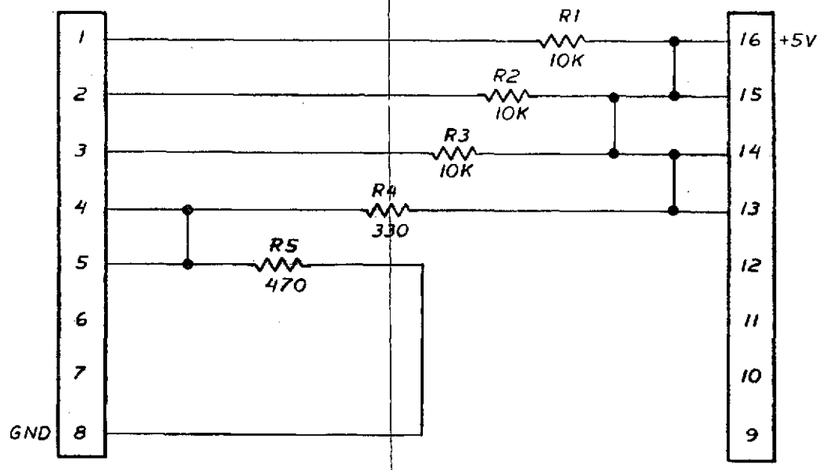
FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



-001 SHOWN



SCHEMATIC DIAGRAM

FOR PARTS LIST SEE PL 204412-001

(6) MARK PER LEACH STD 201179-006 WITH 204412-001 APPROX WHERE SHOWN.

(5) AFTER ASSEMBLY OF ITEM NO.'S 4, 5 & 6 TO ITEM NO. 1, BOND ITEM NO. 2 TO ITEM NO. 1, 2 PLACES AS SHOWN USING ITEM NO. 14.

4.- ALL RESISTOR VALUES ARE IN OHMS, ± 5%, 1/8 W.

3.- REFERENCE DESIGNATIONS ARE ABBREVIATED: PREFIX WITH UNIT NO. AND APPLICABLE SUBASSEMBLY DESIGNATION.

2.- FOR NEXT ASSEMBLY SEE APPLICATION BLOCK.

1.- DO NOT SCALE DRAWING.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PARTS LIST

QTY N/A	QTY U/O	NEXT ASSEMBLY	USED ON
1	1	204274	HD - 103

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCE: FRACTIONS ± .XX ± ANGLES ± .XXX ±

MATERIAL

FINISH

SURFACE ROUGHNESS

CONTRACT NO.

DRAWN [signature] 1-10-73

CHECKED

DESIGN

ENGINEER

PROJECT

RELEASE

DESIGN APPROVAL

DESIGN APPROVAL

LEACH CORPORATION
717 NORTH CONEY AVE.
CONTROLS DIVISION
AZUSA, CALIFORNIA

DESCRETE PLATFORM, RESISTOR NETWORK

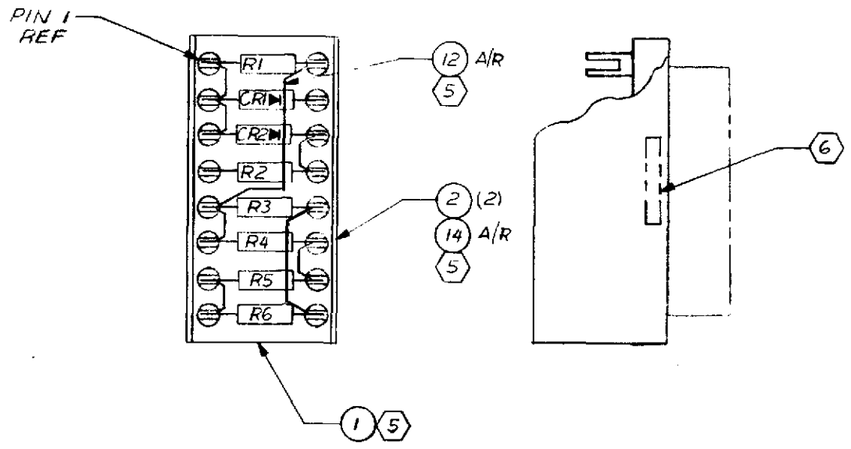
SIZE	CODE IDENT NO.	DWG NO.	REV
C	96261	204412	

SCALE 4/1 LEVEL: 0 SHEET 1 OF 1

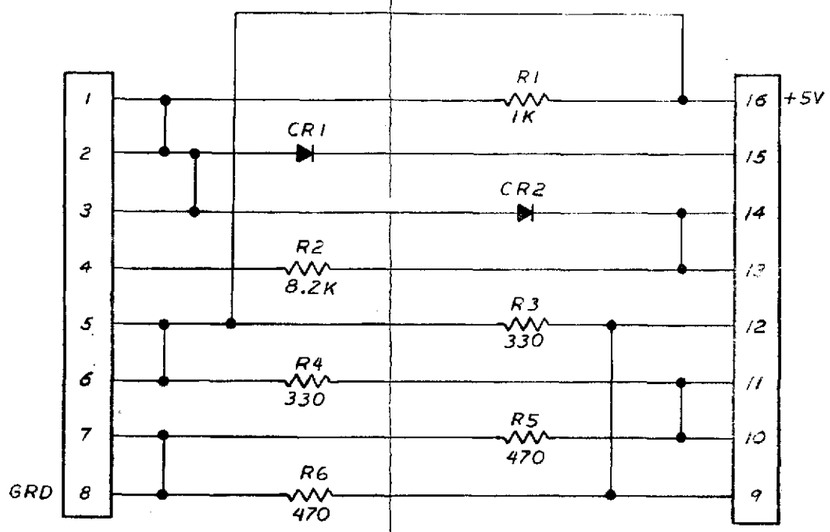
204412

FOLDOUT FRAME

FOLDOUT FRAME



-001 SHOWN



SCHEMATIC DIAGRAM

FOR PARTS LIST SEE PL 204413-001

6. MARK PER LEACH STD 201179-006 WITH 204413-001 APPROX WHERE SHOWN.
5. AFTER ASSEMBLY OF ITEM NO.'S 4 THRU 7 & 10, TO ITEM NO. 1, BOND ITEM NO 2 TO ITEM NO. 1 2 PLACES AS SHOWN, USING ITEM NO. 14.
4. ALL RESISTOR VALUES ARE IN OHMS, ± 5%, 1/8 W.
3. REFERENCE DESIGNATIONS ARE ABBREVIATED: PREFIX WITH UNIT NO. AND APPLICABLE SUBASSEMBLY DESIGNATION.
2. FOR NEXT ASSEMBLY SEE APPLICATION BLOCK.
1. DO NOT SCALE DRAWING.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	FINISH
			LIST OF MATERIALS OR PARTS LIST		

QTY N/A	QTY U/O	NEXT ASSEMBLY	USED ON
1	1	204274	HD-103
		APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ±
ANGLES -
.XX ±
.XXX
MATERIAL
FINISH
SURFACE ROUGHNESS

CONTRACT NO.
DRAWN
CHECKED
DESIGN
ENGINEER
PROJECT
RELEASE
DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
CONTROLS DIVISION
TORRANCE, CALIFORNIA

DISCRETE PLATFORM, RESISTOR & DIODE NETWORK

SIZE	CODE IDENT NO.	DWG NO.	REV
C	96261	204413	

SCALE 4/1 | LEVEL: 0 | SHEET 1 OF 1

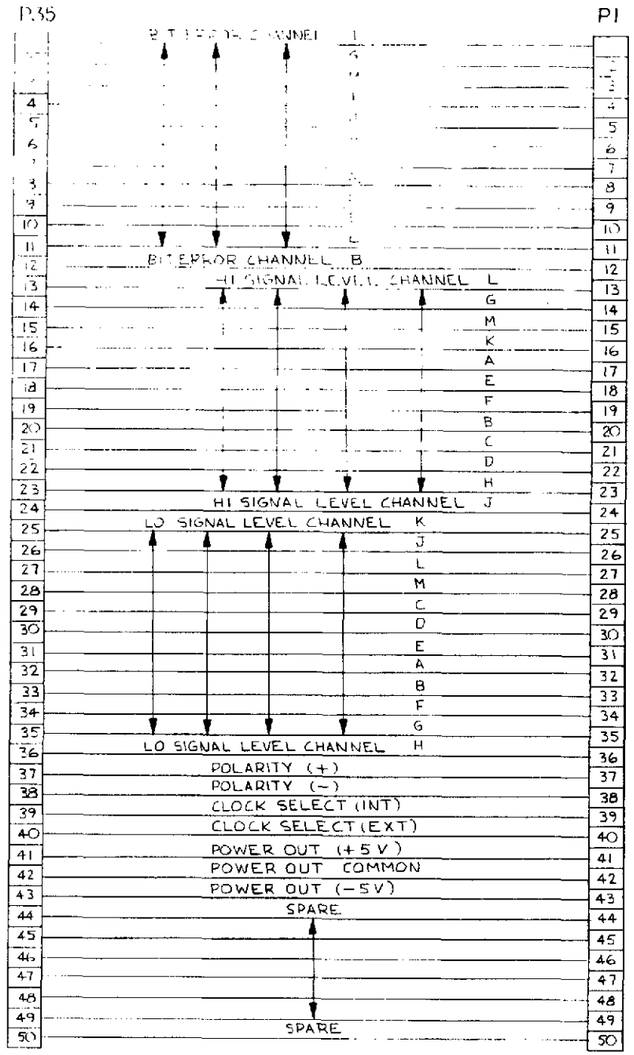
204413

4 3 2 1

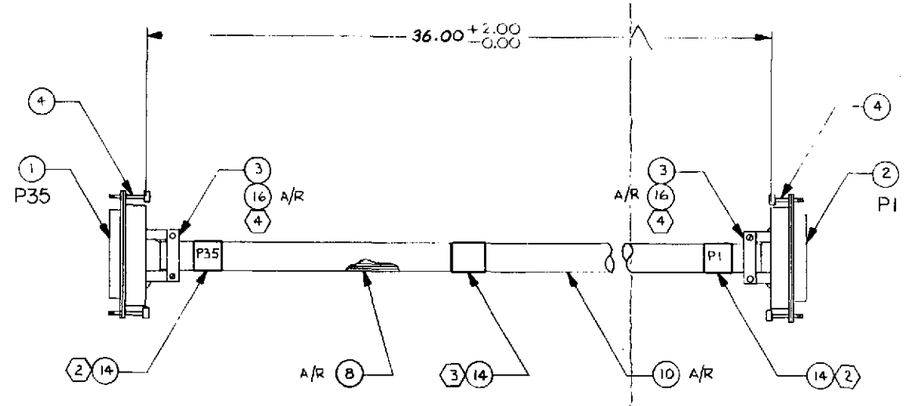
FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



WIRING DIAGRAM



-001 SHOWN

FOR PARTS LIST SEE PL 204420-001

204420

(4) AFTER ASSEMBLY PUT ITEM NO. 3 WITH ITEM NO. 16.

(3) MARK PER LEACH STD 201179-009 WITH 204420-001.

(2) MARK PER LEACH STD 201179-009 WITH REFERENCE DESIGNATION INDICATED.

1.- DO NOT SCALE DRAWING.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PARTS LIST

QTY N/A	QTY U/O	NEXT ASSEMBLY	USED ON
1	1	204433	HD-103
		APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ± XX ± ANGLES ± XXX ±
MATERIAL
FINISH
SURFACE ROUGHNESS

CONTRACT NO.

DRAWN	[illegible]	1-9-73
CHECKED		
DESIGN		
ENGINEER		
PROJECT		
RELEASE		

DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
717 NORTH CONEY AVE. AZUSA, CALIFORNIA
CONTROLS DIVISION

CABLE ASSEMBLY,
POWER SUPPLY/WIRE WRAP PANEL

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204420	

SCALE NONE LEVEL: 0 SHEET 1 OF 1

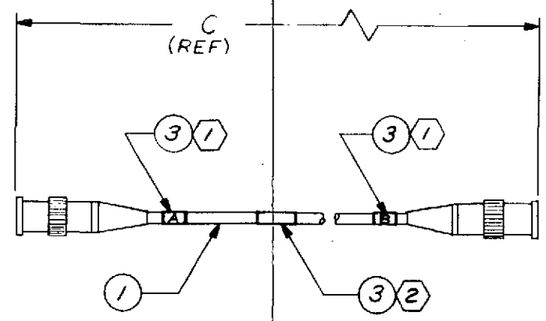
FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

TABLE I

DASH NO.	A	B	C
-001	REPRO-TRACK-2	REPRO-CHAN-A	36 INCHES
-002	3	B	
-003	4	C	
-004	5	D	
-005	6	E	
-006	7	F	
-007	8	G	
-009	9	H	
-009	10	J	
-010	11	K	
-011	12	L	
-012	REPRO-TRACK-13	REPRO-CHAN-M	
-013	REC-TRACK-2	REC-CHAN-A	
-014	3	B	
-015	4	C	36
-016	5	D	24
-017	6	E	
-018	7	F	
-019	8	G	
-020	9	H	
-021	10	J	
-022	11	K	
-023	12	L	
-024	REC-TRACK-13	REC-CHAN-M	
-025	SERVO CLK INPUT	REF OUT	
-026	TAPE SERVO INPUT	REPRO-CHAN-1	
-027	CLK TRACK OUT	REC-CHAN-1	24 INCHES



FOR PARTS LIST SEE PL 204421 AND APPLICABLE DASH NO.

(2) MARK PER LEACH STD 201179-006 WITH 204421 & APPLICABLE DASH NO. IN ACCORDANCE WITH TABLE I.

(1) MARK PER LEACH STD 201179-009 WITH APPLICABLE TRACK & CHANNEL DESIGNATIONS IN ACCORDANCE WITH TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY N/A	QTY U/O	NEXT ASSEMBLY	USED ON
1	1	204433	HD - 103
		APPLICATION	

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ± .XX ±
ANGLES ± .XXX ±
MATERIAL
FINISH
SURFACE ROUGHNESS ✓

CONTRACT NO.
DRAWN 7-11-73
CHECKED
DESIGN
ENGINEER
PROJECT
RELEASE
DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
717 NORTH CONEY AVE. AZUSA, CALIFORNIA
CONTROLS DIVISION

CABLE, RECORD/REPRODUCE

SIZE	CODE IDENT NO.	DWG NO.	REV
C	96261	204421	

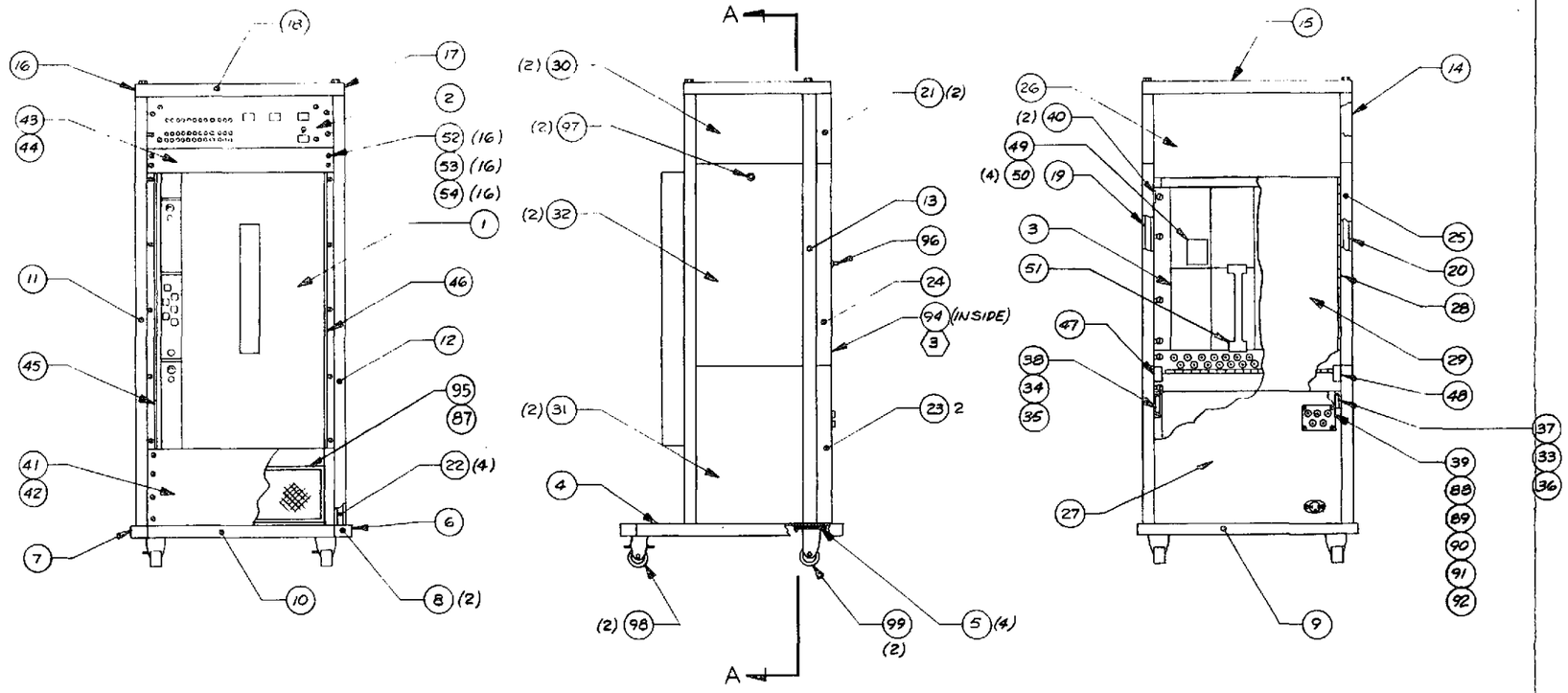
SCALE —— LEVEL : 0 SHEET 1 OF 1

204421

FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



-001 SHOWN

FOR PARTS LIST SEE PL 204433-001

3 PRIOR TO APPLYING LABEL (ITEM NO. 94) INSIDE OF REAR DOOR (ITEM NO. 24) TYPE FOLLOWING INFORMATION IN APPROPRIATE SPACES & SPRAY WITH KRYLON;
MASS DATA STORAGE SYSTEM
PART NO: 204433-001 SERIAL NO: 101
CONTRACT NO. NAS8-28959

2 FOR SCHEMATIC DIAGRAMS SEE DWGS 204257; 204317 & 204302.
FOR CABLE INTERCONNECTION DIAGRAM SEE DWG 204446.
FOR WIRE LIST SEE DWG NO. 204313 (PIN TO PIN LIST - WIRE WRAP PANEL).
FOR ACCEPTANCE TEST PROCEDURE SEE DWG NO. 204411.

1 DO NOT SCALE DRAWING.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PARTS LIST

QTY N/A	QTY U/O	NEXT ASSEMBLY	USED ON
—	—	FINAL	HD-103

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ± .XX ±
ANGLES ± .XXX ±
MATERIAL
FINISH
SURFACE ROUGHNESS ✓

CONTRACT NO.
DRAWN [signature] 1-26-73
CHECKED
DESIGN
ENGINEER
PROJECT
RELEASE
DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
717 NORTH CONEY AVE.
CONTROLS DIVISION
AZUSA, CALIFORNIA

MASS DATA STORAGE SYSTEM

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204433	

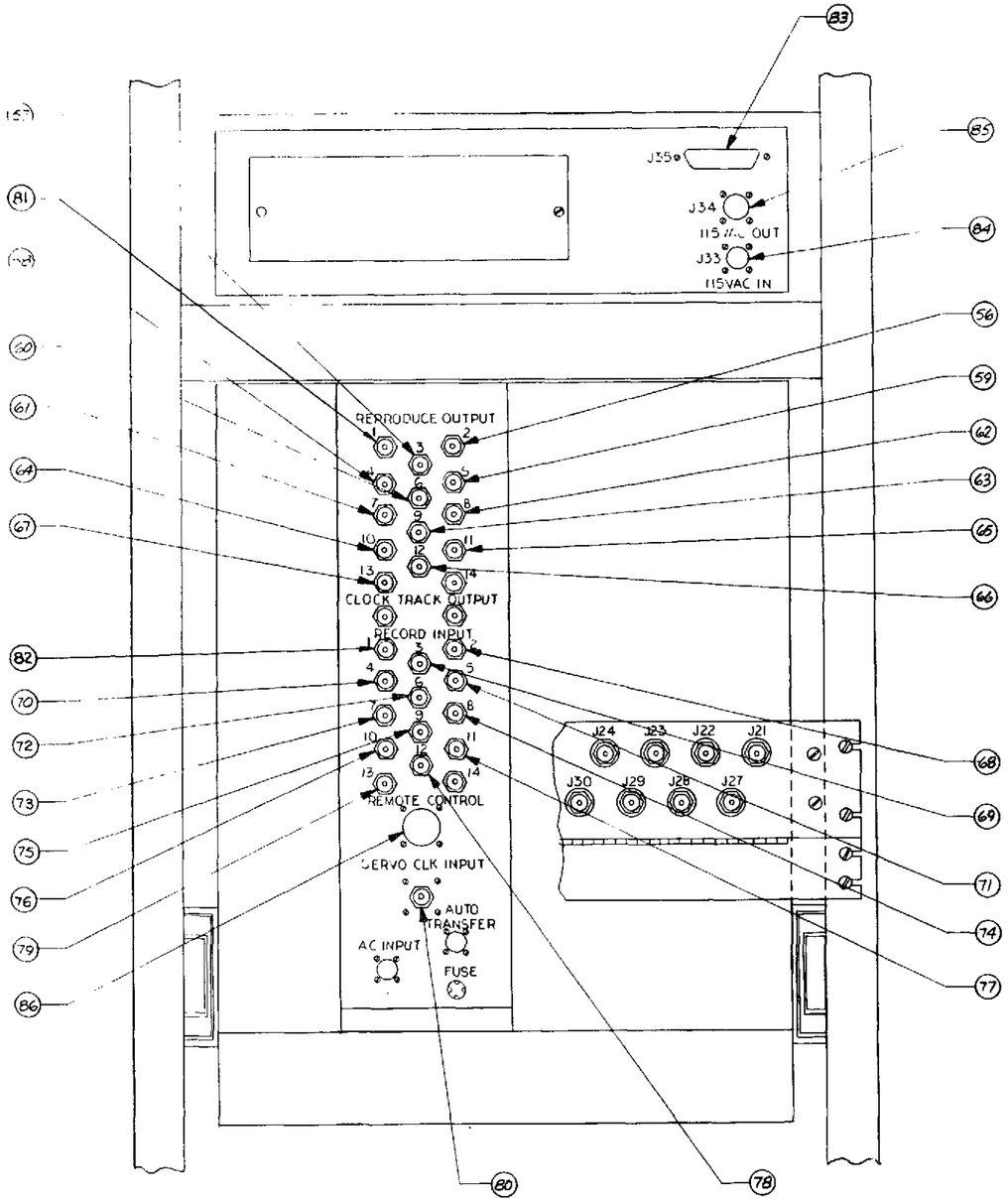
SCALE NONE LEVEL: 0 SHEET 1 OF 2

204433

FOLDOUT FRAME

FOLDOUT FRAME

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



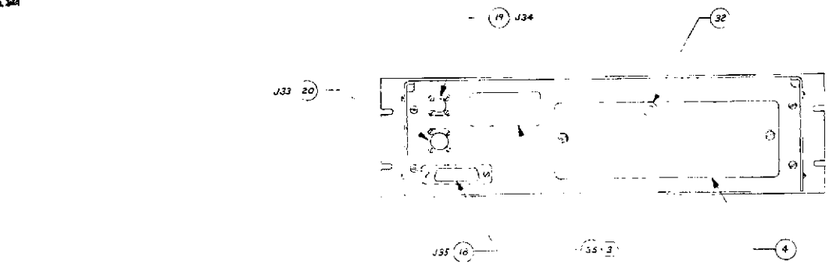
VIEW A-A

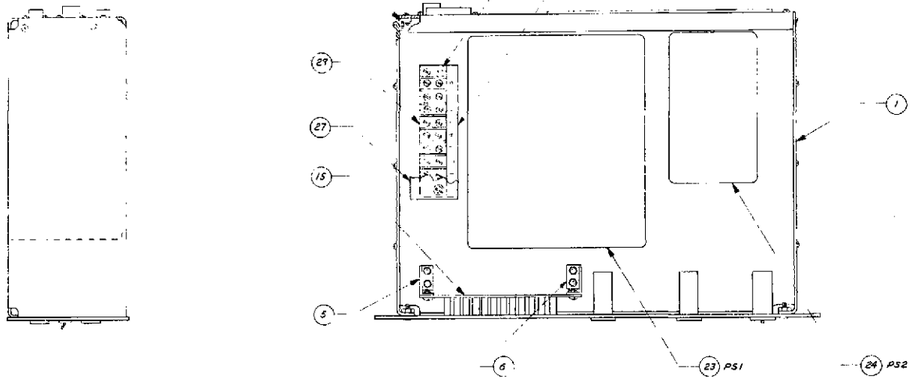
SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204433	
SCALE NONE	LEVEL:0	SHEET 2 OF 2	

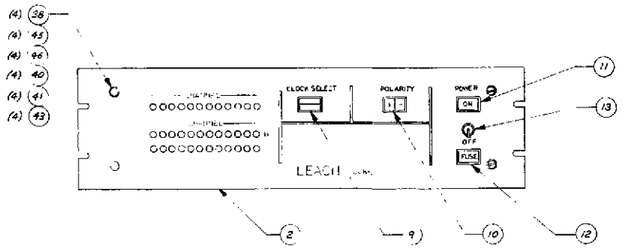
204433

FOLDOUT FRAME

FOLDOUT FRAME







FOR PARTS LIST SEE PL204435-001

3. PRIOR TO APPLYING LABEL (ITEM NO. 35) TO CHASSIS (ITEM NO. 1) TYPE FOLLOWING INFORMATION IN APPROPRIATE SPACES & SPRAY WITH KRYLON:
POWER/CONTROL UNIT
PART NO: 204435-001; SERIAL NO: 103
CONTRACT NO: NAS8-28959

2. FOR NEXT ASSEMBLY SEE APPLICATION BLOCK FOR SCHEMATIC SEE DWG NO. 204317.

1. DO NOT SCALE DRAWING.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PARTS LIST

QTY N/A	QTY U/O	NEXT ASSEMBLY	USED ON
1	1	204439	MD-103
		APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ± .XX ±
ANGLES ± .XXX ±
MATERIAL
FINISH
SURFACE ROUGHNESS

CONTRACT NO.
DRAWN
CHECKED
DESIGN
ENGINEER
PROJECT
RELEASE
DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION CONTROLS DIVISION
70 NORTH CONEY AVENUE AZUSA, CALIFORNIA

CHASSIS ASSEMBLY, POWER SUPPLY

SIZE	CODE IDENT NO.	DWG NO.	REV
E	96261	204435	

SCALE 1/2 LEVEL 10 SHEET 1 OF 1

204435

FOLDOUT FRAME

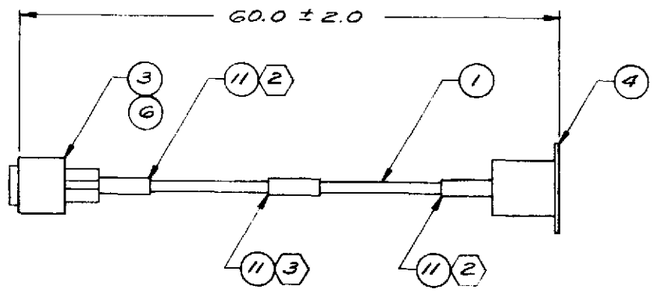
FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

MS310GA10SL-3S

H A
GND B
N C

BRIGHT TERMINAL



FOR PARTS LIST SEE PL204438-001

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PARTS LIST

QTY N/A	QTY U/O	NEXT ASSEMBLY	USED ON
1	1	204433	HD-103
		APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ± .XX ±
ANGLES ± .XXX ±
MATERIAL
FINISH
SURFACE ROUGHNESS √

CONTRACT NO.

DRAWN	MEADER	'267
CHECKED		
DESIGN		
ENGINEER		
PROJECT		
RELEASE		

DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
717 NORTH CONEY AVE.
CONTROLS DIVISION
AZUSA, CALIFORNIA

CABLE, POWER INPUT

SIZE	CODE IDENT NO.	DWG NO.	REV
C	96261	204438	

SCALE NONE | LEVEL: 0 | SHEET 1 OF 1

204438

NOTES: UNLESS OTHERWISE SPECIFIED

〈3〉 MARK PER LEACH STD 201179-009 WITH "204438-001."

〈2〉 MARK PER LEACH STD 201179-009 WITH "115VAC IN."

1 DO NOT SCALE DRAWING.

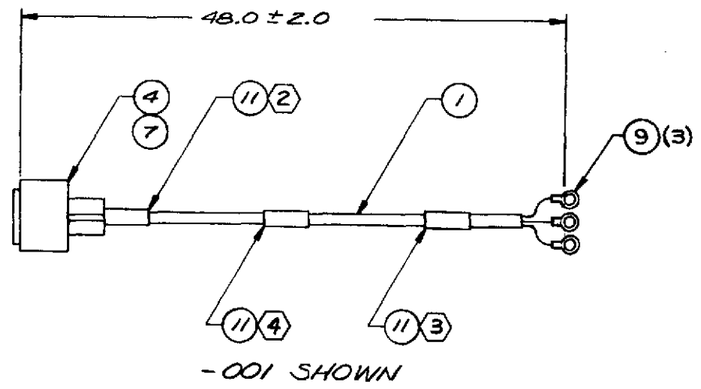
FOLDOUT FRAME

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

MS3106A14S-7P

H	A	BLK → H
GND	B	GRN → GND
N	C	WHT → N



-001 SHOWN

FOR PARTS LIST SEE PL204439-001

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE
LIST OF MATERIALS OR PARTS LIST						

4 MARK PER LEACH STD 201179-009 WITH "204439-001".

3 MARK PER LEACH STD 201179-009 WITH "TB-1".

2 MARK PER LEACH STD 201179-009 WITH "115VAC OUT".

1. DO NOT SCALE DRAWING.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY N/A	QTY U/O	NEXT ASSEMBLY	USED ON
1	1	204433	HD-103
		APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ± XX ±
ANGLES ± .XXX ±
MATERIAL
FINISH
SURFACE ROUGHNESS ✓

CONTRACT NO.

DRAWN	MEADER	12/6/79
CHECKED		
DESIGN		
ENGINEER		
PROJECT		
RELEASE		
DESIGN APPROVAL		
DESIGN APPROVAL		

LEACH CORPORATION
717 NORTH CONEY AVE. CONTROLS DIVISION AZUSA, CALIFORNIA

CABLE, POWER
CONTROL UNIT/ BLOWER

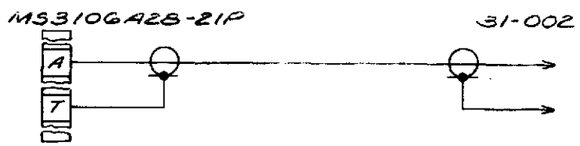
SIZE	CODE IDENT NO.	DWG NO.	REV
C	96261	204439	

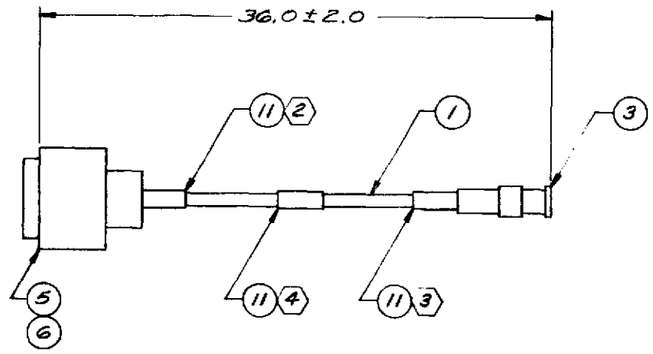
SCALE NONE LEVEL: 0 SHEET 1 OF 1

204439

FOLDOUT FRAME 1

FOLDOUT FRAME 2





-001 SHOWN

FOR PARTS LIST SEE PL 204445-001

REVISIONS					
ZONE	LTR		DESCRIPTION	DATE	APPROVED

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PARTS LIST

QTY N/A	QTY U/O	NEXT ASSEMBLY	USED ON
1	1	204433	HD-103
		APPLICATION	

4 MARK PER LEACH STD 201179-009 WITH "204445-001."

3 MARK PER LEACH STD 201179-009 WITH "REC INDICATE".

2 MARK PER LEACH STD 201179-009 WITH "REMOTE CONTROL".

1. DO NOT SCALE DRAWING.

NOTES: UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ± .XX ±
ANGLES ± .XXX ±
MATERIAL
FINISH
SURFACE ROUGHNESS ✓

CONTRACT NO.

DRAWN	MEALER	1-25-73
CHECKED		
DESIGN		
ENGINEER		
PROJECT		
RELEASE		

DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
717 NORTH CONEY AVE.
CONTROLS DIVISION
AZUSA, CALIFORNIA

CABLE,
RECORD INDICATE

SIZE	CODE IDENT NO.	DWG NO.	REV
C	96261	204445	

SCALE NONE LEVEL: 0 SHEET 1 OF 1

204445

C-7

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

FOLDOUT FRAME 1

FOLDOUT FRAME 2

MASS DATA STORAGE SYSTEM
204433-001

POWER/ CONTROL UNIT
204435-001

115 VAC IN (J33)

115 VAC OUT (J34) — 204439-001

J35 — 204420-001 — J1

BLOWER MODIFIED
Z04496-001

TB1

204497-001

204438-001

PANEL ASSEMBLY, WIRE WRAP 204274-001

REPRODUCE CHANNEL

RECORD CHANNEL

A (J21)	G (J27)	B (J22)	H (J28)	C (J23)	J (J29)	D (J24)	K (J30)	E (J25)	L (J31)	F (J26)	M (J32)	A (J7)	G (J13)	B (J8)	H (J14)	C (J9)	J (J15)	D (J10)	K (J16)	E (J11)	L (J17)	F (J12)	M (J18)	EXT CLOCK (J2)	BIT CLOCK (J3)	BIØ-L (J4)	REC INDICATE (J5)
204421-001	204421-007	204421-002	204421-008	204421-003	204421-009	204421-004	204421-010	204421-005	204421-011	204421-006	204421-012	204421-013	204421-019	204421-014	204421-020	204421-015	204421-021	204421-016	204421-022	204421-017	204421-023	204421-018	204421-024	CLOCK OUT (J20)	BIØ-L OUT (J19)	REF OUT (J6)	204421-025 / 204445-001
2	8	3	9	4	10	5	11	6	12	7	13	2	8	3	9	4	10	5	11	6	12	7	13				

REPRODUCE

RECORD

TAPE SERVO INPUT

CLOCK TRACK OUTPUT

204421-026

204421-027

204447-005
204447-004
204447-003
204447-002
204447-001

J36 J37 J38 J39 J40

SERVO CLK INPUT

PIN A REMOTE CONTROL

J41
115VAC IN

115VAC INPUT

RECORDER / REPRODUCER 203135-005

NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	ITEM NO	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PARTS LIST

REF QTY N/A	REF QTY U/A	NEXT ASSEMBLY	USED ON APPLICATION
		204433	C-D-103

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ± .XX
ANGLES ± .XXX
MATERIAL
FINISH
SURFACE ROUGHNESS

CONTRACT NO
DRAWN J. Smith
CHECKED
DESIGN
ENGINEER
PROJECT
RELEASE
DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
717 NORTH CONEY AVE. AZUSA, CALIFORNIA
CONTROLS DIVISION

INTERCONNECTION CABLE DIAGRAM, MASS DATA STORAGE SYSTEM

SIZE	CODE IDENT NO.	DWG. NO.	REV
D	96261	204446	

SCALE NONE | WEIGHT | SHEET 1 OF 1

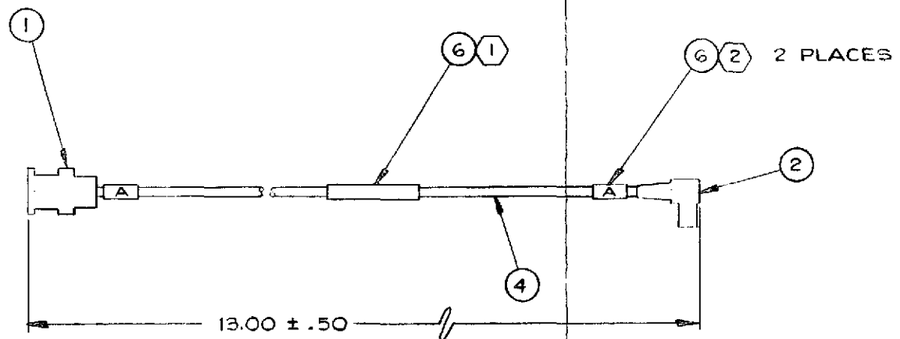
204446

FOLDOUT FRAME

FOLDOUT FRAME

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

TABLE I	
DASH NOMENCLATURE	
NO.	A
001	EXT CLOCK
002	CLOCK OUT
003	BIT CLOCK
004	BIØ-L OUT
005	BIØ-L



FOR PARTS LIST SEE PL204447 AND APPLICABLE DASH NO.

(2.) MARK ITEM 6 PER LEACH STD 201179-009 WITH APPLICABLE NOMENCLATURE AS SHOWN PER TABLE I.

(1.) MARK 6 PER LEACH STD 201179-009 WITH 204447 AND APPLICABLE DASH NO. AS SHOWN PER TABLE I.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE
LIST OF MATERIALS OR PARTS LIST						
1	1	204433	HD-103			

QTY N/A	QTY U/O	NEXT ASSEMBLY	USED ON
		APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ± .XX ±
ANGLES ± .XXX ±
MATERIAL
FINISH
SURFACE ROUGHNESS √

CONTRACT NO.

DRAWN	H.E. Smith	1/23/73
CHECKED		
DESIGN		
ENGINEER		
PROJECT		
RELEASE		
DESIGN APPROVAL		
DESIGN APPROVAL		

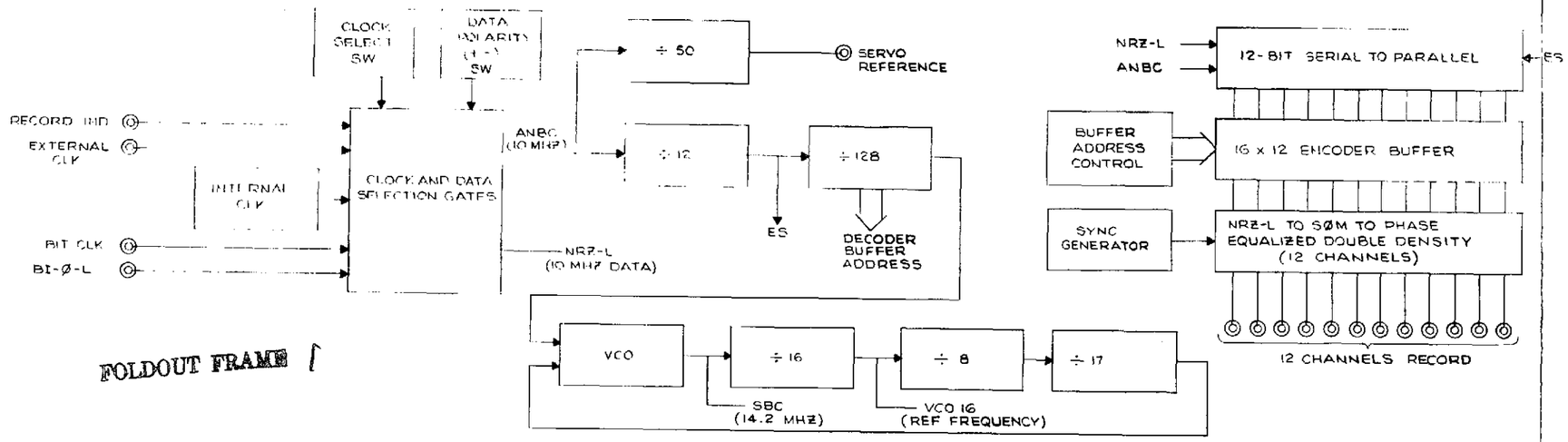
LEACH CORPORATION
717 NORTH CONEY AVE. AZUSA, CALIFORNIA
CONTROLS DIVISION

CABLE, INPUT, WIRE WRAP PANEL

SIZE	CODE IDENT NO.	DWG NO.	REV
C	96261	204447	

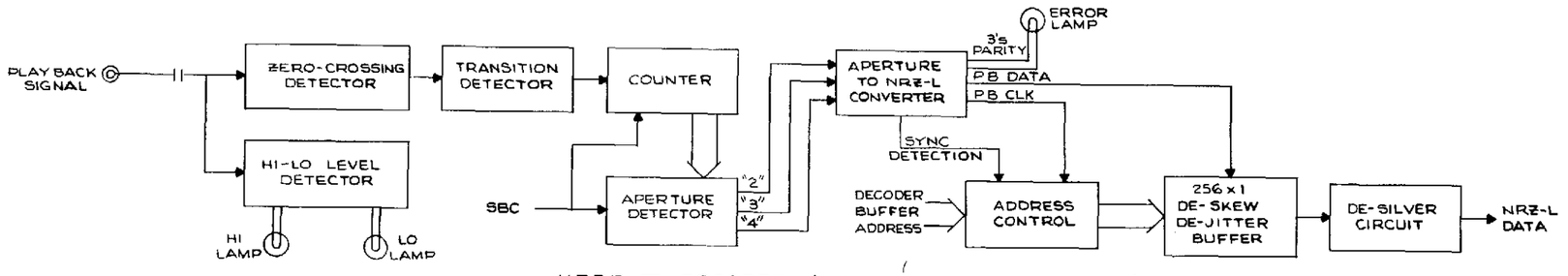
SCALE NONE SHEET 1 OF 1

204447

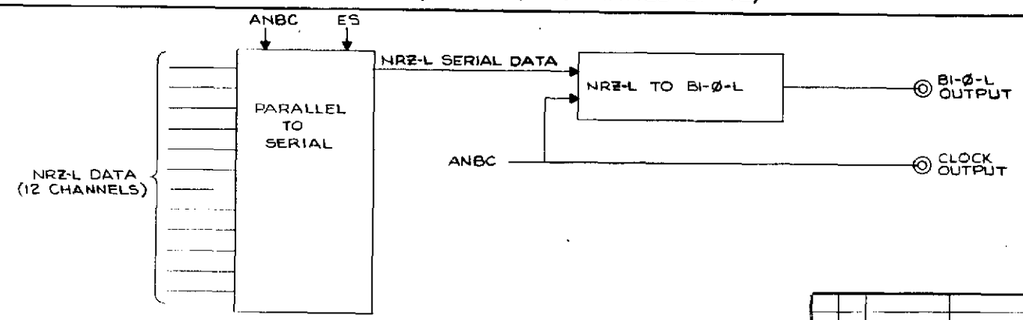


FOLDOUT FRAME 1

HDDR - II 12 CHANNEL ENCODER



HDDR-II DECODER (TYPICAL; 1 CHANNEL OF 12)



PARALLEL TO SERIAL CONVERTER

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ± .XX ±
ANGLES ± .XXX ±
MATERIAL
FINISH
SURFACE ROUGHNESS

QTY N/A	QTY U/O	NEXT ASSEMBLY	USED ON
		APPLICATION	

CONTRACT NO.

DRAWN	F.R.Smith	3/23/75
CHECKED		
DESIGN		
ENGINEER		
PROJECT		
RELEASE		

DESIGN APPROVAL
DESIGN APPROVAL

LEACH CORPORATION
717 NORTH CONEY AVE. AZUSA, CALIFORNIA
CONTROLS DIVISION

BLOCK DIAGRAM, MASS DATA STORAGE SYSTEM

SIZE	CODE IDENT NO.	DWG NO.	REV
D	96261	204448	

SCALE NONE SHEET 1 OF 1

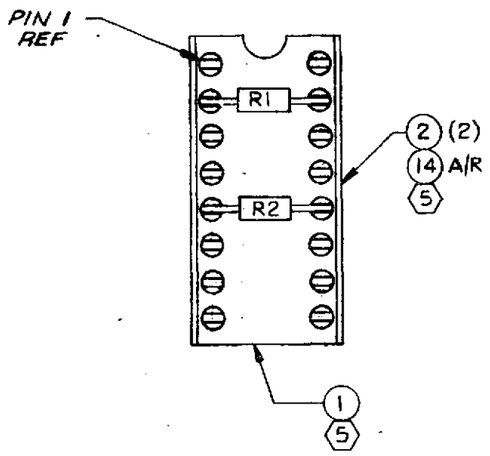
204448

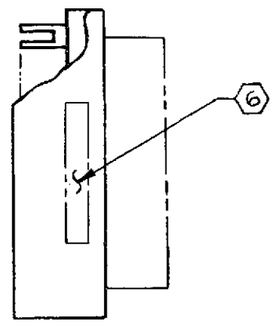
NOTES: UNLESS OTHERWISE SPECIFIED

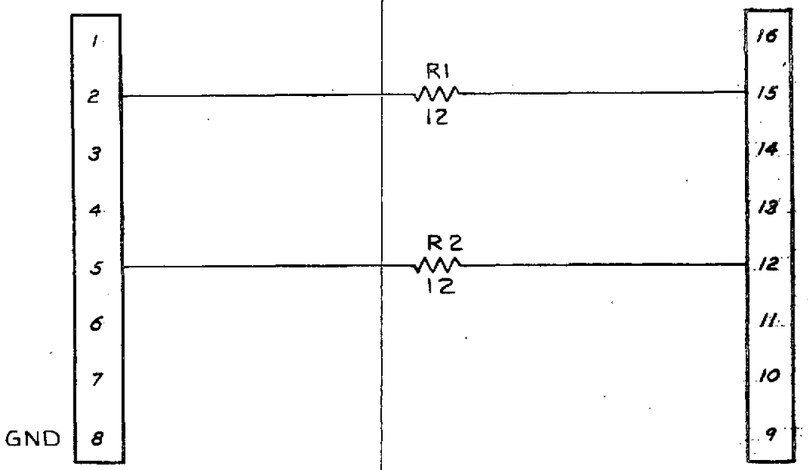
FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED







-001 SHOWN

6. MARK PER LEACH STD 201179-006 WITH 204495-001 APPROX. WHERE SHOWN.

5. AFTER ASSEMBLY OF ITEM NO. 5 TO ITEM NO. 1, BOND ITEM NO. 2 TO ITEM NO. 1 2 PLACES AS SHOWN, USING ITEM NO. 14.

4. ALL RESISTOR VALVES ARE IN OHMS ±5%, 1/8 W.

3. REFERENCE DESIGNATIONS ARE ABBREVIATED: PREFIX WITH UNIT NO. AND APPLICABLE SUBASSEMBLY DESIGNATION.

2. FOR NEXT ASSEMBLY SEE APPLICATION BLOCK.

1. DO NOT SCALE DRAWING.

SCHEMATIC DIAGRAM

FOR PARTS LIST SEE PL 204495-001

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE
LIST OF MATERIALS OR PARTS LIST						

QTY N/A	QTY U/A	NEXT ASSEMBLY	USED ON
1.	1	204274	HD-103
		APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCE
FRACTIONS ± .XX ±
ANGLES ± .XXX ±
MATERIAL
FINISH
SURFACE ROUGHNESS

CONTRACT NO.

DRAWN	DAILEY	2-15-73
CHECKED		
DESIGN		
ENGINEER		
PROJECT		
RELEASE		
DESIGN APPROVAL		
DESIGN APPROVAL		

LEACH CORPORATION
717 NORTH CONEY AVE. AZUSA, CALIFORNIA
CONTROLS DIVISION

DISCRETE PLATFORM DRIVER RESISTORS

SIZE	CODE IDENT NO.	DWG NO.
C	96261	204495

SCALE 4/1 | LEMELIO | SHEET 1 OF 1

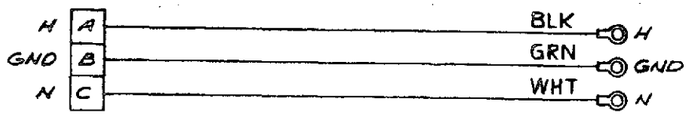
UNLESS OTHERWISE SPECIFIED

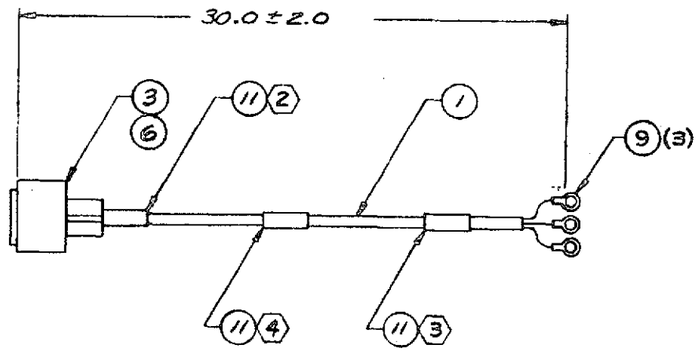
FOLDOUT FRAME 1

FOLDOUT FRAME 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

MS310GA10SL-3S





-001 SHOWN

FOR PARTS LIST SEE PL204497-001

QTY REQD	ITEM NO.	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL	SPECIFICATION	ZONE

LIST OF MATERIALS OR PARTS LIST

(4) MARK PER LEACH STD 201179-009 WITH "204497-001".

(3) MARK PER LEACH STD 201179-009 WITH "TB-1".

(2) MARK PER LEACH STD 201179-009 WITH "115VAC IN".

1. DO NOT SCALE DRAWING.

NOTES: UNLESS OTHERWISE SPECIFIED

QTY	QTY	NEXT ASSEMBLY	USED ON
1	1	204493	HD-109
N/A	U/D	APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

TOLERANCE

FRACTIONS ± .XX ±

ANGLES ± .XXX ±

MATERIAL

FINISH

CONTRACT NO.

DRAWN	MEADER	3-5-13
CHECKED		
DESIGN		
ENGINEER		
PROJECT		
RELEASE		

DESIGN APPROVAL

DESIGN APPROVAL

LEACH CORPORATION
CONTROLS DIVISION
717 NORTH DEWEY AVE. AZUSA, CALIFORNIA

CABLE, POWER
BLOWER/TRANSPORT

SIZE	CODE IDENT NO.	DWG NO.
C	96261	204497

SCALE NONE LEVEL: 0 SHEET 1

204497-001

APPENDIX A

Contract NAS8-28959
Leach Corporation

EXHIBIT "A"
SCOPE OF WORK

A. Technical Requirements

See ~~attached~~ Specification GC110467 for technical requirements for a high bit rate mass storage device, except referenced MIL-STD-480 and MIL-STD-454 are not applicable and compliance to MSFC-STD-421A shall only be required as applicable.

B. Technical Controls

The design, technical approach and status of the effort shall be presented in written and verbal form for review and approval by the MSFC, Technical Representative. The first presentation should be made two months (or earlier if ready) after the effective date of the contract and subsequent presentations should be made at two-month intervals throughout the contract period.

C. Delivery Schedule

1. Delivery of the High Bit Rate Mass Storage Device shall be within six (6) months after award of contract.

2. Delivery of all reports and data shall be as specified on Data Requirements List (DRL) No. 308 and as elsewhere specified in this contract.

3. The final summary report shall be delivered not later than seven (7) months after award of contract.

D. Data Requirement Statement of Work

1. General:

The contractor shall furnish all data identified and described in the Data Requirements List No. 308 (hereinafter called DRL), attached hereto and made a part of this contract. Such data shall be prepared in accordance with the Data Requirement Description (hereinafter called DRD) referenced in the DRL for each line item of data such that the intent and objective of the DRD is satisfied.

Insofar as practical, contractor internal documents will be used to satisfy the data requirements specified on the DRL and will not be retyped or reprinted unless authorized.

Nothing contained in the DRL shall relieve the contractor from furnishing data called for by, or under the authority of, other provisions of the contract which is not identified and described in the DRL.

EXHIBIT "A" (CONT'D)

2. Identification of Data:

All data items delivered, except drawings and microfilm, shall be typewritten and clearly marked on the cover with the contract number, the DRL number, the DRL line item number and response number (i.e., 3rd monthly report, 0003). Documents that satisfy the requirements of more than one DRL line item shall reflect all applicable line item numbers.

3. Title Page for Reports:

All reports shall be submitted under a title page showing the following information:

a. Contractor's name and address, including segment generating the report.

b. Title of report, including period covered, when applicable.

c. Author(s)

d. Type of report and contract number.

e. Date of publication.

f. Prepared for George C. Marshall Space Flight Center, Marshall Space Flight Center, Alabama 35812.

4. Reports Distribution:

All reports (except to DCASO) shall be addressed to National Aeronautics and Space Administration, George C. Marshall Space Flight Center, Marshall Space Flight Center, Alabama 35812 to the codes and in the quantities as shown on the page of this Exhibit "A" entitled Distribution List for Reports and Data. A list of the reports distribution made by the Contractor shall be attached to the reports forwarded to A&TS-PR-M.

APPENDIX B

MSFC FORM 482 (VERTICAL) (AUG 1960)

732639

NOTICE — When Government drawings, specifications, or other data are used for any purpose other than in connection with a definitely related Government procurement operation, the United States Government thereby incurs no responsibility nor obligation whatsoever; and the fact that the Government may have formulated, furnished, or in any way supplied the said drawings specifications or other data is not to be regarded by implication or otherwise as in any manner licensing the holder or any other person or corporation, or conveying any rights or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

APPLICATION		PART No.	MF
NEXT ASSY	USED ON		

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL

A HIGH BIT RATE MASS DATA STORAGE DEVICE, SPECIFICATION FOR

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON: FRACTIONS DECIMALS ANGLES	ORIGINAL DATE OF DRAWING		GEORGE C. MARSHALL SPACE FLIGHT CENTER NATIONAL AERONAUTICS AND SPACE ADMINISTRATION HUNTSVILLE, ALABAMA
	DRAFTSMAN	CHECKER	
	TRACER	CHECKER	
MATERIAL	ENGINEER	ENGINEER	
	SUBMITTED		
HEAT TREATMENT			
FINAL PROTECTIVE FINISH	APPROVED		
	SCALE	DWG SIZE A	GC 110467
	UNIT WT		SHEET 1 OF 11

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1. SCOPE

This specification defines the system design and performance requirements, physical characteristics and limitations, and acceptance criteria for a High Bit Rate Mass Data Storage Device.

1.1 Purpose - The purpose of the High Bit Rate Mass Data Storage Device is to store (record), or dump (playback or reproduce) serial digital pulse code modulated data at a rate of ten (10) megabits per second continuously for a minimum time period of thirty (30) minutes. The storage media containing the stored information (such as a reel of magnetic tape) shall be removable from the device by simple manual means. The storage media will be required to maintain the integrity of the stored information as a separate entity until such time as it shall be reinstalled in a mass data storage device for non destructive playback of the stored data. The device will be required to playback or reproduce the data within the storage media at a serial digital rate of ten (10) megabits per second bi-phase level PCM waveform.

The High Bit Rate Mass Data Storage Device is ultimately intended for use in Space Stations to fulfill a requirement for bulk storage of digital data in a form which can be removed from the Space Station and returned to ground operations. The hardware supplied under this specification is intended for concept verification purposes and for Space Station Sub-System Breadboard integration to verify the intended concept of operation as a part of the Space Station Subsystem.

2. APPLICABLE DOCUMENTS

The following documents of the exact issue shown, form a part of this specification to the extent specified herein. In the event of conflict between the documents referenced herein and the contents of this specification, the contents of this specification shall be considered a superseding requirement.

SPECIFICATIONS

Federal

Military

MIL-D-1000 — Drawings, Engineering and Associated Lists

George C. Marshall Space Flight Center

MSFC-SPEC-331 — Enclosures, Modular, Shielded, Radio Frequency Interference, Specification for

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STANDARDS

Military

MIL-STD-1472	Human Engineering Design Criteria for Military Systems, Equipment and Facilities
MIL-STD-454	Standard General Requirements for Electronic Equipment
MS-33586A	Metals, Definition of Dissimilar
MIL-STD-100A	Engineering Drawings Practices
MIL-STD-480	Configuration Control - Engineering Changes, Deviations, and Waivers

George C. Marshall Space Flight Center

MSFC-STD-421A	Electrical Support Equipment, General Design Requirements for
MSFC-STD-275A	Marking of Electrical Ground Support Equipment, Front Panels, and Rack Title Plates

George C. Marshall Space Flight Center (MSFC) Documents

MSFC-PPD-600	Electrical Preferred Parts, Volume I and Volume II

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3. REQUIREMENTS

3.1 Physical - Limitations on weight, dimensions, and volume shall not be imposed on the equipment.

3.2 Maintainability - System equipment designs shall incorporate maintainability features that will permit accomplishment of all necessary maintenance and repair with a minimum expenditure of manpower and elapsed time. The requirements of paragraph 5.9 of MIL-STD-1472 shall be used as a design guide for incorporation of these maintainability features.

The following maintainability requirements shall apply to system equipment:

a. System equipment shall be designed for 100% replacement capability at the subassembly or component level or by functional substitution.

b. System equipment shall be designed to permit easy access for scheduled maintenance and repair.

c. Access for maintenance shall be accomplished with minimum disconnection of good equipment.

d. Repair, replacement, and assembly tasks shall minimize exposure to hazards.

3.3 Operational Availability - System equipment shall have, as a minimum, a useful life of five (5) years combined storage and service under the environment specified herein.

3.4 Safety - System equipment shall be designed to incorporate personnel and equipment safety features specified herein.

3.5 Personnel/Operator Safety - System equipment designs shall incorporate methods to protect operating and servicing personnel from accidental contact with electrical potentials and shall not embody mechanical features which may reasonably be expected to cause injury during normal operation or because of malfunctioning of equipment. Equipment chassis, enclosures, and frames shall be electrically connected to the facility grounding grid at the nearest point. The length of projecting and overhanging edges shall be held to a minimum and all projecting edges and corners shall be rounded.

3.5.1 Equipment Safety - System equipment shall be designed for protection from overvoltage/undervoltage and transients as specified in MSFC-STD-421A.

3.6 Environment - System equipment shall be designed to withstand the environments specified in the following paragraphs.

3.6.1 Natural Environment - Natural environments shall be as specified in MSFC-STD-421A and as shown in the following paragraphs:

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3.6.1.1 Ambient Temperature - System equipment shall be designed to withstand the ambient temperatures specified below.

	Low Temperature Extreme	High Temperature Extreme
Non-Operating and Storage	- 24°C (-10°F)	+ 52°C (+ 125°F)
Operating	+ 4°C (+ 40°F)	+ 43°C (+ 110°F)

3.6.1.2 Relative Humidity - System equipment shall be designed to withstand the conditions of relative humidity specified below:

a. Operating: Up to 60%

b. Non-Operating: Up to 95%

3.6.1.3 Altitude - System equipment shall be designed to withstand the altitude conditions specified below:

a. Operating: Sea level to approximately 5,000 feet above

b. Non-Operating: Sea level to approximately 10,000 feet above and storage

3.6.1.4 Vibration - System equipment shall be designed to withstand the vibration environment specified below:

a. Operating: No requirement

b. Non-Operating: 0.2 G peak 10 to 100 hz sinusoidal

3.6.2 Induced Environment - Induced environments shall be as specified in the following paragraphs.

3.6.2.1 Electromagnetic Interference - System equipment, when installed in enclosures conforming to Specification MSFC-SPEC-331 or in an otherwise environment of equal electromagnetic control, shall operate as specified when operating either independently or in conjunction with other equipment with which there are electrical connections, or which may be installed nearby; and shall not, in itself, be a source of interference which might adversely affect the operating of other equipment. Interference control shall be considered in the basic design of system equipment. The design shall be such that, before interference control components are applied, the amount of inference internally generated and propagated shall be the minimum achievable.

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3.6.3 Transportability - System equipment shall be designed to withstand the normal handling, and transportation environments when packaged for delivery.

3.6.4 Storage - System equipment shall be designed to withstand storage for periods of up to five years under the environment specified as non-operating in paragraph 3.6.1.

3.7 System Design and Construction Standards - Design and construction standards used in off-the-shelf hardware or hardware previously developed on other Government contracts shall be acceptable provided the equipment is compatible with the performance and environmental criteria as specified in this specification. The design and construction standards specified herein shall apply to system equipment that must be developed.

3.7.1 General Design and Construction Requirements - System equipment shall be designed in accordance with the general requirements of MSFC-STD-421A and as specified in the following paragraphs.

3.7.1.1 Materials, Parts and Processes - Materials, parts and processes shall be of the highest quality compatible with the technical requirements specified herein. Standard, proven and economical parts shall be specified to the maximum extent consistent with reliability, maintainability and performance requirements.

3.7.1.2 Standard and Commercial Parts - Standard and commercial parts shall be used where applicable if compatible with the performance and environmental criteria specified herein. Where standard or commercial parts are not available, maximum utilization shall be made of parts referenced in MSFC-PPD-600.

3.7.2 Electrical Design and Construction Requirements

3.7.2.1 Primary Power - System equipment shall be designed to operate and maintain specified performance from power sources supplying the following ac voltages. AC voltages shall be provided by the facility and shall be 60 hz industrial type power.

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AC Voltages	Specification
1. 115 volts RMS, 60 hz	Industrial
2. 120 volts RMS, 60 hz	Industrial

3.7.2.2 Transient Suppression - Transients shall be suppressed as required for equipment protection and radio frequency interference suppression. In application of suppressors, the operation of associated circuit elements shall not be unduly affected. Transient protection shall be provided in solid-state switching circuits, and so packaged that the switching and protection circuits cannot be separated.

3.7.2.3 Grounding and Shielding - Grounding and shielding of system equipment shall meet the following requirements:

3.7.2.3.1 Equipment Ground - Equipment chassis, enclosures, frames, and neutrals of ac power sources shall be electrically connected to the facility grounding grid at the nearest point.

3.7.2.3.2 Shields - Shields over individual conductors shall be grounded at one point. Shields shall not be used as signal or power return conductors. Any shielding system shall consist of a network without closed loops, and shall be isolated from ground potential except at the single point of connection to ground.

3.7.2.4 Wiring and Cabling - System and equipment cabling and chassis assembly wiring shall be in accordance with MSFC-STD-421A paragraph 5.7.8.

3.7.3 Mechanical Design and Construction Requirements - Where practicable, mechanical design of system equipment shall be in accordance with MSFC-STD-421A, paragraph 5.8.

3.7.4 Moisture and Fungus Requirements - System equipment shall be designed so that the materials comprising its makeup are basically not nutrients for fungus. However, the use of materials which are not moisture or fungus resistant is not prohibited in hermetically sealed assemblies. Fungus inert materials are listed in MIL-STD-454, requirement 4.

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3.7.5 Corrosion of Metal Parts - Metals used shall be of a corrosion-resistance type suitably treated to resist corrosive conditions likely to be met in manufacture, assembly, testing, servicing, storage or normal service use. Unless suitably protected against electrolytic corrosion, dissimilar metals, as defined in MS 33586, shall not be used in direct physical contact.

3.6.6 Contamination Control - Cleanliness of assembled electronic equipment shall be maintained in accordance with good commercial practice.

3.7.7 Interchangeability and Replaceability - All system equipment, and components and subassemblies thereof, designed for replacement as the mode of repair shall be designed to be interchangeable. Interchangeable items shall be as defined in MIL-STD-100A.

3.7.8 Identification and Marking - Identification markings for electrical equipment shall be legible and permanent, and shall be in accordance with MSFC-STD-275A. Vertical racks shall be identified by rack title plates. Marking shall be in accordance with MSFC-STD-275A. Each connector of a cable assembly shall be identified by application of a suitable tag containing the complete reference designation of the cable connector and that of its mating connector.

3.7.9 Workmanship - All system equipment shall be constructed in a thoroughly workmanship-like manner. Particular attention shall be given to neatness and thoroughness of soldering, marking of parts and assemblies, wiring, welding, and brazing, plating, riveting, finishes, machine operations, screw assemblies, and freedom of parts from burrs and sharp edges, or any other damage or defect that could make the part or equipment unsatisfactory for the operation or function intended. The requirements of MIL-STD-454, Requirement 9 shall apply.

3.7.10 Human Performance - System equipment shall incorporate the human engineering design parameters to allow optimum human factors practice to be utilized in the validation of the man/machine relationship. The human engineering design criteria specified in MIL-STD-1472 shall be used as guidelines in the design of system equipment.

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3.7.11 Requirements for Bulk Data Storage - Bulk data storage requirements shall be satisfied by a High Bit Rate Mass Data Storage Device (Subsystem) having the characteristics described in the following paragraphs.

3.7.11.1 Subsystem Interface - The Mass Data Storage Subsystem will interface with a Data Terminal Interface Unit.

3.7.11.2 Input Data Format - The mass data storage subsystem shall accept a data input signal which will be a serial Bi-Phase Level Pulse Code Modulated (PCM) wavetrain of 10 megabits per second. The input data will not be continuous. Discontinuities will occur where the input PCM wavetrain will terminate and the input will remain at 0.0 volt dc. potential (or ground potential) for periods of 5 seconds or longer. The input circuit shall accept a standard TTL logic level compatible signal.

3.7.11.3 Input Data Rate - The mass data storage subsystem shall be capable of recording input data at a rate of 10 megabits per second continuously for a minimum time period of 30 minutes.

3.7.11.4 Input Clock - A 10 megahertz per second clock input signal will be available. The clock signal will be a 10 megahertz per second square wave 50% duty cycle and will be in synchronization with all record data to the mass data storage subsystem. The input clock signal circuitry shall be TTL logic level compatible.

3.7.11.5 Output Data Format - The mass data storage subsystem shall be capable of reproducing the recorded data at a 10 megabit per second rate. The output waveform shall be a serial Bi-Phase Level PCM waveform. The output circuit shall produce a TTL logic level compatible signal.

3.7.11.6 Output Clock - The mass data storage subsystem shall generate an output clock signal during reproduction of stored data which will be in synchronization with the data being reproduced. The clock signal shall be a 10 megahertz per second square wave, 50% duty cycle. The output circuitry supplying the clock signal shall produce a TTL logic level compatible signal.

3.7.11.7 Output characteristics -

3.7.11.7.1 Bit-to-Bit Jitter - Any reproduced output data bit period shall be within 0.25% of the preceding bit period.

3.7.11.7.2 Cumulative Jitter - The cumulative jitter shall be less than $\pm 2.0\%$ of a nominal bit period for any 400 bit sequence where referenced to the first bit or any bit within the 400 bit sequence.

3.7.11.7.3 Short Term Bit Error Rate - The bit error rate from input to output shall not exceed one error in 10^6 bits during any 1.0 second period of output data. Apparent errors due to bit slippage, lost bits, repeated bits, and failure to stay in synchronization shall not be exempt from error rate determination.

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3.7.11.8 Tape Interchangeability - Magnetic tapes recorded on a given mass data storage subsystem shall be capable of being reproduced on a similar subsystem with no degradation in performance or fidelity.

3.7.11.9 Tape Quality - The mass data storage subsystem shall be capable of performing to the required specifications with Scotch No. 888 or equivalent tapes of 1 inch normal width.

3.7.11.10 Tape Reels - The mass data storage subsystem shall accept either precision or non-precision reels of 14 inch diameter conforming to NAB Standards without modification or readjustment and meet all applicable specifications.

3.7.11.11 Controls - The mass data storage subsystem shall have the following controls:

- o Power ON/OFF
- o Record
- o Reproduce (playback)
- o Fast Forward
- o Rewind
- o Stop

A capability for both local and remote operation of the above control functions is required. The subsystem shall include the capability to recognize and execute the above commands from signals received. The signal input circuitry shall be compatible with TTL logic levels.

3.7.11.12 Operation Status Indications - The mass data storage subsystem shall have the following status indications and signals:

- o Record Mode
- o Reproduce Mode
- o Rewind Mode
- o Fast Forward Mode
- o Stop
- o Tape Supply at Beginning
- o End of Tape

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- Record Ready (Record command has been initiated, and subsystem is up to speed and ready for data)

- Reproduce Ready (Reproduce command has been given and subsystem is up to speed and producing valid output data)

The above status signals shall be available for both local and remote operation of the subsystem. Locally, the status signals shall be displayed appropriately on the control panel of the subsystem. Remote status indications will be by individual output signals. The output signals shall be compatible with TTL logic levels.

3.7.11.13 Starting/Stopping Operation - Starting shall be by manual local operation or by remote command. Stopping shall be by local manual operation, or by remote command, or by automatic end-of-tape sensing or tape break sensing by the tape transport. End-of-tape sensing will automatically stop the tape transport before tape runout at either the beginning or end of the tape supply. The transport shall be equipped with a fail-safe emergency braking system which shall operate automatically in the event of power failure.

3.7.11.14 Start/Stop Time - To be determined.

27 June 1972

Purchasing Office
George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama 35812

Attention: W. L. Troupe

Subject: Contract NAS8-28959

Gentlemen:

Enclosed is three (3) copies of the subject contract (proposed) which have been signed by Leach Corporation indicating our acknowledgement of the terms of the negotiated agreement. Although Leach Proposal 732639 was not specified as a part of the contract, compliance with Specification GC110467 will be in accordance with Pages 2-1 through 2-7, Folder 1, of the Contractor's Proposal, with these exceptions called out in Exhibit "A" of the Contract.

It is our understanding that the International system of units is required for use on all technical reports, publications and visual presentations, however, that system of units is not required on the drawings or in the Operation and Maintenance Manual to be supplied with the High Bit Rate Mass Data Storage Device.

Leach Corporation is very pleased to have this opportunity to participate in another of the important programs at the George C. Marshall Space Flight Center.

Please direct all communications to the undersigned who has been given the full administrative responsibility for the contract on behalf of Leach Corporation.

Very truly yours,

LEACH CORPORATION
Controls Division

R. Goulette
Contract Administrator

RG:mm

Enclosures

TECHNICAL PROPOSAL

SECTION I

CONTENTS:

	1.0	Introduction
	2.0	Specification Compliance
	3.0	System Description
	4.0	Summary Specifications
Appendix A	Operation and Maintenance Manual Publication 203273	

1.0 INTRODUCTION

Leach Corporation , Controls Division, offers the Model MTR-7114-1 Magnetic Tape Recorder/Reproducer System with HDDR®-II digital electronics in response to NASA-MSFC RFQ 8-1-2-40-23068 and Equipment Specification GC-110467. This technical proposal describes the equipment offered.

Leach supplied a high bit rate digital data system to the U.S. Air Force over a year ago, which has been in regular use in an airborne environment. This equipment is capable of reading and writing 24 M bits per second, using 12 parallel tracks on a standard IRIG 14 track MTR-7114. The system proposed to NASA is a modification of the Air Force System, capable of handling 10M bits per second and with improved performance. The Air Force unit is presently exhibiting an error rate of 1 in 10^7 or better in an aircraft environment.

The following sections describe the design approach, and include as an appendix the Operation and Maintenance Manual for the Air Force recording system.

2.0 SPECIFICATION COMPLIANCE

Leach has analyzed the NASA-MSFC Equipment Specification GC-110467 in detail and compared our offered equipment. The following paragraphs are numbered to match GC-110467.

2.1 SCOPE

Accepted

2.2 APPLICABLE DOCUMENTS

Specifications

Federal

Military

MIL-D-1000	Drawings, Engineering & Associated Lists	Accepted

George C. Marshall Space Flight Center

MSFC-SPEC-331	Enclosures, Modular, Shielded, Radio Frequency Interference, Specification for

The Leach MTR-7114-1 recorder, and HD103 high density encoder/decoder mounts in a standard RTMA 19-inch panel opening rack. Although this proposal does not include the racks, we assume our equipment will fit the MSFC racks.

Standards

Military

MIL-STD-1472	Human Engineering Design Criteria for Military Systems, Equipment and Facilities
MIL-STD-454	Standard General Requirements for Electronic Equipment

Since the recorder is off-the-shelf and the HD103 is a modification of an existing design, we assume this design specification does not apply.

MS-33586A	Metals, Definition of Dissimilar	Accepted
MIL-STD-100A	Engineering Drawing Practices	Accepted
MIL-STD-480	Configuration Control - Engineering changes, deviations, and waivers.	

Since relatively little design effort is required, conformance to this specification is not included in this proposal.

George C. Marshall Space Flight Center

MSFC-STD-421A	Electrical Support Equipment, General Design Requirements for	

Since the recorder is off-the-shelf and the HD103 is a modification of an existing design, we assume this design specification does not apply.

MSFC-STD-275A	Marking of Electrical Ground Support Equipment, Front Panels, and Rack Title Plates	Accepted

George C. Marshall Space Flight Center (MSFC) Documents

MSFC-PPD-600	Electrical Preferred Parts, Volume I and Volume II	Accepted

3.0

3.1 PHYSICAL

Accepted

3.2 MAINTAINABILITY

Since the Leach MTR7114 recorder is an off-the-shelf unit, we assume the requirements of paragraph 5.9 MIL-STD-1472 do not apply.

Subparagraphs a, b, c, and d are accepted.

3.3 OPERATIONAL AVAILABILITY

Accepted with limitations as detailed under 3.6.4.

3.4 SAFETY

Accepted with comments noted below.

3.5

3.5.1 Equipment Safety

The MTR7100 is an off-the-shelf design following best commercial practice.

3.6 ENVIRONMENT Accepted

3.6.1 Natural Environment Accepted

3.6.1.1 Ambient Temperature Accepted

3.6.1.2 Relative Humidity Accepted

3.6.1.3 Altitude Accepted

3.6.1.4 Vibration Accepted

3.6.2.1 Electromagnetic Interference

The MTR7114-1 recorder was designed to meet MIL-STD-222. It is being operated in many areas requiring EMC control.

3.6.3 Transportability — Accepted

3.6.4 Storage

Tape recording equipment may require bearing relubrication if stored 5 years without operation.

3.7 SYSTEM DESIGN AND CONSTRUCTION STANDARDS

Accepted as modified by subsequent paragraphs.

3.7.1 General Design and Construction Requirements

The equipment is designed to "best commercial practice", and may not meet all applicable paragraphs of MSFC-STD-421A.

3.7.1.1 Materials, Parts and Processes — Accepted

3.7.1.2 Standard and Commercial Parts — Accepted

3.7.2.1 Primary Power — Accepted

3.7.2.2 Transient Suppression

The MTR7114-1 and HD103 may not meet the MSFC interpretation.

3.7.2.3 Grounding and Shielding — Accepted

3.7.2.3.1 Equipment Ground — Accepted

3.7.2.3.2 Shields — Accepted

3.7.2.4 Wiring and Cabling

The MTR7100 recorder is designed to "best commercial practice" and may not meet all the subparagraphs of MSFC-STD-421A, paragraph 5.7.8.

3.7.3 Mechanical Design and Construction Requirements — Accepted

3.7.4 Moisture and Fungus Requirements — Accepted

3.7.5 Corrosion of Metal Parts

An exception is required to this paragraph for all magnetic tape recorders, since the head pole pieces are not protected and are subject to corrosion when the equipment is left unused in a corrosive environment.

3.6.6	Contamination Control	Accepted
3.7.7	Interchangeability and Replaceability	Accepted
3.7.8	Identification and Marking	Accepted
3.7.9	Workmanship	Accepted

3.7.10 Human Performance

Within the constraint that the proposed equipment is very compact and contains many controls and adjustments, MIL-STD-1472 will be used as a guideline during design of the HD103.

We assume that MIL-STD-1472 does not apply to the MTR7114, which is an existing standard Leach product.

3.7.11 Requirements for Bulk Data Storage

Accepted within the clarifications and exceptions listed below.

3.7.11.1	Intersystem Interface	Accepted
3.7.11.2	Input Data Format	Accepted
3.7.11.3	Input Data Rate	Accepted
3.7.11.4	Input Clock	Accepted
3.7.11.5	Output Data Format	Accepted
3.7.11.6	Output Clock	Accepted

3.7.11.7 Output Characteristics

Accepted with limitations noted below.

3.7.11.7.1 Bit-to-Bit Jitter

The tolerance of .25% calls for a maximum jitter of .25 ns, which will be

extremely difficult to measure and impossible to obtain with conventional techniques.

The data will be dejittered by an output buffer, and clocked out of the parallel-to-serial converter with a crystal derived clock having a stability of one part in 10^6.

All logic will be implemented with Schottky clamped TTL logic. Thus the jitter will be a function of the repeatability of this logic and not the tape recorder.

The jitter should be less than 3 ns.

3.7.11.7.2 Cumulative Jitter

Based on the above discussion, the jitter should be less than 3 ns over a 400-bit sequence.

3.7.11.7.3 Short Term Bit Error Rate

Since the tape is not certified to be error free with the proposed recording technique, some tape selection will be necessary to meet this error specification. In carefully reviewing this specification in conjunction with the proposed system, it can be seen that missing or extra clocks constitute the most serious errors since they cause loss of synchronism in the parallel-to-serial converter and erroneous positioning of data in the deskew buffers.

This would cause loss of an entire block of 128 x 12 bits, if it occurs near the start of the block.

Thus, tape with dropouts ranging into the noise floor would have to be culled from the usable tape supply.

The data recovery system will recover data with 20 dB dropouts readily, and provided a minimum amount of tape selection is done, the proposed system will meet the required error rate.

3.7.11.8 Tape Interchangeability Accepted

3.7.11.9 Tape Quality

3M971 high energy tape is recommended in lieu of 3M888. Type 971 is readily available.

3.7.11.10 Tape Reels — Accepted

3.7.11.11 Controls

The MTR7100 has a compatible control system with this paragraph, except that both forward and reverse record and playback operation is obtainable. The command nomenclature is slightly different.

The remote control function must be implemented with open collector drivers for the record, forward, reverse, fast forward, fast reverse, and stop functions. TTL compatible power ON/OFF remote function is not available.

3.7.11.12 Operation Status Indications

Status indications are grounds, intended to provide a ground for a 28V remote indicator lamp.

3.7.11.13 Starting/Stopping Operation — Accepted

3.7.11.14 Start/Stop Time

The start/stop time of the standard Leach MTR7114-1 is 6 seconds, at 120 ips and approximately 3 seconds at 60 ips, the proposed operational speed.

3.0 SYSTEM DESCRIPTION

By examining certain key requirements, it is possible to narrow down the alternatives to the design quickly. The tape reel specification along with the tape type indicates a requirement to avoid a rotating head machine or a high-speed flangeless real approach such as the Newell concept. A more conventional IRIG 14-inch reel instrumentation recorder is desired.

Since the record time is stated as 30 minutes continuous and because of the nature of the data, a track switching technique with tape reversals at each end is undesirable. This leaves us with a 14-inch NAB reel machine operating at a maximum tape speed of 60 ips to provide 30 minutes record time.

The per track bandwidth is the next major recorder parameter to be chosen. This parameter will then, in turn, set the tape width at either 1/2 or 1-inch.

Error rate as a function of maintenance is the real limitation to tape recorder packing density.

A desirable, although not necessarily mandatory, feature of the equipment is to be able to operate within the error rate specification of no more than 10 errors in any one second period over a reasonable period of time, measured in days or weeks rather than hours.

Thus the packing density per tape track should be as low as possible, but consistent with IRIG standard track widths and spacing; "double density" coding such as HDDR-II® code should be used on tape to reduce the density as much as possible consistent with machine-to-machine compatibility. Because of these factors, a 14-track system is selected with data recorded on 12-tracks, one servo track and one spare track on a standard 14-track IRIG interlace 1-inch tape system. Choice of this configuration will allow tapes to be played back on standard wideband equipment. A data packing density of slightly more than 14K bits/inch/track can be achieved.

Leach Corporation and others have delivered equipment operating successfully at higher packing densities and at less than the specified error rate. The configuration of the recorder has now been defined to be a wideband 1-inch tape, 14-inch reel machine with a standard 14-track IRIG head configuration.

Furthermore, it is desirable that the tapes could be reproduced on any IRIG Group II wideband machine suitably equipped with a format converter as a physically external "black box".

This approach has been used successfully with the Leach HD102 converter up to 16.6K bits/inch and data rates up to 1M bit/sec/track. The converter operates with any direct record wideband recorder having phase equalization, with no special adjustments required.

We propose to satisfy this requirement with a new converter and a standard Leach Wideband recorder, the model MTR7114. Operation of the converter is as follows:

The serial input is first applied to a serial-to-parallel converter, the outputs of which drive 12 identical encoder/decoder channels. (Refer to Figure 1.)

Each of these channels contains the necessary electronics for encoding and simultaneously decoding the analog signal off tape.

In order to maintain synchronism of the 12 channels of reproduced data after being subjected to recorder dynamic and static tape skew, a sync word 9 bits in length is added every 128 bits. The sync word is used during playback to synchronize the deskew buffers, thus lining up the channels for parallel-to-serial conversion.

Since data cannot be lost when sync is inserted, the actual recorded data rate must be higher than the 10 megabit incoming rate. This rate is exactly 137/128 higher and is accomplished via a phase lock loop circuit and counter.

Before being recorded, the data is converted to a double density code and low pass filtered to remove the high frequency components which would "beat" with the recorder's bias frequency. On playback, the double-density coded signal coming from the recorder's reproduce amplifier is decoded using a Leach proprietary circuit.

A portion of the decoding circuitry is a unique digital circuit which compensates for the "galloping baseline" or shifting dc level produced by all double density codes.

These codes, while allowing an approximate increase in packing density of 30% (with the same error rate) compared to biphase codes, are pattern sensitive. That is, the signal contains a DC level which is dependent on the pattern of 1's and 0's.

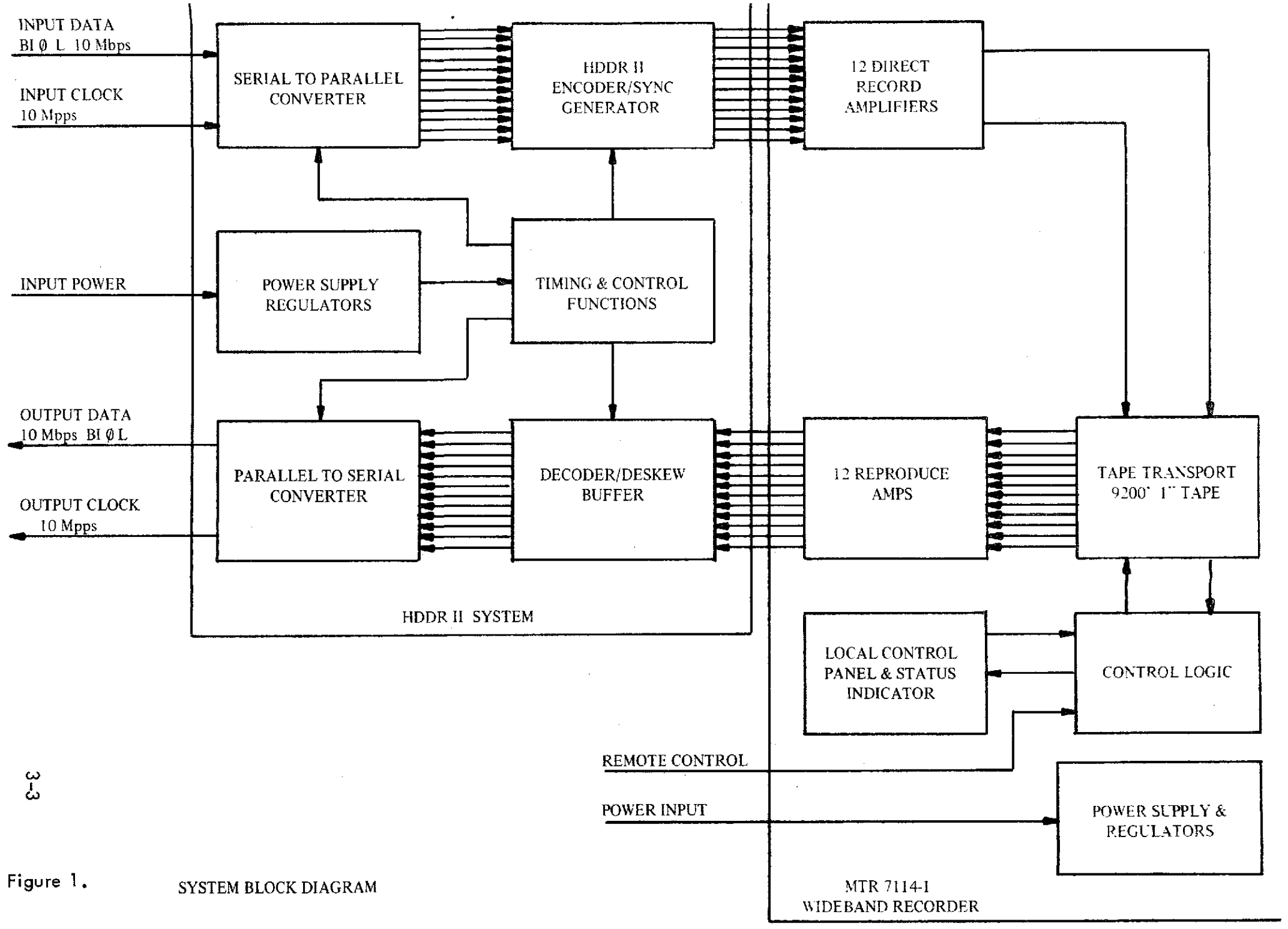


Figure 1. SYSTEM BLOCK DIAGRAM

To successfully decode the zero crossings of the analog signal from the tape requires a compensation circuit to recognize the shifting DC level.

It is this circuit that Leach Corporation has developed, and a patent is pending.

The sync code is detected and used to control the counter and control circuit, which determines the time at which the buffer register begins the load cycle. Data blocks of 128 bits enter the buffers at a different time, but are unloaded at the same time through use of a crystal controlled clock and associated counter/control circuit.

The sync word is automatically discarded during the load operation of the buffer, and in order to maintain the data input rate (less sync) equal to the output rate (which is controlled by the crystal), the tape recovered clock is phase locked through the recorder servo to the buffer unload crystal controlled clock. Short term jitter is, of course, removed from the data by the deskew buffer.

The output of the 12-channels is applied to a parallel-to-serial converter which is reset every 128 incoming bits to preclude a data skew condition from continuing indefinitely.

The data conversion unit is self-contained and requires 10-1/2 inches of panel space. Channel modules containing the electronics are plug-ins, for ease of maintenance. Modular power supplies are included in the main frame as well as the "housekeeping" electronics such as the crystal-controlled oscillator, which is common to all channels.

A complete description of a similar system developed for the Air Force is presented in Appendix A.

4.0	SUMMARY SPECIFICATIONS	
4.1	INPUT	
4.1.1	Data Rate	10^7 bits/sec
4.1.2	Format	Biphase TTL compatible
4.1.3	Clock	10^7 pulses/sec 50% Duty cycle TTL compatible
4.2	TRANSFER AND STORAGE REQUIREMENTS	
4.2.1	Record Time	30 minutes
4.2.2	Bit-to-Bit Jitter	Data bit period shall be within 3% of the preceding bit period (3 ns)
4.2.3	Cumulative Jitter	Less than +3.0% bit period for any 400 bit sequence ($\pm$ 3 ns nominally)
4.2.4	Error Rate	One in 10^6 for any 1 second period of time
4.3	OUTPUT CHARACTERISTICS	
4.3.1	Data	Biphase level TTL compatible
4.3.2	Data Rate	10^7 bits/sec
4.3.3	Output Clock	Synchronous with the data - TTL compatible

4.4 TAPE HANDLING CHARACTERISTICS

4.4.1	Interchangeability	Shall be capable of playback on similar equipment
4.4.2	Tape Type	3M888 or 3M971
4.4.3	Tape Reels	NAB Standard 14 inch diameter
4.4.4	Load/Unload	Coplanar reels

4.4.5 Controls

- Record
- Reproduce
- Fast Forward
- Rewind
- Stop
- Remote Control

ALL ABOVE SIGNALS FROM TTL COMPATIBLE CONTROLLER.

4.4.6 Status Signals

- Record mode
- Reproduce mode
- Rewind mode
- Fast forward mode
- Stop
- Tape Supply at BOT
- E.O.T.
- Record Ready
- Reproduce Ready
- Remote Indications

ALL ABOVE SIGNALS FROM RECORDER SHALL BE TTL COMPATIBLE IN ADDITION TO LOCAL.

4.5	POWER	115-120V 60 Hz Industrial Power
4.6	ENVIRONMENT - OPERATING	
4.6.1	Temperature	+40°F to +110°F
4.6.2	Humidity	Up to 60%
4.6.3	Altitude	Up to 5000 ft

APPENDIX C

TECHNICAL DISCUSSION

ON

DOUBLE DENSITY CODES

Prepared by

LEACH CORPORATION/CONTROLS DIVISION
717 North Coney Avenue
Azusa, California 91702
(213) 334-8211

DOUBLE DENSITY

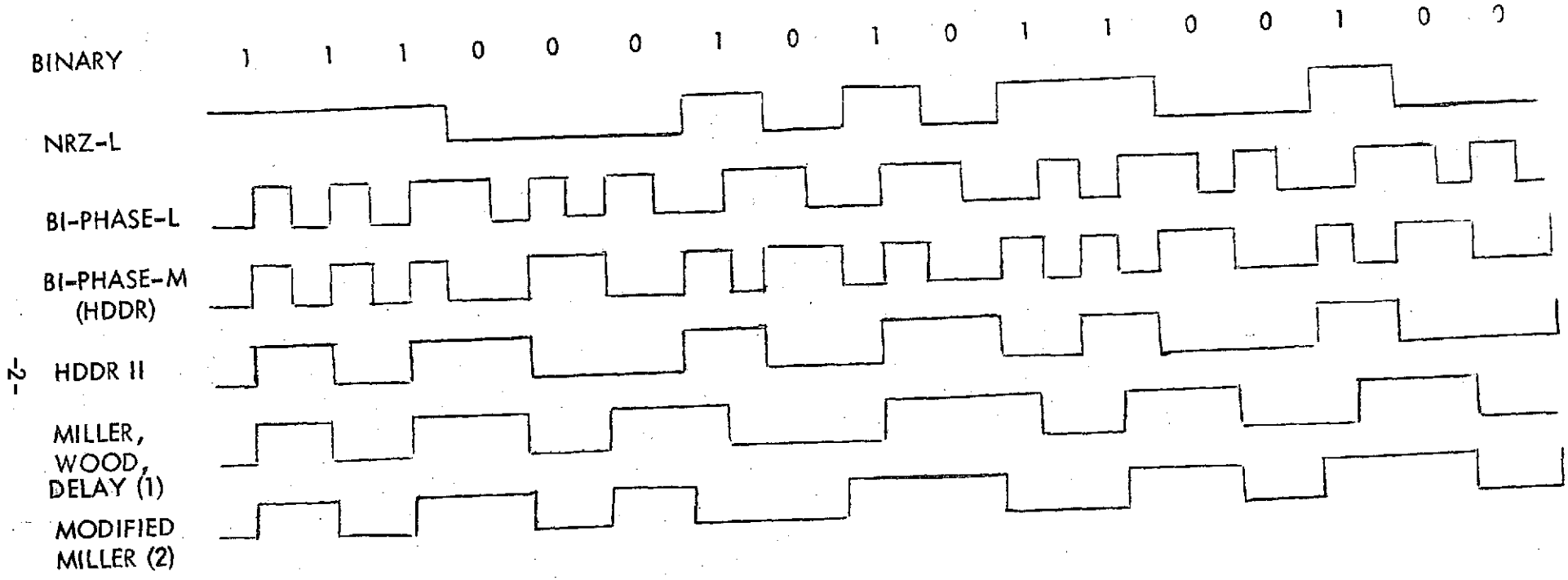
Summary

Double-density codes are compared with bi-phase codes in density attainable, bandwidth required, complexity in decoding, and start-of-record synchronization. A little information theory proves that the logical extensions of double-density to triple-or quadruple-densities are not recoverable by any decoder means. Error detection received special emphasis because double density codes are especially pattern sensitive. Means for both acceptance and quick look error detection are suggested. Described is a double-density code, HDDR II, and means for decoding that compare favorably with other known means. A "performance additive" is a feedback technique that compensates for the galloping baseline that plagues all double-density schemes. Breadboard tests of the described scheme show performance at 30.0 kbpi with error rates less than 1 in 10^6 typical. At these densities the magnetic tape must be very clean. It is recommended that potential customers for any type of double-density equipment be warned to insist that demonstration test patterns properly exercise potential galloping baseline problems.

General

Double-density codes are so named because they require a maximum of one transition per bit compared with two transitions for bi-phase. Just as there are different bi-phase codes, so there are different double-density codes. Figure 1 displays the common codes from each family.

A bi-phase code is recognized by noting either one or two units of delay between transitions. Also, groups of "ones" contain even numbers of "ones". Double-density codes utilize two, three, and four units of delay with an even number of "threes" between "fours".



(1) Miller, Wood, Delay are surprisingly all the same although different descriptions and mechanizations are used by their originators. It is merely Bi-phase L toggled.

(2) Transitions occur on the end of every "zero" and in the center of every "one" except "ones" immediately preceded by "zeros".

FIGURE 1

Double-density and bi-phase are names of families of codes. There is generally too much emphasis laid on the merits of an individual code within a family. People tend to speak of SØM or Miller codes as though the individual codes determined the performance attainable. The performance, of course, is determined by the decoder which solves the problems of the family of codes. A particular code may be easier to instrument with a given decoder than another code but these problems are generally not significant. For example, the HDDR decoder comprising a one - bit delay and exclusive OR gate is a "matched'-filter" detector of all bi-phase codes. It will optimally decode not just SØM but the other members as well (with suitable post-detection digital conversion logic).

DENSITY ATTAINABLE

Although only half as many transitions are required, nowhere near double the density can be attained with double-density codes. There are three limitations at work here. In order of decreasing significance, they are: choice between three delays instead of two; galloping baseline; no known "matched filter" or other optimum detector.

Extra Delay Choices

The information is contained in the delays between transitions. If double-density codes were operated at twice the density of bi-phase, the "eye openings" in the playback waveform would be half as wide as bi-phase. Signal to noise ratio would have to be 6 db greater to compensate. Also, the ordinarily troublesome pattern-sensitive phase shifts of the recorder and equalizers would have to be twice as good. These sources of error have already been optimized for bi-phase, thus, double-density must come down considerably from twice density.

Galloping Baseline

Double-density codes have a DC component that is not preserved through playback. Different bit patterns produce different DC magnitudes. The worst offender would be a "four", "two", "four", "two", ...pattern. In this case, the DC component would be -33.3% of the 0-peak signal voltage. Figure 2 shows a 3,3,3,3,2,4,2,4,2,4 pattern after loss of its DC component.

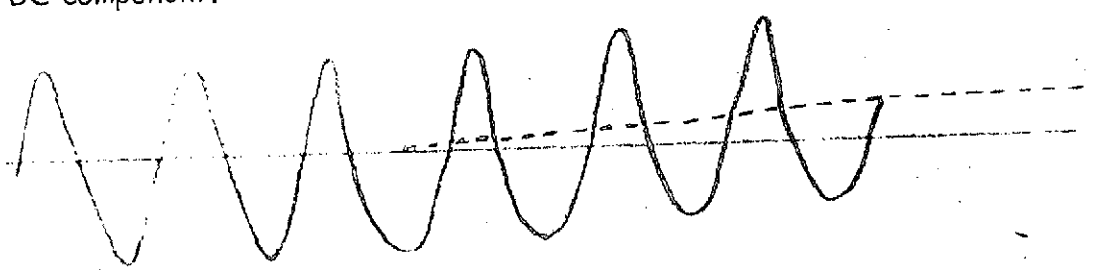
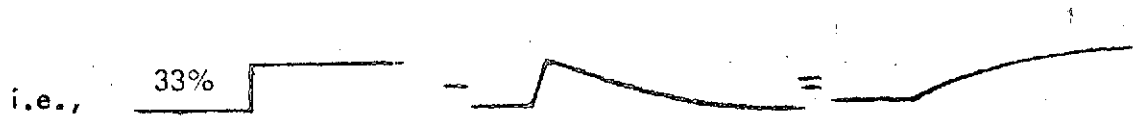


FIGURE 2

The envelope and the ideal zero-crossing threshold (dashed line) have shifted up exponentially. The shape of the envelope shift and its final value are functions of the low frequency response of the recorder. More precisely, if a 33% DC shift occurred in the waveform, the playback envelope would equal a 33% step function minus the recorder's step function response.



Using a fixed threshold detector, the envelope shift in the above waveform has a strong tendency to make "threes" of the "twos" and "fours". This effect is lessened by reducing the density and allowing the resulting harmonics to make more vertical transitions through the threshold (Figure 3).

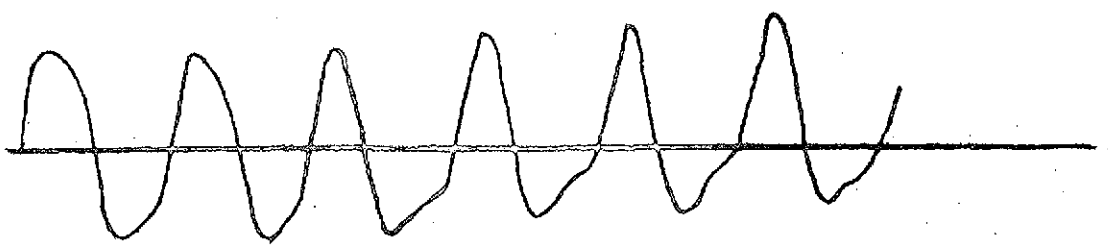


FIGURE 3

To quantitatively assess this problem it would be necessary to relate its effect on closing the "eye openings" of the waveform and then calculating the necessary signal-to-noise ratio increase to maintain the same error rate. The packing density would then be reduced a calculable amount to provide this signal-to-noise ratio increase. "Eye opening" closure is measured by calculating the time displacement of zero crossings made by a finite slope shifting up and down 33 1/3%. The slope is a function of the upper frequency response of the recorder and equalizer; but increasing high frequency response by equalizer adjustments also decreases the signal-to-noise ratio which must be accounted for.

All these calculations seem beyond the scope of this report, therefore, a quantitative evaluation will be abandoned.

No Optimum Detector

Codes in general are created with redundancies or self-checks often quite by accident. The entropy or unpredictableness is thus less than maximum. An optimum detector will utilize these redundancies to most efficiently reduce the error rate. The human brain, for instance, effectively uses word redundancy by listening more to phrases than to individual words. Aperture detectors classify transitions by the length of time from the last transition. They have no memory of previous classifications and, thus, throw away the redundancy or, at best, use it only to detect errors. This writer knows of no double-density detector that properly utilizes the double-density redundancy.

The extent of such loss may be calculated. Entropy is measured in bits of information (Shannons) per bit of data. The entropy of a digitally encoded signal as measured by an optimum detector is one Shannon per bit. A double-density aperture detector will measure a higher value. Random bi-phase data contains 1.5 transitions per data bit. Double-density, therefore, contains 0.75 transitions per bit. With each transition, the aperture detector decides whether it is a "two", "three", or "four". To determine the information content per decision, the a-priori probabilities of "twos","threes", and "fours" must be known.

Look at the bi-phase M and HDDR II waveforms in Figure 1. Suppose the last transition occurred at a bit cell boundary. Then for an HDDR II "two" to occur requires an NRZ "one" to have occurred, and the probability of this is 1/2. A "three" requires a "zero" followed by a "one"---probability of 1/4. A "four" requires a "zero" followed by a "zero"--- probability of 1/4. Now assume the last transition occurred in the midaie of the cell boundary. A "two" requires a "one" --- probability of 1/2. A "three" requires a "zero"---. Now every bi-phase M cell boundary contains a transition but only half the mid-points do. Therefore, HDDR II transitions occur twice as often at cell boundaries than at mid points.

Thus, the a-priori probabilites are:

"twos"	(2/3)	(1/2)	+	(1/3)	(1/2)	=	1/2
"threes"	(2/3)	(1/4)	+	(1/3)	(1/2)	=	1/3
"fours"	(2/3)	(1/4)	+	(1/3)	(0)	=	1/6

Although we used bi-phase M and HDDR II, the same relations hold for bi-phase -L and the double-density codes derived therefrom by merely referring to NRZ changes instead of "ones" and "zeros". Obviously, changes from zero to one and vice-versa are equally probable.

Now the average information per transition is:

$$1/2 \log_2 2 + 1/3 \log_2 3 + 1/6 \log_2 6 = 1.459 \text{ Shannons}$$

And the entropy is found by multiplying by the transitions per bit:

$$(0.75)\quad (1.459) = \underline{1.094} \text{ Shannons per bit}$$

Thus, an aperture detector yields a 9.4% loss. Stated another way; since the redundancy is not utilized for error correction, a code with 9.4% fewer transitions could just as well been used for a 9.4% increase in packing density.

Total Effect

Since the galloping baseline problem is too hard to quantitatively assess, the total effect will have to be sought empirically. An aperture detector was built and tested against HDDR performance. Performance testing shows that the double-density aperture detector performed 75% better than did HDDR.

TRIPLE AND QUADRUPLE DENSITIES

As a further exercise of the simple information theory in the previous section, consider triple density. Here, some bi-phase code is divided by three for an average transition density of 0.5 per bit. Dividing bi-phase by three yields transition lengths of 3, 4, 5 and 6. Assume the lengths equally a-priori probable (thus assuming maximum information per transition). The entropy, there is:

$$(0.5) \quad (4) \quad (1/4 \log_2 4) = 1 \text{ Shannon per bit}$$

This is the minimum possible entropy for a code to have and still be recoverable by any means. Less than this value indicates a loss of one-to-one correspondence between data and signal space; but, the maximum information condition of equally likely transitions lengths had been assumed. If this is true, then an average transition has length $(3 + 4 + 5 + 6)/4 = 4.5$. Now

the transition density is 0.5, therefore 2.25 units per data bit are required; but, as data bits are 2 units long, the transitions are obviously not equally likely and the average information is less than maximum. Thus, the entropy is less than the minimum value necessary for recovery by any means.

Even simpler is quadruple-density. Here transitions of 4,5,6,7 and 8 occur with a density of 0.375. Assuming the transitions equally likely again for maximum information, the entropy is:

$$(0.375) \quad (5) \quad (1/5 \log_2 5) \quad = \quad 0.87 \text{ Shannons per bit}$$

Again an unrecoverable code.

BANDWIDTH

Spectral densities are easier to measure than calculate. The bi-phase and double-density spectra for one million bit pseudo-random sequences are plotted in Figure 4.

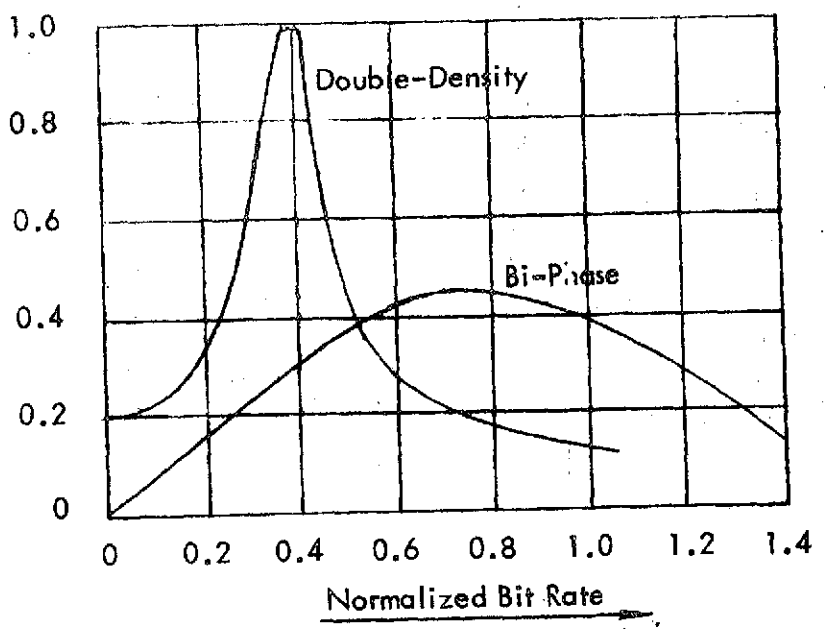


FIGURE 4

The highest low-frequency response required to pass these signals without appreciable error increase can be estimated by adding various RC high-pass networks between the recorder and the playback detector. Bi-phase thus appears to require low-frequency response of 0.4 times the bit rate. A value for double-density is harder to come by because of pattern sensitivity. However, using a 10^6 bit pseudo-random sequence, a 2 KHz maximum low-frequency response appears necessary for a 900 K bit/sec data rate at 30 ips. Oddly, this value appears optimum ---decreasing the cutoff point slightly increases the errors. This phenomenon likely suggests that the existing 400 Hz low end response of the tape recorder has a step function response not as suited for decoding as the simple RC filter. Lowering the RC cutoff brings the recorder cutoff into view and could thus be accentuating the galloping base-line problem.

ERROR DETECTION

Pattern Sensitivity

Double-density error detection is evolving into a fine art. The unusual pattern sensitivity of double-density is forcing this state of affairs. It has become increasingly obvious that there is no absolute worst-case pattern independent of equalization. Although certain patterns are undoubtedly harder to recover than others, no outstanding worst-case pattern emerges. When a pattern seems to be a candidate for this honor, it always turns out that a playback equalizer adjustment or a change in the value of coupling capacitance to the decoder reduces the errors considerably.

The use of long pseudo-random (PR) codes appear to be the only way to set up the equalizer and certain other components in the system to ensure the best average adjustments. The PR codes should be at least many times longer than the ratio of bit rate to system low-frequency response. A million bits seems just adequate for general use. Using the equalizer settings for the PR code, worst case patterns can then be investigated.

Bit errors in the magnetic recording industry are getting increasingly difficult to define. One innovation, apparently spawned in the computer industry, is to ignore "recoverable" errors or errors that are not repeated on successive passes of the same record. Showing even greater ingenuity, some digital recording manufacturers are claiming immunity from media imperfections (dropouts). For example, in the Orion report of the Wood code, only "corrected" errors are reported. "Corrected" errors are those that remain after errors that occur in the same area of the tape are subtracted. Presumably the next step would be to combine these two innovations of definition and leave the manufacturer with no responsibility whatever for errors accrued on his equipment.

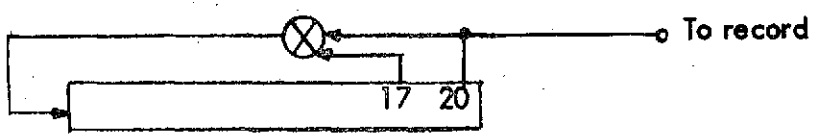
Unfortunately, this state of affairs is unlikely to come about and the manufacturer must reassess his responsibility in this area. Obviously there is no way to wiggle out of dropout induced errors. Dropouts are part of the a-priori conditions of real tape and the manufacturer must build his equipment to best perform with real tape. To claim dropout immunity so as to stress "theoretical" performance of decoding equipment is to admit failure of the theory employed to handle the statistical properties of dropouts. Comparisons between decoding equipments must be made during dropout conditions for, obviously, the prime value of a decoder is its ability to function through dropouts. But neither is this an open and shut case, for supposing one reel of tape were available and this tape had one big hole in it. Obviously, the value of statistical interpretation is being lost in attempting to characterize this one dropout.

Clearly, customers can be hurt more by one type of error than another. It may mean nothing to a user to back up and try to recover errors. Also, the distribution of errors may be important. A burst of 1000 errors is more acceptable to some users than 1000 single errors equally spaced. Other users are only hurt by burst errors. Another distinction is the clock-slip type of error; loss of sync can be devastating to some users. Therefore, the industry can continue to expect certain customers to weight certain types of errors in acceptance test procedures.

The need for a standard error definition still exists, however. Obviously, each bit by bit deviation from a known pattern should be recorded as an error; but what about loss of sync due to clock slip? This is not so obvious. How long should it take to recover sync? During sync loss every bit is meaningless to the user but the error detector signals errors randomly (a function of the auto-correlation properties of the test pattern). Is this satisfactory? The time to recover sync is a function of the length of the test pattern length. Should short patterns be rewarded this way? Double-density decoders in particular require very long sequences for adequate exercise. This emphasizes the stress placed on errors due to sync slip. How can a standard error definition be generally accepted when it requires the specification of the test pattern?

A Possible Solution

No solution will satisfy every aspect of the problem, but there is one technique that appears superior to the rest. This solution rests on the possibility of resynchronizing a 2^N-1 bit PR sequence in N bits after loss of sync. The normal methods of resynchronization including the delay and compare technique popular at Leach, require as many bits to resync as are bits in the pattern. With the new technique, however, a $2^{20}-1$ (one million) bit PR sequence can be resynchronized in 20 bits. This is accomplished as follows. The $2^{20}-1$ bit sequence is generated for recording by exclusive ORing the 17th and 20th bits of a 20 bit shift register and feeding that signal back into the input of the register.



The playback waveform is the input to a similar generator as shown in Figure 5. As soon as the register is full, the exclusive OR gate outputs the proper sequence in sync with the playback sequence. A bit by bit comparison is accomplished with exclusive OR gate A. A single bit error results in three pulses from this gate; one immediately, one seventeen bits later and one twenty bits later. It

does no good to divide the pulses by three to obtain the true error count because error bursts would then be miscounted by a factor of three. Instead, a third generator is employed (in feedback mode) and gate B compares the output of this generator with the playback sequence to obtain the true error count. The third generator is synchronized by transferring the contents of register C into register D if ever an error is detected at gate B simultaneous with no error at gate A.

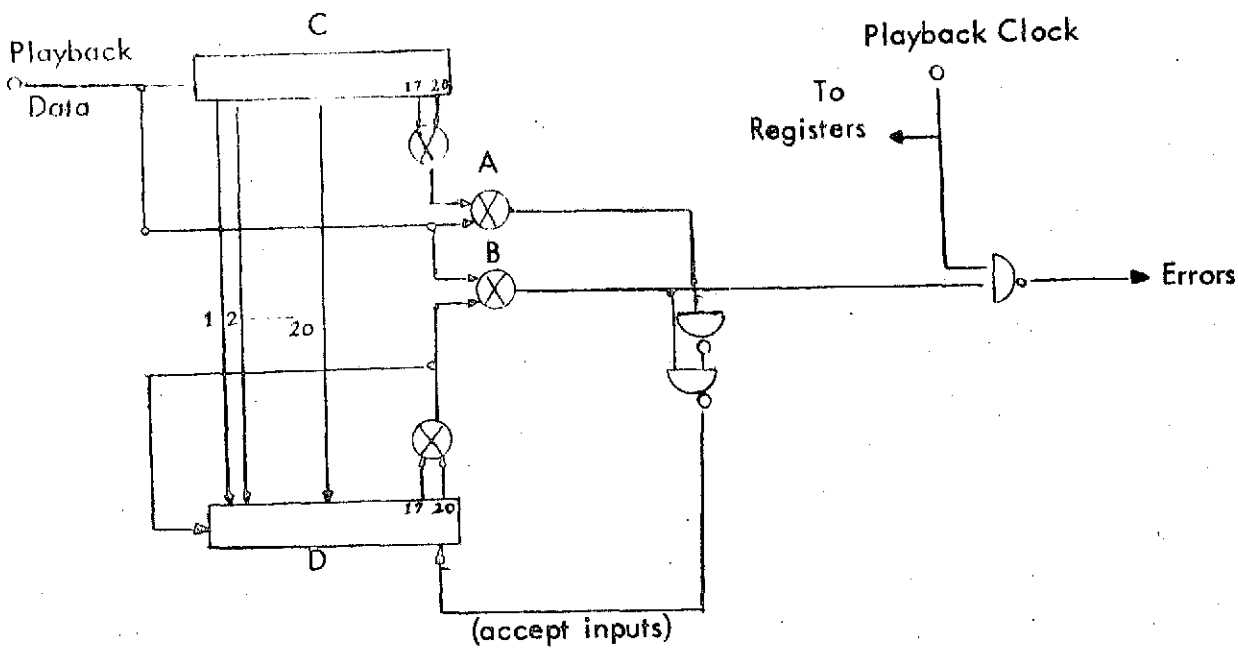


FIGURE 5

PR sequences are becoming more popular for testing. The recent HP PR sequence noise generator Model 3722A and HP binary sequence generator and processor Model 1930A are excellent responses to the demand for PR testing. In fact, the Model 1930A comes very close to fulfilling the recording

industries needs. Unfortunately, error detection synchronization on this model is implemented by a front panel push button (or can be arranged for automatic synchronization but with three times the output errors). Other minor problems make the Model 1930A an unattractive purchase for error detection.

Although the long PR sequence approach is attractive from several angles it will not, of course, guarantee that no other pattern can be found that generates more errors. The long PR sequence comes closer to actual real world operating conditions and should be readily accepted in spite of this possible shortcoming. The long PR sequence offers an attractive means to comparing equipment of different manufacturers since it displays such a wide variety of bit combinations.

Worst Case Patterns

The worst case pattern is the one that gives the greatest number of errors to a particular decoder. It is difficult to tell which of many patterns actually deserves this title, so there come to be many "worst case" patterns. The quotation marks indicates the use of worst case to mean more than one possible. "Worst case" patterns are characterized by strong DC components coupled with a certain degree of randomness. A "worst case" pattern for one double-density decoder is therefore a likely "worst case" pattern for another double-density decoder design.

Some care must be exercised is specifying "worst case" patterns by their NRZ data components alone. The reason is that there are often two double-density realizations of each NRZ pattern depending on whether the initial transition corresponds to a mid cell or cell boundary transition. When NRZ patterns are specified it should be done so assuming the first transition to occur at a cell boundary. This will be called "normal phase". When reverse phase is required, it should be so indicated. When setting up a pattern generator to a given sequence, the resulting double-density pattern should be checked on the scope to verify proper phasing. Power to the generator can be interrupted or the sequence reset from another pattern if the phasing needs to be bumped to the other state. Phasing a test pattern, of course, has nothing to do with normal

operation of the decoder, it is only necessary when repeated results must be obtained from certain "worst case" patterns and ensures that the desired DC components will be obtained. Following are the two states of a certain 20 bit sequence.

NRZ Sequence	1	1	0	1	1	1	0	0	1	0	0	1	1	1	0	0	1	1	1	0
HDDR II (Normal phase)	2	2	3	2	2	3	3	3	3	2	2	3	3	2	2	3				
HDDR II (Reverse phase)	2	3	2	2	2	4	2	4	2	2	2	4	2	2	2	3				

The normal phase pattern spends half of the time at each polarity for a resultant zero DC component. The reverse phase pattern favors one polarity 60% of the time showing a strong DC component. Some NRZ sequences cycle from normal to reverse phases at each completion of the fundamental NRZ pattern.

Twenty bit patterns are favored over other lengths for testing "worst case" conditions because the standard means for checking errors (using a 20 bit delay and compare) results in sync recapture after 20 bits --- exactly the same as the PR tester described above. Thus, direct error comparisons can be made between the two types of sequences.

Quick Look Detection

Opposed to the more formal acceptance type of error detection, double-density is blessed with a "quick look" capability. This capability originates in the slight information redundancy of the codes expressed in the restriction that an odd number of "threes" can't occur between "fours". If a flip-flop is toggled by "threes" and reset by "fours", the state of the flip-flop just prior to being reset must always be true. If not, an error has occurred. In the HDDR II decoder, to be discussed, this flip-flop is in the circuit already for other reasons so it remains only to sense the state of it prior to reset and thus control a visible indicator. Fortunately, all errors involve the parity of "threes"; i.e., if incoming "twos" or "fours" are misread, they will be misread as "threes" unless a very gross problem occurs. The only way to sneak an error past this detector

is to get an even number of errors between "fours" or to arrange the incoming data to not have any "fours".

The advantage of quick look detection, obviously, is that it is pattern insensitive. It is thus convenient for the user to monitor this detector while receiving real-time data.

SYNCHRONIZATION

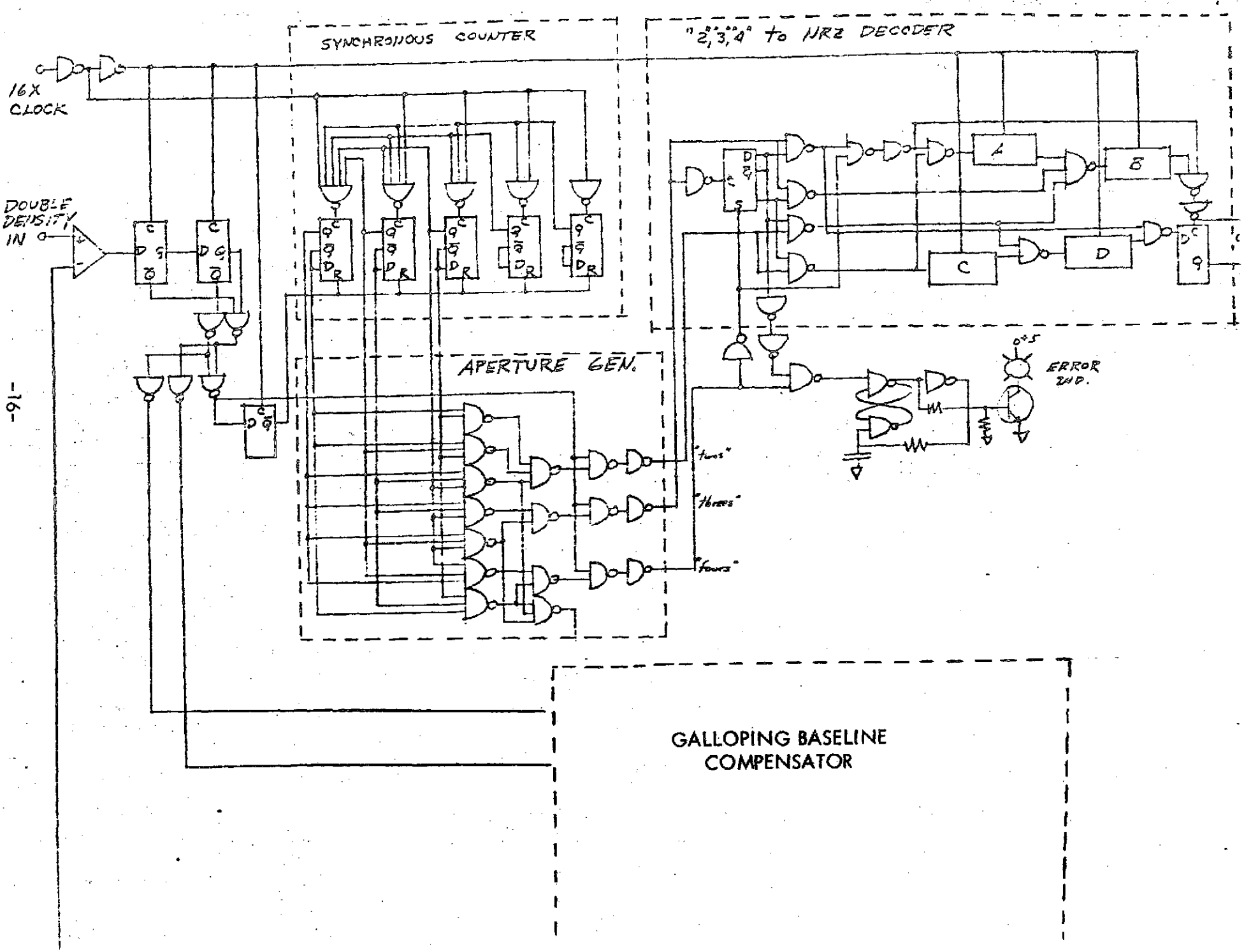
There are two sync problems ---data and frame. Data sync refers to the bit pattern necessary to initiate an ambiguous data detection. For bi-phase M this pattern consists of one or more zeros (which are found often enough in real-world data that no special consideration is given it). Double-density codes require a "four" in the signal for data sync. The Miller, Wood, or Delay codes generate "fours" only from 101 data patterns. HDDR II generates "fours" from 000 patterns and modified Miller requires 010 patterns. Whether this decreased probability of immediate recovery after sync loss is a problem or not is something only the potential user can answer.

Frame sync, of course, signals the major events of beginning and end of frames or records. Frame sync is generally unique, thus employing some signaling means orthogonal to the data signal. HDDR successfully uses zeros at two-thirds frequency to signal frame sync. Double-density codes could similarly use "sixes" (six units delay between transitions).
On playback, an aperture could be sensitive to the receipt of "sixes" thus signaling frame sync. Both schemes require, unfortunately, the interruption of data during frame sync. The question arises as to the applicability of the redundancy of double-density codes for frame sync instead of error detection. Unfortunately, such reworking of the code to capture this effect upsets the data sync capability.

AN HDDR II DECODER

An aperture decoder was constructed to decode HDDR II. The schematic is shown in Figure 6. A synchronous counter counts externally supplied 16X clock pulses and is reset by every incoming transition. A network of gates

FIGURE 6


SYNCHRONOUS COUNTER
"2,3,4" to NRZ DECODER
16X CLOCK
DOUBLE DENSITY IN
APERTURE GEN.
ERROR IND.
A
B
C
D
GALLOPING BASELINE COMPENSATOR

senses the state of the counter and opens three apertures corresponding to the three anticipated delays between transitions. The timing is shown in Figure 7.

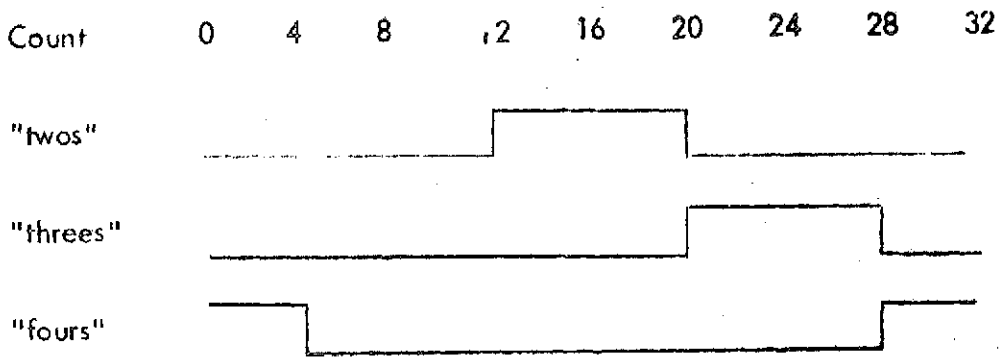


FIGURE 7

The incoming transition, just prior to resetting the counter, is "ANDed" with the three apertures resulting in a pulse from one of the three gates representing the decision for a "two", "three", or "four". Refer to Figure 8. Knowing the last duration between transitions is obviously insufficient to determine the NRZ data. It is necessary to additionally know whether the previous transition was generated from a bi-phase cell boundary transition or from a mid-cell transition. It is obvious on observation that "boundary" transitions occur whenever an even number of "threes" has followed a "four". Similarly "mid-cell" transitions occur after an odd number of "threes". Thus, a flip-flop keeps track of parity by being toggled with "threes" and reset by "fours".

Thus there are six possible conditions to decode--the three possible durations between transitions and the two parities of "threes". For each of these conditions, a data "one" may or may not be appropriate immediately, one cell later, or two cells later. Clock pulses are similarly required at various times. Table 1 indicates the appropriate timing of data "ones" and clock pulses to decode HDDR II. Eight-bit shift registers A and B provide the indicated half and one bit delays of clock pulses while registers C and D delay the data "ones" by half and one bits. Finally, the D flip flop lengthens the pulses corresponding to data "ones" and provides the NRZ data output.

CONDITIONS		DATA "ONE"			NRZ CLOCK		
Transition Duration	"Threes" Pority	Now	1/2bit delay	1 bit delay	Now	1/2bit delay	1 bit delay
Two	Even			X			X
Two	Odd		X			X	
Three	Even					X	
Three	Odd	X			X		X
Four	Even				X		X
Four	Odd				X		X

Table 1

TEST RESULTS

Leach MTR7000 transport (one inch) was used in all tests. Tape speed was 30 ips (the decoder synchronous counter would not permit faster operation). Using 3M 880 tape, tests were first run to determine the optimum amount of comparator feedback. This is summarized in Figure 8.

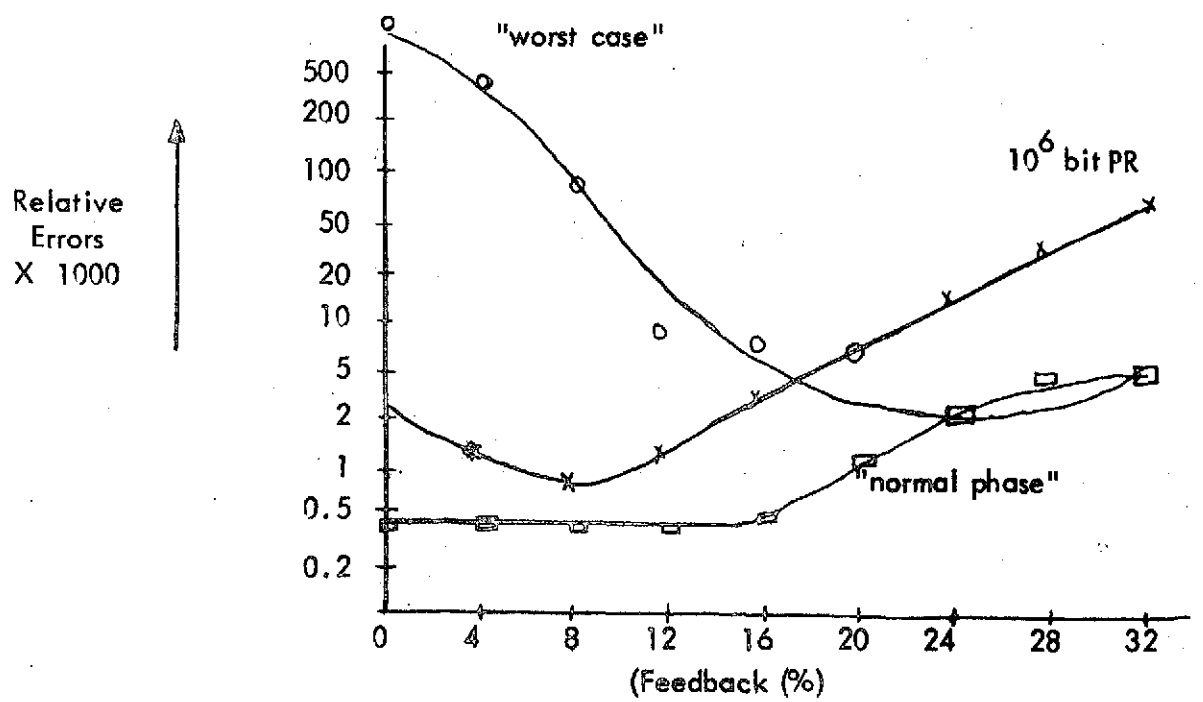


FIGURE 8

Test Results (Cont'd)

The equipment was optimized and equalized for the long PR sequence and subsequently tested at four percent intervals. Then a "worst case" 20-bit pattern was substituted and tested without reequalization. This pattern is the one given previously in Section 3.8.4 (the "reverse phase" pattern). Also, for comparison, the "normal phase" of the pattern was tested. All tests were run at 33 kbpi to ensure plenty of errors.

The "normal phase" of the pattern has no DC component, thus no improvement could be expected using feedback. Twelve to sixteen percent feedback appears to be a reasonable setting for general use.

Next, tests were run at different densities using 3M 888 tape except for two tests run with Leach LC-5 tape. For each tape type, the transport was reequalized for optimum performance at 33 kbpi using the long PR sequence. Tests at each density used 2000' of tape. The same 2000' were used on both tape types.

APPENDIX D

LTP NO. 204411

ORIG. DATE 1/9/73

PAGE 1 OF 8

LEACH CORPORATION
CONTROLS DIVISION
717 CONEY AVENUE
AZUSA, CALIFORNIA

ACCEPTANCE TEST PROCEDURE

HDDR-II

HIGH BIT RATE MASS DATA STORAGE SYSTEM

PREPARED BY R. E. CROWE

APPROVED BY 1-15-73

REL BY 1-15-73

REVISIONS

REV.	BY	DATE	CHANGE	PAGES AFFECTED

FORM NO. L-905

1.0 SCOPE

This Acceptance Test Procedure (ATP) in conjunction with Leach LTP 203333B for wideband tape recorder MTR 7000 series will demonstrate compliance to GMSFC specification GC110467 as modified by Leach Proposal 732639 and Leach letter dated 6/27/72, Subject Contract NAS8-28959.

1.1 The following requirements of GC110467 will be verified by inspection and/or analysis:

3.1 Physical

3.2 Maintainability

a. Parts replacement

b. Accessability

c. Connection of good equipment

d. Minimum hazard

3.3 Operational Availability

3.4 Safety

3.5 Personnel/Operator Safety (Modified)

3.5.1 Equipment Safety (Modified)

3.6 Environment

3.6.1 Natural Environment

3.6.1.1 Ambient Temperature

3.6.1.2 Relative Humidity

a. Operating

b. Non-operating

3.6.1.3	Altitude
	a. Operating
	b. Non-operating
3.6.1.4	Vibration
	a. Operating
	b. Non-operating
3.6.2.1	Electromagnetic Interference (Modified)
3.6.3	Transportability
3.6.4	Storage (Modified)
3.7	System Design and Construction Standards (Modified)
3.7.1.1	Materials, Parts, and Processes
3.7.1.2	Standard and Commercial Parts
3.7.2.1	Primary Power
3.7.2.2	Transient Suppression (Modified)
3.7.2.3	Grounding and Shielding
3.7.2.4	Wiring and Cabling (Modified)
3.7.3	Mechanical Design and Construction Requirements
3.7.4	Moisture and Fungus Requirements
3.7.5	Corrosion of Metal Parts (Modified)
3.7.6	Contamination Control
3.7.7	Interchangeability and Replaceability
3.7.8	Identification and Marking

3.7.9 Workmanship

3.7.10 Human Performance (Modified)

3.7.11.8 Tape Interchangeability

3.7.11.10 Tape Reels

3.7.11.11 Controls (Modified)

3.7.11.12 Operation Status Indications (Modified)

2.0 TEST SET-UP

The test set-up will be per Figure 1

All equipment except for Tektronix Model 7704A oscilloscope (which is leased equipment) and special test jigs will be in current certification per Leach calibration lab procedures.

3.0 TEST PROCEDURE

The following test procedure will be used to verify the requirements of GMSFC specification GC110467 paragraphs 3.7.11.2, 3.7.11.3, 3.7.11.4, 3.7.11.5, 3.7.11.6, 3.7.11.7.1, 3.7.11.7.2, 3.7.11.7.3, 3.7.11.9

3.1 Input Data Format and Data Test

Verify that the output of the pattern generator is operating in synchronism with the 10 Mb ±1% clock and that the format is bi-phase level as defined in Figure 2, using the Tektronix Model 7704A oscilloscope.

3.2 Input Clock

Verify that the phase relationship between the input clock and input data is per Figure 2, using the Model 7704A Tektronix scope.

3.3 Recording Time

Using an appropriate timing device, verify that the recording time exceeds 30 minutes at the tape speed used for recording the 10 Mb serial PCM data.

3.4 Output Data Format

Using the Model 7704A Tektronix scope, verify that the output signal is of the format in Figure 2, and that the output clock is of the correct phase.

3.5 Output Bit-to-Bit and Cummulative Jitter

Using the Model 7704A Tektronix scope, measure the bit-to-bit jitter cummulative jitter of the crystal controlled 10 Mb output clock, over 400 clock pulses. Note: This data will be used to compare with the output data measured jitter. Add a second trace to the scope showing the data. Repeat the measurement and record. The net difference is the "uncorrectable" jitter.

3.6 Error Rate Test

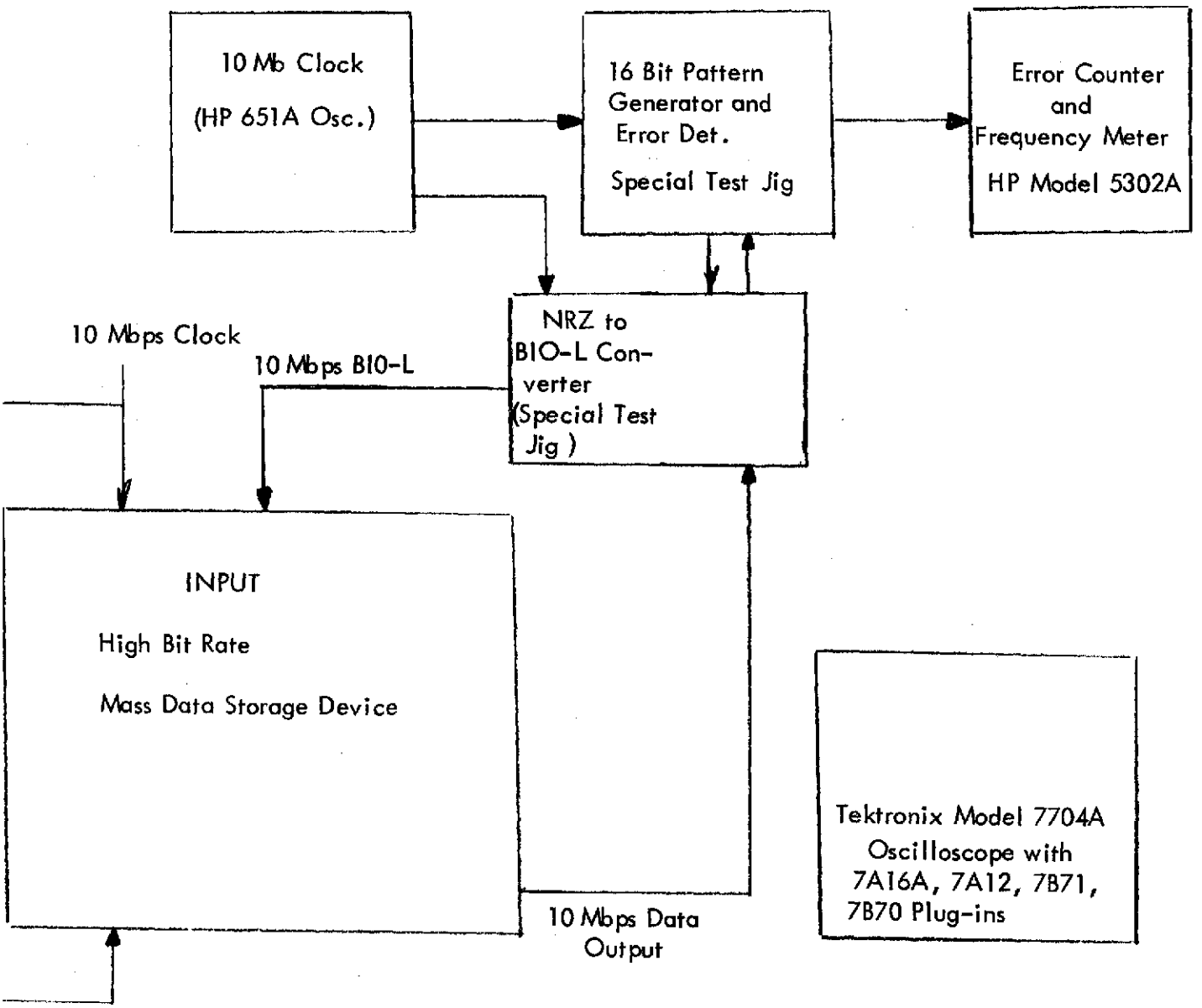
3.6.1 Load the recorder with a pre-selected roll of 3M 971 tape.

3.6.2 Connect the equipment as shown in Figure 1.

3.6.3 Put the recorder in the record/reproduce mode and when up to speed, reset the error counter.

3.6.4 Continue recording for 30 minutes.

3.6.5 At the end of this time, record the number of errors. Divide this number by (10^7) (60) (30) = 1.8×10^{10} to get the average error rate. It shall be less than 10^{-6} .



EQUIPMENT TEST SET-UP

FIGURE 1

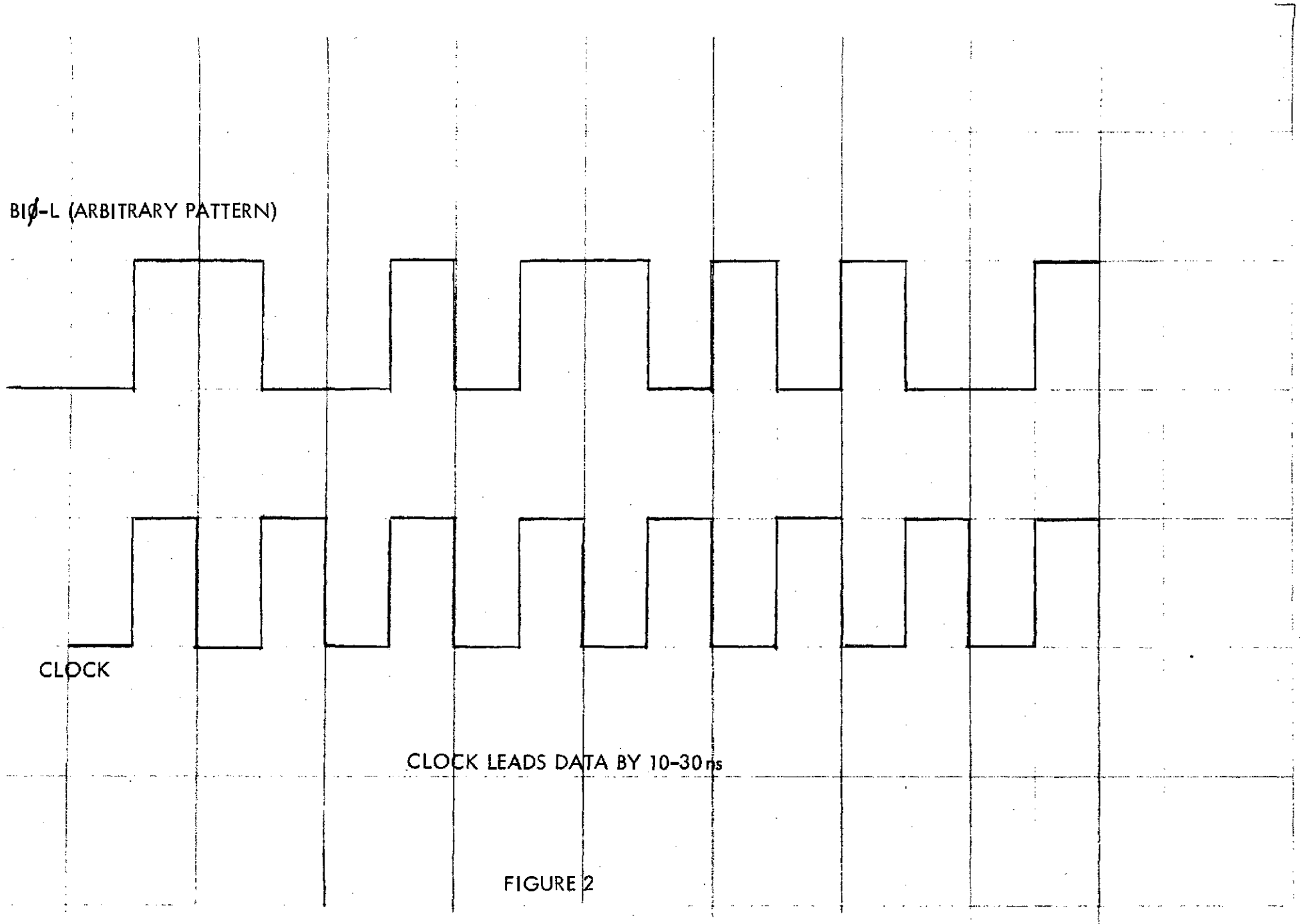


FIGURE 2

DATA SHEET

		Verify	Tolerance
3.1		OK	See Figure 2
3.2		OK	See Figure 2
3.3	30 Minutes		30 Minutes Minimum
3.4		OK	See Figure 2

Measurements

3.5

A.	Short Term Bit-to-Bit(Clock)	_____ ns	NO MEASURABLE JITTER.	N/A
B.	400 Bit Cummulative (Clock)	_____ ns		N/A
C.	Short Term Bit-to-Bit (Data)	_____ ns		N/A
D.	400 Bit Cummulative	_____ ns		N/A
C - A		ON 2 NS SCALE, NO MEASURABLE JITTER.		3 ns Maximum
D - B				3 ns Maximum

3.6 Error Rate

A = No. of Errors/30 Min. 1428

$\frac{A}{1.8 \times 10^{10}}$ = 0.0795 IN $(10)^6$ BITS — 10^{-6} Maximum

LEACH FT 20

L. L. L.
2-16-73