



DEVELOPMENT OF A
UNINTERRUPTED POWER SYSTEM -
AC & DC TO DC CONVERTER

by D. L. Cronin and A. D. Schoenfeld

TRW SYSTEMS

prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

PRICES SUBJECT TO CHANGE

NASA Lewis Research Center

Contract NAS 3-15827

Reproduced by
NATIONAL TECHNICAL
INFORMATION SERVICE
US Department of Commerce
Springfield, VA. 22151

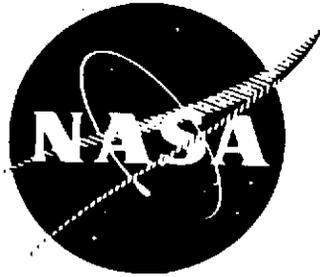
(NASA-CR-134497) DEVELOPMENT OF A
UNINTERRUPTED POWER SYSTEM: ac AND dc TO
dc CONVERTER (TRW Systems Group) 30 p
HC

34 CSCL 10B

N74-29413

Unclas

G3/03 44966



DEVELOPMENT OF A
UNINTERRUPTED POWER SYSTEM -
AC & DC TO DC CONVERTER

by D. L. Cronin and A. D. Schoenfeld

TRW SYSTEMS

prepared for

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

NASA Lewis Research Center
Contract NAS 3-15827

1. Report No.	2. Government Accession No.	3. Recipient's Catalog No.	
4. Title and Subtitle AC & DC to DC Power Processor Uninterrupted Power Systems		5. Report Date July 1973	
		6. Performing Organization Code	
7. Author(s) D. L. Cronin, A. D. Schoenfeld		8. Performing Organization Report No.	
		10. Work Unit No.	
8. Performing Organization Name and Address TRW Systems Group One Space Park Redondo Beach, Calif. 90278		11. Contract or Grant No.	
		13. Type of Report and Period Covered Contractor Report	
12. Sponsoring Agency Name and Address National Aeronautics & Space Administration Lewis Research Center 21000 Brookpark Road Cleveland, Ohio 44135		14. Sponsoring Agency Code	
		15. Supplementary Notes Project Manager: J. H. Shank Lewis Research Center Cleveland, Ohio 44135	
16. Abstract <p>This program covered the design, fabrication and testing of an advanced development model uninterrupted power system. The input and output requirements imposed on the power processor were specified such that the unit is electrically interchangeable with existing power systems used by the Federal Aviation Administration in installations which have a history of failure due to electrical transient conditions.</p> <p>It was the object of this program to transfer power processor technology, developed by NASA Lewis Research Center, to F.A.A. hardware requirements. To this end, the power processor is designed to be very versatile and as a result may be interchanged in several field applications.</p> <p>The AC & DC to DC Converter applies new technology in the areas of SCR Circuit Configuration (Series Inverters) and Advanced Control Concepts (ASDTIC).</p> <p>Input power is from either of two single-phase ac power sources or batteries with electronic selection and transfer between power sources. Battery reconditioning is automatic when either ac source is present. The output power is rated at 840W; the nominal output is 24V at 35A. Within the 840W limit, the regulated output voltage is adjustable from 22V to 30Vdc. Protection against continuous overloading or short circuit is provided.</p> <p>The unit is packaged in a standard 19-inch rack mount configuration with 7-inch panel height. Controls are on the front panel with power input and output through connectors on the rear surface. Cooling is by free convection from fin areas located on the side and rear panels. The packaged unit weighs 52.8 lbs., which can be reduced significantly if a three-phase ac power source is used.</p>			
17. Key Words (Suggested by Author(s)) Control Systems (ASDTIC) Uninterrupted Power Series Resonant Inverter		18. Distribution Statement Unclassified - Unlimited	
19. Security Classif. (of this report) Unclassified	20. Security Classif. (of this page) Unclassified	21. No. of Pages 34	22. Price* 4.50

* For sale by the National Technical Information Service, Springfield, Virginia 22151

FOREWORD

We would like to thank Mr. P. A. Thollot and Mr. J. H. Shank of the NASA Lewis Research Center, Cleveland, Ohio, for the technical guidance during the development. The contribution by Mr. E. F. Van Vlaanderen of F.A.A. in evaluation of the application requirements is also acknowledged.

PRECEDING PAGE BLANK NOT FILMED

TABLE OF CONTENTS

	<u>Page No.</u>
1.0 SUMMARY	1
2.0 INTRODUCTION	3
3.0 REQUIREMENTS vs. CAPABILITIES	5
4.0 ELECTRICAL DESIGN	7
4.1 Functional Description	7
4.2 Circuit Description	7
4.2.1 86V Bus	8
4.2.2 Series Inverter	10
4.2.3 EMI Filters	11
4.3 Series Inverter Characteristics and Equations	16
4.3.1 Steady-State Operation	16
4.3.2 Transient Operation	19
4.3.3 The Spillover Network	20
5.0 UNIT DESCRIPTION	22
5.1 Mechanical Characteristics	22
5.2 Mechanical Design	22
5.3 Electrical Characteristics	24
6.0 RELIABILITY PREDICTION	25
7.0 DISCUSSION OF TEST RESULTS AND RECOMMENDATION	26
8.0 UNIQUE FEATURES	28
9.0 CONCLUSIONS	29
10.0 REFERENCES	30

PRECEDING PAGE BLANK NOT FILMED

1.0 SUMMARY

This program covered the design, fabrication, and testing of an advanced development model uninterrupted power system. The input and output requirements imposed on the power processor were specified such that the unit is electrically interchangeable with existing power systems used by the Federal Aviation Administration in installations which have a history of failure due to electrical transient conditions. To this end the power processor is designed to be very versatile and as a result may be interchanged in several field applications.

It was the object of this program to transfer power processor technology, developed by NASA Lewis Research Center, to F.A.A. hardware requirements. The AC and DC to DC Converter applies new technology in the areas of SCR Circuit Configuration (Series Inverters) and Advanced Control Concepts (ASDTIC).

The application of the series-inverter technology has provided the following design features:

(1) Reduced Power Processor Weight

The inverter allows higher frequency operation of the power SCR's through the self-commutation as a result of the sinusoidal current developed.

(2) Higher Efficiency

The SCR switching conditions are ideal; the SCR current is essentially zero during the turn-on and turn-off periods.

(3) Improved Reliability

The reliability is greatly enhanced by the series-inverter configuration where component electrical stresses are inherently limited during transient and overload operations.

The use of ASDTIC control has contributed significantly to the capability of the power processor in isolating the electrical disturbances on the input power lines from the load. These disturbances include lightning, variable frequency input, slowly rising and falling input voltage, battery charging and discharging, and automatic transfer of power sources.

Input power is from either of two single phase ac power sources or batteries with electronic selection and transfer between power sources. Battery re-conditioning is automatic when either ac source is present. The output power is rated at 840W; the nominal output is 24V at 35A. Within the 840W limit, the regulated output voltage is adjustable from 22V to 30V dc. Protection against continuous overloading or short circuit is provided.

The unit is packaged in a standard 19 inch rack mount configuration with 7 inch panel height. Controls are on the front panel with power input and output through connectors on the rear surface. Cooling is by free convection from fin areas located on the side and rear panels. The packaged unit weighs 52.8 lbs.. This weight can be reduced if a three-phase ac power source is used to replace the single-phase sources presently available.

2.0 INTRODUCTION

Although the Silicon Controlled Rectifier (SCR) has been applied increasingly in power processing equipment for military and industrial applications, the full potential is just beginning to be realized in equipment applications requiring very light weight, very high efficiency, and superior performance capability. Through the utilization of unique circuit design techniques and by taking advantage of advances in component developments, large improvements in these power processing equipment characteristics are achievable. This report presents the results of work performed under Contract NAS 3-15827 for the Lewis Research Center to develop an equipment reflecting such state-of-the-art capabilities.

The specific objective of this contract was the development of an uninterrupted power system meeting stringent requirements on weight, size, efficiency and performance. The central part of the power system is a LC series resonant inverter using SCR's as power switches [1,2,3]. The power supply is rated at 840W, and furnishes a well regulated and transient free voltage over an adjustable output range of 22 to 30Vdc. Input power may be supplied from any of three input power sources: main ac, auxiliary ac, or battery. AC input power sources are 50 to 400Hz, 117V \pm 10%. The battery source is sized to supply maximum output power (840W) for 15 minutes minimum. The converter circuit interfacing with the input power source is mechanized in such a way that the converter can engage in its normal operation and satisfy all output specifications under any of the following power-source combinations: (1) main ac only, (2) auxiliary ac only, (3) battery only for 15 minutes, (4) main ac and auxiliary ac, (5) main ac and battery, (6) auxiliary ac and battery, and (7) main ac, auxiliary ac, and battery. Furthermore, automatic battery recharging will take place when either ac source is present.

The input ac power is modulated in conduction angle using SCR's, and is then rectified and filtered to obtain an 86Vdc bus. A series inverter operates from the 86V bus to accomplish the functions of voltage transformation, input/output isolation, and voltage regulation. The inverter output voltage is rectified and filtered to yield the desired dc output meeting the ripple specification. Standby batteries are floated across

the 86V bus. Through a bus current control loop, the battery charging current is automatically controlled as a function of the power supply output load. Maximum battery charging current occurs at the minimum-load operation.

A unique two-loop feedback technique embodying the use of an Analog Signal to Discrete Time Interval Converter (ASDTIC), provides the high static and dynamic performance characteristics of the power supply. [3,4].

Reliability is optimized by inherent circuit protection of the critical components during all conditions of overload and abnormal source voltages and by maintaining semi-conductor elements below their maximum ratings during turn-on, steady-state, and transient load and line conditions.

Reliability is further enhanced in that forced commutation of inverter SCR's is not required due to the self-commutation characteristics inherent in the series inverter configuration. Since the sinusoidal current developed in the series-inverter SCR's depends primarily on the well-controlled characteristic impedance of the LC series resonant circuit, the output short-circuit protection is thus inherently achieved. The significance of this protection cannot be overstressed in view of the low maintenance requirement imposed by unattended and remote installations.

3.0 REQUIREMENT VS. CAPABILITY

TABLE 1 SUMMARY OF REQUIREMENT VS CAPABILITY

Item	Requirement	Capability	NAS3-15827 Reference								
Input Power	<ol style="list-style-type: none"> 1. The converter shall operate from a main single phase ac power source with a nominal line voltage of 117V, rms, sinusoidal waveform, and frequency in excess of 50 Hz. 2. The converter shall operate for 15 minutes when the supply line voltage falls below 105V, rms, and including complete failure. During this period, the converter shall be powered from a storage battery. The battery voltage shall not vary by more than 5% during this 15 minute interval. 3. The converter shall operate from an auxiliary ac power source whose specifications are the same as those of the main ac supply as stipulated in Section E., 1.1. 	<p>Converter complies with requirement.</p> <p>Converter complies with requirement. Tested for full performance for 28 minutes. C&D batteries type 3DCU-3 39 cells.</p> <p>Converter complies with requirement. Automatic transfer between power sources.</p>	<p>E., 1.1</p> <p>E., 1.2</p> <p>E., 1.3</p>								
Output Voltage	24Vdc nominal at full load.	Output voltage is adjustable between 22 to 30Vdc.	E., 2.1.1								
Output Current	35Amps at 24Vdc.	Tested for 840W @ output voltage setting from 22 to 30Vdc.	E., 2.1.2								
Output Power	840W		E., 2.1.3								
DC Output Voltage Variation	<p>The maximum dc output voltage variation from nominal shall be $\pm 1\%$ as a result of the cumulative effects due to any and all of the following causes:</p> <ol style="list-style-type: none"> a) The effects of internal converter functions. b) Converter generated harmonics. c) Load variations from zero to full load. d) Line voltage variations per MIL-STD-704A. e) Transition from main supply to battery and vice-versa; or from auxiliary supply to battery and vice-versa. 	<table border="0"> <tr> <td>100% load change</td> <td>0.2%</td> </tr> <tr> <td>Line voltage $\pm 10\%$</td> <td>0.007%</td> </tr> <tr> <td>Temperature -10 to $+50^\circ\text{C}$</td> <td>0.007%</td> </tr> <tr> <td>Total deviation =</td> <td>0.2%</td> </tr> </table>	100% load change	0.2%	Line voltage $\pm 10\%$	0.007%	Temperature -10 to $+50^\circ\text{C}$	0.007%	Total deviation =	0.2%	E., 2.2
100% load change	0.2%										
Line voltage $\pm 10\%$	0.007%										
Temperature -10 to $+50^\circ\text{C}$	0.007%										
Total deviation =	0.2%										

TABLE 1 SUMMARY OF REQUIREMENT VS. CAPABILITY (CONT'D)

Item	Requirement	Capability	NAS3-15827 Reference
"Lock Out" Circuit	The converter shall be stopped when both the main and/or auxiliary ac sources exceed the limitations imposed by MIL-STD-704A and the battery voltage is less than 74V.	No interruption of service due to transients per MIL-STD-704A. System shuts off when battery reaches depth of discharge: 74Vdc.	E., 3.4
Battery "Trickle-Charge"	Maintain the standby battery in a ready condition by continuously replenishing the "trickle-charge" lost by the battery.	Battery reconditioning provided; minimum charge rate = 2A.	E., 3.5
MTBF	Exceed 10,000 hours	15,000 hr.	B., 5
Overload	The converter shall not sustain any permanent damage when the output terminals are shorted for any length of time.	Tested for all overload conditions to short circuit.	B., 6
Current Limiting	The output current shall be limited to be not more than twice the steady-state nominal rated operating current.	Current limited @ 37.5A.	B., 7
Ohmic Isolation	Ohmic isolation shall be provided between the prime electric power sources and output.	10,000 ohms minimum.	B., 8
Operating Temperature Range	The converter shall operate without any performance degradation between the temperatures of -10°C and +50°C.	Tested in still air oven over the ambient range.	B., 9
Power Factor	The power factor measured at the ac input terminals shall be equal to or greater than 0.75 when the converter is supplying loads between 50 & 100% of rated capacity.	.7 @ 50% load. .75 @ 100% load. Measured @ nominal line voltage.	B., 10
EMI	Not specified.	Designed to MIL-STD-461A, Notice 3.	
Lightning Strike	Not specified.	Lightning arrester on input power lines mounted external to the converter.	
AC Input Power Dropout without Batteries	Not specified.	Designed for 16ms total ac power dropout without deviation of load power quality.	

4.0 ELECTRICAL DESIGN

4.1 FUNCTIONAL DESCRIPTION

A functional block diagram of the power supply is presented in Figure 4.1. The main power level functions, from input to output, are the input SCR rectification, input filter, series inverter, and output filter. Circuit breakers and EMI filters are also shown between the power sources and the SCR rectifiers.

The SCR rectifiers and input smoothing filter convert the ac inputs to 86Vdc. The battery power source is connected directly across the 86Vdc. This bus is the power source for a series inverter consisting of SCR power switches, a series tuned LC network and an output transformer, which inverts the nominal 86Vdc to high frequency ac. The output of the transformer is rectified and filtered by the output smoothing filter to obtain the desired dc output voltage.

The control circuitry associated with the 86V bus accomplishes the bus voltage regulation and current limiting by modulating the conduction angle of the input line SCR rectifiers. In addition, the control circuitry establishes (1) the selection of the power source from which the converter derives its power, and (2) the transfer between power sources when the bus voltage excursion exceeds a designated range of 74 to 86Vdc, and (3) the series inverter command off when the bus voltage is below 74V.

The control circuitry associated with the series inverter effects pulse-frequency modulation of the series inverter SCR's to achieve: (1) output voltage regulation and (2) output overload protection.

4.2 CIRCUIT DESCRIPTION

Schematic diagrams for the complete power supply are shown in Figures 4.2 and 4.3, and described in the following paragraphs. Since the series inverter is the central part of this power supply, characteristics and design equations for the series inverter power stage are also presented.

4.2.1 86V Bus Voltage and Current Control

The 86V bus is controlled only when ac power (main or auxiliary) is present. When the battery is the only power source, its terminal voltage (varies between 74 and 86V) becomes the bus voltage.

The 86V bus voltage control circuitry, shown in Figure 4.2, consists of:

- A voltage regulator common to both ac inputs.
- SCR tripping control for each of the two ac input lines.
- Voltage sensing circuitry between the two ac sources to effect ac power transfer and inhibit.

The voltage regulator employs a two-loop control in which both dc and ac control signals are utilized. The ac information is derived from the smoothing filter inductor L1, and injected in series with the dc information obtained from the 86V bus voltage divider, R35 and R36. These two signals are processed by integrator-amplifier U5. Clamping networks are provided across integrating capacitor C5 to limit the amplifier output voltage excursion in the near vicinity of the reference voltage VR2 thus improving the transient response time of the 86V bus voltage.

In conjunction with the integrator amplifier U5, information concerning the 86V bus current is also processed. The information is sensed by resistor R43, and amplified by amplifier U6. The output of U6 is "OR" gated into the input of U5 through diode CR27. When the bus current reaches a predetermined level, the current signal will override the bus voltage regulator loop, thus limiting the bus current. Since the bus feeds both the series inverter and the battery bank connected across it, the sum of the battery charging current and the current drawn by the series inverter is regulated. The predetermined regulation level for the bus current is 16A, which is approximately 2A above the maximum 14A required by the series inverter under full-load condition. Consequently, the battery recharge current varies from 2 to 16A as the series inverter operates from full load to no load.

The output signal of the integrator amplifier is summed with a cosine function generated from each of the two ac source sinewaves. The resulting signal with its dc level and ac component operates on comparators. The zero or one output of the comparator controls the output signal to the gate of its associated SCR's.

With a zero state at the output of the comparator, the gate drive amplifiers are switched in synchronism with the associated ac input sinewaves, firing alternately and in-phase with the proper SCR. With a one signal present at the output of the comparator, both U1 and U2 are in an on state shorting the gate drive transformer winding and removing all SCR firing power.

The main voltage sensing and transfer circuitry operates an SCR firing in like manner. If the main voltage drops below the lower limit of 105Vdc the inhibit signal is removed from the auxiliary and applied to the main. When the main voltage is normal, operation reverts to main and auxiliary is inhibited.

The main sensing and transfer circuitry has hysteresis built in to prevent oscillatory transfer between main and auxiliary. In addition, the voltage sensing reference is shifted when the auxiliary is not present to allow operation on the main supply below the 105Vac level.

Transformers T1 & T2 are provided to synchronize the gate firing signal and to supply control bus power during the initial starting periods. The output of these transformers is rectified, filtered, and fed through a series regulator (Q18) to a common 15V control bus.

After the initial starting period and when the 86V bus has reached 84V, a 15V control power and an isolated 20V supply for the series inverter are derived from a dc to dc converter operating from the 86V bus.

The inverter is of the "flyback" type where on-time, off-time modulation controls output voltage. The control loop is of the ASDTIC type using both ac and dc sensing. AC information is taken from a winding on the

flyback transformer T5 and integrated in capacitor C7. R39 and R39 make up a voltage divider across the 15V bus to obtain dc information. A hysteresis is provided (R40,R44) to set frequency of operation and peak to peak detector levels for comparator U12. The digital output of the comparator controls the power transistor Q6.

86V bus under voltage protection is provided by U11 and associated circuits. A hysteresis is provided and selected to sense an upper limit of 84Vdc (turn-on) and a lower limit of 74V (turn-off). The output of U11 operates on the control power converter to shut it off when the 86 dc bus reaches its lower limit of 74V and turn on at bus voltages above 84Vdc.

Application or removal of control power to the series inverter serves to turn the series inverter on or off.

4.2.2 Series Inverter

The circuit schematic for the series inverter and its control circuitry is shown in Figure 4.3.

The series inverter power stage generates bi-polar high frequency half-sinewave current pulses by alternately firing SCR's Q7 and Q8 in series with a tuned circuit made up of L2 or L3, the parallel capacitors C21 and C22, and the primary winding of output transformer T8.

The output voltage of T8 is rectified and filtered to complete the system. Voltage regulation and current limiting is accomplished by reducing the frequency of SCR firing from a predetermined design maximum. The pulse repetition frequency for this design is 10kHz maximum and diminishes with decreasing load to nearly zero frequency at no load.

The control system is based on a unijunction pulse generator, flip-flop, and the power amplifiers which pulse drive the SCR gates of Q7, Q8.

A current source made up of Q14 and its associated circuitry provides a linear voltage ramp for unijunction operation. This current source is modified by: (1) the output current as sensed by current transformer T12, and (2) the inverter output through CR67 when the voltage is below 20Vdc. Both of these control functions reduce frequency for current limiting under abnormal operating conditions such as sustained overload or filter charging during startup.

The voltage control loop operates on the unijunction frequency by shifting the stand-off ratio of the unijunction. The peak amplitude of C23 ramp voltage is clamped by resistor dividers R130 and R72, and rectifier CR38. The base-two of Q15 is shifted above or below the firing point by a zero or one state from comparator U13. The comparator is operated on by a saw tooth ramp at the output of the amplifier integrator U14. AC information for this ASDTIC control system is derived from a current transformer T9 which measures filter capacitor current. The dc information is taken from a resistor divider at the output of the unit. A potentiometer (R84) is provided for adjustment of output voltage.

Circuitry to inhibit operation of the series inverter when control power is below 18Vdc is shown in Figure 4.2. Q16 and Q17 and associated circuits make up a 20V bus voltage sensor. Q16 acts to short out the unijunction charging capacitor when the control bus is below 18V.

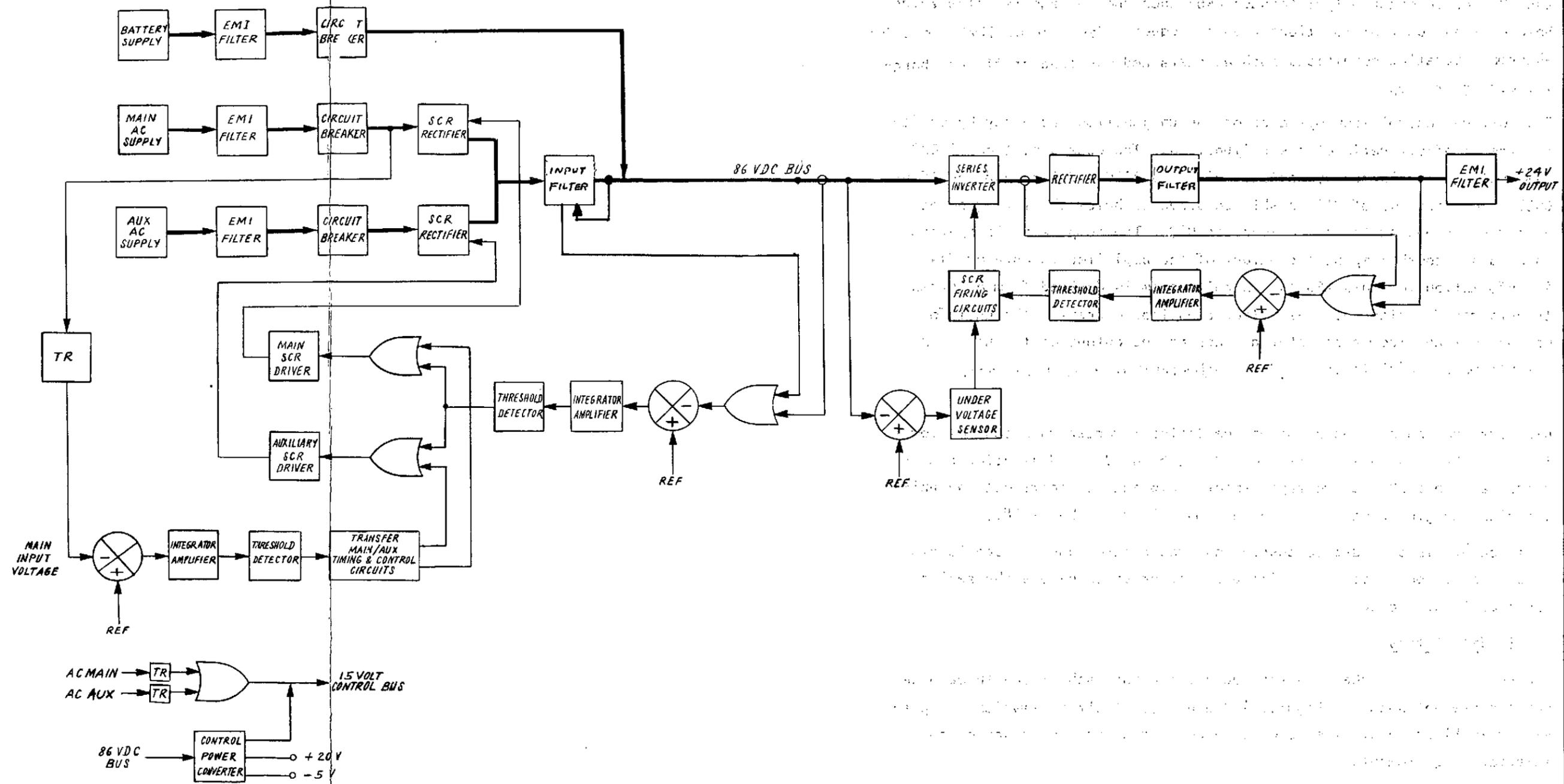
This feature is provided to ensure that the control bus voltage is high enough for proper timing and firing characteristics before the series inverter is activated.

4.2.3 EMI Filters

The EMI Filters for the converter output and for each of the three power sources are not shown in Figures 4.2 and 4.3. Their schematics are presented in Figure 4.4. They are designed to meet the input and output interface requirements.

FOLDOUT FRAME

FOLDOUT FRAME



SIZE	CODE	REV. NO.
D	11982	
SCALE	NONE	SHEET

12 Figure 4.1 Block Diagram of the Uninterrupted AC/DC to DC Power Processor

FOLDOUT FRAME

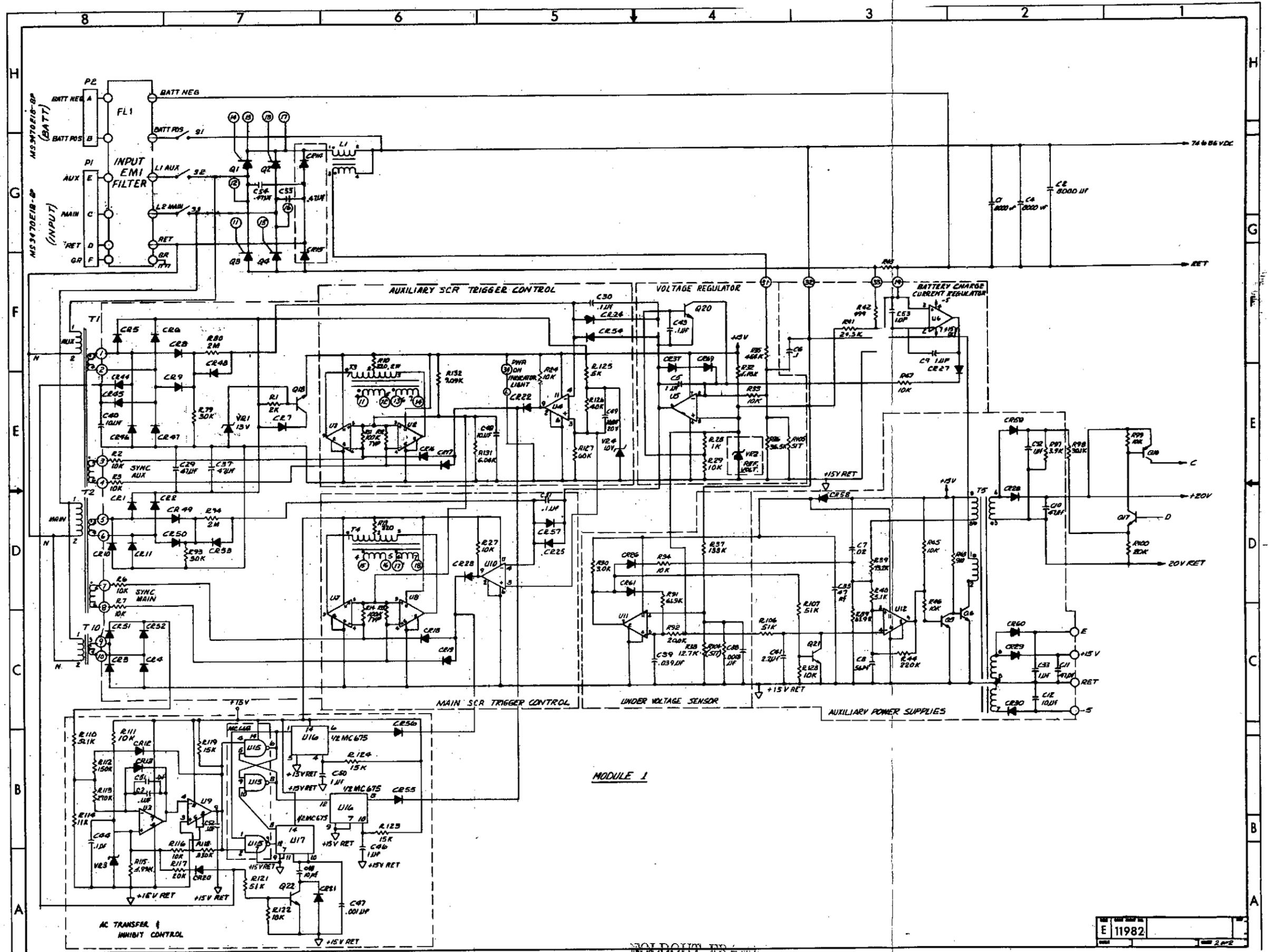


Figure 4.2 Schematic Diagram of the 86V Bus Voltage and Current Control

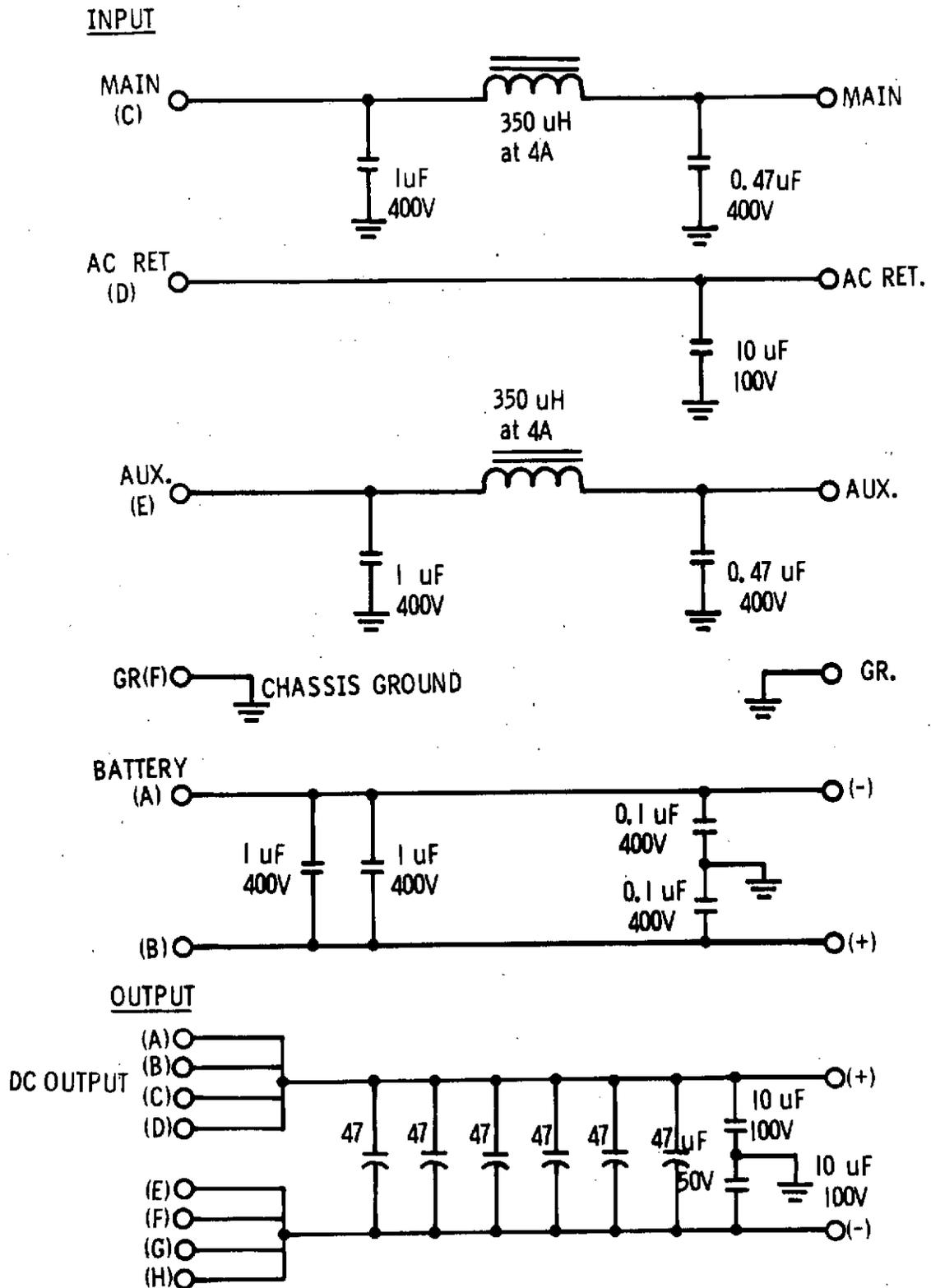


Figure 4.4 Schematics of Input and Output EMI Filters

4.3 SERIES INVERTER CHARACTERISTICS AND EQUATIONS

The series controlled rectifier inverter utilizes a series LC resonant circuit to provide the means of commutation of the inverter SCR's. Figure 4.5 illustrates, in basic form, a series inverter without a spill-over network. When one controlled rectifier is turned on, an oscillatory current flows through the series combination of the inductor L, the load transformer T, and the series capacitor C. The sinusoidal current flow, occurring at a frequency determined by the LC components, is zero when an SCR is initially turned on, builds up to a maximum determined by the circuit parameters, and then returns to zero. As the current passes through zero, the conducting SCR reverts to a non-conducting state. To illustrate certain characteristics peculiar to this type of inverter and to develop the basic equations of operation for the series inverter, the equivalent circuit of Figure 4.5 during one half cycle of operation is redrawn in Figure 4.6, from which an analysis is performed based on the following simplified assumptions:

1. The SCR's are ideal, i.e., zero forward drop, zero current when reverse-biased, and zero turn-on time as well as turn-off time.
2. The load transformer is ideal, and C_{out} is large enough to effect essentially a square-wave voltage across the primary with an amplitude V.
3. The LC components are lossless, with initial voltage across the bottom capacitor as V_0 . The two series capacitors are identical, i.e., $C_1 = C_2 = C$.
4. The source voltage is E, with zero internal impedance.

4.3.1. Steady State Operation

The two loop equations for currents i_1 and i_2 are the following:

$$E - L(d/dt) (i_1 - i_2) - V - \frac{1}{C} \int i_1 dt = 0 \quad (4.1)$$

$$L (d/dt) (i_1 - i_2) + V - \frac{1}{C} \int i_2 dt = 0 \quad (4.2)$$

By subtracting equations (4.2) from (4.1) and adding (4.2) to (4.1), and then differentiating the obtained difference and sum, one has

$$(d^2/dt^2) (i_1 - i_2) + (1/2LC) (i_1 - i_2) = 0 \quad (4.3)$$

$$(d/dt) (i_1 + i_2) = 0 \quad (4.4)$$

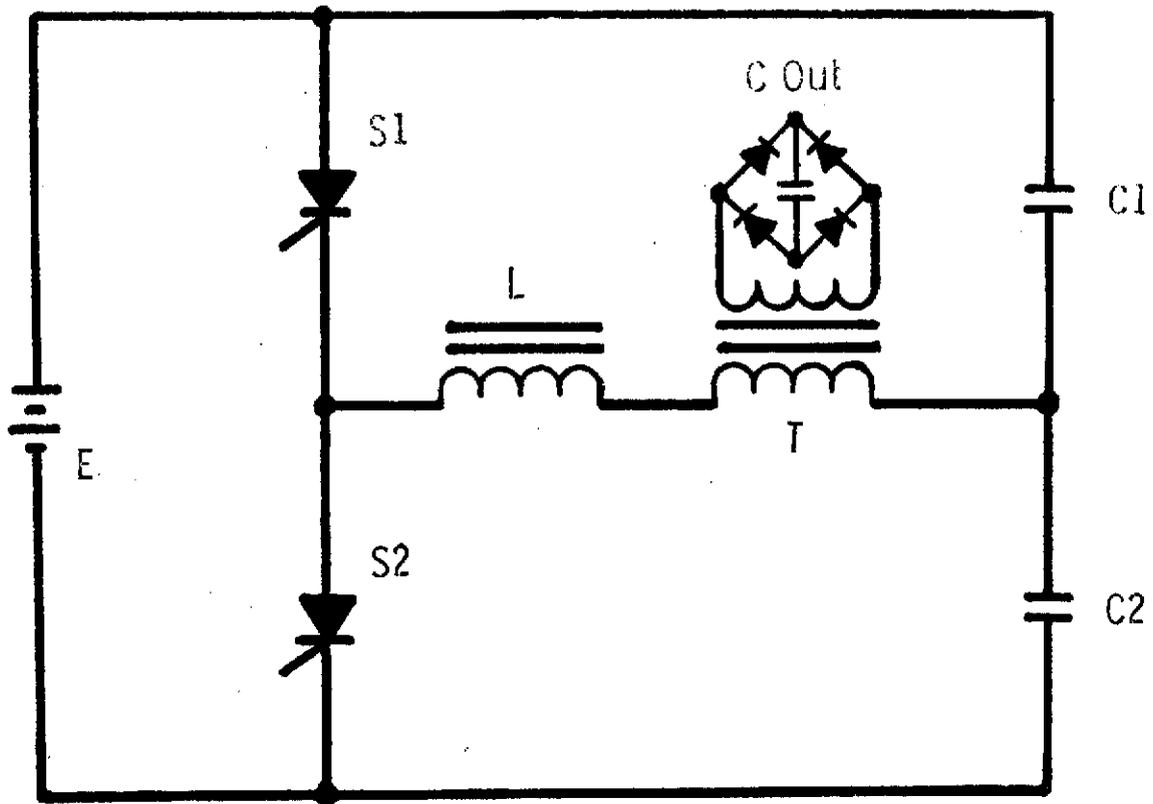


Figure 4.5 Basic Series Inverter

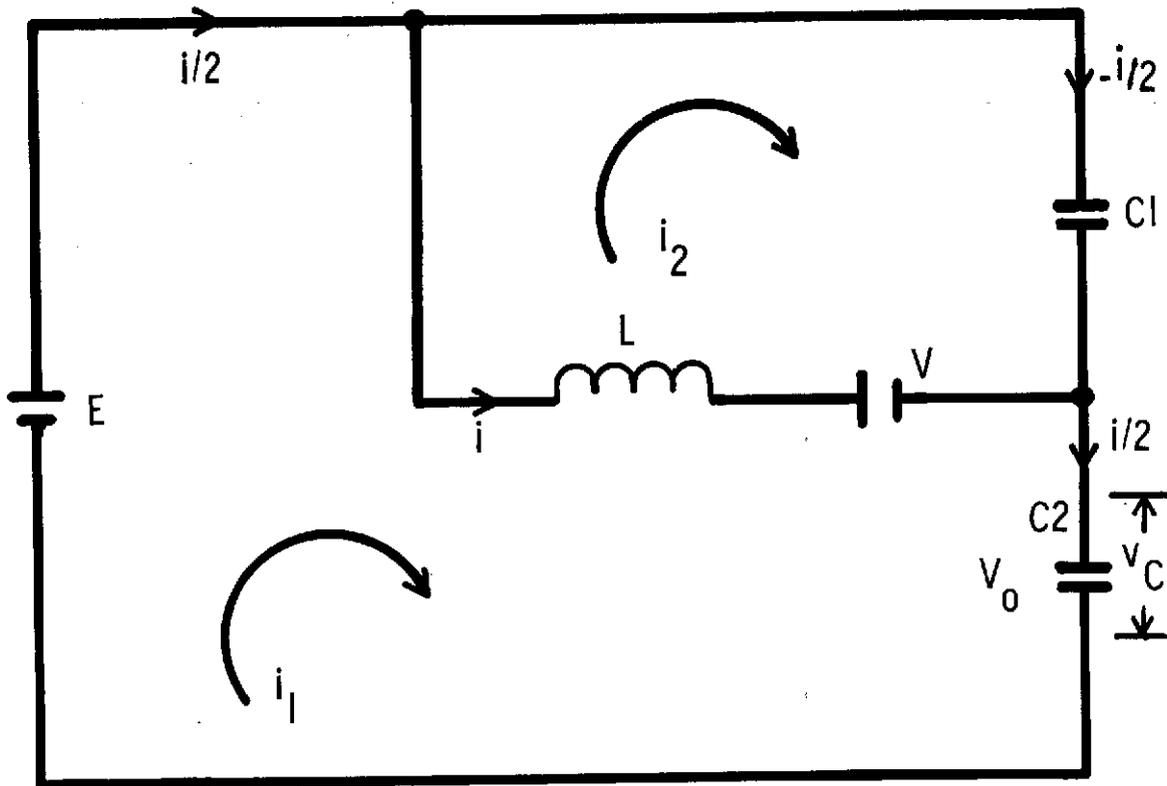


Figure 4.6. Equivalent Circuit for Series Inverter Analysis

Solving equations (4.3) and (4.4) yields

$$i_1 - i_2 = K_1 \sin(t/\sqrt{2LC}) \quad (4.5)$$

$$i_1 + i_2 = K_2 \quad (4.6)$$

Realizing that $i_1 - i_2 = i_1 + i_2 = 0$ at $t = 0$, the constant K_2 vanishes, giving

$$i_1 = -i_2 = (K_1/2) \sin(t/\sqrt{2LC}) \quad (4.7)$$

Substituting equation (4.7) into (4.1),

$$v_c = E - 2L(di_1/dt) - V = E - V - K_1\sqrt{L/2C} \cos(t/\sqrt{2LC}) \quad (4.8)$$

Since it is known at $t = 0$ that the voltage across the bottom capacitor is $v_c = V_o$,

$$K_1 = (-V - V_o + E) / \sqrt{L/2C} \quad (4.9)$$

Thus

$$i_1 = -i_2 = \frac{E - V - V_o}{\sqrt{2L/C}} \sin(t/\sqrt{2LC}) \quad (4.10)$$

When the voltage across the bottom capacitor is V_o , that across the top capacitor is V_M , where V_M is related to V_o by:

$$V_o = -V_M + E \quad (4.11)$$

Since the current through the inductor and the transformer is $i = i_1 - i_2$, from equations (4.10) and (4.11),

$$i = i_1 - i_2 = \frac{V_M - V}{\sqrt{L/2C}} \sin \frac{t}{\sqrt{2LC}} \quad (4.12)$$

The voltage ($E - v_c$) across the top capacitor, based on equations (4.8), (4.9), and (4.11), becomes

$$(V_{c \text{ top}})_1 = V + (V_M - V) \cos(t/\sqrt{2LC}) \quad (4.13)$$

Referring to Figure 4.6, the current through each series capacitor is $i/2$. The current through the inductor and the transformer, $i_1 - i_2$, is i . As a consequence, the current through the power source, E , is also $i/2$.

4.3.2 Transient Operation

In Figure 4.5, with V being the amplitude of the square-wave voltage across the transformer primary, and with V_{Mt1} being the initial voltage across the top capacitor at the beginning of the first half cycle of conduction through $S1$, the voltage across the top capacitor during this first half cycle can be expressed in equation (4.13), with V_M being replaced by V_{Mt1} .

After the half cycle of conduction by $S1$, $S1$ is turned off, and $S2$ is turned on. During this second half cycle, voltage across the top capacitor $C1$ can be shown to be:

$$(V_{ctop})_2 = E - V - (E - V - V_{Mt2}) \cos \frac{t}{\sqrt{2LC}} \quad (4.14)$$

Here, V_{Mt2} is the initial voltage across the top capacitor at the beginning of the second half cycle (or, the end of the first half cycle).

Starting with V_{Mt1} and employing equations (4.13) and (4.14) alternately, each time using the respective proper initial voltage, the voltage V_{Mtn} at the end of n th cycle can be shown to be

$$V_{Mtn} = 2nE - 4nV + V_{Mt1} \quad (4.15)$$

or,

$$dV_{Mtn}/dn = 2(E - 2V) \quad (4.16)$$

Equation (4.16) indicates that:

- (1) For $E < 2V$, V_{Mtn} shall decrease with n , i.e., voltage across the top capacitor $C1$ cannot build up. In steady state inverter operation, $E < 2V$ is thus impossible.
- (2) For $E = 2V$, V_{Mtn} would be identical for each n , i.e., steady-state operation can result if the inverter is indeed lossless as assumed. However, the source energy over a single switching event consists of energy delivered to the load, to the circuit loss elements, plus a surplus amount which is stored in the series capacitors. Consequently, $E = 2V$ is practically unfeasible for sustained oscillation.

(3) For the condition of $E > 2V$ during which the energy from the source is more than that demanded by the load and the loss, V_{Mtn} would increase with n , i.e., voltage across the capacitors would build up indefinitely. The rate of increase is maximum at $V = 0$, as is evident from equation (4.16). This is entirely reasonable, for there can be no output power from equation (4.16). Since the energy not consumed by the load must be stored in the capacitor, the rate of storage is highest at $V = 0$, and decreases during normal steady state operation. Assuming (1) $V=0$ and (2) voltage $V_{Mt1} = E/2$ is charged to each capacitor initially prior to closure of the SCR switch, then, at the end of the first cycle of switching, i.e., for $n = 1$ in equation (4.15), V_{Mt1} would become $5E/2$. Thus the capacitor voltage on C1, which initially was $E/2$ only, has, in the course of two power pulses (one in each half cycle), changed to $5E/2$. Thus it is seen how quickly an intolerable buildup can occur.

From the foregoing discussion, it becomes apparent that: (1) $E > 2V$ is a necessary condition for the inverter to overcome circuit and loss dissipation to sustain oscillation, and (2) the condition $E > 2V$ tends to lead to a runaway capacitor voltage. It is for the protection against this voltage buildup that the spillover network, to be discussed subsequently, is needed.

4.3.3 The Spillover Network

The technique for protecting against voltage buildup can be described using the schematic diagram of Figure 4.3. The components CR42, CR43, T3, and the secondary windings of L2 and L3, provide this capability. Excess energy, manifested as an induced voltage on the secondary winding of L2 and L3 during their respective discharge cycles, is fed through a saturable reactor into the output filter capacitors and the load. The reactor T13 supports an increment of voltage on each half cycle to ensure the resonant capacitors C21 or C22 have a peak voltage greater than the dc bus voltage, which guarantees a reverse voltage bias on the conduction SCR (Q7 or Q8) during its recovery period. After magnetic saturation of T13 the inductor L2 or L3 voltage is clamped to the output dc level. The ex-

cess energy is thus delivered to the output filter and output load at a constant di/dt rate depending on the dc output voltage and inductance $L2$ or $L3$. At the end of the so-called "spill-over" cycle, capacitors $C21$ and $C22$ are charged in such polarity as to yield a constant series inverter output current, cycle to cycle.

Voltage and current relationships during series inverter SCR switching is shown in Figure 4.7.

Instantaneous SCR and spill-over currents are shown in Figure 4.8.

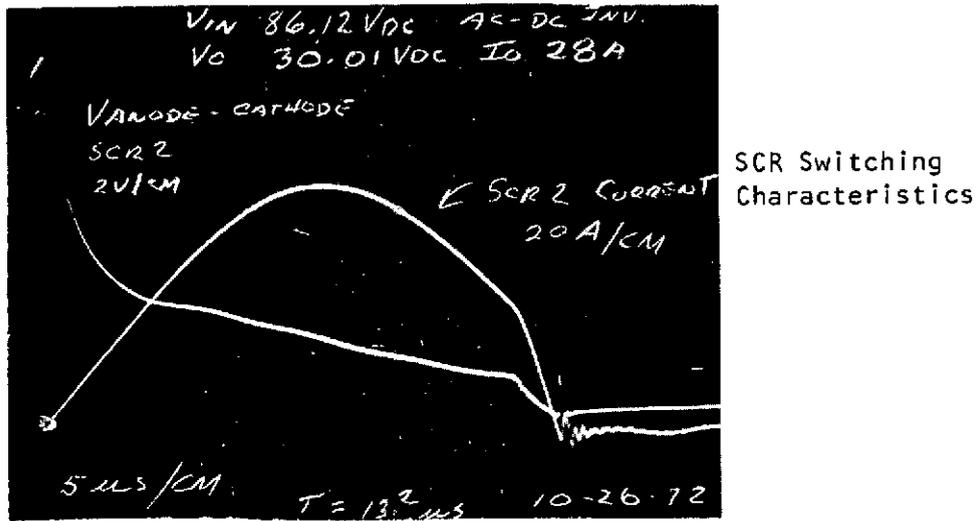


Figure 4.7. Series Inverter SCR Switching Waveform

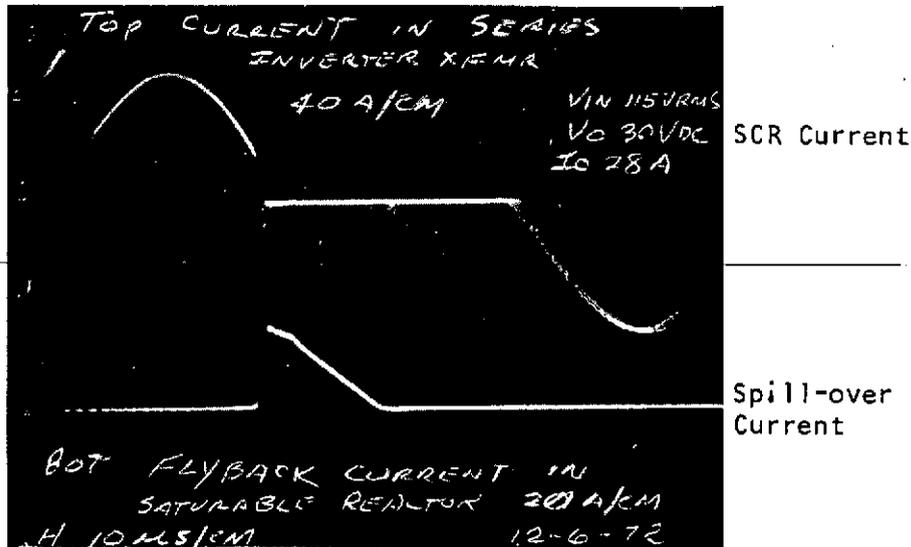


Figure 4.8. Instantaneous SCR and Spill-over Currents

5.0 UNIT DESCRIPTION

5.1 MECHANICAL CHARACTERISTICS

A photograph of the uninterruptible power supply (UPS) NAS3-15827 is shown in Figure 5.1.

The power supply is designed for shelter or van use. It is of unitized construction for individual drawer-type mounting.

The top and bottom covers are removable to obtain access to the internal components. These covers are each held with 10 self locking screws.

The front panel contains all controls that include the following:

1. AC main power breaker and on-off switch.
2. AC auxiliary power breaker and on-off switch.
3. Battery power breaker on-off switch.
4. Power on indicating light.

An output voltage adjustment potentiometer is located on the control card, which is accessible by removing the bottom cover. Three quick-connect connectors protrude from the rear of the unit for making the following electrical connection to the UPS:

1. AC input
2. DC output
3. Battery input

Handles and mounting holes are provided on the front panel for mounting in standard relay rack enclosures.

5.2 MECHANICAL DESIGN

The mechanical design of the ac & dc to dc converter (NAS3-15827) is such as to divide the unit into five modules: the control card plug-in, the rear panel, the left side panel, the right side panel, and the front panel chassis assembly.

Heat generating components are mounted thermally to three finned surfaces which make up the rear, left and right side panels. These finned

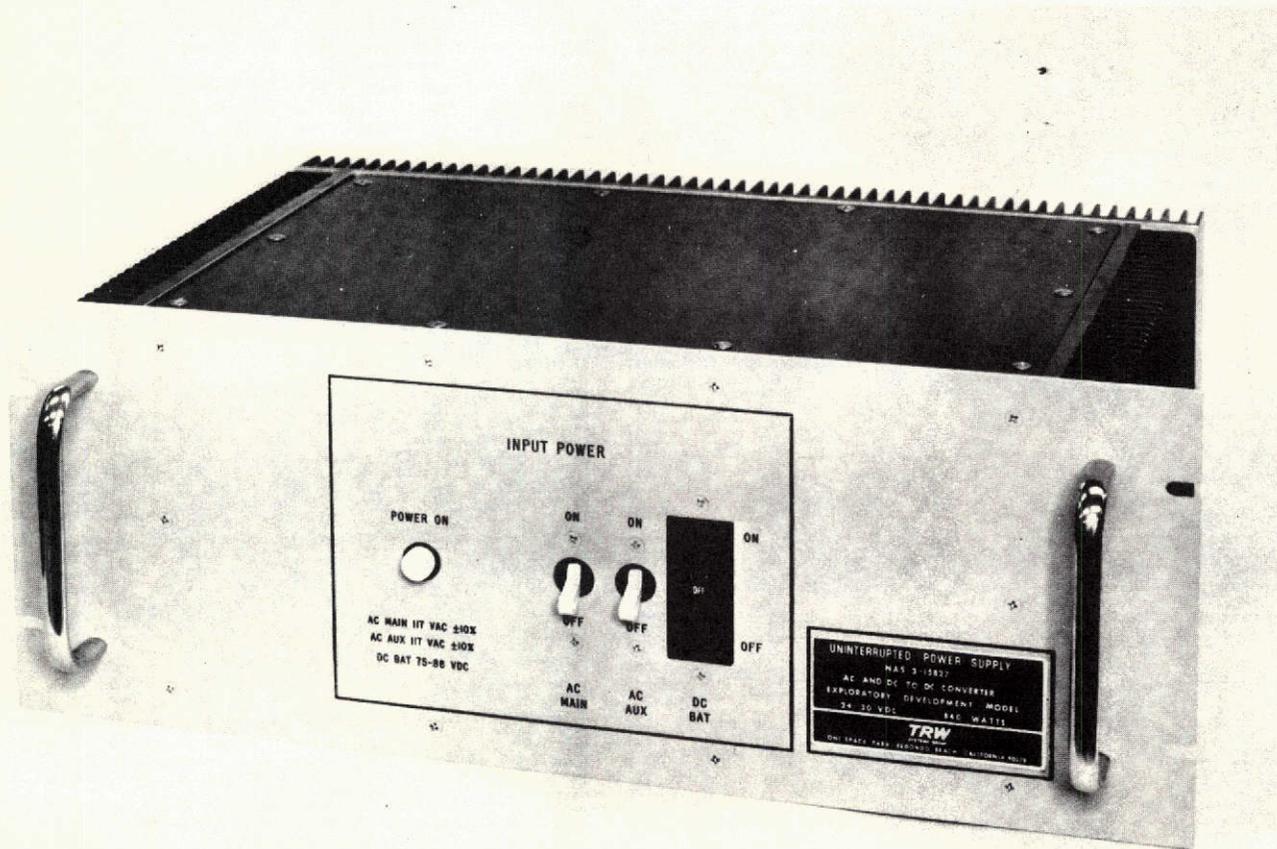


Figure 5.1 The Packaged Uninterrupted AC/DC to DC Power Supply

surfaces provide the major means of heat removal for the power supply. Installation should be such that free air flow is available for three surfaces.

All wiring connections between modules are made with removable lugs on terminal blocks or terminal posts.

Mechanical Characteristics

Construction	Unitized Construction for Drawer Type Mounting
Dimensions	7 inch Front Panel by 11.2 inches Deep-Standard 19 inch Rack
Weight	52.8 lbs
Cooling	Natural Convection

5.3 ELECTRICAL CHARACTERISTICS

5.3.1 The Salient Electrical Characteristics are Listed Below:

Input Power (Any single source, combination of any two sources, or all three sources.)

Main	117 ± 10% - 50 to 400Hz
Auxiliary	117 ± 10% - 50 to 400Hz
Battery	74 to 86Vdc, 13 type (3DCU-3) batteries C&D or equivalent

Output Power

Voltage	22 to 30Vdc adjustable
Current	35A @ 24Vdc
Power	840W maximum
Ripple Voltage	1% p-p

Voltage Regulation	$\frac{\Delta V}{V}$	$\frac{+}{-}\%$
Load	96mV	0.2%
Line ± 10%	3.4mV	0.007%
Temperature	3.4mV	0.007%
Overload Protection	37.5A maximum	

Battery Reconditioning	2A min. rate
Ambient Temperature	-10 to 50°C
Reliability	>15000 hrs. MTBF

6.0 RELIABILITY PREDICTION

A reliability assessment in terms of mean time between failures (MTBF) was performed for the power supply in accordance with MIL-STD-756A procedures, and utilizing MIL-HDBK-217A component failure rate. The prediction assumed a series system. Component failure rates were established using individual part stress ratios and actual component ambient temperature obtained in an overall operational environment of 120°F. Failure rates for part classes and the total for the power supply are listed in Table 6-1. The calculated value for MTBF was in excess of 15000 hrs.

TABLE 6-1
Component Failure Rate Tabulation

<u>Component</u>	<u>Bits (1 per 10⁹ hrs)</u>
Resistors	
Composition	1600
Film	420
Variable, wire wound	10024
Capacitors	
Electrolytic	750
Ceramic	242
Mica	1
Solid tantalum	270
Polypropolyene	315
Magnetics	3000
Semiconductors	
Silicon diodes (<1 watt)	9680
Zener diodes	1950
Silicon rectifiers (<1 watt)	1400
Silicon controlled rectifiers	10500
Silicon transistors NPM	5240
Silicon transistors PNP	17000
Integrated circuits	3000
Circuit Breakers	1000
Lamp	200

$$\lambda_T = 66592$$

$$MTBF = \frac{1}{\lambda_T}$$

15,016 hours

7.0 DISCUSSION OF TEST RESULTS AND RECOMMENDATIONS

Results obtained from testing the uninterrupted power supply can be discussed in terms of the following performance aspects:

(1) Steady-State Performance

The test results demonstrate excellent performance in areas of current limiting, output ripple, voltage regulation and audio susceptibility. The high performance is primarily due to the implementation of the two-loop ASDTIC control concept described in Section 4.

(2) Transient Performance

Good transient response and effective inrush-current limiting during converter starting and sudden output short circuit were obtained. The transient capability was demonstrated with any and all combinations of the three input power sources.

(3) Thermal Control

The test results show that component thermal stress is well controlled below component ratings to enhance reliability predictions. In addition, fin utilization is optimized to accommodate components with widely different temperature capabilities.

(4) Versatile Field Application

A meeting with FAA application engineers was held in the early program stage. As a result of the meeting, the original design goals concerning size, weight, efficiency, and power factor were compromised slightly in favor of a more versatile power-processor field application that includes the following additional capabilities:

- Automatic and unattended battery charging built into the power supply.
- Complete and automatic transfer between two ac power sources, without the battery.
- Adjustable output voltage between 22 to 30Vdc.
- The ability to withstand lightning strike when installed with the specified lightning arrestor.
- Full power processor performance with one cycle drop out of the ac source.

The first four capabilities were verified through extensive power processor testing. Although not tested for a cycle "dropout" of a single ac source (with no batteries), the unit was designed to accommodate this condition without deviation from the output power specification.

(5) Recommendation of Performance Improvements

Although within specifications, the output ripple was significantly higher in the packaged unit when compared with that of the breadboard. The difference was attributed to inductive coupling associated with the output lines connecting the power smoothing filter output to the EMI filter. This problem could be corrected by mechanical design changes, which would relocate magnetic component or reroute the cables feeding the output EMI filter.

For the packaged power processor, approximately 90mV of output-voltage change occurred during no load/full load tests. The difference was due to ohmic voltage drop in three feet of wire between the voltage sensing point and the EMI filter box, the connector pins, and the EMI filter. This output voltage variation could be reduced drastically by mechanizing the system with remote sensing, in which case this voltage drop would be within the ASDTIC control loop.

8.0 UNIQUE FEATURES

Unique features were developed in the following areas:

- o SCR Inverter Power Stage
- o Input AC Line Regulators

8.1 SCR Inverter Power Stage

The technique of discharging series inverter inductor energy with secondary winding directly to the output provides the following advantages:

- o Improved efficiency due to the low forward drop, fast recovery rectifiers instead of SCR for this function.
- o Lower volt-sec requirements on the power transformer because "spill-over" energy does not flow through the transformer.
- o Control of main SCR reverse bias conditions under all operating conditions without use of auxiliary SCR's and their associated sensing and control circuitry.

8.2 Input AC Line Regulators

The power stage gain of the ac line modulators varies radically with conduction angle. To stabilize the control loop, especially at light load, where current is not continuous in the smoothing filter inductor, a cosine function was summed with the ASDTIC integrator output signal to normalize power stage gain.

9.0 CONCLUSIONS

The successful completion of the power-processor development has demonstrated the feasibility of lightweight, uninterrupted power systems capable of isolating electrical disturbances on the input power lines from the load. These source disturbances include lightning, variable frequency input, slowly rising and falling input voltage, battery voltage variations during charging and discharging, and automatic transfer of power sources.

Reduced power processor weight and higher efficiency were achieved, primarily due to the series-resonant inverter characteristics. The inverter allows higher-frequency operation of the power SCR's as a result of self commutation and the sinewave current developed. The SCR switching conditions are ideal; the SCR current is essentially zero during the turn-on and turn-off periods.

High reliability, the most important aspect required of an uninterrupted power supply, is enhanced greatly by the series inverter configuration where component electrical stresses are inherently controlled during transient and overload operations.

The power processor was developed with the objective of being interchangeable with several existing power systems used by the FAA in installations which have had a history of failure due to electrical transients. In addition, a second objective of this program was to transfer power processing technology advanced by NASA Lewis Research Center to satisfy the FAA hardware requirements. To this end the power processor is designed with such versatility that in many aspects it exceeds what was actually required in meeting the first objective. As a consequence, the power processor is capable of performing in many other field applications. Needless to say, the circuit complexity and the weight of such a multiple-purpose power processor can be significantly reduced when the power processor design is only required to satisfy a specific field application. In this regard, the superior reliability, the light weight, and the high efficiency characteristics of the power processor, made possible primarily by the utilization of the series inverter, are readily adaptable to other critical high power applications.

10.0 REFERENCES

1. Schwarz, F. C., "Power Processing," Proceedings of the 8th International IEEE Symposium on Electronic Devices, Washington, D. C., 1968.
2. Schwarz, F. C., "A Method of Resonant Current Pulse Modulation for Power Converters," IEEE Transactions on Industrial Electronics & Control Instrumentation, Vol. IECI-17#3, May 1970, pp. 209-220.
3. Cronin, D. L., "2800 Watt Series Inverter DC Power Supply," Power Conditioning Specialists Conference, Pasadena, California, 1971, pp. 117 through 123.
4. Lalli, V. R., and Schoenfeld, A. D., "ASDTIC Duty-Cycle Control for Power Switches," NASA Technical Memorandum, NASA TMX-68066.
5. Yu, Y., Biess, J. J., Schoenfeld, A. D., and Lalli, V. R., "The Application of Standardized Control and Interface Circuits to Three DC to DC Power Converters," IEEE Power Electronics Specialists Conference Record, 1973, pp. 237-248.