MIDAS, PROTOTYPE MULTIVARIATE INTERACTIVE DIGITAL ANALYSIS SYSTEM — PHASE I

Volume III: Wiring Diagrams

by

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The MIDAS System is a third-generation, fast, multispectral recognition system able to keep pace with the large quantity and high rates of data acquisition from present and projected sensors. MIDAS, for example, can process a complete ERTS frame in forty seconds and provide a color map of sixteen constituent categories in a few minutes. A principal objective of the MIDAS Program is to provide a system well interfaced with the human operator and thus to obtain large overall reductions in turnaround time and significant gains in throughput. This goal is elaborated in this report as an objective of the Phase II program.

This report describes the hardware and software generated in Phase I of the overall program. The system contains a mini-computer to control the various high-speed processing elements in the data path and a classifier which implements an all-digital prototype multivariate-Gaussian maximum likelihood decision algorithm operating at $2 \times 10^5$ pixels/sec. Sufficient hardware has been developed to perform signature extraction from computer-compatible tapes, compute classifier coefficients, control the classifier operation, and diagnose operation.

Volume I describes the MIDAS System in detail; Volume II contains the diagnostic programs used to test MIDAS' operation; Volume III displays the MIDAS construction and wiring diagrams.

### Key Words
- Real-time processing
- Wirewrap
- A/D-D/A conversion
- Multispectral recognition system
- Multivariate-Gaussian maximum likelihood decision algorithm

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PREFACE

A comprehensive multispectral program devoted to the advancement of state-of-the-art techniques for remote sensing of the environment has been a continuing program at the Environmental Research Institute of Michigan (ERIM), formerly the Willow Run Laboratories of The University of Michigan. The basic objective of this multidisciplinary program is to develop remote sensing as a practical tool to provide the user with processed information quickly and economically.

The importance of providing timely information obtained by remote sensing to such people as the farmer, the city planner, the conservationist, and others concerned with problems such as crop yield and disease, urban land studies and development, water pollution, and forest management must be carefully considered in the overall program. The scope of our program includes: (1) extending the understanding of basic processes; (2) discovering new applications; (3) developing advanced remote-sensing systems; (4) improving fast automatic data processing systems to extract information in a useful form; and also (5) assisting in data collection, processing, analysis and ground truth verification. The MIDAS program applies directly to No. (4) with its improved data processing capability.

This document is the final report for Phase I of the MIDAS program under NASA Contract NAS1-11979 and covers the period from October 1972 through February 1974. The contract effort was monitored by Mr. William Howie of NASA-Langley. The overall program is guided by Mr. R. R. Legault, Vice President of ERIM, and Director of the Infrared and Optics Division. Work on this contract was directed by J. D. Erickson, Head of the Multispectral Analysis Section, and by F. J. Kriegler, Principal Investigator. The ERIM number for this report is 195800-25-F.

ERIM personnel who contributed to this project and who co-authored this report are Dempster Christenson, Michael Gordon, Roland Kistler, Seymour Lampert, Robert Marshall, and Rowland McLaughlin. In addition to providing the text, their individual contributions were as follows: Dempster Christenson and Michael Gordon provided system programming and diagnostic software; Roland Kistler and Seymour Lampert provided the detailed design and performed system checkout; Robert Marshall aided in overall system configuration; Rowland McLaughlin organized this report. The authors wish to acknowledge the direction provided by Mr. R. R. Legault and Dr. J. D. Erickson. Outstanding contributions were made by the following persons: John Baumler, Clyde Connell, William Juodawlkis, Robert Pierson, Cary Wilson, and Nancy Wilson for their efforts in system construction.
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<th>Description</th>
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<tr>
<td>35</td>
<td>Video and Calibration Generator (C 6,7 )</td>
</tr>
<tr>
<td>36</td>
<td>A/D-D/A Clock Generator (C 8 )</td>
</tr>
<tr>
<td>37</td>
<td>D/A Line-Count Clock (C 9 )</td>
</tr>
<tr>
<td>38</td>
<td>D/A Duty Cycle Generator (C 10 )</td>
</tr>
<tr>
<td>39</td>
<td>Digital Input Programmer I (C 11 )</td>
</tr>
<tr>
<td>40</td>
<td>Digital Input Programmer II (C 12 )</td>
</tr>
<tr>
<td>41</td>
<td>Digital Output Programmer I (C 13 )</td>
</tr>
<tr>
<td>42</td>
<td>Digital Output Programmer II (C 14 )</td>
</tr>
<tr>
<td>43</td>
<td>System Conditioner I (C 15 )</td>
</tr>
<tr>
<td>44</td>
<td>System Conditioner II (C 16 )</td>
</tr>
<tr>
<td>45</td>
<td>A/D Line-Control, Digital Transfer Control, and DR-11C Transfer Logic (C 17 )</td>
</tr>
<tr>
<td>46</td>
<td>A/D Word Transfer (C 18 )</td>
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<td>47</td>
<td>Delay-Gate Generator (C 19 )</td>
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<td>Wiring of Card (2-C)</td>
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<td>Physical Layout of Plug Card (4-C)</td>
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<td>60</td>
<td>Wiring of Card (4-C)</td>
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<td>Cable Terminations for Data Transfer to Computer from Classifier</td>
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INTRODUCTION

This volume contains block diagrams and schematics detailing the construction of the MIDAS Classifier. Their organization forms a tree structure in which the more general block diagrams reference the more detailed block diagrams which lead to the schematics. This provides a self-explanatory set of diagrams enabling the reader to acquaint himself with system design and circuitry to any desired level of detail.
2 GENERAL SYSTEM CONFIGURATION

The Phase-I MIDAS System is most easily visualized if organized into subsystems as shown in the block diagram of Fig. 1. The system is under complete control of the Digital Equipment Corporation (DEC) PDP-11/45 computer system. All control inputs by an operator are made by way of the computer keyboard. All commands are translated by computer software into code words and sent out over interface devices to set up the hardware registers in the special-purpose processor. These codes are decoded in three of the blocks shown in Fig. 1. These three places are: (1) in the control section, (2) in the clock section, and (3) in the Diagnostic/Output section. These codes will be described in detail in subsequent sections.

The MIDAS System is housed in one 6-foot rack. The physical location of the major components is shown in Fig. 2. Each of the 4 quadratic pipes is housing in a wire-wrap card file containing 13 wire-wrap circuit boards. The quadratic calculation is accomplished by a set of 12 boards in each bay while the other board in each bay is different as shown in Fig. 2.

High-speed mass data is transferred to and from the computer by means of (1) the A/D-D/A (hybrid) section, (2) the clock section, and (3) Diagnostic/Output section. High-speed multichannel data is transferred through the hybrid section and the quadratic computation pipes. The figure numbers shown in each of the blocks of Fig. 3 refer to more detailed figures describing that block.

The control bay and the hybrid bay have room for 22 circuit boards. There are 20 boards in the control bay numbered C-1 through C-20. There are 19 boards in the hybrid file numbered H-1 through H-19.
FIGURE 1. BLOCK DIAGRAM OF THE MIDAS SYSTEM
FIGURE 2. LOCATION OF MAJOR MIDAS COMPONENTS
FIGURE 3. BLOCK DIAGRAM OF THE QUADRATIC PIPE
CLASSIFIER SECTION

A detailed description of the Classifier is given in Sections 4 and 6 of Volume I.

A block diagram of the quadratic pipe computation is shown in Fig. 3.
FIGURE 4. BLOCK DIAGRAM OF THE MEAN CARD

- 16-Word x 8-Bit RAM
- 8-Bit Adder
- Output Latch
- Clock
- to Variance Card
- Clock
- to Diagnostic Latch
- Clock
- to RAM Selects
- Clock
- to Diagnostic Selects
- Strobe from PDP-11/45
- 4-line to 16-line Decoder
- RAM Location
- Data Bus
- Clock
- Strobe from PDP-11/45
- Diagnostic Location

NOTE: For schematic, see Fig. 13.
FIGURE 5. BLOCK DIAGRAM OF THE VARIANCE CARD

NOTE: For Schematic, see Fig. 14.
FIGURE 6. BLOCK DIAGRAM OF THE MATRIX MULTIPLIER CARD
NOTE: For Schematic, see Fig. 16.

FIGURE 7. BLOCK DIAGRAM OF THE SQUARE CARD
FIGURE 8. BLOCK DIAGRAM OF THE SQUARE-ACCUMULATOR CARD

NOTE: For Schematic, see Figure 17.
FIGURE 9. BLOCK DIAGRAM OF THE DIAGNOSTIC/OUTPUT CARD.
FIGURE 10. BLOCK DIAGRAM OF THE CLOCK CARD

NOTE: For Schematic, see Fig. 19.
NOTE: For Schematic, see Fig. 20.

FIGURE 11. BLOCK DIAGRAM OF THE k^2 CARD
NOTES: Strobe occurs at Time 8 or 14. For schematic, see Fig. 21.
FIGURE 13. MEAN (MN) (Concluded)
FIGURE 15. 8 × 8 MATRIX MULTIPLIER (MTX) (Continued)
(c) Switching Diagram and Controls

FIGURE 18. DIAGNOSTIC/OUTPUT (Concluded)
CONTROL AND HYBRID SECTION

The hybrid section of the classifier contains nineteen cards, of which sixteen are identical printed circuit cards. These cards, located in slots H-1 through H-16, perform the transfer of data to the classifier. A block diagram of the control and hybrid section is shown in Fig. 22 and a detailed block diagram of the hybrid cards is shown in Fig. 23. For a description of this classifier section, see Section 6 of Vol. I.

The transfer of data from the PDP-11/45 computer is accomplished by the circuitry shown in the block diagram of Fig. 24. The transfer of digitized data to the computer is controlled by the digital output synchronizer shown in the block diagram of Fig. 25.
FIGURE 22. CONTROL SECTION
FIGURE 25. DIGITAL OUTPUT SYNCHRONIZER (C) [13, 14]
FIGURE 28. INPUT BUS AND PORT DECODER (H 17)
FIGURE 32. ANALOG LINE-COUNT DECODER (C2)
FIGURE 45. A/D LINE-COUNT CONTROL, DIGITAL TRANSFER CONTROL, AND DR-11C TRANSFER LOGIC (C 17)
FIGURE 48. PLAYBACK SYNC AND LINE-COUNT CLOCK GENERATOR (C 20)
BACKPLANE INTRA-BAY WIRING

The wirewrap card files have backplanes with wirewrap connectors. These back-bay connectors have 122 pins, of which 10 are used for power and 10 for ground. Connections are shown in Fig. 49. Signal origins are shown by arrows. The various card locations are designated by odd numbers 1, 3, …, 25.
FIGURE 49. BACKPLANE INTRA-BAY WIRING (Continued)
(b) Sheet 2

FIGURE 49. BACKPLANE INTRA-BAY WIRING (Concluded)
6 SYSTEM CABLEING

6.1 CABLING BETWEEN HYBRID AND CONTROL BAYS

The wiring for data and control signals flows between the hybrid and control bays including PC-board card plugs that terminate the cables interconnecting the bays. One end of each printed circuit board accommodates cable wires at tie points (T.P.) on the card; the other end of the PC board has a printed circuit connector that mates with a card slot in the connector housing associated with a particular bay.

The connector housings comprise two auxiliary files located at the rear of the control and hybrid bays, respectively. In each of these files are four card slots for the card plugs of the cables. Each slot is assigned a number (1 through 4) and a code letter (C or H) to give its position in the file and identify that file with one of the two bays (control or hybrid). Figure 50 shows overall system cabling; the table below lists the terminations of the cables that originate in the two auxiliary files.

<table>
<thead>
<tr>
<th>SLOT in Aux. File</th>
<th>TERMINATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control Bay</td>
<td></td>
</tr>
<tr>
<td>1-C</td>
<td>MIDAS CLASSIFIER</td>
</tr>
<tr>
<td>2-C</td>
<td>2-H</td>
</tr>
<tr>
<td>3-C</td>
<td>CONTROL PANEL</td>
</tr>
<tr>
<td>4-C</td>
<td>DR-11C INTERFACE</td>
</tr>
<tr>
<td>Hybrid Bay</td>
<td></td>
</tr>
<tr>
<td>1-H</td>
<td>DR-11B INTERFACE</td>
</tr>
<tr>
<td>2-H</td>
<td>2-C</td>
</tr>
<tr>
<td>3-H</td>
<td>BNC CONNECTOR PANEL</td>
</tr>
<tr>
<td>4-H</td>
<td>BNC CONNECTOR PANEL</td>
</tr>
</tbody>
</table>

The description of the interconnecting cables to and from the bays is given in Figs. 51 to 60; these figures detail the card plugs and also further describe the termination of the cables that tie into the auxiliary card files. As indicated in these diagrams, certain of the signals are buffered on the card plugs by line drivers (8T13) and line receivers (8T14). From Fig. 50 we see that cable 1C terminates eventually at the classifier. This is via a card plug that mates with a standard DEC block; then from the DEC block the signals are brought to the classifier using point-to-point wirewrap. Figure 55 shows the layout of the card plugs associated with the DEC block while Fig. 56 gives the block configuration. It may be noted that the cables originating from slots 3-H and 4-H are not detailed in this section.

6.2 CABLING BETWEEN CLASSIFIER AND COMPUTER

As indicated in the system cabling diagram (Fig. 50), a cable runs from the classifier to a DR-11B interface; it is used to carry information (e.g., RAM load, classifier output, diagnostic info) to and from the classifier through the DEC block. At the classifier end, this cable terminates in a card plug which connects to a DEC block (for block layout, see Fig. 56). The classifier
FIGURE 50. SYSTEM-CABLING DIAGRAM
FIGURE 51. PHYSICAL LAYOUT OF PLUG CARD 1-H
<table>
<thead>
<tr>
<th>No.</th>
<th>DR-11B Pin</th>
<th>Input Cable Connector</th>
<th>Function</th>
<th>No.</th>
<th>DR-11B Pin</th>
<th>Output Cable Connection</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>A1</td>
<td>A</td>
<td>Cycle Request A</td>
<td>1.</td>
<td>V1</td>
<td>N</td>
<td>(GO)</td>
</tr>
<tr>
<td>2.</td>
<td>B1</td>
<td>1</td>
<td>End Cycle Out</td>
<td>2.</td>
<td>F2</td>
<td>12</td>
<td>C1 Control</td>
</tr>
<tr>
<td>3.</td>
<td>C1</td>
<td>B</td>
<td>Data 00</td>
<td>3.</td>
<td>H1</td>
<td>P</td>
<td>Function 2</td>
</tr>
<tr>
<td>4.</td>
<td>D1</td>
<td>2</td>
<td>Data 01</td>
<td>4.</td>
<td>H2</td>
<td>13</td>
<td>Single Cycle</td>
</tr>
<tr>
<td>5.</td>
<td>D2</td>
<td>C</td>
<td>Data 02</td>
<td>5.</td>
<td>J2</td>
<td>R</td>
<td>Function 3</td>
</tr>
<tr>
<td>6.</td>
<td>E1</td>
<td>3</td>
<td>Data 03</td>
<td>6.</td>
<td>K1</td>
<td>14</td>
<td>Data 11</td>
</tr>
<tr>
<td>7.</td>
<td>E2</td>
<td>D</td>
<td>Data 04</td>
<td>7.</td>
<td>K2</td>
<td>S</td>
<td>Data 15</td>
</tr>
<tr>
<td>8.</td>
<td>F1</td>
<td>4</td>
<td>Data 05</td>
<td>8.</td>
<td>L1</td>
<td>15</td>
<td>Data 09</td>
</tr>
<tr>
<td>9.</td>
<td>F2</td>
<td>E</td>
<td>Data 06</td>
<td>9.</td>
<td>L2</td>
<td>T</td>
<td>Data 14</td>
</tr>
<tr>
<td>10.</td>
<td>H1</td>
<td>5</td>
<td>Data 07</td>
<td>10.</td>
<td>M1</td>
<td>16</td>
<td>Data 07</td>
</tr>
<tr>
<td>11.</td>
<td>H2</td>
<td>F</td>
<td>Data 08</td>
<td>11.</td>
<td>M2</td>
<td>U</td>
<td>Data 13</td>
</tr>
<tr>
<td>12.</td>
<td>J1</td>
<td>6</td>
<td>Data 09</td>
<td>12.</td>
<td>N1</td>
<td>17</td>
<td>Data 05</td>
</tr>
<tr>
<td>14.</td>
<td>K1</td>
<td>7</td>
<td>Data 11</td>
<td>14.</td>
<td>P1</td>
<td>18</td>
<td>Data 03</td>
</tr>
<tr>
<td>15.</td>
<td>K2</td>
<td>J</td>
<td>Data 12</td>
<td>15.</td>
<td>P2</td>
<td>W</td>
<td>Data 10</td>
</tr>
<tr>
<td>16.</td>
<td>L2</td>
<td>8</td>
<td>Data 13</td>
<td>16.</td>
<td>R1</td>
<td>19</td>
<td>Data 01</td>
</tr>
<tr>
<td>17.</td>
<td>M1</td>
<td>K</td>
<td>ATTN.</td>
<td>17.</td>
<td>R2</td>
<td>X</td>
<td>Data 08</td>
</tr>
<tr>
<td>18.</td>
<td>M2</td>
<td>9</td>
<td>Data 14</td>
<td>18.</td>
<td>S1</td>
<td>20</td>
<td>Data 00</td>
</tr>
<tr>
<td>19.</td>
<td>N2</td>
<td>L</td>
<td>Data 15</td>
<td>19.</td>
<td>S2</td>
<td>Y</td>
<td>Data 06</td>
</tr>
<tr>
<td>20.</td>
<td>S2</td>
<td>10</td>
<td>Busy</td>
<td>20.</td>
<td>T2</td>
<td>21</td>
<td>Data 04</td>
</tr>
<tr>
<td>21.</td>
<td>T1</td>
<td>M</td>
<td>GND</td>
<td>21.</td>
<td>U1</td>
<td>Z</td>
<td>Cycle Request B</td>
</tr>
<tr>
<td>22.</td>
<td>U2</td>
<td>11</td>
<td>INIT.</td>
<td>22.</td>
<td>U2</td>
<td>22</td>
<td>Data 02</td>
</tr>
</tbody>
</table>

Note: Gnd. (T1) on both input and output cable to card.

Figure (a)

Note: Gnd. (F1) and output cable to gnd on card.

Figure (b)

FIGURE 52. OUTPUT CONNECTOR WIRING OF PLUG CARD 1-H
Note: GND carried separately from flat cable
Pin 22 to GND bus on card

FIGURE 53. WIRING OF PLUG CARD 2-H
FIGURE 54. PHYSICAL LAYOUT OF PLUG CARDS 2-H AND 2-C
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FIGURE 55. PLUG CARD 1-C (Continued)
<table>
<thead>
<tr>
<th>Block Connector 2-A Position 2</th>
<th>Block Connector 2-A Position 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1 Gnd.</td>
<td>A1 2⁰ Data Word</td>
</tr>
<tr>
<td>B1 Clock Busy</td>
<td>B1 2¹¹ Data Format</td>
</tr>
<tr>
<td>C1 Gnd.</td>
<td>C1 2¹⁰ Data Format</td>
</tr>
<tr>
<td>D1 C4</td>
<td>D1 2⁹ Data Format</td>
</tr>
<tr>
<td>E1 Gnd.</td>
<td>E1 2⁸ Data Format</td>
</tr>
<tr>
<td>F1 C3 Clock Reset</td>
<td>F1 2⁷ Data Format</td>
</tr>
<tr>
<td>H1 Gnd.</td>
<td>H1 2⁶ Data Format</td>
</tr>
<tr>
<td>J1 C2 Clock Strobe</td>
<td>J1 2⁵ Data Format</td>
</tr>
<tr>
<td>K1 Gnd.</td>
<td>K1 2⁴ Data Format</td>
</tr>
<tr>
<td>L1 C1 Data Strobe</td>
<td>L1 2³ Data Format</td>
</tr>
<tr>
<td>M1 Gnd.</td>
<td>M1 2² Data Format</td>
</tr>
<tr>
<td>N1 CØ</td>
<td>N1 2¹ Data Format</td>
</tr>
<tr>
<td>P1 Gnd.</td>
<td>P1 2⁰ Data Format</td>
</tr>
<tr>
<td>R1</td>
<td>R1 2⁵ Data Word</td>
</tr>
<tr>
<td>S1 Gnd.</td>
<td>S1 2⁴ Data Word</td>
</tr>
<tr>
<td>T1</td>
<td>T1 2³ Data Word</td>
</tr>
<tr>
<td>U1 Gnd.</td>
<td>U1 2² Data Word</td>
</tr>
<tr>
<td>V1</td>
<td>V1 2¹ Data Word</td>
</tr>
</tbody>
</table>

(c) Connector Wiring of DEC Block Termination

**FIGURE 55. PLUG CARD (1-C) (Concluded)**
FIGURE 56. DEC BLOCK LAYOUT

VIEWED FROM CARD SIDE WITH COMPONENT ON RIGHT SIDE
FIGURE 59. PHYSICAL LAYOUT OF PLUG CARD 4-C
connection to the computer via the DR-11B is through line drivers and receivers located on the card plugs; these cards are detailed in Figs. 61 and 62. The classifier inter-bay wiring and cabling to the DEC block are shown in Fig. 63.
FIGURE 61. CABLE TERMINATIONS FOR DATA TRANSFER FROM COMPUTER TO CLASSIFIER
FIGURE 62. CABLE TERMINATIONS FOR DATA TRANSFER TO COMPUTER FROM CLASSIFIER
(b) Sheet 2

FIGURE 63. INTER-BAY WIRING (Concluded)
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