INFLUENCE OF MATERIAL QUALITY AND PROCESS-INDUCED DEFECTS ON SEMICONDUCTOR DEVICE PERFORMANCE AND YIELD

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I. INTRODUCTION

The semiconductor industry has made great strides in the past few years towards the development of better process controls and techniques in an effort to increase device performance and yields. However, many problems associated with starting material quality and process-induced defects still remain and continue to take their toll on device yields each day. With the introduction of new crystal purifying and growing techniques, the "perfect" silicon crystal is now almost a reality. Crystals with virtually zero dislocation density are now being manufactured.[1]

In spite of these tremendous advances in crystal growing technology, device yields do not show a corresponding improvement. The primary reason for this is because process-induced defects are, and have been, the major source of crystal lattice imperfections and impurities.[1,2,3] Many of these defects are introduced during the oxidation, diffusion and photolithographic processes. Although defects created early in the manufacturing process can be critical, most IC failures have consistently been due to defects introduced in the latter processing steps such as metalization, bonding, passivation and encapsulation.[4] With today's emphasis on LSI, further improvements in each processing step will have to be made to increase device yields and performance.

It is difficult to generalize on which problems are most significant without classifying them according to device type. For instance, the predominate sources of failure in MOS devices are oxide shorts, oxide contamination and poor metalization.[4] Failure of most transistor types is due to surface defects, bonding, metalization, and packaging.[5] A major problem with power devices is second breakdown and hot spot formation due to precipitation effects within

the crystal lattice. Microwave device problems include electromigration of aluminum metalization due to large bias currents, stress effects due to thermal mismatching and collector - emitter shorting due to extremely small base widths. In the bipolar LSI technology, oxide pinholes, wire bonds and surface contamination effects are of major concern.[4]

A brief overview of major causes of device yield degradation indicates that the problems are very much a function of device type. Therefore, some processes are more critical to yields of certain devices than others. In the following sections device types will be related to critical processes and typical defects which often occur. The influence of the defect on device yield and performance will also be presented. The result will be a comprehensive correlation between the problem, the defect which caused it, the process in which the defect was probably generated and the process changes recommended to reduce or eliminate the problem. Further, various defect characterization techniques commonly used to detect critical defects are described, and the following section of this handbook is devoted to the description and applications of specific characterization techniques.

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II. DEFECT CHARACTERIZATION TECHNIQUES

In order to determine the cause for poor yields and performance variation for a particular group of devices, there must be a means of detecting the type of imperfections present which might cause the specific failure. Many such characterization techniques exist and each has its own special application. These methods may be classified generally into five major groups: 1)Microscopy, 2)Spectroscopy, 3)X-ray Topography, 4)Chemical Etch and Visual Inspection, and 5)Various electrical, parameter and bulk property measurements.

Each technique will be discussed in general by listing the various defects the technique will reveal, the advantages, disadvantages and limitations of the technique, approximate analysis times, and specific characteristics of the technique. The details of instrumentation and procedure are widely available for the more commonly used techniques and will not be discussed here. Where the technique is not often used, reference is made to other sources for further details.

MICROSCOPY

Scanning Electron Microscopy (SEM)

This instrument can be very useful and operates in many different modes. The SEM can be used as a relatively low power microscope for inspecting wire bonds, oxide steps, and metalization patterns with distinct advantages over optical microscopes because of its great depth of field. Using this mode of operation, corrosion and adherence of wire bonds, open metal at oxide steps, quality of metalization etch, surface debris, and many other characteristics may be observed.[1]

Another important application of the SEM is its use in the voltage contrast mode.[2,3] The voltage contrast technique includes a conduction and emissive mode. In the conduction mode, currents generated in the specimen by the electron beam are detected and displayed to give information concerning the bulk properties of the silicon material. Used in this manner, boundaries of diffusion regions, junction profiles, dislocations near the junction, and similar bulk characteristics may be observed. In the emissive mode, the device is properly biased, and the secondary electrons emitted by the specimen are used to reveal the potential gradients on the surface of the device. Potential differences as small as one-quarter of a volt have been detected by this method, and defects such as open metalization, thin metal over oxide steps at contact windows, surface leakage between diffused regions, shorted metalization, and other anomalous potential gradients may be revealed.[3]

A third mode of operation for the SEM requires that an X-ray spectrometer be used in conjuction with it.[1] This method allows the detection of foreign particles in localized concentrations less than .1% through analysis of characteristic X-rays emitted when the SEM electron beam impinges upon an area of the specimen. Many other techniques used to detect small amounts of impurities are not this sensitive.[4]

Transmission Electron Microscopy (TEM)

This tool for defect characterization is limited in its applications, and it is a destructive technique compared to the largely non-destructive tests implemented with the SEM. In order to observe a specimen with TEM techniques, the sample must first be thinned to less than approximately 1μm. Often the specimen is chemically thinned from the substrate side leaving only the surface for observation. Usually the interface regions will be removed so that thinning

from both sides must be done if junctions and other interface regions are to be observed. An ion-beam thinning technique has also been developed so that wafer cross sections including all the junctions might be examined.[5]

The TEM is useful in delineating many types of crystallographic imperfections. The growth of dislocations and stacking faults from epitaxial surfaces are easily observed. Surface damage due to ion implantation, dislocation networks, precipitates, doping variations, and various crystallographic inhomogineities may also be revealed.[6] The disadvantages, however, are that this method of microscopy is time consuming (typically many hours) and destructive.

Infrared Transmission Microscopy

Another transmission microscopy technique has been developed that is completely non-destructive, simple and inexpensive, and has relatively high resolution and contrast.[7,8] The infrared transmission microscope consists of a simple lens system, and x-y-z stage, a silicon vidicon T.V. camera and a video monitor. Features less than 2μm in size can be resolved, and specimens in the range of .25mm (10 mils) in thickness may be studied. The system is useful as a high power microscope for surface studies of integrated circuits, or it may be used to detect precipitates, decorated dislocations, and doping variations in silicon material.

Optical Microscopy

There are some advantages to optical microscopy which should not be ignored. A high quality metallurgical microscope may be used as a simple and quick method for high resolution surface studies. When used in conjunction with various chemical etches, much information can be revealed about the quality of the silicon surface and process-induced imperfections. It may also be used

to inspect oxide steps, metalization patterns, wire bonds and packages containing processed devices. The advantages over the SEM, which is also used for similar studies, are superior resolution, color contrast, time savings, and ease of operation.

SPECTROSCOPY

Auger Electron Spectroscopy[4,9,10]

Auger spectroscopy is a procedure for detecting trace impurities in semiconductor surfaces. The technique involves the evaluation of emission spectra from samples bombarded by a low energy electron beam. The system is very sensitive to all elements except hydrogen and helium, and can detect at atomic concentrations of less than 0.1%.[10] When Auger analysis is combined with ion-beam etching impurity profiles may also be obtained. The technique may be used to trace the source of precipitate impurities and study any other failures which might be caused by random impurities.

Secondary Ion Mass Spectroscopy[11,12]

This technique employs an ion-beam that sputters secondary ions from the specimen surface where mass analysis can be used to determine identity and concentrations of an impurity. The specimen surface is actually eroded away, and therefore, depth profiles of the impurity may be obtained with better sensitivity than Auger spectroscopy. Typical sensitivities range from 1.6×10^{11} atoms/cm^3 for chromium to 4.1×10^{15} for silicon, depending upon the ion source. This method may be used in failure studies similar to those listed for Auger analysis.

Ion Induced X-ray Analysis[13]

X-rays that are characteristic of various elements are emitted when bombarded

by a high energy (30-300 Kev.) ion or proton beam. This is the principle behind ion-induced X-ray analysis. The technique can be used for trace impurity anlaysis in semiconductor material where relatively large probing depths are desired (approx. 2μm). This method of impurity detection has practically no advantages over the other techniques that have been discussed, and the major disadvantages are its high cost and longer analysis time.

X-RAY TOPOGRAPHY

Lang Technique[14]

X-ray topography is an excellent technique for examining defect structures in silicon because it is non-destructive and therefore potentially applicable to process control. The Lang technique is based on the variation in diffraction intensity of transmitted X-rays in the presence of changing crystallographic orientation or dislocations. The X-ray topograph, as recorded on a photographic plate, reveals these variations and dislocations as dark areas. The method has very high contrast and high resolution, but it requires long exposure times and cannot be used in the presence of large amounts of elastic or residual strain.[15] Therefore, large area topographs are impractical.

This method of recording X-ray topographs is primarily useful in detecting small amounts of lattice strain, dislocation networks, stacking faults, and other crystal misorientations. This particular technique is not directly applicable to process control because exposure times for suitable areas usually require many hours. It can be useful in other types of defect analysis where high resolution over small areas is of prime importance.

Scanning Oscillator Technique

Another modification of the basic X-ray transmission method overcomes the major disadvantages of the Lang technique. Large area topographs can be made

with much shorter exposure times (less than one hour) using the scanning oscillator technique.[16] An automatic Bragg angle control has been devised and may be added to the system to further reduce exposure times.[15] Contrast is also improved with an increase in picture definition. The topographs are uneffected by the presence of residual or elastic strains, therefore, silicon wafers may be examined before and after various process steps to pinpoint the generation of the defects. This method can reveal the presence of dislocations, stacking faults, precipitates, and various crystal misorientations.

Video Displayed X-ray Topographs[17]

This method utilizes an X-ray sensitive vidicon T.V. camera to display crystal imperfections. The resolution of this system is not as good as that for the techniques described above, but single dislocations may be directly viewed eliminating long exposure times. This system is still in the early stages of development however, and its applications are very limited. The technique has been used to view moving dislocations, indicating the feasibility of studying the dynamic properties of dislocations.

Limited Projection Topography

It is often useful to know exactly where in the crystal dislocations are located. The X-ray topograph techniques discussed thus far show a superposition of the dislocations scattered throughout the entire thickness of the crystal. Using limited projection topography, dislocations in different layers of the crystal may be separately observed.[18] The technique is valuable in that the relationship between the locations of dislocations, stacking faults and other imperfections, and the location of the active regions of devices may be determined non-destructively.

CHEMICAL ETCH AND VISUAL INSPECTION

Sirtl Etch

This is by far the most commonly used etch to delineate various crystallographic faults which intersect the surface of the silicon wafer. Some of the defects which may be revealed include microcracks, lap damage, dislocations, slip lines, stacking faults, resistivity rings, swirls, and twins.[19] Sirtl etch is prepared by dissolving 50gm of chromic acid (CrO_3) in 100ml of deionized water and adding 75ml of concentrated hydrofluoric acid. Etching times vary from 30 seconds for cracks, lap damage and other heavy work damage, to 5 minutes for dislocations, stacking faults and other crystallographic imperfections. To insure uniform etching, the solution should be constantly agitated during the etching process. After first etching and then flushing with deionized water, and drying with hot, filtered nitrogen, various structures corresponding to the defects present should be visible. These typical structures are pictured with a brief description in the appendix.

A metallurgical microscope with a wide range of magnifications and bright field - dark field capability is necessary to observe and interpret the structures formed by this etch as well as the other etches to be described. The dark field illumination is most useful in observing microcracks, microscratches, and various residues. Also, with this etch, as with all preferential etches, the defect characterization process is always destructive, and this eliminates their usage for in-process test procedures on a production line.

Dash Etch[20]

This etch is used in much the same way as Sirtl etch except that the etching time is greatly increased. Because the etching time is long compared

to Sirtl etch, it is seldom used. However, the etch is used on (100) oriented silicon because Sirtl etch does not work well with this particular orientation. Dash etch may be used to delineate dislocations, swirls, and other crystal imperfections which intersect the silicon wafer surface. This etch consists of one part by volume hydrofluoric acid, three parts nitric acid, and ten parts glacial acetic acid. The amount of acetic acid used may be reduced, however, resulting in a much faster etch rate.

Other Preferential Etches[21]

A number of other etches which delineate various crystallographic faults may be used. These are listed below with their chemical compositions:

CP-4 - 15ml HF, 25ml HNO_3, 15ml CH_3COOH, .3gm Br_2

White - 1 part HF to 3 parts HNO_3

No. 1 - 1 part HNO_3, 2 parts HF, 1 part $Cu(NO_3)_2$ solution (10%)

Iodine - 110ml CH_3COOH, 100ml HNO_3, 50ml HF, 3gm I_2

SD-1 - 25ml HF, 18ml HNO_3, 5ml CH_3COOH, .1gm Br_2, 10ml H_2O, 1gm $Cu(NO_3)_2$

WAg - 40ml HF, 20ml HNO_3, 40ml H_2O, 20gm $AgNO_3$

Etching times for these etches may vary from one to five minutes, depending upon the amount of strain or damage in the sample.

ELECTRICAL, PARAMETER, AND BULK PROPERTY MEASUREMENTS

Device Parameter Measurements

There are many different instruments available to measure various parameters of finished devices. If the device is encapsulated, measurements such as transistor gain, junction leakage current, dynamic resistance, breakdown voltage and similar characteristics are easily made. These parameters are most often measured before encapsulation, however, and various manual, semi-automated

and automated probing stations are used to detect faulty devices. These are all routine measurement techniques used in every semiconductor production facility.

Detecting parameter variation in this manner is usually the first step in failure analysis. If a large number of devices are failing in the same manner, immediate characterization of the defect and tracing the source of the failure will be necessary. This characterization may include any of the more sophisticated techniques already mentioned, or more in depth electrical measurements may reveal some information about the cause of failure. Of course, these techniques may also be used to study poor yield problems where sudden failure of a group of devices is not necessarily involved.

Scattered Light Surface Defect Detection[22]

This technique may be used to quickly examine entire polished wafer surfaces for defects such as pits, mounds, scratches, particulates, and debris. The system includes a 5 mw laser as a light source and a photomultiplier tube as the detector which senses the amount of scattered light corresponding to a surface defect. The output can be displayed on an oscilloscope or automatically processed and used to automate rejection of damaged wafers. The method may be used to monitor the quality of wafer polishing, clean up processes, condition of epitaxial surfaces and other processing steps which might introduce detectable surface defects.

ASTM Standards[19]

The annually published ASTM standards contain many material characterization techniques applicable to semiconductor devices. These are listed in part 8 of the standards each year, and the standards pertaining to the electronics

industry have alphanumeric identification codes beginning with the letter "F".

The entries include many types of material, process, and reagent evaluation techniques. Many of the more common material bulk property measurements described are useful in characterization of silicon material. Tests for the evaluation of various processing environments and reagents are included and can be used to monitor critical areas of device fabrication. An especially good standard entitled "Nomenclature and Recommended Practices for the Identification of Structures and Contaminants on Specular Silicon Surfaces" (F 124-72T) is also included. This entry briefly describes most types of surface defects which occur on silicon material and provides an example of how each particular defect appears when observed by a specific observation technique.

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III. CRITICAL DEVICES

Typical yield percentages for semiconductor devices range from 90% to 100% for many transistors, diodes, and small scale integrated digital IC's to less than 1% for many large scale integrated IC's. There are certain critical device types which are clearly identified by their lower yields. Specific defect types are more critical to the operation of theses devices because the electrical effects of the defect have become more pronounced under the conditions of operation, or the defect occurs with greater frequency because of the particular device geometry.

These critical devices include both bipolar and MOS types, integrated and single device structures and both linear and digital functions. Bipolar devices which exhibit the poorest yields are high frequency transitors, high voltage transistors, high current power devices, linear IC's and large scale integration (LSI) devices. MOS devices generally exhibit poorer yields than bipolar devices because of the nature of the critical device problems and because the MOS technology is more recently developed technology which has not been subject to the many years of improvement as has the bipolar technology. Critical MOS devices include n-channel transitors and LSI, MOS digital arrays such as memories and electronic calculator circuitry.

The high frequency bipolar transistors are sensitive to certain defects because the base widths have to be made much narrower than the lower frequency types. Process-induced dislocations and stacking faults introduced during epitaxy provide precipitation sites for heavy metal impurities and can enhance diffusion so that emitter - collector shorts result.[1,2,3,4,5] Further, incomplete oxide removal from diffusion windows can cause drastic variations in junction

depths in shallow diffused transitors. Slight variations in diffusion temperature from batch to batch are more detrimental to high frequency devices because the corresponding small changes in base width are a much greater percentage of the total base width and severly reduce frequency response.

High voltage transistors are more sensitive to doping variations. High resistivity material (low doping density) is required in high voltage devices to give the required breakdown characteristics. Localized impurity concentrations have more pronounced effects in high resistivity material because the unwanted impurity can be a much greater percentage of the total impurity present.[1,6] Therefore, stray impurities and precipitates can drastically reduce the junction reverse breakdown voltages, and doping variation across a wafer can cause large variation in breakdown voltages.

Many bipolar power devices which conduct high currents are susceptible another breakdown phenomenon known as second breakdown.[7] Second breakdown in transistor structures manifests itself as a sharp drop in V_{ce} and an increase in I_c. It results from an increase in temperature due to hot spot formation caused by localized current crowding. Precipitates in the vicinity of a junction can be responsible for the current crowding phenomenon.[8,9] Also, diffusion spikes caused by enhanced diffusion along dislocation lines can create locally high electric fields which can lead to second breakdown.[6] Diodes and P-N-P-N power devices also exhibit second breakdown for similar reasons. In diodes, this type of reverse breakdown is often revealed by low voltage resistive breakdown occuring before avalanche breakdown.

MOS devices are much more sensitive to oxide contamination than are bipolar devices. Ionic contaminants, mostly sodium, can have very detrimental effects on n-channel MOS transistors. Under proper bias, the positive ions in the oxide

may migrate to the oxide-silicon interface and, by inducing a negative image charge in the silicon, can greatly reduce the gate threshold voltage.[10,11] Nevertheless, with improved processing techniques, n-channel devices can be made more stable than p-channel types. These improvements include using phosphosilicate glass (PSG) for gate oxides and using (100) oriented silicon for n-channel devices instead of the (111) orientation used for p-channel devices. MOS devices are much less sensitive to crystallographic defects, and almost all yield problems are associated with the oxide, metalization, or encapsulation.

The greatest yield problems in the semiconductor industry occur in the processing of LSI circuitry. The large die sizes and reduced geometry of LSI circuits make them much more sensitive to surface defects and impurities. Because the area of the LSI chip is so much larger, the number of defects per chip should be expected to increase under normal IC processing conditions. Also, the smaller geometry of the individual devices in an LSI circuit makes them more defect sensitive. A relatively low density of defects can reduce the yield of these devices to almost zero because of the large number of defects per device and the increased vulnerability to defects.

To achieve practical yields, LSI devices must be manufactured in extremely clean environments and with the purest reagents. Dust, residual photoresist, and impurities in the reagents cause defects which account for a great percentage of LSI yield losses. In the photoresist process, any particulates in the emulsion can cause pinholes in the oxide resulting in unwanted diffusions and possibly metalization shorts. Also, the registration requirements for LSI photomasks are more stringent, and slight errors result in shorted diffusions, inadequate metal contact coverage and gate misalignment in MOS devices which leads to threshold voltage problems. Ionic contaminants in the oxide can result

in surface inversion that may create conductive paths between normally isolated regions. Thus, the purity at the oxide growth environment is of extreme importance, especially in the manufacture of MOS, LSI devices.

There are also problems associated with the application of new process techniques used in the production of LSI devices. Special packaging problems and multilevel metalization are two of the most troublesome. Defects associated with multilevel metalization include metal to metal shorts, open metal at oxide steps and overalloying. Metal to metal shorts result from oxide pinholes which arise from the photoresist problems discussed above. Open metal at the oxide windows between metalizations is a common problem. This type of defect arises from the difficulty of covering the steep and sometimes undercut oxide steps with metal. These problems occur due to the thickness of the isolation oxide and the variations of oxide etch rate with depth. Overalloying metal contacts to MOS gates can also occur. Gate oxides are approximately 1000 Å thick, and in areas where the oxide is thin, aluminum can often penetrate the oxide in a short time (10 minutes) at standard alloying temperatures.[12]

Packaging presents a greater problem to LSI devices than conventional IC's because of increased package sizes and number of external leads. Hermetic sealing of packages can be very critical because contaminants leaking into the container tend to cause gross surface effects which may result in device failure. Square package lids are subject to higher stresses at corners sometimes resulting in package leaks. Circular lids have been effective in eliminating these leak problems.[13] Die bonding may also be a problem in LSI encapsulation because the increased die sizes make LSI circuits more susceptible to void formation between die and package.[14] These voids can result in hot spots which may cause device failure.

The critical device types which have been discussed are by no means the only types that experience special difficulties. The defects encountered in the processing of the devices discussed are well documented in the literature. The devices which were not discussed are not documented in the open literature. This void of information points to the need for further experimental work and better documentation of typical process-related device problem areas. New types of defect problems occur with each new device type while improved fabrication techniques are reducing other defect problems. Processing steps and typical defects which are often generated in each are the subject of the following section. A basic knowledge of the defects which commonly occur during different processing steps will be very helpful in device failure analysis.

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IV. Process Steps - Defects Which Typically Occur

During the production of semiconductor devices, silicon wafers are subjected to many different processes in varied environments. Proceeding in the order of normal occurrence, processing steps include: wafer preparation (growth, sawing, polishing), clean up, epitaxy, oxidation, photomasking, diffusion, metalization, die separation and bonding, wire bonding and encapsulation. Different groups of defects are commonly generated in each of these processes due to inadequate device design, poor processing techniques, insufficient control of process parameters, or combinations of these reasons.

WAFER PREPARATION

The defects introduced at this stage are generally due to mechanical damage. In order to achieve highly polished wafer surfaces, the wafer is both mechanically and chemically polished on one side. Insufficient chemical etching can leave small amounts of surface damage, especially towards the edges of the silicon wafer. When the damaged wafer is exposed to the high temperature oxidation and diffusion processes, this damage can result in points of high stress which often cause the generation of large dislocation loops and serve as sites for heavy metal precipitation.[1,2] Microcracks may also be present due to insufficient chemical etching. This type of defect can initiate slip in epitaxy and oxidation and often causes yield losses due to edge chipping. Further, edge chipping may leave small silicon particles on the wafer surface which can cause oxidation and photoresist problems.

WAFER CLEAN-UP

This step is a very critical process of fabrication, especially for the

production of LSI devices. The surface of incoming wafers is always thoroughly cleaned using one of many clean-up procedures usually employing a strong solvent such as trichloroethylene, an alcohol rinse, a hot acid treatment, and deionized water rinses. Ultrasonic cleaning and chemical etching are also used to remove surface impurities. Contaminated cleaning solutions, containers, and cleaning equipment can leave impurities on the wafer surface which result in pinholed oxides, stacking faults in epitaxial layers, poor photoresist adhesion, poor metal adhesion, precipitation at defect centers, and many other types of device degradation. Wafer clean-ups and rinses are used throughout the manufacturing process, therefore, contamination introduced in this particular step has a high probability of occurence unless the purity of all reagents and deionized water are constantly and carefully monitored.

EPITAXY

The most common defect introduced during epitaxy is the edge dislocation.[3] These dislocations cause strain in the silicon lattice and can act as sites for the precipitation of impurities present in the lattice. They can be extentions of dislocations present in the substrate surface or caused by a poorly cleaned surface of the substrate. Stacking facults are another defect type generally caused for the same reasons. Work damage, impurities and particulates, and local stress on substrates can also induce the growth of stacking faults. Further, incomplete oxide removal may cause them to occur. Stacking faults as well as dislocations cause locally enhanced diffusion resulting in junction shorts and decreased breakdown voltages.[4,5]

Other defect structures which can occur include hillocks and pyramids. Hillocks are formed in much the same way as stacking faults. Pyramids are

created on the surface when layers of high doping concentration are grown. All of these lattice defect types can be virtually eliminated by proper surface cleaning procedures. An effective in situ cleaning procedure widely used is to pre-clean the substrate in H_2 at 1200°C and then flush with HCl just prior to epitaxial growth.

OXIDATION

The oxidation process is used in all semiconductor manufacturing technologies. The oxide may serve many purposes including masking in diffusion, passivation, insulation, and as a part of the device structure in MOS transistors and some integrated capacitors. Typical problems associated with the oxide are pinholes, rupture, strain induced dislocations, contamination, surface inversion and some etching difficulties. The oxide is a direct electrical component of MOS devices, and accordingly more MOS device failures are attributed to oxide defects. Oxide defects are not as critical in bipolar devices, but oxide device-degradation can occur.

Most oxides are thermally grown at high temperatures using either steam, wet or dry oxygen as a growth ambient. For a given temperature and time, steam will produce the thickest oxide and dry O_2 the thinnest. However, the steam grown oxide is generally more contaminated and for this reason a dry O_2 grown oxide is used for thin gate oxides while steam and wet O_2 are used for isolation and diffusion oxide masking.[6] The largest contaminant in all oxides is sodium which ionizes and becomes mobile in the oxide lattice. These ions drift, depending upon operating temperatures and bias, causing various surface instabilities. Surface inversion creating conducting channels between normally isolated regions causes large increases in leakage currents in bipolar

planar devices. In MOS devices, especially N-channel types, mobile ions can cause large changes in gate threshold voltages as well as increased leakage currents.[6,7,8] The use of phosphosilicate glass and silicon nitrides as passivation layers have decreased mobile ion problems in many device structures.[9]

Thermal strain at oxide-silicon interfaces can occur during diffusion and result in strain-induced dislocations and oxide rupture.[3] These dislocations in the area of the junction can cause increased leakage currents and ruptures and microcracks which may lead to diffusion shorts, leakage, or decreased breakdown voltages due to unwanted diffusions. Diffusion windows which have square corners seem to exhibit more strain than ones with rounded perimeters, as would be expected. Pinholes in the oxide can also lead to unwanted diffusions and metalization shorts to underlying silicon. These pinholes are caused by the presence of surface debris during photolithography or by inherently nonuniform oxide growth across the wafer. Thin oxide regions due to nonuniform growth may lead to capacitive inversion of underlying silicon or cause changes in MOS threshold voltages and gate breakdown voltages.

Oxidation may also induce stacking faults in the silicon wafer surface.[4,10,11] This type of defect may cause locally enhanced diffusion resulting in collector-emitter shorts in shallow transistors or decreased breakdown voltage and increased reverse leakage. Other oxide failures are due to poor design of oxide steps at diffusion windows and oxide etching procedures. Oxide window edges which are very steep or undercut are difficult to cover with metal.[9,12] Steep edges are usually due to poor design, and undercutting can occur when etching some types of doped glasses. LSI circuits with multilevel metalization are particularly sensitive to these problems because a very thick oxide must be grown between

metalizations, and the deep windows cut for interlevel connections sometimes exhibit etching difficulties.[12] Phosphosilicate glass passivation layers are susceptible to undercutting because the oxide near the silicon etches at a faster rate due to the higher phosphorous concentration there.[9] Underetching can also be a problem. If the wafer is not sufficiently etched during window cutting, thin oxides will be left in some windows while the silicon surface is exposed in others. This will cause large variations in junction depths resulting in drastic variations in device parameters.

PHOTOLITHOGRAPHY

Most of the defects that occur at this step are due either to a defective mask or mask misregistration. Typical defects resulting from errors in this process include oxide pinholes, unwanted diffusions, thinned oxides and shorts or opens in the metalization. Misregistration of the diffusion masks may cause unwanted diffusions resulting in poor device performance, increased leakage, or shorts between normally isolated diffusion regions. During metalization, mask misregistration may cause shorts, opens, or weak interconnects susceptible to electromigration. In MOS devices, metalization mask misregistration may cause high fields to exist at the gate resulting in ionic surface leakage and oxide breakdown.

A defective mask or debris on the mask or wafer surface may lead to oxide pinholes, unwanted diffusions and further mask damage if debris is present. Etching the undeveloped photoresist for oxide removal can be very critical, especially for MOS and LSI circuits. Some breakdown of the photoresist during the pre-ohmic etching procedure can create shorted MOS gates and thinned oxides causing capacitive inversion of underlying silicon. Prolonged etching times

may result in oxide undercutting which may cause poor reproduction of the photomask pattern where small line widths are involved. Underetching diffusion windows can cause drastic variations in junction depths due to the thin oxides which may be present in some windows. If underetching occurs in the pre-ohmic etch, open metalization contacts may occur. After metalization, selective etching to create the interconnect pattern may leave shorts due to formation of hydrogen bubbles on the metal surface which prevent etching. This problem may be reduced by ultrasonic agitation during etching.

The photomasking procedure is a very critical step in LSI processing. Much tighter requirements on mask registration and cleanliness have led to the development of new photomasking procedures. Double layers of photoresist and multiple exposures have been used to reduce the number of defects generated, but this makes the tolerances on alignment even more critical. Thus, other techniques such as projection photomasking and electron beam exposure are being developed.[13,14]

DIFFUSION

Although various defects introduced during this process have been extensively studied by researchers over the past two decades, still relatively little is known about the actual mechanisms of defect generation during diffusion. However, some very definite conclusions may be drawn from the work already done and used to increase device performance and yield. The most common defect occcuring during diffusion is dislocation of the silicon lattice. These dislocations can be generated due to internal stress caused by contraction of the lattice during phosphorous or boron diffusion, or by external stress due to non-uniform radial temperature distributions or silicon-oxide interface stresses at diffusion window edges.[2,8,15,16,17] Dislocations induced by non-

uniform temperature distributions can be significantly reduced by processing wafers horizontally so that all areas of the wafer cool uniformly. However, an economical production means of doing this has not yet been developed. Dislocations usually cause degradation only when they are in the vicinity of the junction. They may cause high leakage currents or induce locally enhanced diffusion which may cause junction shorts or lower breakdown voltages.[4,5,18]

When precipitation occurs at a defect site, such as a group of dislocations, the electrical effects can be greatly increased. Precipitation of impurities such as heavy metals may cause large increases in junction leakage currents and seriously lower junction breakdown voltages.[15,19] Gold diffused into bipolar devices to decrease switching times may also precipitate and form a complex with phosphorous in N^+ regions.[2] These precipitates rob the lattice of the gold and reduce its ability to decrease storage times, and they may generate small microplasmas leading to second breakdown and reduce breakdown voltages.

These diffusion defects may have little effect on most device types, but shallow diffused bipolar transistors and bipolar LSI devices are very sensitive to them. The small geometry used with LSI is susceptible to lateral diffusion problems also. Unless diffusion times and temperatures are well controlled, shorts and reduced punch through voltages between junctions may occur.

METALIZATION

A great part of the process-induced defects which occur are created in latter processing steps including metalization, bonding, and encapsulation. The metalization defects which most often occur include open metal, high resistance regions, low resistance conductive paths and shorts. The phenomena responsible for these types of failures are electromigration, Al-SiO_2 reactions,

Al-Si reactions, and corrosion.[20]

Electromigration occurs in thin aluminum films at elevated temperatures when the cross-sectional area of the conductor is sufficiently reduced.[21] Most devices should be designed so that current densities greater than 2×10^5 A/m^2 do not occur.[9] However, various processing errors may cause failures even though the design was proper. Mask misregistration and mask defects may result in conductor stripes which are too thin or shorts between adjacent stripes and open circuits. Current densities in thin conductors may become excessive and eventually cause electromigration failure. Oxide steps are often difficult to cover, because of steep edges, and can cause thinned regions in the conductor path to occur. These regions are very susceptible to electromigration failure due to a local high current density. Multiple deposition sources are used when evaporating aluminum films to eliminate shadowing at oxide steps and result in a more uniform metal thickness, but steep oxide steps are still difficult to uniformly cover. Poor monitoring of film thickness during deposition may also result in thin metalizations.

Opens and shorts in metalization stripes may occur due to scratches or smears incurred during handling or deficient procedures. Overetching the aluminum while cutting the metalization pattern may result in opens as the etch slowly dissolves metal under the photoresist. The problem is more often due to poor adhesion of the resist caused by contamination of the wafer surface or the resist. In multilevel metalizations, overetching of the first level metal may occur when etching the feed-throughs to the second level. Shorts between the aluminum and underlying silicon may occur during excessive heat treatments due to a slow Al-SiO_2 reaction at elevated temperatures. At annealing temperatures,

the reaction proceeds fast enough to short through the SiO_2 layer in sufficiently thin regions, such as thin regions of an MOS gate oxide, within normal annealing times (10-15 mins.).[12] Also, an Al-Si reaction can occur during annealing at contact cuts and result in metal shorts to underlying silicon. Migration of aluminum outward from Al-Si contacts along the Si-SiO_2 interface may also occur during annealing and may short to another p-type region or form a Schottky diode to n-type silicon. This type of defect is more likely to occur in LSI devices where diffusions are very closely spaced.

Chemical and electrolytic corrosion of the metalization may occur and lead to open metal conductor stripes. Chemical corrosion may be caused by traces of various etchants that were not removed from the wafer surface and is usually a time dependent failure accelerated by temperature and energizing the device.[12] Electrolytic corrosion is perhaps more likely because only an ionic medium and bias to the device is required.

DIE ATTACHMENTS

There are three different techniques which are commonly used to attach die to packages.[9] An alloy mount is made by alloying a thin gold layer on the die which is bonded to the package. The frit mount is made when a low melting temperature glass is used as the bonding material. Conductive and non-conductive epoxies are also used to bond die to packages.

Alloy mounts may cause problems when complete wetting of the die and package does not occur. Voids can form and reduce the ability of the package to dissipate heat generated in the device.[12] Non-uniform or excess wetting of the die and package may cause the die to bond so that it is not parallel to the package surface. This may lead to excessive necking-down of wire bonds and

decreased bond strength. Both of these problems are greatly magnified for LSI devices because chip power densities are much greater and chip sizes are larger. Void formation may also be caused by intermetallic impurity formation and solid state diffusion reactions at higher temperatures.[22] These types of voids may occur with power devices and can cause excessive chip temperatures as can other types of voids.

Oxide impurity may be a source of failure of frit glass mounts. Tight control of glass composition is essential for uniform devitrification. Small amounts of oxide impurity may cause brittle glass to form which can result in failure during shock testing.[9,23]

Epoxy mounts are susceptible to thermal expansion problems.[9] Expansion coefficients of the epoxy may be ten or more times that of the die and package substrate, and burn-in tests with temperatures greater than 100°C may induce large stresses. Also, if the epoxy is not completely thermally cured, thermal expansion during device operation may result in die separation and cracking.

WIRE BONDING

Two types of wire bonds are in general use today. Thermocompression bonding with gold wire has been the standard method of interconnection for many years. Ultrasonic bonding has recently become widely used and aluminum wire is used for the interconnections. A common problem with either type bond is intermetallic compound formation at gold - aluminum interconnects which may lead to weakened bonds and bond separation.[24] Formation of these compounds may result from excessive temperature, bonding pressure, bonding energy (ultrasonic) or bonding time. Exposure to temperatures above 200°C during operation also greatly accelerate their formation. Reliable bonds can be made however by

minimizing the total mass of aluminum available for solid state diffusion at the surface and minimizing the total time - temperature product the device undergoes in manufacture and use.[25]

Other wire bond failures include shorts and opens caused by poor bonding techniques or bonding parameters. Excessive slack in the bonding wires or excessively long pigtails can cause shorts between nearby wires or shorts to metal packages. The temperature - pressure - time combination is very critical in thermocompression bonding.[12] Too much of either parameter may result in weak bonds due to overbonding. Likewise, too little of either parameter may cause similar weaknesses due to underbonding. The parameters which are critical in the ultrasonic bond are energy, clamping force and time. Further, variation in wire tensile strength, ductility, and diameter may cause changes in bond strength if parameter adjustments are not made to compensate for them.[9]

ENCAPSULATION

Many types of device packages are used to encapsulate semiconductor devices of all types. The package types may be generally grouped into four categories including metal, ceramic, glass and plastic packages. Each of these groups may be subdivided further by package material and lid sealing compounds.

Most package failures are due to loss of hermeticity.[9] Leakage can lead to device degradation by ionic contamination, bond and metalization corrosion and increased surface leakage. Device failure may also result if the hermetic seal possesses a large water content. The water in the package can promote metal corrosion and severly increase leakage currents. For the large sealing lids used for LSI devices, lid shape can significantly effect the ability to make hermetic seals.[26] Lids with sharp corners tend to experience higher stresses.

at these points during processing. Plastic dip packages, especially the larger ones used for IC's, cause device electrical failure due to thermal intermittents.[27] The difference in thermal expansion properties of the plastic, chip, and bonding wires may cause bonds to open due to thermal stresses.

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V. Correlation Between Device Failure, Defect Type, and Defect Cause

In the previous sections, various types of failures and degradations have been described. Specific defect types were discussed along with characterization techniques used to reveal the presence of these defects. Further, the sources and generation mechanisms of these defects were discussed and related to specific processing errors, device geometries, and material quality. The purpose of this section is to correlate, in a concise tabular form, the device type, defect, defect influence, analysis techniques, and probable defect causes.

The format of this section is arranged so that all of the information which has been discussed in detail in the previous sections is indexed, by device type, according to a particular kind of device degradation or yield problem. Problems associated with most all semiconductor devices is presented first, and three other categories specific to Bipolar, MOS, and LSI device degradation follows. It is arranged in this manner because, in production, the influence of the defects on device parameters or the condition of the device material is the first indication of degradation. Following the defect influence in the table, probable causes of this influence in terms of particular defect types is given. Then, an anlaysis technique and reference to an example of that particular defect is provided so that positive identification of the defect may be made. If its presence is verified, probable sources of that defect are given to facilitate corrective measures to reduce or eliminate the problem. A more detailed description of the brief statements in the table may be found by referring to the discussions in previous sections of the defect, process, and device type of interest. Of course, not all device manufacturing problems will be found in this table but most of those which are likely to occur or have previously been identified and analyzed are listed.

G E N E R A L

DEFECT INFLUENCE	PROBABLE CAUSE	ANALYSIS TECHNIQUE	DEFECT EXAMPLE	PROBABLE SOURCE
yield loss due to wafer edge chipping	microcracks and work damage, stress on wafer edges or handling damage	SEM, optical microscopy Sirtl etch, light surface defect detection	Figs. 3 & 4	starting material wafers not sufficiently chemically polished after grinding and mechanical polishing
rough surface texture after epitaxial growth (pyramids)	poor surface preparation prior to epitaxy	SEM, optical microscopy		occurs in epitaxial layers of high doping density
unwanted diffusions causing shorts and leakage	oxide pinholes	SEM (conductive mode), infrared transmission microscopy, optical microscopy	Fig. 5	scratched or blemished photomask, particulate impurity in photoresist, particulate matter on photomask or wafer surface during exposure
	photomask misregistration or defective photomask	SEM (conductive mode), infrared transmission microscopy	Fig. 14	defective mask alignment equipment, operator's error
metal to silicon shorts	oxide pinholes	SEM (emissive mode) infrared transmission microscopy, optical microscopy	Fig. 5	scratched or blemished photomask, particulate impurity in photoresist, particulate matter on photomask or wafer surface during exposure
shorted metalization stripes	hydrogen bubble formation during metal removal etch	SEM (emissive mode), optical microscopy		failure to agitate while etching (ultrasonic agitation is best)
open metalization stripes	difficulty in cutting reliable oxide steps in phosphosilicate glass	SEM (emissive mode), optical microscopy		oxide unreasonably thick, poor oxide step design, overetching contact windows in oxide
	poor metal adhesion	SEM (emissive mode), optical microscopy	Fig. 12	wafer surface contamination occuring prior to or during metal deposition, overetched contact windows causing steep oxide steps
	residual oxide in contact windows	SEM (emissive mode), optical microscopy		underetching contact windows during oxide removal
	electromigration	SEM (emissive mode), optical microscopy		metal too thin (caused by poor monitoring of deposition thickness),

CONTINUED

G E N E R A L

DEFECT INFLUENCE	PROBABLE CAUSE	ANALYSIS TECHNIQUE	DEFECT EXAMPLE	PROBABLE SOURCE
"	"	"		oxide step at contact window is too steep, shadowing at oxide steps may occur if a multifiliment system is not used
excessive leakage	surface inversion caused by mobile ions in oxide	SEM (conductive mode)		oxide growth ambient is impure
	capacitive surface inversion	SEM (conductive mode)		nonuniform oxide growth causing thin areas to occur, breakdown of photoresist during any oxide window cut causing partial etching of oxide in some areas
open wire bonds	intermetallic impurity formation	SEM, optical microscopy, Auger spectroscopy		corrosion due to hermetic package leaks, overbonding, excessive chip temperatures
	bond detachment due to weak bond	X-ray of closed plastic packages, SEM, optical microscopy		incorrect bonding parameters, minor variations in wire properties from spool to spool (poor quality), overbonded wire because die not bonded parallel to package
failure of frit glass die bonds	oxide impurity in glass causing nonuniform devitrification			
shorts occuring after encapsulation	shorts between adjacent bond wires or shorts between metal packages and bond wires	X-ray of closed plastic packages, optical microscopy		excessive slack in bond wires, excessive pigtail lengths
general device parameter degradation after packaging (metal packages)	failure of hermetic seal resulting in package leaks which allow moisture to enter and cause surface leakage and corrosion (especially LSI)	one of many hermetic seal tests		poor package design resulting in thermal stress failure at sharp corners in lids or poor lid sealing process
	excessive moisture concentration within the hermetic seal			excessive moisture in the lid sealing ambient

CONTINUED

GENERAL

DEFECT INFLUENCE	PROBABLE CAUSE	ANALYSIS TECHNIQUE	DEFECT EXAMPLE	PROBABLE SOURCE
open metal occuring after extended use	electromigration occuring at metal over oxide steps	SEM (emissive mode), optical microscopy		poor oxide step design resulting in steep edges or shadowing occuring during metal deposition because too few metal sources are used
	electromigration due to generally high current densities in thin metal depositions	SEM (emissive mode), optical microscopy		inadequate metal thickness in design or poor monitoring of metal deposition thickness
thermally intermittant opens with plastic encapsulated devices	bond wires opening due to thermal expansion and contraction	X-ray of package		poor thermal properties of the plastic packaging material

B I P O L A R

DEFECT INFLUENCE	PROBABLE CAUSE	ANALYSIS TECHNIQUE	DEFECT EXAMPLE	PROBABLE SOURCE
high leakage currents	precipitation of heavy metal impurities near the junction	X-ray topography, infrared transmission microscopy, TEM, spectroscopy		high oxygen content in starting material or trace impurities left by the photomasking process
	high dislocation densities	Sirtl etch - optical microscopy	Figs. 2,7 & 10	poor surface preparation prior to epitaxy or swirl patterns in starting material
	emitter edge dislocations	Sirtl etch - optical microscopy	Fig. 9	sharp corners in oxide windows resulting in high thermal stresses
	radial dislocation pattern	Sirtl etch - optical microscopy	Figs. 6 & 10	wafer cool down from high temperature process is too fast
soft junction characteristics	precipitation of heavy metal impurities at dislocations near the junction	X-ray topography, infrared transmission microscopy, TEM, spectroscopy		any of the sources listed for high leakage currents
drastic nonuniformity in characteristics	nonuniform junction depths due to incomplete oxide removal prior to diffusion	optical microscopy,		oxide removal etch was too short
collector to emitter shorting	enhanced diffusion along dislocation lines, lattice slip, or stacking faults located in the base region	Sirtl etch, TEM, SEM (conductive mode)		poor surface preparation prior to epitaxy, nonuniform doping and wafer surface damage
	precipitation of heavy metal impurities at crystalligraphic faults extending through the base region	X-ray topography, infrared transmission microscopy, TEM, spectroscopy		those sources listed above in combination with any of the sources listed for high leakage currents
reduced minority carrier lifetimes	high density of small crystallographic defects such as dislocations and stacking faults	Sirtl etch - optical microscopy, TEM, X-ray topography	Figs. 9 & 11	see Section 4, Epitaxy, Diffusion, Oxidation.
				CONTINUED

B I P O L A R

DEFECT INFLUENCE	PROBABLE CAUSE	ANALYSIS TECHNIQUE	DEFECT EXAMPLE	PROBABLE SOURCE
second breakdown	precipitation of heavy metal impurities at dislocations and stacking faults	X-ray topography, Sirtl etch, infrared transmission microscopy		any of the sources listed for high leakage currents
	diffusion spikes resulting from enhanced diffusion at dislocations and stacking faults	TEM, SEM (conductive mode)		sharp corners in oxide diffusion windows, poor surface preparation prior to epitaxy or some type of wafer surface damage
hot spot formation in power devices	see causes for second breakdown	see analysis techniques for second breakdown		see sources for second breakdown
	resitivity variations causing locally high current densities	Sirtl etch, infrared transmission microscopy	Fig. 1	poor wafer loading or temperature gradients in furnace causing non-uniform doping, starting material resistivity variation
	current crowding at heavy metal precipitation sites	infrared transmission microscopy, X-ray topography, spectroscopy		any of the sources listed for high leakage currents
reduced junction breakdown voltages	see causes for second breakdown	see analysis techniques for second breakdown		see sources for second breakdown
	slight amounts of conductive impurities causing locally high fields	spectroscopy		contamination of wafer surface prior to oxidation or diffusion (residual photoresist, etc.)
high power device failure during extended use	void formation in die bond causing excessive chip temperature	SEM, optical microscopy		poor wetting of die bond due to impurity on wafer surface or package substrate

M O S

DEFECT INFLUENCE	PROBABLE CAUSE	ANALYSIS TECHNIQUE	DEFECT EXAMPLE	PROBABLE SOURCE
low forward transconductance (g_m) in p-channel MOSFET'S	contamination of oxide by mobile ions such as sodium	spectroscopy		contamination of furnace tubes or containers and tools used to handle wafers prior to oxide growth, contamination of water used for steam or wet oxide growth
high source drain conductance in n-channel MOSFET'S	contamination of oxide by mobile ions such as sodium	spectroscopy		contamination of furnace tubes or containers and tools used to handle wafers prior to oxide growth, contamination of water used for steam or wet oxide growth
large MOS gate threshold voltage variation	contamination of oxide by mobile ions such as sodium	spectroscopy		contamination of furnace tubes or containers and tools used to handle wafers prior to oxide growth, contamination of water used for steam or wet oxide growth
	gate misalignment	optical microscopy		poor alignment of photomask caused by defective equipment or the operator
	gate oxide thickness variation over the wafer surface	visual observation		nonuniform oxide growth due to poor growth conditions (thermal gradients, etc.)
reduced MOS gate breakdown voltage	thinned gate oxide	visual observation		nonuniform oxide growth due to poor growth conditions
	extended Al-SiO_2 reaction	optical microscopy		overalloying of aluminum - silicon contacts after metal deposition
shorted MOS gates	extended Al-SiO_2 reaction	SEM (emissive mode), optical microscopy		overalloying of aluminum - silicon contacts after metal deposition

L S I

DEFECT INFLUENCE	PROBABLE CAUSE	ANALYSIS TECHNIQUE	DEFECT EXAMPLE	PROBABLE SOURCE
general yield reduction due to catastrophic failures	trace impurities causing oxide pinholes and unwanted diffusion	SEM, optical microscopy	Figs. 5 & 14	dust and debris on wafer or photomask surfaces, residual photoresist left after photolithographic process, trace impurites in reagents
open metal in multilevel metalization feed-throughs	no contact at interface between the two levels	SEM (emissive)		incomplete removal of oxide in contact window or overetching of oxide resulting in removal of first level metal in bottom of window
	open metal at the oxide step	SEM (emissive), optical microscopy		oxide step is too steep, shadowing occuring during metal desposition because of too few filament sources
loss of hermetic seal in large packages	thermal stress on package lids causing them to open			sharp corners on square lids may induce high thermal stresses (round lids are more reliable)
failure of device during extended use (or burn-in)	void formation in die bond causing hot spots and excessive chip temperature	optical microscopy		poor wetting of die bond due to impurities on wafer surface or package substrate

VI. Conclusion

This handbook is the accumulation of a thorough search of todays literature concerning the influence of process-induced defects on semiconductor device performance. It further contains the results of device-processing research done at the Institute for Solid State Electronics at Texas A & M University during the past three years. During the preparation of this handbook it has become increasingly more evident that the need is great for a better understanding of the device - defect - cause relationship.

Although many defects which occur during the fabrication of silicon semiconductor devices have been thoroughly analyzed and are well understood, the conditions which cause a host of other defects to occur have not been satisfactorily explained. Most of the defect types which are well understood have been discussed in the previous sections of this handbook and a correlation between them and their causes and sources are presented in tabular form in section 5. Typical defects which were discussed in the earlier sections that do not appear in the table are among those which can not yet be satisfactorily explained or correlated.

The information presented in this handbook is intended to bring together the critical information which is currently available concerning the nature of those defects which are presently understood. Three sections of this handbook are separately devoted to presenting this information. The first is a discussion of particular critical device types and the defects which cause major problems with each type. The second is a discussion of various defects which may occur in one of the numerous processes required of the silicon material during device fabrication. Following that is a pictorial characterization of the types of crystallographic defects, contamination, bonding and packaging failures which typically occur. Taken together, the three viewpoints present a balanced discussion

of defect generation and how the defects cause device degradation. It is from these sections that the table of section 5 has been prepared where the device - defect - cause correlation is presented.

While this handbook does not represent the complete processing guide to defects created during device fabrication, it does contain information pertinent to many of the more commonly observed defects and their most probable effect and source.

A P P E N D I X

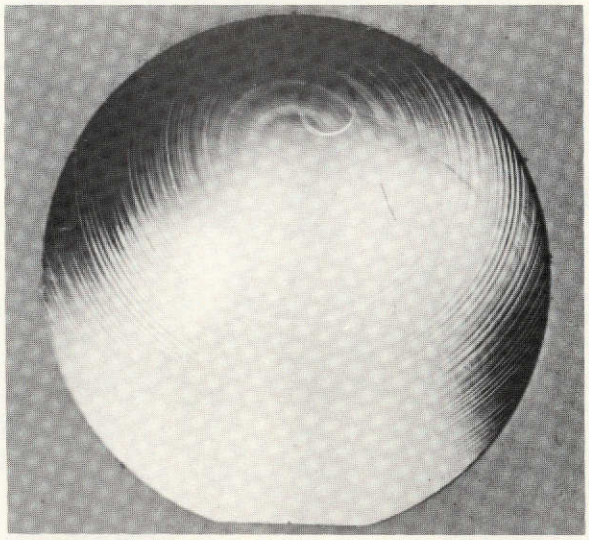

Figure 1: Resistivity rings created during crystal growth. (2X)

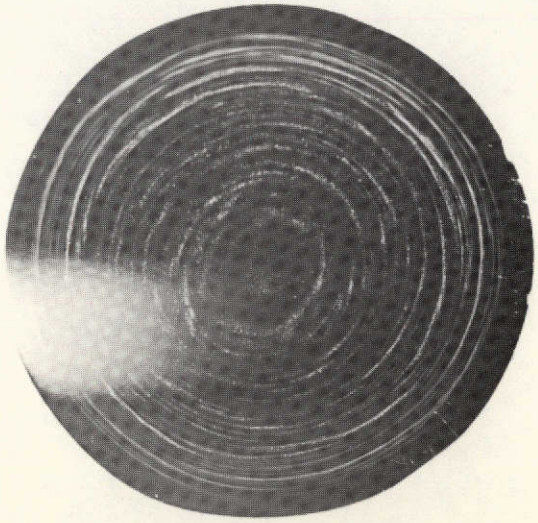

Figure 2: Vacancy cluster swirls created during crystal growth. (2X)

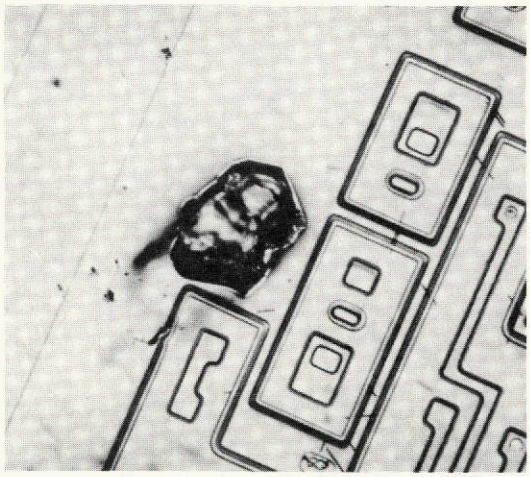

Figure 3: Chip in a wafer surface probably due to handling damage. (175X)

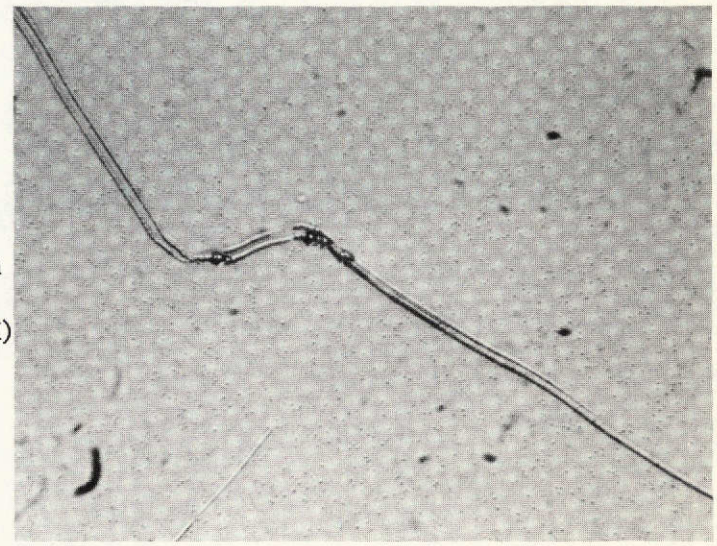

Figure 4: A microscratch typically caused by handling damage. (175X)

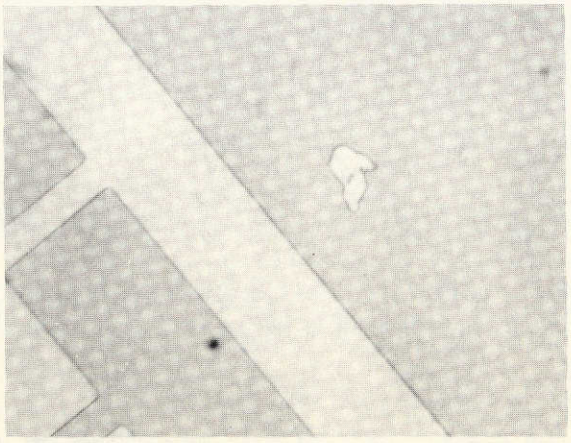

Figure 5: A large oxide pinhole due to some type of photoresist failure. (175X)

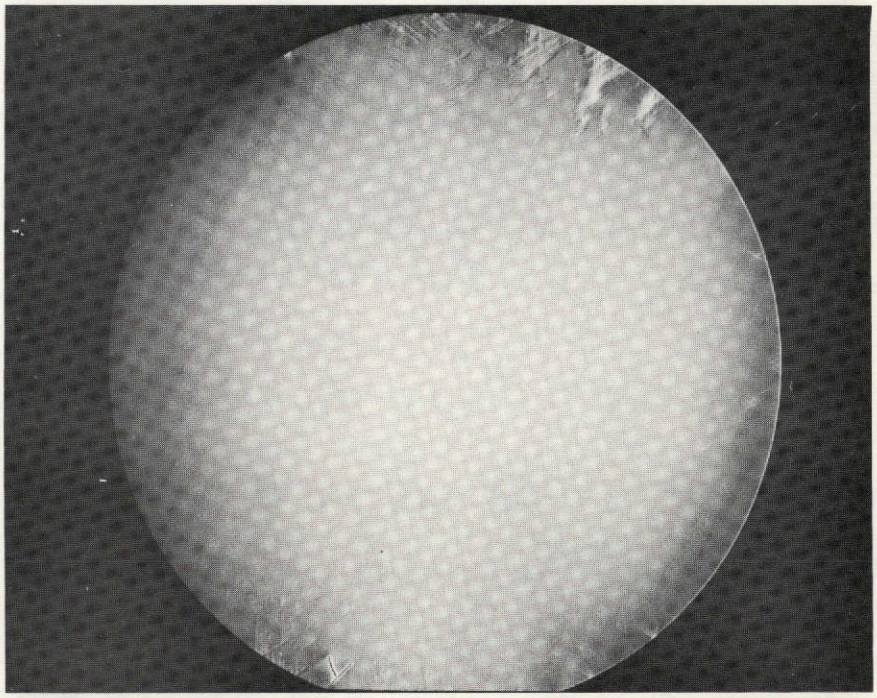

Figure 6: Thermally induced radial dislocation patterns as revealed by an X-ray topograph. (2X)

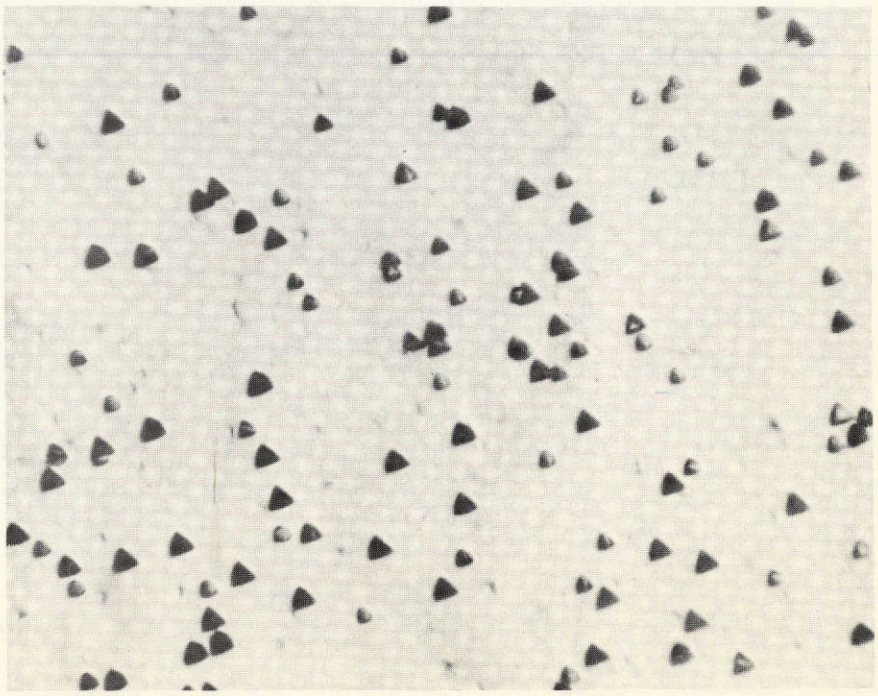

Figure 7: An array of dislocation etch pits revealed by Sirtl etching. (175X)

Figure 8: Massive crystal damage near a wafer scribe mark viewed in dark field optical microscopy. (175X)

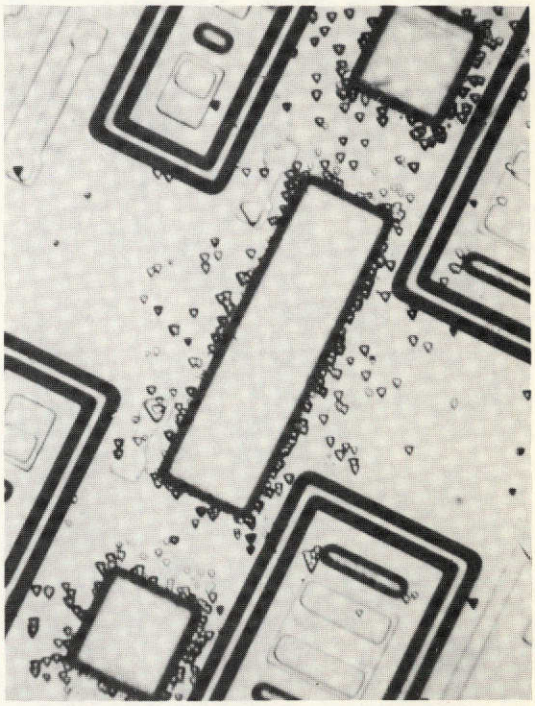

Figure 9: Large numbers of dislocations generated near an oxide step surrounding a heavy diffusion. (175X)

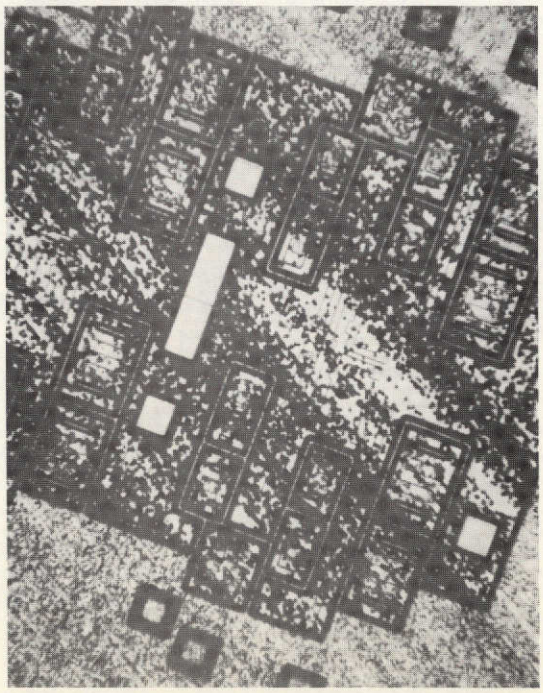

Figure 10: Etch pits revealing large numbers of dislocations throughout the device area due to thermally induced strain near a wafer edge. (70X)

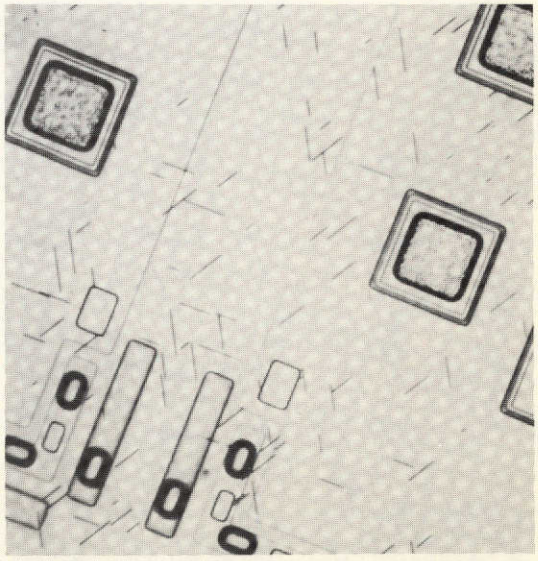

Figure 11: An array of stacking fault structures in an epitaxial layer containing processed devices. (175X)

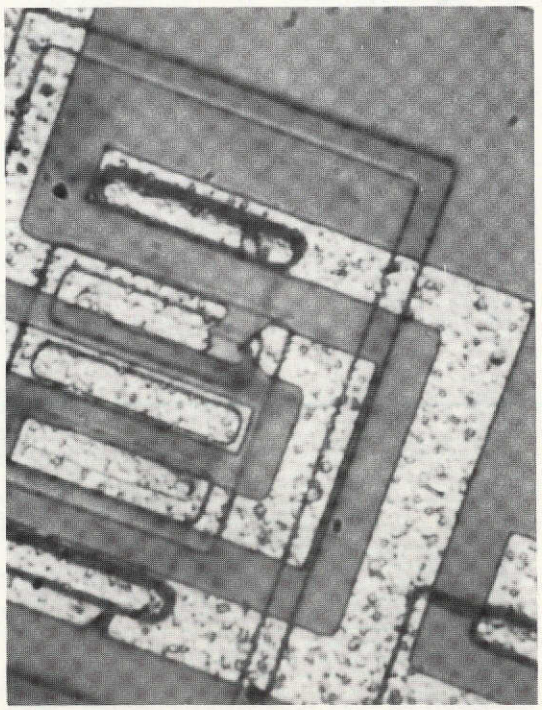

Figure 12: Open metal over an oxide step due to poor metal adhesion or failure of the photoresist. (425X)

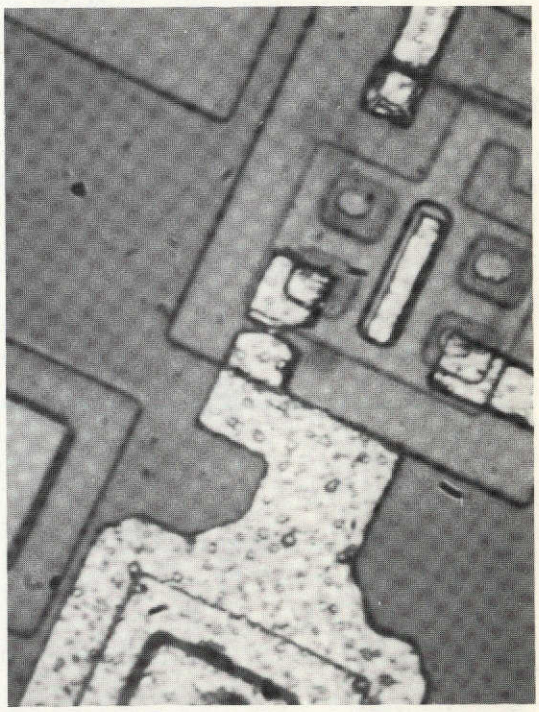

Figure 13: A narrow metalization path due to undercutting during the metal removal etch. (425X)

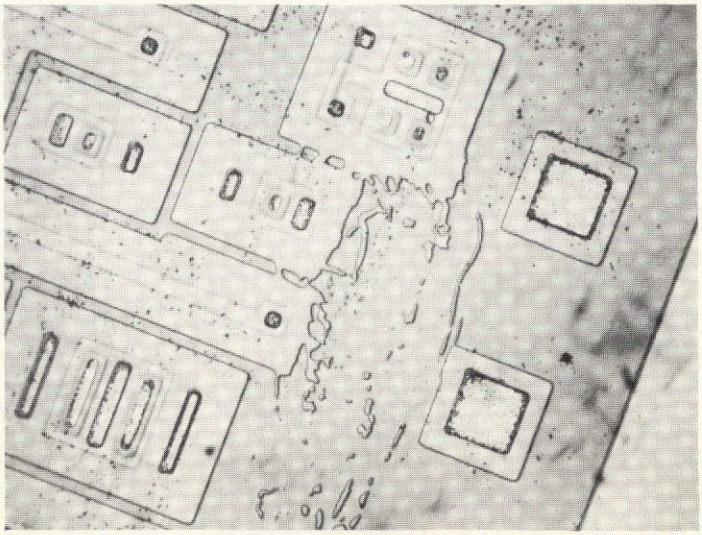

Figure 14: Conductive paths between normally isolated regions probably due to some type of mask defect. (175X)