AU8-26193 FR 1

ELECTRICAL

ENGINEERING

[redacted]

[redacted]

ENGINEERING EXPERIMENT STATION

AUBURN UNIVERSITY

AUBURN, ALABAMA

A DIGITAL MIXER

Prepared by

ELECTRONICS RESEARCH LABORATORY

M. A. HONNELL, PROJECT LEADER

FINAL REPORT
PART II

September, 1974

CONTRACT NAS8-26193
GEORGE C. MARSHALL SPACE FLIGHT CENTER
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
HUNTSVILLE, ALABAMA

(NASA-CR-120585) A DIGITAL MIXER, PART 2 Final Report (Auburn Univ.) 36 p HC $3.75 CSCL 09E N75-16750

Unclas
G3/33 09940

APPROVED BY:

J. D. Irwin, Head
Electrical Engineering

SUBMITTED BY:

M. A. Honnell, Professor
Electrical Engineering

FOREWORD

This report is a technical summary presenting the results of a study by the Electrical Engineering Department, Auburn University, under the auspices of the Engineering Experiment Station toward fulfillment of the requirements of NASA Contract NAS8-26193. The report describes studies made concerning "Frequency Stabilization and Modulation Techniques for High Frequency and High Data Rate Telecommunication".

Part II of the report presented herein describes a digital mixing technique investigated for its possible application in digital telemetry systems. Part I of the report presented under separate cover describes a stable, linear frequency modulated oscillator with dc response designed to accept analog, digital or television signals.

ABSTRACT

This report describes an experimental study made to determine the characteristic response of D flip-flop digital logic units used as mixing devices for telemetry applications. The study indicated that the D flip-flop performs the mixing operation under a variety of input frequency conditions. The output signal is a rectangular wave whose long term average frequency is the desired difference frequency. The output signal contains frequency jitter which is a function of the relationship between the two input frequencies. The seriousness of the jitter depends on the application desired.

TABLE OF CONTENTS

LIST OF FIGURES

A DIGITAL MIXER

W. P. Albritton

I. INTRODUCTION

A study was carried out to determine the salient characteristics of D flip-flop digital logic units used as a mixing device. Since, at this stage, only preliminary information was desired, the effort was confined to a case oriented hardware study rather than to an elaborate mathematical treatment.

II. THE DIGITAL MIXER

The device used as a mixer was the Fairchild TTL/SSI 7474 dual D flip-flop. The dip pack used showing pin locations and function identification is shown in Figure 1.

Clock triggering of data on D input for the 7474 occurs on the positive edge of the incoming clock pulse. Typical supply voltage and logic level voltage is +5V. Typical clock frequency is 25 MHz. For these experiments the clock frequency is restricted to the range of 1 to 20 kHz.

The output frequency, f_Q, is a function of the input frequencies on the D input line and the clock input line. The D input frequency, f_D, should be greater than the clock input frequency, f_C, in order to obtain useful frequency difference information at the output. Figure 2 indicates the required frequency input relationships. Note that the useful range, for the differencing operation of the output frequency, f_Q, is from zero to 1/2 f_C.

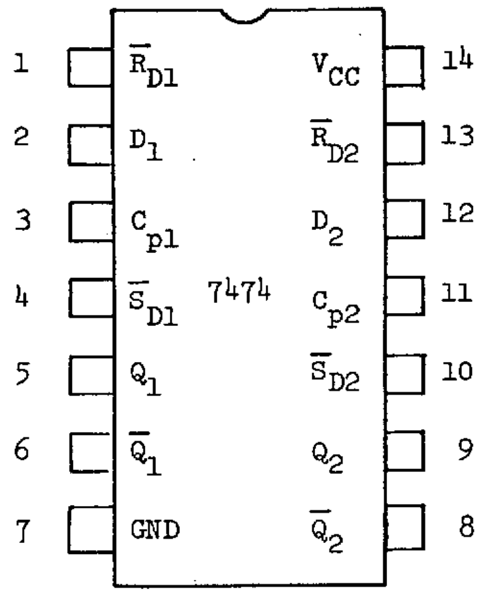


Figure 1 Pin connections of the Fairchild TTL/SSI 7474 dual D flip-flop.

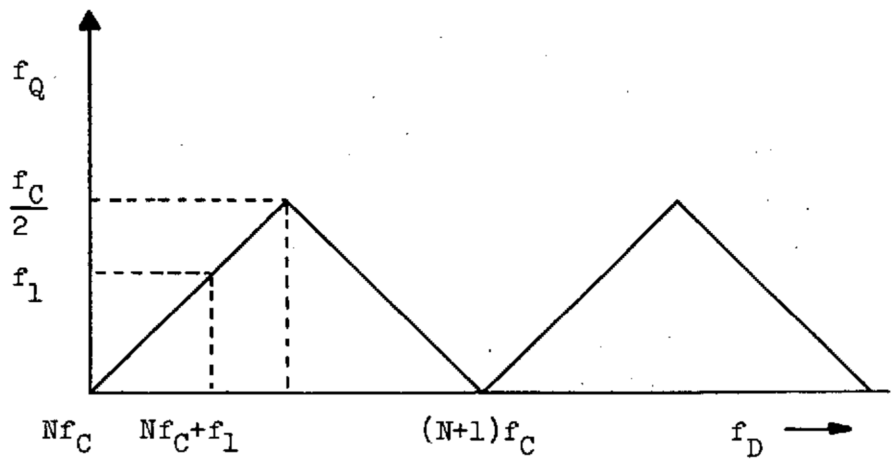


Figure 2 The required frequency relationships.

For

$$N = 1 \qquad f_D = f_C + f_1$$

$$f_D - f_C = f_Q \leq 1/2\ f_C$$

$$f_C + f_1 - f_C = f_1 \qquad \therefore f_1 \leq 1/2\ f_C$$

There are many combinations of input frequencies which can be applied to the input lines. An examination of the stability and period characteristics of f_Q is carried out by making case studies. Also, a correlation is suspected between the stability of f_Q in frequency and the relationship between f_D and f_C.

To obtain the different frequencies to apply to the inputs of the mixer, a TTL/MSI 7490 decade counter is used to count down a reference clock.

Case 1: Let f_D/f_C be a rational number and f_{CL} be the reference clock frequency. If $f_D = f_{CL}/8$ and $f_C = f_{CL}/10$ then $f_D/f_C = 1.25$. Figure 3 shows the connections for this case.

The divide by 10 function is obtained by connecting the 7490 as shown in Figure 4. The output of this device is labeled f_C in Figure 5(a). The 7490 is a negative-edge-triggered device.

The divide by 8 function was obtained using two 7474 dual D flip-flops employing both flip-flops of the first chip and one of the second. The connections are shown in Figure 6.

The divide by 8 and divide by 10 are shown relative to the clock in Figure 5(a). The output f_Q is shown relative to f_D and f_C in Figure 5(b). Calculations describing Figure 5(b) are shown below.

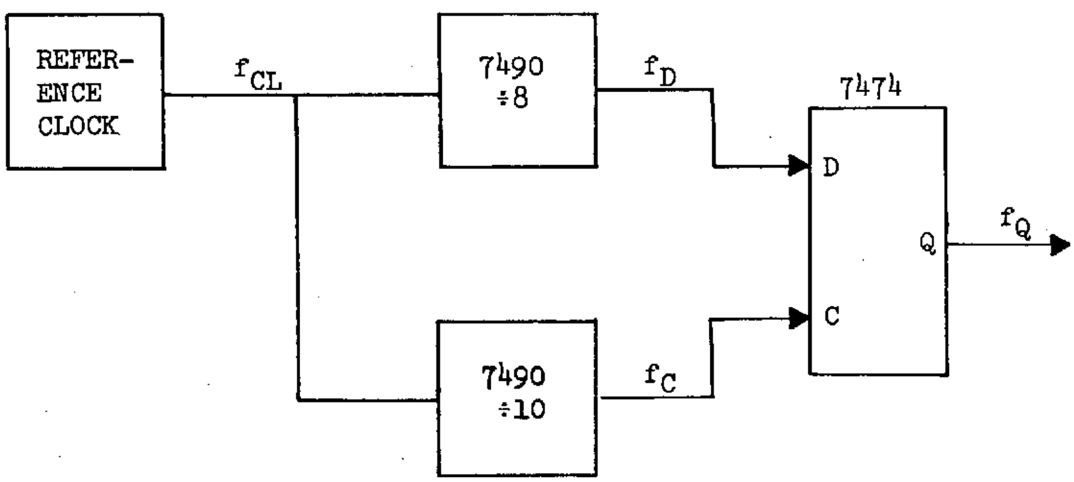


Figure 3 Test circuit for Case 1.

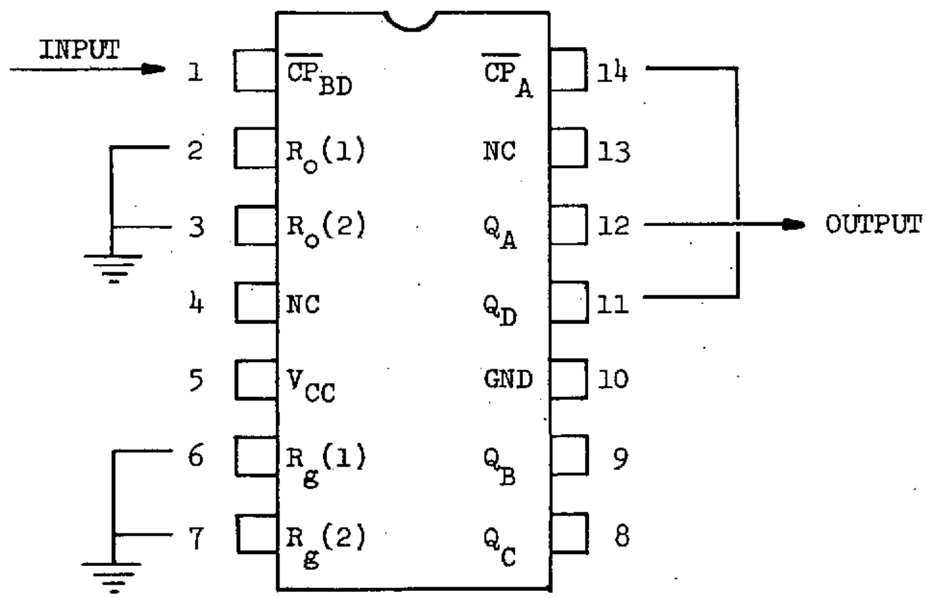


Figure 4 The TTL/MSI 7490 decade counter connections for divide by 10 mode.

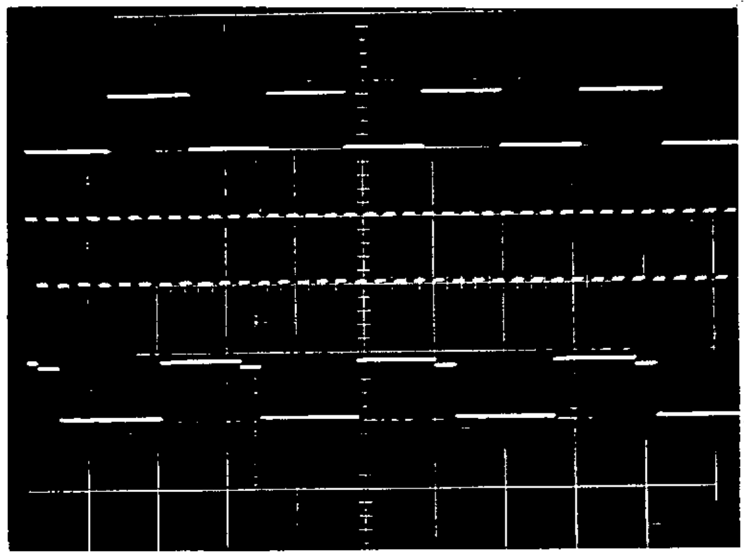


Figure 5(a) Divide by 8 and 10 waveforms.

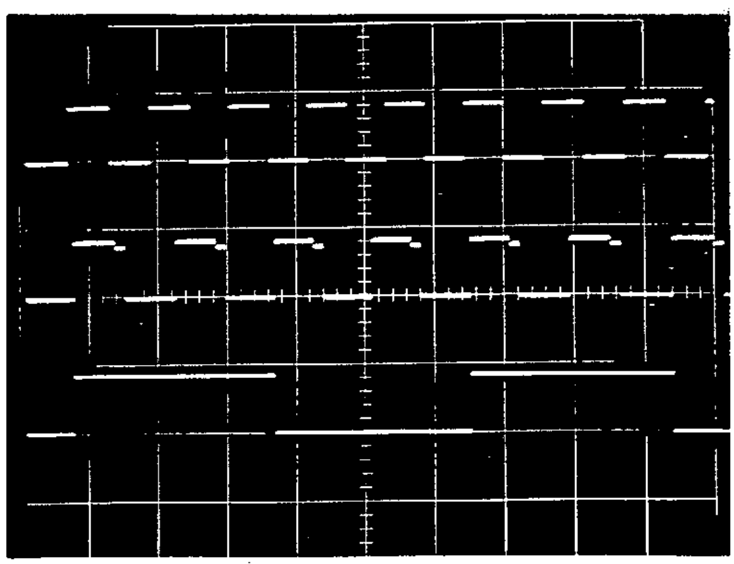
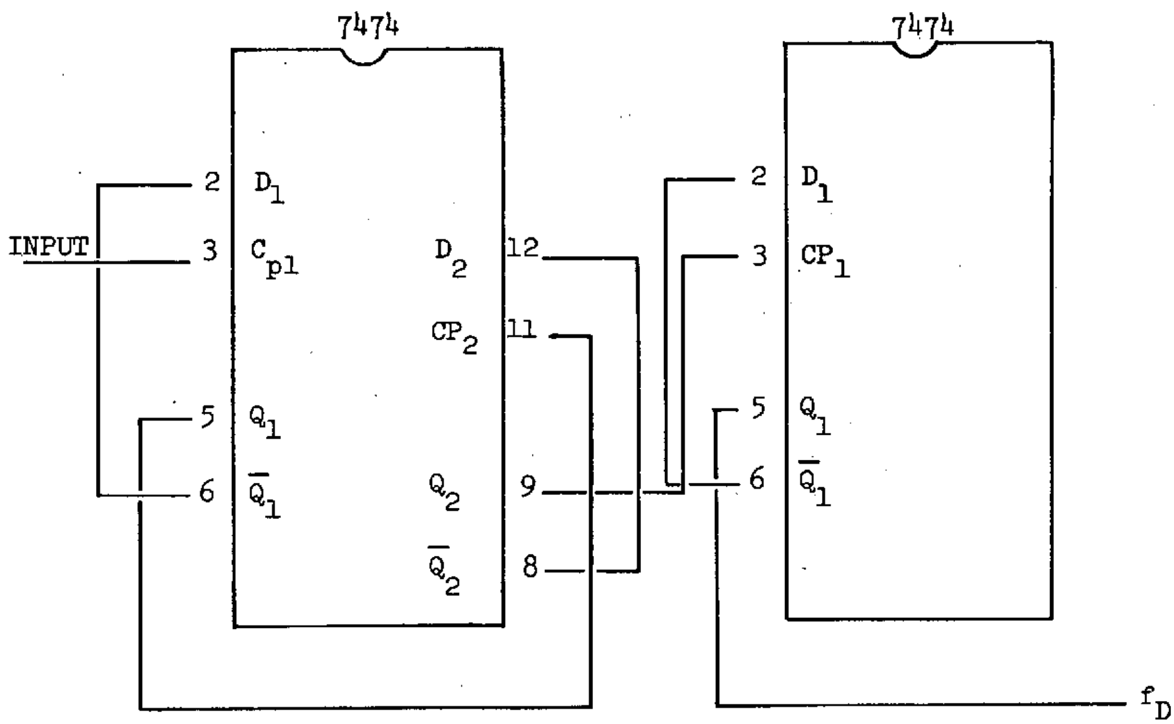


Figure 5(b) Output wave form of f_Q relative to f_C and f_D.



Note: Pins 1 and 14 should be connected to assure high on pin 1 even though TTL voltage level goes high when unconnected.

Figure 6 Two 7474 flip-flops connected to provide divide by 8, 4 and 2 functions.

$$f_D = f_{CL}/8 = 10f_C/8 = 1.25f_C$$

$$f_C = f_{CL}/10$$

$$f_Q = f_D - f_C = 1.25f_C - f_C = .25f_C$$

$$T_Q = 1/f_Q = 1/.25f_C = 4T_C$$

Notice that T_Q is equal to $4T_C$ in Figure 5(b).

Case 2: $f_D/f_C = (f_{CL}/9)/(f_{CL}/10) = 1.111 \cdots$.

The divide by 10 connections shown in Figure 4 using the 7490 are used in this case as the f_C input to the mixer.

The divide by 9 function is achieved with the 7490 by connecting pins 11 and 12 to reset pins 2 and 3. Notice the BCD count sequence in Figure 7(a). The rest of the connections are shown in Figure 8.

When Q_D and Q_A go high on the ninth count, the counter is reset and the nine count is resumed.

The circuit under test is shown in Figure 9. In Figure 10(a), the two input frequencies are shown relative to the reference clock. In Figure 10(b), the two input frequencies are also shown along with f_Q, the output of the mixer.

The following calculations describe the pictures of Figure 10.

$$f_D = f_{CL}/9 = 10f_C/9 = 1.111\cdots f_C$$

$$f_C = f_{CL}/10$$

$$f_Q = f_D - f_C = 1.111\cdots f_C - f_C = .111\cdots f_C$$

$$T_Q = 1/f_Q = 1/(.111\cdots f_C) = 9.\overline{009}\ T_C$$

Notice T_Q is approximately $9T_C$.

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Figure 7(a). Count Sequence of Decade Counter.

				OUTPUT			
$R_0(1)$	$R_0(2)$	$R_9(1)$	$R_9(2)$	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

Figure 7(b). Reset Truth Table.

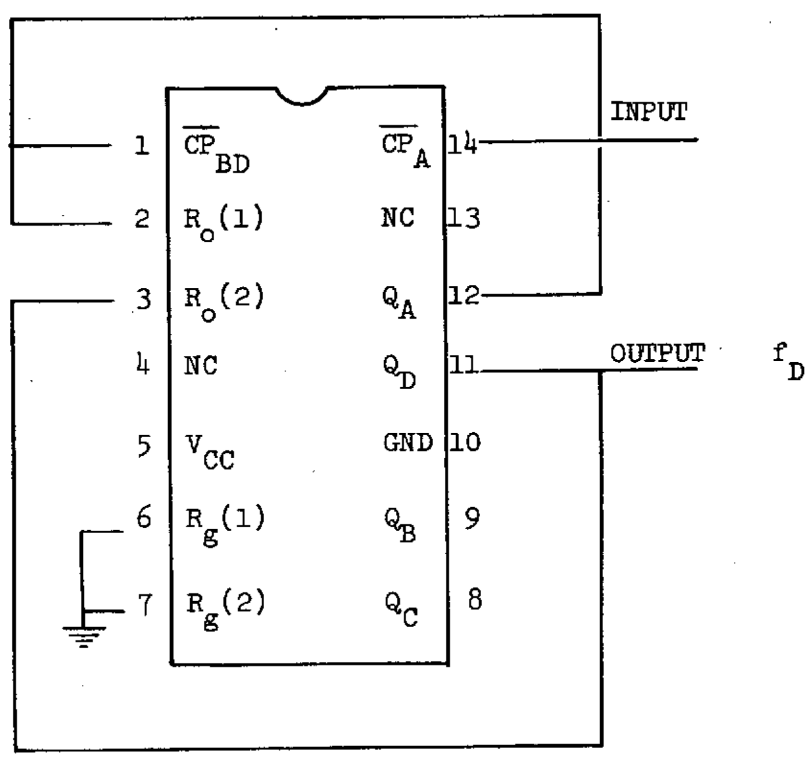


Figure 8 Connections for a divide by 9 mode.

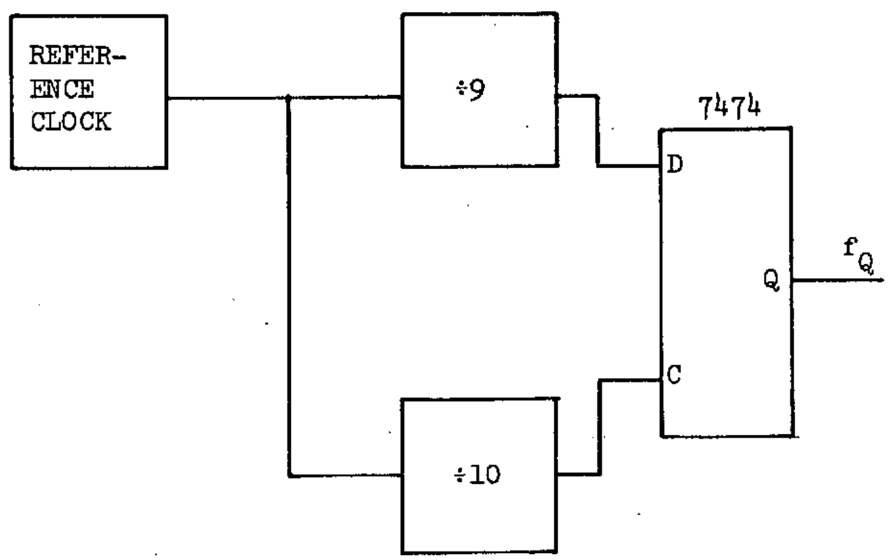


Figure 9 The circuit for Case 2.

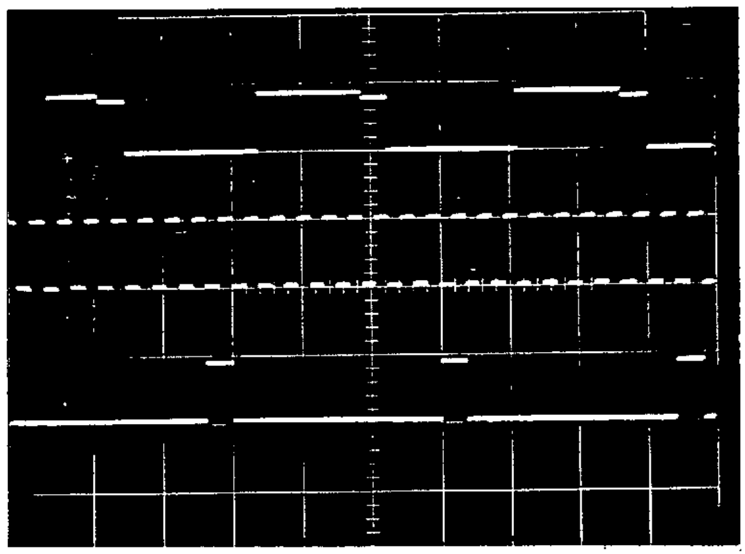


Figure 10(a) The divide by 9 wave forms showing the two input frequencies relative to the reference clock frequency.

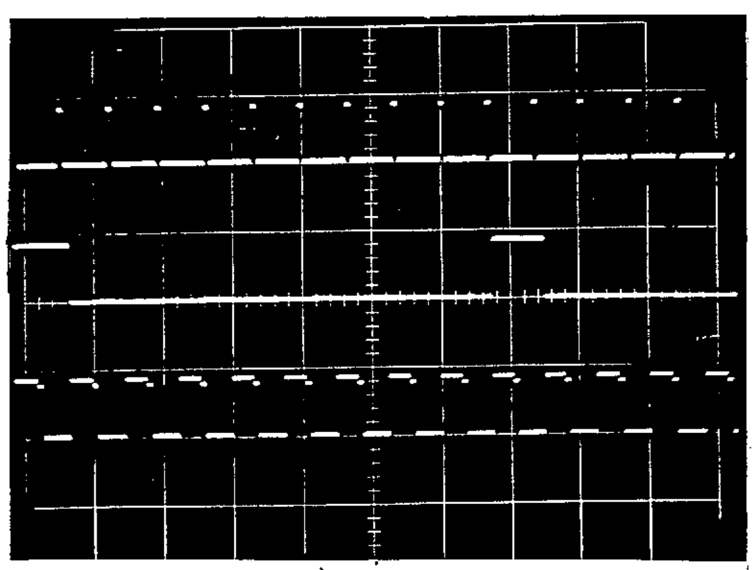


Figure 10(b) Output f_Q relative to f_C and f_D.

Case 3: $f_D/f_C = (f_{CL}/3)/(f_{CL}/4) = 1.333\cdots$.

To obtain a divide by three, the 7490 decade counter was used. The reset pins 2 and 3 were connected to pins 9 and 12 as shown in Figure 11. Observe in Figure 7(a) the logic levels of Q_B and Q_A on the third count. On the third count the reset pins go high and reset the counter, and the three count is resumed.

The divide by four function is obtained by using two D flip-flops as shown in Figure 6. The third D flip-flop is not used and a divide by four output is taken from pin 9. The connections for this case are shown in Figure 12. f_D, f_C, f_{CL} and f_Q are shown in Figure 13(a) and (b). Calculations describing the events in Figure 13(b) are as follows

$$f_D = f_{CL}/3 = 4f_C/3 = 1.333\cdots f_C$$

$$f_C = f_{CL}/4$$

$$f_Q = f_D - f_C = 1.333\cdots f_C - f_C = .333\cdots f_C$$

$T = 1/f_Q = 3T_C$ Notice in Figure 13(b) that

T_Q is $= 3T_C$

Case 4: $f_D/f_C = (f_{CL}/7)/(f_{CL}/9): = 1.2857142$. The divide by 9 connections are shown in Figure 8.

In Figure 7(a) notice the Q_B and Q_A columns on count 6 and 7. The diode is attached between pins 9 and 12, Q_B and Q_A respectively. Then pin 9 is connected to pin 2 (reset). The Q_C output on pin 8 is connected to the other reset, pin 3. Notice that during the sixth count the diode holds Q_B low, so there is no reset. On the seventh count Q_C, Q_B and Q_A are high so there is a reset condition and the seven count is established.

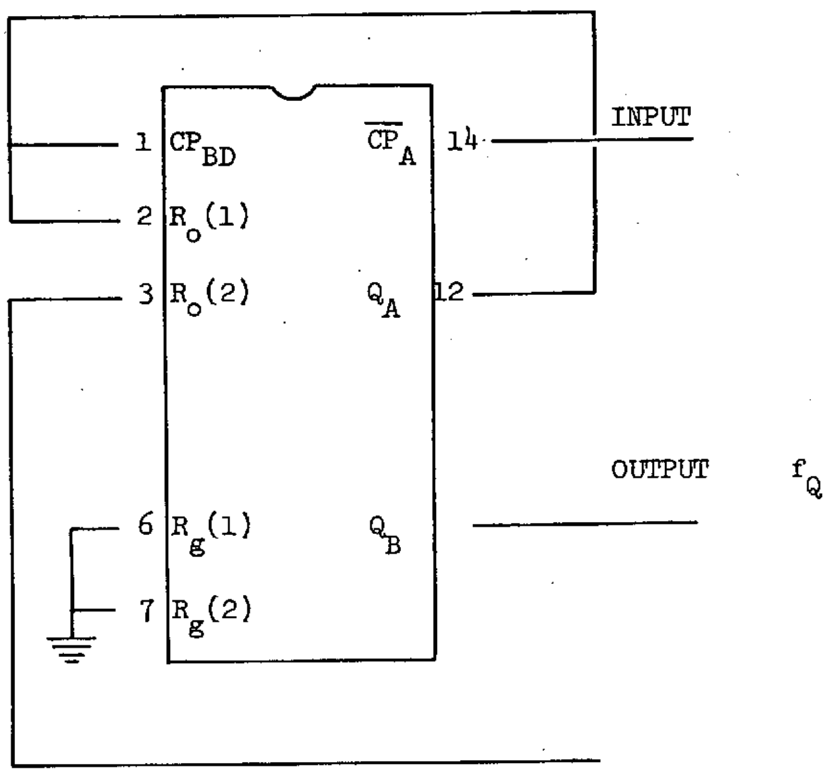


Figure 11 Connections of the 7490 for divide by 3 mode.

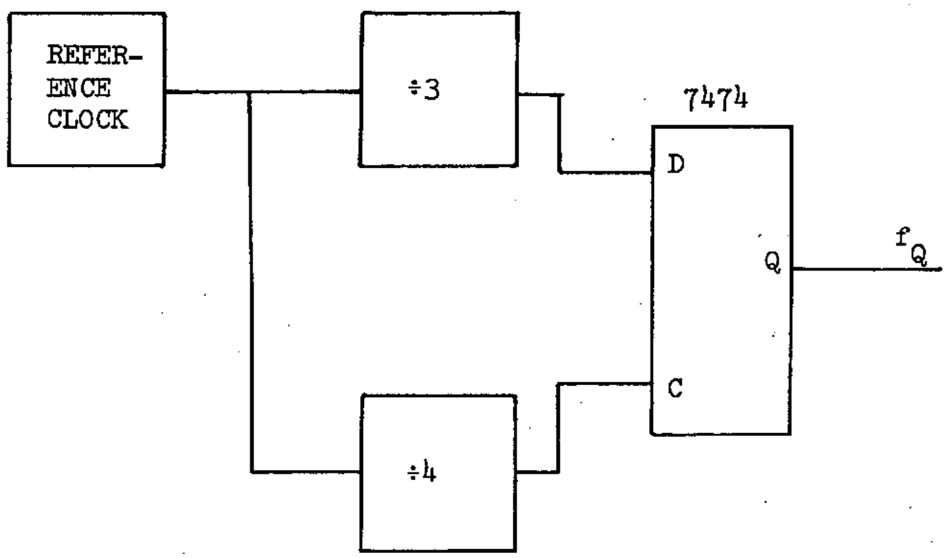


Figure 12 Test circuit for Case 3.

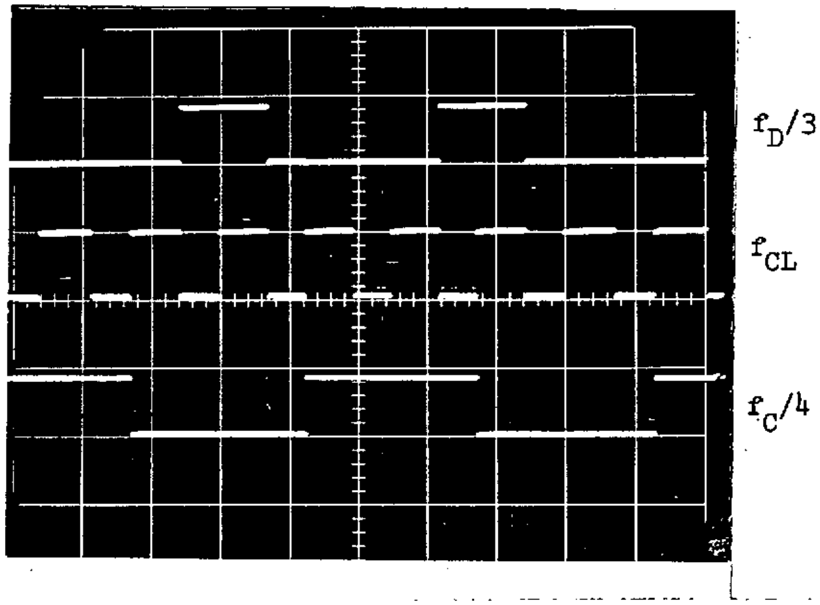


Figure 13(a) Divide by 3 and divide by 4 waveforms.

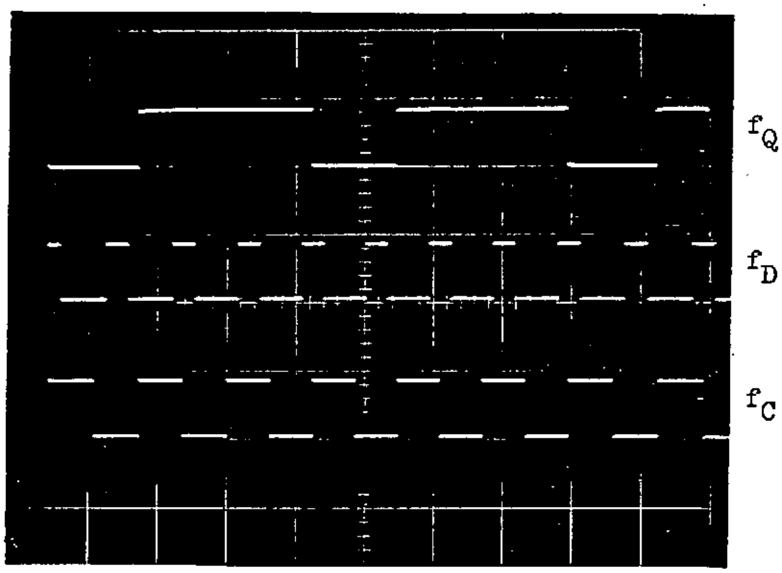


Figure 13(b) Output f_Q relative to f_C and f_D.

The Divide by 7 connections are shown in Figure 14. The overall circuit connections are shown in Figure 15.

The inputs and output are shown in Figure 16(a) and (b). Notice the two quasi periods of f_Q, T_1 and T_2, that when averaged equals the T_Q calculated in the following equations

$$f_D = f_{CL}/7 = 9f_C/7 = 1.2857142f_C$$

$$f_C = f_{CL}/9$$

$$f_Q = f_D - f_C = 1.2857142 - f_C = .2857142f_C$$

$$T_Q = 1/f_Q = 1/.2857142f_C = 3.50000T_C$$

$$T_1 = 3T_C \; ; \quad T_2 = 4T_C$$

$$T_Q = 7T_C/2 = 3.5T_C$$

Case 5: $f_D/f_C = (f_{CL}/7)/(f_{CL}/10) = 1.4285714$: The divide by 10 function is achieved with the connections shown in Figure 4. The divide by 7 is shown in Figure 14. The overall circuit is shown in Figure 17. Refer to Figure 18(a) and (b) for the inputs and output of the mixer.

The calculations necessary to describe the pictures are as follows.

$$f_D = f_{CL}/7 = 10f_C/7 = 1.4285714f_C$$

$$f_C = f_{CL}/10$$

$$f_Q = f_D - f_C = 1.4285714f_C - f_C = .4285714f_C$$

$$T_Q = 1/f_Q = 1/.4285714 = 2.3333\cdots T_C$$

In Figure 18(b), notice that T_1, T_2, and T_3, when averaged, equals the predicted period T_Q relative to T_C.

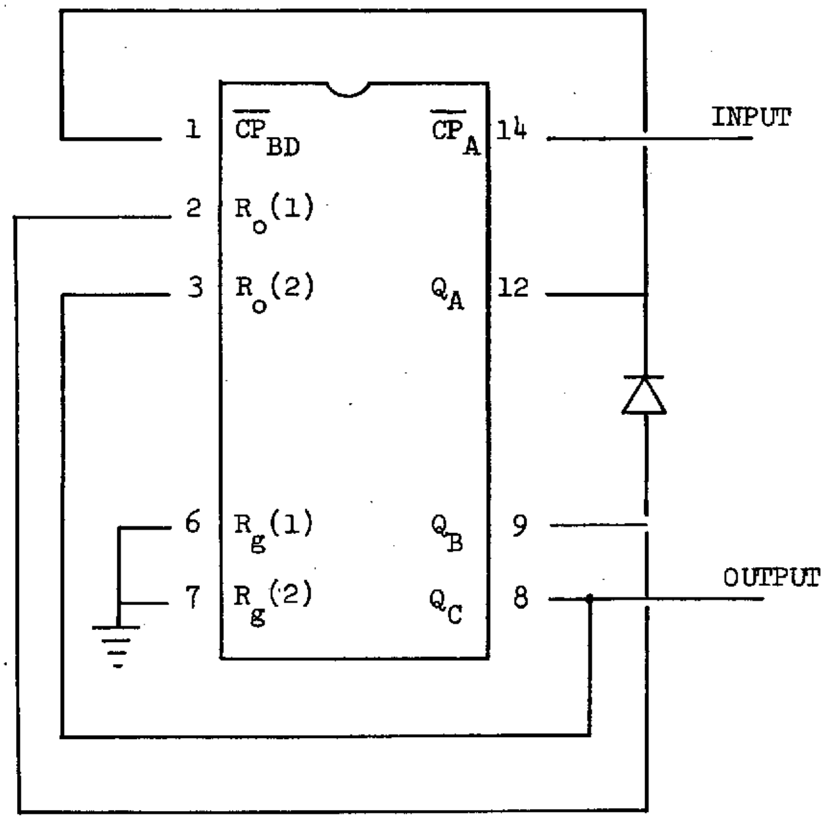


Figure 14 The 7490 connections for divide by 7 mode.

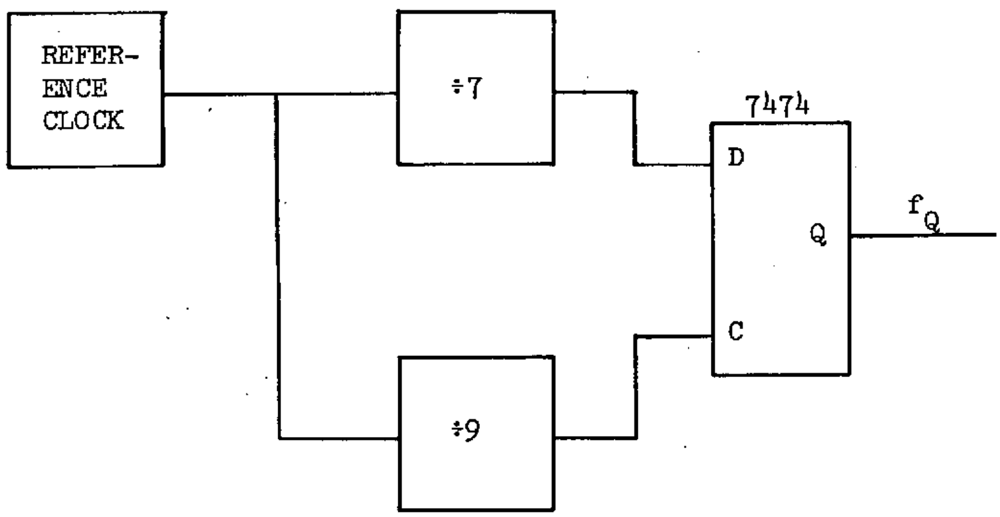


Figure 15 Test circuit for Case 4.

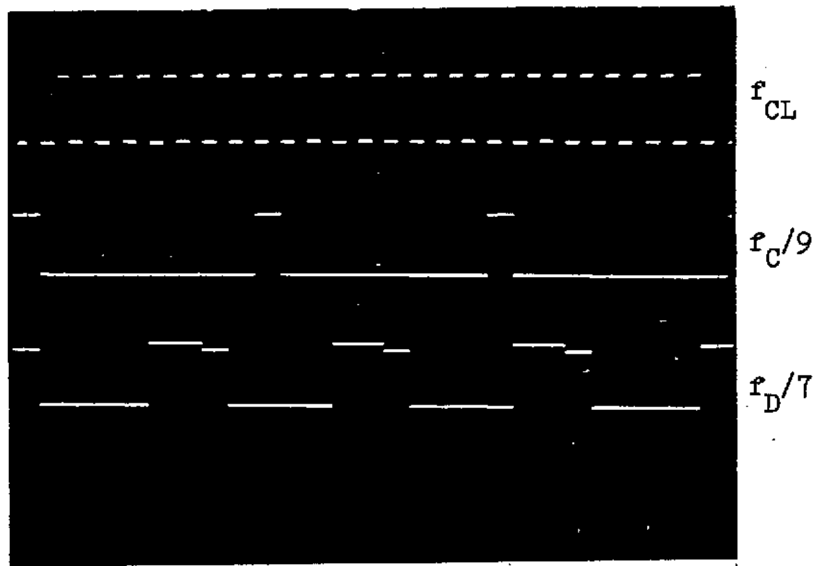


Figure 16(a) Divide by 7 and divide by 9 waveforms.

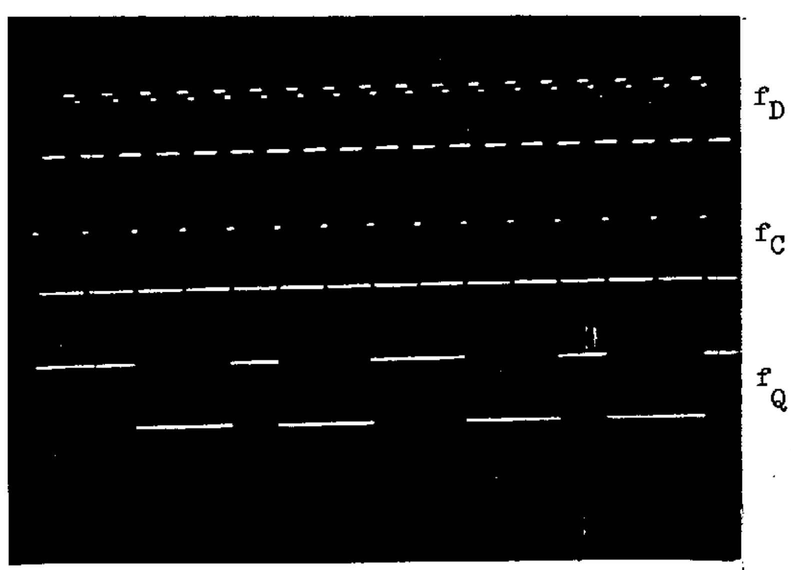


Figure 16(b) Output f_Q relative to f_C and f_D.

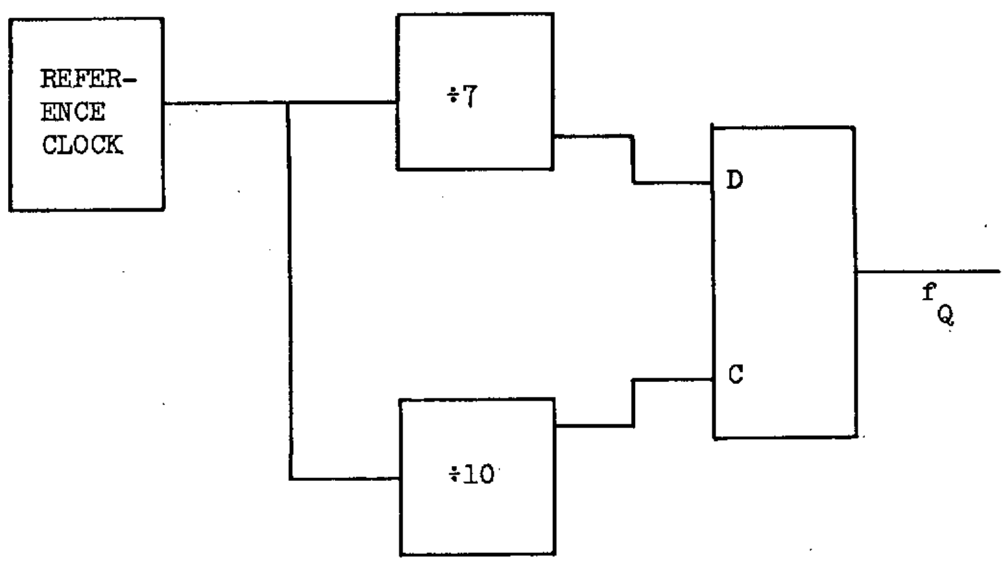


Figure 17 Test circuit for Case 5.

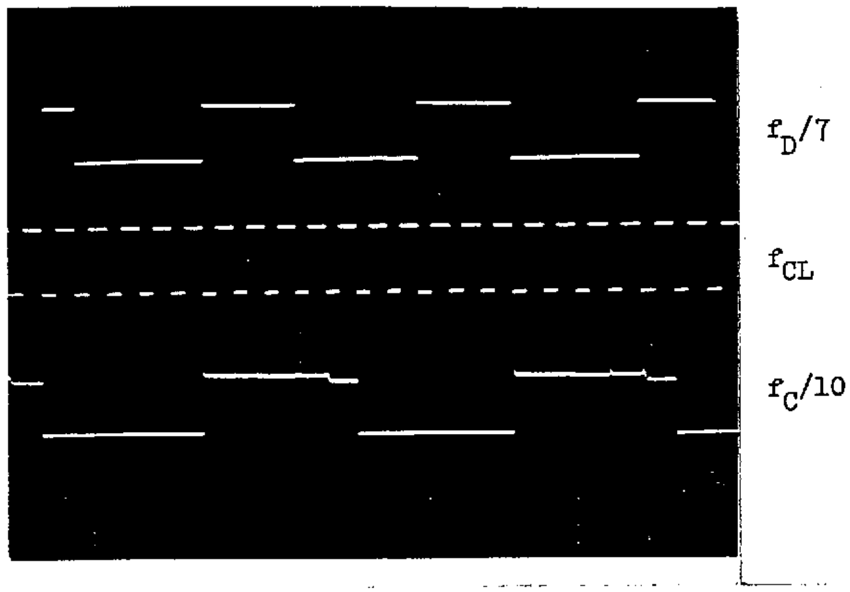


Figure 18(a) Divide by 7 and divide by 10 waveforms relative to clock waveforms.

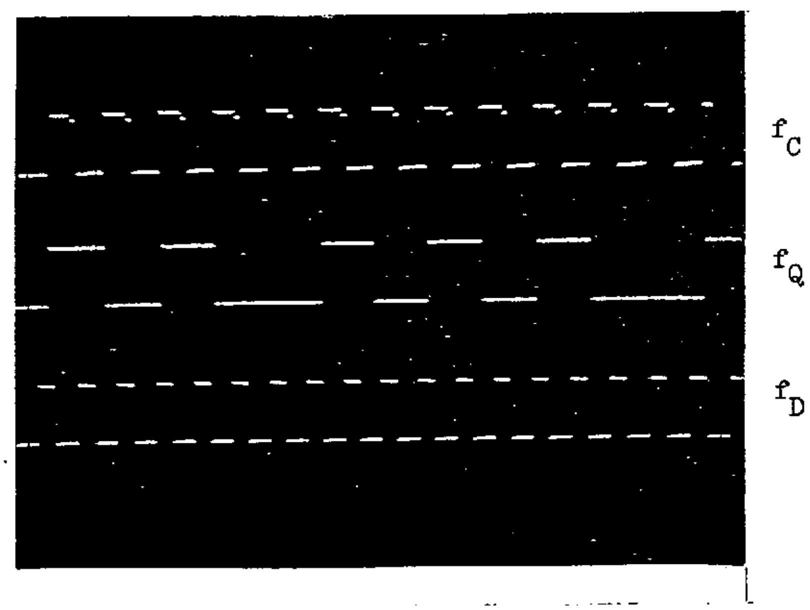


Figure 18(b) Output f_Q relative to f_C and f_D.

It was of interest to know how much of the spectral content of the output waveform was at frequency f_Q relative to the other components. A calculation of the Fourier series amplitudes yields the desired information. The Fourier analysis is performed on the inverted output of f_Q which is $f_{\bar{Q}}$. See Figure 19 for the waveform and Figure 20 for the frequency spectrum.

$$A_o = \frac{2}{T_o} \int_{\frac{-6T_o}{14}}^{\frac{-4T_o}{14}} V(t)dt + \frac{2}{T_o} \int_{-T_o/7}^{0} V(t)dt$$

$$A_o = \frac{4V}{7}$$

$$A_N = \frac{4}{T_o} V \int_{\frac{-6T_o}{14}}^{\frac{-4T_o}{14}} \cos\left(2\pi N f_o t\right)dt + \frac{4V}{T_o} \int_{-T_o/7}^{0} \cos\left(2\pi N f_o t\right)dt$$

$$A_N = \frac{2V}{\pi N}\left[\sin\frac{-4N\pi}{7} - \sin\frac{-6N\pi}{7} - \sin\frac{-2N\pi}{7}\right]$$

$$V_1 = \frac{.231(V)}{\pi} \qquad V_6 = \frac{-.04(V)}{\pi}$$

$$V_2 = \frac{.307(V)}{\pi} \qquad V_7 = 0$$

$$V_3 = \frac{.724(V)}{\pi} \qquad V_8 = \frac{.03(V)}{\pi}$$

$$V_4 = \frac{-.55(V)}{\pi} \qquad V_9 = \frac{.07(V)}{\pi}$$

$$V_5 = \frac{-.126(V)}{\pi} \qquad V_{10} = \frac{.2189(V)}{\pi}$$

$$V_{11} = \frac{-.2(V)}{\pi}$$

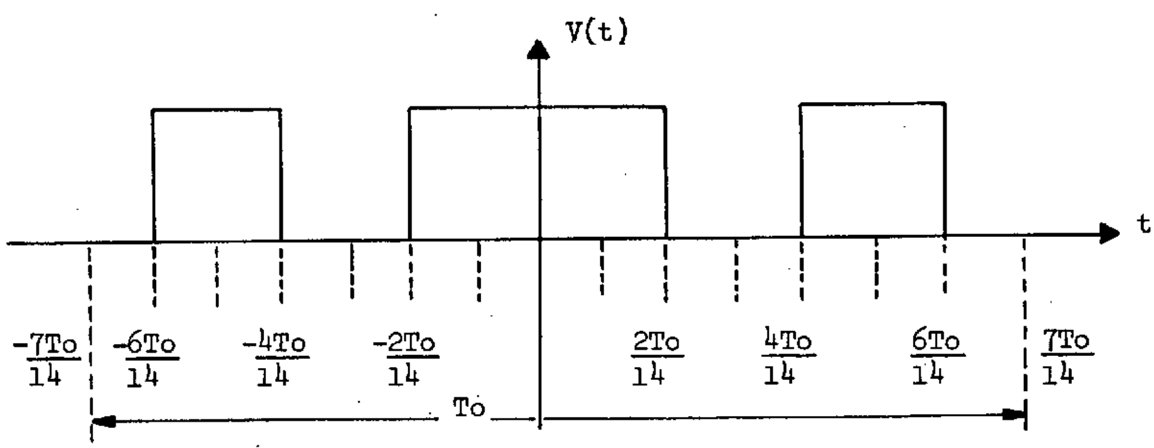


Figure 19 One period T_0 of the inverted output of f_Q.

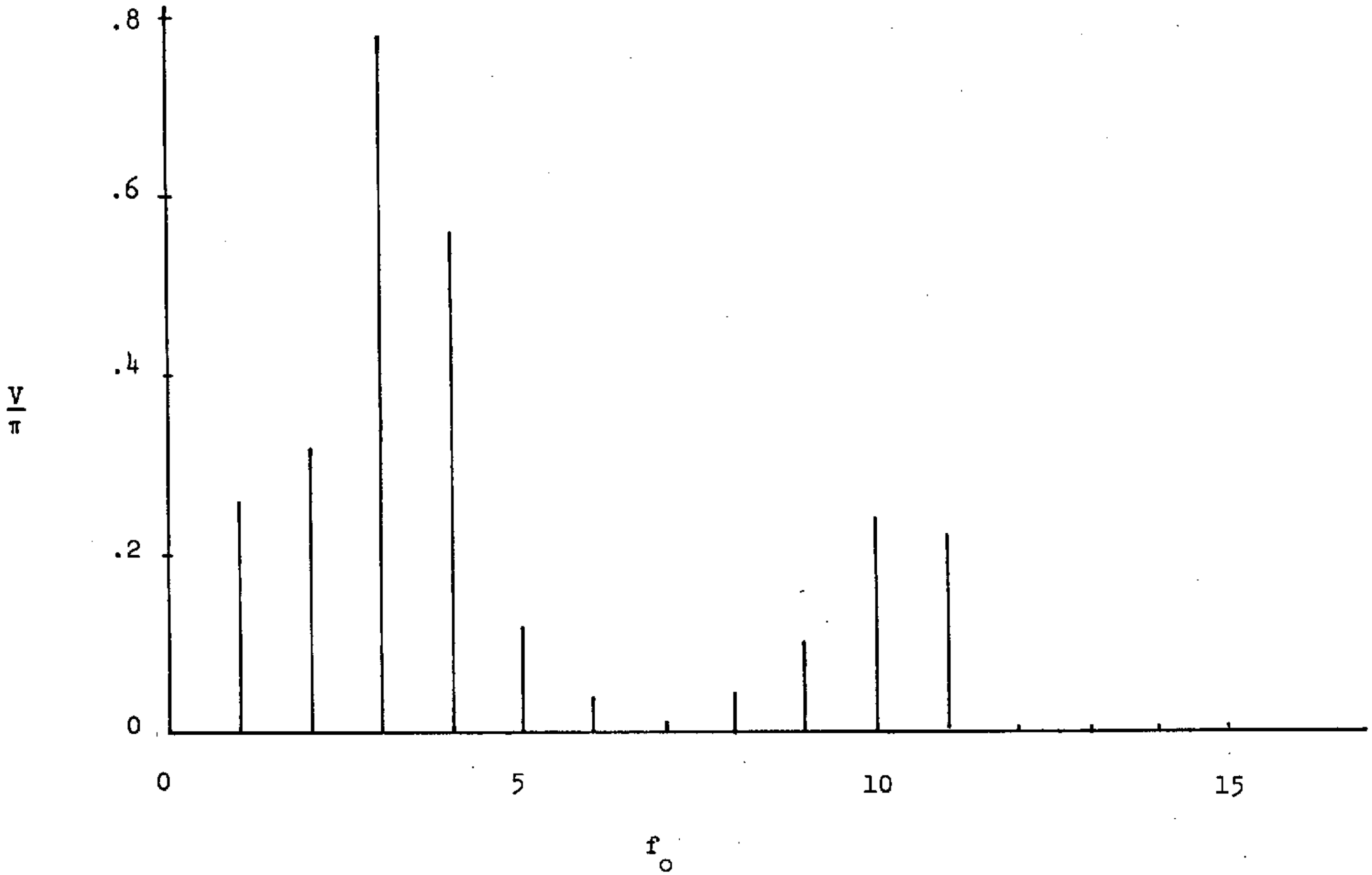


Figure 20 Calculated frequency spectrum of the waveform of V(t) in Figure 19.

Case 6: Using two independent pulse generators for inputs f_D and f_C, with f_D being greater than f_C.

In the synchronous case the overall period was found by averaging the quasi periods. The output of the mixer was predictable due to the fact that the input frequencies were synchronized with a common clock.

When two inputs to the mixer have no direct relation to a common clock, or to each other, the output frequency of the mixer is unpredictable. The independent phase relations are continuously drifting in relation to each other mainly because of the frequency instability in each generator. Since the mixer is purely combinational logic, its output is a direct function of its inputs. So the output frequency shifts according to the phase relation at the input.

The spectral analysis of the output would have a major component at the correct frequency as predicted by $f_D - f_C$, but this would move on the frequency axis in relation to f_D and f_C.

On an oscilloscope the changes in frequency on the mixer output are observed as time jitter in the low-to-high and high-to-low transitions. See Figure 21.

III. CONCLUSIONS

The case studies outlined above indicated that the D flip-flop does perform the mixing operation under a variety of input frequency conditions. The output signal, however, is not a square wave at the desired difference frequency. It is, rather, a rectangular wave whose long term average frequency <u>is</u> the desired difference frequency.

What this means is that the output contains frequency jitter. The amount of jitter and the spectral properties of the jitter will be a

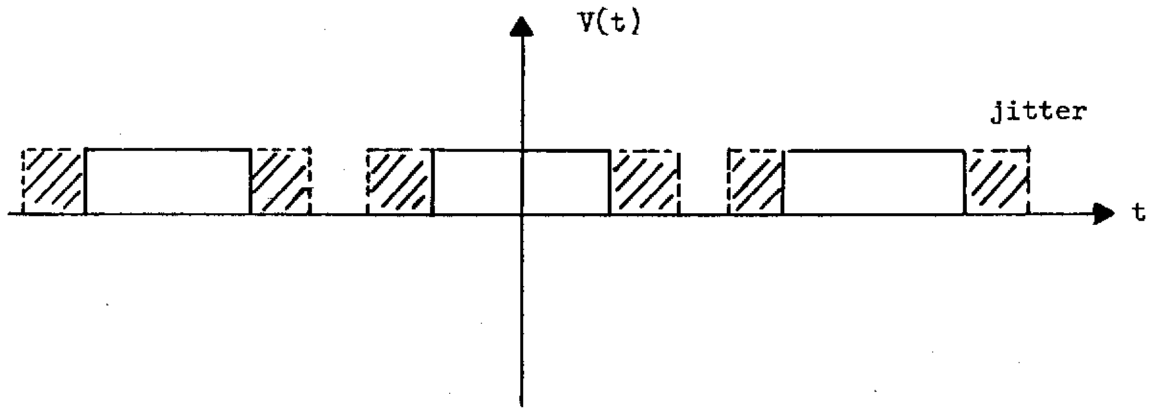


Figure 21 Jitter as seen in the time domain.

function of the relationship between the two input frequencies.

For a fixed relationship between the two input frequencies the jitter should be a deterministic quantity, describable in terms of the deterministic inputs. A possible exception to this would be a case where the ratio of the two input frequencies was an irrational number.

For a random relationship between input frequencies, such as would be the case when one input frequency contained signal information, the jitter would be random. It would therefore have to be described in statistical terms.

The effect of the jitter produced by the mixing operation would depend on the application. In a phase-locked loop, with the usual low-pass filter following the phase detector, the jitter might be a surmountable problem. That might require, however, an unduly long time-constant in the low-pass filter with attendant loss in loop response speed.

Each different application would present its own special set of difficulties.

It is clear that a D flip-flop mixer would be an additional source of phase jitter which would not be present if other mixing techniques were employed. The seriousness of the added jitter would depend on the application at hand.