PROCESSOR ARCHITECTURES UTILIZING
MAGNETIC BUBBLE AND SEMI-CONDUCTOR MEMORIES

Interim Report

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Interim Report

The Design and Operation Manual of an Experimental Control Panel for a Low Cost Omega Navigational Receiver
FOREWORD

This report presents the detailed design equations and an operation manual for the man-machine interface to an experimental Omega Navigational Receiver. Included in the report are all circuit diagrams, system-interface connections, software flow charts, and software listings.
1.0 Introduction

To aid work being conducted at the Langley Research Center on the feasibility of a low cost Omega Navigational Receiver, a control panel was designed and constructed according to supplied specifications. Since the proposed Omega Receiver is designed around a microprocessor, software engineering necessary for control panel operation is also included in the design. The control panel is to be used as an operational model for use in the design of a prototype receiver.

The first part of this report provides a detailed description of the hardware design followed by a description of the software needed to operate the panel. The second part is a complete description of the operating procedures for the panel.
2.0 **Control Panel Design**

2.1 **Specifications**

The block diagram of the control panel is shown in Fig. 1. The following design specifications were used for the panel:

1. The control panel has two modes of operation: data entry (or change) and data display.
2. In the data entry mode, the operator may select one of eight parameters and input data regarding that parameter.
3. In the data display mode, the operator may display any one of eight input parameters or any one of eight calculated values.
4. The operator may change any input parameter at any time.
5. Certain indicators will be provided.

Most of these specifications involved both hardware and software considerations.

2.2 **Hardware Implementation**

The hardware problem was that of interfacing an INTEL 4004 4-bit microprocessor using a SIM-4 board to the receiver control panel. Some interface logic had been previously incorporated in the receiver such that the following input/output organization was dictated for the front panel interface:

1. One 4-bit data input bus (positive-logic)
2. One 4-bit data output bus (positive-logic)
3. Single bit control lines (negative-logic)

Most of the control lines were such that only one could be activated at any given time. However, a few of the control lines could be activated independently.
Details of the elements in the front panel block diagram of Fig. 1 will be explained in the following sections. Included on the front panel but not shown in the block diagram are a "power on" switch and a variable signal threshold selector (potentiometer). The threshold selector circuitry is shown in Fig. 2.

It should be noted that the choice of a large majority of the hardware used was purely on the basis of availability due to a limited time schedule. Therefore, it may be prudent to replace some of the components for the prototype version.

2.2.1 Keyboard

Data entry was complicated by two constraints. The first constraint was the lack of interrupt capability in the INTEL 4004 microprocessor thereby forcing the computer to scan the keyboard, in some fashion, for a key closure. The second constraint was providing the capability to change the input parameters at any time. This meant that a parameter change could occur after the receiver had locked onto an Omega signal but keyboard scanning could occur only at given times. Also, not knowing how much time would be needed for calculations, it was not certain how much time would be available for the keyboard scan nor whether key closure could be easily detected.

Several schemes were investigated from a software key closure scan to a completely "buffered" keyboard. The software scan was a scheme in which the column of a keyboard matrix was enabled and the rows interrogated for a key closure. This scheme was abandoned because of the excessive computer time required since switch debouncing was done in software. The fully "buffered" keyboard scheme was one in
which the entire input parameter value would be held in flip-flop memory and the computer flagged only when this value was ready to be processed. This scheme required hardware to display and clear the characters, clock circuitry to shift the characters within the memory as new characters were entered, and a keyboard providing a coded output. This was abandoned due to excessive hardware cost.

The final design was a compromise of the above two schemes that incorporated the lower hardware cost of the first scheme and the minimum computer time of the second. The "semi-buffered" keyboard scheme allowed for storing one character until the computer could process it.

The circuit used is shown in Fig. 3. The keyboard, a Microswitch 12NW47-1, is a 4 x 3 coded keyboard with buttons for the digits 0-9, "enter", and "clear entry". The keyboard provides a negative-logic BCD code assignment and a delayed key closure strobe. When a button is depressed, the button code assignment is placed on the keyboard data lines and the strobe pulse, which is delayed for data line settling purposes, is generated. This strobe pulse sets a "data ready" flip flop (7472) which in turn activates a monostable multivibrator (74121). The multivibrator output is then used to load the keyboard data into a 4-bit latch, where it will remain until the computer can process it. The "data ready" flip flop (7472) will remain set until the computer generates a logic 1 on the "data ready reset" line. Until the "data ready" flip flop is reset, no new entry will be accepted and put into the data latch.

Information from the keyboard interface is entered into the computer via its 4-bit data input bus. The information is "wire-ored"
onto the bus by means of a tri-state device (80C97). The output of
the "data ready" flip flop (7472) is placed on the bit line of the
data bus by a logic on the "data ready enable" line, while the keyboard data is placed on the bus by a logic on the "keyboard data enable" line. It is assumed that both enable lines and the "data reset" line are logic "1" normally (positive logic).

It has been shown, therefore, that with this scheme the computer
has only to process keyboard information if a key has been depressed,
thereby greatly reducing the computer time needed. In addition, an entry will not be lost if the computer is not able to accept it at
time of entry.

2.2.2 Display

The display circuit, shown in Fig. 4, is common to many displays. The display consists of four digits using seven segment light-emitting-diodes (LED). Each digit is a Fairchild FND5 $\Phi$ LED and uses a Fairchild matching seven-segment driver (9368) in order to eliminate the need for current-matching resistors. The LED drivers include both a 4-bit latch and a BCD-to-seven segment decoder. This allows the display data to be put on the computer's data output bus and loaded into the correct display digit latch using a control line from the computer. The decoder/driver also includes the ripple blanking capability which was used for the display. The display control lines were normally at logic level "1" while a logic "$\Phi$" enables the corresponding digit latch.

2.2.3 Data Selector Circuit

The data selector circuit allows the operator to select one of eight variables to be entered or displayed or one of eight results to be displayed. Since the number of result values equals the number
of input variables, the circuit is designed so that each position of the data selector will indicate either an input variable or a result value. Which of these two parameters is chosen is determined by a mode switch.

The data selector circuit is shown in Fig. 5. The data selector is a double-pole, non-shorting, eleven position rotary switch of which only eight positions are used. A 5 volt, 60 milliampere incandescent lamp, used to indicate switch position, is connected to each of the eight positions used on one pole (wafer) of the switch. The contacts of the eight positions on the other pole (wafer) of the switch are connected to the eight least significant output lines of a four-line-to-sixteen-line decoder (7442). The wiper of this pole is connected to the computer data input bus via a tri-state device (80C97). The inputs of the decoder (7442) are connected to the output data bus of the computer. The rotary switch position information is obtained by placing a BCD number between zero and eight on the output data bus. This will cause one of the outputs of the decoder (which are normally at logic "1") to obtain a logic "0". If the wiper of the rotary switch is on that decoder output, the logic "0" is placed on the input bus. The computer varies the value on the output data bus until a logic "0" is detected on data line φ of the input bus which indicates the switch position has been found. The value on the output bus is used as an indication of the actual switch position. A pull-up resistor (R4) is necessary on the rotary switch wiper to maintain a logic "1" while the switch is between positions.

The data mode switch is a double-pole, double-throw, center-off toggle switch. It is used to indicate one of three modes; data entry,
entry data display, and result data display. This switch provides a code to be placed on lines 1 and 2 of the data input bus from which the computer can determine the correct mode of operation. The switch also activates a red incandescent lamp, labeled "data in", when in the data entry mode. All of the data selector circuit information is placed on the computer's data input bus by a logic "4" on the "rotary switch enable" line. The codes for the data selector positions and mode switch positions are given in Fig. 6.

2.2.4 Indicator Circuits

Several computer controlled indicator lamps are provided on the front panel. These lamps include indications for distance to destination less than five miles, signal sync detection, and arrows for track deviations. The circuits for these indicators are shown in Fig. 7. The indicators are 5 volt, 60 milliampere incandescent lamps driven by DTL (diode-transistor logic) open-collector power gates (858). These particular power gates were necessary because of current requirements of the lamps. The two input nand gates (7400), used as inverters, enable a logic "4" from the computer to activate the lamps.

2.3 Hardware Results

A picture of the experimental control panel is shown in Fig. 8. The dimensions of seven inches by ten inches were forced by the hardware used. It should again be noted that the criteria used for choosing the particular hardware was mainly availability. This fact did force the panel to be larger than necessary and can be reduced in size in the prototype version.

The positions of the components on the two printed circuit boards used are shown in Figs. 9 and 10. The dimensions of these printed
circuit boards are actual size in the figures. All interfacing to the front panel is done through a 36 pin connector. Fig. 11 gives these front panel pin connections.

2.4 Software Implementation

An overview of the Omega Receiver software requirements is shown in Fig. 12. The input/output pilot interface or front panel operation software is a completely self-contained subroutine package (except for two system subroutines) which requires no parameter transfer upon entry. The two subroutines which are not included in the software package operate the control lines used by both the pilot interface and the Omega data acquisition circuits. One of the subroutines, AENAB, produces a pulse output on a control line specified upon entry. The other subroutine, BENAB, produces a level output on a control line again specified upon entry. The front panel software package contains a main routine and nine subroutines. A detailed explanation of these programs follows.

The flow charts for the software package is found in Appendix A. Appendix B contains the program listings.

2.4.1 Main Routine

The main routine of the front panel control software is organized as a subroutine which needs no parameters upon entry. Operation of the front panel is solely by a call to this subroutine. For each entry to this main routine, only one panel operation is performed, i.e. the displaying of a value or the processing of a character that has been entered.

Upon entry to the routine, the computer must first determine by interrogating the mode switch whether the operation requested is data
entry or data display. If data display is requested the position of the data selector and mode switches are then determined. The position of the mode switch is needed to determine if the data of interest is input parameter data or calculated result data. Since all data values are stored in binary format in the computer, the value of interest is converted to BCD (Binary coded decimal) format which is needed by the display unit. The value is displayed on the LED display and the panel routine is exited.

If, on the other hand, it is found that the operation requested is data entry, the panel is interrogated for a character awaiting entry. If this is the first data entry request since a data display request, four RAM (random access memory) locations are zeroed and LED display unit is blanked. The four memory locations are used as a buffer to hold the entered digits until an "E" or "CE" command is entered. The routine is exited if no keyboard entry is found. If, however, a keyboard entry is available, the computer inputs the entry and decides whether it is an "E", a "CE", or a digit. For a digit entry, each digit already in the memory buffer is shifted to its next higher significant position and the new entry then becomes the least significant digit. The most significant digit of the digit buffer area is always lost. The contents of the buffer area is displayed and the routine is exited.

A "CE" (clear entry) causes the digit buffer area to be zeroed and the display to be blanked. If the entry is an "E", the contents of the digit buffer, which is in BCD format, is converted to binary format and stored in three memory locations in the computer. The specific memory locations are determined by the position of the data selector. The digit buffer area is then zeroed, the display blanked, and the routine exited.
2.4.2 **Display Subroutine**

The Display subroutine, `OUTSB`, displays the four BCD digits found in the RAM digit buffer area onto the LED seven-segment display. No parameters are transferred upon entry. The displaying is accomplished by consecutively placing one of the BCD digits on the output data bus and activating its control line.

2.4.3 **Rotary Switch Position Subroutine**

The Rotary Switch Position subroutine, `ROTPOS`, determines the position of the data selector switch. The data output bus address, the data input bus address, and the data selector enable code are transferred into the routine when the subroutine is called. A register returns from the routine with an index number between 0 and 7 indicating the switch position.

2.4.4 **Rotary Switch Address Subroutine**

The Rotary Switch Address subroutine, `ROTSW`, determines the address of a specified binary data value. The routine requires, upon entry, that the starting address of the binary data value area be contained in one register pair and an index (0-7) in another register. Upon return from the subroutine, the register pair will have been modified to contain the address of the least significant bits of the specified data value. The subroutine assumes that each data value occupies three 4-bit bytes.

2.4.5 **Addition Subroutine**

The addition of two 12-bit numbers is performed by the Addition subroutine. The subroutine has two entry points, `ADD` and `ADD1`. Entering the routine at `ADD` resets the carry condition bit to zero while entering at `ADD1` leaves the carry bit unaffected. The two 12-bit numbers are
transferred into the subroutine in two groups of three index registers each. The result of the addition returns from the subroutine in one of these groups of index registers.

2.4.6 Subtraction Subroutine

The Subtraction subroutine performs the subtraction of two 12-bit numbers. This subroutine also has two entry points, SUB and SUB1, which provide the same capability as in the Addition subroutine; that is, resetting the carry bit. The transfer of information to and from the Subtraction subroutine is accomplished as in the Addition subroutine.

2.4.7 Increment Subroutine

The Increment subroutine is used to increment the contents of a particular register pair. The subroutine has two entry points, INC and INCl. Entering the routine at INCl will cause the register pair to be incremented by one. Entering at INC, however, will cause the register pair to be incremented by the contents of the accumulator. The particular register pair is fixed within the subroutine and is not transferred into the routine as a parameter.

2.4.8 Zero Ram Subroutine

The Zero Ram subroutine, with entry point BLANK, is used to zero four consecutive RAM locations. The starting RAM address is transferred to the routine in a register pair. A limitation to the routine occurs since the consecutive RAM addresses are determined by incrementing only the four least significant bits and not the entire eight bit address. This means that the four most significant bits never change regardless of the starting RAM address. Details and ramifications of this can be easily seen by examining the program listing.
2.4.9 Multiply Subroutine

The Multiply subroutine, MUL, is used to multiply a twelve bit number by a four bit number. The result of this multiplication must not exceed twelve bits. Upon entry to the subroutine, two registers and the accumulator will contain the twelve bit number and the address of the four bit number will be found in a register pair. On exit, the result is placed in a group of three index registers. The multiplication is accomplished within the routine by repetitive addition. The main use of this subroutine is for BCD to binary conversion.

2.4.10 Divide Subroutine

The Divide subroutine, DIV, performs the division of two twelve bit numbers. The result of this operation can occupy no more than four bits or a memory byte. Two groups of index registers, three registers each, contain the two numbers at time of entry to the routine. Another register pair contains the address into which the result will go. At exit from the routine, one of the index register groups contains the remainder and the register pair contents have been decremented. The division operation is accomplished by repetitive subtraction. This subroutine helps perform binary to BCD code conversion.

2.5 Software Results

As stated before, the control panel software package requires no additional software other than the two system subroutines mentioned. Also, no additional software is needed during power-up initialization phase. No other program, however, must alter the contents of certain RAM locations. These locations are those specified by hexadecimal addresses 24 through 23 and RAM status character $ of RAM $.
Software requires 288 words of PROM (programmable read-only memory). Optimization of the software with respect to minimizing memory used has been attempted; however, still more optimization may be possible.
3.0 **Operating Procedures**

The operating procedure for the experimental control panel will be presented in a step-by-step manner. The nomenclature will refer to that on the constructed panel which is shown in Fig. 8.

3.1 **Data Input**

1. Position the **mode selector switch** labeled "DATA" to the "IN" position. The "DATA IN" lamp will light.

2. Position the **rotary data selector switch** to the desired variable. The labels above the green lamps are the input variables. The appropriate green lamp will light.

3. Enter the desired number followed by a "E" (#). As each digit is entered it will appear on the display. Only the last four digits entered are significant. A "CE" (*) entry will remove the digits previously entered thereby blanking the display. A "E" (#) entry will assign the number in the display to the parameter chosen by the data selector.

**NOTE:** The above procedure is used whether initially entering the parameters or at any time changing a parameter or parameters.

3.2 **Data Display**

1. Position the **mode selector switch** labeled "DATA" to the center position for displaying input parameters or to the position labeled "OUT" for the calculated results.

2. Position the **rotary data selector switch** to the desired parameter. The labels above the lamps are the input parameters and the labels below are the calculated results. The appropriate lamp will light and the value of the parameter will be displayed.
Figure 1. Control Panel Block Diagram
Figure 2. SYNC Threshold Adjustment
Figure 3. Coded Keyboard Interface
Figure 4. Display Interface
Figure 5. Data Selector Interface
DATA SELECTOR CODE

CODE (BINARY) | SELECTOR LABEL
--- | ---
000 | X DESTINATION, X POSITION
001 | Y DESTINATION, Y POSITION
010 | X SET, HEADING CORRECTION
011 | Y SET, BEARING TO DESTINATION
100 | φx, DISTANCE TO DESTINATION
101 | φy, TIME TO DESTINATION
110 | Dx, GROUND SPEED
111 | Dy, TRACK HEADING

MODE SELECTOR CODE

CODE (BINARY) | SELECTOR LABEL
--- | ---
00 | DATA RESULT DISPLAY (DOWN POSITION)
01 | DATA INPUT (UP POSITION)
10 | DATA INPUT DISPLAY (CENTER POSITION)

Figure 6 Selector Codes
Figure 7. Indicator Circuits

*5 volt, 60 milliampere incandescent lamp
Figure 9. Keyboard Interface
Bottom View
(Circuit Side)(Actual Size)
Figure 10. Front Panel Interface
Bottom View
(Circuit Side)(Actual Size)
<table>
<thead>
<tr>
<th>PIN #</th>
<th>F.P. CONN.</th>
<th>PIN #</th>
<th>F.P. CONN.</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>+5 VOLTS</td>
<td>19</td>
<td>+5 VOLTS</td>
</tr>
<tr>
<td>2</td>
<td>NC</td>
<td>20</td>
<td>NC</td>
</tr>
<tr>
<td>3</td>
<td>BIT φ</td>
<td>21</td>
<td>BIT φ</td>
</tr>
<tr>
<td>4</td>
<td>BIT 1 DATA INPUT</td>
<td>22</td>
<td>BIT 1 DATA INPUT</td>
</tr>
<tr>
<td>5</td>
<td>BIT 2 BUS</td>
<td>23</td>
<td>BIT 2 BUS</td>
</tr>
<tr>
<td>6</td>
<td>BIT 3</td>
<td>24</td>
<td>BIT 3</td>
</tr>
<tr>
<td>7</td>
<td>KB DATA ENABLE</td>
<td>25</td>
<td>READOUT ENABLE(L.S.DIGIT)</td>
</tr>
<tr>
<td>8</td>
<td>DATA READY ENABLE</td>
<td>26</td>
<td>READOUT ENABLE</td>
</tr>
<tr>
<td>9</td>
<td>KB RESET</td>
<td>27</td>
<td>READOUT ENABLE</td>
</tr>
<tr>
<td>10</td>
<td>CENTER TAP OF POT</td>
<td>28</td>
<td>READOUT ENABLE(M.S.DIGIT)</td>
</tr>
<tr>
<td>11</td>
<td>NC</td>
<td>29</td>
<td>ROTARY SWITCH ENABLE</td>
</tr>
<tr>
<td>12</td>
<td>NC</td>
<td>30</td>
<td>NC</td>
</tr>
<tr>
<td>13</td>
<td>NC</td>
<td>31</td>
<td>DESTINATION LIGHT</td>
</tr>
<tr>
<td>14</td>
<td>NC</td>
<td>32</td>
<td>+ LIGHT</td>
</tr>
<tr>
<td>15</td>
<td>NC</td>
<td>33</td>
<td>+ LIGHT</td>
</tr>
<tr>
<td>16</td>
<td>NC</td>
<td>34</td>
<td>SYNC LIGHT</td>
</tr>
<tr>
<td>17</td>
<td>NC</td>
<td>35</td>
<td>NC</td>
</tr>
<tr>
<td>18</td>
<td>GROUND</td>
<td>36</td>
<td>GROUND</td>
</tr>
</tbody>
</table>

Figure 11. Front Panel Pin Connections
Figure 12. Omega Receiver Software Requirements
FRONT PANEL MAIN PROGRAM

START

Load "rotary switch enable" code

Output command (BENAB)

Read "Data In" switch

Is data to be input?

Yes → 50

No → Zero "Indicator"

10
FRONT PANEL MAIN PROGRAM CONTINUED

10

Determine position of rotary switch (ROTPOS)

Determine if display data is input or calculated data

Determine address of display data (ROTSW)

Convert binary to BCD data and store in ram (uses DIV)

300
FRONT PANEL MAIN PROGRAM CONTINUED

50

Disable "rotary switch enable" (AENAB)

Read "Indicator"

Is "Indicator" zero?

Yes

"Indicator" equals 1

Reset "character ready" Flip Flop (AENAB)

Blank BCD digit buffer (BLANK)

Display Blanks (zeros) (OUTSB)

No

75
FRONT PANEL MAIN PROGRAM CONTINUED

75

Enable "Data Ready" line (BENAB)

Input "data ready" bit

Disable "data ready" line (AENAB)

Is a character ready?

Yes

Enable "Data" lines (BENAB)

80

No

310
FRONT PANEL MAIN PROGRAM CONTINUED

80

Input character

Disable "Data" lines and reset "character ready" Flip Flop (AENAB)

Is character an "G"?

Yes → 100

No

Is character a "CE"?

Yes → 180

No

Shift characters left 1 place and add new character

300
FRONT PANEL MAIN PROGRAM CONTINUED

100
Enable "Rotary Switch" line (BENAB)

Determine position of rotary switch (ROTPOS)

Determine address of input value to be stored (ROTSW)

Convert BCD digits to binary (uses MUL)

Store in ram locations

180
Clear BCD values (BLANK)

300
Display values in BCD slots (OUTSB)

310
RETURN
DISPLAY OUTPUT SUBROUTINE

OUTSB

Set counter to -4 and pointers

Read BCD digit from ram

Output character to bus

Enable "Readout control" line (AENAB)

Increment "Readout control"

Increment ram address and counter

Is counter zero?

Yes
RETURN

No
10
ROTARY SWITCH POSITION SUBROUTINE

ON ENTRY: Register pair 5 has output port address. Register pair 4 has input port address and the starting index number. Register pair 6 has the rotary switch enable code.

ON EXIT: Register 9 has index number (0-7).

FLOW DIAGRAM:

```
ROTPOS

Output index to bus

Input result of output

Is index at correct position

Yes  20

No

Increment index

20

Disable "Rotary Switch" line (AENAB)

RETURN
```
ROTARY SWITCH ADDRESS SUBROUTINE

ON ENTRY: Register 9 contains index position of rotary switch (0-7).
          Register pair 7 has base address of data area.

ON EXIT: Register pair 7 has the address of the least significant bits of the binary data of interest.

FLOWCHART:

1. **ROTSW**
2. Increment index (Reg. 9)
3. Decrement index
4. Is index zero?
   - Yes: 20
   - No: Increment register pair 7 by 3 (INC)

RETURN
ADDITION SUBROUTINE

ON ENTRY: Registers 6, 7, 8 have a 12 bit number
           Registers 9, 10, 11 have a 12 bit number

ON EXIT:  Register 9, 10, 11 have the result of the sum
           of the two 12 bit numbers

ADD1

ADD

Clear carry and accumulator

Add least significant 4-bit bytes

Add next significant 4-bit bytes

Add most significant 4-bit bytes

RETURN
SUBTRACTION SUBROUTINE

ON ENTRY: Registers 6, 7, 8 contain a 12 bit number
Registers 9, 10, 11 contain a 12 bit number

ON EXIT: Registers 9, 10, 11 contain the 12 bit result

- Clear carry and accumulator
- Subtract least significant 4-bit byte
- Complement carry bit
- Subtract next significant 4-bit byte
- Complement carry bit
- Subtract most significant 4-bit byte
- RETURN
INCREMENT SUBROUTINE

ON ENTRY: Register pair 7 has a value
Accumulator may have a value

ON EXIT: Register pair 7 has a modified value

- Accumulator = 1
- Clear carry bit
- Add accumulator to Register pair 7
- RETURN
ZERO RAM SUBROUTINE

ON ENTRY: Register pair 5 has a ram address

- BLANK -
  
  Set Counter to -4
  
  Clear Accumulator
  
  Set memory to 0
  
  Increment memory address
  
  Increment counter
  
  Is counter zero?
  
  Yes
  
  RETURN
MULTIPLY SUBROUTINE

ON ENTRY: Registers 6, 7, accumulator contain one multiplier
Register pair 6 contains the address of the other multiplier

ON EXIT: Binary result is added to registers 9, 10, 11
Register pair 6 contains the next address
MULTIPLY SUBROUTINE CONTINUED

30

Is loop count zero?

50

Increment address of loop count

RETURN

10

No
DIVIDE SUBROUTINE

ON ENTRY: Registers 6, 7 and accumulator have values to divide into values in registers 9, 10, 11. Register pair 6 has the address for the result.

ON EXIT: Registers 9, 10, 11 have the remainder. Register pair 6 has been decremented.
DIVIDE SUBROUTINE CONTINUED

20

Add number back to registers 9, 10, 11 to obtain remainder (ADD)

Store "count" as the answer

Decrement address of result

RETURN
MAIN ROUTINE

Start
FIM P6 Load "rotary SW enable" code
JMS
$E Enable rotary SW, etc.
BENAB
FIM P5 P5 = output bus CMD
2$ P4 P4 = input bus CMD
FIM $F
SRC P4 Output input CMD
RDR Input data on bus
RAR
RAR Shift data SW to carry
XCH 2 Save reg 2
JCN CY = 1 Jump if data to be input
LB5$ CLB
WR$ Set indicator = $
JMS
XCH 2 Determine rotary SW pos
RAR Restore SW status
FIM P7 P7 = Starting addr of input data
6$ JCN CY = 1 Jump if outputing input data
LB2$ LB5$ P7 = Starting addr of output data
FIM 78
LB2$ JMS Determine addr of data to be displayed
FIM P6 Addr of MS display digit
23 FIM P1 Value = -3 for counter
D$ LB3$
SRC P7 Load value to be displayed
RDM to regs 9,A,B from RAM
XCH E
XCH A
XCH 9
JMS
INCl 2
LB3$
FIM P3 Reg 6,7,8 = 1000
6$ E
LDM 3
JMS Determine MS digit
DIV
FIM P3 Reg 6,7,8 = 100
LDM  φ
JMS  Determine 2nd digit

DIV
FIM  Reg 6, 7, 8 = 10
  P3
  A φ

LDM  φ
JMS  Determine 3rd digit

DIV
SRC  Store l.s. digit in RAM
  P6
LD
WRM  9
JUN

LB5 φ
JMS  Disable "rotary SW enable"
SRC  AENAB
P4  Read "indicator"
RDφ
JCM  ACC ≠ 0
  ACC = 0 Jump if "indicator" = 1
LB75
LDM  Set "indicator" = 1
  P6
WRφ
FIM  Reset "Char Avail" flip flop
  P6
LC
JMS  AENAB
JMS  Blank BCD digit LOCS
JMS  BLANK
Display blanks

LB75
FIM  P6
JMS  Enable "data ready" line
1D
 SRC  BENAB
P4  Read "data ready"
RDR
XCH  Save in Reg. 2
2
JMS  Disable "data ready" line
  AENAB
JMS  Blank BCD digit LOCS
XCH  Amplify blanks
  2
RAR  Restore "data ready" bit

JCN  Jump if not ready
  CY = 0
LB310
INC  Increment CMD line ADR
  D
JMS  Enable data lines
  BENAB
SRC  P4
RDR  Input data char
XCH  Save char in reg 2
  2
XCH  2
FIM  Save char in reg 2
  P6
LC
JMS  Disable "data" lines and reset
  "Char Avail" FF
AENAB
CLC
LDM  ACC = "CE"
  A
SUB 2
JCN CY = φ
JCN ACC = φ
LB1φφ
JCN ACC = φ
LB18φ
FIM P7 2φ
FIM P7 2φ
FIM P7
FIM P7
LB85
FIM LE3φφ
FIM P6 2φ
JMS BENAB
JMS ROTPOS
FIM P7 6φ
JMS ROTSW
FIM P6 2φ
FIM P3 Aφ
FIM PH P5 2φ
FIM P6
SRC P6
RDM P6
XCH 9
INC D
JMS MUL
FIM P3 46
LDM φ
JMS MUL
FIM P3 6E
LDM 3
JMS

Jump if char was a "E"
Jump if char was an "CE"
P7 = Addr of BCD digits in RAM
Shift chars left 1 and add new char
Enable "Rotary switch" line
Determine position of rotary switch
Addr of input data
Determine addr of data value
Determine binary from BCD
Regs 6,7,8 contain multiplier
Regs 9,A,B hold accumulation
Read L.S. digit
Add to accum regs
Regs 6,7,8 = 1φ
Reg 6,7,8 = 1φφ
Regs 6,7,8 = 1φφφ
FIM
MUL
P1
Reg 2 = -3

FIM
XCH
Dφ
Store binary in RAM

FIM
XCH
B

FIM
XCH
A

FIM
XCH
9

FIM
SRC
P7

WRM
JMS
INC1
Increment reg E and F if carry

ISZ
2

LB11φ
LB11φ
LB11φ
LB11φ

JMS
BLANK
Blank 4 locations

JMS
OUTSB
Display BCD values

LB3φφ
LB3φφ
LB3φφ
LB3φφ

BEL
φ
Exit
### DISPLAY SUBROUTINE

<table>
<thead>
<tr>
<th>OUTSB</th>
<th>FIM P1</th>
<th>Pl = OUTPUT command and -h (counter)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2C</td>
<td></td>
</tr>
<tr>
<td>FIM P6</td>
<td>Output Code for L.S. Digit display</td>
<td></td>
</tr>
<tr>
<td>FIM P2</td>
<td>Address of L.S. Digit (BCD)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2¢</td>
<td></td>
</tr>
<tr>
<td>OUT1¢</td>
<td>SRC P2</td>
<td></td>
</tr>
<tr>
<td>RDM</td>
<td>Read BCD Digit</td>
<td></td>
</tr>
<tr>
<td>SRC P1</td>
<td>Output digit</td>
<td></td>
</tr>
<tr>
<td>WRR</td>
<td>Latch digit to display</td>
<td></td>
</tr>
<tr>
<td>JMS</td>
<td>INC D</td>
<td>Increment command code</td>
</tr>
<tr>
<td></td>
<td>INC 5</td>
<td>Increment Address</td>
</tr>
<tr>
<td>ISZ</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OUT1¢</td>
<td>Return</td>
</tr>
<tr>
<td>BBL</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Return</td>
<td></td>
</tr>
</tbody>
</table>
ROTARY SWITCH POSITION SUBROUTINE

ROTPOS
SRC  P5
LD   9
WRR
SRC  P4
RDR   Input status of line
RAR
JCN  CY = φ Jump if switch position found
ROTP2φ
INC  9 Increment index
JUN
ROTPOS
ROTP2φ
JMS Disable "Rotary switch" line
AENAB
BRL  φ Return
ROTARY SWITCH ADDRESS SUBROUTINE

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROTSW INC</td>
<td>Register 9 has index no. (0-7)</td>
</tr>
<tr>
<td>ROT1 XCH</td>
<td>Jump if index = φ</td>
</tr>
<tr>
<td>DAC JCN ACC = φ</td>
<td></td>
</tr>
<tr>
<td>ROT2 XCH</td>
<td>Bump address in Register pair 7 by 3</td>
</tr>
<tr>
<td>LDM 3</td>
<td></td>
</tr>
<tr>
<td>JMS INC</td>
<td></td>
</tr>
<tr>
<td>JUN ROT1</td>
<td>Return</td>
</tr>
<tr>
<td>ROT2 BBL</td>
<td>φ</td>
</tr>
</tbody>
</table>
ADD
ADD1
CLB
LD  9  Add L.S. bytes
ADD 6
XCH 9  Save L.S. byte
LD A  Add next bytes
ADD 7
XCH A
LD B  Add M.S. bytes
ADD 8
XCH B
BBL 4  Return
SUBTRACTION SUBROUTINE

<table>
<thead>
<tr>
<th></th>
<th>Action</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SUB</td>
<td>CLB</td>
<td>Clear carry and accumulator</td>
</tr>
<tr>
<td>SUBl</td>
<td>LD 9</td>
<td>Subtract L.S. bytes</td>
</tr>
<tr>
<td></td>
<td>SUB 6</td>
<td>Complement Carry</td>
</tr>
<tr>
<td></td>
<td>XCH 9</td>
<td>Subtract next bytes</td>
</tr>
<tr>
<td></td>
<td>LD A</td>
<td>Complement Carry</td>
</tr>
<tr>
<td></td>
<td>SUB 7</td>
<td>Subtract M.S. bytes</td>
</tr>
<tr>
<td></td>
<td>CMC</td>
<td></td>
</tr>
<tr>
<td></td>
<td>XCH A</td>
<td></td>
</tr>
<tr>
<td></td>
<td>LD B</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SUB 8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>XCH B</td>
<td></td>
</tr>
<tr>
<td>BBL</td>
<td>⬤</td>
<td>Return</td>
</tr>
</tbody>
</table>
# INCREMENT SUBROUTINE

<table>
<thead>
<tr>
<th>INCl</th>
<th>LDM</th>
<th>1</th>
<th>Accumulator = 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>INC</td>
<td>CLC</td>
<td></td>
<td>Clear Carry</td>
</tr>
<tr>
<td>ADD</td>
<td>F</td>
<td></td>
<td>Add Acc to Reg</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ster pair 7</td>
</tr>
<tr>
<td>XCH</td>
<td>F</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LDM</td>
<td>$\phi$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADD</td>
<td>E</td>
<td></td>
<td></td>
</tr>
<tr>
<td>XCH</td>
<td>E</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BEL</td>
<td>$\phi$</td>
<td></td>
<td>Return</td>
</tr>
</tbody>
</table>
ZERO RAM SUBROUTINE

<table>
<thead>
<tr>
<th>BLANK</th>
<th>FIM P1</th>
<th>( \phi C )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>LDM ( \phi )</td>
<td>Clear Accumulator</td>
</tr>
<tr>
<td>BL1( \phi )</td>
<td>SRC P5</td>
<td>Write in RAM</td>
</tr>
<tr>
<td></td>
<td>WRM</td>
<td>Increment address</td>
</tr>
<tr>
<td></td>
<td>INC B</td>
<td>Increment counter and jump if not zero</td>
</tr>
<tr>
<td></td>
<td>ISZ 3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>BL1( \phi )</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EBL ( \phi )</td>
<td>Return</td>
</tr>
</tbody>
</table>
MULTIPLY SUBROUTINE

<table>
<thead>
<tr>
<th>MUL</th>
<th>XCH</th>
<th>8</th>
<th>Move accumulator to register 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>SRC</td>
<td>P6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RDM</td>
<td></td>
<td></td>
<td>Find multiplier by address in P6</td>
</tr>
<tr>
<td>JCN</td>
<td>acc</td>
<td>phi</td>
<td>Jump if count = phi</td>
</tr>
<tr>
<td></td>
<td>MUL5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MUL1</td>
<td>XCH</td>
<td>2</td>
<td>Save loop count</td>
</tr>
<tr>
<td></td>
<td>JMS</td>
<td></td>
<td>Add number to accumulation area</td>
</tr>
<tr>
<td>LD</td>
<td>2</td>
<td></td>
<td>Decrement loop count</td>
</tr>
<tr>
<td>DAC</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>JCN</td>
<td>acc</td>
<td>phi</td>
<td>Jump if not phi</td>
</tr>
<tr>
<td></td>
<td>MUL1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MUL5</td>
<td>INC</td>
<td>D</td>
<td>Increment BCD address</td>
</tr>
<tr>
<td></td>
<td>BBL</td>
<td>phi</td>
<td>Return</td>
</tr>
</tbody>
</table>
## DIVIDE SUBROUTINE

<table>
<thead>
<tr>
<th>DIV</th>
<th>XCH</th>
<th>8</th>
<th>Move accumulator to register 8</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>LDM</td>
<td>F</td>
<td>Register 2 = -1 (count)</td>
</tr>
<tr>
<td></td>
<td>XCH</td>
<td>2</td>
<td>Subtract registers 6,7,8 from 9,A,B</td>
</tr>
<tr>
<td>DIV1+</td>
<td>JMS</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SUB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>INC</td>
<td>2</td>
<td>Increment &quot;count&quot;</td>
</tr>
<tr>
<td></td>
<td>JCN</td>
<td>CY = 1</td>
<td>Jump if result not negative</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>JMS</td>
<td></td>
<td>Add registers 6,7,8 to result-remainder</td>
</tr>
<tr>
<td></td>
<td>ADDL</td>
<td></td>
<td>Store &quot;count&quot; in BCD location</td>
</tr>
<tr>
<td></td>
<td>SRC</td>
<td>P6</td>
<td></td>
</tr>
<tr>
<td></td>
<td>LD</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>WRM</td>
<td></td>
<td>Decrement address</td>
</tr>
<tr>
<td></td>
<td>LD</td>
<td>D</td>
<td></td>
</tr>
<tr>
<td></td>
<td>DAC</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>XCH</td>
<td>D</td>
<td></td>
</tr>
<tr>
<td></td>
<td>BBL</td>
<td>φ</td>
<td>Return</td>
</tr>
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# DISTRIBUTION LIST

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<th>Copy No.</th>
<th>Name</th>
<th>Position</th>
<th>Address</th>
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<tbody>
<tr>
<td>1 - 5</td>
<td>Mr. John Wells, Jr.</td>
<td>National Aeronautics and Space Administration</td>
<td>Mail Stop 470, National Aeronautics and Space Administration, Langley Research Center, Hampton, Virginia 23365</td>
</tr>
<tr>
<td>6</td>
<td>Mr. Dennis Joe Martin</td>
<td>Office of University Affairs</td>
<td>Mail Stop 105A, National Aeronautics and Space Administration, Langley Research Center, Hampton, Virginia 23365</td>
</tr>
<tr>
<td>7 - 8</td>
<td>E. A. Parrish, Jr.</td>
<td></td>
<td></td>
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<tr>
<td>9 - 10</td>
<td>J. H. Aylor</td>
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<td>11</td>
<td>J. N. Warfield</td>
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<td>I. A. Fischer</td>
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<tr>
<td>13 - 14</td>
<td>E. H. Pancake</td>
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</tbody>
</table>
PROCESSOR ARCHITECTURES UTILIZING
MAGNETIC BUBBLE AND SEMI-CONDUCTOR MEMORIES

Interim Report

NASA Contract Number NSG-1067

Submitted to:
Mr. John Wells, Jr.
Mail Stop 470
National Aeronautics and Space Administration
Langley Research Center
Hampton, Virginia 23365

Submitted by:
E. A. Parrish, Jr.
Associate Professor

and

J. H. Aylor
Research Engineer

Department of Electrical Engineering
RESEARCH LABORATORIES FOR THE ENGINEERING SCIENCES
SCHOOL OF ENGINEERING AND APPLIED SCIENCE
UNIVERSITY OF VIRGINIA
CHARLOTTESVILLE, VIRGINIA

Report No. EE-4027-102-75
April 1975

Copy No. 4
The University of Virginia's School of Engineering and Applied Science has an undergraduate enrollment of approximately 1,000 students with a graduate enrollment of 350. There are approximately 120 faculty members, of whom, about 90% hold a doctorate. Excellence in graduate education is aided and supplemented by a research program approximating $3 million per year. This relatively high level of participation in sponsored research is one factor which helps our faculty consistently to maintain high quality graduate education at all degree levels.

As research is an integral part of the educational program, research interests parallel academic specialties. These interests range from the traditional engineering departments of Chemical, Civil, Electrical and Mechanical to include departments of Biomedical Engineering, Engineering Science & Systems, Materials Science, Nuclear Engineering, and Applied Mathematics & Computer Science. In addition to these departmental interests, there are interdepartmental groups in the areas of Automatic Controls and Applied Mechanics. All departments are authorized to offer the doctorate while the Biomedical and Materials Science Departments are graduate degree granting departments only.

The School of Engineering and Applied Science, is an integral part of an outstanding University, which has strong professional Schools of Law, Medicine, and Business Administration. In addition, the College of Arts and Sciences has strong basic science departments in Mathematics, Physics, Chemistry, and other departments relevant to the engineering research program. This not only provides an excellent scholarly climate, but also enhances the school's potential for creating truly interdisciplinary teams in the pursuit of our basic goals of education, research, and public service.

Inside this cover are listed some of the present research activities of the department from which this report originates. For more information on this or other areas, address the department chairman or Dean J. E. Gibson, Commonwealth Professor and Dean, School of Engineering and Applied Science, University of Virginia, Charlottesville, Virginia 22901.