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EFFICIENCY AND WEIGHT OF VOLTAGE MULTIPLIER TYPE ULTRA LIGHTWEIGHT D. C. - D. C. CONVERTERS

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Summary

This paper presents an analytical and experimental study of a capacitor-diode voltage multiplier without a transformer which offers the possibility of high efficiency with light weight. D.c.-d.c. conversion efficiencies of about 94 percent were obtained at output powers of 150 watts at 1000 volts using 8x multiplication. A detailed identification of losses was made, including forward drop losses in component, switching losses, reverse junction capacitance charging losses, and charging losses in the main ladder capacitors.

Introduction

Power processing equipment used in space flight applications should be lightweight, and have the ability to deliver a wide range of output power while maintaining a high efficiency. Presently available equipment, which typically is a d.c.-d.c. converter including a transistor chopper with a transformer for voltage transformation, does not completely meet these requirements. Systems with high efficiency (90 to 95 percent) can be designed and built, but the total system weight is substantially higher than desired. The voltage multiplier concept, which uses capacitors and diodes for voltage transformation, appears attractive as an alternative.

This paper extends the concept of the transistor chopper driven capacitor diode voltage multiplier (CDVM) d.c.-d.c. converter (Refs. 1 to 4) to a wide range of weights, efficiencies, and output power by exploring the tradeoffs between the CDVM converter design parameters. Investigation indicates that it is possible to design either a very lightweight converter with somewhat reduced efficiency, a very high efficiency converter with a somewhat increased weight, or an in-between converter where the efficiency and weight can be tailored to a given application.

A 100-watt, 1000-volt experimental model with a chopping frequency of 70 kHz was used for all testing. Efficiencies as high as 94.1 percent were attained at 100 watts output with a component weight of about 2 kg/kW and a 92.3 percent efficiency at a component weight of 1 kg/kW. Thus the CDVM d.c.-d.c. converter offers a better combination of efficiency and weight, compared to conventional power processing, and also has the capability of a wide range of weight and efficiency to fit a given application.

Experimental Model

Figure 1 shows a circuit diagram of the experimental CDVM converter used to obtain the data in this report. The converter consists of a transistor chopper (drive at 70 kHz) connected directly into a voltage multiplier with N = 8. No transformer is required, which is a major advantage from a weight, cost, and efficiency standpoint. Two d.c. power supplies were used in the experimental setup for versatility and convenience. One supply could be used (with a voltage of 2 Vf) without affecting the converter performance. The nominal output voltage of the experimental model was 1000 volts with the input power supplies at +130 volts and -130 volts.

Losses and Efficiency

The tradeoff between efficiency, weight, and output power in the CDVM converter can be determined from a study of the losses involved in the system. These losses along with approximate expressions for their value, are listed in ten categories. They are:

1. Capacitance charging losses (Ref. 5) in the voltage multiplier capacitors while the diodes are conducting. This includes series resistance losses in the leads, and in the equivalent series resistance of the capacitors. It is treated in detail in Ref. 5 and will not be derived here. Both losses in charging a capacitor from another capacitor and in charging a capacitor from another capacitor are included as appropriate. The expression for this loss (P1) for a voltage multiplier with N diodes and N capacitors, a load current IL and unit capacitors C0 operated at a frequency f is

\[ P_1 = \frac{12NC_0}{12C_0} \]  

(1)

2. Charging losses of the reverse biased...
junction capacitance of the CDVM diodes during the time when the diodes are not conducting. This loss \( P_2 \) is given by

\[
P_2 = 4N Imper V^2 f
\]

where \( C_{BP} \) is the junction capacitance of each diode in the voltage multiplier. As the diode junction begins to block where the input voltage swings from \(+V_f\) to \(-V_f\) or vice versa, the diode voltage changes from about a volt in the forward direction to \(2V_f\) in the reverse. The charge taken from the capacitors \( C_u \) and the voltage sources to charge \( C_{BP} \) to \(2V_f\) is then \( 2C_{BP}V_f \). Since the battery and/or capacitors supply the charge at a voltage \(2V_f\), the amount of energy used in this junction capacitance charging is \( 4C_{BP}V^2_f \) per diode. The total energy loss for the \(N\) diodes is then \( 4C_{BP}V^2_f \) for each charging cycle, which occurs \( f \) times per second. The power loss due to this cause is therefore \( 4C_{BP}V^2_f f \).

(3) Charging losses of the chopping transistor junction capacitance (output capacitance) during the transistor "off" period. This loss \( P_3 \) is given by

\[
P_3 = 8C_{TR} V^2 f
\]

It is similar to \( P_2 \). The junction capacitance \( C_{TR} \) of the individual transistor is charged to a voltage \( 2V_f\) each cycle, with a consequent energy loss of \( 4C_{TR}V^2_f \). Since there are two transistors operating at a frequency \( f \), the total power loss is given in Eq. (3).

(4) Forward conduction losses of the CDVM diodes. This loss \( P_4 \) is due to the forward voltage drop across the diodes during their "on" time. This power loss \( P_4 \) is therefore

\[
P_4 = NV_{FD}I_f
\]

where the average diode current must be equal (ignoring leakages) to the load current. \( V_{FD} \) is the forward voltage drop of the conducting diode when carrying the load current, which was taken as a constant for this treatment. The factor \( N \) enters because there are \(N\) diodes, each of which must carry the load current \( I_f \) as an average current.

(5) Transistor forward conduction losses in the transistor chopper. As in the case of the diode, this is due to the saturation voltage across the transistors during the conduction cycle. This power loss \( P_5 \) is given by

\[
P_5 = 2V_{FD}N I_f
\]

where \( V_{TF} \) is the forward conduction drop of the transistor. The number of diodes enter because the transistor current in \( N I_f \), neglecting second order effects, and the factor of \( 2 \) is needed because two transistors are used.

(6) Reverse bias d.c. leakage losses in the CDVM diodes caused by reversed current flow while the diodes are off. This power loss \( P_6 \) is given by

\[
P_6 = 2V_{FD} I_{BA} N
\]

and is due to the use of \( N \) diodes, charged to a voltage \( 2V_f\), with a leakage current \( I_{BA} \). For good diodes, the leakage current is in the micromicroampere range, so that \( P_6 \) is usually negligible compared to other losses.

(7) D.C. leakage losses of the transistors in the "off" state. This loss is comparable to \( P_6 \) for the diodes. The expression for it is

\[
P_7 = 2V_{FD} I_{OFF}
\]

where \( I_{OFF} \) is the residual current flowing through the transistor when it is off. This current is of the order of milliamperes so that \( P_7 \) cannot be ignored as \( P_6 \) was. Again, the factor of \( 2 \) is necessary because the chopper has two transistors.

(8) Transistor base drive losses. This is about 1 watt at 100 watts output. An approximate expression for this loss is

\[
P_8 = 1/2 V_d^2 f
\]

where \( V_d \) is in the transistor drive voltage. The average transistor collector current is \( N I_f \), so that the average base current is approximately \( I_f/N \), and the base drive power is as given in Eq. (8). Again, second order effects were ignored, it is believed that this loss can be decreased as the output power is reduced.

(9) Switching losses in the chopper transistors. This power loss \( P_9 \) is for turn on only, since the current goes to zero as capacitor charging is completed, and this occurs before the square wave voltage output from the chopper changes sign. The current driven through the transistor is approximately a half sine wave (positive for one transistor, negative for the other) with a half period in each case of about 3.5 microseconds \( (T_f \approx 7 \mu s) \). The switching loss was calculated by assuming a linear switching decrease in voltage across the transistor from \( V_f \) to zero in the turn on time of the transistor \( T_f \). Integrating these two together over the transistor switching time \( T_f \), and multiplying by the chopping frequency \( f \), gives the power loss \( P_9 \).

\[
P_9 = \frac{2V_f I_f N}{3} \left( \frac{1}{T_f} \right)^2
\]

This switching loss is unusual in that it does not depend on the chopping frequency \( f \). The reason for this is that peak value of the transistor current wave shape with period \( T_f \) is inversely proportional to \( f \) so that the factor drops out.
in the final result.

(10) Switching losses in the CDVM converters.

The switching losses of the CDVM diodes,

The diode switching loss $P_{10}$ is negligible,
since the switching time for turn on is substantial
largely for good diodes than for transistors.

The equation given for $P_{10}$ in Table 1 is an
upper limit for the case of zero rise time on the
diode voltages.

Table 1 lists these losses, the equation
which characterizes each loss, and a calculated
value for each loss (for an output power of 100 W)
as a percentage of the output power. Transistor
losses made up about 20 percent of the total,
second order effects have not been included, since
the individual losses are small. The definition
of symbols used in the equations are given in
Table II. The values of the parameters needed for
the calculations were either determined from a di-
rect laboratory measurement or obtained from the
manufacturer's specification. The values used are
given in Table II. The values shown are for com-
mercially available components. Further selection
or special development of components would bring
further reduction of losses or weight. This is
especially true of the capacitors, which make up
the bulk of the weight of the converter.

With the above losses it is possible to write
an overall efficiency equation as follows:

$$
\eta = \frac{P_1}{P_1 + P_2 + P_3 + \ldots + P_{10}}
$$

If the experimental test model values are
used in the above equation, a value of 94 percent
is obtained for the overall efficiency at an output
of 100 watts. The measured efficiency of the
experimental model checks closely with this figure.

**EXPERIMENTAL RESULTS**

Because of the lower frequencies normally
used in conventional d.c.-d.c. converters, the re-
verse junction capacitance charging losses ($P_3$
Table 1) have little effect on conversion effi-
ciency, and are not normally treated. Because the
CDVM converter operates at a higher frequency
(70 kHz) these losses do contribute to the total
loss of the system. Therefore they were experi-
mentally verified by adding extra capacitance
across the diodes and/or transistors to simulate
larger junction capacitance. In these measurements
(Fig. 2) efficiency is reduced linearly with an increase in capacitance,
which demonstrates the importance of designing
with low junction capacitance transistors and
diodes.

The effect of these losses is further illus-
trated in Fig. 3 where efficiency of the experi-
mental model is shown as a function of output
power for various combinations of junction capaci-
tance and unit capacitance ($C_u$) values. The
lowest efficiencies occur for high values of junction
capacitance and low values of $C_u$. The maximum
value of efficiency was obtained (about 95.4 per-
cent) with a $C_u$ value of 4 $\mu$F. $C_u$ values varied
during the tests from 1 $\mu$F to 4 $\mu$F with
weights and efficiencies at 100 watts output vary-
ing from 1.2 kg/kW at 96 percent to about 2 kg/kW
at 95.7 percent, respectively. The transistor
base drive circuit losses ($P_9$, Table II) is not
included in this figure, but an estimate indicates
that this loss will lower the efficiency by
about 1 percent. The experimental data also
indicates that the overall efficiency remains rela-
tively constant over a wide range of output power.

For a value of $C_u$ of 2 microfarads the
 capacitors $C_1$ to $C_6$ make up about two thirds
of the total weight, with the rest being due to
transistors, diodes, and other components. For
the case when $C_u$ is equal to 4 microfarads, the
capacitor weight is five sixths of the total.
Reducing the capacitance value $C_u$ reduces the
weight, but increases the losses due to capacitor
charging. Clearly, what is needed here is a
higher energy density (lighter weight) capacitor,
so that it would be possible to keep the effi-
ciency high with large values of $C_u$ without
paying a corresponding weight penalty.

**SUMMARY OF RESULTS**

An analytical and experimental investigation
of a d.c.-d.c. converter using a capacitor-diode
voltage multiplier was made with the following
results.

1. Ten separate losses were identified in
the CDVM converter.

2. Losses are a function of:

(a) Chopping frequency

(b) Capacitance size ($C_u$)

(c) Transistor junction capacitance

(d) Diode junction capacitance

(e) Transistor forward voltage drop

(f) Diode forward voltage drop

(g) Transistor switching speed

(h) Diode switching speed

(i) The number of stages in the CDVM

(j) Output voltage and output current

(k) Chopper transistor base drive losses
3. 60 (60 percent) of the losses were in the transistors.

4. The junction capacitance charging from varied linearly with the junction capacitance.

5. It is possible to use the tradeoffs to obtain an optimum system design for a given converter application.

6. A better combination of weight and efficiency are available with voltage multiplier d.c.-d.c. converters than with presently available converters.

7. Efficiency is relatively insensitive to output power.

8. Most of the weight of the converter is in the multiplier capacitors.

Difficult design problems are not anticipated when the CDVM converter is extended to a power processing system. The input filter design should be straightforward and have a low component weight due to the higher chopping frequency, and the output filtering should be minimal due to the filtering action of the CDVM.

REFERENCES


<table>
<thead>
<tr>
<th>Loss type</th>
<th>Formula for loss</th>
<th>Percent loss @ 100 W</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Capacitor charging loss</td>
<td>( P_1 = \frac{1}{2} \left( \frac{V^2}{L} + \frac{1}{2} \right) )</td>
<td>1.5</td>
</tr>
<tr>
<td>2. Diode reverse junction charging loss</td>
<td>( P_2 = 2NC_{DV} \frac{V^2}{f} )</td>
<td>3</td>
</tr>
<tr>
<td>3. Transistor reverse junction charging loss</td>
<td>( P_3 = 8C_{T1} \frac{V^2}{f} )</td>
<td>7</td>
</tr>
<tr>
<td>4. Diode forward conduction losses</td>
<td>( P_4 = NV_{DV} )</td>
<td>8</td>
</tr>
<tr>
<td>5. Transistor forward conduction losses</td>
<td>( P_5 = 2V_{TF}N_{T1} )</td>
<td>1.3</td>
</tr>
<tr>
<td>6. Diode reverse bias d.c. leakage losses</td>
<td>( P_6 = 2V_{I1}I_{Rk} )</td>
<td>0</td>
</tr>
<tr>
<td>7. Transistor &quot;off&quot; d.c. leakage losses</td>
<td>( P_7 = 2V_{I1}I_{OFF} )</td>
<td>3</td>
</tr>
<tr>
<td>8. Transistor base drive loss</td>
<td>( P_8 = \frac{1}{2} NV_{dv} )</td>
<td>1</td>
</tr>
<tr>
<td>9. Transistor switching losses</td>
<td>( P_9 = \frac{2}{3}V_{I1}N \left( \frac{I}{I_{TF}} \right)^2 )</td>
<td>4</td>
</tr>
<tr>
<td>10. Diode switching losses</td>
<td>( P_{10} = \frac{2}{3}V_{I1}I_{N} \left( \frac{I_{D}}{I_{DN}} \right)^2 )</td>
<td>0</td>
</tr>
<tr>
<td>Total losses</td>
<td></td>
<td>6.3%</td>
</tr>
<tr>
<td>Efficiency</td>
<td></td>
<td>94.3%</td>
</tr>
</tbody>
</table>
TABLE II. - DEFINITION OF SYMBOLS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>C_{DR}</td>
<td>reverse junction capacitance of diode. Assumed to be the same for all diodes, ( V )</td>
</tr>
<tr>
<td>C_{TR}</td>
<td>transistor &quot;off&quot; junction capacitance. Average value for the two transistors, ( V )</td>
</tr>
<tr>
<td>C_{u}</td>
<td>unit CDVM capacitance (value for each capacitor for case where ( C_1 = C_2 = \ldots = C_{N_d} ), ( V )</td>
</tr>
<tr>
<td>C_{1} \ldots C_{N_d}</td>
<td>CDVM capacitors, ( V )</td>
</tr>
<tr>
<td>f</td>
<td>frequency, Hz</td>
</tr>
<tr>
<td>I_{DR}</td>
<td>reverse leakage current of diodes at voltage ( 2V_{d} )</td>
</tr>
<tr>
<td>I_{L}</td>
<td>load current, A</td>
</tr>
<tr>
<td>I_{T,OFF}</td>
<td>transistor &quot;off&quot; d.c. leakage current, A</td>
</tr>
<tr>
<td>N</td>
<td>number of diodes (also voltage multiplication factor)</td>
</tr>
<tr>
<td>P_{1}</td>
<td>power loss due to CDVM capacitor charging loss</td>
</tr>
<tr>
<td>P_{2}</td>
<td>power loss due to reverse junction capacitance charging of diodes</td>
</tr>
<tr>
<td>P_{3}</td>
<td>power loss due to transistor &quot;off&quot; junction capacitance charging</td>
</tr>
<tr>
<td>P_{4}</td>
<td>power loss due to forward diode conduction drops</td>
</tr>
<tr>
<td>P_{5}</td>
<td>power loss due to forward transistor conduction drops</td>
</tr>
<tr>
<td>P_{6}</td>
<td>power loss due to reverse bias leakage of diodes</td>
</tr>
<tr>
<td>P_{7}</td>
<td>power loss due to transistor &quot;off&quot; d.c. leakage</td>
</tr>
<tr>
<td>P_{8}</td>
<td>transistor base drive power loss</td>
</tr>
<tr>
<td>P_{9}</td>
<td>transistor switching loss</td>
</tr>
<tr>
<td>P_{10}</td>
<td>diode switching loss</td>
</tr>
<tr>
<td>V_{DS}</td>
<td>diode conduction drop, V</td>
</tr>
<tr>
<td>V_{T}</td>
<td>transistor drive voltage, V</td>
</tr>
<tr>
<td>V_{1}</td>
<td>input voltage</td>
</tr>
<tr>
<td>V_{19}</td>
<td>transistor average forward conduction drop, V</td>
</tr>
<tr>
<td>( \alpha )</td>
<td>chopper transistor current gain</td>
</tr>
<tr>
<td>T_{D}</td>
<td>diode switching time, sec</td>
</tr>
<tr>
<td>T_{ID}</td>
<td>period of diode current, sec</td>
</tr>
<tr>
<td>T_{TF}</td>
<td>period of transistor input current, sec</td>
</tr>
<tr>
<td>T_{T}</td>
<td>transistor turn on time, sec</td>
</tr>
</tbody>
</table>

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### TABLE III. - PARAMETER VALUES

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{DR}$, diode reverse bias junction capacitance</td>
<td>7 pF</td>
</tr>
<tr>
<td>$C_{TR}$, transistor &quot;off&quot; junction capacitance</td>
<td>80 pF</td>
</tr>
<tr>
<td>$V_{TF}$, diode conduction drop</td>
<td>1.0 V</td>
</tr>
<tr>
<td>$V_{TP}$, transistor forward conduction drop</td>
<td>0.8 V</td>
</tr>
<tr>
<td>$I_{T, OFF}$, transistor &quot;off&quot; leakage current</td>
<td>1.0 mA</td>
</tr>
<tr>
<td>$V_{D}$, transistor drive voltage</td>
<td>10-15 V</td>
</tr>
<tr>
<td>$\beta$, chopper transistor current gain</td>
<td>10</td>
</tr>
<tr>
<td>$\tau_{T}$, transistor turn on time</td>
<td>0.25 μsec</td>
</tr>
<tr>
<td>$\tau_{D}$, diode switching time</td>
<td>&lt;0.1 μsec</td>
</tr>
<tr>
<td>$\tau_{DI}$, period of diode current</td>
<td>2 μsec</td>
</tr>
<tr>
<td>$\tau_{IT}$, period of transistor input current</td>
<td>7 μsec</td>
</tr>
<tr>
<td>$N$, number of capacitors or diodes in CDN</td>
<td>8</td>
</tr>
<tr>
<td>$V_{in}$, input voltage</td>
<td>130 V</td>
</tr>
<tr>
<td>$f$, operating frequency</td>
<td>70 kHz</td>
</tr>
</tbody>
</table>
Figure 1. - Transformless capacitor diode voltage multiplier DC-DC converter. Either $V_{II}$ or $V_{2I}$ can be zero or chosen arbitrarily within component ratings.

Figure 2. - Efficiency versus added capacity. Output power, 60 watts. $C_u = 1 \mu F$
Figure 3. - Efficiency versus output power. High capacity diodes, 25 PF; low capacity diodes, 7 PF.