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CAMERA MEMORY STUDY

for

LARGE SPACE TELESCOPE

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16. Abstract The purpose of this study is to develop recommended specifications for a memory system to be used as the storage media for camera detectors on the Large Space Telescope (LST) satellite. Detectors with limited internal storage time such as intensities charge coupled devices (ICCD) and silicon intensified targets (SIT) are implied. The study reports on the general characteristics of different approaches to the memory system with comparisons made within the guidelines set forth for the LST application. Priority ordering of comparisons is on the basis of cost, reliability, power, and physical characteristics. Specific rationales are provided for the rejection of unsuitable memory technologies. A recommended technology is selected and used to establish specifications for a breadboard memory. Procurement scheduling is provided for delivery of system breadboards in 1976, prototypes in 1978, and space qualified units in 1980.			
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## PREFACE

To resolve the multiplicity of conflicting claims made by proponents of competing memory technologies and thereby select the most cost-effective, lowest risk, and highest performance storage media for near term (3-to-5 years) spacecraft and satellite memory applications, NASA Goddard undertook sponsorship of the present agency independent study of camera memory technologies applicable to the large space telescope (LST). Performance of this study effort was by personnel at the Westinghouse Systems Development Division in Baltimore, Maryland. This report presents the final technical results, conclusions, and recommendations secured from the study.

The full spectrum of memory technologies seen as potential candidates for the LST application are surveyed initially. Information is presented from an extensive literature search, attendance at memory technical meetings, and phone conversations with and visits to personnel and organizations having expertise in the respective technologies. Through this effort the field of memory technologies is narrowed to four prime candidates. These include magnetic bubbles, charge coupled devices (CCD), N-channel metal oxide semiconductors (N-MOS), and nitride interfaced MOS (MNOS).

A detailed investigation of each prime candidate is conducted to determine (1) the state of development, (2) potential of meeting the LST time scale and memory system requirements, (3) associated problems and limitations, and (4) probable NASA development investment necessary. In support of this work, tentative memory configurations are generated using each of the prime technologies to facilitate a series of system trade-off studies. Individual and comparative evaluations of the prime candidates are made based on their potential for the application, relative cost, inherent reliability, energy consumption, and physical characteristics.

Two distinctly different memory systems are treated in this respect. The first, designated system "A", has a capacity of 32,768 hexadecimal words (524 K-bits). It is configured to serve as the storage media for the dual 100 x 160 element ICCD detectors presently being developed for LST-1. The second unit, system "B", has a capacity of 262,144 hexadecimal words (4.2 M-bits) and is intended to serve as the data memory for 500 x 500 element cameras like those being projected for LST-2.

With all factors considered, it is concluded that the volatile N-MOS technology best meets the low-risk/low-cost requirements of system A; but that the nonvolatile MNOS technology is better able to fulfill the higher reliability needs of system B. Accordingly, it is recommended that commercially available 4 K-bit N-MOS RAM chips be used in system A, and that 8 K-bit MNOS BORAM chips be pursued for system B. Detailed specifications are included for the procurement of a system A breadboard in 1976; and delineation is made of the probable development schedule for flight hardware by 1980.

## TABLE OF CONTENTS

1.0	INTRODUCTION	1-1
1.1	<u>Study Format</u>	1-2
1.2	<u>LST Application</u>	1-5
1.3	<u>Results Summary</u>	1-11
2.0	PROGRAM DISPOSITION	2-1
2.1	<u>Memory Objectives</u>	2-2
2.2	<u>Functional Requirements</u>	2-5
2.3	<u>Interface Definitions</u>	2-10
3.0	TECHNOLOGY EXAMINATION	3-1
3.1	<u>Candidate Assimilation</u>	3-4
3.2	<u>Preliminary Screening</u>	3-6
3.3	<u>Prime Investigation</u>	3-13
	3.3.1 Bubble	3-14
	3.3.2 N-MOS	3-22
	3.3.3 CCD	3-28
	3.3.4 MNOS	3-39
4.0	RELIABILITY EVALUATION	4-1
4.1	<u>Modeling Approach</u>	4-2
4.2	<u>Feasibility Analysis</u>	4-11
	4.2.1 System A	4-13
	4.2.2 System B	4-15
5.0	SYSTEM CONSIDERATION	5-1
5.1	<u>Storage Concepts</u>	5-2
5.2	<u>Device Alternatives</u>	5-8
	5.2.1 N-MOS	5-9
	5.2.2 CCD	5-24
	5.2.3 MNOS	5-35
5.3	<u>Application Constraints</u>	5-44
	5.3.1 Dissipation	5-45
	5.3.2 Radiation	5-49
	5.3.3 Functionality	5-53
6.0	PERORATION	6-1
6.1	<u>Technology Selections</u>	6-2
6.2	<u>Design Suggestions</u>	6-5

6.2.1 System A	6-6
6.2.2 System B	6-20
6.3 <u>Procurement Estimates</u>	6-24
APPENDICES	
A - Developmental Breadboard Specification	A-D
B - Program Statement of Work	A-1/A-12
C - Unsuitable Memory Technologies	B-1/B-6
D - Westinghouse MNOS BORAM 6001	C-1/C-18
	D-1/D-10
Glossary	E-1
References	F-1
Bibliography	G-1

## LIST OF ILLUSTRATIONS

### Section 1:

- (p. 3) 1. Camera Memory Study Plan
- (p. 6) 2. Camera System Hardware Definition Diagram
- (p. 7) 3. LST Orbital Timeline Orbit Constraints
- (p. 9) 4. Mapping Correction of Memory Capacity Limit Effects

### Section 2:

- (p. 6) 1. Camera System Photoelectron Event Counting Performance Envelopes
- (p. 10) 2. Camera Memory "Black Box" Diagram

### Section 3:

- (p. 2) 1. Memory Technology Survey Plan
- (p. 15) 2. Simplified Bubble Memory Device Concepts
- (p. 17) 3. Magnetic Bubble Materials "Size-Velocity" Band
- (p. 23) 4. N-MOS Memory Transistor Cell Structure
- (p. 29) 5. Cross-Sectional Structure of Two-Phase Surface Channel CCD
- (p. 40) 6. Unscaled Cross-Section of MNOS Memory Transistor

### Section 4:

- (p. 16) 1. System B Reliability Versus Mission Time

### Section 5:

- (p. 3) 1. First-Order Camera Memory Functional Concept Diagram
- (p. 5) 2. Data Word Memory System Structures
- (p. 5) 3. Data Block Memory System Structures
- (p. 10) 4. Random Accessed N-MOS Memory Chip Functional Diagram
- (p. 15) 5. Random Accessed N-MOS Data Storage Hierarchies

(section 5 cont.)

- (p. 21) 6. Alternate N-MOS System A Power Requirements
- (p. 22) 7. N-MOS System A Storage Power Boundaries
- (p. 23) 8. N-MOS System B Storage Power Boundaries
- (p. 25) 9. Track Accessed CCD Memory Chip Functional Diagram
- (p. 25) 10. Parallel Loop CCD Memory Chip Functional Diagram
- (p. 29) 11. Track Accessed CCD Data Storage Hierarchies
- (p. 29) 12. Parallel Loop CCD Data Storage Hierarchies
- (p. 36) 13. Block Accessed MNOS Memory Chip Functional Diagram
- (p. 39) 14. Block Accessed MNOS Data Storage Hierarchy
- (p. 46) 15. Comparison of Alternate System A Power Budgets
- (p. 47) 16. Comparison of Alternate System B Power Budgets
- (p. 50) 17. Partical Dose Rates Verse Aluminum Shield Thickness for LST
- (p. 56) 18. 4K/N-MOS RAM Based SECOR ELSEG
- (p. 59) 19. Simplified Representation of Error Exorcism Principle

Section 6:

- (p. 8 ) 1. Functional Block Diagram for N-MOS System A Camera Memory
- (p. 10) 2. Consensus 4K/N-MOS RAM Minimum Read-Modify-Write Cycle
- (p. 13) 3. N-MOS System A RMW Multiplexed Adder Timing Diagram
- (p. 16) 4. System A Conceptual Mechanical Configuration
- (p. 21) 5. Functional Block Diagram for MNOS System B Camera Memory
- (p. 21) 6. Data Latch and Adder Circuitry
- (p. 22) 7. MNOS System B Camera Memory Timing Sequence

(list of illustrations continued)

Appendix A:

- (p. 5) 1. Spacecraft Sensor Instrument Memory Subsystem
- (p. 6) 2. Sensor Instrument Memory Electrical Interface

Appendix B: (none)

Appendix C: (none)

Appendix D:

- (p. 4) 1. BORAM 6001 Chip Block Diagram
- (p. 7) 2. BORAM 6001 Read-Modify-Write Cycle
- (p. 9) 3. BORAM Microcircuit Physical Package
- (p. 10) 4. MNOS Microcircuit Functional Organization

## LIST OF TABLES

### Section 1: (none)

### Section 2:

- (p. 2) 1. Memory Technology Evaluation Guidelines
- (p. 9) 2. Camera Memory Guideline Requirements
- (p. 13) 3. Camera Memory Functional Modes

### Section 3:

- (p. 5) 1. Assimilated Memory Technology List
- (p. 7) 2. Order of Magnitude Parameters of Selected Technologies
- (p. 10) 3. Adequacy of Technologies for Camera Memory Use
- (p. 21) 4. Cost Estimate for  $10^8$  Bit Bubble Memory
- (p. 21) 5. Anticipated Characteristics of Bubble Systems
- (p. 26) 6. Physical Parameters of MOS Memory Products
- (p. 33) 7. Physical Parameters of CCD Memory Die
- (p. 33) 8. Area Utilization of CCD Memory Die
- (p. 34) 9. Comparison of CCD and N-MOS Die Parameters
- (p. 48) 10. Equivalently Processed Cell Areas of Alternate Technologies

### Section 4:

- (p. 3) 1. MOS Failure Rate Modeling Terms
- (p. 5) 2. MOS Chip Failure Rates In Space Environment
- (p. 8) 3. Reliability Modeling Terms
- (p. 14) 4. System A Single Section Failure Rate Budget

### Section 5:

- (p. 10) 1. 4K/N-MOS RAM Sources
- (p. 12) 2. Guaranteed Specifications for Standard 4K/N-MOS RAM's

(list of tables continued)

- (p. 27) 3. Compendium of Announced CCD Memory Chip Specifications
- (p. 34) 4. Alternate CCD Camera Memory Characteristics
- (p. 36) 5. Projected 8 Kbit MNOS Memory Chip Specifications

Section 6:

- (p. 18) 1. 4K/N-MOS RAM Based System A Characteristics
- (p. 23) 2. 8K/MNOS BORAM Based System B Characteristics
- (p. 24) 3. Estimated Memory System Costs and Program Durations

Appendix A:

- (p. 7) 1. SIM Functional Mode Requirements
- (p. 10) 2. Sensor Instrument Memory Characteristics

Appendix B: (none)

Appendix C: (none)

Appendix D:

- (p. 5) 1. Westinghouse BORAM 6001 MNOS Chip Specifications

## 1.0 INTRODUCTION

The purpose of this study is to identify memory technologies suitable for use as high-speed-access storage media for camera detectors during space missions. Detectors with limited internal storage time such as intensified charge coupled device (ICCD) and silicon intensified target (SIT) cameras are implied. The study reports on the general characteristics of different approaches to memory implementation. Technologies are compared in the context of the Large Space Telescope (LST) application, and specific reasons are given for the rejection of alternatives. Information obtained from the study is used to establish a specifications guide for procurement of spacecraft memory systems that can have breadboard units produced in the near future.

The purpose of this section is to provide a degree of familiarity with the background and orientation of the respective investigations, and to summarize the study results. The items covered include an overview of the study procedures followed, a review of application considerations for the LST camera memory, and a general description of the findings made for sensor instrument memories used on space missions. Although the directives of the effort are guided by the memory needs of the LST satellite, the results obtained appear to be directly extrapolateable to numerous other spacecraft which are under active consideration.

## 1.1 Study Format

The organizational sequence of investigations undertaken during the camera memory study is based on the directives set forth in NASA's original statement of work (SOW — see Appendix B). The main thrust of this effort consists of a survey of memory devices capable of operating in conjunction with an imaging device and an associated data processor. Detectors with which it is required that operation be assured are short internal storage time structures such as Intensified Charge Coupled Devices (ICCD), Silicon Intensified Targets (SIT), IR bolometers, UV linear arrays, and photomultipliers. Technology and system alternatives are judged from the following four criteria, in the order of priority given:

- Cost
- Reliability
- Power
- Physical (size/weight)

Included in the cost criteria is a relative maturity consideration which strongly influences development investment needed. Information obtained from the study is used as a guide in establishing design specifications for spacecraft memory systems which can be produced in breadboard form in the near future.

Figure 1-1 denotes the principal elements of the approach taken to the camera memory study. Initial phases of the effort encompass both a technology survey and an evolution of system techniques. The survey includes a broad literature search which is used to identify the most promising technologies. This is followed by a more detailed inquiry into a group of "prime candidate" technologies. Activities during this phase included interviews with and visits to key personnel in selected companies active in the development of the respective technologies, and the assimilation and coordination of supplemental information supplied by NASA.

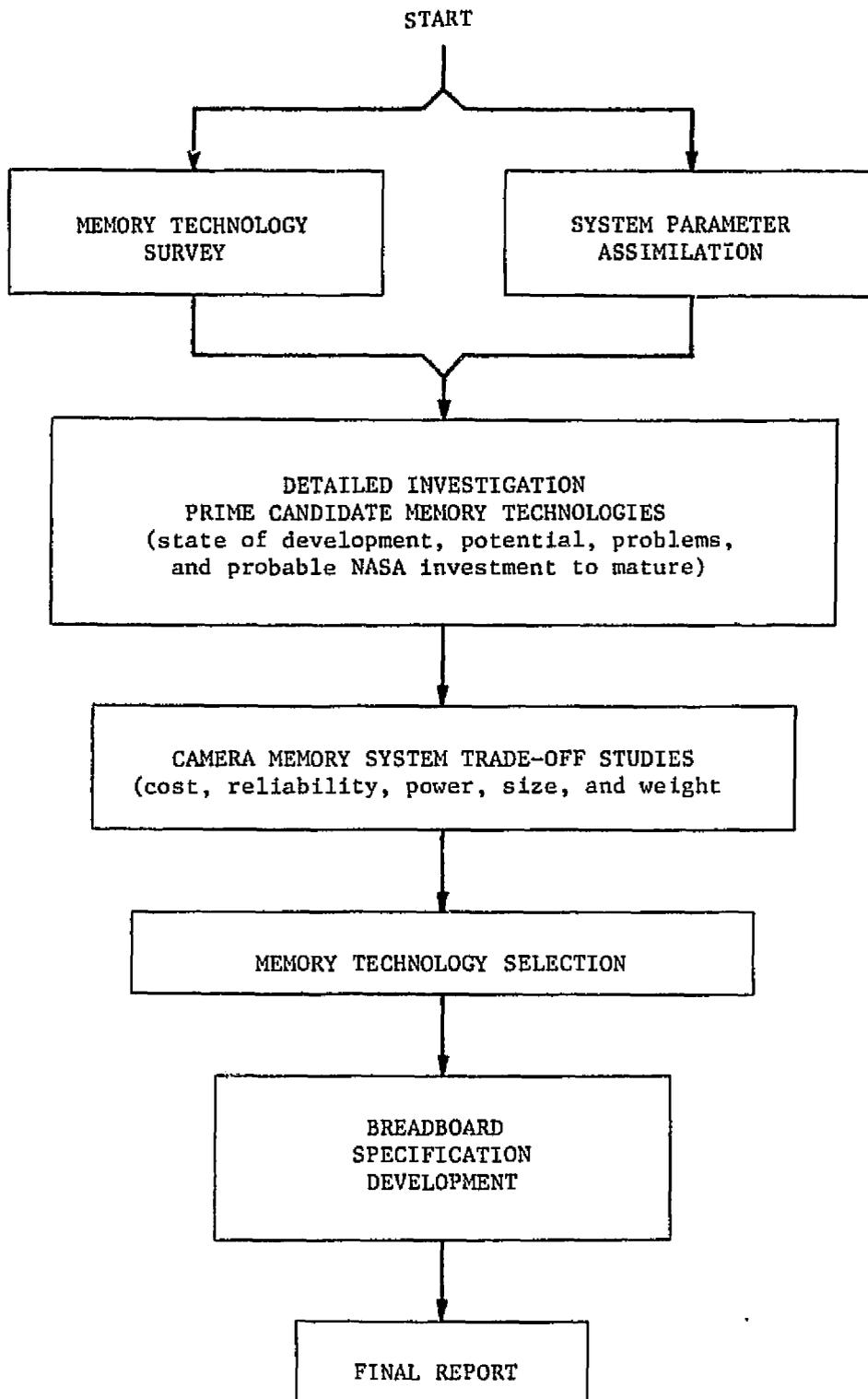


Figure 1-1. Camera Memory Study Plan

Pursuant to this, a series of interrelated system studies is conducted to establish the advantages and disadvantages of each technology option. Care is exercised throughout this phase to consider the impact of technology parameters on system and subsystem designs, and to ascertain the true performance versus cost trades of those designs. Conclusion of this work is followed by delineation of the final technology choices and preparation of the breadboard system development specifications.

For purposes of this study, NASA's time frame of interest for the production of test and evaluation breadboard units is 1976, with projections for flight hardware to follow by 1980. Accordingly, the recommended memory approach provides a breadboard of conceptual design which reflects 1976 state of the art, not necessarily present day data storage capabilities. Throughout the study, technologies are compared in the context of the LST application. Technical interchanges with NASA personnel and NASA consultants provided the required background information on the mission parameters.

## 1.2 LST Application

The Large Space Telescope (LST) in its simplest conceptualization is a satellite which has been especially configured and instrumented to provide earth bound astronomers with remote, sensitive eyes capable of observing distant planets and star patterns unobstructed by the earth's atmosphere. Presently at least two LST's are foreseen as being launched into low earth orbits in the late 1970's to early 1980's. The space shuttle will be used for both initial launch and subsequent servicings on a one to two year mission time basis. The types of sensors under consideration or being developed for the LST are varied and continually changing, and a final selection has not been made. It is projected, though, that on LST-1 the largest photon counting systems and imaging arrays will have on the order of 32K pixels (e.g., as might be secured with dual 100 x 160 pixel ICCD cameras). On LST-2 and all subsequent flights, cameras containing 250K (500 x 500) or possibly 1M (1000 x 1000) pixels are being anticipated.

A scientific instrument package (SIP) will house the full complement of sensors for the LST, while a separate service and support module (SSM) oversees the operation and safety of the spacecraft. Accordingly, it appears<sup>(1)(2)</sup> that unique, individually programmable processors should be supplied for the SIP and the SSM. To abrogate the consideration of factors which are irrelevant to the viability decision on a memory technology, the discussions in this section will be based on the assumed further division of storage within the SIP into two distinct parts consisting of a camera (or scientific instrument) memory and a central processor memory. This arrangement of structured modularizations of the spacecraft subsystems has the desirable attribute of introducing a set of clean, well defined hardware interfaces which should lead to simpler and less costly hardware and software

developments. As indicated in Figure 1-2, the camera system is perceived as consisting of five principal blocks (counting I/O interfaces separately). Any one of the multiplicity of camera (or sensor) units is selectively activated and its signals fed through the endo-system interface to the camera memory during data accumulation periods. Data readout is accomplished through the exo-system interface which steers the stored data to the proper down

\* Camera Memory Only is Given Detailed Consideration in this Report

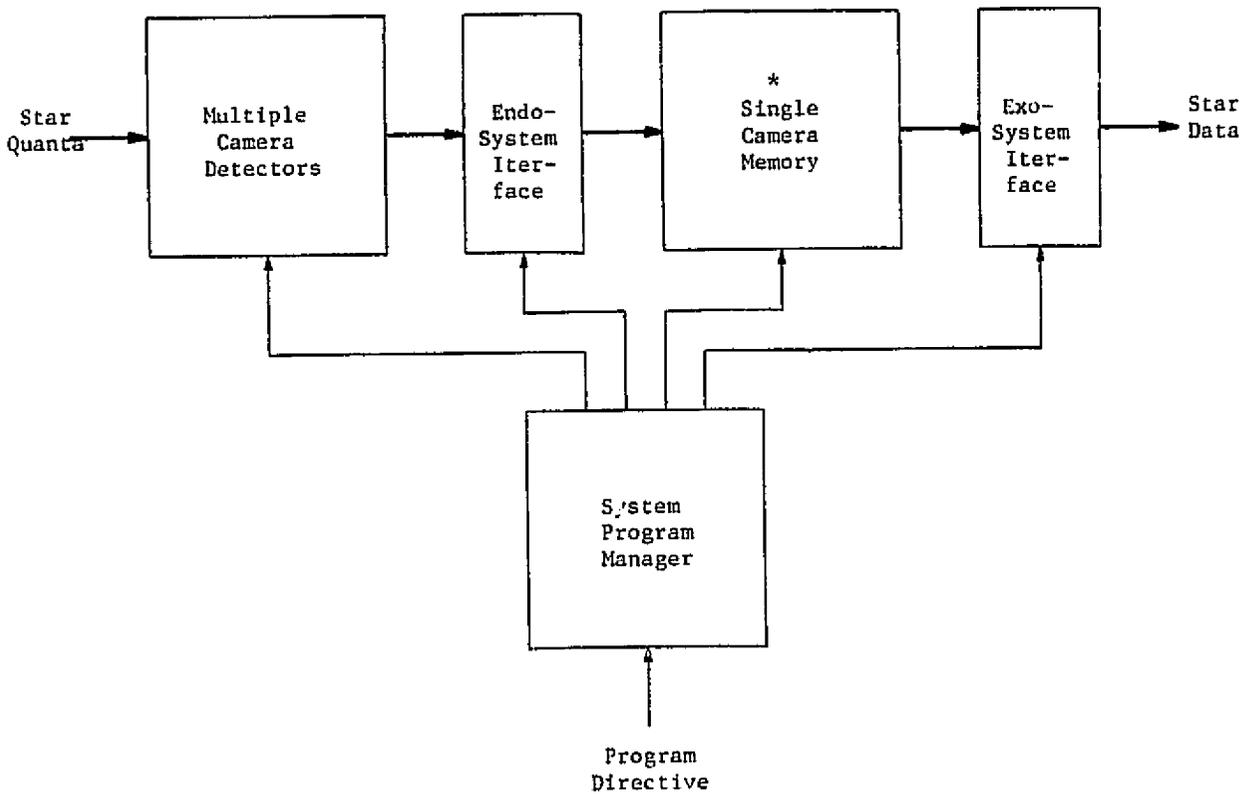


Figure 1-2. Camera System Hardware Definition Diagram

stream usage unit (such as the down-link rf transmitter or the on-board tape recorder). These I/O operations, as well as Copernicus or ERTS-B type fault detection and isolation routines, are the responsibility of the SiP's camera system program management section (not the memory module itself), with overall program directives being provided from the SSM either automatically or under ground control.

All electronics in the LST, including of course the camera memory, will be subjected to launch shock and the radiation environment of low earth orbits. The orbital time table, calling for approximately 96 minute cycles, is depicted in Figure 1-3 along with representative radiation levels expected to be encountered. Postulated astronomical observations carried out with the photon counting cameras<sup>(1)(3)</sup> may involve pixel event rates of up to 10 events/pixel/second. Minimization (beyond the three sigma level) of the Poisson

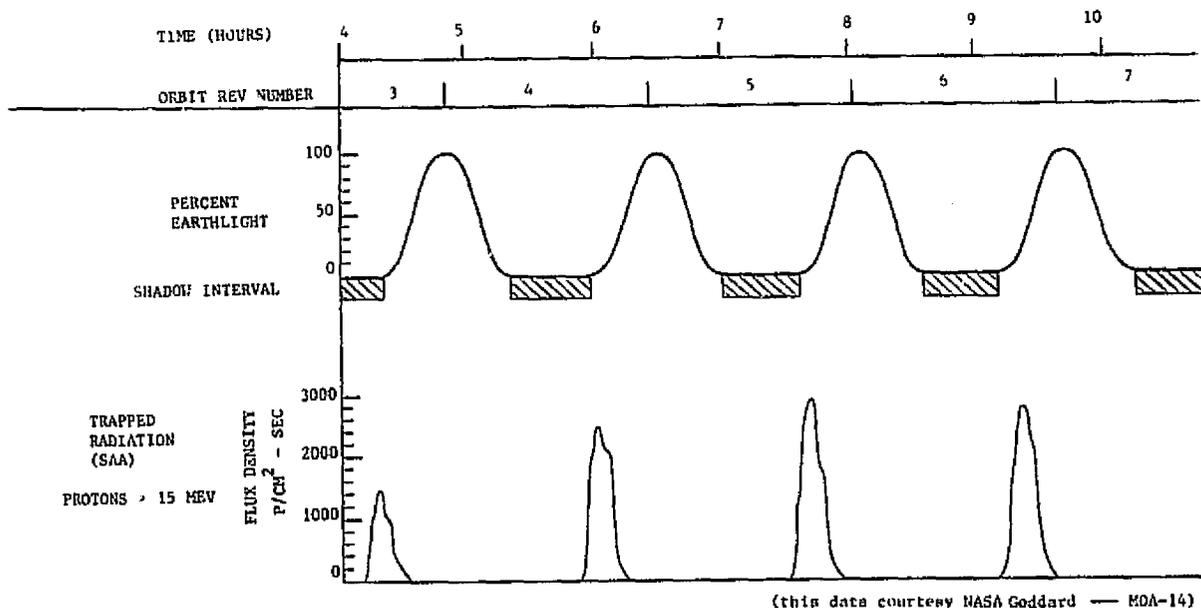


Figure 1-3. LST Orbital Timeline Orbit Constraints

distributed probability of multiple events piling up during a pixel framing period calls for the camera scanning rates to be adjusted so that the average pixel event density is held to around 0.1 event/pixel/frame. From this it follows that the camera frame rates would have to be 100 frames/second. And this in turn implies a pixel scanning rate for LST-1 (having dual 100 x 160 arrays) of 3.2 MHz, and for LST-2 (having a 500 x 500 array) of 25 MHz. This latter figure is expected to be cut back to around 10 MHz by practical considerations of sensor readout. The camera memories will accordingly be assumed to possess the capability of accomplishing their data update and refiling operations (read-modify-restore cycles) in about 300 nanoseconds for LST-1 and in about 100 nanoseconds for LST-2. Dead-time corrections needed for near saturation event burst periods can then be considered solely a function of the sensor plane characteristics.

To attain non-overfill photometric counting accuracies of within less than 0.5% deviation, a storage word size of around 16 bits assigned to each pixel site has been shown<sup>(3)(4)</sup> to be adequate. Single, centroided event data incrementing will occur with Boksenberg-type<sup>(5)</sup> camera systems. Analog imaging cameras, on the other hand, may output four or more A/D converted data bits per pixel event. Overfill of storage locations, producing cratered count accumulation distributions like that depicted in Figure 1-4, will not require additional on-board processing but rather will be recognized and compensated by count contour mapping computer programs at ground installations. Window algorithms around selected portions of a sensor viewing area have been considered and could be used to reduce either the total storage capacity or the effective average event rate requirement imposed on the

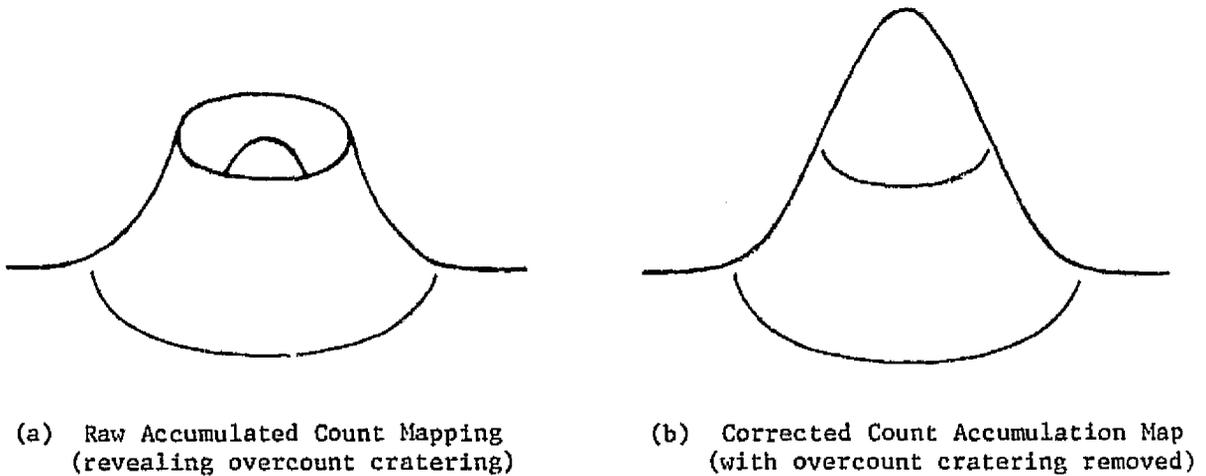


Figure 1-4. Mapping Correction of Memory Capacity Limit Effects

camera memory. Data handling soft error rates in the transmission down-link are expected to be on the order of  $10^{-5}$  errors/bit. A comparable level for the memory system, allowing for the difference in number of times that the data must be handled, would be on the order of  $10^{-10}$  errors/bit for LST-1 and  $10^{-11}$  errors/bit for LST-2.

The minimum mission time for the LST will be greater than 1 year. With the sensors having no more than an 89% reliability figure for this period, the memory must have better than a 95% capability to achieve the desired 85% probability of success for the composite camera system. Allowable degradation in the system consists of the loss of one camera (out of the two duplicates) and/or its associated storage section on LST-1, and the loss of up to 10% of the camera pixels or storage sites on LST-2. These systems will generally

function at around a 35% active usage time duty cycle, resting in a powered down condition for 65% of the time. Temperature of the SIP will be held at a nominal 20°C by thermal management heaters during flight, but may reach 60°C prior to launch or during shipment. Power requirements for the memory are expected to vary with event data rate. The target power budget allows 10 Watts continuous dissipation for either system, and peak burst levels of 30 Watts for LST-1 and 50 Watts for LST-2. The volume and mass of these memories are to be held to within 16 liters and 5 Kg, respectively, for flight qualified units. Memory designs must incorporate sufficient flexibility to accommodate a variety of cameras and allow for in-flight adjustments in sensor oriented parameters and control algorithms.

### 1.3 Results Summary

An extensive assortment of data was collected over the course of the camera memory study. So far as possible every item relevant to equitable comparisons between alternatives is included in this report, along with sample illustrations of how specific comparisons are made and the cumulative results obtained. At the outset of the study the data requirements, detector characteristics, and memory concepts for the LST were still in a formative stage. Refinement and extension of the preliminary system objective was secured through a series of technical interchanges with NASA personnel and consultants as additional information became available. This permitted establishing a mutually agreeable set of concise, definitive, and inclusive guideline requirements for the development of an LST camera memory. The evolutionary context of these guidelines is discussed in Section 2.

During the initial phases of this study an extensive search was made of published literature on every conceivable type of memory device to determine the full range of technologies potentially applicable in spacecraft data storage units. The bibliography and reference listings found at the end of this report have been culled from the broad range of information sources encountered. They include publications of both historical and advanced state-of-the-art significance, and collectively present a comprehensive overview of storage device developments. Using the data contained in these sources, Section 3 collates the capabilities and limitations of some thirty diverse memory technologies and evaluates them in light of the LST requirements.

Based on considerations of their fit to the application, relative maturity, and economic drivers, four technologies are selected for detailed

examination. The remainder are shown to be grossly unsuitable, with the most frequent bases for rejection being:

- lack of developmental maturity, in the case of new technologies, like silicon-on-sapphire (SOS) and integrated injection logic (I<sup>2</sup>L);
- insufficient economic drivers, in the case of cost-ineffective technologies like ferroelectric and magnetostrictive thin films; and
- inadequate reliability capability, in the case of mechanical motion technologies like tape and disk recorders, or high vacuum technologies like optical and electron beam addressed memories (OBAM and EBAM, respectively).

Treatment of specific reasons for the nonselection of a particular technology alternative is relegated to Appendix C.

Within the group of four "prime" technologies which are given serious attention, an even split exists between volatile and non-volatile types. The list of "primes" consists of

- magnetic Bubble (Bubble)
- Charge Coupled Device (CCD)
- N-channel MOS (N-MOS)
- Nitride interfaced MOS (MNOS)

with CCD and N-MOS being volatile in nature while Bubble and MNOS produce nonvolatile stores. Investigation of the fundamental characteristics and developmental directives of these technologies quickly reveals that an unresolvable mismatch exists between bubble type stores and the needs of high speed memories designed to interface with spaceborne photodetectors. Interviews with workers active in the development of bubble systems -- such as Dr. Robert Stermer at NASA, Langley -- confirm this premise. In particular, bubble memories are being pursued as replacements for spacecraft tape recorders. As a consequence, they exhibit insufficient speed capabilities to meet the LST camera memory requirements.

As work progressed on the study, it was determined that the data storage requirements on LST-1 would be significantly different from those encountered on subsequent flights. Accordingly, a decision was made to treat two alternate storage capacity systems. The general characteristics of different approaches to memory implementation are established for these two systems and a check made of the feasibility of achieving reliable operation from each. From this it is concluded that excellent reliability levels — greater than 95% probability of success for 1 year missions — can be provided by "simplex" (i.e., nonredundant) forms of a spacecraft memory using a volatile technology such as N-MOS so long as the storage capacity is no greater than about  $10^5$  bits. Volatile technologies can be employed in memories having up to  $10^7$  bits, but will require some form of redundancy (such as Hamming code error correction circuitry) to maintain acceptable reliability levels. Above  $10^7$  bits a nonvolatile technology like MNOS appears essential to the production of practical storage devices for applications calling for long (> 2 year) mission times. Further elucidation of these points is presented in Section 4.

To provide a working base for high-order comparisons, macroscopically equivalent preliminary memory organizations are evolved for the three remaining prime technologies (viz., CCD, N-MOS, & MNOS). Using confirmed parameters of memory devices that have been produced with each technology — and are known unequivocally to be scheduled for mass production by early 1976, in the case of volatile devices, or by 1978, in the case of nonvolatile devices — analytical examinations are made of the power dissipation levels of the respective memory modules. Owing to their serial I/O nature, memories built with the CCD or MNOS technologies exhibit constant energy requirements. The N-MOS technology, on the other hand, produces a random accessed memory (RAM)

in which the power drain varies as a direct function of the stored data updating rate. Findings from these calculations indicate that the CCD technology consumes the greatest average power and is marginal at best when considered in the context of the LST application. Details of the individual power analyses cited here can be found in Section 5.

Through the foregoing process of elimination, this study concludes that the N-MOS technology should be used to realize spacecraft camera memories of up to approximately  $10^6$  bits (like that for LST-1), because it appears to be the lowest risk, most cost-effective option available. Chips having 4096 bits are in fact already available in quantity from multiple sources at low prices, and over the next few years the pricing structure is expected to become even more advantageous. For systems requiring storage capacities of greater than  $10^6$  bits or unattended mission times of over 2 years, though, it is recommended that the MNOS technology be employed. From a production volume and cost standpoint, MNOS is presently less mature than N-MOS, but its potential for cost reduction is significantly greater. Furthermore, within 3 years 8192 bit MNOS chips suitable for high capacity memories (such as will be needed on LST-2 and other companion satellites) should be available in volume production for Department of Defense (DOD) requirements from at least two major semiconductor houses. For reference, the fundamental characteristics of the MNOS 8 Kbit BORAM device being developed by Westinghouse are described in Appendix D.

Complete listings of the technology recommendations and suggested system implementations are given in Section 6. Also included are cost and scheduling estimates applicable to an orderly memory development effort.

These estimates are based on a three phase program which leads successively to the production of a breadboard, then a prototype, and finally a flight qualified memory unit, with the full development schedule spread over a three-to-four year period. A detailed design specification for a 512 Kbit memory which can be procured in breadboard form in the near future is presented in Appendix A.

## 2.0 PROGRAM DISPOSITION

As the camera memory study progressed, the investigational directives were revised to be more explicit and the breadth of the study was narrowed to specific design considerations. Initially there existed only a tentative formulation of the operational requirements that should be sought in high speed sensor instrument memories which are to be used on extended or on attended space missions. To establish a starting base from which gross viability assessments of technology alternatives could be made, the planning stage needs projected for the Large Space Telescope scientific instrument package camera systems were adopted. Coordination of the findings made during this study with updated LST application information made available by NASA through its detector working groups and consultants permitted these original design objectives to be refined into a cohesive listing of spacecraft sensor instrument memory guideline characteristics which can be readily provided by 1976 level state-of-the-art storage media capabilities — without the need of excessive funding for technology maturation or application grooming.

## 2.1 Memory Objectives

At the outset of this study it was understood that flexibility would have to be maintained as to the parameters of the desired memory system. The reason for this is simply that the memory design objectives available at that time were generated solely from preliminary data supplied by early LST planning groups and had to be made somewhat abbreviated and imprecise to avoid arbitrarily excluding potentially viable device or design alternatives. These objectives, listed in Table 2-1, are therefore limited in utility to first-order evaluation guidelines.

Table 2-1. MEMORY TECHNOLOGY EVALUATION GUIDELINES

Characteristic	Guideline Value
volume	16 liters
weight	5 kilograms
storage capacity	$10^7$ bits
Power (continuous)	10 watts
power (data burst)	50 watts
reliability	2 years
data rate	$10^7$ bits/sec
data access	serial anticipated parallel to memory subsections via a high speed buffer will be permitted.

Points of contention that arise with regard to these guidelines deal with meaningful interpretation of the reliability parameter and amicable settlement of the classical parametric tug-of-war which features storage capacity and data rate bucking power consumption. The disparity with the reliability value cited in Table 2-1 is that it seems to be describing a memory MTBF (mean time between failure) of 2 years. If it is interpreted that way, the probability of the memory successfully completing a 2 year mission would be only 36.8% — a rather undesirable situation for a spacecraft. Obviously a different means of specifying reliability must be employed.

The correct procedure for defining system reliability is to specify two basic parameters:

- probability of success desired
- mission time of spacecraft

As supplements to these fundamental characteristics, stipulation should also be made of the operational duty factor (i.e., percentage of total mission time that system is powered up) and the maximum number and type(s) of storage site and/or system failures which can be tolerated before the memory is considered useless (viz., definition of the mortality failure state). With this information in hand, a contractor can evaluate his system design to see whether it will meet the mission reliability requirements. Naturally the less stringently these parameters are defined, the more easily and less expensively they can be met. Caution against overspecification is therefore advisable to maintain reasonable cost levels.

With regard to the conflict indicated between capacity, speed, and power, it appears that the classical solution to this classical problem must be invoked; namely, one or the other of the diametrically opposed parameters must be relaxed slightly. This philosophy generally dictates that the memory needs of a spacecraft must be dealt with on an individual basis to facilitate reducing the storage capacity and/or data rate sufficiently to be compatible with the assigned power budget. In the case of the LST, consideration should be given to at least two different camera memories: one configured for the first LST mission, and the other outfitted for subsequent launches.

## 2.2 Functional Requirements

Working from the basic goal inputs received from the various LST working groups over the course of this study, agreement was ultimately established<sup>(6)</sup> that two distinctly different systems would be treated. The first system, designated "A", is to have a capacity of 32,768 words of 16 bits as required by the dual ICCD detectors of 100 x 160 pixels each which are currently under NASA contract development for LST-1. The second system, designated "B", is to have a capacity of 262,144 words of 16 bits and be designed to work with detectors in the general size range of 500 x 500 elements like those that are forecast for use with LST-2. Both are required to handle either Boksenberg type photon counting or binary converted analog imaging data, with the pixel scan rate for System A being no greater than 3.0 MHz and for System B being no greater than 10 MHz. Within these boundaries the astronomers using the composite camera systems will be free to choose the pixel event rate and density they desire for prescribed accuracy levels. The effect which alternate choices here have on overall system performance can be readily grasped from the event counting performance envelopes plotted in Figure 2-1.

An example of the use of these curves would be to choose pixel event rate and density parameters of 10 events/pixel/second and 0.1 events/pixel/frame. Proceeding horizontally across and vertically upward to the intersection point of these two variables it is found that the system frame rate to satisfy the chosen conditions is 100 Hz. Then, proceeding upward along the 100 Hz frame rate line to the axis intersection point reveals that the scan rate for System A would need to be just slightly over 3.0 MHz, while for System B it would need to be greater than 25 MHz. Thus,

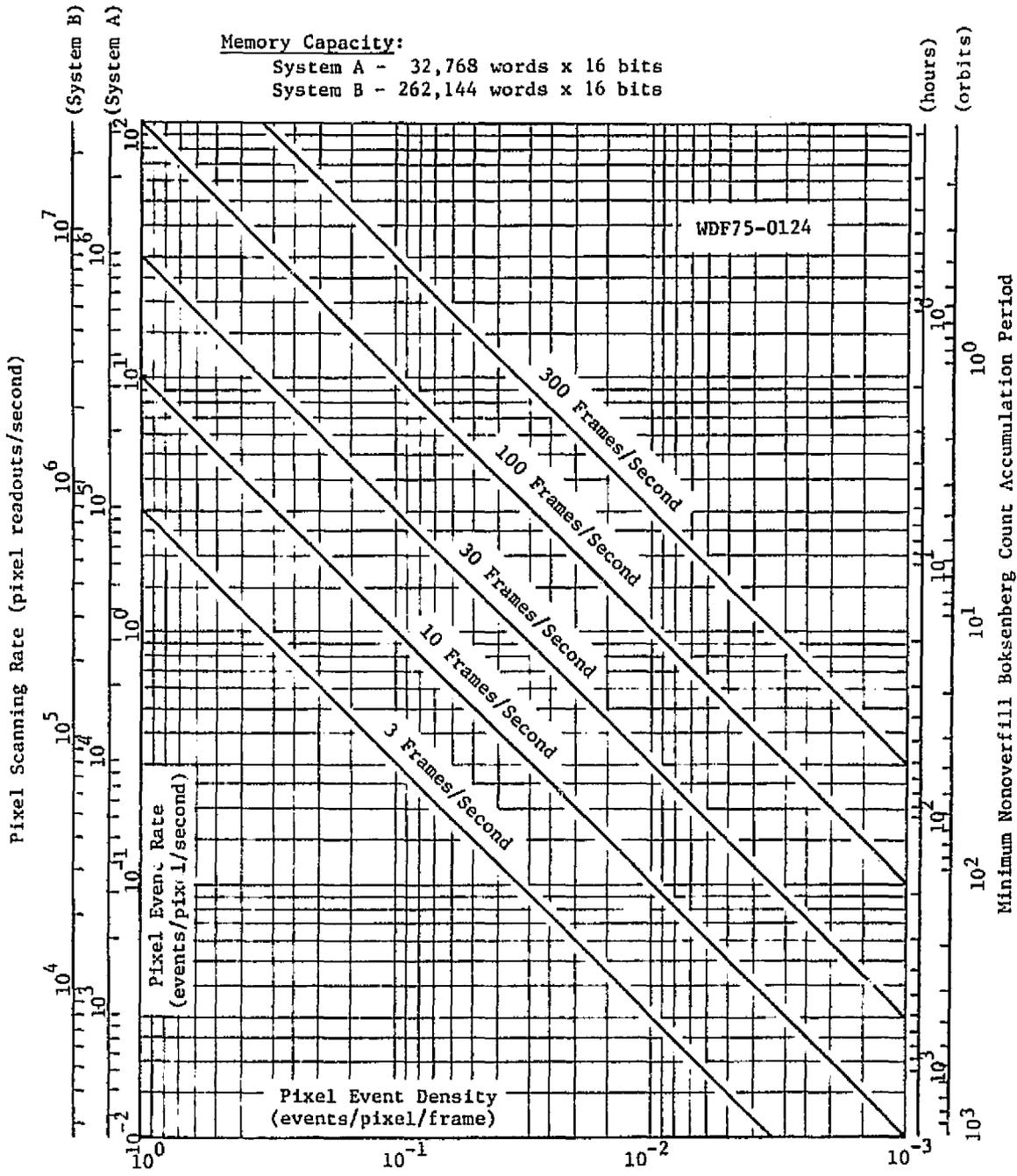


Figure 2-1  
 Camera System Photoelectron Event Counting Performance Envelopes

the originally chosen conditions could very nearly be met with System A, but they would be totally impractical with System B since its maximum scan rate is limited to 10 MHz. In this case either the original event counting parameters would have to be adjusted or a supplemental system function would have to be brought into play to place a "window" algorithm around the area(s) of interest in the detector scene so that an effective reduction in pixel capacity and scan rate could be realized. The final bit of information available from Figure 2-1 is the maximum period over which the camera system can continue to incrementally accumulate photoelectron event counts (Boksenberg-style) before reaching a storage word overflow condition for any given choice of pixel event rate. This data is based on an assumed 96 minute orbital interval and a 16 bit word size. Using our previous example of 10 events/pixel/second, the maximum nonoverflow period is seen to be slightly under 2 hours, or just slightly over 1 orbit. Accordingly, either the accumulated data should be dumped each orbit or an adjustment should be made in the pixel event rate parameter. The working astronomers will ultimately have to make the trade-off decisions necessary.

Further working group reviews of intended mission goals as they related to the original target specifications (presented earlier in Table 2-1) resulted in the remaining guideline requirements for the two memories being firmed up. System A is to be partitioned into two sections to provide a degree of modularized independence for the two detector scenes it must store. The mortality failure level for this system will be taken as that point when less than one full section is functional. No specific organization is demanded of System B, but its mortality failure point is more stringently defined as being that point when greater than 10% of the total

storage words have suffered a failure. The average continuous power for the memories is nominally set at 10 Watts for both System A and System B (with average being interpreted as that level existing when the system is handling data at 1/10th or less of its peak rate). The corresponding peak burst power limits are 30 Watts and 50 Watts, respectively, with System A processing event counts at 3.0 MHz and System B cycling at 10 MHz. Temperature rise conditions within the memory can be evaluated on the basis of the case temperature during operation being maintained between 0°C and +30°C. The I/O data format for the memories will be word serial and bit parallel for data input to the system (see Figure 1-2), but totally word and bit serial for data output from the system; with the output bit rate being comparable to the input word rate. Table 2-2 summarizes the complete list of guideline requirements assimilated for the two camera memories, including both the factors noted here and those discussed earlier regarding background development considerations.

Table 2-2

## Camera Memory Guideline Requirements

Characteristic	System A	System B
Organization (sections/memory)	2	(undefined)
Storage Capacity (words/memory)	$\geq 32K$	$\geq 250K$
Word Size (bits/word)	$\geq 16$	$\geq 16$
Data Format: Input Output	word serial/bit parallel word serial/bit serial	word serial/bit parallel word serial/bit serial
Data Rate: Peak (pixels/sec.) Average (pixels/sec.)	$3.0 \times 10^6$ $3.0 \times 10^5$	$1.0 \times 10^7$ $1.0 \times 10^6$
Power: Data Burst (Watts) Continuous (Watts)	$\leq 30$ @ 3.0 MHz $\leq 10$ @ < 300 KHz	$\leq 50$ @ 10 MHz $\leq 10$ @ $\leq 1$ MHz
Ambient: Operating ( $^{\circ}C$ ) Storage ( $^{\circ}C$ )	-10 to +40 -55 to +70	-10 to +40 -55 to +70
Soft Error Rate (errors/bit)	$\leq 10^{-10}$	$\leq 10^{-11}$
Hard Error Limit (@ mortality)	1 section	10% words
Usage Duty Factor (%)	35	35
Mission Time (years)	> 1	> 1
Reliability (% success probability)	> 95	> 95
Physical: Volume (liters) Mass (kg)	$\leq 16$ $\leq 5$	$\leq 16$ $\leq 5$
Scaleability (@ reduced reliability)	up to $\sim 10^5$ words	up to $\sim 10^6$ words
Procurement: Breadboard Flight Model	1976 1980	$\sim 1978$ $\sim 1982$

### 2.3 Interface Definitions

To facilitate equitable comparisons of memory systems evolved around divergent technologies and provide a working base from which a contractor can develop a functional system, it is necessary to establish a technology independent definition of the electrical interface conditions which the system should meet or supply. Detailed specifications regarding unique timing restrictions or particular voltage levels are not included as they tend to be highly technology dependent. Such data must be either provided by NASA or worked out between NASA and the ultimate contractor at the time of procurement.

Figure 2-2 presents the "black-box" description of the interfaces to the camera memory. Implicit in this diagram and all discussions related to the memory interface specifications is the assumed existence of a processor

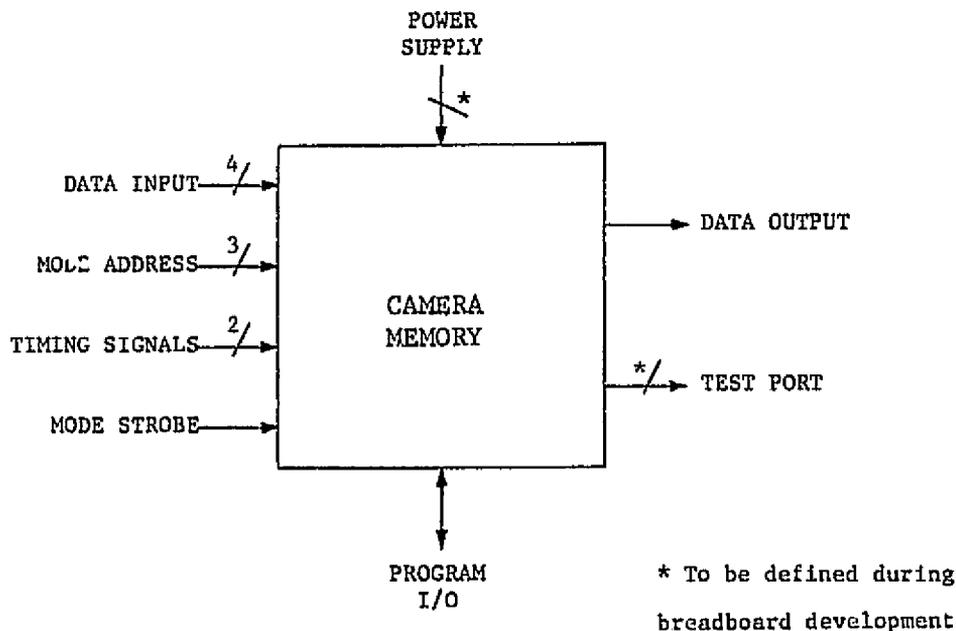


Figure 2-2 Camera Memory "Black Box" Diagram

or controller external to the memory which coordinates all elements of the camera system. In this context, reference can be made back to Figure 1-2 and the related discussion. The interface is seen to consist nominally of 7 lines (or sets of lines) with an optional eighth test port. Indirect control of memory functions is provided by the bidirectional program enter/verify line which facilitates the changing of timing parameters, address sequences, and any other operating options via a "program word" that is entered serially under control of the timing signals. Once stored in the memory's program storage section it can be read back out serially for verification, again under sequencing control of the timing signals. This arrangement provides maximum design flexibility and growth potential by virtue of the fact that the length of (number of bits in) the control word is not prespecified and can be readily adjusted to allow for future system modifications.

Data input to the memory is accomplished via a set of lines which transfer pixel event word bits in parallel. For Boksenberg type photon counting a single line would be used, but for analog imaging at least 4 (with System A) and possibly up to 12 (with System B) parallel lines could be employed between the camera A/D converter and the memory input. The format of the input data is thus word serial/bit parallel, with the word progression in both the memory and the data originating camera controlled by the timing line signals. Outputting of data takes place over a single data output line in a word serial/bit serial format with successive bits clocked out again under control of the timing signals. A totally serial output format is adopted because it minimizes the number of electrical components required, thus conserving power and enhancing reliability. No restrictions are placed

on the rate uniformity or minimum rate at which functional sequencing takes place at any memory I/O interface. The only restriction is that it cannot proceed more rapidly than the maximum memory data rate (viz., 3.0 MHz with System A and 10 MHz with System B). Allowance must be made through the timing signals for ensuring that operating sequences in the individual elements of the camera system remain in step with one another. Without this proviso, noise disturbances could cause the separate address generators in the individual subunits to independently jump cadence and result in the mispositioning of stored data.

A master clock input comprises one of the timing signals provided to the memory. Specification of this signal is necessary to ensure that the read/modify/write cycle of operations within the memory is time partitioned into the smallest time increments required to establish the necessary sequence of events. It accordingly should be an exact harmonic multiple of the fundamental data input word rate and is anticipated as being 4 to 16 times the data strobing rate, depending on specific design parameters adopted. Supply lines into the memory carry the necessary power to operate the system. The specific voltage and current levels and the number of lines involved must ultimately be settled between NASA and the system contractor. The final option specified for the memory interface is a test port. This line conceivable could prove advantages during certain self-test or externally programmed test routines. Final determination of the need for this line must be made by the contractor during development of the breadboard.

By way of the cited interface lines a full range of functional modes can be instituted for the camera memory. Direct control of the eight modes listed in Table 2-3 is provided by the three mode input lines. Considering

Table 2-3 CAMERA MEMORY FUNCTIONAL MODES

Mode Number	Mode Name	Mode Description
0	POWER DOWN	Power down all electronics except the mode circuitry and related power switches
1	ACTIVE STANDBY	Activate control and programming circuitry
2	INITIALIZE	Initialize control circuitry; and clear memory to zero if control bit in program word is set
3	ENTER PROGRAM	Enable memory to receive a serial program word on the program I/O line as clocked in by the timing signals
4	VERIFY PROGRAM	Enable memory to transmit the currently stored program word on the program I/O line as clocked out by the timing signals
5	SCAN	Enable memory operation. Increment address in response to timing signals. If input data is non-zero, add data to present contents of memory. Recycle addressing as specified by program word.
6	OUTPUT	Enable memory read operation. Beginning at first address place data bit serially on the data output line as clocked out by the timing signals
7	TEST	Enable ROM controlled self-test routine. Test sequence proceeds in response to timing signals. Test results appear on data out line and/or optional test port

them individually and in order, the POWER DOWN mode is provided to enhance the reliability of the memory. In this mode all electrical stresses are removed from the operating circuitry in the memory. Only the power switches and mode control circuitry remain active (and even the mode circuitry could be powered down if it were in the form of an electrically alterable non-volatile store). During the power down state it is not necessary to retain memory contents. The lowest level powered up mode is ACTIVE STANDBY. During

this mode the memory is fully active and all stored data is retained but no I/O operations occur. This mode may need not exist as a uniquely enterable systemological state since it can also be established as a substate of both mode 3 (PROGRAM ENTER) and mode 4 (PROGRAM VERIFY). It probably will prove more useful under laboratory conditions than during space flight. The INITIALIZE mode ensures that address counting begins at zero — or at the lowest address called for in the program word — and that all control circuitry within the memory is in the proper initial state. If a designated control bit in the program word is set, this mode will also result in the entire data storage section being cleared.

The PROGRAM ENTER mode exists solely for the purpose of changing the contents of the "program word" storage register in the memory so that a new set of functional conditions will be established for all subsequent memory operations. Before reinitiating memory operation, the PROGRAM VERIFY mode can be used to confirm that the program word stored in memory matches that transmitted. All stored data is retained whenever either of these modes are in effect, but all data I/O operations cease. Full memory operation in conjunction with a camera detector obtains during the data inputting SCAN mode. A concordant state of full memory operation in conjunction with a data consumption device exists during the data reading OUTPUT mode. The fault detection TEST mode gives the memory a means of checking the operational status of its functional parts. The actual tests can be accomplished by either a built-in self-test circuit, an on-board support processor, or a ground based processor. The approach suggested is that the memory contain a ROM self-test subroutine which can be called up, exercised, and directly

monitored by the on-board sensor instrument package (SIP) program management processor. The processor would examine the test results and report any malfunctions. The nature of the self-test circuitry is a strong function of the memory design details. Its definition is therefore made a portion of the memory development effort.

### 3.0 TECHNOLOGY EXAMINATION

In this section available technologies are reviewed for compatibility with the LST application and time frame. The respective discussions explain how the technology survey was conducted, give the decision criteria involved, and comment on the characteristics of the prime candidate technologies. Technologies considered unsuitable for use as a camera memory are commented on in Appendix C.

The procedure followed during the technology survey is summarized by Figure 3-1. The plan begins with a wide ranging literature search to compile a list of modern memory technologies with at least a remote chance of application to the LST mission. The resulting list is initially screened on the basis of gross incompatibility with the guideline requirements. Survivors of the initial screen are termed "candidate" technologies and are subjected to further detailed examinations. If certain aspect of a given technology are found to be in conflict with the LST needs, it is rejected. However, since the scope of this survey is limited to the context of the LST application, the rejection of a specific technology cannot be interpreted as an all inclusive negative commentary on its suitability for another application nor for its use in a different time frame.

Ultimately the search is narrowed to a set of "prime" candidate technologies. These are examined in the context of trial system configurations and in the light of information obtained from personal interviews with experts in the respective fields. A practical constraint of major importance in choosing a technology is the degree of supplemental investment remaining to be made to fully mature the technology. For purposes of

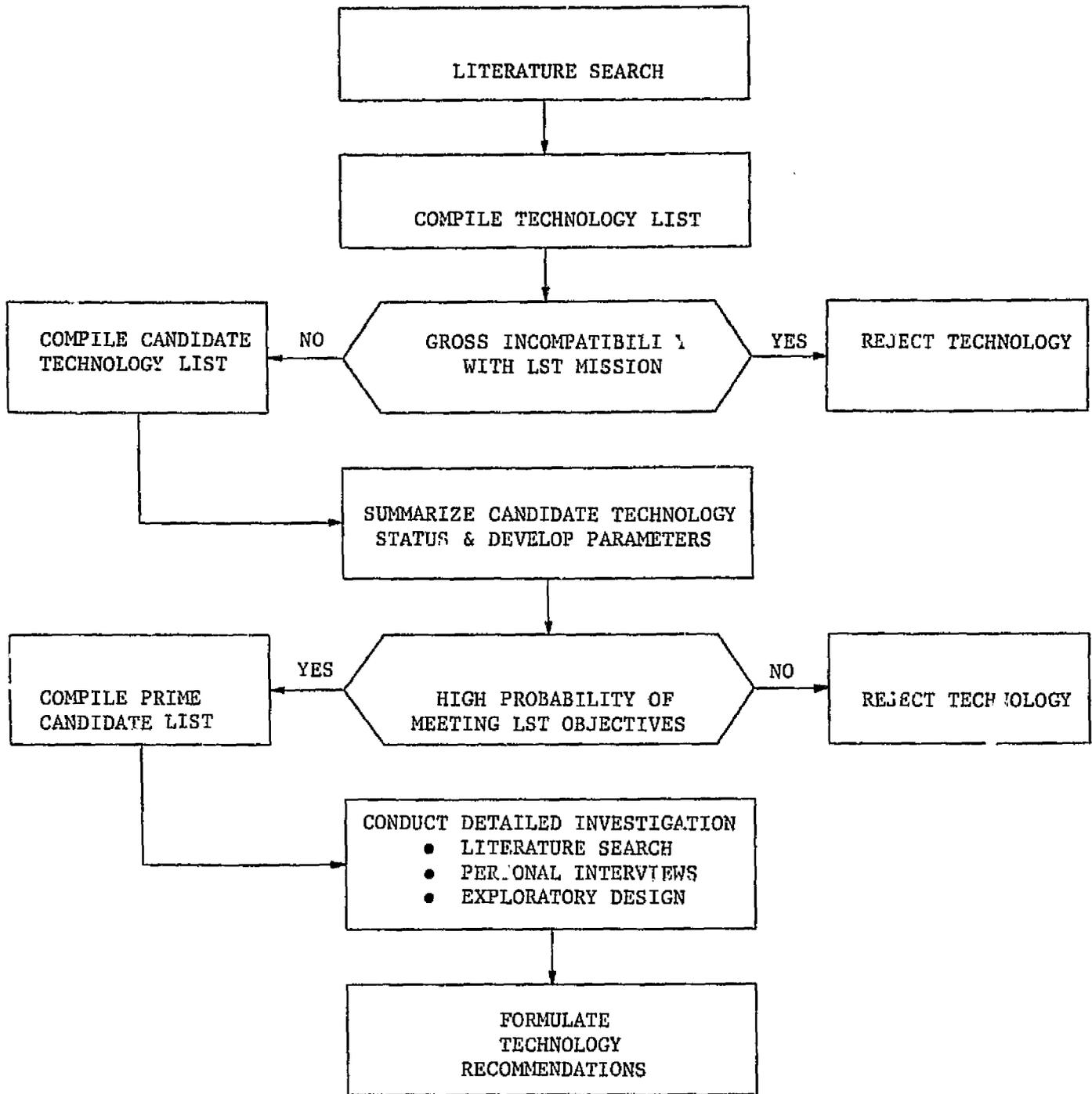


Figure 3-1. Memory Technology Survey Plan

this study, it is required that any recommended technology not involve extensive NASA funding for memory component development. Procurement funding will be limited solely to the utilization of established components in the development of a camera memory system. Recommended Technologies must have clearly identifiable economic driving forces independent of the camera memory requirement.

### 3.1 Candidate Assimilation

Almost every physical phenomenon which exhibits two or more stable states has been considered, at one time or another, as a possible memory technology. An exhaustive survey of all the spurious attempts at memory realization is obviously beyond the intent of this study. Still, it seems desirable to begin by "casting a wide net". Accordingly, Table 3-1 presents the full list of plausible technologies identified during an initial broad ranging literature search. Included here is every known, major implementation approach to suitably sized memories that has been mentioned in the open literature and which is either under active development or in production. In certain cases the level of effort in a particular technology area is very low keyed, or it is being pursued principally for an application other than its use as a storage medium.

Memory technologies in Table 3-1 are grouped initially according to their generic class. Specific technologies in each class are further subgrouped according to similarities in either their storage phenomena, mode of operation, or device fabrication features. As a result of this coordinated listing procedure, easy associations can be made between related technology species. The final column of this table denotes the common acronyms for the specific technologies. The general characteristics of these technologies are presented in the preliminary screening discussions of the next section. The source listings included in the Bibliography at the end of this report encompass the main stream of both published and unpublished material consulted in compiling the potential field of technologies and in ascertaining their respective attributes and limitations. Other sources obviously exist, but those reviewed represent a reasonably comprehensive cross-section of the developments that have, are, and will be taking place in the rapidly changing memory field.

Table 3-1. ASSIMILATED MEMORY TECHNOLOGY LISTING

Generic Class	Specific Technology	Acronym
Magnetics	Fixed Head Drum Moving Head Disc Tape Recorder Ferrite Core Plated Wire Closed Flux Oligatomic Film Ferromagnetic Film Domain Wall Domain Tip Cylindrical Domain	DRUM DISC TAPE CORE WIRE CFM OFM CROSSTIE DYNABIT DOT BUBBLE
Semiconductors	Metal Oxide Semiconductor Charge Coupled Device Nitride Interfaced MOS Complementary MOS CMOS On Sapphire MNOS On Sapphire Nitride Storage CCD Integrated Injection Logic Bipolar Semiconductor Amorphous Semiconductor Metal Alumina Semiconductor	MOS CCD MNOS CMOS CMOS/SOS MNOS/SOS MNOS/CCD I <sup>2</sup> L BIPOLAR JVNIC MAS
Ferroacoustics  Electrostatics Electrooptics Storage Tubes Cryogenics	Magnetostrictive Wire Magnetostrictive Film Surface Wave Delay Line  Ferroelectric Film  Optical Beam  Electron Beam  Josephson Effect	FAME SONISCAN SAW  MENTOR  OBAM  EBAM  JEM

### 3.2 Preliminary Screening

Following the common practice encountered in published literature, Table 3-2 presents order of magnitude parameters for those memory technologies that have sufficient data readily available. Since conditions at the component level are of secondary concern from a systems analysis perspective, tabulated values express as nearly as possible full system level parameters. To expedite feasibility decisions, an abbreviated list of camera memory objectives is included at the bottom of this table.

Density tabulations of this nature are employed frequently in the open literature to provide insight into the potential of specific technologies. Tables generated by alternate sources seldom agree in all details, however, and the biases evident on the part of some authors make the reliability of their data highly suspect. Different references often vary by an order of magnitude, and in some cases three orders of magnitude difference will be found. Part of the discrepancy lies with the fact that density parameters are too frequently quoted without a clear distinction made as to whether they refer to the storage cell level, the memory chip level, or the full system level. Dramatically different numbers result at each. To secure the values given in Table 3-2, the statistics of specific systems were used whenever possible. Even this process is complicated somewhat by the lack of a one-for-one correspondence of the data source configurations with the camera memory configuration.

Volumetric and mass densities ( $\text{bits/cm}^3$  and  $\text{bits/gram}$ , respectively) depend on both the memory components used and the design approach taken in packaging a system. In the area of semiconductor technologies, an option

Table 3-2. ORDER OF MAGNITUDE COMPARISONS OF SELECTED TECHNOLOGIES

Technology Base	Volatility		Density Parameters			
	V	NV	bits/cm <sup>3</sup>	bits/gram	Watts/bit*	cents/bit
DRUM		X	10 <sup>1</sup>	10 <sup>2</sup>	10 <sup>-5</sup>	10 <sup>-1</sup>
DISC		X	10 <sup>2</sup>	10 <sup>2</sup>	10 <sup>-6</sup>	10 <sup>-2</sup>
TAPE		X	10 <sup>5</sup>	10 <sup>6</sup>	10 <sup>-9</sup>	10 <sup>-3</sup>
CORE		X	10 <sup>1</sup>	10 <sup>2</sup>	10 <sup>-4</sup>	10 <sup>0</sup>
WIRE		X	10 <sup>3</sup>	10 <sup>2</sup>	10 <sup>-5</sup>	10 <sup>0</sup>
OFM		X	10 <sup>2</sup>	10 <sup>2</sup>	10 <sup>-5</sup>	10 <sup>-1</sup>
DYNABIT		X	10 <sup>2</sup>	10 <sup>2</sup>	10 <sup>-6</sup>	10 <sup>-1</sup>
DOT		X	10 <sup>3</sup>	10 <sup>3</sup>	10 <sup>-6</sup>	10 <sup>-1</sup>
BUBBLE (near term)		X	10 <sup>4</sup>	10 <sup>4</sup>	10 <sup>-7</sup>	10 <sup>-1</sup>
BUBBLE (projected)		X	10 <sup>7</sup>	10 <sup>7</sup>	10 <sup>-9</sup>	10 <sup>-2</sup>
MOS	X		10 <sup>3</sup>	10 <sup>3</sup>	10 <sup>-5</sup>	10 <sup>-2</sup>
CCD	X		10 <sup>3</sup>	10 <sup>3</sup>	10 <sup>-5</sup>	10 <sup>-2</sup>
MNOS (near term)		X	10 <sup>3</sup>	10 <sup>3</sup>	10 <sup>-6</sup>	10 <sup>-1</sup>
MNOS (projected)		X	10 <sup>6</sup>	10 <sup>6</sup>	10 <sup>-11</sup>	10 <sup>-3</sup>
CMOS	X		10 <sup>2</sup>	10 <sup>2</sup>	10 <sup>-6</sup>	10 <sup>0</sup>
I <sup>2</sup> L	X		10 <sup>2</sup>	10 <sup>3</sup>	10 <sup>-6</sup>	10 <sup>-1</sup>
BIPOLAR	X		10 <sup>1</sup>	10 <sup>2</sup>	10 <sup>-4</sup>	10 <sup>0</sup>
FAME		X	10 <sup>2</sup>	10 <sup>2</sup>	10 <sup>-7</sup>	10 <sup>-1</sup>
SONISCAN		X	10 <sup>3</sup>	10 <sup>3</sup>	10 <sup>-7</sup>	10 <sup>-1</sup>
EBAM	X		10 <sup>2</sup>	10 <sup>3</sup>	10 <sup>-5</sup>	10 <sup>-1</sup>
Evaluation Guidelines	(none)		625	2000	10 <sup>-6</sup>	10 <sup>-1</sup>
System B Requirements	(none)		262	839	2 x 10 <sup>-6</sup>	10 <sup>-1</sup>
System A Requirements	(none)		32	102	2 x 10 <sup>-5</sup>	10 <sup>0</sup>

\* see text discussion on power parameter variance.

exists of placing one memory chip or several memory chips in a single hermetic package. Standard MOS as well as CMOS, CCD, and BIPOLAR values based on assuming one chip in a package. MNOS and BUBBLE, on the other hand, are estimated assuming 16 chips per enclosure. These choices are made on the basis of available system examples. Obviously the densities will vary with the local arrangements for heat removal and the power dissipation of the memory system.

Power densities (Watts/bit), as tabulated here, represent results achieved in specific systems or claimed for proposed systems. Power is, however, an extremely sensitive function of the data rate. The near term bubble technology estimate is based on the goals for a NASA bubble memory tape recorder replacement. This  $10^8$  bit system is projected as dissipating 15 Watts at an output data rate of 15 Kbytes/sec ( $\sim$  120 Kbits/sec). A number more representative of the technology would be the power per bit with the field rotating at the maximum practical rate, which in this case is probably about 150 KHz. As the data rate increases the power density per bit degrades rapidly. Similar effects occur for the other technologies, so each must be examined closely to ensure that the camera memory objectives can be met.

Cost projections (cents/bit) reflect the statements of authorities in given technology areas with only minor adjustments. Invariably the less mature the technology the more optimistic the projection. Wherever possible the cost figures given reflect a total system configuration built to military or NASA type requirements. Lower systems costs reported in the literature usually apply to the commercial computer market.

Table 3-3 presents the results of the preliminary screening activity. Each technology is rated as to whether available information indicates that it has a reasonable chance of meeting the camera memory needs. The status of a technology in each category was graded as being:

- (A) probably adequate for the LST camera memory,
- (D) adequacy doubtful or unclear from available data,
- (N) not adequate for use in this application.

The judgement criteria for the eight categories are derived from the "evaluation guidelines" data presented previously at the bottom of Table 3-2. The first five categories (columns) are considered essential. A not adequate grade (N) in any one of these areas, or a doubtful rating in more than two is considered sufficient grounds to reject the technology from further consideration. Appendix C is devoted to brief discussions of each rejected technology. The last three categories represent items which are the subject of trade-off studies.

Category one specifies the overall match of the technology to the camera memory application. The questions of relevance to making this judgement are:

- Do any overt aspects of the technology make it unsuitable for use in space?
- Is the technology appropriate for being configured into a 10<sup>7</sup> bit capacity system?
- Will any intrinsic characteristic of the technology prevent achievement of the required performance goals?

Maturity is the second category. Assessment of this factor involves consideration of the application timeframe as reflected in the following questions:

Table 3-3. ADEQUACY OF TECHNOLOGIES FOR CAMERA MEMORY USE

Memory Technology	Match to Application	Maturity	Economic Drivers	Cost Potential	Reliability	Power	Volume	Mass
DRUM	N	A	A	D	N	N	N	N
DISC	N	A	A	A	N	N	N	N
TAPE	N	A	A	A	N	D	A	A
CORE	D	A	A	N	D	N	N	N
WIRE	D	A	A	N	D	N	D	N
CFM	D	N	D	D	D	N	D	N
OFM	D	N	N	D	D	N	N	N
CROSSTIE	D	N	D	D	D	D	D	D
DYNABIT	D	D	N	D	D	D	N	N
DOT	D	D	D	D	A	D	A	D
BUBBLE	D	A	A	A	A	D	A	A
MOS	A	A	A	A	D	D	A	A
CCD	A	A	A	A	D	D	A	A
MNOS	A	A	A	A	A	D	A	A
CMOS	A	A	A	N	D	D	D	D
CMOS/SOS	D	D	A	N	D	D	D	D
MNOS/SOS	D	D	A	D	D	D	A	A
MNOS/CCD	D	N	D	D	D	D	A	A
I <sup>2</sup> L	D	D	A	D	N	D	D	D
BIPOLAR	D	A	A	N	N	N	N	N
OVONIC	N	D	D	N	D	N	N	N
MAS	N	N	D	D	D	D	D	D
FAME	N	D	N	D	D	D	N	N
SONISCAN	N	N	N	D	D	D	D	N
SAW	N	D	A	N	N	D	N	N
MENTOR	N	N	N	D	D	D	D	D
OBAM	N	D	A	A	D	D	N	N
EBAM	N	D	D	D	N	N	N	N
JEM	N	N	D	D	D	N	N	N

A = Adequate  
D = Doubtful (or uncertain)  
N = Not Adequate

- Can a fully functional system breadboard be procured within the next few years?
- Will the technology have memory chips of sufficient capacity in volume production at that time?
- Are there any potential reliability and/or cost problems which may remain unresolved?

The third category is economic drivers. NASA does not wish to fund component development. Accordingly, it must be determined whether positive answers exist to the following:

- Do identified sponsors exist for a technology if additional development is required?
- Do the parameters of the technology indicate sound economic justification for continued development?

Category four is cost potential. This is a difficult subject in that NASA has expressed the desire for absolute minimum cost in a camera memory procurement. For the purpose of technology screening, this is interpreted as implying that a volume production potential cost on the order of 0.1 cents or less per bit will be necessary. Subsequently, the pricing of individual technologies is evaluated in the context of a military system, but not necessarily a space qualified system.

Reliability is the fifth category. For memories intended to store data from sensor instruments on space vehicles having extended mission times, the reliability goals are quite complex. In many cases it is unclear as to whether a given technology has a reasonable chance of success. In those cases where not adequate grades are given, negative commentaries were encountered on the following points:

- Are there any overt characteristics of the technology which will lead to poor reliability?
- Can the camera memory reliability goals be met using cost effective amounts of redundancy?

The last three categories treat system level power, volume, and mass. Direct use is made of the "evaluation guidelines" cited in Table 3-2 to make judgements in these areas.

In certain cases, supplemental evaluation criteria can readily be brought to bear in screening the list of memory technologies. No distinction is made between P-channel and N-channel MOS structures in the ratings of Table 3-3. But, of the two, N-MOS devices inherently exhibit better speed due to higher carrier mobility and they appear to have much greater potential for low cost. Only N-MOS is therefore given serious consideration. Similarly, systems involving mechanical motion are rejected automatically due to the proven poor reliability of such mechanisms. Finally, semiconductor technologies which use silicon on sapphire (SOS) processing are rejected because the reliability and cost aspects of SOS are still being evaluated. SOS does offer certain advantages, but the length of time that will be needed to prove them out is difficult to assess accurately. Once this is accomplished, the SOS options should be given serious reconsideration because of their intrinsic radiation resistance.

### 3.3 Prime Investigation

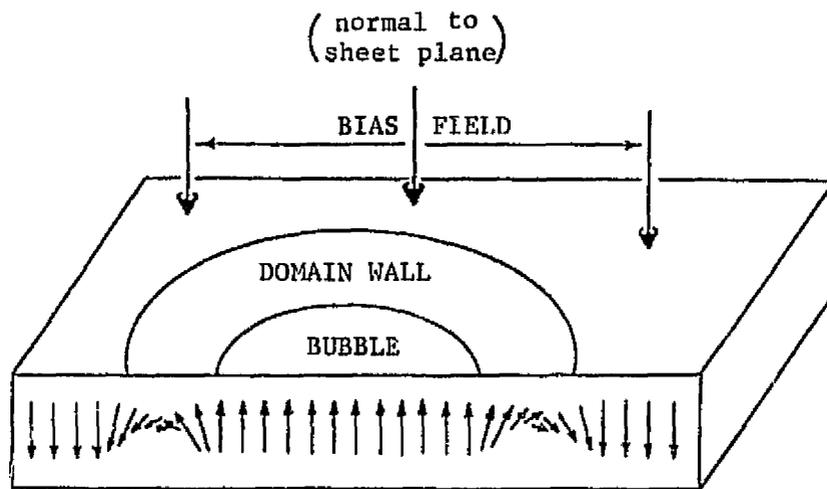
A check of the preliminary screening adequacy ratings of Table 3-3 reveals that only four technologies possess the proper set of attributes to be given serious consideration for use as the storage media in high-speed memories deployed aboard spacecraft which will be launched during the next few years. In particular, it is found that the Bubble, MOS (N-channel fabrication), CCD, and MNOS technologies have "adequate" ratings in nearly every category. All four are somewhat questionable in the area of power, but no technology is given a completely clean bill of health in this area. The Bubble and MNOS technologies are nonvolatile and, as a result, are ranked as having sufficient reliability capabilities. N-MOS and CCD, on the other hand, are volatile by nature and will probably require some form of redundancy to achieve the system guideline reliability goals. They are therefore given a questionable mark in this category. Similarly, the Bubble technology is considered to be poorly matched to the overall camera memory application due to its very poor speed capability.

In the following paragraphs each of the "prime" technologies is subjected to further detailed investigation. The work conducted which contributed to the discussions made here consisted of additional literature searches, personal interviews with experts in the respective technologies, and preliminary considerations of exploratory camera memory organizations applicable with each technology. Specific comments are included on every major aspect of these technologies which have relevance to the LST camera memory application.

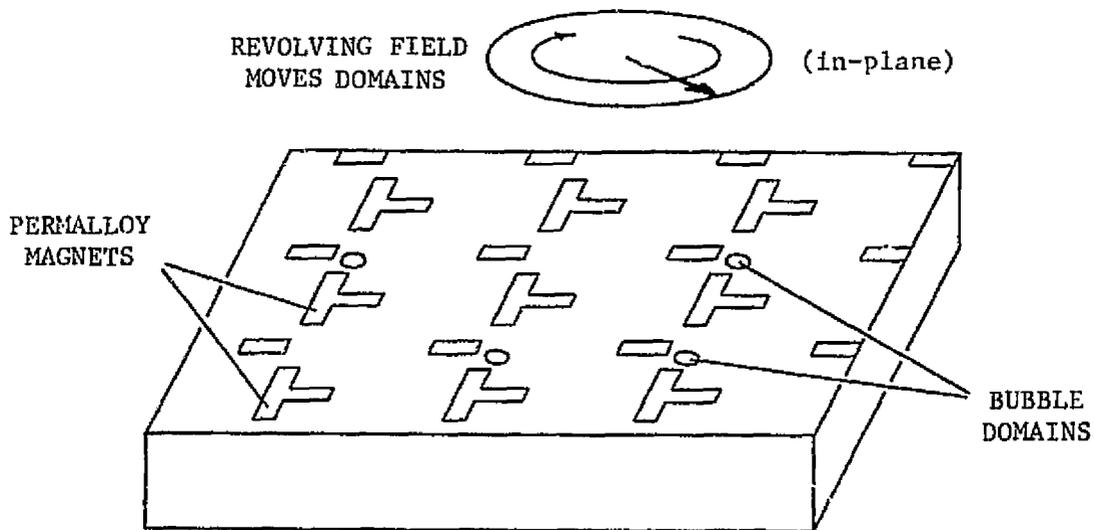
### 3.3.1 Bubble

This is an emerging technology which is presently receiving a great deal of attention. It is based on the generation and dynamic control of cylindrical magnetic domains in certain special types of ferromagnetic materials. Cylindrical domains are usually referred to as "bubbles", since, when observed through a microscope using polarized light, they take on the visual appearance of bubbles moving about on the surface of the material. The presence or absence of a domain at a particular physical location is used to represent the storage of binary information. An extensive literature exists (see bibliographical listings) which describes the physical principals involved and reports on various aspects of device and system realization. A "broad-brush" treatment of this material facilitates a ready grasp of the basic concepts.

In simplified terms a magnetic bubble is a round cylindrical domain of upward (or downward) magnetization in a thin sheet of magnetic material surrounded by a region of downward (or upward) magnetization in the manner depicted in Figure 3-2. These domains are produced in materials of high magnetic crystalline anisotropy, where the axis of easy magnetization is normal to (perpendicular to the plane of) the sheet, whenever a uniform magnetic bias field of the proper magnitude is applied along this axis. If the magnetic intensity is not uniform, the domains will move to where the bias field is lowest. When a pattern of local minima of intensity is established and moved along in some path, the bubbles follow the pattern. The bubbles repel each other like parallel dipoles and, in practical devices, must be kept about four diameters apart to minimize undesirable interactions.



(a) Visualization Of Domain Wall Formation



(b) T-Bar Domain Control Structure

Figure 3-2. Simplified Bubble Memory Device Concepts

Stable bubbles exist only within a limited range of applied magnetic field intensities. The Interaction of the applied field and domain wall energies tends to reduce the bubble volume and the total wall surface area. At some critical upper field limit ( $H_2$ ) the domains collapse entirely leaving a "sea" of unidirectionally magnetized material. At the other extreme, magnetostatic energy acts to increase bubble surface area. As the bias field is reduced the bubbles grow in size until, at some lower field limit ( $H_1$ ), they cease to be circular and predictable control over them is lost. Bubble stability is thus a function of the complex interplay of many factors which cause the domain wall to always take on a shape that minimizes its net energy.

The major theoretical relationships of importance to the realization of magnetic bubble memory devices are fairly well documented. A parameter "L" having a dimension expressed in terms of length has been defined as the ratio of the energy-per-unit-area of a domain wall to the energy-per-unit-volume of the domain. The optimum thickness for a sheet of magnetic material is  $4L$ , and at that thickness stable domains will have a diameter of about  $8L$ . The ratio of  $H_2$  to  $H_1$  (which specifies the applied field operating margin) is typically about 1.6 to 1. The required bias field to maintain the  $8L$  domain is about  $1.2\pi M_s$ , where  $M_s$  is defined as the saturation magnetization. The choice of the magnetic material determines L, and thus determines whether a practical memory device is feasible.

At the present time, the maximum rotational field rate for practical bubble memories is under 200 KHz (typically 100-to-150 KHz) using bubble domains in the range of 4-to-6 microns in diameter. Experimental laboratory devices have operated at slightly over 1 MHz, but employed

bubbles an order of magnitude larger (viz., 40-to-60 microns). A fundamental materials limitation appears to exist which prevents the simultaneous attainment of small (sub-micron) sized bubbles and high field rotational shift rates ( $> 1$  MHz). As indicated in Figure 3-3, the development trend for ferromagnetic materials able to support stable bubbles has thus far been such that the domain velocity varies approximately as a cubic power of the bubble size. Unless a truly major breakthrough is made in this area, the field rates in large scale bubble memory systems will probably be limited to no more than 250 KHz.

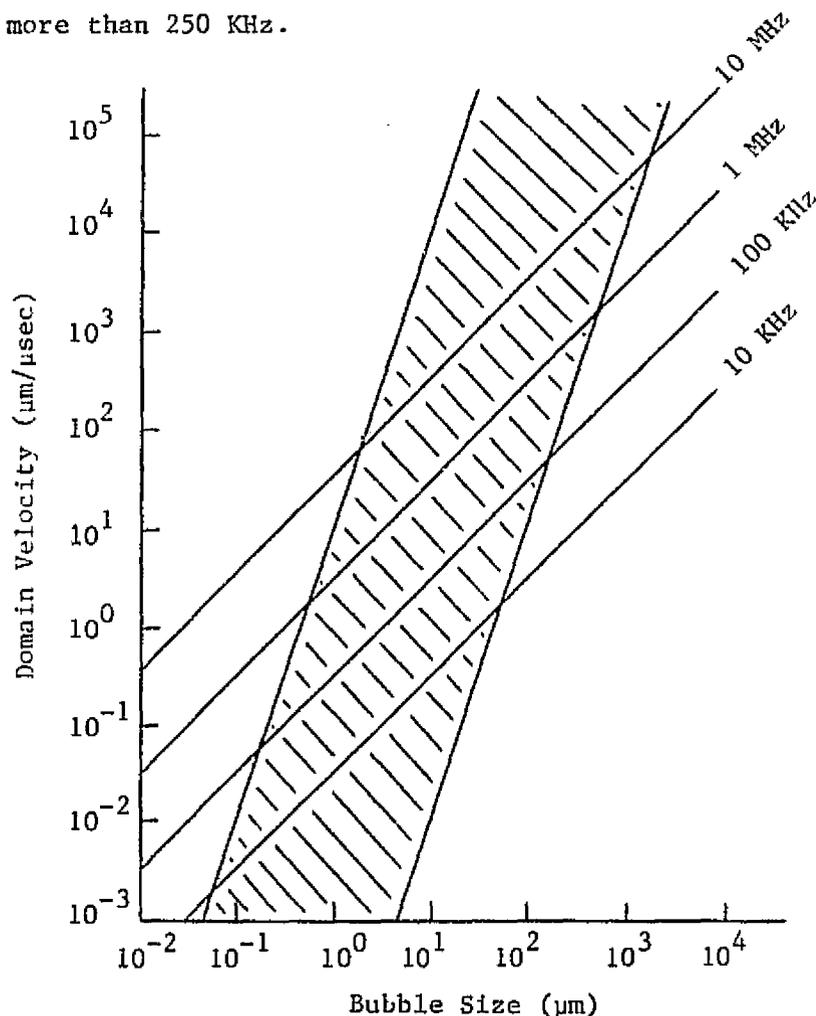


Figure 3-3. Magnetic Bubble Materials "Size-Velocity" Band  
 All known materials (ferrites, garnets, etc.)  
 capable of supporting stable cylindrical  
 magnetic domains fall conservatively  
 within the indicated band.

Because the bubble memory is basically a low data rate device, a requirement for a high data rate will increase both the cost per bit and the power dissipation. Cost impact occurs at both the chip design and the system level. To achieve high data rates at the chip level, multiple I/O ports must be used. If one port can provide a bit rate of 150 KHz, N ports can provide  $N \times 150$  KHz. But chip cost is a strong function of die size, and minimum die size is achieved by having as few I/O ports as possible. Bubble shift registers use chip area very effectively, but this is not true of the output sensor. A common practice is to expand the domain before sensing. Larger bubbles passing under the sensor provide a larger signal, and thus a larger signal-to-noise ratio. Multiple sensors significantly increase the die area.

To achieve high data rates at the system level the bit streams from many different chips must be multiplexed. This can be efficiently accomplished if the multiplexed chips are all under a common bias and rotating field assembly. The chips in such an assembly must be carefully matched to insure that proper bias margins exist over all operating conditions. A practical upper limit to the number of chips per field coil is 16. A certain amount of overhead hardware is required for data sensing, selection, and switching. This hardware increases proportionally with the number of chips to be multiplexed.

When more than one rotating field must be in operation, the low power per bit potential which accrues to a bubble system by virtue of its nonvolatile storage rapidly disappears. A ballpark number for the power dissipation associated with each rotating field assembly operating at 150 KHz, for instance, is 30 Watts. If a bubble chip design existed which would allow a read/modify/write operation to be conducted directly on a

per bit basis at this 150 KHz rate, then a camera memory having 16 bit wide words processed at a rate of  $10^7$  words/second would require the multiplexing of 1067 output lines from its storage section. If each of the 16 chips in the respective rotating field assemblies has only one output line, 67 different rotating fields would have to be in operation at the same time. This implies an average power of more than 2000 Watts. If each chip had 10 output lines, on the other hand, this could be brought down to 200 Watts.

Bubble system design must give careful attention to the off-chip electronics and magnetic field generation structure for the price per bit to be competitive with other technologies. The cost burden of these memory support components must be spread over as many bits as possible with both chip and system design contributing to the sharing of the overhead. This constraint, plus the competitive pressure of semiconductor alternatives, tends to limit bubble memories to configurations of  $10^8$  bits or larger. In addition, this boundary will probably move upward as semiconductor memory bit densities increase and their associated costs per bit drop.

One of the problems associated with design considerations of the peripheral circuitry is that bubble devices are nonvolatile conditionally on the rotating fields being shut down properly. Dr. Robert Stermer, who heads the magnetic project office at NASA Langley Research Center, has indicated that this has proven to be a difficult task. Working at a field rate of only 100 KHz, a development effort extending over better than 1 year was necessary to evolve a circuitry scheme capable of deactivating the fields within the narrow  $\pm 5^\circ$  phase angle necessary to prevent data storage perturbations. The problem is obviously compounded as the field rate and drive current levels are increased.

Under the auspices of Dr. Stermer's office, a bubble domain flight recorder having a storage capacity of  $10^8$  bits and containing 1000 memory chips is presently being developed for NASA by Rockwell. The cost goals established for this recorder include a volume production chip price of \$46 to \$48 and a targeted system price of \$100K per copy after initial development. These projections yield a cost of 0.1¢/bit; but, being based on estimates made a few years ago, they do not allow for the effects of inflation and may be slightly low for the real-world of 1978. Similar projections made in 1971 by other bubble advocates produced an estimated price of \$200K for a  $10^9$  bit system, or about 0.02¢/bit.<sup>(7)</sup> The overoptimism evident in this projection is attributable to the relative immaturity of the technology at that time, the assumed availability of  $10^6$  bit chips costing only \$24 each, and the use of labor rates and support component cost figures which were low by at least a factor of two.

Persuent to this, an independent exercise must be performed to ballpark a more realistic sell price for a  $10^8$  bit bubble system based on the use of more practical  $10^5$  bit chips. Following the lead of Dr. Stermer, a bubble chip price of \$47 is assumed. The results of this estimation process are summarized in Table 3-4. By correlating this information with the previously cited data secured through interviews with workers active in the development of bubble systems, it is possible to make the definitive deliniation of the descriptive parameters listed in Table 3-5 for working bubble memories over the next few years.

Upon reviewing the discussions made here it is seen that there are a number of areas in which the bubble technology is not well matched to the camera memory application. The small memory size will not allow sufficient

Cost Factor	Cost Estimate
Memory Chip	\$47K
Support Circuitry and Hardware	\$48K
Assembly, Test, and Labor	\$90K
Total Direct	\$185K
Approximate Sell	\$240K

Table 3-5. ANTICIPATED CHARACTERISTICS OF BUBBLE SYSTEM

Parameter	Value
Field Shift Rate	< 200 KHz
Chip Capacity	~ 100 Kbits
Chips/Field Assembly	16 (maximum)
Cost/Chip	~ \$48 (in volume)
Cost/System	> 0.2¢/bit

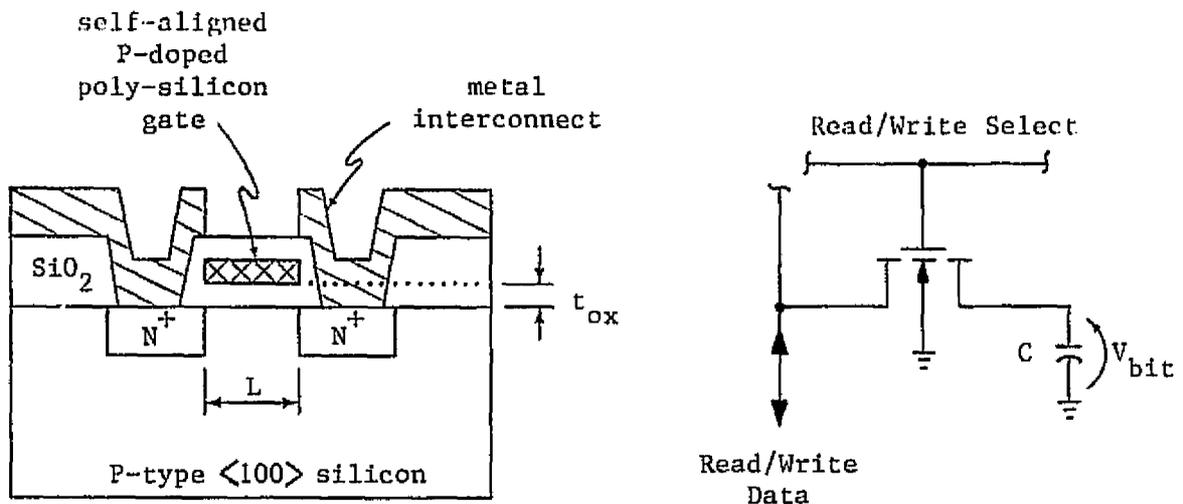
cost sharing of the off-chip overhead to achieve the 0.1 cent/bit cost goal. The requirement for high data rates causes several problems. Achievement of a 10 Watt average power level using any currently projected bubble chips appears virtually impossible. Custom development of a bubble device having many output lines is considered as violating the study guideline of "no NASA funds for component development". Moreover, even if such a chip were developed, the cost of that device would be higher than smaller chips and its off-chip overhead circuitry requirements would still be unreasonably high. Consequently, the bubble technology is dropped from any further consideration for use as the storage media in the LST camera memory.

### 3.3.2 N-MOS

Of the four prime candidate technologies investigated, N-channel MOS is the most mature. It represents the present apex of semiconductor volume manufacturing technology. It is currently replacing the older P-channel technology for RAM applications and within the next few years it is expected to totally supplant P-MOS as the major MOS technology in all but a few highly specialized areas.

MOS technology, N-MOS or P-MOS, has distinctive characteristics which make it attractive for memory fabrication. It is self isolating, so isolation diffusions are not required and die area is conserved. Input impedances are high, allowing information to be readily stored on the gate capacitance of a transistor. Dynamic circuit operation is thus practical with memory cells containing only a few transistors. One to three transistors per cell is quite common. The manufacturing process itself is relatively simple with only five to seven masking steps normally involved. This leads to high fabrication yields and favorable device economics.

Figure 3-4 presents a cross-sectional view of a modern, self-aligned, silicon gate N-MOS transistor along with a circuitry scheme for employing it as a single transistor (1T) memory cell in a two-dimensional array of cells. When the silicon gate of this device is held at a sufficiently positive potential with respect to the substrate the region under the gate inverts to N-type. This inversion layer permits electron conduction to occur between the N<sup>+</sup> source and drain diffusions whenever a potential difference exists between them. When the gate has zero or negative potential



(a) N-MOS Transistor Cross-Section

(b) Basic 1T Dynamic Memory Cell

Figure 3-4. N-MOS Memory Transistor Cell Structure

relative to the source, the inversion layer disappears and no source to drain current flows. Only leakage currents from the source and drain diffusions exist under this condition.

Fundamental advantages accrue to N-MOS devices (compared to P-MOS) by virtue of the electron mobility being 2 to 3 times higher than hole mobility. In particular, both the gain and the bandwidth (speed) of any MOS transistor is proportional to the conduction factor,  $\kappa$ ; which is expressed in terms of intrinsic device parameters as

$$\kappa = \mu C_{ox} W/L$$

where the capacitance per unit area in the gate region ( $C_{ox}$ ) is given by

$$C_{ox} = k_{ox} \epsilon_o / t_{ox}$$

In these relationships, the nomenclature employed is as follows:

$\mu$  - majority carrier mobility (electrons for N-MOS and holes for P-MOS)

$k_{ox}$  - dielectric constant of oxide (= 4 for  $SiO_2$ )

$\epsilon_0$  - permittivity of free space (=  $8.85 \times 10^{-6}$  pF/ $\mu$ )

W - channel width

$t_{ox}$  - gate oxide thickness

L - channel length

Accordingly, it is seen that N-MOS devices inherently have greater gain and speed than similarly sized P-MOS devices. If the transistors are designed for equal speed, the N-MOS device would be smaller. Consequently, an N-MOS memory chip can employ smaller transistor geometries and achieve higher bit density than a P-MOS chip with similar performance characteristics.

One of the difficulties with N-MOS which initially retarded its development is its tendency to produce devices which operate in the depletion mode (normally ON) rather than in the enhancement mode (normally OFF) as is desired. The reason for this is that the polarity of the charges trapped in the interface region between the silicon and the silicon dioxide is such that the silicon surface of an N-MOS structure tends to invert with no bias applied. This problem is overcome by a combination of processing techniques. These include:<sup>(8)</sup>

- use of <100> crystal orientation silicon to secure the lowest possible interface state density.
- use of higher dopant concentrations in the bulk silicon to make surface inversion more difficult.
- use of self-aligned gate processing to minimize to gate to source (or drain) overlap capacitance.

- use of thicker gate oxides to lower the capacitance per unit area ( $C_{OX}$ ) and hence increase the threshold voltage.
- use of reverse substrate bias "body effect" (potential between substrate and source) to increase the threshold voltage

By virtue of its having an innate tendency to produce low threshold devices, though, the N-MOS technology lends itself to the use of low power supply voltages. An accompanying merit of the use of low voltages is that depletion layers within the silicon spread by a minimum amount and close packing of components on the chip can be achieved. Additionally, low voltage operation facilitates easy and direct interfacing with standard T<sup>2</sup>L and CMOS logic families. Peripheral circuitry design are therefore simplified. This allows the power and time delay losses in level shifters to be either eliminated or minimized, and the clock driver power requirements to be made moderately low compared to on-chip dissipation.

The current focus of attention by N-MOS technology manufacturers is on the production of 4096 bit RAM's. As further experience is gained with the technology, tighter dimensions are being applied to the processing of N-MOS devices. As a point of reference, Table 3-6 itemizes the physical parameters of an abbreviated selection of MOS memory products. The data presented here is somewhat historical in that it includes only two devices (the 7127 and the 2107) which are considered of reasonably modern vintage. Since the time of accumulating this information, 4K/N-MOS RAM chips having even smaller cell and die areas have been announced. Moreover, indications are that within one to two years, 8 and/or 16 Kbit devices may become available. This will allow systems built with 4K units to be doubled or quadrupled

Table 3-6. PHYSICAL PARAMETERS OF MOS MEMORY PRODUCTS

Part Number	Technology	Bits/Chip	Cell Area mils <sup>2</sup>	Overhead Factor
1103	P-MOS RAM	1024	5.8	2.7
7111	N-MOS RAM	2048	5.2	1.6
7112	N-MOS RAM	4096	2.7	2.2
7127	N-MOS RAM	4096	1.9	2.7
2107	N-MOS RAM	4096	2.0	2.5

in capacity with only minor control circuitry modification, or else permit the use of one half to one fourth as many memory parts (which impacts directly on realizable system reliability).

Vendors of 4K/N-MOS RAM's have recently begun to ship parts in significant volume. Individual firms have and probably will continue to experience sporadic yield problems, but it appears that 1976 availability of this particular type of N-MOS memory chip is well assured. Firms active in the field are, in fact, presently engaged in attempts to establish second sources and common pinouts among groups of similarly fabricated devices. Circuitry refinements are also being incorporated to enhance operating margins and reduce pin counts. Little effort has as yet been expended on military qualification or radiation hardening features. Discussions of military specifications for 4K/N-MOS devices appear at present to be confined to the tentative military standard 883/235 suggested by Texas Instruments in a proposal submitted to the Rome Air Development Center. Since the

predominant application for N-MOS memory products is in commercial computer mainframes, few significant economic drivers exist for developing devices which are highly radiation resistant. Even without special emphasis on this characteristic, MOS processing is sufficiently advanced that typical devices exhibit a cumulative dosage tolerance level on the order of  $10^5$  rads before the onset of major numbers of failures from excessive parameter degradations. Most space vehicles either already contain or easily accommodate the moderate amount of shielding necessary to insure staying well below this dosage level over their assigned mission times.

From the viewpoint of the camera memory application, several conclusions can be drawn from the foregoing discussions. First and foremost is the fact that N-MOS performance is adequate to build an LST camera memory. System A can certainly be implemented and, although N-MOS may not provide the most attractive alternative, System B conceivably could also be built. Device availability in the 1976 timeframe is assured, with an excellent probability of multiple sources and common pinouts being established for several devices. Small quantity prices are presently at about 0.5¢/bit, and are projected to go below 0.2¢/bit by 1980 (note: this costing does not include reliability screening adders). By 1976 the failure rate of N-MOS RAM's as a generic class should be clearly established with many specific parts having accumulated sufficient data to allow individual judgements as to their suitability for space qualified sensor instrument memory applications. In short, N-MOS appears to constitute an excellent option for the near term LST camera memory requirements.

### 3.3.3 CCD

Charge coupled device (CCD) technology is a recent addition to the semiconductor class of memories. Considered in general terms, the CCD is similar to MOS in that both devices are unipolar and depend on majority charge carrier action for their operation. In its information storage area, though, a CCD needs no PN junctions (buried channel devices introduce them intentionally) and has neither contacts to the silicon nor any form of load element or flip flop. Functionally, CCD's store minority carriers in potential wells (regions depleted of majority carriers) either at the silicon surface or at buried sites in the bulk material, and move these charge packets by effectively moving the wells. The presence or absence of charge in a well represents a logic one or zero.

From a structural point of view, the CCD is a linear array of closely spaced MOS capacitors. The basic structure of a surface channel CCD, as seen in Figure 3-5, consists of N-type bulk silicon, a dielectric layer of silicon dioxide, and a set of conductive electrodes. When a negative step of voltage is applied to a given electrode, majority carrier electrons in the silicon under that electrode are repelled and respond within the dielectric relaxation time (which is typically on the order of 100 picoseconds) to produce a depletion layer of positively charged donor states (i.e., a "potential well") near the surface of the silicon. Thermally generated minority carrier holes in this region are trapped by the residue field existing within the depletion layer and, after a period of time on the order of seconds, will accumulate in sufficient quantity to "fill" the potential well and cause the depletion layer to collapse into a strong inversion layer.

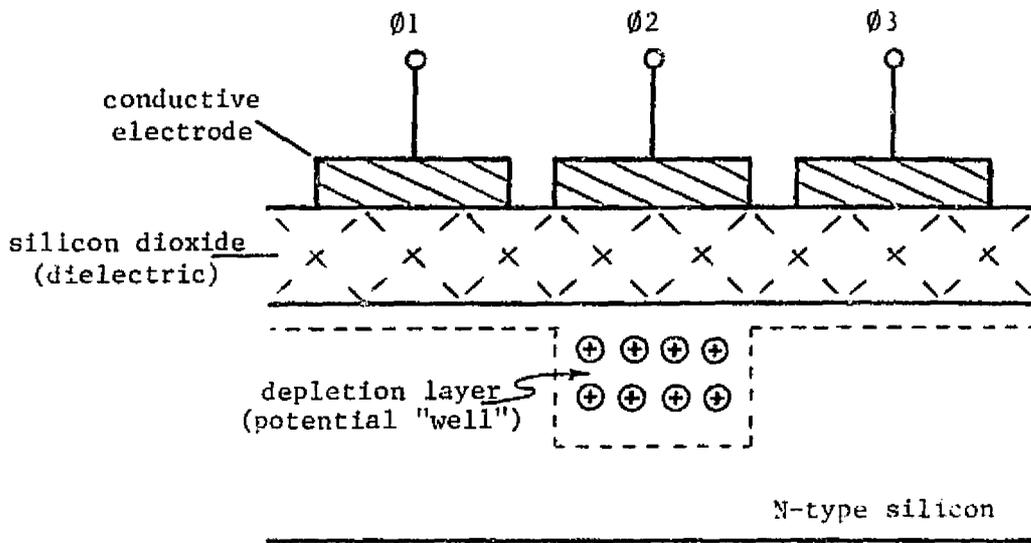


Figure 3-5.

Cross-Sectional Structure of Two-Phase Surface Channel CCD

The potential applied to the gate electrode (referenced to the silicon substrate) divides between the oxide and the depletion layer. The structure can be thought of as two capacitors in series. The voltage across the depletion layer is the surface potential. For time intervals much shorter than the thermal relaxation time, the depth of the potential well can be changed by changing the electrode voltage. The addition of charge into the well reduces the surface potential, and thus the depth of the well.

A CCD shift register moves charge from one electrode to an adjacent electrode by altering the well depths using phased clock voltages. When an adjacent well is deeper, some percentage of charge moves into that

well in the time available for transfer. The fraction of the total charge transferred is called the transfer efficiency  $\eta$ . This is an important design parameter. Transfer inefficiency ( $\epsilon = 1 - \eta$ ) is also a convenient way of describing this phenomena.

Many factors have an effect on the transfer. First, the capacitors have to be close enough so that the depletion layers overlap strongly. The surface potential in the gap should have a smooth transition. The charge movement is affected by charge repulsion, by thermal diffusion, and by the influence of fringing fields. Charge is lost to fast interface states. Fast interface states fill rapidly, but empty at a rate which depends on the energy level of the state. Thus, some of the signal charge can be captured and then later be released into subsequent signal packets. One approach to reducing this problem is to continually propagate a small amount of charge (Fat Zero) to keep the surface states continuously filled. Another approach is to move the potential wells away from the Si-SiO<sub>2</sub> interface by means of including a layer of opposite conductivity to the substrate under the SiO<sub>2</sub>. This is called a buried channel device.

CCD cannot be said to imply some particular homogeneous process sequence or physical structure. Many approaches to CCD shift register realization have been reported. The most distinct difference is in the charge coupling gate structures. In practical devices some form of multi-level electrodes are required. The most popular approaches currently center around the use of aluminum and poly-silicon. Other fabrication differences relate to the means for channel confinement, the choice of substrate resistivity, and the choice of surface or buried channel.

A practical CCD memory chip must contain MOS structures to perform control and interface functions. In addition it must also contain the complex CCD electrode structures. This means that the CCD manufacturing sequence is of greater complexity than MOS-only processing. This rather obvious fact has not been clearly reported in the literature. CCD's differ from MOS in certain respects which are important in manufacturing. Thin oxide regions cover a large percentage of a CCD register. To achieve a given yield for a given size die, the oxide quality must be generally better on a CCD than on an MOS part. In fact, some workers believe that the state of the art of oxide preparation and cleanliness will be stressed by the challenge of CCD fabrication. Properties of the silicon which are important to CCD operation may not be of the same degree of importance to MOS devices. Fast interface states is one example.

The yield of CCD parts (as well as those of other LSI technologies) depends on the quality of masks, photoresist, oxides, and silicon material. The absence of PN junctions and ohmic contacts in the CCD register has been cited as a reason for expecting high yield, but these factors are of relatively minor concern when considered in the context of all the causes of yield loss. The lack of junctions and contacts does contribute to CCD's major asset-viz., a small cell size. CCD layout can make efficient use of area by virtue of the designer not being constrained by such factors as minimum contact areas and tolerances for metal overlap. Present day CCD chips have cell sizes on the order of 1.3 mils<sup>2</sup>. Commercial N-MOS RAM chips, in comparison, have cell areas on the order of 2 mils<sup>2</sup>. This apparent advantage in cell size for CCD's is believed to be only a transitory condition existing at this particular point in time. It is expected to diminish markedly as the state of the art of photolithography progresses.

Cell size is, of course, only a part of the story. The peripheral circuitry required to form a useful chip requires a significant amount of area. The effective cell size can be defined as the total chip area divided by the total bits per chip. As an alternate it can also be expressed as the product of total cell area times an overhead factor. As with all LSI devices, the overhead factor for CCD chips is a function of the particular chip design. Specific examples found in published literature include devices from RCA, Intel, Fairchild, and Bell Northern of Canada.

RCA is reported working on a 16,384 bit SPS chip with a  $1.44 \text{ mil}^2$  cell size, and dimensions of  $224 \times 240$  mils. This is an effective cell size of  $3.28 \text{ mil}^2$ , with an overhead factor of 2.28. Intel's recently announced 2416 part is also a 16,384 bit memory. Published reports indicate that the die area is  $33,000 \text{ mils}^2$ . By correlating a photograph of the die (which appeared on the cover of the February 15, 1975 issue of Electronic Design) with the stated area and working out its length-to-width ratio, the die is estimated to be 216 mils by 153 mils. A similar analysis of the shift register area leads to a cell size estimate of  $0.86 \text{ mils}^2$ . The effective cell size is thus  $2.02 \text{ mils}^2$  with the chip exhibiting an overhead ratio of 2.35. The Fairchild CCD450, on the other hand, is a 9216 bit chip with a  $1.3 \text{ mil}^2$  cell and dimensions of  $200 \times 135$  mils. This is an effective cell size of  $2.93 \text{ mils}^2$ , or an overhead factor of 2.25. The device developed by Bell Northern Research is an 8192 bit chip with a  $1.76 \text{ mil}^2$  cell and dimensions of  $168 \times 178$  mils. The effective cell area for this device is  $3.65 \text{ mils}^2$ , and the overhead factor is 2.07. Table 3-7 summarizes the physical parameters of the RCA, Intel, Fairchild, and Bell Northern CCD memory chips.

Table 3-7. PHYSICAL PARAMETERS OF CCD MEMORY DIE

Manufacturer	Bits/Chip	Dimensions mils x mils	Cell Area mils <sup>2</sup>	Overhead Factor
RCA	16,384	240 x 224	1.44	2.28
Intel	16,384	216 x 153	0.86	2.35
Fairchild	9,216	200 x 135	1.30	2.25
Bell Northern	8,192	178 x 168	1.76	2.07

R. Foss of Microsystems International, at the IEEE Mass Memory Workshop (May 22-23, 1974, Arlington, VA), predicted the availability of CCD chips with 0.8 mil<sup>2</sup> cells and 1.8 overhead factors. Strong CCD proponents like Mr. Foss have generally claimed that the technology will allow lower overhead than competing alternatives. Examination of the actual overhead areas for the four CCD chips investigated does not support this claim. From the data in Table 3-8 it appears that an efficient CCD design typically needs on the order of 15,000 mils<sup>2</sup> for overhead. An efficient N-MOS RAM design, on the other hand, requires approximately 12,000 mils<sup>2</sup> for overhead functions.

Table 3-8. AREA UTILIZATION OF CCD MEMORY DIE

Manufacturer	Die Area	Memory Area	Overhead Area
RCA	53,760	23,593	30,167
Intel	33,048	14,090	18,958
Fairchild	27,000	11,981	15,019
Bell Northern	29,904	14,418	15,486

If 20,000 mils<sup>2</sup> is taken as a desirable size from a yield standpoint, N-MOS and CCD densities can be compared. Table 3-9 summarizes the results of this comparison. For this size chip a CCD device would cost more than an N-MOS device. As the die size increases the relative density achieved will in the limit approach the ratio of the cell sizes. Thus the "typical" density improvement factor of CCD over N-MOS is close to unity (1.0:1) — denoting no improvement advantage — and the "best" density limit appears to be less than 2.5:1. The economic justification for CCD memory technology rests on whether this potential density improvement can overcome its typically lower yield relative to N-MOS and thereby provide lower cost per bit.

Table 3-9. COMPARISON OF CCD AND N-MOS DIE PARAMETERS

Device Parameter	CCD (typical)	CCD (best)	N-MOS (typical)
die area	20,000	20,000	20,000
peripheral area	15,000	12,000	12,000
storage area	5,000	8,000	8,000
cell size	1.3	0.86	2.0
total bits	3,846	9,302	4,000
relative density	0.96	2.33	1

Intel is approaching CCD technology with a wait and see attitude. Gordon Moore was recently quoted (Electronics, October 17, 1974, p. 65) as saying, "CCD is just another MOS device. Neglecting the imaging application, the whole question in memories is whether CCD gives enough of a cost advantage over what you can do with RAM's. Everytime (we) learn to do something with

CCD's it gives us another idea for what (we) can do with RAM's. For the same cost, the RAM is generally a more powerful function. They are not the same cost yet—the CCD is about a factor of two ahead of the RAM. So the question is—is that enough? I personally think CCD could be an important memory technology, but I wouldn't stake my company on it."

If memory products were the only application for CCD technology its future would have to be questioned. This, however, is not the case. CCD's provide the unique capability of working with analog data. Imaging and signal processing applications are providing the economic drive which is maturing the technology. Whether memory CCD's achieve any significant production volume will be a function of chip availability and the timing of advances by competitive technologies. The immediate market foreseen for CCD memory chips is as an alternative to dynamic shift registers. There may also arise a variety of small special purpose applications, but it is doubtful if the cost per bit of the CCD versus the RAM will ever be low enough to justify a place for the CCD in the general purpose computer hierarchy. The construction of  $10^7$  and  $10^8$  bit CCD memories does not seem attractive in view of competition from nonvolatile technologies like MNOS and magnetic bubbles.

The volatility of CCD memories is a draw back from the point of view of reliability and power dissipation. In a large CCD memory every chip must be continuously under electrical stress — i.e., in the active state. When a chip is not in use it must still be cycled to maintain its data. The minimum recirculation shift rate is an important parameter for the achievement of low power systems. For a nonvolatile technology the chips would almost always be in a powered down mode — i.e., dormant state. It has been established that integrated circuits in the dormant state enjoy a failure rate

of less than one tenth the failure rate of circuits in the active state. This feature becomes important in applications involving a large number of chips and/or long mission times.

Early CCD spec sheets indicate that at 70°C a cell must be refreshed within 1.1-to-1.3 milliseconds. The vendor's requirement for a minimum clock rate is usually stated for some specified maximum temperature. A reasonable procedure for predicting the minimum shift rate at another temperature is to allow for a doubling of the rate with every 10°C increase according to the relationship

$$f_c = k \cdot 2^{T_c/10}$$

where "k" is a constant computed from

$$k = f_{cs} \cdot 2^{-T_{cs}/10}$$

with the terminology employed being defined as follows:

$f_{cs}$  - specified min shift rate

$T_{cs}$  - specified max temperature

$f_c$  - min shift rate at a temperature of interest

$T_c$  - temperature of interest

The Intel 2416 specification allows a maximum shift period of 9 microseconds at 70°C. With refresh occurring every 128 stages, this a refresh interval of 1.152 milliseconds. The Fairchild CCD450 preliminary specification guarantees only a 100 KHz minimum shift rate capability at 55°C (although 50 KHz is called out as being typical) with refresh also occurring every 128 stages. The guaranteed maximum 55°C refresh interval is thus 1.28 milliseconds, and this implies a 70°C refresh interval of 0.453 milliseconds. It appears that at present Fairchild is hedging slightly on this specification until greater knowledge of the production distribution becomes available.

Maximum shift rates are determined by the CCD transfer efficiency. This is a function of cell design, fast interface states, electrode geometry, and a host of other interrelated factors. It appears that practical guaranteed maximum shift rates will be on the order of 1 to 2 MHz. The realization of higher shift rates would most likely require a less dense chip design, and would thus imply a higher cost per bit. To compute the power dissipation of a CCD chip the current flow at every pin must be accounted for. Both dc and transient components exist, and power depends strongly on data rate. The bulk of on-chip dissipation is related to the 2 or 3 power supply pins. The bulk of the off-chip dissipation is associated with driving the highly capacitive clock lines. For these lines a minimum power of  $fCV^2$  is required from the power supply and, since typical clock drivers are not very efficient, this can easily grow to  $2fCV^2$ .

CCD's appear to be more sensitive to radiation than the other memory technologies under consideration. In a recently published report on work carried out at the Naval Research Labs,<sup>(9)</sup> test results for three different CCD structures were presented which revealed that device failures are encountered at dose levels below  $10^3$  rads. In this case the mechanism is fat zero saturation. Some compensation is possible by altering operating voltage levels, but above  $10^4$  rads a number of other failure mechanisms come into play and render both surface channel and buried channel devices inoperative. Numerous suggestions have been made for improving radiation resistance, but it is doubtful if these items will be incorporated in commercial CCD designs.

From the preliminary examinations made here it is concluded that CCD devices can be used to form a camera memory. Because of the lack of a clear cut price advantage over N-MOS RAM's, though, CCD is a marginal memory technology. CCD's are receiving development support primarily because of their imaging and analog signal processing capabilities. Commercial memory devices have now been announced, so the probability of device availability is good. As noted, radiation resistance is poor and reliability experience either does not exist or has not been published. Performance in the camera memory application is hampered by the relatively limited maximum shift rates achievable by the emerging devices. Power is expected to be relatively high because of the need for continuous recirculation at 100 KHz rates to refresh the memory. Volume and mass density objectives for the camera memory appear practical because of the chip bit density.

### 3.3.4 MNOS

Metal-nitride-oxide-semiconductor (MNOS) technology has been under development by many different organizations in several countries for almost a decade. The fundamental mechanisms and material properties associated with the memory transistor have been studied in detail (see, for example, the works of White, Lampe, Cricchi, and Brewer in bibliographical listing), and the technology has achieved the level of maturity necessary to allow the design and fabrication of practical memory chips. A number of companies have in fact been producing various MNOS products for the past few years.

The full potential of the MNOS technology only recently has begun to be well understood, so it has not been publicized broadly. As a technology base, MNOS encompasses a tremendous realm of practical applications and actually consists of at least six different sub-technologies aimed at specific functions. These include:

1. Electrically Alterable ROM (EAROM)
2. Block Organized RAM (BORAM)
3. Non-Volatile RAM (NOVRAM)
4. Non-Volatile SAM (NOVSAM)
5. Non-Volatile CCD (NOVCAM)
6. Non-Volatile LSI Logic (NOVLOG)

Each of these sub-technologies employs MNOS memory transistors, but the respective transistor designs and their characteristics are typically quite different. In addition, the transistor structure and manufacturing sequence will vary widely from company to company and the on-chip peripheral circuitry is quite different in some of the categories. Specific comments on MNOS structure made in this report are based primarily on current practices at the Westinghouse Advanced Technology Laboratories.

The MNOS transistor is an insulated gate field effect transistor with a two layer insulator. A simplified unscaled cross-section of a P-channel MNOS transistor is provided in Figure 3-6. The nitride layer thickness is typically  $300\text{\AA}$  to  $500\text{\AA}$ . If the transistor is intended to be a memory component, the oxide layer will typically be  $20\text{\AA}$  to  $40\text{\AA}$ . For a nonmemory transistor, the oxide would be greater than  $500\text{\AA}$ . The memory type MNOS transistor provides storage by injecting or removing charge from deep trap sites located near the oxide-nitride interface. Because a relatively large amount of energy is required to lift the charge out of the traps, long retention times are obtained.

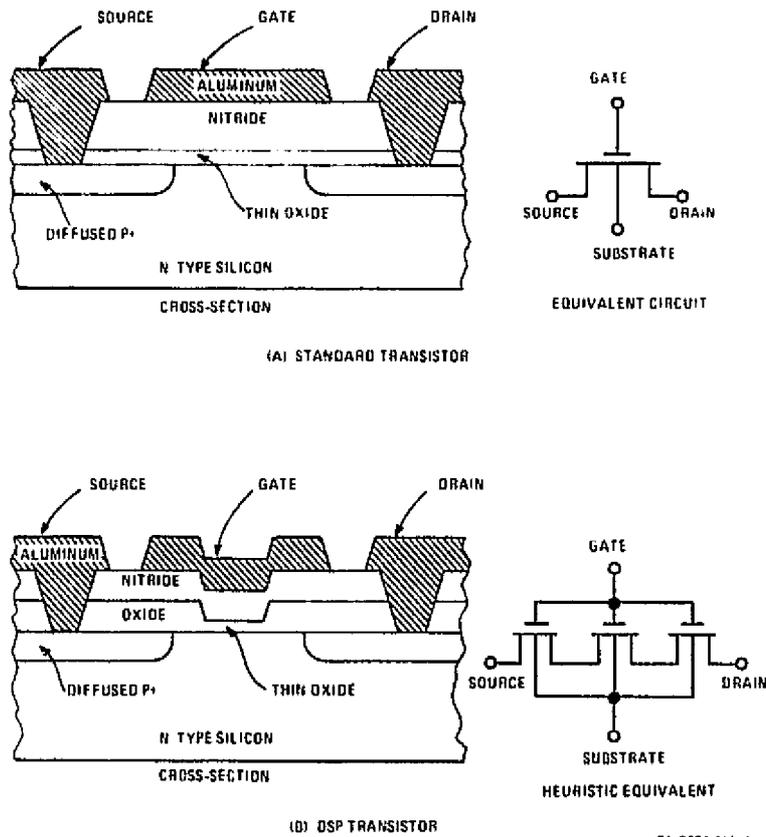


Figure 3-6. Unscaled Cross-Section of MNOS Memory Transistor

In an MNOS memory device, charges are transported to the oxide-nitride interface by tunneling through the thin oxide. Current flow in the nitride is negligible because it is much thicker than the oxide. Application of a positive gate voltage of sufficient magnitude will cause tunneling such that a net negative charge is stored at the oxide-nitride interface. This results in the device threshold being shifted in the positive direction. In a similar fashion, the application of a negative voltage of sufficient magnitude causes the threshold to shift in a negative direction. Small gate voltages do not disturb the threshold, and thus a nondestructive readout of the memory device is possible. A number of independent workers have contributed to the formulation of mathematical models which explain the behavior of MNOS memory transistors. Expressions for threshold voltage shift and retention characteristics have been developed based on a direct tunneling theory. The charge decay mechanism is tunneling from the deep traps to the silicon. Because tunneling is not a temperature sensitive process, both charge retention and the device overall operation are relatively temperature independent.

The conventional MNOS transistor shown in (a) of Figure 3-6 cannot be readily employed in integrated circuit memory arrays because of its tendency to operate in the depletion mode while in the positive threshold state. It also has the severe restriction that performance characteristics degrade with use. After about  $10^6$  clear-write cycles, the positive and negative threshold states cannot be distinguished. This state of affairs discouraged early development efforts. MNOS memory transistors did not in fact become suitable for widespread application until after the invention of the drain-source-protected (DSP) memory transistor by J. R. Cricchi

of Westinghouse. This device provides enhancement mode operation, eliminates voltage restrictions on the drain and source, and does not exhibit threshold window closure with clear-write cycling. Clear-write cycle tests have shown no significant degradation after  $10^{12}$  cycles. Part (b) of Figure 3-6 shows the DSP transistor in cross-section. The thin tunneling oxide is located some distance away from the  $P^+$  diffused regions. Thick nonmemory oxides are employed in those regions. Also depicted is the three transistor heuristic equivalent circuit for a DSP type MNOS device. The two outer transistors are nonmemory devices which can tolerate large gate-to-drain or gate-to-source voltages. The central memory device can be pulsed into a positive threshold depletion mode state, but since it is in series with two enhancement mode devices, the overall DSP structure continues to operate in the enhancement mode.

Circuit design is an important aspect of providing practical MNOS memory devices. While a transistor is not being addressed, the substrate to gate potential should be held at zero. This prevents nitride leakage effects from affecting retention time. The read circuit for the MNOS device must avoid read disturb effects. Writing and clearing circuits should consider both static and transient conditions to insure that safe operating margins are maintained at the MNOS memory gate. A number of satisfactory circuit solutions for these functions have been developed and are in use. MNOS writing and clearing does require voltages on the order of 20 or 30 Volts. With a well planned design of the on-chip peripheral circuitry, the driver circuitry required to operate at those voltage levels can be minimal. Recent chip designs have demonstrated that this is true. The point is of interest because early device designs required an unreasonable amount of external circuitry.

The ability to form memory and nonmemory transistors on the same chip is an important asset of any LSI technology. This gives MNOS a distinct advantage over technologies like magnetic bubbles which are not totally LSI in concept. The system designer does not have to be concerned with sense electronics nor critical signal to noise problems. No high current, high power drivers are needed. Quite often in logic systems it is an advantage to have a nonvolatile latch, register, or counter available. With MNOS these features can be incorporated right on an LSI chip. The Westinghouse Metering Subsystem chip is an example. This device has a nonvolatile counter along with other logic functions required for remote monitoring of residential power consumption.

Probably the most well known MNOS sub-technology is the electrically alterable ROM (read only memory). The ROM devices are designed for long retention. Long write times are required -- typically 10-to-100 milliseconds. Read time is a function of circuit design. Cycle and access times can be made quite small, but this has not been done in currently available devices. Commercial parts have been available since the early 70's from NCR and Nitron Corporation. NCR's latest device is a 4096 bit fully decoded EAROM (EAROM is an NCR trademark). This device is in high volume production to meet system requirements within NCR. It has a typical access time of 1.6 microseconds. The Nitron NC7010, which is a 1024 bit chip, has a typical access time of 20 microseconds. There are indications that development efforts by several major vendors will result in additional ROM products.

Obviously ROM oriented devices are too slow to be employed in the camera memory application. Work is currently underway to develop MNOS RAM chips, with the economic driving force being military requirements for radiation hardened nonvolatile RAM's in missile systems. Present systems

use plated wire which is expensive and heavy. Westinghouse is under contract to explore the feasibility of such chips for use in the next generation of Minuteman missiles. The nonvolatile RAM effort is an important landmark for the MNOS technology in that significant funding levels are involved. The benefits of this work will advance the state of the art for all of the MNOS sub-technologies.

A special class of MNOS RAM chips is designed for very high speed operation. For these devices read and write speeds below one microsecond are commonly required, with retention times on the order of minutes usually considered adequate. Because of the high speed and radiation considerations, special on-chip circuit techniques are employed. Power dissipation and bit density are secondary considerations. Although these devices are able to perform the Camera memory function, a drawback exists in that chips available within the next few years will probably be no larger than 1024 bits. The cost per bit would therefore be above the LST objective.

BORAM (block oriented random access memory) and NOVSAAM (nonvolatile sequentially access memory) chips are very similar in terms of their memory transistor structures. At the individual memory transistor cell level, clearing and writing are accomplished in 10-to-200 microseconds. Reading of an entire block of 32-to-64 bits requires less than 10 microseconds. Retention time varies with writing time, but is normally on the order of 4000 hours to several years. At the I/O ports of these devices much higher data rates are maintained than at the memory transistor level. Information is stored in an X-Y array with multiple bits written or read simultaneously. Data bit blocks are bidirectionally loaded between the storage matrix and a set of on-chip shift registers and shifted out of or into the chip serially at high speed.

BORAM devices are intended for secondary storage applications where data is handled in blocks of about 1024 bytes (a byte in this case being 8 bits). A BORAM system "module" typically ranges in size from  $10^6$ -to- $10^8$  bits. NOVSAM devices are intended for mass storage applications involving larger block sizes, such as in system ranging in size from  $10^8$ -to- $10^{12}$  bits. NOVSAM structures are, however, still in the test vehicle stage. These chips will ultimately have very dense arrays with more than 500 Kbits per chips. At the present level of support funding, several years of work are anticipated before this MNOS sub-technology achieves full fruition. MNOS BORAM technology, on the other hand, is being developed to meet the processing military need to replace electromechanical secondary storage devices which are not suitable for field use. MNOS BORAM offers both high reliability and nonvolatility, plus providing greatly improved performance. It will eventually compete on a direct cost basis with drums and discs.

At least two BORAM programs are currently underway. The U. S. Navy is sponsoring a module development with Univac in St. Paul, and the U. S. Army Electronics Command (ECOM) is sponsoring a module development with Westinghouse in Baltimore. Recently the Naval Air Systems Command joined in the sponsorship of the latter program. ECOM has broad ranging plans to bring the BORAM technology to the level of maturity appropriate to field application. This includes the establishment of a reliability data base and the improvement of the basic BORAM concept through better chip designs and simplified production processes. A portion of those plans have been implemented in specific contracts — three of which are of interest here. The primary ECOM contract is system oriented, and calls for the fabrication of an 18 megabit module. A second contract requires the performance of a

variety of accelerated stress tests on the memory chips. Analysis is to be performed on any failed parts to establish failure mechanisms and to provide feedback to the chip production effort. A third contract is concerned with the design of new BORAM chips to provide increased producibility and higher chip bit density. At present a 2048 bit BORAM chip is in production to meet the first module requirements. A new 8192 bit device will be phased into production during the last quarter of 1975. This latter device would seem to be in harmony with the 1978 timetable for System B. By that time a suitable reliability data base will exist to enable precise prediction of system reliability.

A memory system built with nonvolatile MNOS devices will retain its stored data unconditionally on power shutdown or interruption. This may prove to be an essential requirement for space applications, particularly where there is a high probability of supply disruptions. The implications of nonvolatility, however, go far beyond simple data retention. It has direct implications on the system reliability. Operation of a high-speed camera memory normally will involve only a few chips in data transactions at any given time. If the chips are volatile, they must all be in the active mode in order to retain data. If the chips are nonvolatile, only the chips engaged in the data transactions need be active. An MNOS part is in essence an MOS structure, and as such it shares the same failure modes and has the same failure rates. No pronounced differences in active mode failure rates have shown up in available test data. It is known that when electrical stresses are removed from an MOS part, its failure rate (dormant mode) drops more than an order of magnitude. This results in a reliability advantage for a nonvolatile system which becomes more dramatic for larger systems and/or longer mission times.

Obviously, a power switched nonvolatile system will have a power advantage over competitive memory technologies. Power will be determined by how many chips must be turned on simultaneously to meet data rate requirements. If minimum power (at the expense of data rate) is the major design objective, it is feasible to build a  $10^7$  bit memory with less than 1 watt of dissipation. In less esoteric applications, the benefits of low power are reduced power supply cost, weight, and volume, and lower temperature operation. This latter feature enhances reliability and reduces the cost, weight, and volume problems associated with heat removal.

As was mentioned earlier, MNOS charge storage is not a temperature sensitive phenomena. Consequently, the operating temperature range is established by the design margins allowed in the on-chip peripheral circuitry rather than by leakage in the memory cell. No critical temperature problems exist as with the bias margins of magnetic bubbles, or with the leakage limitations of N-MOS and CCD. Furthermore, the radiation resistance of MNOS memory cells has proven to be quite good. Presently MNOS is being studied seriously for use in radiation hardened systems. The limiting feature of memory chips for radiation tolerance is believed to be the on-chip peripheral circuitry. It appears reasonable to expect the peripherals to withstand more than  $10^5$  rads total dose. This is, of course, a function of circuit design and would have to be confirmed by tests on specific parts. Present BORAM chips use P-channel technology which is less sensitive than N-channel technology to surface damage induced by high radiation flux densities.

An MNOS memory cell can be made extremely small. The storage component is a single transistor which requires no storage capacitor as in

dynamic memories. BORAM chips currently under development have cells sizes on the order of 0.5 mils<sup>2</sup>. This is significantly smaller than the typical 1.3 mils<sup>2</sup> of CCD devices. As photolithographic capabilities improve MNOS density will improve and should remain well ahead of other semiconductor technologies. Demonstration of this point is provided by a recent study performed at Westinghouse by Dr. M. H. White. In that study an examination was made of the cell sizes which could be achieved by various technologies if give the equivalent capability of forming 2.5 micron lines and 2.5 micron spacings. The results of the study are summarized in Table 3-10.

Table 3-10.  
EQUIVALENTLY PROCESSED CELL AREAS OF ALTERNATE TECHNOLOGIES

technology	cell area (mils <sup>2</sup> )
MNOS	0.085
CCD	0.12
MOS (P or N)	0.16
Bubbles (4μ)	0.39
Bipolar	1.9
CMOS	3.2

A further attribute of BORAM type MNOS chips is their capability of efficiently transferring blocks of data at high rates. This factor comes about by way of the on-chip parallel transfer of data to shift registers which operate at 5 MHz rates over a wide temperature range. In contrast, the data rate of N-MOS RAM's is typically limited to less than 2 megahertz while CCD shift rates are limited to about the same speed by

the interposition of refresh stages. Manufacturers of these devices have indicated a low likelihood of guaranteeing much more than 2 megahertz within the near future.

MNOS provides a system advantage in that it avoids some of the off-chip overhead of other technologies. For example, CCD and N-MOS systems must have refresh logic. Magnetic bubbles are, of course, dependent on off-chip electronics for operation, and have a large ratio of off-chip components to memory chips. On the other hand, it should be noted that MNOS circuits will generally use (but not require) power switching circuitry. These circuits are low power and usually consist of a few transistor per printed circuit card. As is generally true of semiconductor technologies, MNOS interface problems are minimal. MNOS BORAM accepts voltage logic signal levels and outputs voltage logic levels. This facilitates easy addressing by any standard voltage logic family of binary elements (such as T<sup>2</sup>L or CMOS).

Like other semiconductor technologies, MNOS is batch fabricated and low cost per bit can be achieved. When the cost potential of MNOS is compared to that of N-MOS, MNOS costs are found to be significantly less on a per bit basis. N-MOS processing typically requires 5 masking operations while MNOS memories require 7 maskings. This means that, for equal physical size chips, the MNOS chip will cost about 15-to-20% more than the N-MOS chip. But, because of memory cell size differences, the MNOS chip should contain 2-to-3 times as many bits. Thus, the MNOS cost per bit should be 0.4 to 0.6 that of the N-MOS device.

It is difficult to make a direct cost comparison between CCD and MNOS devices because of unresolved conflicts existing in various claims

made regarding the complexity of CCD production. Existing CCD devices require as many as 10 or 11 photomask operations, but CCD advocates claim that a 6 photomask process is possible. In any case, the real factor of interest to a user is memory system cost. Because of the nonvolatility feature of MNOS and its associated benefits, MNOS will provide a significantly lower system price. This will be most dramatic when price is computed as cents/bit/year of operating life.

Upon drawing together the divergent factors that have been discussed, it is observed that the major merits of MNOS stem from its combined attributes of being an LSI technology and possessing nonvolatile memory cells. The tabular listing shown below points up the fundamental MNOS advantages which accrue to memory systems in which it is used. In summary, MNOS is an emerging memory technology with a wide range of applications. At least six distinct sub-technologies exist within the MNOS category. One of these sub-technologies, nonvolatile BORAM, can provide components suitable for use in spacecraft sensor instrument memories within the next few years. On chip multiplexing and high speed shift registers which are designed-in provide the required data rate capability. Suitable memory chips are now being developed to meet Army-Navy computer system secondary memory needs. This particular development effort is compatible with the System B camera memory timeframe. In light of the advantages cited for its use in table below, MNOS appears to constitute an excellent option for use in high-speed-access, spacecraft sensor instrument memory applications where the storage capacity is over  $10^6$  bits.

#### MNOS MEMORY SYSTEM ADVANTAGES

- Nonvolatile Storage
- High Reliability
- High Bit Density
- High Data Rate
- Good Radiation Resistance
- Temperature Insensitivity
- Easy Interface Provision
- Minimum Support Circuitry
- Low Power Dissipation
- Low Cost Batch Fabrication

#### 4.0 RELIABILITY EVALUATION

The long mission times and high probability of success (reliability) desired for space applications make reliability prediction an essential portion of any system design effort. In the case of the camera memory, it is necessary to perform some exploratory studies to determine the general practicality of various approaches to system implementation. The questions to be examined are the need for redundancy and the minimum acceptable bit density per chip. The following text defines the objectives and ground rules for the investigation, and then reports the separate findings for systems "A" and "B".

The purpose served by these reliability examinations is to ascertain whether or not it is indeed feasible to produce the desired spacecraft memory systems in a form that meets the reliability objectives that have been set forth. To do this, consideration is given to both nonredundant (simplex) and redundant memory design philosophies, and allowance is made for degraded modes of operation complying with the guideline requirements of the individual systems. The approach taken to the investigations consists of the use of mathematical models which reflect specific design constraints. These models are patterned after the analytical techniques established in the military standard handbook MIL-HDBK-217B.

#### 4.1 Modeling Approach

The camera memory reliability requirements are sufficiently complex that mathematical modeling must be used to determine the feasibility of proposed designs. The primary tool of this investigation is the circuit models defined by handbook MIL-HDBK-217B. The techniques of this recently released handbook are the only recognized authoritative means available for rapidly exploring the reliability of diverse memory system designs. It is anticipated that predictions resulting from this approach will be conservative because of the reliability learning curve which is characteristic of the integrated circuit industry. The statistical data base on which HDBK-217B is founded represents product performance achieved years before the models were issued.

The critical item in a memory system model is the memory chip. Section 2.1.4 of HDBK-217B treats monolithic forms of bipolar and MOS memories. MOS is defined as including N-MOS, P-MOS, CMOS, and MNOS fabricated on various substrates. CCD structures are not explicitly included (or excluded), but it is logical to project that, being based on a physical surface control phenomenon much like that of other MOS devices, they will exhibit a similar failure rate capability when fully matured. This has not as yet been confirmed, though, due to the comparative "newness" of CCD fabrication techniques.

The mathematical reliability model for a memory chip is a series of equations built up from the six basic terms shown in Table 4-1. The first two terms listed here reflect the status of the part as procured for a given application. The next two reflect the acceleration of the part failure rate by temperature. The final two reflect the acceleration of the part failure

rate by the stresses of the use environment. The fundamental "starting point" equation in which these six terms are employed is

$$\lambda_p = \pi_M \cdot \pi_Q \cdot (C_T \cdot \pi_T + C_E \cdot \pi_E)$$

which denotes the effective "failure rate" that can be expected from the given part under the constraints of a particular set of production and application conditions. A point of note here is that failure rates are commonly expressed in terms of "fits", with a fit being defined as

$$1 \text{ fit} = 1 \text{ failure in } 10^9 \text{ hours or part life.}$$

This terminology convention is adhered to in the following discussions.

Table 4-1. MOS FAILURE RATE MODELING TERMS

Term	Definition	Relationship
$\pi_M$	device maturity factor	(*)
$\pi_Q$	device qualification factor	(*)
$C_T$	temperature complexity factor	(1) $C_T = 1.99 \times 10^{-3} B^{0.603}$
$\pi_T$	temperature acceleration factor	(2,3) $\pi_T = 0.1e^x$
$C_E$	environment complexity factor	(1) $C_E = 560 \times 10^{-6} B^{0.644}$
$\pi_E$	environment acceleration factor	(*)

\* see text discussions

Notes:

- (1) B = number bits/device
- (2)  $T_j$  = junction temperature in °C
- (3)  $x = -8121 \left( \frac{1}{T_j + 273} - \frac{1}{298} \right)$

NASA has indicated that parts procurement for space missions like the LST will probably be per specification MIL-M-38510 Class B (JAN), with the added feature of part screening by NASA. According to the cited MIL reliability handbook, this type of buy produces a qualification rating factor ( $\pi_Q$ ) of 2. This is a conservative value for modeling purposes, as NASA retains the further option of actually buying at level A screening to secure an additional reliability margin ( $\pi_Q$  would then have a value of 1). The device maturity factor ( $\pi_M$ ) is provided to allow for the uncertainty associated with new or modified devices which have not been thoroughly debugged. For a new device  $\pi_M$  is assigned a value of 10. By the ground rules of this study, the devices used in the camera memory must be in production for other applications. It is therefore assumed that sufficient reliability history has been established to allow a  $\pi_M$  value of 1 to be used.

The MOS and bipolar models of HDBK-217B differ in the form of the temperature acceleration factor ( $\pi_T$ ). In this study attention is directed exclusively toward MOS devices. To use the model it is necessary to make some assumptions concerning the thermal environment. Because of the optical equipment in the instrument package, the LST will have some provision for regulating the temperature in that portion of the satellite to about 21°C. It is assumed that the chassis of the camera memory will be held close to that temperature. In the class of construction being considered for the memory it is reasonable to expect a thermal impedance of from 5-to-15°C/W from the chassis to the components on a multilayer circuit board. To ensure never exceeding a worst case operational temperature of 51°C, the average circuit board power must be less than  $(51-21)^\circ\text{C}/(15^\circ\text{C}/\text{W}) = 2$  Watts. The

power dissipation in the integrated circuits under consideration is quite low, however, so no more than a one or two degree rise is expected from case to junction.

Obviously there will be temperature differences from component to component, but for the purposes of this exploratory study all integrated circuits will be assumed to be at 50°C. This assumption is admittedly conservative, but is consistent with the present level of knowledge of the system. Table 4-2 shows the affect of temperature on failure rate for memory chips of different bit densities. Clearly this is a very important parameter, and control of the thermal environment is one design option available to achieve reliability goals.

Table 4-2. MOS CHIP FAILURE RATES IN SPACE ENVIRONMENT

Chip Capacity (bits/chip)	Junction Temperature (°C)							
	25	40	50	55	70	85	90	125
1,024	46	116	233	332	956	2,516	3,400	24,460
2,048	70	178	358	510	1,470	3,870	5,230	37,630
4,096	108	270	540	768	2,208	5,808	7,848	56,448
8,192	168	416	830	1,180	3,388	8,908	12,036	86,556
16,384	254	627	1,243	1,772	5,084	13,364	18,056	129,836

Notes: (1) All failure rates are stated in fits  
(1 fit = 1 failure-per-10<sup>9</sup> hours).

(2) All values given are derived using  
standard MIL-HDBK-217B practices.

The environment to which the camera memory is exposed will consist of a sequence of changing conditions. As an example, if system life is considered to start after the final test during manufacturing, the memory might experience an environmental exposure sequence as follows: transport, receiving test, storage, transport, preinstallation test, installation, prelaunch test, launch, and finally flight operation. The analyses conducted here focus on the flight environment for which HDBK-217B assigns  $\tau_E$  a value of 0.2. Obviously, at some more mature stage of development all of the environments should be considered. The launch phase, for instance, definitely imposes large mechanical stresses. But, the difference in the launch and flight time periods (plus the fact that the memory is not expected to be operating during launch) makes it reasonable to treat only the flight conditions at this time.

An implicit assumption of MIL-HDBK-217B is that component failure rates are constant (i.e., that failures occur according to an exponential time distribution law). The failure rate established by the HDBK-217B model represents what is known as the "active" failure rate. Active implies that the device has power applied. Contrastingly, when power is removed from the device it is considered to be "dormant" and exhibits a much lower failure rate. By agreement with NASA, the dormant state failure rate is modeled as one tenth that of the corresponding active state failure rate. It appears, however, that this treatment of the powered down state may be markedly conservative in light of additional data becoming available on dormancy.

In a recent publication<sup>(10)</sup> covering the results of work sponsored by Rome Air Development Center it was observed that, "Since the observed

failure modes and mechanisms for dormancy are the same as those for the energized state, it can be concluded that dormancy itself is not the causative factor. Rather, device material properties or incipient defects are. Both types of these failure mechanisms can be correlated with dormant time as well as operating time. The rate at which failures occur in dormancy is lower because of zero or near zero electrical stresses applied." Also included in this document is data indicating that class B monolithic integrated circuits of the complexity level of interest here typically exhibit failure rates of about 2 fits, while class A circuits of the same complexity have failure rates on the order of 1 fit. By way of comparison, note that the use of one tenth of the active failure rate from Table 4-2 for a 4096 bit chip at 50°C leads to an estimate of 54 fits.

Dormancy failure rates are applied in two ways to the analysis of the camera memory. First, NASA has specified that the memory will be used for 35% of the flight time. Thus, for 65% of the mission the entire memory is powered down and enjoys a dormant state failure rate—regardless of whether volatile or nonvolatile memory devices are employed. Second, if a nonvolatile technology is used, then most of the memory can remain powered down even during the 35% of the mission that the memory is operating. Consequently, the dormant failure rate continues to apply to all devices still having electrical stresses removed. The basic reliability equation denoting these factors is

$$R = e^{-N\lambda t/D}$$

where "D" is a dormancy improvement factor given by

$$D = \frac{K_\lambda}{1 + \left(\frac{K_\lambda - 1}{K_N K_t}\right)}$$

The terms employed in these two relationships are defined in Table 4-3. Points to note with regard to the dormancy factor (D) are:

- (1) all " $K_j$ " terms must satisfy the inequality

$$1 \leq K_j \leq \infty$$

- (2) as the  $K_N \cdot K_t$  product becomes  $\gg K_\lambda$ , the value of D approaches its upper limit of

$$D \leq K_\lambda.$$

Table 4-3. RELIABILITY MODELING TERMS

Term	Definition	Relationship
t	total mission time	1 year = 8766 hours
$\lambda$	chip failure rate	*
N	total chip count	*
$K_N$	total-to-active chip count ratio	(3) $K_N = \frac{N_{\text{total}}}{N_{\text{active}}}$
$K_\lambda$	active-to-dormant failure rate ratio	(2) $K_\lambda = \frac{\lambda_{\text{active}}}{\lambda_{\text{dormant}}}$
$K_t$	total-to-active mission time ratio	(1) $K_t = \frac{t_{\text{mission}}}{t_{\text{active}}}$

\* see text discussions

Notes:

(1)  $K_t = \left(\frac{1}{0.35}\right) = 2.857$ ; assuming a 35% duty cycle

(2)  $K_\lambda = \left(\frac{1}{0.1}\right) = 10$ ; with  $\lambda_d$  taken as  $0.1\lambda_a$

(3)  $K_N = \begin{cases} = 1; & \text{for volatile devices} \\ > 1; & \text{for nonvolatile chips} \end{cases}$

For reliability analysis purposes, it is assumed that the memory can be modeled as two lumped equivalent circuit parts. The first part will be called the "storage circuitry" section. It contains the memory chips plus a minimum of buffers and drivers. The second part will be called the "peripheral circuitry" section. It contains the control electronics, data adder, signal routing, and all other related devices necessary to the operation of the memory. A single failure in the "peripheral" circuitry in this simplified model is considered to cause a mortal failure of that section of the memory. A single failure in the "storage" circuitry, on the other hand, causes the loss of an elementary failure unit segment of the memory. Whether or not this is amortizing to the memory section as a whole depends on the failure definition of the system (i.e., the number of unit failures that can be tolerated before the memory section is considered functionally useless).

Allowance for a degraded mode of operation for the memory gives the designer some degree of freedom in establishing boundary conditions for the achievement of high reliability with a minimum of overhead redundancy in the data storage or peripheral supporting circuits. A point on which this bears is the system organization as it is affected by the number of I/O data lines available in parallel from each memory chip. Most commercial chips have only a single set of I/O lines. This fact requires that the number of bits of storage on any given chip correspond to an equivalent number of words of memory; and that, to supply the number of bits needed in each word, an equivalent number of separate chips be interconnected in an elementary failure unit segment and operated in parallel. Without error correction redundancy circuits present, a failure of any one of these chips amortizes the entire elementary unit.

In a totally nonredundant design there is no motive for having successive bits of a stored word located in separate chips. Contrarily, in fact, the use of memory chips having multiple outputs should be given serious consideration since this would allow either the system power (in the case of volatile devices) or the number of powered up devices (for a nonvolatile technology) to be minimized. Although the presence of multiple outputs will increase the per chip failure rate slightly, it facilitates a significant reduction in the number of chips assigned to each elementary segment (ELSEG). If the memory word size is 16 bits, then 16 single I/O chips would be required to form a segment. Use of a chip having 8 parallel I/O's, on the other hand, would mean that only 2 chips are needed per segment. Consequently, the failure of a chip (and hence of a segment) will effect a smaller fraction of the total memory. It therefore appears that at least a cursory trade off study of this option might be worthwhile during the camera memory breadboard development.

## 4.2 Feasibility Analysis

To determine the total memory reliability ( $R_M$ ), the reliability levels of the storage array ( $R_S$ ) and the peripheral circuitry ( $R_P$ ) can be computed independently using the foregoing equations and then multiplicatively combined as

$$R_M = R_S \times R_P$$

For the LST application, it is stipulated that the camera memory must have a composite reliability ( $R_M$ ) of at least 0.95 over a 1 year mission time (t) while operating at a 35% powered up duty cycle. The failure rate budget ( $N\lambda$ ) permitted by these conditions must be shared in some fashion between the storage array and peripheral circuitry.

As a first-order approximation, the circuitry required to implement the peripheral functions can be taken as being about 200 integrated circuits. To ensure against obtaining results that are overly optimistic, a conservative effective failure rate to use for these parts would be 50 fits at 50°C. This implies a failure rate budget requirement for the peripheral IC's of

$$N \times \lambda = 200 \times 50 = 10,000 \text{ fits}$$

Upon allowing an additional 1,500 fits for the various circuit boards, connectors, and passive components, it is seen that a total "peripherals" budget of around 11,500 fits should be allowed. Additionally, if this circuitry is implemented in a non-redundant, volatile form, it will have a dormancy improvement factor of

$$D = \frac{10}{1 + \left( \frac{10 - 1}{1 \times \frac{1}{0.35}} \right)} = 2.4096$$

under the given system operating conditions.

By using these two values in the general exponential reliability equation, the anticipated reliability of nonredundant peripheral support circuitry for alternate one, two, and three year mission times is found to be

$$\underline{1 \text{ year}}: R_p = e^{-11,500 \times 8766/2.4096} = 0.959$$

$$\underline{2 \text{ year}}: R_p = e^{-11,500 \times 17,532/2.4096} = 0.920$$

$$\underline{3 \text{ year}}: R_p = e^{-11,500 \times 26,298/2.4096} = 0.882$$

From this it is concluded that nonredundant common electronics in a spacecraft memory appears practical over a 1 year mission period. For a 2 year mission, though, the circuit designer would be hard pressed to maintain an acceptable reliability level. The concordant implication for a 3 year mission is that redundancy will probably be mandatory.

To conduct an equivalent examination of the "storage" array section of the memory, certain general assumptions must be made regarding its basic functional architecture. In the analyses that follow it is presumed that memory chips having only single input and single output data lines are used. This necessarily implies that, to form a 16 parallel bit word, 16 chips must be operated together. If any one of these 16 chips fails, an "elementary segment" (or simply ELSEG) group of words fail. The number of words per ELSEG is equivalent to the number of bits per chip. Modeling of the storage array is as a set of independent ELSEG's wherein the failure of one does not affect the operation of any other. Further specific conditions are prescribed separately for systems A and B.

#### 4.2.1 System A

For use aboard LST-1, the System A camera memory is conceived as being composed of two identical sections, with the storage capacity of each being 16,384 words. A failure of any ELSEG in either section is taken as being fatal to that section, but the system as a whole is considered to be operational so long as one or both sections are functional. With the memory subdivided in this manner the reliability requirement of each section ( $R_{\alpha}$ ) is related to the total system reliability ( $R_M$ ) according to

$$(1 - R_M) = (1 - R_{\alpha})^2$$

which, in terms of  $R_{\alpha}$ , is

$$R_{\alpha} = 1 - \sqrt{1 - R_M}$$

Since it is required that  $R_M$  be 0.95 (i.e., that the system have a 95% probability of success), the per section reliability must be

$$R_{\alpha} = 1 - \sqrt{1 - 0.95} = 0.7764$$

or, in other words, it must have about a 78% probability of success.

Detailed examination of the per section failure rate budget is facilitated by solving the general reliability equation in terms of " $N\lambda$ ". This process yields

$$(N\lambda)_{\alpha} = - \left( \frac{D}{t} \right) \ln (R_{\alpha})$$

If it is assumed that the memory is implemented in a nonredundant (or "simplex") form using volatile storage devices, solution of the above equation produces

$$(N\lambda)_{\alpha} = - \left( \frac{2.4096}{8766} \right) \ln (0.7764) = 69,570 \text{ fits}$$

Given this failure rate budget, is it a reasonable undertaking to build the System A memory sections in a nonredundant form? If so, what size memory chip is practical? To answer these questions, reference is made to Table 4-4.

Table 4-4. SYSTEM A SINGLE SECTION FAILURE RATE BUDGET

memory chip storage capacity (bits/chip)	memory chip failure rate (fits)	total memory chip count (chips/section)	failure rate required by memory chips (fits)	failure rate left over for peripherals (fits)
1,024	233	256	59,648	9,924
2,048	358	128	45,824	23,748
4,096	540	64	34,560	35,012
8,192	830	32	26,560	40,012
16,384	1,243	16	19,888	49,684

In this table a complete breakdown is given of the failure rate budget allotted to the memory chips and the amount left over for peripherals using different size chips.

Upon reviewing the values listed in this table in light of the available budget it is concluded that a nonredundant design for System A can indeed provide a viable implementation. Furthermore, it appears that the choice of a 4096 bit chip will allow a comfortable failure rate budget for both the storage array and peripheral circuitry sections, with an adequate design margin in reserve to ensure achievement of the reliability goal.

#### 4.2.2 System B

For use aboard LST-2 and later flights, the System B camera memory is conceived as being composed of a single section which has a capacity of 262,144 words. Using single I/O 4096 bit chips, the memory structure consists of 64 ELSEG's which have noninteractive failure mechanisms. The failure of a single chip in any given ELSEG thus results in the loss of 4096 words. The criteria for system failure is the loss of more than 10% of the total memory words — i.e., > 26,214 word. Under the assumed organizational constraints, this translates into a mortality state definition of 7 ELSEG's. As a working hypothesis, the reliability of the peripheral circuitry ( $R_p$ ) is taken as being a minimum of 0.955 for any mission time. This implies that the reliability of the storage array ( $R_s$ ) must satisfy the condition

$$R_s \geq R_M/R_p = 0.95/0.955 \approx 0.995$$

to ensure that the composite memory attains its assigned reliability goal.

The probability of success for the storage section is formulated as the probability of having 58 or more of the 64 ELSEG's operational using the binomial distribution relationship

$$R_s = \sum_{k=58}^n \binom{n}{k} (R_E)^k (1 - R_E)^{n-k}$$

In this truncated series, " $R_E$ " is the reliability of an ELSEG; which, in turn, is expressible in terms of the chip reliability ( $R_C$ ) as

$$R_E = (R_C)^{16} = e^{-16\lambda t/D}$$

Using volatile chips, all ELSEG's must be active whenever the system is being exercised. The associated volatile dormancy factor ( $D_v$ ) has a value of

$$D_v = 2.4096$$

derived in the same manner as explained earlier. With nonvolatile chips only 2 of the 64 ELSEG's must be active at any given time while the memory is operating. Consequently, the nonvolatile dormancy factor ( $D_N$ ) has an improved value of

$$D_N = \frac{10}{1 + \left( \frac{10 - 1}{\frac{64}{2} \times \frac{1}{0.35}} \right)} = 9.1038$$

A comparison of the relative roll-off in System B storage section reliability versus mission time for volatile and nonvolatile 4096 bit chips is presented in Figure 4-1. This data was obtained by programming the binomial reliability distribution expression and performing a series of exploratory computer runs on TYMESHARE.

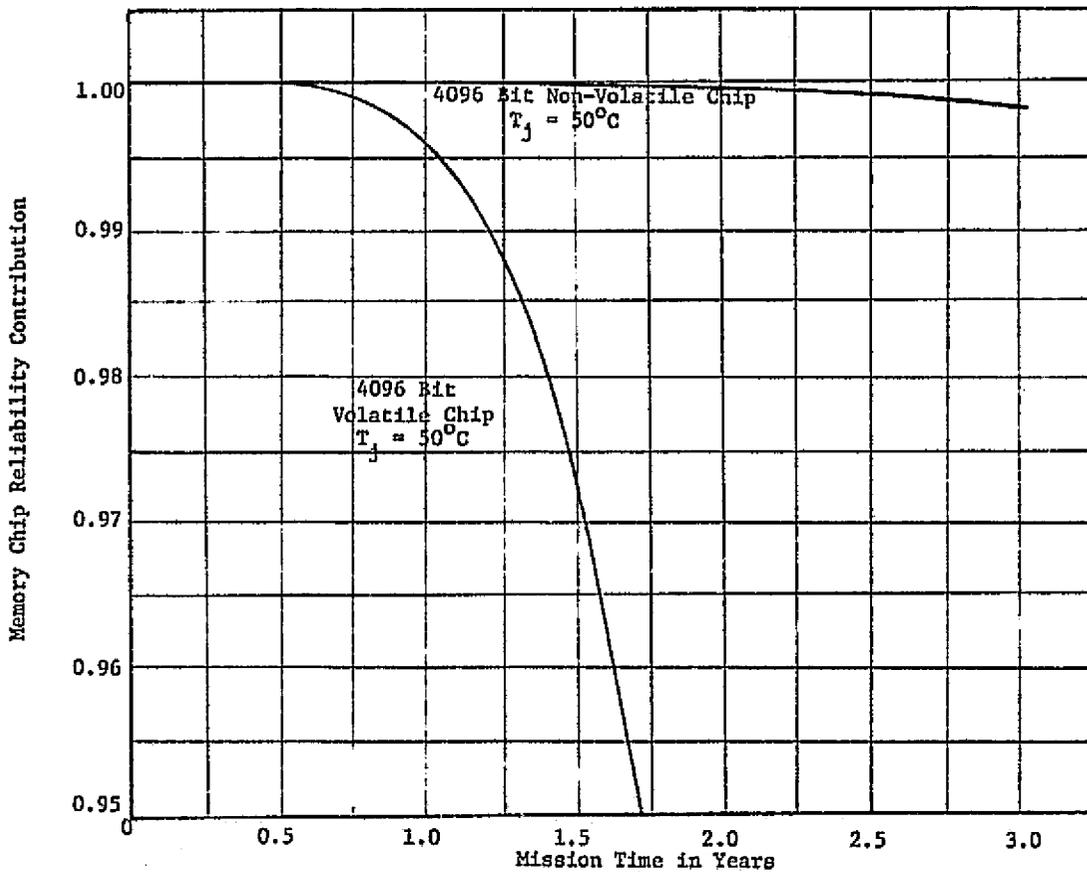


Figure 4-1. System B Reliability Versus Mission Time

Given the criteria of 0.995 reliability, the curves of Figure 4-1 indicate that a volatile storage form of the System B memory would just make a one year mission. At the one year point the predicted reliability is 0.996. During the second year of operation it decreases to 0.906. After three years it falls off drastically to a level of 0.647. A nonvolatile storage section is seen to hold up much better. At the end of one year it exhibits a computed probability of success of 0.999998. Over the second year its reliability decreases only slightly to 0.99985. After three years of service it still maintains a predicted capability of 0.9984.

To exploit the reliability potential of nonvolatile devices power switching must be employed. Improperly designed switching circuitry could, of course, degrade overall system reliability. For the types of memory circuits considered this should not be a problem since very small amounts of power are involved and the switches can be heavily derated if necessary. Operation of the power switches will be very similar to the repeated operation of a simple logic gate. Their use has the obvious supplemental attribute— in addition to facilitating enhanced reliability — of reducing system power and thereby easing thermal management constraints by de-energizing all devices not explicitly in use.

Drawing together the multifaceted aspects of the exploratory modeling that has been conducted, it is concluded that the System B reliability goals — interpreted literally, exactly as given — can be met using volatile or non-volatile memory chips in a SIMPLEX storage section design. With volatile chips, though, little if any design safety margin exists. It is clear that nonvolatile chips return a significant reliability dividend, and thereby allow consideration

of much longer mission times and/or larger memory capacities. A point of awareness is that a major contributing factor in the feasibility of a non-redundant storage unit is the 10%-word-failure fault tolerance stipulation made in the system requirements. Designs for the common peripheral support circuits are affected very little by this provision, however, so some reliability enhancement through redundancy appears desirable in those areas.

## 5.0 SYSTEM CONSIDERATION

The discussions thus far have been fundamentally general in nature. This was necessary to facilitate the gross investigation of a broad spectrum of memory technologies. The disclosures made through these "broad-brush" treatments which have direct bearing on system considerations are:

- rejection of all but three technologies (namely N-MOS, CCD, and MNOS)
- decision to treat two memory systems (one for LST-1 and one for LST-2)
- definition of the electrical interfaces (according to diagram in Figure 2-2)
- delineation of the functional requirements (summarized in listings of Table 2-2)
- selection of nonredundant design approach (acceptable reliability up to  $10^7$  bits)

By carefully weighing the respective application parameters against the inherent capabilities and limitations of the individual technologies, a final determination can be made of their suitability for implementation as the storage media in high speed sensor instrument memory systems to be used aboard spacecraft.

To ensure the highest possible measure of objectivity in the respective evaluations, a full development is made of the data storage processes exhibited by the individual technologies, and functionally equivalent system architectures are evolved for each. Points of divergence among these memory organizations are examined with respect to their affect on system performance and power drain. All calculations made are based on the use of N-MOS, CCD, or MNOS devices possessing confirmed operational characteristics. Supplemental factors — such as radiation hardening, reconfigurability, and redundant circuitry — are reviewed to determine their overall affect on system parameters and thereby adjudge their relative merits.

## 5.1 Storage Concepts

With the interfaces and functional requirements for the camera memory established from Section 2 it is now necessary to delve into the memory structure to determine the effects these requirements have on its overall organization and what alternatives remain open. Obviously, for the camera memory to accomplish its prime task of receiving binary sensor data, adding it to prior data, and restoring the sum in a continually updated cycle of events, it must have not only a data storage section but also sufficient peripheral sections to perform the necessary data coordination and processing operations. Figure 5-1 presents a first-order diagram of the LST camera memory functional concept. This diagram is intentionally generalized to make it independent of the memory technology being considered. Design details within the respective blocks will reflect the constraints of the particular technology employed.

As it stands, Figure 5-1 shows that the camera memory concept demands that there be five distinctly identifiable circuitry subgroupings within the unit. The central block is, of course, the data storage section. Around it are found: (1) the timing and control section, into which all external control signals are routed, and from which issues all sequencing directives to the other memory sections; (2) the data I/O interface with the outside world, through which passes input write data which will be summed with previously stored data and returned to storage, and output read data as it is transferred to a companion machine; (3) the data summer, which performs the actual operation of combining the new and old data into a single resultant parcel of data; and (4) the read/write interface, through

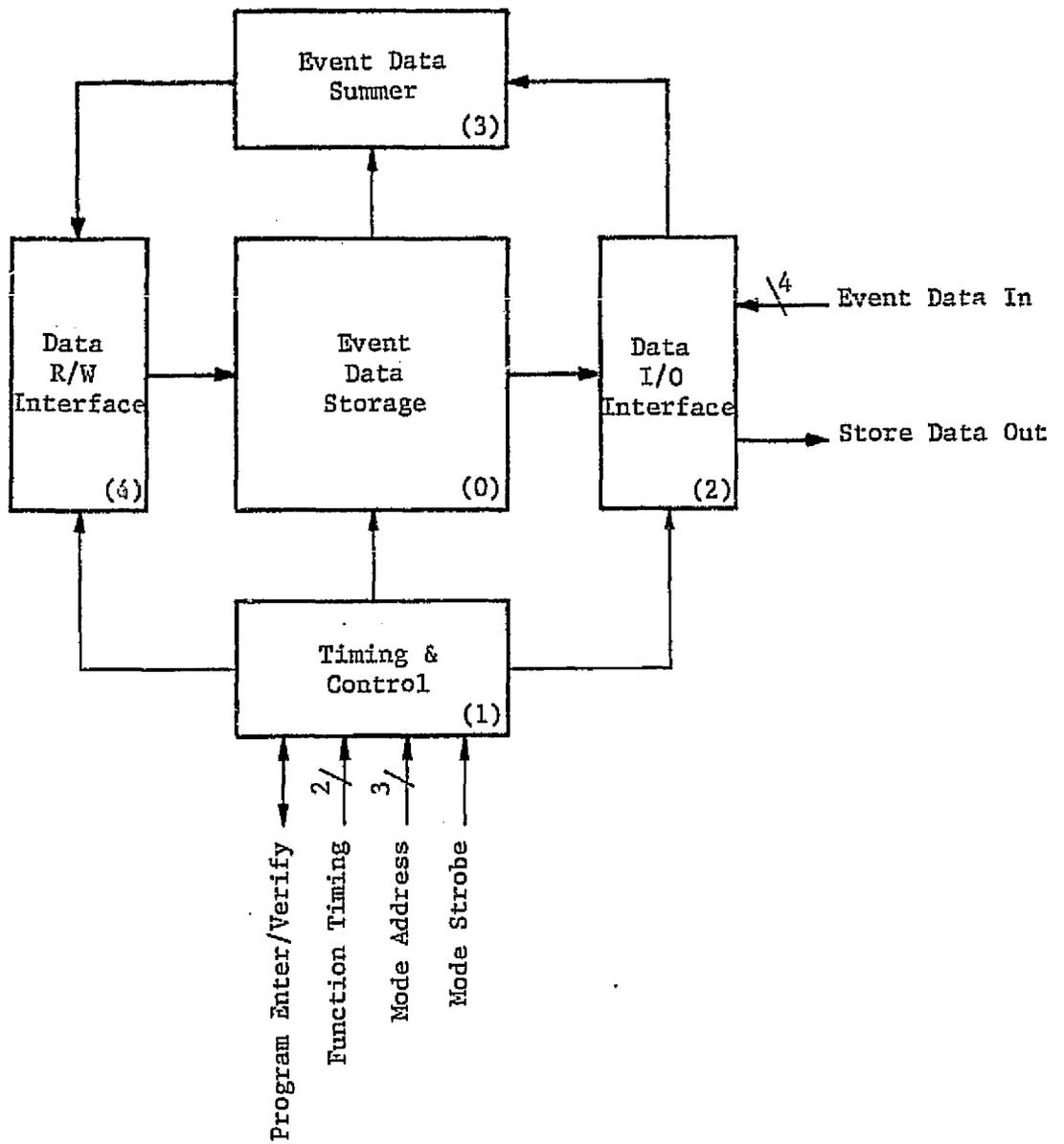
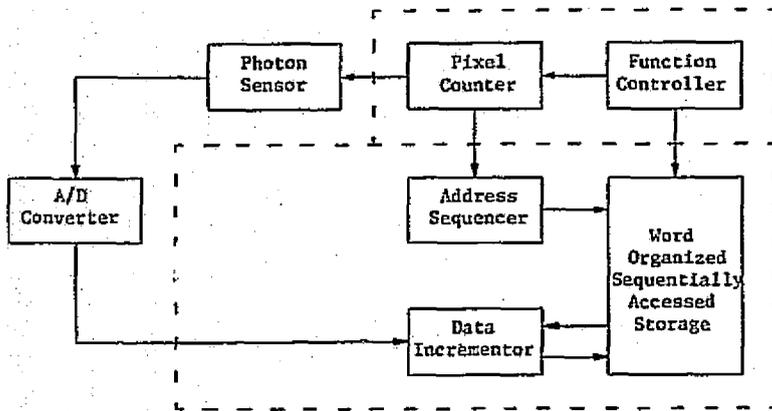


Figure 5-1. First-Order Camera Memory Functional Concept Diagram

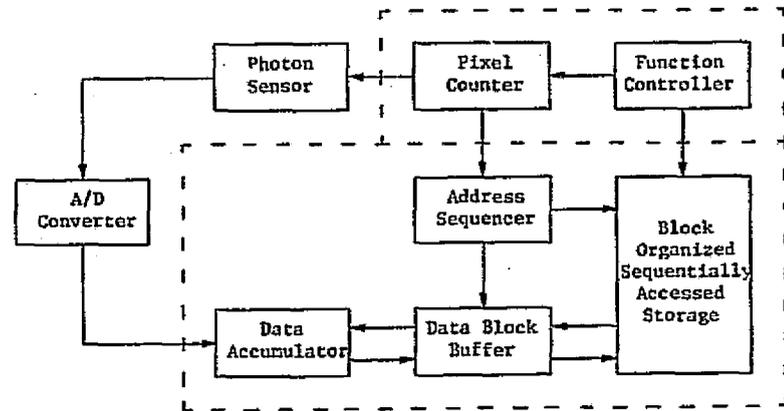
which passes the modified (or summed) data parcels that are written back into storage, and which originates the sequencing signals involved in executing a read or a write cycle by the data storage section. The same electrical interface signals to the memory (less supply and test port lines) appear here as were shown previously in Figure 2-2.

Within the framework of the camera memory functional concept depicted by Figure 5-1, it is possible to envision two primary architectures for the memory. These are: (1) a word organized memory and (2) a block organized memory, either of which may be (a) sequentially or (b) random accessed. Figures 5-2 and 5-3 present technology independent block descriptions of the four resultant system organizations (note that for completeness in visualizing the various system interactions, the photon sensor and A/D converter — both of which are part of the camera unit rather than the memory unit — are included in these diagrams, and a single pixel counter is depicted rather than separate ones for the camera and the memory).

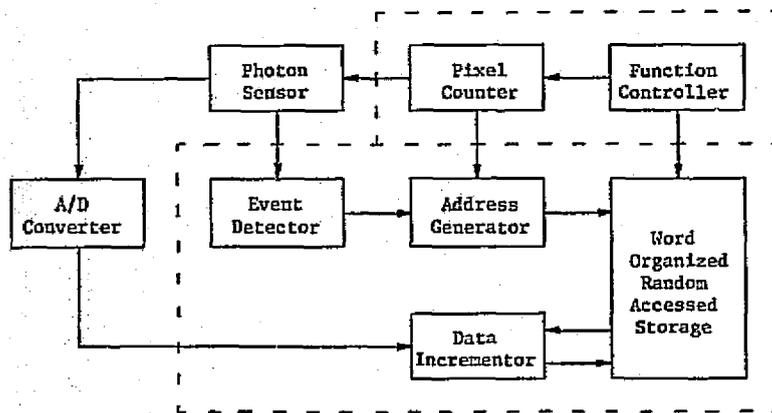
The fundamental difference between the "word" and "block" organizations is the size of (total number of bits in) the data packet which is processed as a unit during an access operation with the memory. An access order to a word organized memory results in a single data word being coupled to its output port. An access instruction to a block organized memory causes a multi-word data packet to be coupled to its output port. In systems where the machine or subsystem making the data accessing request of the memory acts individually on data words, word organized memories are the obvious (but not exclusive) choice and are therefore most frequently used. An equivalent observation applies to block organized memories in systems where the requesting machine always acts collectively on multi-word blocks of data.



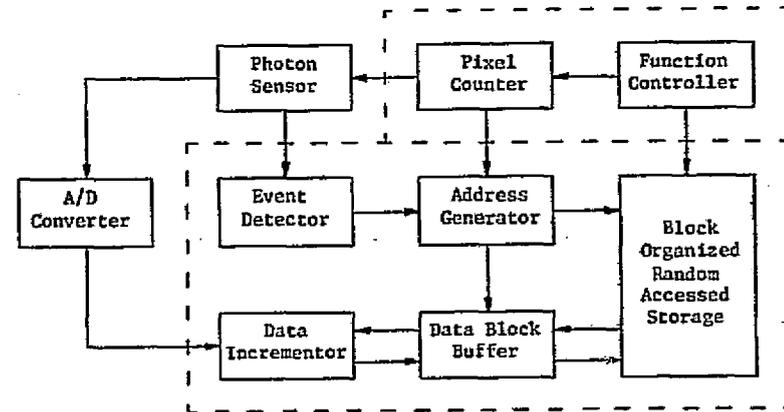
(a) WOSAM



(A) BOSAM



(b) WORAM



(b) BORAM

Figure 5-2. Data Word Memory System Structures (Technology Independent)

Figure 5-3. Data Block Memory System Structures (Technology Independent)

An additional point of difference between the word and block organized memory formats is that with the block format a temporary storage buffer having sufficient capacity to hold the entire block of data that has been addressed must exist (this function is frequently accomplished "on-chip" by the storage device), whereas with the word format there is no such requirement and the memory can interact directly with the data word incrementor. Upon comparing the sequential (SAM) and random (RAM) accessed memory organizations it is found that the SAM address "sequencer" runs continuously to keep the memory cycling in step with the sensor scanning. The address "generator" of the RAM, on the other hand, only functions to hold detected photon event pixel addresses long enough for the memory to increment the data stored in those address locations. It is otherwise quiescent with regard to input and output operations.

In conjunction with this it will be observed that a SAM does not employ an event detector (while a RAM does) because its data accessing operations are continuous (while the RAM's are intermittent). As a result, the power drain of a SAM tends to be constant, independent of the photon event accumulation data rate. Contrastingly, a RAM displays a direct variance in power drain with the received photon event rate. Which organization shows the lowest power dissipation at any given data rate is largely dependent on the parameters of the devices used to implement the memory.

A final point to be cognizant of before proceeding to considerations of specific memory devices is that, as established here, storage within the memory is based on a one-to-one correspondence between a memory address and an elemental detector site in the sensor array (i.e., a picture element — commonly referred to as a "pixel"). It is conceivable to base the storage of detected photoelectron event data from the camera on the

principle of recording the pixel address, but this would be a very inefficient use of memory. Also plausible is the use of a bank of binary counters interconnected to hold the array of pixel data, but this would be exceedingly inefficient at the storage cell level and would dramatically degrade the effective bit storage density of the system. Under the storage philosophy adopted, a record is maintained of the number of events which occur at each pixel by storing a 16 bit binary encoding of that number in a file location having a prescribed address.

## 5.2 Device Alternatives

Selection of a specific memory device imposes a number of design constraints on the fundamental memory organizations that have been discussed. The three device technologies that will be reviewed here are N-MOS, CCD, and MNOS. As pointed out in the technology survey of Section 3, these LSI technologies are the ones which hold the greatest promise of being able to fill the LST camera memory requirements within the assigned time frame. The potentially viable devices obtained from the N-MOS and CCD technologies are dynamic and volatile in nature. This means that their individual storage cells must be powered continuously and be refreshed at regular intervals (typically within 2 milliseconds @ 70°C) to ensure retention of their assigned data states. The devices secured with the MNOS technology, on the other hand, have static, nonvolatile storage cells. Consequently, they can be quiescent or even totally powered-down and still retain their data. At the storage cell level there is a slight speed penalty paid for the MNOS nonvolatility (i.e., it takes longer to write into an MNOS cell than into a CCD or N-MOS cell), but this factor is made virtually transparent at the system level by special structuring of the on-chip I/O cell interface circuitry.

In the following paragraphs an examination is made of the chip organizations which have evolved for the three prime technologies. Camera memory structures based on each of these technologies are evaluated in the context of the system "A" and "B" applications to determine whether the respective data rate requirements and power budget limitations can be met by the available alternatives. An intercomparison of the results of the individual discussions is then made to determine which candidate(s) should be pursued for each system.

### 5.2.1 N-MOS

While numerous memory devices have been built from the basic MOS technology, only the most recent 4 Kilobit N-MOS RAM's have sufficient per chip bit density to be serious contenders for the LST camera memory application. These devices are well characterized and are available from a rapidly proliferating number of commercial sources at highly competitive prices. From this standpoint they are very attractive. Table 5-1 presents a full listing of the major semiconductor houses that have committed to the production of 4K/N-MOS RAM's. Also indicated are the devices which are intrinsically compatible and the availability time frame for production quantities of each. Note that the specific device numbers given are representative only and by no means constitute a complete listing since several manufacturers have brought out multiple and improved versions of their devices.

While there are differences in fabrication and/or constructional detail (e.g., different chips use different numbers of rows and columns, and some chips have 3T cells while others use a 1T storage cell), the standard line of 4K RAM's all employ a functional organization like that depicted in Figure 5-4. A row decoder selects 1-out-of-N rows of M memory cells to be coupled simultaneously to their respective column sense amplifiers and write-in buffers. The column decoder interface section then selects 1-out-of-M of the available columns to be coupled to either the data input or data output line, depending on whether the chip is currently in its read or write mode of operation. The processes of inputting, outputting, and refreshing data are initiated by a "Chip Enable" clocking pulse (not cited specifically in Figure 5-4).

Table 5-1. 4K/N-MOS RAM SOURCES

Manufacturer	Device Number	Availability	Compatibility
MIL	MF7112	Now	(none)
Motorola	MCM6605L	Now	AMI part
AMI	S6605	Now	Motorola part
AMS	AMS6004	2nd quarter '75	RCA part
RCA	WM7004D	1st quarter '75	AMS part
Mostek	MK4096	Now	Fairchild part
Fairchild	4096D	2nd quarter '75	Mostek part
Electronic Arrays	EA4096	2nd quarter '75	Mostek part
Western Digital	WM1701H	Now	Intel part
Electronic Arrays	EA2107	1st quarter '75	Intel part
AMD	AMD2107	2nd quarter '75	Intel part
MIL	MF2107C	1st quarter '75	Intel part
TI	TMS4030	Now	Intel part
Intel	2107B	Now	TI part
Signetics	N2605	Now	TI part
National	MM5270	2nd quarter '75	TI part
Intersil	(no # available)	3rd quarter '75	TI part
Harris	(no # available)	3rd quarter '75	TI part

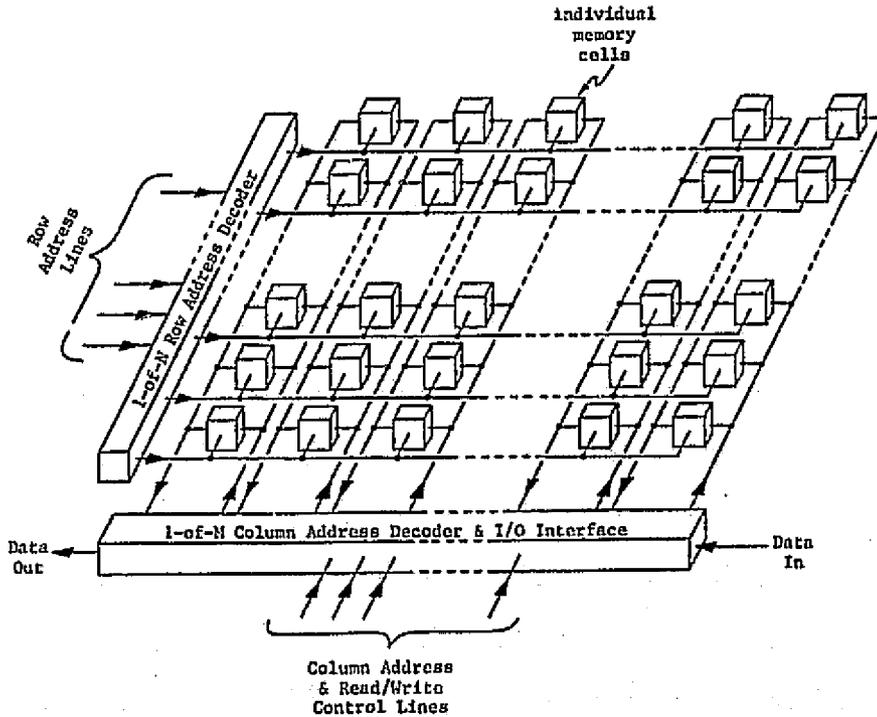


Figure 5-4. Random Accessed N-MOS Memory Chip Functional Diagram

Refreshing of stored data is normally carried out row-at-a-time on M cells simultaneously by individually exercising each of the N rows on the chip while it is deselected and neither inputting nor outputting data. A complete sequence of refreshes for all cells on a chip requires N row address cycles. Commercial grade chips must be refreshed within each 2 millisecond interval to ensure retention of their correct cell states at an operating ambient of +70°C. Industry representatives<sup>(11)</sup> are working to finalize a set of military standard 883 level B type specifications for an operating temperature range of -55°C to +100°C. Included in these specs is a refresh period of 0.5 milliseconds @ +100°C. From the general refresh relationship for N-MOS dynamic RAM's,

$$2^{(T_o - T)/\delta} \times \tau_{\text{refresh}} \times f_{\text{clock}} = 2^\eta = N_{\text{rows}} \quad (@ T_o)$$

where  $\eta$  = number address bits cycled for complete chip refresh and  $\delta$  is nominally 10°C, it is seen that this proposed mil spec refresh interval constitutes a factor of two improvement over current commercial grade specifications when referenced to a common operating temperature.

Table 5-2 presents a cross-section of the guaranteed worst case +70°C operating specifications for representative 4K/N-MOS RAM's that are available as standard line items. This table also includes the nominal operating voltages, package pin counts, and current manufacturer quoted book prices for various quantity level purchases. While all chips except the Mostek device are shown as being supplied in a 22-pin pack, there have recently been announced 18-pin pack versions by manufacturers like TI and National which do not require the address multiplexing that is necessary

Table 5-2. GUARANTEED WORST CASE SPECIFICATIONS FOR REPRESENTATIVE STANDARD-LINE 4K/N-MOS RAM'S

	Motorola MCM6605L	AMI S6605A	Intel 2107B	TI TMS 4030	MIL MF2107C	Western Digital FML701H	Mostek MR4096	RCA WM7004D	Concensus Specifications
Nominal Supply Voltages: $V_{DD}$ (Volts)	+ 12	+ 12	+ 12	+ 12	+ 12	+ 12	+ 12	+ 12	+ 12
$V_{CC}$ (Volts)	+ 5	+ 5	+ 5	+ 5	+ 5	+ 5	+ 5	+ 5	+ 5
$V_{SS}$ (Volts)	0	0	0	0	0	0	0	0	0
$V_{BB}$ (Volts)	- 5	- 5	- 5	- 3	- 3	- 5	- 9	- 5	- 5
Nominal Supply Currents: $I_{DD}$ (mA)	36	40	35	35	40	35	30	40	35
(at maximum) $I_{CC}$ (mA)	1	1	1	1	1	1	1	1	1
(cycle rate) $I_{BB}$ (uA)	100	200	100	100	100	100	100	100	100
Nominal Power Drains: active (mW)	350	400	400	400	400	400	400	500	400
refresh (mW)	3	2	2	2	2	2	12	5	3
Refresh Parameters: control bits	5	5	6	6	6	4	6	6	5
@ up to 70°C cycles/refresh	32	32	64	64	64	16	64	64	32
ambient temp total period (ms)	2	2	2	2	2	2	2	2	2
cycle rate (KHz)	16	16	32	32	32	8	32	32	16
Read Access Time (ns)	300	300	300	300	300	300	350	250	300
Read Cycle Time (ns)	470	470	500	470	470	470	500	380	500
Write Cycle Time (ns)	590	600	500	470	470	470	500	380	600
Read-Modify-Write Cycle Time (ns)	690	700	700	710	710	710	700	640	700
Address & Data Line Capacities (pF)	5	6	7	7	5	6	10	6	6
Chip Enable Line Capacitance (pF)	30	30	30	27	23	30	(N.A.)	30	30
Device I/O Pinout Count	22	22	22	22	22	22	16	22	22
Device Costing: 25 pc quant (\$)	--	33	31	33	--	28	42	26	30
(1st Quarter) 100 pc quant (\$)	22	26	26	26	28	24	28	21	25
'75 Vendor) 1K pc quant (\$)	16	--	--	22	23	--	22	14	20
Book Prices									

Most attractive parts appear to be: (1) Motorola's MCM6605L - due to fastest available RMW cycle at lowest power drain  
(not necessarily in order) (2) MIL's MF2107C - due to greatest ease in testing to flight qualification levels

with the 16-pin Mostek unit. In the final column of this table will be found what is called a "consensus specification" for a fictitious device having the average or most common specifications. These will be referred to throughout this report when considering any phase of detailed design implementation of the LST camera memory using 4K/N-MOS RAM chips.

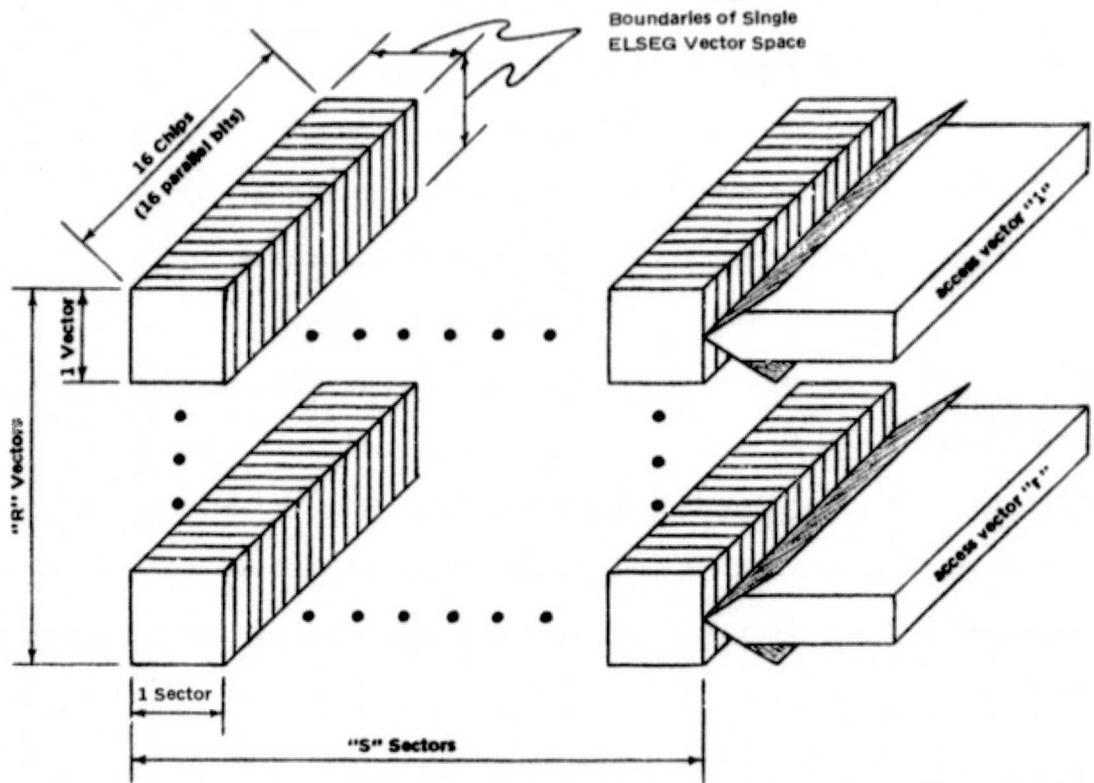
Memory Module Configurations. As illustrated in Figure 5-4, available 4K RAM's are organized at the chip level to process only a single read-out or write-in bit of data through their I/O interface upon receiving an access request. Due to this, each individual chip can contribute only one bit to successive bit-parallel pixel words as needed in an LST camera memory. There have, of course, been smaller capacity MOS memory chips built with the ability to process two or even four storage bits simultaneously, but the devices in this category have insufficient per chip capacity to be contenders for the present application. An advantage to their class of operation, however, is that fewer chips would be needed to produce a 16 parallel bit data word. With the standard 4K devices, a 16 chip assembly is required to form an "elementary segment" (ELSEG) of storage which has a capacity of 4096 words by 16 parallel bits/word.

From the consensus device specifications of Table 5-2 it is seen that, allowing for 100 nanoseconds to perform the data summing function in an external circuit, individual ELSEG's can execute a read-modify-write (RMW) cycle in about 800 nanoseconds or, equivalently, can process words at a 1.25 MHz rate. This means that to attain the 3.0 MHz peak event counting rate demanded for System A, at least 3 ELSEG's (and preferably 4 to maintain a binary interrelationship) must be operated in some form of time shared parallel. For System B the number of paralleled ELSEG's increases to 8 to

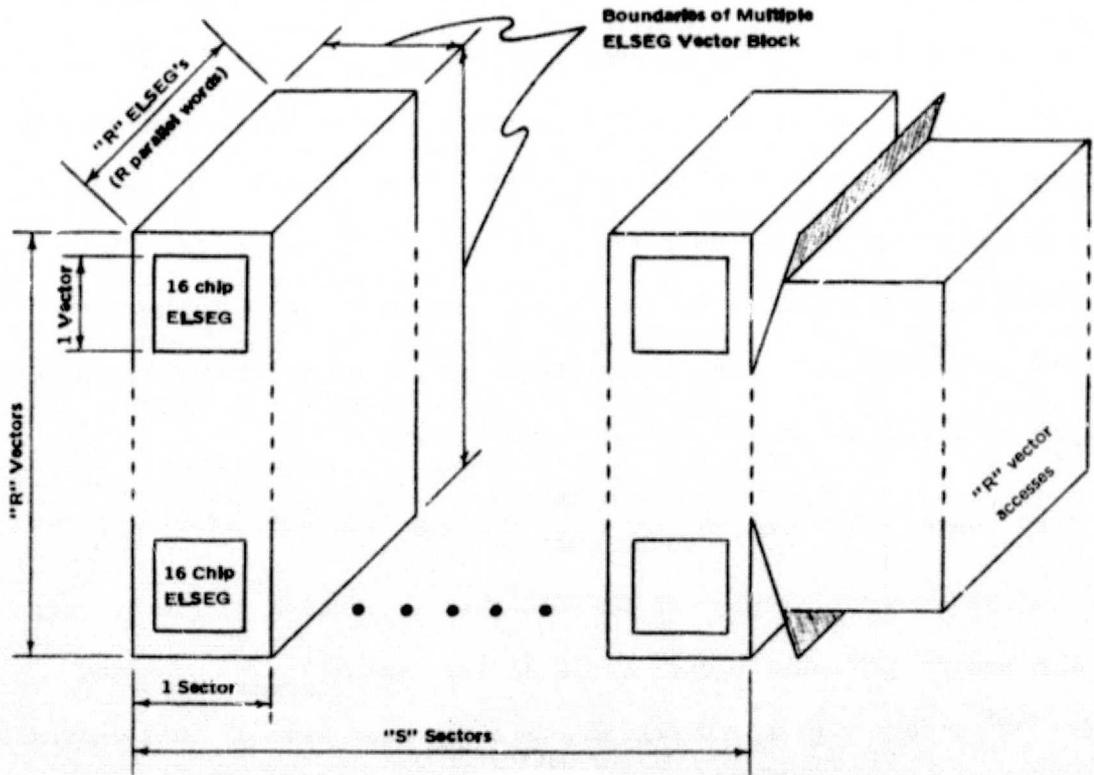
provide a 10 MHz peak event counting capability. If the paralleled ELSEG's are considered to be data address space "vectors" in a "sector" of memory storage, multiple sectors can be assimilated in either of the arrangements shown in Figure 5-5 to secure the total data storage capacity needed.

The alternate organizational hierarchies described by the diagrams in (a) and (b) of this figure both produce system level memory organizations which are random accessed in nature, but the type (a) structure leads to a word organized (WORAM) system while the (b) format results in a block organized (BORAM) system. Functionally, the "word random" configuration is set up on the basis of handling data words individually in the vector space addressed ELSEG's forming a sector by using multiple time phased RMW cycles which are individually enabled by a photon event occurrence detector. Contrastingly, the "block random" configuration is established on the premise that a buffer register/latch circuit will accumulate the data from either 4 (for System A) or 8 (for System B) successive pixel word periods. If a photon event occurs for any one or more of these pixels, all vector space ELSEG's in a sector will be forced simultaneously and collectively through their RMW cycles, even though some or even most may not have any new data added to their stored counts. The disadvantage to this scheme is intuitively obvious: it consumes excess RMW cycling energy at all but the maximum event counting rate.

Power Calculations. Since the ELSEG's in a 4K/N-MOS RAM based LST camera memory are formed from 16 parallel connected chips, each ELSEG will contain 4096 words of 16 bits and can process word update data at an RMW cycle rate of 1.25 MHz. When used to implement systems A or B, the resultant structural characteristics will be:



(a) Word Random Format (WORAM)



(b) Block Oriented Format (BORAM)

Figure 5-5. Random Accessed N-MOS Data Storage Hierarchies

System A: ELSEG Count =  $32,768 \div 4096 = 8$  ELSEG's/memory

Chip Count =  $16 \times 8 = 128$  chips/memory

Organization = 4 Vectors by 2 Sectors

System B: ELSEG Count =  $262,144 \div 4096 = 64$  ELSEG's/memory

Chip Count =  $16 \times 64 = 1024$  chips/memory

Organization = 8 Vectors by 8 Sectors

Since both the WORAM and BORAM forms of these systems would have the same structural characteristics, the first point of concern is to determine which organization is best for the present application. To accomplish this System A will be taken as a test case and an examination made of its power requirements when configured in the alternate word and block random hierarchies.

From the consensus specifications in Table 5-2, it is seen that the active power drain per chip ( $P_{a/c}$ ) in an ELSEG which is updating its stored data continuously at the maximum RMW rate ( $f_{\text{max/chip}}$ ) of 1.25 MHz will be about 400 milliwatts. These same ELSEG's, when simply refreshing their stored counts over a data refresh interval ( $\tau_{\text{dri}}$ ) of 2 millisecond, will draw a refresh power per chip ( $P_{r/c}$ ) of about 3 milliwatts. If a camera memory is configured to have  $R_t$  total vectors in  $S_t$  total sectors with  $B_e$  chips in each of its ( $R_t \times S_t$ ) ELSEG's, the composite on-chip power for the system's storage module can be computed from

$$P_{\text{chip}} = B_e (P_{a/c} A_e \left( \frac{f_{\text{max/chip}}}{f_{\text{count/chip}}} \right) + P_{r/c} (R_t S_t - A_e^{-\beta}))$$

where  $A_e$  is the effective number of ELSEG's that are active on the average during each memory RMW count update cycle at any given  $f_{\text{count/chip}}$  data rate. The " $\beta$ " superscript appearing on the right-hand side of this expression

allows either a pessimistic ( $\beta = \infty$ ) or an optimistic ( $\beta = 1$ ) calculation to be made. At present a pessimistic viewpoint will be taken and the value of  $\beta$  set to infinity so that the  $\lambda_e^{-\beta}$  term becomes zero and drops out of the equation completely.

The other element of power drain associated with the storage module of the camera memory is the  $fCV^2$  power needed to drive the cumulative line capacities of the RAM chips. The chip enable clocking capacitance ( $C_c$ ), being on the order of 30 pF, is the largest single line capacitance. It must be pulsed during each active ELSEG count update cycle and during each of the  $2^n$  different chip address states needed to accomplish a complete refresh cycle (note here that "n" is the number of address line bits supplied to the on-chip decoder to select 1-of- $2^n = 1$ -of-N of the rows shown in Figure 5-4). For a clocking voltage amplitude of  $V_c$ , the total CE line power needed will accordingly be given by

$$P_{ce} = B_e (A_e f_{\text{count/chip}} + R_t S_t (\frac{2^n}{\tau_{dri}})) C_c V_c^2$$

The remaining lines contributing to the storage module capacitive power are the 12 word address lines and 1 each data-in, data-out, and read/write control lines. Each of these lines typically exhibits a capacitance ( $C_a$ ) of approximately 6 pF. Considering the address line power first, it must be recognized that successively higher ordered bits are sequenced at 1/2 the rate of the preceding bit. This means that progressively more significant address bits contribute 1/2 as much power to the cumulative total power as their respective less significant neighbor bits. In closed summation form, the resultant word address line capacitive power is given by

$$P_{wa} = B_e R_t S_t f_{\text{max/chip}} C_a V_a^2 \sum_{k=1}^{12} (\frac{1}{2^k})$$

with  $V_a$  denoting the amplitude of the address line driving signals. Direct evaluation of the summation term here reveals that

$$\sum_{k=1}^{12} \left(\frac{1}{2^k}\right) = 0.9998 \approx 1.0$$

Consequently, the equation for word address capacitance power can be expressed simply as

$$P_{wa} = B_e R_t S_t f_{\max/\text{chip}} C_a V_a^2$$

Unlike the address lines which are driven continuously, the data-in, data-out, and read/write lines are activated only during actual I/O operating sequences. Their combined capacitive power is therefore given as

$$P_{i/o} = 3B_e A_e f_{\text{count}/\text{chip}} C_a V_a^2$$

Upon collecting the individual elements, it is found that the total capacitive power supplied to the storage module of an N-MOS RAM based camera memory can be computed from

$$P_{\text{cap}} = B_e V_c^2 \left( A_e \frac{f_{\text{count}}}{\text{chip}} (C_c + 3C_a) + R_t S_t \left( f_{\frac{\max}{\text{chip}}} C_a + \left(\frac{2^n}{\tau_{\text{dri}}}\right) C_c \right) \right)$$

where it is implicitly assumed that CMOS logic devices are used throughout at all storage module interfaces so that  $V_a = V_c$ .

In the WORAM form of System A, the "effective" number of ELSEG's active per count cycle at the peak data rate of 3.0 MHz will be

$$A_e = (3.0/1.25) = 2.4 \text{ active ELSEG's/memory count cycle}$$

Furthermore, each active ELSEG will be updated at the maximum RMW chip cycling rate (i.e.,  $f_{\text{count}/\text{chip}} = f_{\max/\text{chip}} @ f_{\text{data}/\text{system}} \geq f_{\max/\text{chip}}$ ).

Upon plugging these values into the expression for module power, along with the other applicable device and system parameters, it is found that

$$P_{\text{chip}} = 16(0.4 \times 2.4 \left(\frac{1.25}{1.25}\right) + 0.003 \times 4 \times 2)$$

$$= 15.744 \text{ Watts}$$

$$P_{\text{cap}} = 16(12)^2(2.4 \times 1.25(30 + 3 \times 6) + 4 \times 2(1.25 \times 6 + \left(\frac{2^6}{2000}\right) 30)) \times 10^{-6}$$

$$= 0.488 \text{ Watts}$$

Summing these two values shows that the peak data burst WORAM storage section power is

$$P_{\text{module}} = 15.744 + 0.488 = 16.232 \text{ Watts (WORAM-peak)}$$

To compute the corresponding power level for the BORAM heirarchy, it is necessary that recognition be given to the fact that, due to its functional philosophy, there will always be 4 ELSEG's active per memory count cycle (i.e.,  $A_e = R_t$ ). The system power will therefore be the same for any data I/O counting rate between 1.25 MHz ( $f_{\text{max/chip}}$ ) and 5.0 MHz (the organization establish  $f_{\text{limit/system}}$ ). Allowing for this, it is found that

$$P_{\text{chip}} = 25.084 \text{ Watts}$$

and  $P_{\text{cap}} = 0.709 \text{ Watts}$

so,  $P_{\text{module}} = 26.693 \text{ Watts (BORAM-peak)}$

Comparing the results of these two sets of calculation reveals that an excess overhead power of 10.461 Watts accrues to the BORAM architecture at the peak System A event counting data rate.

Similar sets of calculations can be made for the two alternate memory organizations at any system data rate between 0 Hz and  $f_{\text{limit/system}}$  by taking into account the following bounded variations in the controlling system parameters.

$$\begin{aligned} \text{WORAM: } A_e &= 1 && ; \text{ for } f_{\text{max}}^{\text{chip}} \geq f_{\text{data}}^{\text{system}} > 0 \text{ Hz} \\ A_e &= \frac{f_{\text{data}}^{\text{system}}}{f_{\text{max}}^{\text{chip}}} && ; \text{ for } f_{\text{limit}}^{\text{system}} \geq f_{\text{data}}^{\text{system}} > f_{\text{max}}^{\text{chip}} \\ \text{(both): } f_{\text{count}}^{\text{chip}} &= f_{\text{data}}^{\text{system}} && ; \text{ for } f_{\text{max}}^{\text{chip}} \geq f_{\text{data}}^{\text{system}} > 0 \text{ Hz} \\ f_{\text{count}}^{\text{chip}} &= f_{\text{max}}^{\text{chip}} && ; \text{ for } f_{\text{limit}}^{\text{system}} \geq f_{\text{data}}^{\text{system}} > f_{\text{max}}^{\text{chip}} \\ \text{BORAM: } A_e &= R_t && ; \text{ for all } f_{\text{data}}^{\text{system}} \end{aligned}$$

Note here that in general  $f_{\text{limit}}^{\text{system}} = R_t \times f_{\text{max}}^{\text{chip}}$  if the memory capacity and/or

peak data rate requirements are changed (such as occurs later when considering System B). Upon doing this it is found that at the average data rate of 300 KHz—somewhat arbitrarily taken as 1/10th of the peak rate—the dissipation levels of the alternate System A memory organizations are

$$\begin{aligned} \text{WORAM: } P_{\text{module}} &= 2.109 \text{ Watts} && \text{(average)} \\ \text{BORAM: } P_{\text{module}} &= 6.817 \text{ Watts} \end{aligned}$$

Similar calculations at a 0 Hz data rate—such as occurs in the STANDBY mode—reveal that, when the memory is merely refreshing its stored data and not conducting any data I/O operations, the storage module power levels for the two organizations are the same. Specifically,

$$P_{\text{module}} = 0.540 \text{ Watts} \text{ ---- } (\text{WORAM or BORAM-static})$$

These sample calculations at selected data rates indicate that the WORAM hierarchy is definitely superior to the BORAM structure on the basis of power dissipation.

Figure 5-6 presents continuous plots of the variations in the System A storage module dissipation using equivalent BORAM and WORAM architectures. Also included on this figure are the support electronics

power levels that engineering "guesstimates" indicate will accompany each organization and must be added in to derive the total memory system power. These plots collectively demonstrate that the "word" organization requires less power for its operation at all data rates except the extreme limiting cases of 0.0 Hz and 5.0 MHz. The "block" organization is therefore eliminated from any further serious consideration in 4K/N-MOS RAM based LST camera memory systems.

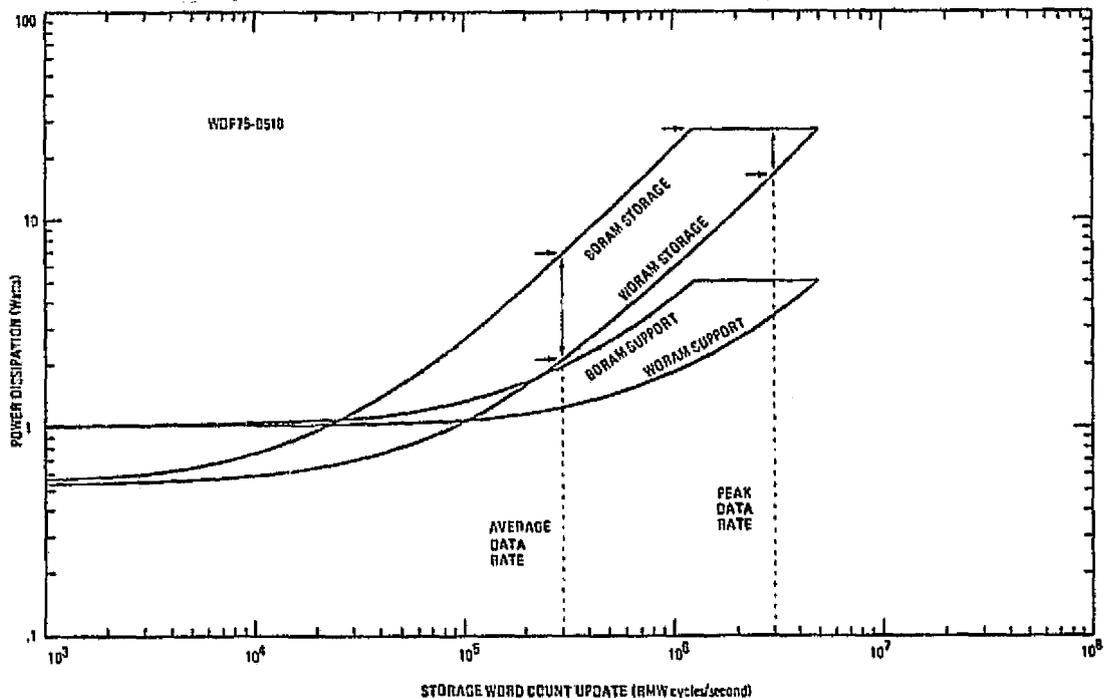


Figure 5-6. Alternate N-MOS System A Power Requirements

A few final points of concern remain, however. Namely, what range of power dissipation can be expected from viable implementations of System A using the N-MOS technology; what is the probability of securing a viable implementation of System B by scaling up the capacity of a System A design; and what is the range of power drains that will occur for up-scaled System B capacity memories? Using the established equations for N-MOS RAM system power, each of these questions can be answered graphically by preparing a series of plots. The first, shown in Figure 5-7, illustrates the

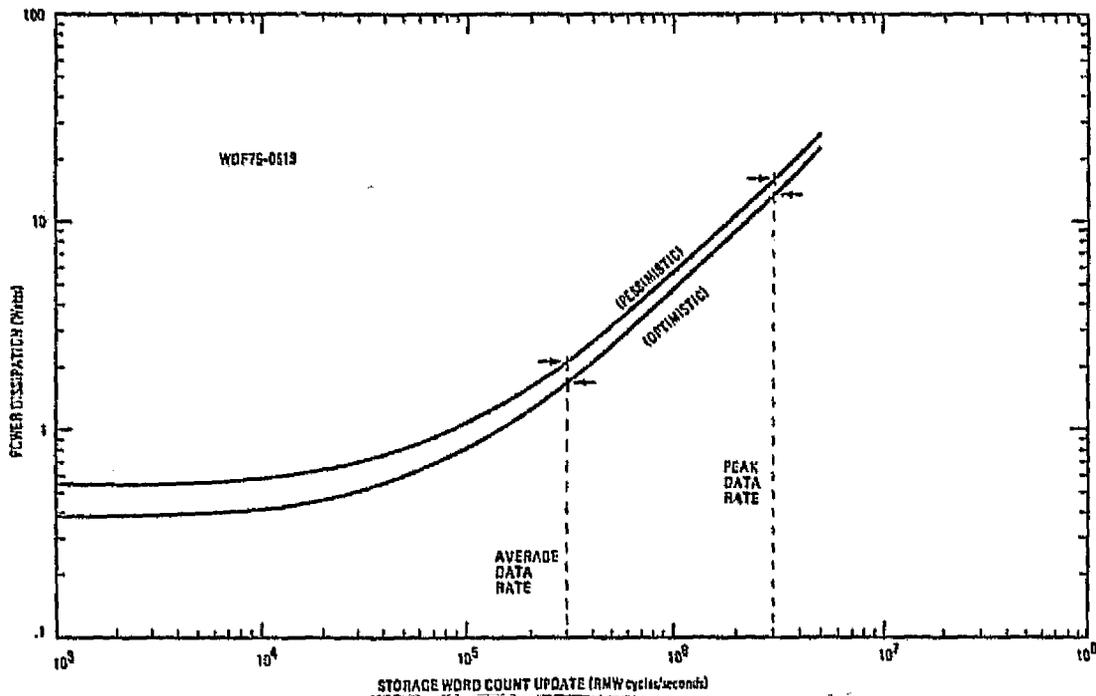


Figure 5-7. N-MOS System A Storage Power Boundaries

range of power requirements obtained for a WORAM form of System A by taking alternately a pessimistic and an optimistic viewpoint on the device characteristics of Table 5-2. With either it is seen that the resultant power levels are well within the targeted System A limits of 10 Watts average at  $\leq 300$  KHz and 30 Watts peak at 3 MHz. A high margin of overhead therefore remains for support circuitry to secure a viable system meeting the stipulated functional requirements.

To make an equivalent plot for a System B version of the LST camera memory and thereby check the potential viability of 4K/N-MOS RAM's for higher capacity systems, it is only necessary to substitute the appropriately modified structural parameters into the respective power relationships. The specific parameters that must be changed and their new values are:

$$R_t = 8 \text{ vectors/memory}$$

$$S_t = 8 \text{ sectors/memory}$$

$$\frac{f_{\text{limit}}}{\text{system}} = 10.0 \text{ MHz}$$

The results of introducing these changes into the system composition, taking first a pessimistic and then an optimistic approach to the 4K RAM characteristics, are summarized in the plots of Figure 5-8.

As indicated here, the power requirements for the storage module at data rates below  $10^5$  words/second are well within the targeted System B limits. But, at the nominal  $10^6$  words/second average and  $10^7$  words/second peak data rates they are marginal at best and leave virtually no overhead for support circuitry. With a relaxation of the System B power budget, the N-MOS technology could conceivably be employed. But, the poor operating margins available and the probability of significantly reduced reliability tend to counterindicate 4K/N-MOS RAM's as a viable alternative for use in the LST camera memory System B.

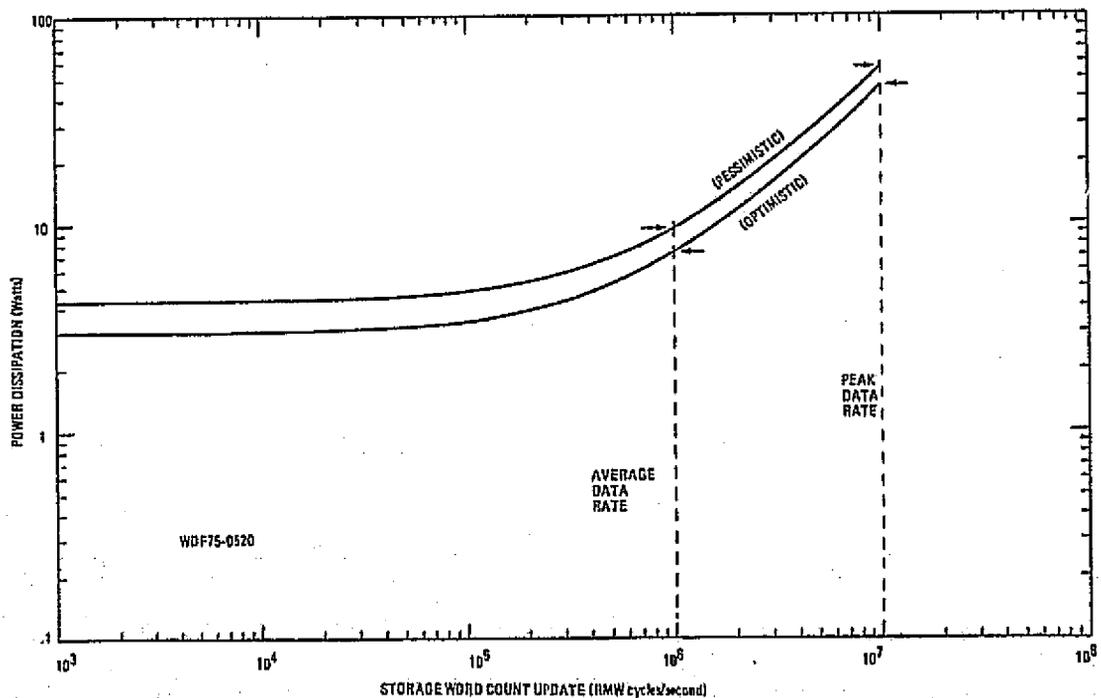


Figure 5-8. N-MOS System B Storage Power Boundaries

### 5.2.2 CCD

At the time of this report there have been only three CCD memory chips announced in sample quantities on the commercial market. These are an 8 Kbit device from Bell Northern Research (BNR) of Canada, a 9 Kbit device from Fairchild, and a 16 Kbit device from Intel. Two of the three — the Intel and BNR chips — appear to be directed almost exclusively toward drum and disk replacement applications. They employ a chip organization like that shown in Figure 5-9. This chip configuration employs a decoder to select one-out-of-N shift register "tracks" to be coupled to separate unilateral input and output lines. All other tracks are shifted in parallel with the selected track, but their data are simply recycled. A deselect provision is included whereby all tracks are recycled and the I/O terminals are disabled. Each track is a SISO (serial-in and serial-out) CCD shift register which is M bits long with refresh stages spaced along its length at every "J'th" bit position. To allow for device operation at up to +70°C, a refresh operation must typically be conducted within each 2 millisecond interval. Refresh staging in the BNR device is every 32 bits while in the Intel (and Fairchild) device it is every 128 bits. According to the general relationship

$$2^{(T_0 - T)/\delta} \times \tau_{\text{refresh}} \times f_{\text{clock}} \geq J_{\text{staging}}; \text{ where } \delta \approx 10^\circ\text{C} \\ (\text{@ } T_0)$$

it follows that the BNR chip can be shifted at a minimum rate of  $f_{\text{clock}} = 16$  KHz, which is four times better than the minimum rate of  $f_{\text{clock}} = 64$  KHz for the Intel (and Fairchild) chip.

An alternate functional concept is employed on the Fairchild chip. As seen in Figure 5-10, this chip provides for simultaneous I/O operations

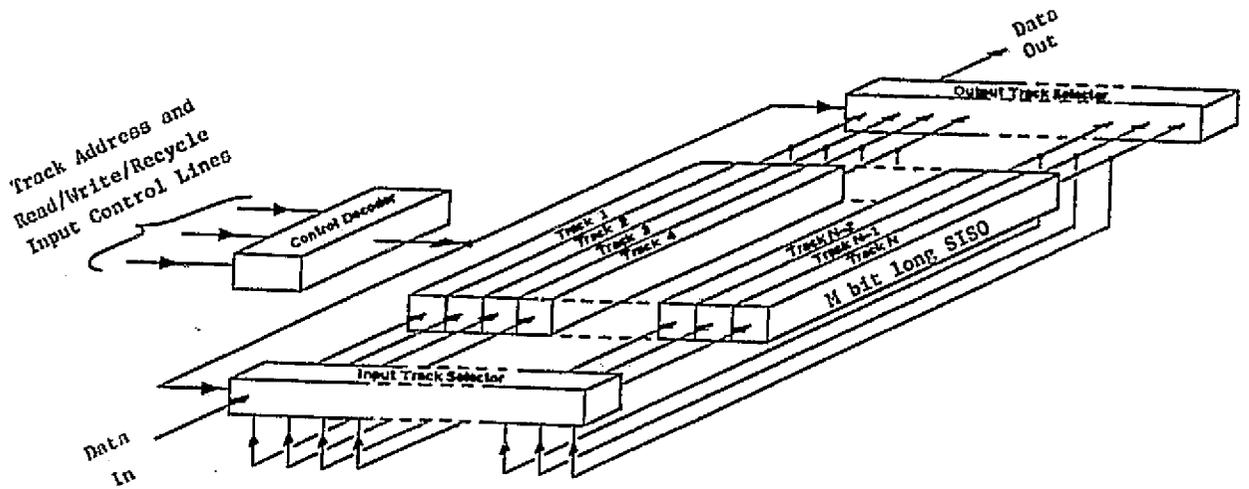


Figure 5-9. Track Accessed CCD Data Storage Hierarchies

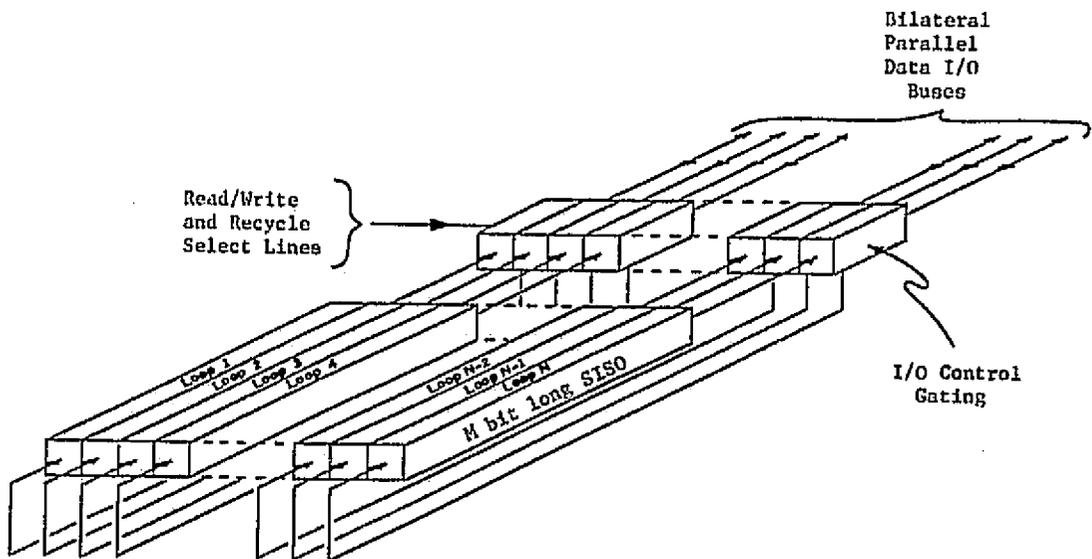


Figure 5-10. Parallel Loop CCD Memory Chip Functional Diagram

from N parallel, identically clocked register loops. To hold down the pin count and make it more generally applicable in a wide variety of bus oriented memory configurations, data input or output exchange operations with the individual loops on this device take place over bilateral, tri-state bus lines. Control signals into the I/O gating section determine whether the register data will be read-out, written-in, or simply recycled. This device contains 9 separate loops of 1024 bits each. On the alternate track accessed chips each track is 256 bits long, with the Intel device containing 64 tracks and the BNR unit possessing 32 tracks.

Table 5-3 presents a cross-sectional compendium of the operating specifications for the three announced CCD memory chips. The top portion of this table is a condensation of manufacturer supplied data sheets and quoted operating specifications. The bottom portion presents a set of consensus specifications for these device organizations, assuming identical processing for each and the normalization of all characteristics to an operating ambient of 0°C to +70°C. These commonalized specifications will be used to examine the power budgets and overall viability of alternate storage section configurations which might be proposed to meet the data rate and capacity requirements of memory Systems A and B using CCD memory chips functionally structured like the representative devices.

Memory Module Configurations. As has been pointed out, there are currently two devices available with established characteristics that have track selectable organizations. While these chips both have 256 bits per track and other quite similar specifications, each must be examined separately to determine the net effect of their difference in capacity. With this type of chip organization each individual chip can contribute only one bit to successive bit-parallel pixel words. Based on this it is possible to

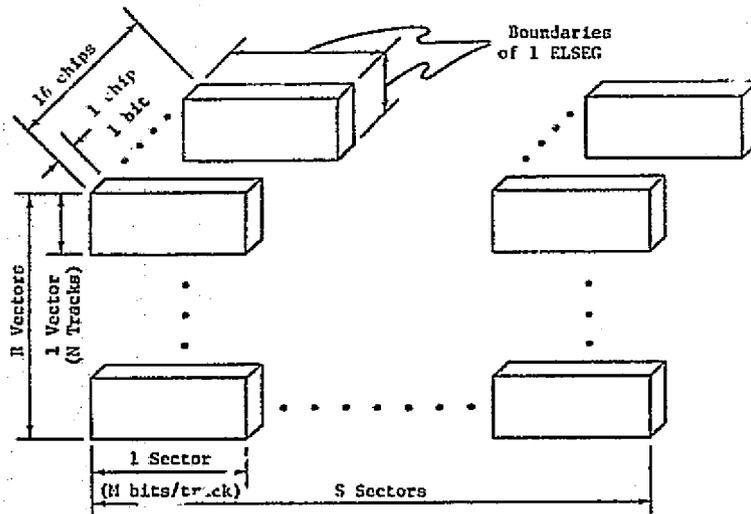
Table 5-3. COMPENDIUM OF ANNOUNCED CCD MEMORY CHIP SPECIFICATIONS

Characteristic	Fairchild CCD 450	BNR CC8M01	Intel CC2416	
Capacity	9216 bits	8192 bits	16384 bits	Device Descriptions
Organization	9 loops x 1024 bits/loop	32 tracks x 256 bits/track	64 tracks x 256 bits/track	
Type Access	9 parallel loops	1-of-32 track selection	1-of-64 track selection	
I/O Form	9 bilateral buses	single input & output lines	single input & output lines	
Refresh Staging	128 bits/refresh	32 bits/refresh	128 bits/refresh	
Supply Voltages	+12 <sup>v</sup> , +5 <sup>v</sup> , Gnd, & -3 <sup>v</sup>	+10 <sup>v</sup> , Gnd, & -3 <sup>v</sup>	+12 <sup>v</sup> , +5 <sup>v</sup> , Gnd, & -3 <sup>v</sup>	Data Sheet and/or Manufacturer Quoted Specifications (as of 2/10/75)
Clock Amplitude	12 Volts	10 Volts	12 Volts	
Clock Phasing	2Ø	3Ø	4Ø	
Max Clock Rate	> 1 MHz (guaranteed)	> 1 MHz (guaranteed)	> 1 MHz (guaranteed)	
Min Clock Rate	< 50 KHz (typical)	< 20 KHz (typical)	< 100 KHz (typical)	
Refresh Rate Chip Power	~ 50 mW/chip	~ 50 mW/chip	~ 100 mW/chip	
Max Rate Chip Power	~ 250 mW/chip	~ 250 mW/chip	~ 500 mW/chip	
Active I/O Line Capacitances	8 pF/line	5 pF/line	6 pF/line	
Clock Line Capacitances	400 pF/Ø	* 500 pF/Ø	400 pF/Ø	
Ambient Temperature	0°C to +55°C	0°C to +70°C	0°C to +70°C	
Min Refresh Rate	64 KHz	16 KHz	64 KHz	Consensus Design Specifications
Max BM <sup>2</sup> Data Rate		1.25 MHz		
Effective Clock Capacitance		0.05pF/bit/Ø		
Chip Dissipation @ < 300 KHz		6.1 mW/bit		
Chip Dissipation @ 1.25 MHz		30.5 mW/bit		
Clock Amplitude		12 Volts		
Clock Phasing		2Ø		
Operating Ambient		0°C to +70°C		

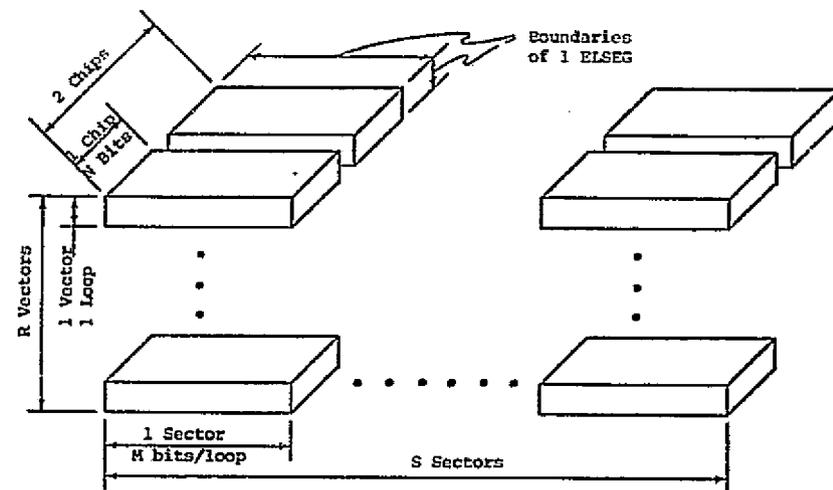
\* BNR chip is early lab model device having oversized cells approximately double the size of the alternate chips shown. The consensus specification for clock capacitance reflects a commonization of all chip cell sizes to the more recent designs.

envison a memory storage section which is configured as shown in either (a) or (b) of Figure 5-11. In both arrangements a 16 chip assembly is required to form an "elementary segment" (ELSEG) of storage having  $N \times 256$  words with 16 parallel accessed bits per word (as necessitated by the LST camera memory requirements). In the type (a) structure a stack of "R" ELSEG address vectors is introduced to facilitate multiplexing up from the practical chip RMW (read-modify-write) rate to the required system level data (word) rate. For System A there would be 4 vector spaces while for System B there would be 8. Multiples of these R-vectorized stacks are laid side by side in "S" sectors to fill out the composite memory system capacity. The central theme of this approach is to provide a storage section hierarchy in which the minimum number of chips are running at their maximum shift rate to achieve the necessary system I/O data rate while the maximum number of chips idle at the lowest possible frame synchronous recycle rate. In the type (b) structure the fundamental philosophy is simply to run all ELSEG's in parallel at the lowest possible rate consistent with multiplexing up to the desired system I/O word rate. This approach results in the storage section hierarchy being formed as a single sector that has a large number of vector addressed storage spaces.

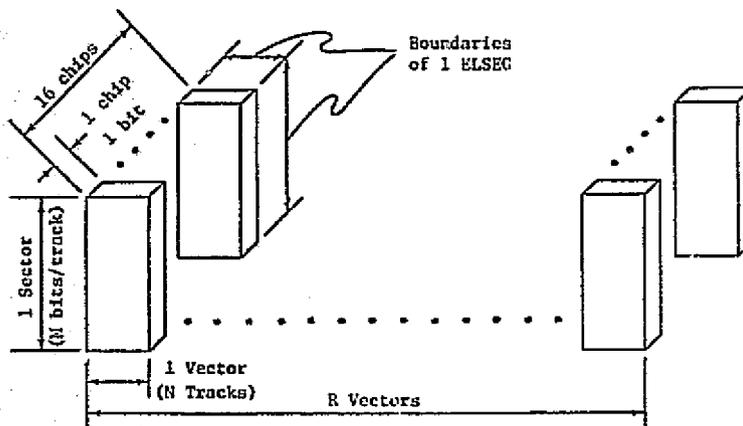
The surrogate form of CCD memory chip that is available with established characteristics has a parallel loop organization in which each chip can contribute up to 9 bits to successive bit-parallel pixel words. Based on this the MM (Min high and Max low clock rate) and CC (multi-plexed Common Clock rate) memory storage section configurations, equivalent to those discussed for the track accessed chips, will appear as shown in (a) and (b), respectively, of Figure 5-12. In this instance



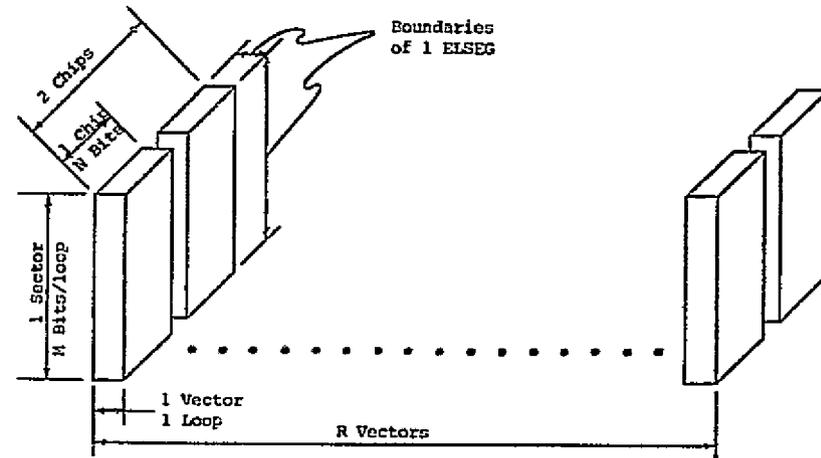
(a) High and Max Low Clock Rate Format



(a) Min High and Max Low Clock Rate Format



(b) Multiplexed Common Clock Rate Format



(b) Multiplexed Common Clock Rate Format

Figure 5-11. Track Accessed CCD Data Storage Hierarchies

Figure 5-12. Parallel Loop CCD Data Storage Hierarchies

only 2 chips are needed to form each ELSEG (as opposed to 16 with the track accessed chips). Additionally, the respective ELSEG's will supply 18 (rather than just 16) parallel accessed bits per word, although each ELSEG stores fewer total words (1024 compared to 8192 or 16384).

With the MM structure, System A requires that 4 vector spaces be used to achieve the specified data rate and that 8 sectors be included to fill out the total storage capacity, while System B requires 8 vectors and 32 sectors. With the CC structure, System A will employ 32 vectors while System B has 256 vectors, with both having the equivalent of a single sector. Each of these storage module architectures, as well as those for the track accessed chips, produce a memory fitting into the BOSAM category discussed earlier. The CC structure yields a small number ("1" with parallel loop chips and "N" with track accessed chips) of large data blocks while the MM format breaks the data up into a larger number ("S" with parallel loop chips and "S x N" with track accessed chips) of small blocks. The "block buffer" function called out in Figure 5-3 will, in this instance, be provided via the multiplexed reinsertion of modified data back into its original source register chain directly at the storage module interface.

Power Calculations. To determine whether any of the available CCD memory chips hold promise of meeting the LST camera memory guideline requirements, the specifications for each are introduced into their respective track accessed or parallel loop forms of CC and MM memory storage module hierarchies and the resulting system parameters computed. Since all of these calculations proceed in a similar manner, for the sake of brevity, only one example is considered in detail and a summarization given of the

results of the other cases. As the case in point, an evaluation is made of the use of a consensus spec version of the BNR type of 8192 bit, track accessed CCD memory chip in a CC organization of System A.

To facilitate this analysis it is first recalled that each chip contributes only one bit to successive pixel words. Consequently, the number of chips in each ELSEG must be

$$\text{ELSEG Chip Count} = 16 \text{ chips/ELSEG}$$

With 32 selectable tracks of 256 bits each, the number of words stored in each ELSEG will be

$$\text{ELSEG Word Capacity} = 8192 \text{ words/ELSEG}$$

To supply the required system capacity of 32,768 words, the number of ELSEG's needed is

$$\text{Memory ELSEG Count} = 4 \text{ ELSEG's/memory}$$

The CC architecture calls for all memory ELSEG's to be paralleled, so the memory's organizational matrix will consist of 4 address vectors and 1 sector.

Before proceeding a check must be made to ensure that the system level data rate requirement can be met. Allowing for the multiplexing of 4 ELSEG vectors with each ELSEG able to handle event count accumulation rates of up to 1.25 MHz, it is seen that the maximum data rate for the present memory design would be

$$\text{Max Memory Data Rate} = 4 \times 1.25 = 5.0 \text{ MHz}$$

and, since this exceeds the 3.0 MHz system requirement, the design is confirmed as being feasible (if the chip capacities had been 16 Kbits rather than 8 Kbits, on the other hand, there would have been only 2 quadrants and the memory could have operated at only 2.5 MHz — so the design would have been infeasible). The remainder of the analysis will check its power requirement viability.

The actual I/O data rate per ELSEG for a 3.0 MHz system level data rate will be

$$\text{ELSEG Data Rate} = (3.0/4) \times 10^6 = 750 \text{ KHz}$$

With each of the 16 chips in the ELSEG having an effective total clock line capacitance of

$$\text{Chip Clock Capacitance} = 0.05 \times 10^{-12} \times 8192 \times 2 = 820 \text{ pF/chip}$$

the clocking capacitance of each ELSEG will be

$$\text{ELSEG Clock Capacitance} = 16 \times 0.82 \times 10^{-9} = 13.1 \text{ nF/ELSEG}$$

By extrapolation from the device specifications in Table 5-3, the on-chip dissipation at a clocking rate of 750 KHz is found to be

$$\text{Chip Dissipation} = (6.1 \times 10^{-6} \times 8192) \left(1 + \left(\frac{30.5}{6.1} - 1\right) \left(\frac{750-300}{1250-300}\right)\right)$$

$$\text{Chip Dissipation} = 145 \text{ mW/chip @ 750 KHz}$$

Since there are  $(16 \times 4) = 64$  chips total in the memory, the total chip power in the memory module will be

$$P_{\text{chip}} = 64 \times 0.145 = 9.28 \text{ Watts}$$

and the total line capacitance drive power with a 12 volt amplitude clock swing will be

$$P_{\text{cap}} = 13.1 \times 10^{-9} \times 4 \times (12)^2 \times 800 \times 10^3 = 6.04 \text{ Watts}$$

Summing these two values shows that the total memory module power, exclusive of support electronics and line driver inefficiency considerations, will be

$$P_{\text{module}} = 15.32 \text{ Watts}$$

Recognizing that this power level constitutes a steady dissipation that does not fluctuate appreciably with the actual event counting rate — it is

set instead directly by the pixel scan rate — comparison to the system power budget guideline of 10 Watts average reveals that the use of 8 Kbit track accessed CCD memory chips does not prevent a viable means of implementing the System A version of the LST camera memory.

A complete summary tabulation of the foregoing analysis is presented in Table 5-4 along with the results of equivalent computations for the other feasible (i.e., potentially viable) combinations of CCD memory chips and storage module organizations. Combinations found to be system-ologically impractical include the MM form of System A using the 8 Kbit chip and both forms of System A using the 16 Kbit chip. The 8 Kbit chip MM organization is impractical because it results in a single sector memory identical to that of the CC organization. Neither of the 16 Kbit chip organizations are practical because the track accessed nature of the 16 Kbit chip makes its size incompatible with simultaneously providing the System A specifications of 32,768 words and 3.0 MHz word rate. To reach the necessary data rate, a camera memory using these chips would have to have a capacity of at least 49,152 words (3 x 16,384).

As indicated in the viability decision row along the bottom of Table 5-4, the only design combinations which might lead to an acceptable CCD based LST camera memory are the two forms of System A obtained with the parallel loop 9 Kbit chips. When a support electronics power level of at least 5 Watts is added in, even these become borderline and might require slight relaxation of the 10 Watt average power specification. When considered in light of poorly established reliability characteristics and lack of any projected cost advantage, this marginal power requirement indicates that no form of CCD memory constitutes a truly viable candidate for the LST camera memory application.

Table 5-4. ALTERNATE CCD CAMERA MEMORY CHARACTERISTICS

	LST Camera Memory System A (Simplex)			LST Camera Memory System B (Simplex)					
	9K Bit PL/CCD MM Org	8K Bit TA/CCD CC Org	9K Bit PL/CCD CC Org	8K Bit TA/CCD MM Org	9K Bit PL/CCD MM Org	16K Bit TA/CCD MM Org	8K Bit TA/CCD CC Org	9K Bit PL/CCD CC Org	16K Bit TA/CCD CC Org
System Data Rate ( $\times 10^6$ words/second)	3.0			10.0					
System Frame Rate (frames/second)	91.55			38.15					
Memory Word Capacity (words/memory)	32,768			262,144					
Memory Bit Capacity (bits/memory)	589,824	524,288	589,824	4,194,304	4,718,592	4,194,304	4,194,304	4,718,592	4,194,304
ELSEG Word Capacity (words/ELSEG)	1,024	8,192	1,024	8,192	1,024	16,384	8,192	1,024	16,384
Memory Word Size (bits/word)	18	16	18	16	18	16	16	18	16
Memory ELSEG Count (ELSEG's/memory)	32	4	32	32	256	16	32	256	16
ELSEG Chip Count (chips/ELSEG)	2	16	2	16	2	16	16	2	16
ELSEG Clock Capacitance (pF/ELSEG)	1.84	13.1	1.84	13.1	1.84	26.2	13.1	1.84	26.2
Organization (vectors x sectors)	4 x 8	4 x 1	32 x 1	8 x 4	8 x 32	8 x 2	32 x 1	256 x 1	16 x 1
Active ELSEG Count (ELSEG's/frame)	4	4	32	8	8	8	32	256	16
Active ELSEG Data Rate ( $\times 10^3$ words/second)	750	750	93.75	1,250	1,250	1,250	312.5	78.125	625
Refresh Chip Clock Rate ( $\times 10^3$ bits/second)	107.143	N.A.		26.042	80.645	78.125	N.A.		
Refresh Rate Chip Power (mW/chip)	56	N.A.		50	56	100	N.A.		
Active Rate Chip Power (mW/chip)	163	145	56	250	281	500	53	56	237
Memory Chip Power (Watts/memory)	4.44	9.28	3.58	51.2	32.3	76.8	27.1	28.7	60.7
Line Capacitance Power (Watts/memory)	1.59	6.04	0.80	20.0	8.0	40.1	18.9	5.3	37.7
Memory Module Total Power (Watts/memory)	6.03	15.32	4.38	71.2	40.3	116.9	46.0	34.0	98.4
System Peak Power Budget (Watts/system)	30			50					
System Average Power Budget (Watts/system)	10			10					
Design Viability Decision (Yes, No, or Uncertain)	Uncertain	No	Uncertain	No	No	No	No	No	No

### 5.2.3 MNOS

The MNOS technology, which produces nonvolatile storage cells into which data may be written and retained for many thousands of hours without receiving any form of additional static or dynamic refresh or state maintenance energy, is not presently available on the commercial market in a form which is directly applicable to the LST camera memory. Current commercial chips, such as those from Nitron (McDonnell-Douglas) for example, are directed exclusively toward EAROM (electrically alterable read only memory) or RMM (read mostly memory) applications where their inherently slow—compared to other LSI technologies—writing and clearing time characteristics are of no real concern.

To make the MNOS technology acceptable for use in either of the camera memories being considered, it is mandatory that the read/write and clear time requirements of typically  $> 10$  microseconds/operation/chip be masked at the chip level so they are essentially transparent when viewed from any higher level in the system hierarchy. The Westinghouse "BORAM" approach, being developed under the auspices of the U.S. Army, appears to constitute the most successful technique for producing high speed MNOS memory devices. It is based on a functional chip organization similar to that shown in Figure 5-13. As seen here, a hybrid operational philosophy—wherein both random and sequential accessing features are incorporated—has been adopted to prevent the slow cell interface sequences from dictating the aggregate speed of the entire chip, and hence the composite memory.

Fully developed, functionally confirmed, and contractually delivered MNOS memory devices fitting the high speed classification are currently being designed into military grade equipment as both buffer and main stores

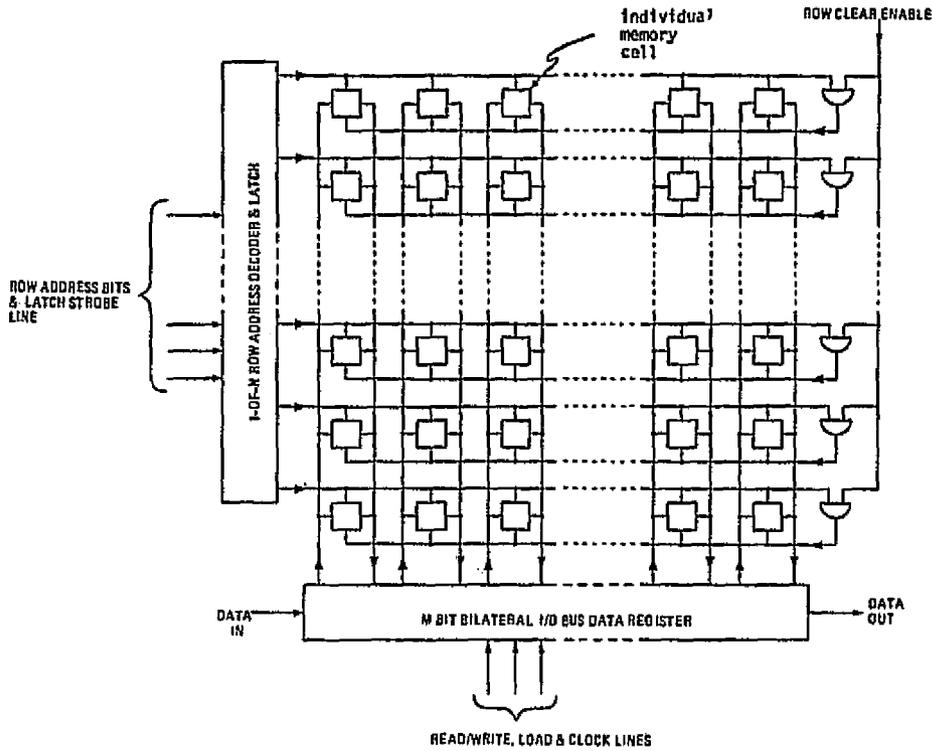


Figure 5-13. Random Serial-Bit-Block Accessed MNOS Memory Chip Functional Diagram

Table 5-5. PROJECTED 8 KBIT MNOS MEMORY CHIP SPECIFICATIONS

Characteristic	Device Specification
Capacity	8192 bits
Organization	64 rows x 128 bits/row
Type Access	128 bit data block
I/O Interface	128 bit BIOD register
Supply Voltages*	+15 <sup>v</sup> , Gnd, -5 <sup>v</sup> , & -15 <sup>v</sup>
Clock Amplitude	15 volts
Clock Phasing	20
Clock Frequency	1/2 of data rate
Max I/O Data Rate	> 5 Mba
Min I/O Data Rate	0 Hz
Clock Line Capacitance	1pF/SR bit/D
Transfer Line Capacitance	30 pF
Address Latch Capacitance	20 pF
Chip Select Capacitance	40 pF
All other Line Capacitances	4 pF
Standby On-Chip Power	30 <sup>uW</sup> /chip
Standy On-Chip Power	2 <sup>uW</sup> /chip
Max Active On-Chip Power	30 <sup>uW</sup> /chip
Operating Ambient Temperature	0°C to +70°C

\*Supply levels shown are for interface with CMOS logic family.  
Equivalent TTL interface supply levels are +5<sup>v</sup>, Gnd, -15<sup>v</sup>, & -25<sup>v</sup>

having capacities of up to  $10^8$  bits. While the size of present chips is limited to 2048 bits, final process refinement and mask layout confirmation work is being concluded on a 4096 bit chip, and development schedule plans have been laid for the production of 8192 bit and a 16,384 bit chips by 1978. The MNOS memory designs considered in this report will be conservatively based on the characteristics shown in Table 5-5 for the projected 8 Kbit chip. This particular device is structured to have  $N = 64$  rows by  $M = 128$  columns of nonvolatile storage cells and employs a dual dynamic ratioless form of bilateral-I/O-bus (BIOB) register conservatively rated at a two phase multiplexed, 5 MHz data shifting rate.

The sequence of operations for Westinghouse type block organized MNOS memory chips is broken into three principal parts: read, shift/modify, and write. During the "read" interval a row address is latched and decoded, an enabling signal is applied to the selected row, and the data contents of the M cells in the row are parallel loaded into the output serializing I/O bus register. During the "shift/modify" time the read accessed block of M data bits is shifted sequentially out one end of the BIOB register to the external adder circuit which modifies it and inserts it back into the other end of the register, with successive bits processed within one data period (which, at 5 MHz, is 200 nanoseconds).

Concurrent with the external shifting operation, a clearing pulse is applied to the addressed row to reset its cells preparatory to their being written to new data states at the end of the shift/modify sequence. Finally, during the "write" period the modified data in the I/O bus register is dumped in parallel back into the previously enabled and cleared row of storage cells. Upon completing this writing operation, the row address is changed and the three part functional sequence is repeated with a new data block row.

## Memory Module Configuration

All currently projected "BORAM" style high-speed MNOS memory chips that are applicable to the LST camera memory will be structured as shown in Figure 5-13. In each, M bit blocks of data are processed in bit-serial fashion through a single set of input and output port terminals. As a result, individual chips can contribute only one bit to each of the multiple parallel bit words used in the memory system. This means that a set of 16 chips must be employed to form an ELSEG of storage in the camera memory. Each ELSEG thus established will process sequential blocks of M words having 16 parallel bits per word when its output is enabled for a read-out or write-in operation.

Due to the unique operating sequence of the MNOS chips — which requires that a two part non-I/O-interactive time interval be included with the externally functional shift/modify interval to form a complete data processing cycle — a pair of ELSEG's must be operated in a phased-tandem or flip-flop arrangement to allow a continuous, uninterrupted sequence of event count updates to be maintained. With each such pair able to process data at up to a 5 MHz rate, two pairs can be activated simultaneously and their outputs multiplexed to achieve the required 10 MHz data rate of System B (no direct consideration is given here to System A because of the incompatibility of its procurement time frame with the availability of production quantities of MNOS memory chips).

A well ordered memory module hierarchy is formed for the system by considering each duo of ELSEG pairs to be two storage address vectors for successive memory sectors in the manner depicted in Figure 5-14. With each flip-flop ELSEG vector space storing  $(2 \times 8192) = 16,384$  data words,

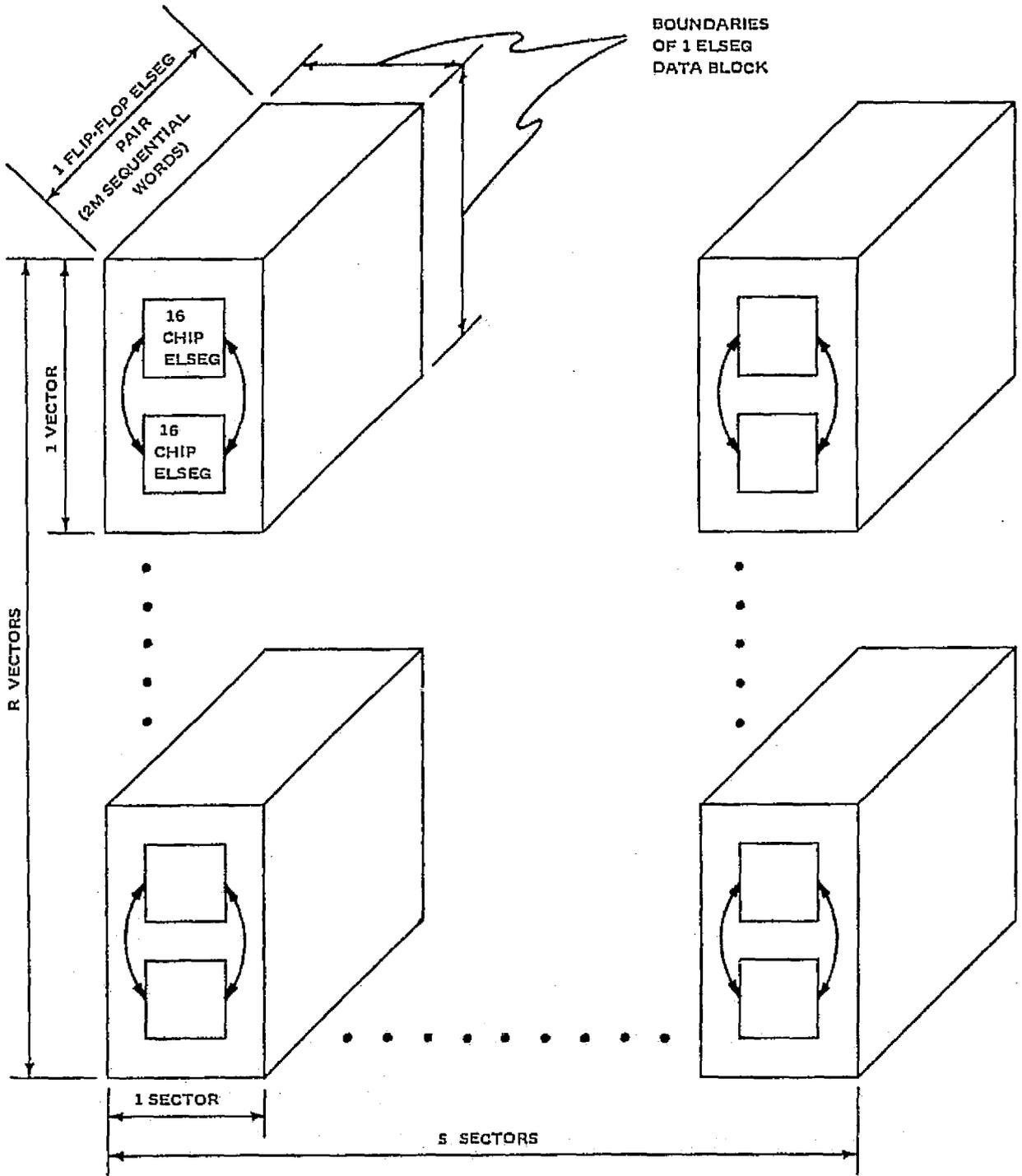


Figure 5-14. Block Accessed MNOS Data Storage Hierarchy

successive sectors will contain  $(2 \times 16,384) = 32,768$  data words. Hence,  $(262,144 \div 32,768) = 8$  separate sectors will be needed to provide the full System B pixel word capacity.

Unlike memories incorporating dynamic forms of memory devices, however, only one sector in an MNOS camera memory need be powered up at any given time. The other seven sectors are totally powered down with every form of electrical stress — whether it be from supply voltages or interface driving signals — completely removed. In this state the failure rates of the individual memory chips are, according to establish military standard HDBK-217B guidelines, typically lowered by at least a full order of magnitude. Consequently, a significantly improved reliability figure is realized for the composite memory. This factor, as noted earlier in Section 4, has been and remains one of the prime motivations behind the development of LSI nonvolatile MNOS storage devices for use in high capacity applications such as required by LST-2.

As a result of their serialized I/O nature, the use of high speed MNOS chips in a camera memory system produces a storage module hierarchy that fits into the "BOSAM" classification. In the generalized case described by Figure 5-14, the stored data is handled in a format consisting of "S x N" blocks (where it will be recalled that "N" is the number of storage cell rows per chip) with each block containing "2 x R x M" words. The "block buffer" function called out in Figure 5-3 is supplied here by the on-chip BIOB registers which temporarily hold half of a data block internal to the memory chips prior to its being written-in or read-out while another half of a data block is being externally shift/modify processed.

Power Calculations. Under the organizational constraints imposed, an 8K/MNOS based LST camera memory will be composed of 16 flip-flop pairs of ELSEG's, with each ELSEG containing 16 memory chips. Any given pair can store a total of 16,384 words of 16 bits and maintain a continuous data updating RMW cycling rate of 5.0 MHz. To attain the 10 MHz data rate requirement of System B, two ELSEG pairs must function in parallel with their I/O operations being multiplexed. Only a single set of 4 ELSEG's will be active at any given time, and only half of these will contribute  $FCV^2$  shift register power to the composite system dissipation. The remaining 24 ELSEG's which fill out the aggregate storage capacity of the system will be powered down, and hence require no power.

Using the device specifications listed in Table 5-5, it is found that the shifting power per MNOS chip actively executing I/O operations will be

$$\begin{aligned} \text{Chip SR Dissipation} &= \left(\frac{5 \times 10^6}{2}\right) \times 2 \times 128 \times 10^{-12} \times (15)^2 \\ &= 144 \text{ mW/active chip} \end{aligned}$$

With 16 chips in two ELSEG's contributing clocking power, the total shifting power in the memory module (ignoring inefficiencies in the driver electronics) is found to be

$$P_{\text{SR}} = 16 \times 2 \times 144 \times 10^{-3} = 4.608 \text{ Watts}$$

All 64 chips which are powered up contribute to the on-chip dissipation of the system. At a 5 MHz cycling rate each active chip draws a time average power of 50 milliwatts. The total on-chip power for the memory module is therefore

$$P_{\text{chip}} = 16 \times 2 \times 2 \times 50 \times 10^{-3} = 3.2 \text{ Watts}$$

Upon summing these two values, it is found that the total dissipation of the data storage module in an MNOS System B camera memory is

$$P_{\text{module}} = 7.808 \text{ Watts}$$

exclusive of overhead support, control, and power switching requirements.

A source of power consumption ignored in the foregoing calculations is that related to the capacitances of the address, selection, and control lines connected to the memory chips. Justification for this is that the highest frequency pulses applied to any of these lines is 1/128th that of the per ELSEG data rate (i.e.,  $5 \text{ MHz} \div 128$ ). Consequently, the sum total contribution from this source — allowing for 64 active memory chips in the storage module — is less than 32 milliwatts. Its effect on system dissipation is thus negligible.

Consideration of the peripheral circuitry is necessary to ascertain a final projection on the MNOS camera memory power. If allowance is made for 50% efficient clock drivers, a dissipation of

$$P_{\text{drivers}} \cong P_{\text{SR}} = 4.608 \text{ Watts}$$

will occur in those circuits. The remaining power consumption in the system is used by the supporting adder, interface, and control logic sections. An engineering estimate of the combined needs of these networks yields a value of around 6.4 Watts as an upper limit. Including all elements of power drain, it is accordingly found that a pessimistic estimate yields

$$P_{\text{system}} = 17.8 \text{ Watts}$$

as the power requirement for an 8K/MNOS implementation of System B.

Comparison of the computed power requirements with the allotted budget for the LST-2 camera memory reveals that it exceeds the 10 Watt average

specification; but due to the MNOS memory drain being independent of data rate variance, it is well within the peak burst limit of 50 Watts. This indicates that a slight relaxation is necessary in the average power specification to achieve strict compatibility, but doing so appears warranted in light of the significant gains made in system reliability through the nonvolatility of the MNOS technology. Upon weighing each of these trade-offs it is concluded that, with careful attention to design detail and selection of an optimal mix of low power support logic circuits, the use of 8K/MNOS BORAM chips does provide a viable approach to the implementation of LST camera memory System B.

### 5.3 Application Constraints

In reviewing the suitability of alternate types of memories in a particular application situation, care must be exercised to ensure that maximum compatibility exists between the capabilities and limitations of the chosen technology and the requirements and restrictions of the usage environment. The constraints applicable to a high-speed-access, spacecraft memory intended to be used as the data storage medium for signals generated by a variety of sensor or scientific instruments encompass both electrical and physical aspects of implementation. Experience has shown, however, that the viability of a memory approach is determined most often by its operational parameters, rather than by its physical size and mass. Accordingly, the discussions made here are centered around the functional features of and general spaceflight environmental effects on the memory electronics.

The specific factors of importance that are reviewed in this section are the power dissipation, radiation resistance, and functional utility of a memory. Exorbitant power requirements are found to preclude the use of certain types of memory designs, almost totally irrespective of how good their operational characteristics may be, due to power budgeting and thermal management considerations aboard a space vehicle. The inherent "hardness" of a memory technology to the various sources of radiation encountered in space will have bearing on the amount of shielding necessary to prevent premature failure, and hence on the total payload that can be included on a particular mission. The functionality of a memory is considered here in the context of the effects that reconfigurability, redundancy, and self-test have on the overall system reliability. Where possible, the implications of trade-offs are pointed out with delineation made of those areas in which further development effort can be profitably pursued.

### 5.3.1 Dissipation

Power is limited—an obvious statement, but one that is especially true for long mission time, unattended space flights. Energy sources aboard a spacecraft as well as the equipments using their energy outputs are subject to failures and/or degraded outputs. Accordingly, the greater the operating margins that can be tailored into the systems aboard the craft the greater its probability of accomplishing a useful task. In the preceding sections the dissipation requirements of N-MOS, CCD, and MNOS forms of LST-1 and LST-2 camera memories were individually examined. Here the results of those calculations are collectively summarized and compared in light of the assigned power budget for each mission.

Within the timeframe of the first LST flight, the MNOS technology will not be available in the desired volume quantities. Only N-MOS and CCD memories are considered for the System A sensor instrument memory. Figure 5-15 shows a plot of the projected power dissipation levels for these two technologies along with the targeted budget for the mission. For simplicity, straightline approximations of the variations of power drain with word processing rate are used in this figure for both the N-MOS memory and the assigned budget. The CCD based memory shows no variation with event counting data rate because its dissipation is fixed instead by the pixel scan rate used with the particular sensor. In the case of System A, the scan rate established operational boundary is 3.0 MHz.

Visual comparison of the curves given shows that the "word random" format of the N-MOS memory results in its dissipation following the general trend-line shape of the assumed power budget, but remaining well below the limits set by that budget—even allowing for a pessimistic

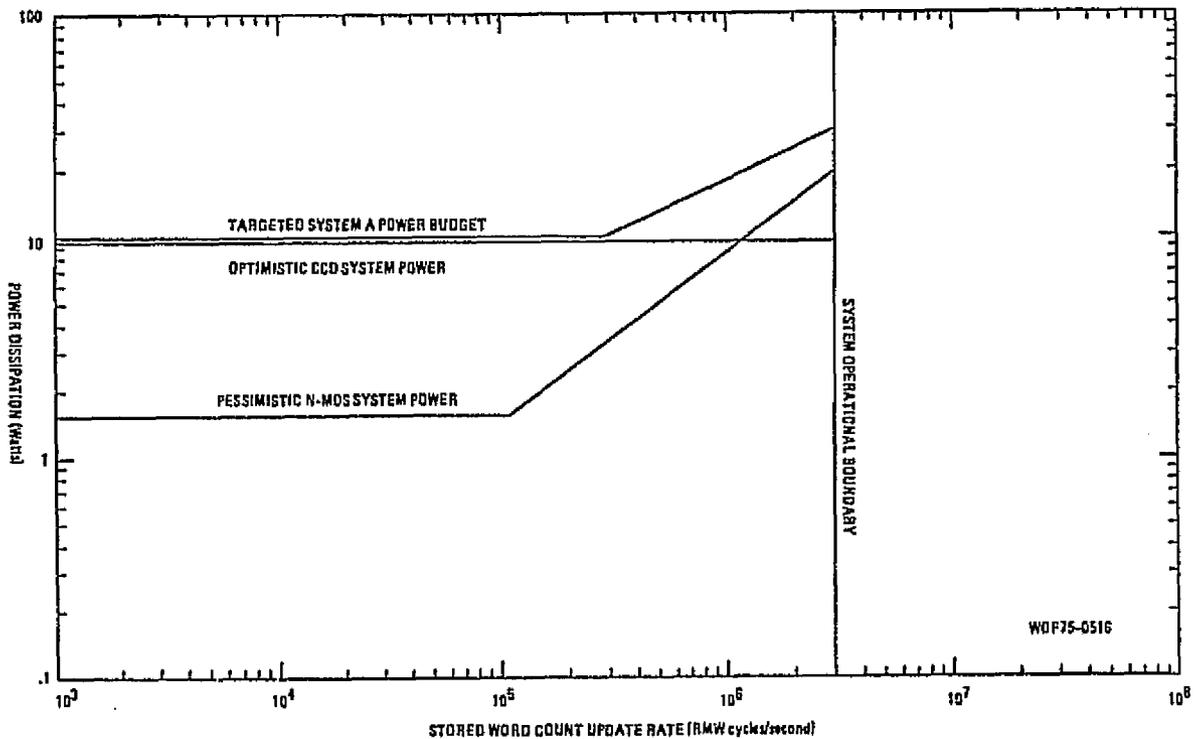


Figure 5-15. Comparison of Alternate System A Power Budgets

viewpoint of the memory's power consumption. The CCD memory, on the other hand, exhibits a constant dissipation which is well within the 30 Watt peak budget but, even when based on highly optimistic calculations, is only marginally within the 10 Watt average power budget for data rates of one tenth or less of the maximum. From this the conclusion is that either technology, strictly from power considerations, could be used, but N-MOS is far superior.

An equivalent set of comparison curves is presented in Figure 5-16 for camera memory System B. Within the timeframe of the LST-2 mission, MNOS devices should be readily available, so the projected dissipation level for an MNOS type memory is included. As shown by the figure, a CCD type

camera memory for LST-2 is totally nonviable. The most optimistic estimate of its dissipation level barely sneaks under the 50 Watt peak burst power budget at the 10 MHz word updating operational boundary. An equivalently optimistic estimate of the N-MOS based memory shows its dissipation under the best circumstances to be slightly in excess of the system budget at any data rate greater than 1 MHz.

The MNOS technology, due to its I/O operations being serialized, also exhibits a constant power dissipation independent of the event counting data rate. Pessimistically an MNOS form of the System B camera memory would require less than 18 Watts for its operation during periods of full activation. This exceeds the average 10 Watt budget but is well within the 50 Watt peak budget. Two observations must be made in this regard, however. First, the

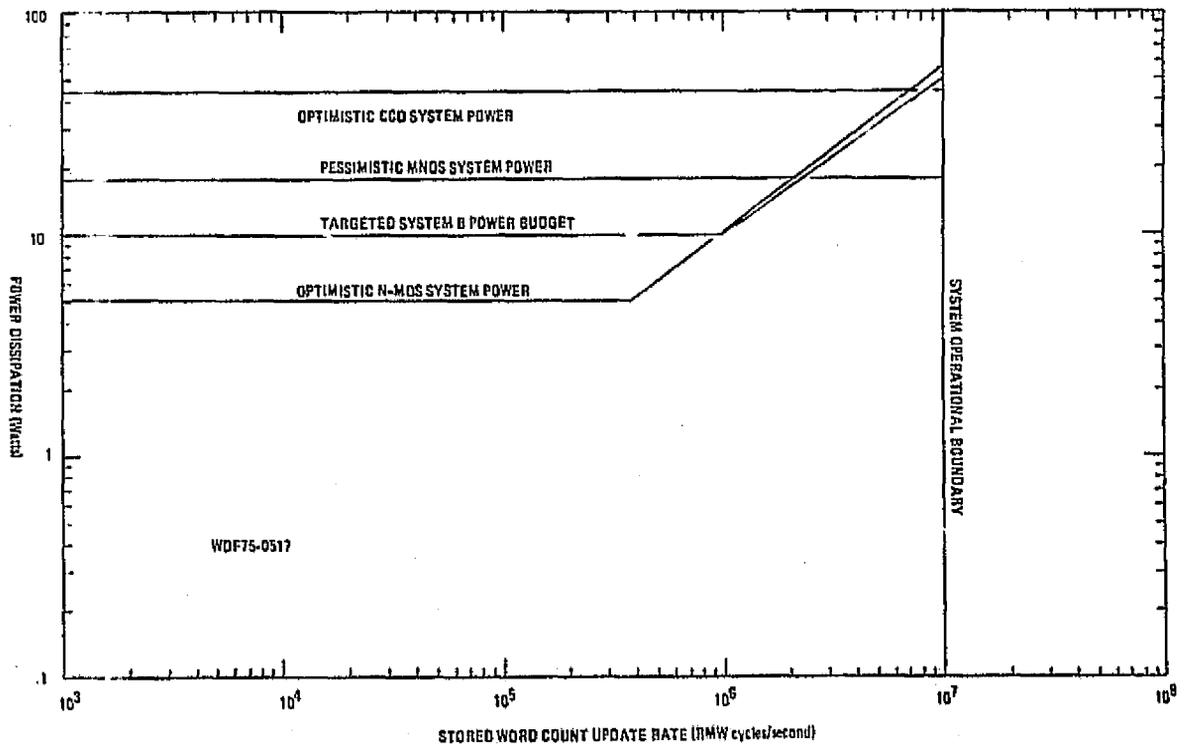


Figure 5-16. Comparison of Alterante System B Power Budgets

capacity of an MNOS based memory could be expanded by an order of magnitude or more and, for the same operating conditions, would require less than 2 Watts of additional power (strictly to support the increase in peripheral logic circuitry that would be necessary). Second, the data contents of the MNOS memory will be held inviolate even in the presence of temporary spacecraft power failures. Both of these factors are direct consequences of the inherent nonvolatility of the memory chips, and must weigh heavily on any decision regarding the power requirements of competing design alternatives. Without allowing for these aspects of system operation, no clear advantage can be cited at all data rates for either an N-MOS or an MNOS type System B camera memory. But, allowing for them, the MNOS system shows a distinct advantage for the total application.

### 5.3.2 Radiation

On space missions the radiation resistance of electronic equipment — especially memories — is very important. Depending on the type of mission, there are a number of different radiation environments to which a spacecraft may be exposed. For the present, attention is directed solely to the type of radiation exposure which a sensor instrument memory aboard an LST satellite will encounter in low earth orbits. For the projected LST orbital parameters of 330 nautical miles altitude and  $28.8^\circ$  polar inclination, NASA has determined<sup>(12)</sup> that the prime source of radiation is the South Atlantic Anomaly in the Van Allen belt which is centered at about  $35^\circ$  south latitude. Most radiation damage incurred by the LST will result from its passage through the edges of this zone. Figure 5-17 shows a cumulative plot of the average daily dose rate for the LST.

Under the particular orbital constraints of the LST, energetic electrons and protons are of nearly equal concern. At different altitudes and inclinations this is not always the case<sup>(13)</sup> and in general the proton component of the dose is the most important one to consider. Bremsstrahlung radiation has at times been a cause of worry, but all recent data indicates that it constitutes a second order source of radiation damage compared to protons. As seen from the cited dose rate plots, with aluminum shield thicknesses of under 100 mils, there is about three orders of magnitude difference between the contribution of electrons or protons and that of Bremsstrahlung radiation. For shield thicknesses greater than about 100 mils, both the electron and Bremsstrahlung components become negligible and only high energy proton effects remain.

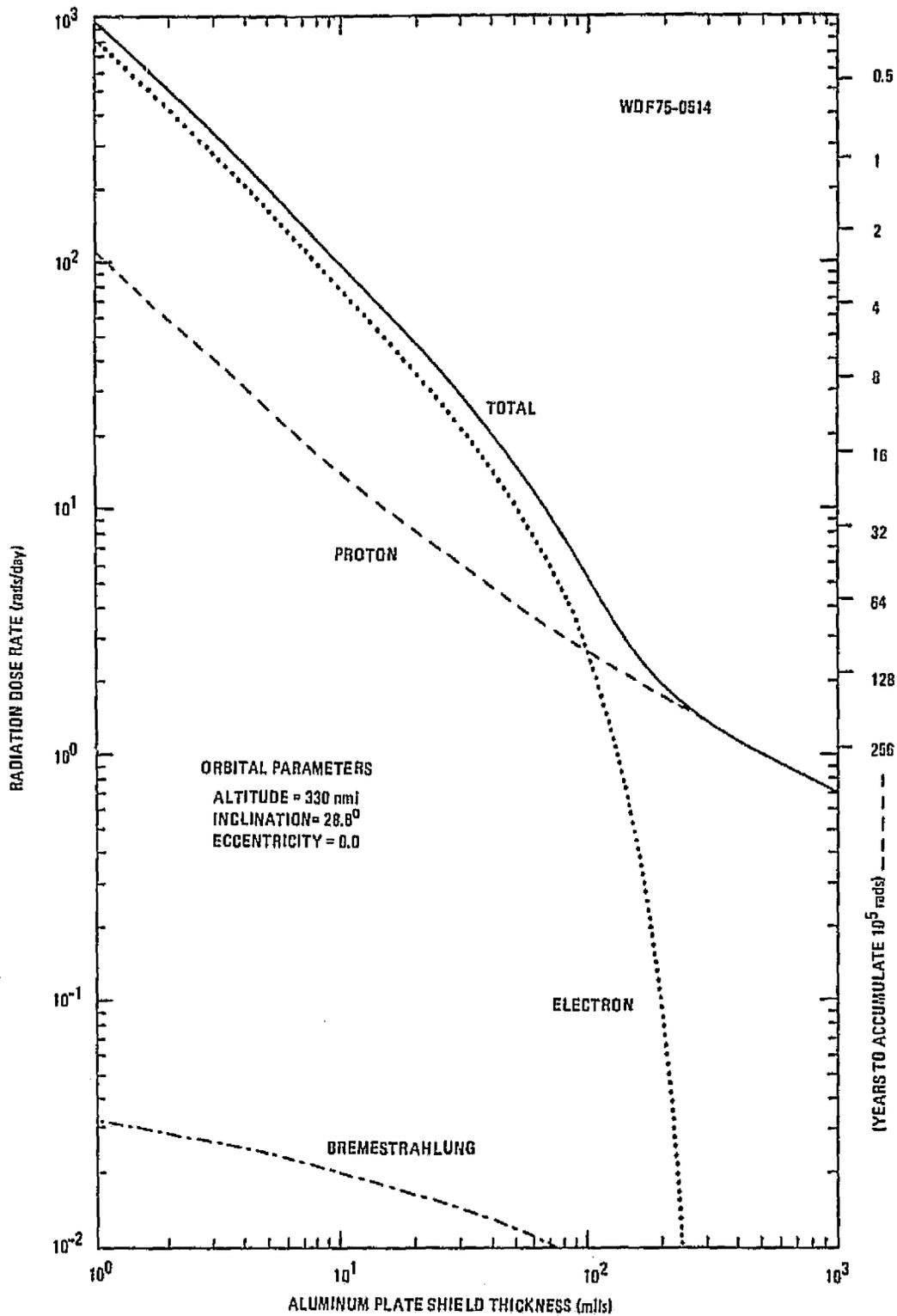


Figure 5-17. Particle Dose Rates Versus Aluminum Shield Thickness For LST

Numerous studies have been conducted by NASA, the Navy, and various companies in the space industry on the effects of radiation on LSI electronic components.<sup>(14)(15)</sup> As one expert noted,<sup>(16)</sup> "Experience has shown that, with today's level of processing technology, it is generally necessary to stay below approximately  $10^5$  rads cumulative dosage with any form of MOS device—either N or P-channel—to stay out of trouble with excessive threshold voltage shifts." This comment applies to all present forms of non-radiation-hardened MOS devices (P-MOS, N-MOS, MNOS, etc.), including both the 4K/N-MOS RAM's and 8K/MNOS BORAM's. It does not, at present, reflect the situation with CCD memory chips. A recent study by NRL<sup>(9)</sup> has shown that, due possibly to its presently less mature state of development, CCD technology structures can tolerate no more than about  $10^4$  rads before suffering excessive flat-band voltage shift, major degradation in transfer efficiency, and complete loss of effective dynamic range.

A factor not included in permanent radiation exposure considerations is the effect of peak instantaneous radiation flux density transient exposures, such as occur during passage through the Van Allen belt anomaly or during solar flare activity. It has been observed that transient exposure degrades performance of a memory device by inducing additional leakage in much the same manner as operation at elevated temperatures; and, it is compensated in the same way—namely, by increasing the refresh rate employed. Since MNOS devices are nonvolatile and require no refresh to maintain their stored contents, this is no major concern to their use. It could prove extremely important for certain types of spacecraft when using a volatile technology, however, and warrants careful consideration as it pertains to the specific mission.

In the case of the LST satellites, it appears conclusive from the foregoing observations that non-radiation-hardened N-MOS or MNOS memory devices possess sufficient intrinsic radiation tolerance to accomplish the assigned mission given a comparative minimum of enclosure shielding. Tests have shown<sup>(17)</sup> that aluminum shield thicknesses of no more than about 1/8th inch ( $\leq$  125 mils) are needed to effectively stop most primary electrons. Referring back to Figure 5-17 it is seen that, using only a 1/16th inch (62.5 mil) shield, an LST camera memory built with MOS devices capable of tolerating a cumulative dose of  $10^5$  rads would have to remain in orbit for better than twenty years before suffering major failures from the effects of permanent radiation damage. Transient radiation effects may therefore predominate on the LST mission, and further consideration of this point should be made prior to prototype memory development.

### 5.3.3 Functionality

To enhance the functional utility of a memory system, a number of schemes have been devised. Most involve the use of additional support and/or memory circuits that are tightly coupled to the main data storage array. This supplemental circuitry typically serves one or more of three principal purposes—namely:

- Reconfiguration — allows reorganization of the storage hierarchy so that different word sizes and/or word capacities are obtained.
- Redundancy — enhances reliability through the use of replicated circuits, switchable spares, error correction codes, or other fault circumvention technique.
- Self-Test — checks operational status of system by individually exercising respective components and subassemblies according to a predetermined (wired-in) test sequence.

Expansion of system complexity to accomplish these three goals is readily justified at ground based installations where maintenance is a comparatively easy task. Equivalent structuring of a memory intended for use on space vehicles which will be expected to function totally unattended over long mission times cannot be endorsed without carefully weighing the tradeoffs involved to determine whether the price that is paid — monetarily as well as in physical parameter effects — is too steep for the purported gains to be realized in performance.

To be viable for application in spacecraft memories, it is virtually mandatory that any specific approach to functionality expansion not degrade the overall system reliability. This requirement has the effect of excluding any design which serves exclusively to provide only one of the three main objectives listed above. Reconfigurability in a memory, for instance, when it is aimed solely at modification of the system

architecture to permit an altered global software viewpoint, will be unacceptable due to the degraded operational lifetime of the system which results from the increased overhead circuitry needed. Techniques which are practical for space missions incorporate elements of all three of the design criteria listed, and are universally founded on the principle of decomposition into "elementary segments" of repeatable and discretely analyzable circuitry blocks. (18) Modular redundancy, wherein the entire memory or else the storage and peripheral circuitry sections are duplicated with a switching network used to select between the primary and backup units, is the simplest concept. (19) Device sparing at the memory chip level with selection of good chips and deactivation of defective chips via a coordinate switching matrix is a closely related although considerably more intricate concept. (20) Both of these schemes bridge the boundaries of redundancy and reconfigurability but require some form of supplemental test function to determine when to shift between the replicated elementary segment units.

The two approaches to functional utility assurance which appear most desirable for exploitation in a spacecraft sensor instrument memory are:

- SECOR — single error correction based on "Hamming" type binary encoding using redundant parity bits of storage in each segment.
- EREX — error exorcism based on a shrinking-memory principle wherein failed segments are skipped in the memory addressing sequence.

Both of these schemes make provisions for all three main utility criteria, but in distinctly different ways. It is beyond the scope of this report to delve into detailed circuit designs for either since the variety of permutations possible is almost limitless. For the purposes of the present discussion, the fundamental features and characteristics of each technique will be briefly reviewed as it might exist in a camera memory built around

random accessed memory chips (such as the 4K/N-MOS RAM's). Similar, though somewhat modified and possibly more difficult to implement, operational features can be postulated for sequentially accessed structures.

SECOR. It will be recalled that an elementary segment (ELSEG) of storage in a totally nonredundant 4K/N-MOS RAM based memory contains 16 chips. According to standard Hamming coding theorems, to encode data words containing 16 bits in a manner which permits automatic correction of any single bit error in a word requires the use of 5 parity bits. Since these parity bits must be unique to each word and be made available at the same time that any given word is accessed, storage space must be provided within the ELSEG for these bits. This necessitates the introduction of 5 additional memory chips in each ELSEG; which, in turn, means that the ELSEG's storage capacity is increased from  $(4096 \times 16) = 65,536$  data bits to  $(4096 \times 21) = 90,112$  total bits, and thus has a 37.5% overhead burden.

In addition to the extra storage needed, support circuitry in the form of parity generators and error correction "trees" must be incorporated into the system. The exact point in the overall memory where these support functions are provided depends on the track taken to system organization. For simplicity in illustration, Figure 5-18 depicts the block diagram of a SECOR form of ELSEG as it would appear in a "modularized" memory where each elemental storage unit is able to functionally stand alone. The alternate to this is to employ an "OR-tie" design philosophy which calls for the commonalization at a single, bus interconnected site of all circuitry performing nonunique operations in successive ELSEG's. This has the desirable attributes of reduced component count and lowered dissipation, but it also allows greater interaction of failure modes among the bus connected ELSEG's.

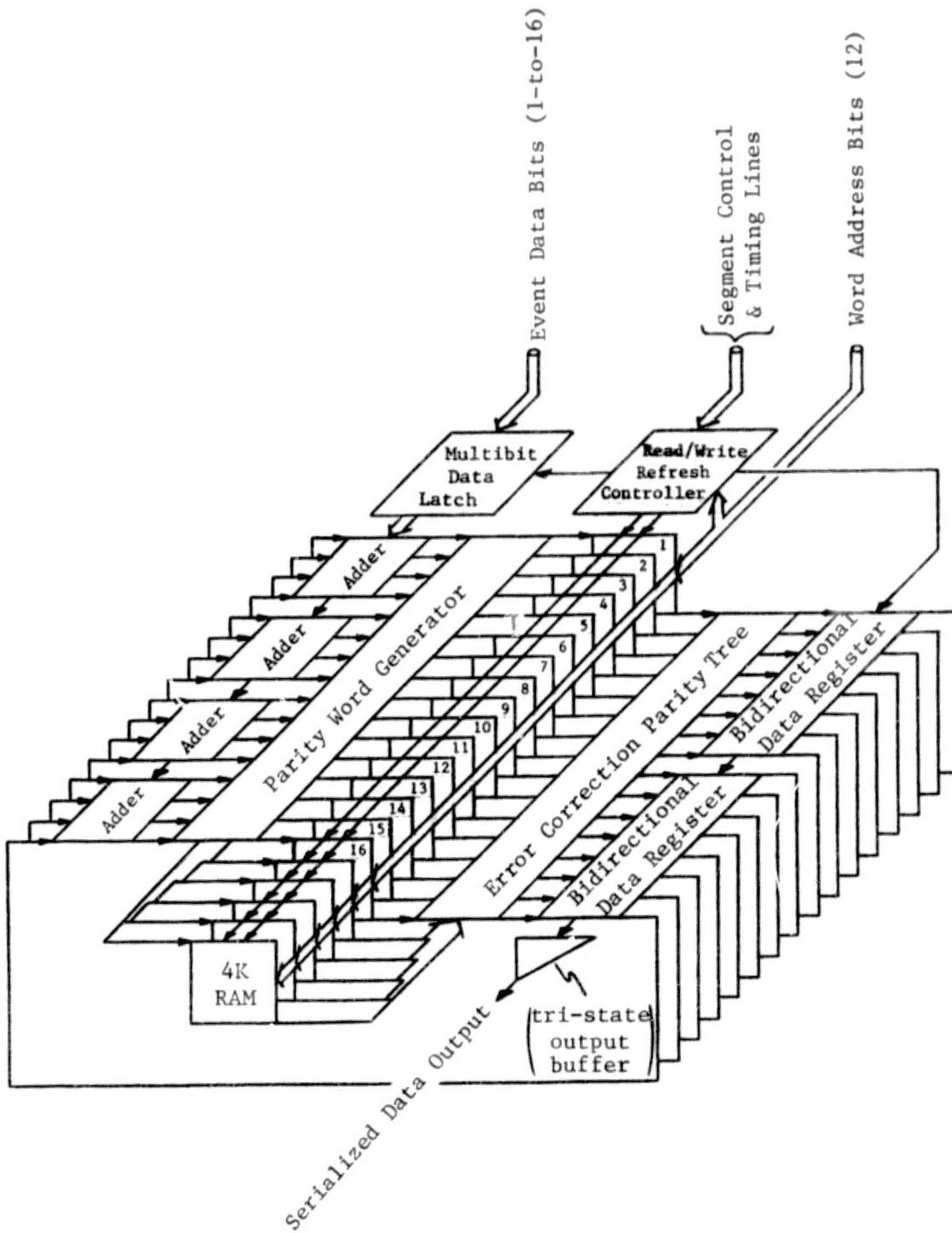


Figure 5-18.

4K/N-MOS RAM Based SECOR ELSEG Block Diagram

With the arrangement shown, operation of an individual storage segment proceeds as though it is an independent sub-memory. Refresh sequences and read/write timing signals are generated within each ELSEG in response to the master timing and control line inputs. Being self-contained, all refresh functions are transparent from any higher level in the system hierarchy. Individual ELSEG's thus appear to provide static data storage so long as the master clock continues to run and the word address lines are cycled in a normal fashion. With the "OR-tie" design this is not the case and direct consideration of necessary refresh operations must be made at the full system level.

During the SCAN mode of operation for the SIM (sensor instrument memory), the data "writing" sequences are enabled by the control signal commands. Subsequently, in response to the vector-unique timing signals (see paragraph 5.2.1), the 16 bit data word specified by the address bits is fetched, processed through the error correction parity tree to check for and remove any single bit errors, and loaded into the data registers where it is held temporarily. A parallel addition is then carried out between the register throughput bits and the incoming count update pixel event word. The resulting sum is written back into the original accessed word storage sites following generation of a new single error correction (SECOR) parity word. Output data "reading" proceeds in a similar fashion, but instead of coupling the accessed word back around to the adder, the bidirectional data register serializes successive bits in the word and shifts them out through a tri-state line driver.

In the modularized format depicted, the design of an ELSEG can be based on the exclusive use of CMOS or SOS/CMOS logic circuits. In the alternate bussed organization, the adder and certain line driver functions

will require the use of  $T^2L$  (or an equivalent family of devices) due to the higher speeds and greater line capacitances involved with shared function techniques. The component count for the modularized approach will be about 43 IC's per ELSEG, however, in contrast to roughly 25 IC's with the bussed design. As a result, the modular form of memory will have at least a factor of two more nonstorage components in a fully implemented system. This tends to counterindicate its use (but does not exclude it) and makes the bussed architecture the preferred approach.

EREX. Although the name given to this approach to functionality enhancement is somewhat ostentatious, it is reasonably apropos. Exorcism is defined as the process of driving out evil spirits through adjuration under penalty of suffering a curse for failure. In the case of "error-exorcism" from a memory, the evil spirits are defective storage sites, the adjuration is an electronically uttered admonition to avoid faulty areas, and the curse incurred by not expelling disruptive elements is functional death to the entire system. Each segment of storage exorcised from the memory causes the effective, usable capacity of the memory to shrink by a discrete, elemental amount. Thereafter the system performs in a totally normal manner, except that it gives the appearance of having been implemented with a lower than expected storage capability. A simplified representation of the error-exorcism principle is depicted in Figure 5-19.

Error exorcism is not to be confused with switchable sparing techniques. The use of spares in a memory system requires that the storage section of the memory be especially configured to include a matrix (of one form or another) of switches and a corresponding maze of interconnect lines.

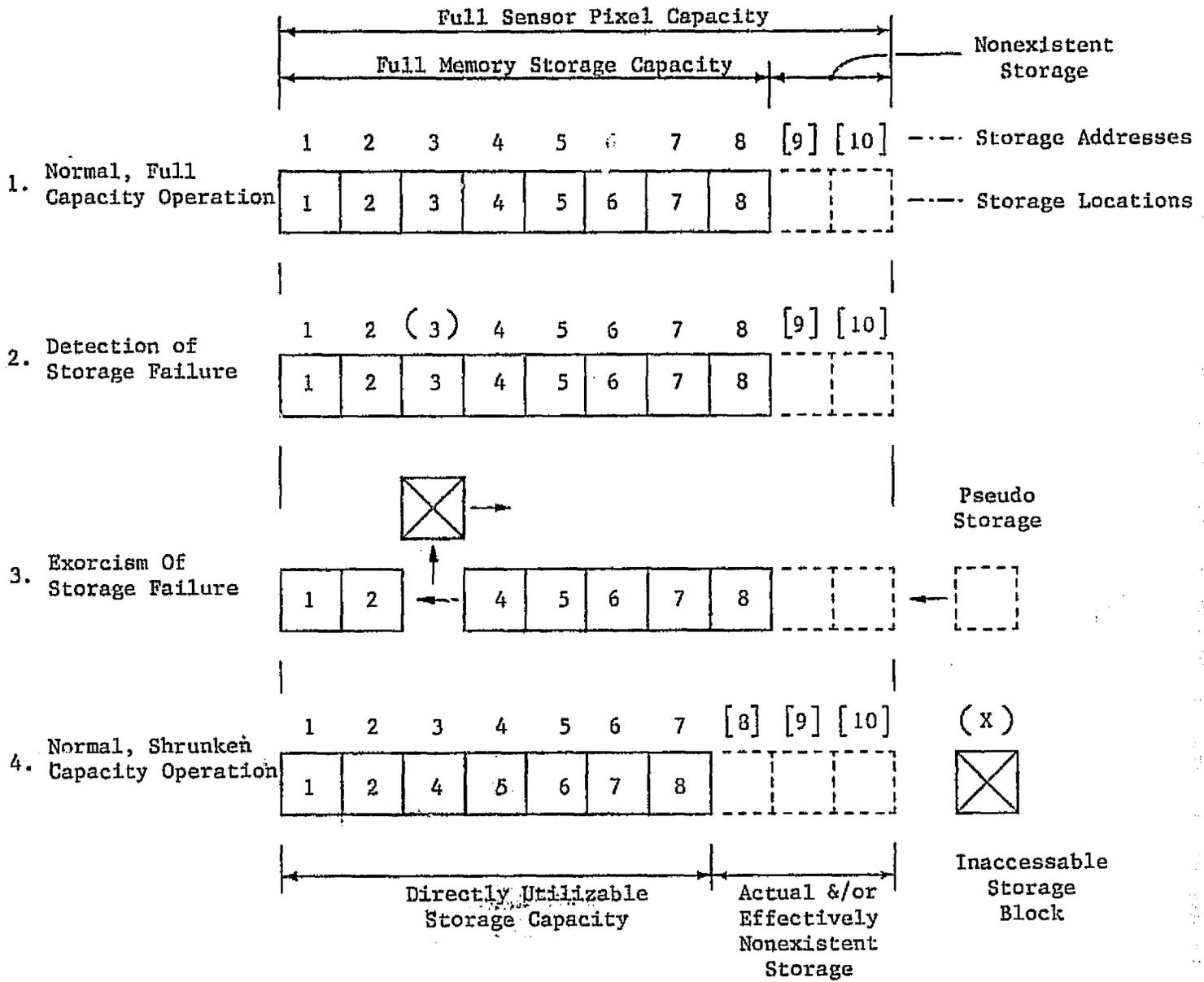


Figure 5-19.

Simplified Representation OF Error Excision Principle

The application of EREX techniques, contrastingly, involves no alteration in the basic storage array design and necessitates only minor interfacing modification of the memory address generator and data I/O circuitry. The electronics necessary to perform the error exorcism function is effectively an "add-on" item which can be included or deleted from the memory peripheral circuitry section.

In practical realizations of the EREX principle, both an "on-line" section and an "off-line" section will be present. The "on-line" section checks the current and up-coming memory storage addresses against a set of storage site error flags which are filed according to the address location and causes those sites which are "flagged" to be skipped in the accessing sequence. This section performs its assigned tasks while the memory is dynamically interactive with another machine (which, in the case of the LST application, would be when it is either inputting data from one of the sensor instruments or is outputting data to one of the down stream data handing devices, such as the rf data link transmitter). The "off-line" section is responsible for detecting storage site problems and "flagging" those portions which are defective. It contains a controller which exercises each storage location according to a prescribed test sequence while the system is not engaged in processing data. Typically, all elemental storage units in the memory are subjected to the test, even though specific ones may have been set aside as inoperative previously. This allows for the possibility of self-healing, which has been found to occur on occasion. A major consideration in the design of the self-test circuitry is the test pattern employed.<sup>(21)</sup> Overly intricate patterns will consume excess time, whereas those that are too simple will miss certain kinds of defects.

Shrinking capacity fault tolerance schemes like EREX are most readily implemented in memory systems having a random accessed (either word or block) organizational hierarchy and a well defined or fixed addressing sequence. While the problem is not insurmountable, difficulty is encountered with a serial memory in maintaining synchronization as portions of storage are deleted. Similarly, predetermination of the accessing order is not mandatory, but without it the speed of operation will suffer. Full assessment of the tradeoffs between SECOR and EREX as they relate to memories intended for use on space missions would require the use of lengthy and exceedingly complex reliability modeling equations.<sup>(22)</sup> cursory examination of the two approaches to functionality enhancement does, however, point out certain general traits ascribable to each. Specifically,

- SECOR, like switchable sparing, demands a specially designed storage array section.
- EREX requires no special storage array design and is introduced as an "add-on".
  
- SECOR causes an across-the-board burden of at least 38% in redundant main memory parts.
- EREX involves no main memory parts redundancy and only about a 20% increase in support circuits.
  
- SECOR is based on established Hamming encoding techniques and has proven designs already available.
- EREX constitutes a new, less widely recognized concept and still needs design confirmation.

Review of these factors leads to the observation that, although it involves a slightly higher development risk, EREX ranks as the preferred approach and should be given further consideration during the early phases of design work on any spacecraft sensor instrument memory having a capacity of  $10^5$  words or greater.

## 6.0 PERORATION

This report has presented a number of wide ranging discussions, some of which have been broad in nature and others of which have dealt with narrowly defined specific factors, related to the subject of high-speed-access sensor instrument memories which may find use on future space missions. To tie the diverse considerations involved concisely together, three main points must be covered:

- Identification of the memory technology(ies) best suited to the production of a camera memory for LST-1 (system A) and for LST-2 (system B).
- Elucidation of suggested design implementations which may be applied to the production of system A and B camera memory breadboards.
- Delineation of the estimated scheduling and funding necessary to the procurement of developmental system A and B camera memories.

It is the purpose of this section to treat these three topics in sufficient detail that NASA can proceed in an enlightened manner with the planning of near term (3-to-6 years hence) space missions which require the availability of reasonable cost, high performance memory systems.

The choices made between memory technologies and the suggested system design implementation techniques are derived or are direct extensions of the material developed at length in prior sections. Consequently, certain points are called out or cited without further elucidation. Clarification of these points, when encountered, can be secured by referring back to the appropriate section in which they were first developed. The costing and scheduling estimates given are based on best engineering judgment and reflect present projections on both device pricing and man-hour costing rates over the next few years.

## 6.1 Technology Selections

After screening the full spectrum of memory technologies that are potentially applicable to the LST memory requirement, three prime candidate technologies are found to remain; namely--N-MOS, CCD, and MNOS. These technologies have been individually examined and compared under two sets of spacecraft camera memory requirements: one having a 500 Kbit storage capacity (System A), and the other having a 4 Mbit capacity. The selections of recommended technologies for these applications are based on considerations of cost, reliability, and power when evaluated within the context of satisfying availability timeframes of 1976 and 1978, respectively, for systems A and B.

Cost comparisons are made on the basis of current device costs being projected into the time periods of interest. Presently the 4K/N-MOS RAM's possess a distinct price advantage, and it is anticipated that this advantage will be maintained through 1976. With the assumption that the economic drivers behind each technology remain firm, a crossover point will be reached about 1978 when little cost differential exists among the three technologies. Beyond that time a rapidly widening margin in favor of MNOS is forecast. Hence, on the basis of cost, the use of 4K/N-MOS RAM's in System A and 8K/MNOS BORAM's in System B loom as the most cost effective approaches to the respective applications.

Reliability considerations are reflected in both system organizations and inherent device characteristics. Reliability enhancement at the system level is accomplished through redundancy of one form or another. Its use, however, adversely affects system complexity, cost, and power. At the device level, improved reliability is secured through inactivity of the storage medium (i.e., by making it "dormant"). This capability is inherent in the

nonvolatile MNOS technology. Subsequently, analysis of the reliability of 500 Kbit and 4 Mbit memory capacities configured from volatile and nonvolatile technologies reveals that nonredundant organizations are capable of realizing 95% probability of success levels over 1 year mission times for System B as well as System A — provided nonvolatile chips are used in System B. Thus, on the basis of reliability, the use of 8K/MNOS BORAM chips is indicated for System B; while for System A the preferred choice is 4K/N-MOS RAM chips due to their established reliability history.

Power budgeting in a spacecraft is a well known critical parameter. Examinations of the dissipation requirements of camera memory designs based on the N-MOS, CCD, and MNOS technologies indicate that random accessed 4K/N-MOS memory units come closest to meeting the overall system boundary specifications. In the System A application, the pessimistic power requirement of a 4K/N-MOS RAM design, including all peripheral support circuitry power, is well below the budgeted 10 Watts average at photoelectron event counting rates of less than 1 MHz, and remains below 20 Watts at the maximum event counting rate of 3 MHz. In comparison, a CCD design with support circuits optimistically draws a constant 10 Watts of power in this application, independent of the event occurrence rate. Since the estimated rate will generally, except for bursts, be below 1 MHz, the use of 4K/N-MOS RAM's is seen from the standpoint of the power criteria as being the best approach for System A. In the System B application the N-MOS technology continues to exhibit the lowest average operating power when nonredundant design philosophies are maintained. CCD requires the most power, running about a factor of four above MNOS which is estimated at 8 Watts for the storage section alone. Although it draws the least power, N-MOS cannot meet the

system reliability requirements of System B in the nonredundant configuration. Consequently, the best choice is clearly the use of 8K/MNOS devices, even though the system power budget would have to be relaxed slightly to allow for an average power of about 18 Watts to cover both the memory and its support circuits.

To summarize, the conclusions reached by this study regarding technologies recommended for use in spacecraft memories that will be deployed in the near future are as follows:

(System A) technology - N-MOS  
device - 4096 bit RAM  
design - Simplex (nonredundant)

(System B) technology - MNOS  
device - 8192 bit BORAM  
design - Simplex (nonredundant)

The bases for these recommendations are:

(System A) - absolute lowest cost and power option available

(System B) - power for reliability trade-off at lowest cost.

## 6.2 Design Suggestions

The design of a camera memory system to be used on a space mission must be efficient in its utilization of parts, power, and space. Parts count will have a direct bearing on the memory's production costs as well as its subsequent operating lifetime (reliability). Power dissipation within the memory will be reflected in the spacecraft thermal management provisions required and the power cell weight loads. The volumetric needs of the camera memory are affected by the components used, the design philosophy applied, and the packaging technique employed.

As indicated earlier in Table 2-2, the requirements for the forthcoming LST satellite missions treat two different sensor instrument (or camera) memory systems. The designs suggested for these two memories are nonredundant (or simplex) in their basic implementation philosophy, with the storage media being 4K/N-MOS RAM chips in System A and 8K/MNOS BORAM chips in System B. Organizational details of the respective designs are based on the commonization of circuit functions through the use of bussed interconnect techniques to minimize system component count and power dissipation. Structuring of the storage section hierarchy follows the principles evolved in Section 5, with interfaces established in accordance with the "black box" I/O's defined by Figure 2-2.

In the following paragraphs consideration is given individually to the circuitry schemes applicable to the implementation of LST camera memory systems A and B. Detailed treatment is given to the N-MOS design approach suggested for System A and a preliminary design for the MNOS form of System B is described. The terminology employed follows the conventions established in previous sections, and some foreknowledge of this material is assumed.

### 6.2.1 System A

The suggested design approach for a spacecraft sensor instrument memory (SIM) in the capacity range of LST camera memory System A consists of a nonredundant (simplex) system architecture having a storage hierarchy based on the "word random" accessing philosophy, with implementation facilitated through the use of commercially available 4096 bit N-MOS RAM devices. This approach has the combined attributes of: (1) minimum investment in reliability enhancement overhead electronics, (2) use of memory devices of proven characteristics which are in volume production and are inexpensive, and (3) direct variance of power with quantity per unit time of photo-event data processed rather than sensor sequencing rate.

Electrical Design. Data storage in the memory is built up from elementary segments (ELSEG's) containing 16 memory chips of 4 Kbits each. The storage capacity of an ELSEG is 4096 words, each of which contains 16 bits accessed in parallel. The data word rate handling capability of an ELSEG is identical to the data bit rate capability of its constituent chips. With designs founded on 4K/N-MOS RAM interchangeable consensus specifications, this means that an ELSEG can perform a read-modify-write operation in 800 nanoseconds, or, equivalently, that it can update its storage contents at a continuous rate of  $1.25 \times 10^6$  words/second. By employing one ELSEG in each of 4 separate, quadrature-time-phase related "vector" addressing spaces and multiplexing their I/O operations, a peak data rate of 5.0 MHz can be attained. This constitutes a design margin of 67% beyond the 3.0 MHz requirement of System A, and allows for perturbations in the initial bread-board development.

The 4 time phased ELSEG vectors that are placed in parallel to achieve the necessary data rate form one "sector" of memory storage having a capacity of  $(4096 \times 4) = 16,384$  words. Since this is exactly half of the total capacity needed by System A, a single sector of storage exactly corresponds to one "section" of the memory. Two sections (or simply two sectors) provide 32,768 words of storage, just slightly in excess of the minimum 32,000 word capacity requirement for the system.

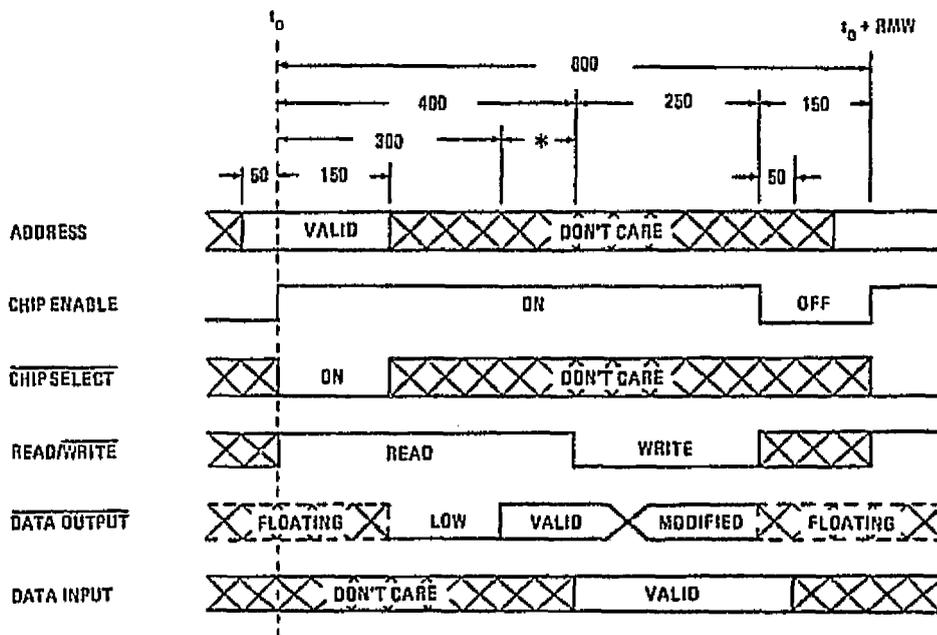
Note: Do not confuse the terms "sector" and "section". Specification of the number of sections to be used in the memory is made on the basis of macroscopic system level considerations of the application requirements. Determination of the storage capacity of successive sectors is made from microscopic device level implementation considerations. Any system may have one or more sections, and each section may contain one or more sectors. It is purely coincidental that in System A the boundaries of a sector and a section are identical.

Figure 6-1 presents a full block diagram of the suggested design for LST camera memory System A. The assorted I/O lines denoted here correspond to those established from "black box" definitions of the system electrical interfaces. Subdivision of the memory electronics is into three principal parts; viz, the "peripheral" control circuitry and two data storage sections (or sectors). The ELSEG's located adjacent to one another in the two sectors are considered part of the same storage access "vector" and therefore have their data I/O, address, and control lines bus connected in common across the sector boundaries. Maintenance of the separation of failure modes between the two storage sections is secured through the use of section-unique I/O line buffers (which, in this instance, are considered to be contained in the 4K-Word ELSEG blocks). This "or-tie" approach to system design is adopted in preference to any form of "self-sufficiency" scheme because it contributes to simpler ELSEG's, reduced support electronics, and lower memory dissipation.



To address individually any of the 32,768 words in System A requires a binary address counter of 15 bits. The two least significant bits (LSB's) out of the counter are decoded into 4 lines which are used to strobe the respective storage vector cycle enable latches. These latches serve to hold the 4 most recent states of the event detection data line. The 12 ISB's (intermediate significant bits) are fed through line drivers to the address inputs of every RAM chip in the memory to allow progressive selection of words from the 4 ELSEG's in the active storage sector. The MSB (most significant bit) from the address counter is used to alternately inhibit and enable the chip select lines of the ELSEG RAM's in each of the two memory sectors. Separation of the count accumulation or imaging data from two quasi-independent 100 x 160 element camera detectors is provided by reserving one sector (i.e., section) of storage for each camera output.

Read-Modify-Write (RMW) cycle timing for the 4K/N-MOS RAM's contributing individual bits to each ELSEG word is shown in Figure 6-2. This diagram is derived from consensus specifications of currently available chips and facilitates the interchangeable use of the major semiconductor manufacturer's standard line devices. This factor should be particularly convenient during the initial phases of breadboard development. All sequences within a 4K RAM are initiated by a low-to-high transition of the chip enable (CE) clocking signal and must be concluded while this signal is in its high state. The chip select ( $\overline{CS}$ ) line determines whether externally interactive data I/O exchanges will take place or simply an internal cell refresh operation. If data is to be read-out or written-in, the  $\overline{CS}$  signal must be low for 150 nanoseconds following the CE low-to-high transition. Its state at all other times is indeterminate (i.e., "don't care").



\* 100 NANOSECOND PERIOD ALLOTTED TO EXTERNAL CIRCUITRY TO MODIFY VALID READ DATA AND RETURN IT AS VALID INPUT WRITE DATA.

(all numerical time intervals are in nanoseconds)

Figure 6-2. Consensus 4K/N-MOS RAM Minimum Read-Modify-Write Cycle

The 12 bit-selection addresses to each RAM are set up 50 nanoseconds prior to and are held for 150 nanoseconds following the CE clock edge. At all other times the states of the address lines are "don't care" and they are free to change at will. Read accessing of valid output data occurs within 300 nanoseconds of the CE leading edge when the read/write ( $R/\bar{W}$ ) line is in its high state. During the time when accumulated photoelectron count information is being output from the memory to a down-stream companion machine, only the "read" portion of the illustrated RMW cycle will be executed. This is facilitated by holding the  $R/\bar{W}$  line in a constant high state. In contrast, a burst refresh of all cells on the chip is accomplished by holding the  $\bar{CS}$  line high and the  $R/\bar{W}$  line low while sequencing through the 5 or 6 (depending on which particular vendor's chips are being used) LSB row addressing bits.

In the complete data accumulation RMW cycle, the modified data is latched and held as valid input write data 400 nanoseconds after the CE clock edge. At the same time the  $R/\bar{W}$  signal is transitioned from high-to-low to cause the input data to be written into the selected storage cell. The minimum low state interval for the  $R/\bar{W}$  line is 250 nanoseconds. At the end of that time the CE line is returned low and the  $R/\bar{W}$  line is free to change until the next low-to-high CE transition. Following turn off of the CE signal the input data remains held in a valid state for at least 50 nanoseconds. After that, up until the time it is again latched in the next RMW cycle, it is free to change. Completion of the RMW cycle requires that the CE line remain low for at least 150 nanoseconds while internal nodes in the chip are precharged. The elapsed time for a full RMW cycle is 800 nanoseconds, corresponding to the specified 1.25 MHz RMW rate for individual ELSEG's.

With operation of successive vectors being time phased, it is necessary that each vector be supplied with an independently generated set of CE and  $R/\bar{W}$  signals. Master phasing control of these vector-unique signals is facilitated through the multi-phased memory clock generator while divides down the externally supplied master system clock. Synchronization of the memory address generation process with the sensor pixel scan is via a secondary timing signal fed to the clock generator. Mode inputs to the program mode and self-test controller are used to establish the functional states necessary throughout the memory for the writing, reading, and storage testing modes of operation.

No specification of the exact form of the optional test port is made. It is possible to accomplish the test mode operations solely through

the single data output port, but a faster and more versatile arrangement may be to tap out the 16 parallel data bit lines appearing at either the input or output of the adder. This aspect of the memory design will ultimately be settled during system breadboarding.

To conserve on total support electronics overhead power, extensive use should be made of CMOS or SOS/CMOS logic families. The only place where variance from the theme is necessary is for the binary adder. No known CMOS adder combination can complete a 16 bit addition in a guaranteed time of under 100 nanoseconds. TTL adders, on the other hand, can, so they are specified for the memory despite the power penalty that is incurred by their use. To ensure that this adder overhead power cost is paid only once, though, the design of System A incorporates a multiplexing scheme whereby a single 16 bit adder is shared among the 4 time phased vectors. Inputs to the adder are derived from the detector pixel word data lines (which may be either 1 or 4 bits wide) and from the 1-of-4 vector word multiplexer (which throughputs 16 parallel bits from the selected vector ELSEG).

Aside: Observe that all 16 bits in a stored word must be processed through a RMW cycle each time a given word is accessed from memory. Consequently, the simplest means of incrementing the stored count in response to the bit pattern in the input photo detection word is to provide a 16 bit adder circuit to accomplish the necessary operations all in one step. Once such an adder is in place it makes no difference whether the input word contains 1 bit or 4 bits (or even 16 bits for that matter) in parallel. Although the system is spec'd to handle only 4 bit A/D signals, it could just as easily process data from 8, 10, or 12 bit A/D's. The total capacity would, of course, be exceeded much more rapidly if the system continues to be used in a count accumulation mode. The more likely use with wider width A/D's is frame-to-frame image comparison or subtraction operations.

Figure 6-3 illustrates the sequence of waveforms needed by the vector word multiplexer to allow it to share the availability time of the

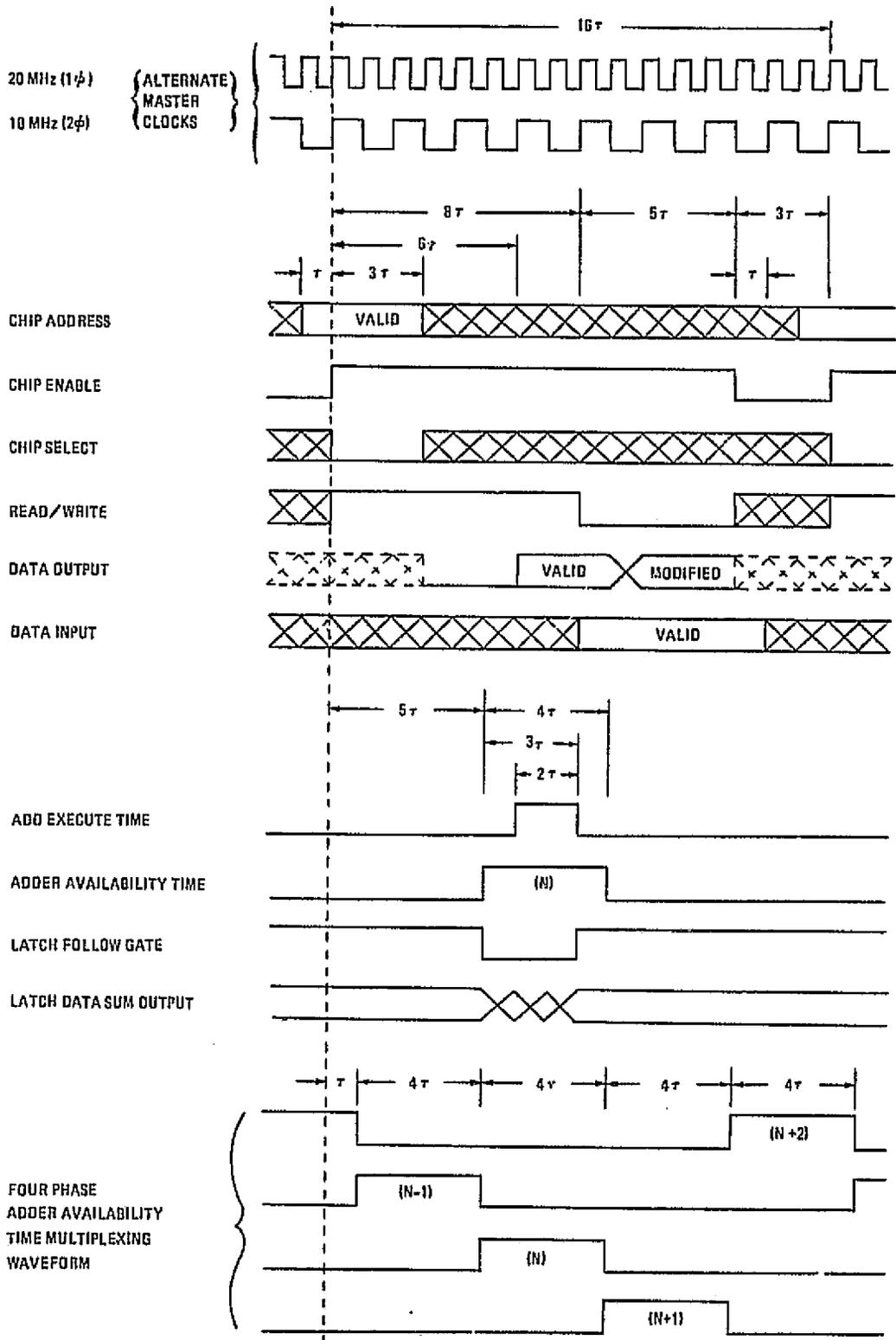


Figure 6-3. N-MOS System A RMW Multiplexed Adder Timing Diagram

adder between the memory's four storage vectors. This diagram depicts in a totally generalized format the timing interrelationships between the vector output multiplexer sequencing, the adder and data latch operation, and the ELSEG chip RMW cycling for any "r'th" vector. The time periods follow those described on Figure 6-2, which gave the minimum periods permissible. Variations of the memory address and camera pixel scanning rates can be tolerated over the range of

$$50 \text{ nanoseconds} \leq \tau < (2000/2^n) \text{ microseconds}$$

where "n" is the number of row address bits necessary to a chip refresh cycle. Subdivision of the memory timing sequences into the incremental  $\tau$  intervals required to establish the timing depicted is facilitated through the use of either a two phase clock running at a rate of  $1/2\tau$  (10 MHz for  $\tau = 50\text{ns}$ ) or a single phase clock running at  $1/\tau$  (20 MHz for  $\tau = 50\text{ns}$ ).

Nonzero event count data must be available from the sensor element corresponding to the memory word addressed during the r'th adder availability interval. To allow for the delay in accessing read data from the RAM chips, and to prevent RMW cycling for zero count (no event) pixels, a two-bit-time delay register is introduced between the external data input port and the adder input while an "Exclusive-OR" form of event detector is used to feed a state control signal to each vector's cycle enable latch. Strobing of the event detection signal occurs on the trailing (high-to-low transition) edge of the individual vector's CE generator signal. The resulting latch output determines whether that vector's next RMW cycle is executed or skipped.

Implemented according to the electrical design principles that are suggested here, a System A sensor instrument memory will be able to perform all of the tasks set forth for the LST-1 camera memory. Operation can proceed with any type of limited internal storage time detector possessing either a high-speed, multi-bit A/D converter or a binary threshold detector and centroiding circuit (such as exists in a Boksenberg photon counting camera). Data from detector arrays having up to 32,768 pixels can be stored directly, or sections of the size can be selected from larger arrays. The windowing algorithms necessary to accomplish the desired area segregation, however, must be generated and controlled by the on-board sensor instrument package processor. Such algorithms are invisible to the camera memory, other than in the manner in which they affect the "program word" (see Section 5).

Physical Parameters. For the suggested System A memory design, the cumulative component count consists nominally of 128 N-MOS 4 K bit RAM's, approximately an equal number of SSI and MSI logic devices, and on the order of 100 passive filter capacitors. Based on worst case power calculations, the system dissipation should be below 25 watts @ 3.0 MHz and below 5 watts @  $\leq$  300 KHz. Assuming a total thermal resistance from chip surface to memory module chassis of  $50^{\circ}\text{C}/\text{W}$ , the worst case temperature rise of any chip above the operating chassis ambient should be less than  $10^{\circ}\text{C}$ .

Figure 6-4 depicts one conceptual format of the System A mechanical packaging configuration. The chassis dimensions anticipated are on the order of 9.5 x 9.5 x 6.5 inches, yielding a total volume of approximately  $586 \text{ in}^3$  (or about 9.6 liters). Component assembly is based on standard multilayer p.c. board processes using mil grade dip packages. The total

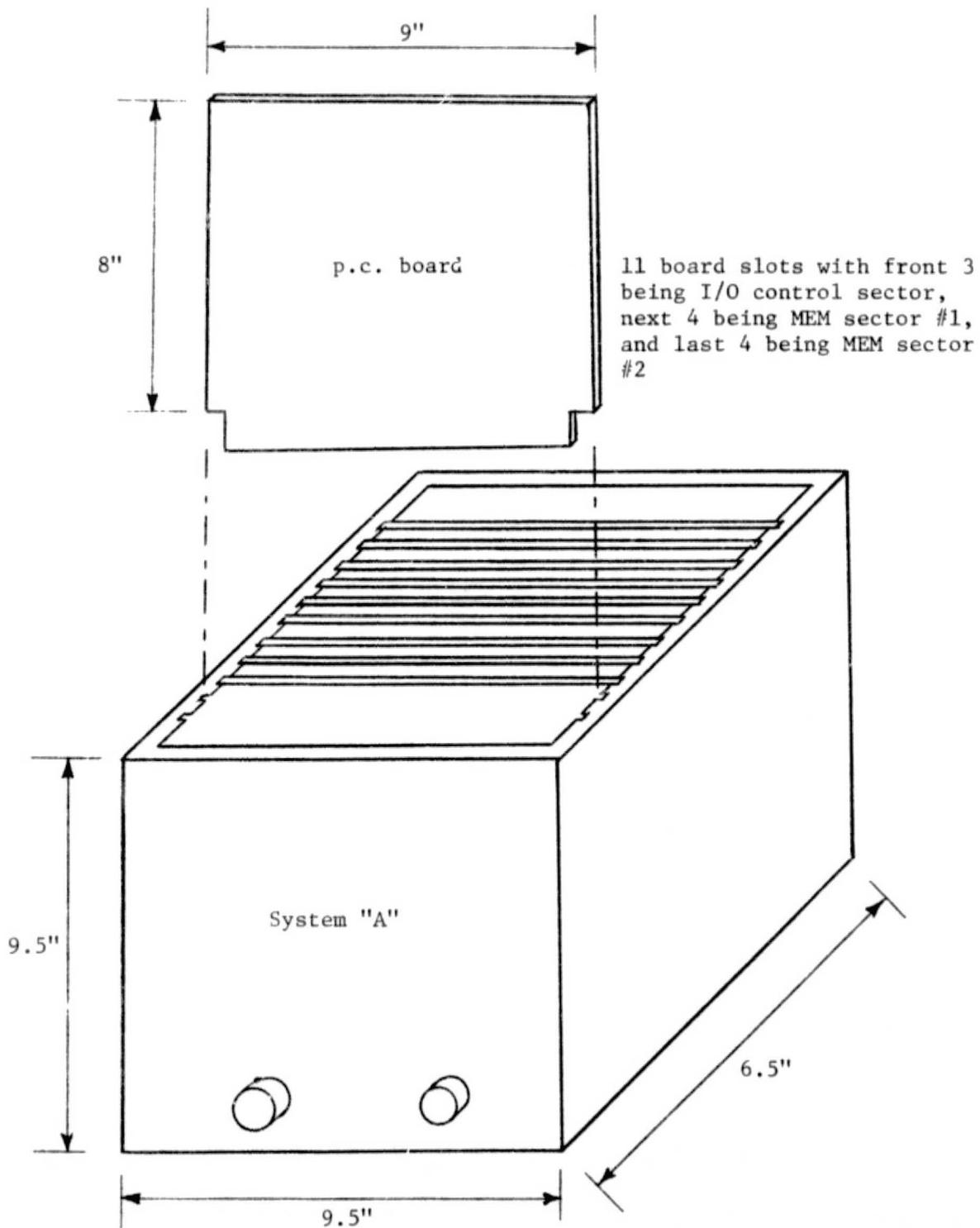


Figure 6-4. System "A" Conceptual Mechanical Configuration  
(with board access cover plate removed)

mass of a flight qualified unit, allowing for 1/16 inch aluminum for added radiation shielding to ensure a total dosage tolerance level of  $> 10^5$  rads, should be no greater than 10 pounds ( $\approx 4.5$  Kg). Table 6-1 itemizes the list of characteristics projected for a 4K/N-MOS RAM implementation of the System A camera memory. All the system requirements can be met or exceeded in flight qualified models.

System Scaling. It is possible to expand the storage capacity of the design suggested for System A up to approximately the level required by the LST-2 camera memory System B, but at some cost in performance and a marked sacrifice in reliability. The smallest interchangeable expansion block of storage is one sector, which contains 16K words. By incorporating 16 such sectors a total capacity of 262,144 words can be provided, but the data word rate of the resultant system would be limited to 5.0 MHz.

In general the data rate handling capability of the memory is directly related to the number of addressable storage vectors in each sector according to

$$f_{\text{data}} = 1.25 \times 10^6 \times R \frac{\text{vectors}}{\text{sectors}} \text{ (words/second).}$$

Accordingly, to achieve (at least marginally) a 10 MHz word processing rate,  $R = 8$  ELSEG vectors would be needed — rather than four as in System A. With eight phases required to access the paralleled storage vectors, the add time allotted to successive vectors using a single, shared adder circuit would then be only 50 nanoseconds. It is expected that this will prove to be too critical a parameter and will necessitate a modification in the multiplexing scheme applied to the adder, probably involving the use of two adders.

Table 6-1. PROJECTED 4K/N-MOS RAM BASED SYSTEM A CHARACTERISTICS

Parameter	Characteristics
Organization (memory sectors/system)	2
Word Capacity (words/memory)	32,768
Word Size (bits/word)	16
Bit Capacity (bits/memory)	524,288
Pixel Scan Rate (MHz)	3.0
Pixel Count Size (bits/count)	1 or 4
Active Component Count (total chips/system)	~ 260
Memory Chip Count (RAM chips/system)	128
Average Power Dissipation (watts/system)	< 5 @ $\leq$ 300 KHz
Peak Burst Power Dissipation (watts/system)	< 25 @ 3 MHz
Physical Construction	ceramic dip/pc boards
Physical Volume (liters/in <sup>3</sup> )	~ 9.6/586
Physical Mass (Kg/lbs)	~ 4.5/10
System Scaleability (max # words)	$\leq$ 262,144 @ reduced reliability
Storage Ambient ( $^{\circ}$ C)	-55 to +70
Operating Ambient ( $^{\circ}$ C)	-10 to +40
Radiation Tolerance (rads total dosage)	> $10^5$
Soft Error Rate (errors/bit)	< $10^{-10}$
Hard Error Limit (for system failure)	< 1 full sector functional
Mission Time (years)	1
Reliability (% probability of success)	> 95
Availability: breadboard system	1976
flight prototype units	1978

Expansion of the number of storage vectors or the number of sectors in the memory also introduces additional support circuitry. When the number of vectors is increased from 4 to 8, one additional bit must be included in the address counter. Similarly, if the number of sectors is increased from 2 to 8 (or 16), then 2 (or 3) additional bits will be needed in the counter chain. The system power will thus increase and its reliability decrease as direct functions of the total data storage capacity. This is the adverse trade-off which ultimately limits the maximum degree of system scaling practical.

### 6.2.2 System B

A camera memory design using the Westinghouse MNOS BORAM 6001 device is briefly reviewed below. A description of this memory chip is presented in Appendix D, along with an explanation of its mode of operation and a discussion of the memory building block a 131,072 bit hybrid circuit. The organization, operation, and physical structure of the memory module are presented here.

The MNOS camera memory can be configured to correspond with the interface requirements stated in paragraph 2.3. Figure 6-5 shows the functional organization. The manner of operation of the data latch, adder, and storage section is as follows. Incoming data is latched and added to data coming from the storage. The resultant sum is returned to storage. Figure 6-6 shows one way of realizing this function. This particular configuration should operate properly within the 100 ns requirement of System B. The  $7\frac{1}{2}$  chips required dissipate a total of 647 mW.

The timing cycle and operating sequence of the storage section are the aspects of the design which are unique to MNOS BORAM implementation. All timing intervals are of course derived from the scan rate of the external sensor. Information in the BORAM shift registers must be made available to the adder at the specified 10 MHz rate. Every 100 ns a new 16 bit word must enter the adder.

The elementary segment for the MNOS memory will be two words wide; viz., 32 bits. This means that 32 different chips located in 8 different microcircuits will be powered up to process data. The chip data rate will be 5 MHz, and the shift rate will be 2.5 MHz. The time to process 128 data

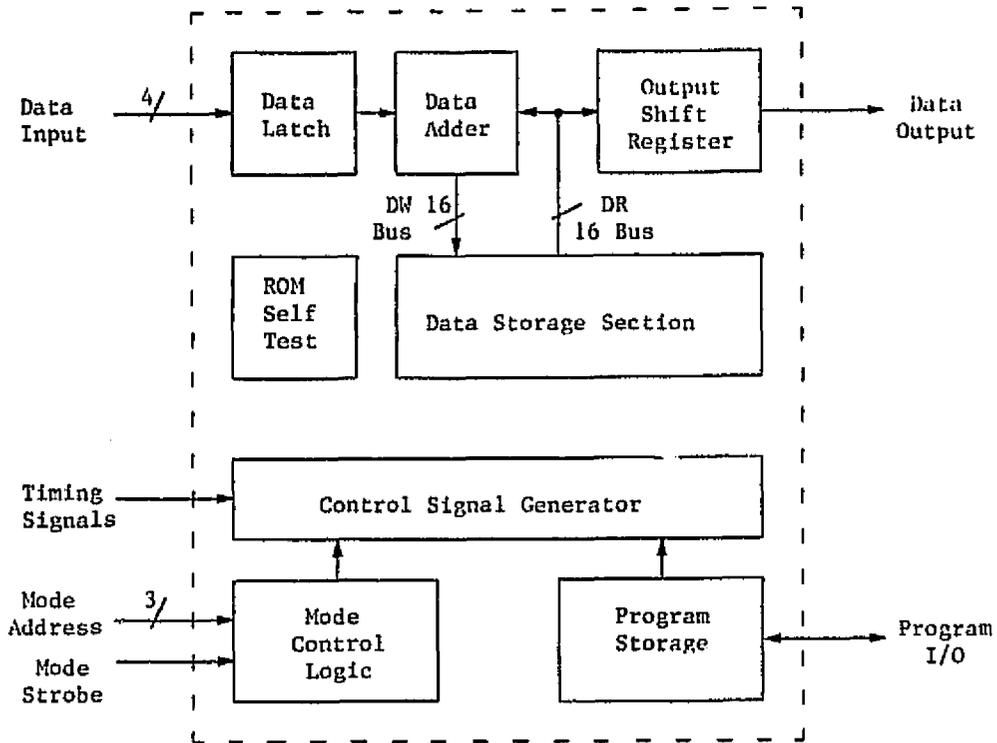


Figure 6-5. Functional Block Diagram for MNOS Camera Memory

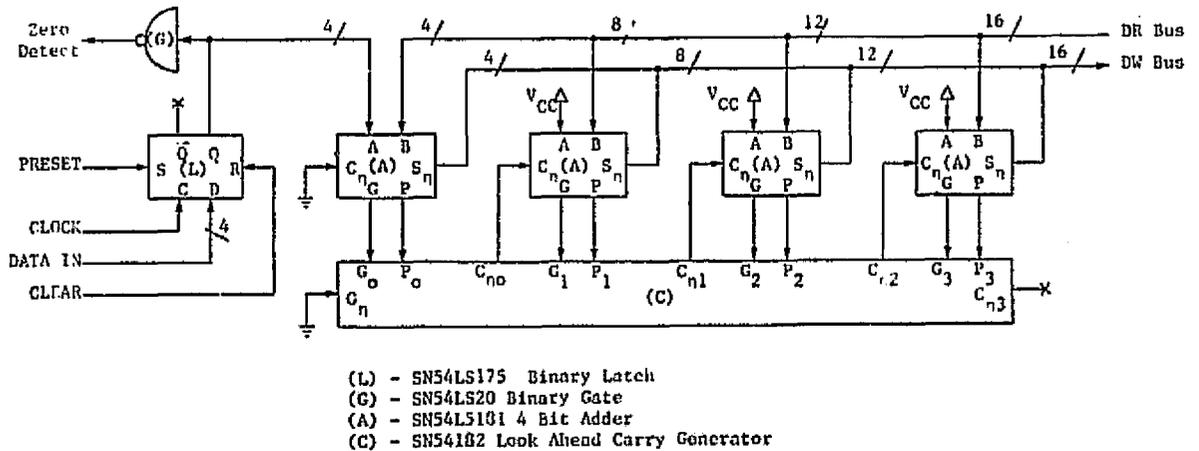


Figure 6-6. Data Latch and Adder Circuitry

bits at the chip level is 25.6 microseconds. To maintain a steady data flow two segments will operate in an overlapped manner in a  $2 \times 25.6 = 51.2$  microsecond cycle as shown in Figure 6-7. The MNOS chips go through three modes of operation within a read-modify-write cycle: read, shift and clear, and write. While one segment is shifting data, the other segment will be writing and clearing.

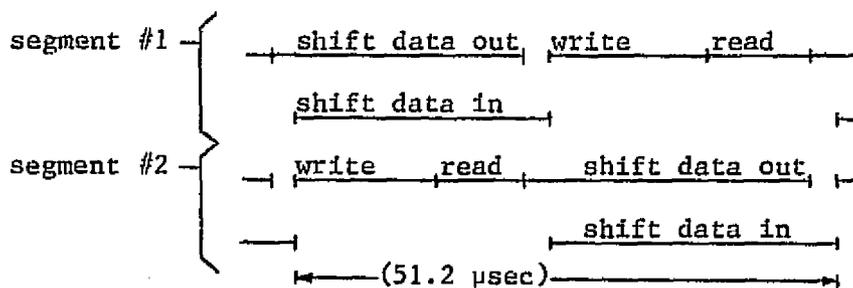


Figure 6-7. MNOS Camera Memory Timing Sequence

Physically the memory can be made quite compact. Eight microcircuits containing 16 chips each, plus all supporting drivers and buffers can be comfortably placed on a multilayer card 6.75" x 7.00". Four such cards will be required to hold the memory components. Two additional cards should be adequate to complete the camera memory. With allowance for back-plane wiring and cable connectors, the entire unit can be packaged in 8" x 3.5" x 7.5". This is 3.44 liters (210 cubic inches). The mass should be less than 2750 grams (6.05 pounds). This configuration is well within System B requirements of 16 liters and 5000 grams. In terms of density parameters the MNOS memory provides better than  $1200 \text{ bits/cm}^3$  and 1500 bits/gram.

If the system were expanded to 10,485,760 bits by using 10 memory cards, the dimensions would become 8" x 6.5" x 7.5". This is 6.39 liters (390 cubic inches). The mass would be less than 5,112 grams. In terms of density parameters this is  $1640 \text{ bits/cm}^3$  ( $26,900 \text{ bits/in}^3$ ) and 2050 bits/gram

(58,100 bits/oz). Thus the MNOS configuration appears to be compatible with the original LST camera memory volume and mass goals.

Power dissipation estimated for the storage section while operating at a 10 MHz scan rate is about 10.7 Watts. The total power for the memory should be less than 15 Watts. This assumes that the control section will be implemented using a mix of low power TTL and CMOS devices. The self-test circuits and the output shift register will be powered down. Although the MNOS configuration does not meet the System B average power goal of 10 Watts, it is well within the peak power objective of 50 Watts. If the scan rate is reduced the dissipation will reduce. If the memory is expanded to 10,485,760 bits, the power dissipation does not change significantly. Dissipation is a function of the segment width rather than of memory capacity. Table 6-2 summarizes the complete list of characteristics projected for the MNOS BORAM implementation of System B.

Table 6-2. MNOS BORAM SYSTEM B CHARACTERISTICS

Characteristic	MNOS System B Value
Capacity	262,144 words
Word Size	16 bits/word
Data Rate	$10^7$ words/sec
Error Rate	$10^{-13}$ errors/data bit
Average Power	15 Watts
Peak Power	15 Watts
Operating Temperature	$-10^{\circ}\text{C}$ to $+40^{\circ}\text{C}$
Volume	3.44 liters (210 cubic inches)
Mass	2.75 Kg (6 pounds)
Reliability	>0.95 for 90% words operating over 1 year mission times
Availability	1978 breadboard system 1980 flight qualified system

### 6.3 Procurement Estimates

Estimates of the program duration and total cost to develop the breadboard and subsequent prototype and flight memory units for both System A and System B are shown in Table 6-3. The costs are total or sell costs to NASA, and have a burden typical of a CPFF contract plus an assumed 10 percent fee. Labor costs included in these totals are based on projected engineering and support rates for the years 1976 through 1980. Material costs have a handling burden and normal attrition factors included.

Table 6-3. ESTIMATED MEMORY SYSTEM COSTS AND PROGRAM DURATIONS

SYSTEM A	BREADBOARD	PROTOTYPE	FLIGHT
Period Program Duration - Months	1976 12	1977-78 15	1978-79 12
Costs			
Labor	\$122,931	257,961	231,720
Memory Devices	\$ 3,315	7,042	7,000
Support Material	\$ 2,035	13,074	13,000
Direct Cost	\$128,281	278,077	251,720
Sell Cost	\$159,806	346,414	31,358
SYSTEM B	BREADBOARD	PROTOTYPE	FLIGHT
Period Program Duration - Months	1978 12	1979-80 15	1980-81 12
Costs			
Labor	\$276,725	441,014	374,759
Memory Devices	\$ 19,634	22,400	22,400
Support Material	\$ 2,568	19,400	19,400
Direct Cost	\$296,908	469,729	409,856
Sell Cost	\$369,873	585,165	510,578

OB

Estimates for both breadboard systems are based on providing units that would meet the electrical interface and performance requirements but would be unrestricted with respect to physical characteristics such as size, shape, and weight. The units must tolerate normal laboratory handling and usage. Component costs were based on prices quoted for standard parts suitable for military applications. These parts are capable of being purchased to flight quality specifications on subsequent buys.

The prototype and flight model costs are based on an estimated total effort to design, test, and qualify units for delivery that would meet all of the physical and electrical performance requirements of a flight qualified system. A significant decrease in the cost estimates occurs for the flight model memories compared to the prototype units, even though an increase in labor rates of about 11 percent per year are projected and factored in. This reduction in system cost results from an estimated drop in the overall engineering hours required, as the major design effort will be completed with the prototype units.

The total costs of both systems have been broken down to reflect the portion of the direct costs that can be attributed to memory device costs, supporting material costs, and direct labor costs. Assumptions made to arrive at these total costs are as follows:

- All interface inputs and requirements of the LST Camera are known or resolved at the start of the program.
- All material required is readily available.
- The 4K RAM memory device costs of \$22 for standard units and \$34 for qualified units used in the System A estimates are based on inputs from K. Blair, Motorola MOS Product Manager.

- The 4K MNOS BORAM memory device costs of \$28.68 for breadboard units and \$32.78 for prototype model units used in the System B estimates are based on projections from recent production runs at Westinghouse.

The direct labor costs are based on the estimated total manhours required at the projected labor rates for the periods indicated. All component costs shown have factors for attrition and a material handling burden included. Supporting material costs also include costs of material required for test purposes such as test fixtures for production and qualification, and for memory devices for qualification tests at the printed circuit board assembly level.

The final cost item included but not called out explicitly in Table 6-3 is a memory controller. Such a controller must be provided as a deliverable item to facilitate exercising the delivered memory units. It will control operating modes as directed and check the ability of the memory to store and return words. Cost of a complete simulator to fully exercise the memory was not required by the study. Accordingly, the price tag for any given exercisor will depend to a large extent on what facilities can be made available by NASA in the time frame of interest. As a guideline it is estimated that a bare bones exercisor to provide a full system test capability would cost approximately \$50,000.

## Appendix A

### Developmental Breadboard Specification

The specification enclosed herein has been generated to facilitate procurement of a breadboard sensor instrument memory fitting the data storage requirements of the cameras on LST-1. This specification provides procurement guidelines on the following items:

- System Requirements
- Physical Characteristics
- Design and Construction
- Documentation
- Quality Assurance
- Delivery

TYPE B2, CRITICAL ITEM DEVELOPMENT SPECIFICATION

for

SENSOR INSTRUMENT MEMORY MODULE BREADBOARD

1. SCOPE

1.1 Scope. This specification establishes the performance, design, development, and test requirements for a sensor instrument memory module breadboard critical item.

2. APPLICABLE DOCUMENTS

2.1 Government documents. The following documents of the exact issue shown form part of this specification to the extent specified herein. In the event of conflict between the documents referenced herein and the contents of this specification, the contents of this specification shall be considered a superseding requirement.

SPECIFICATIONS:

(To be supplied by NASA)

STANDARDS:

(To be supplied by NASA)

DRAWINGS:

(To be supplied by NASA)

OTHER PUBLICATIONS:

(To be supplied by NASA)

### 3. REQUIREMENTS

3.1 Definition. A solid state digital storage unit suitable for use on a spacecraft as part of a sensor instrument package is to be designed and breadboarded. The memory shall operate in conjunction with one or more limited internal storage time detectors, such as ICCD or SIT cameras, under the direction of an external controller or computer, and shall have hardware boundaries established in accordance with Figure 1. The design analysis shall show that performance, reliability, and physical packaging objectives for a spaceflight qualified unit can be achieved. The breadboard sensor instrument memory (SIM) module shall be a deliverable item suitable for use by NASA in a normal laboratory environment. The breadboard shall meet all electrical performance objectives. Breadboard packaging and components may be of commercial quality, and no special form factor is required. The preferred memory component is an N-MOS 4096 bit RAM device.

The SIM module is to provide two storage sections of 16,000 words each. A word contains 16 data bits. All electrical connections to the module shall be through two cable connectors. A power connector shall provide dc voltages. A signal connector shall allow for the data and control signals defined in Figure 2. The cable format, interface signal levels, and timing restrictions are to be mutually defined with NASA during the design effort.

The contractor is to construct a simplified controller circuit which will allow operation of the breadboard at the maximum specified data rates. The controller is to generate the appropriate external signals to allow verification of all operating modes. The controller is to be a delivery item.

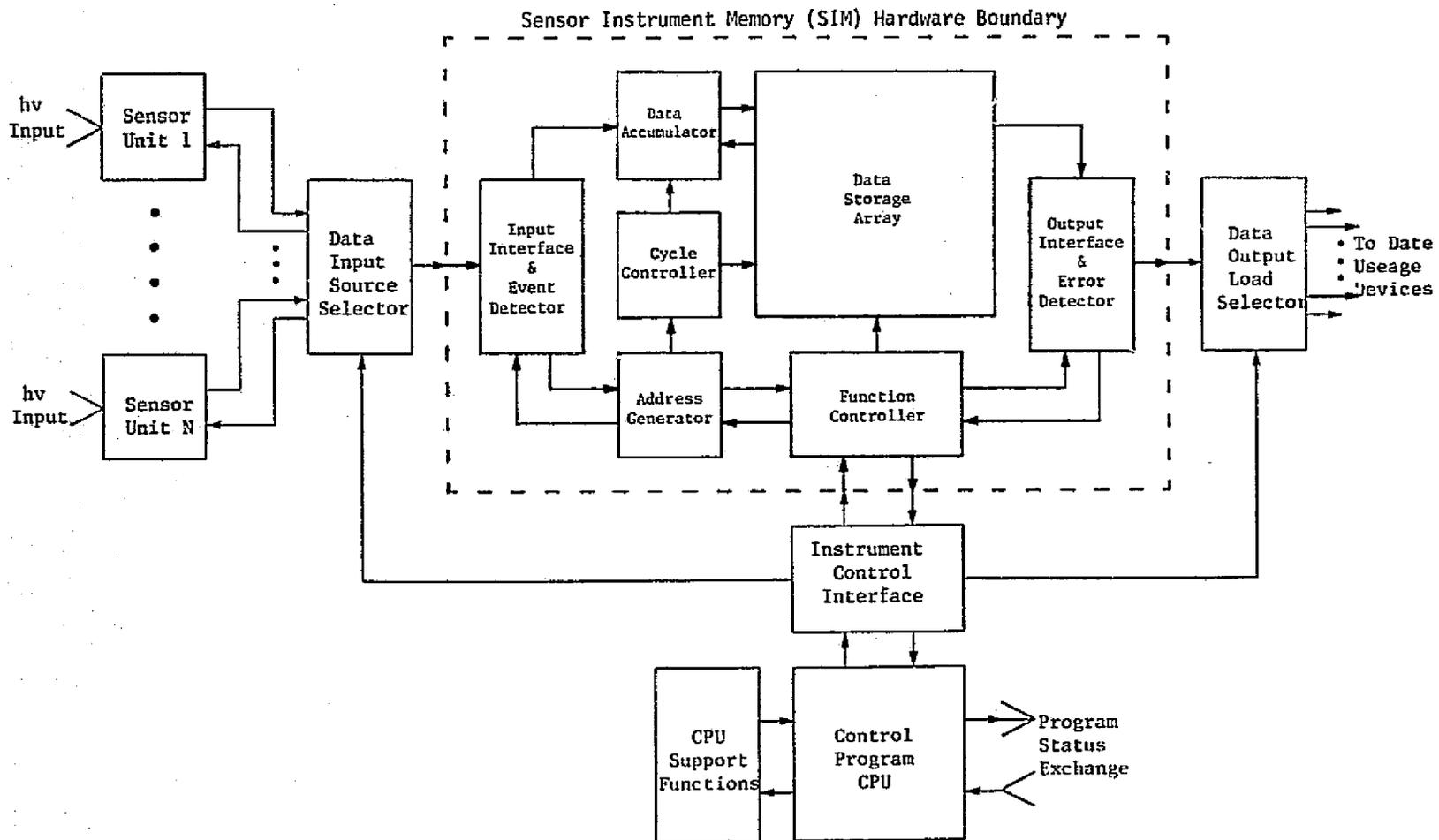
The memory shall be capable of operating in the eight modes specified in Table 1. A mode command shall be entered via the three MODE INPUT lines on a transition edge of the MODE STROBE signal. The mode commands shall be asynchronous and shall override all other inputs.

In the POWER DOWN mode all voltage stresses are to be removed from operating components. Only the necessary power switching circuits are to remain active. Memory contents or memory program information need not be retained.

During ACTIVE STANDBY memory contents and memory program information must be retained. All other circuitry nonessential to the retention function, except for the necessary power switching, is to be powered down.

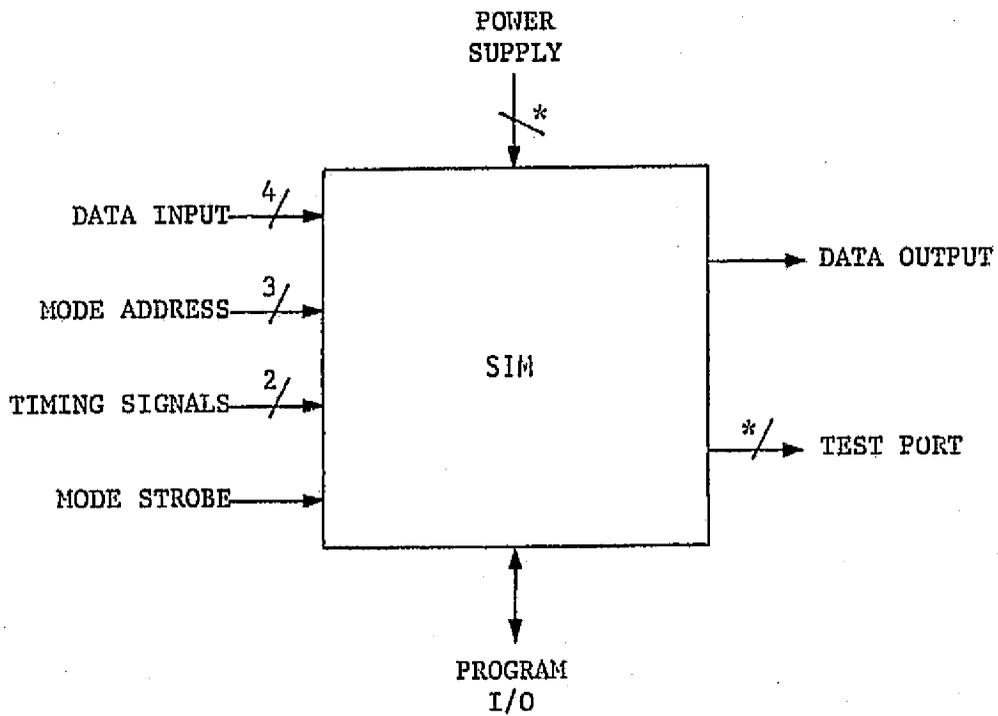
The INITIALIZE mode establishes the proper starting conditions for the memory control circuitry and address counters. If a designated control bit in the program word is set, the INITIALIZE mode will also clear the entire memory to zero.

The SIM design format is intended to be sufficiently flexible to allow its use with different sensor arrays. The memory is able to accept a "program word" which will electronically modify the memory operation to match the needs of specific sensors. Array size is an



A-5

Figure 1. Spacecraft Sensor Instrument Package Subsystem



\* To be defined during breadboard development

Figure 2. Sensor Instrument Memory Electrical Interface

Table 1. SIM FUNCTIONAL MODE REQUIREMENTS

Mode Number	Mode Name	Mode Description
0	POWER DOWN	Power down all electronics except the mode circuitry and related power switches.
1	ACTIVE STANDBY	Activate control, programming, and data storage circuitry.
2	INITIALIZE	Initialize all count and control circuitry; and clear memory to zero if control bit in program word is set.
3	ENTER PROGRAM	Enable memory to receive a serial program word on the program I/O line as clocked in by the timing signals.
4	VERIFY PROGRAM	Enable memory to transmit the currently stored program word on the program I/O line as clocked out by the timing signals.
5	SCAN	Enable memory write operation. Increment address in response to timing signals. If input data is nonzero add data to present contents of memory. Recycle addressing as specified by program word.
6	OUTPUT	Enable memory read operation. Beginning at program word specified initial place data serially on the data output line as clocked out by the timing signals.
7	TEST	Enable ROM controlled self-test routine. Test sequence proceeds in response to the timing signal. Test results appear on data out line and/or optional test port line(s).

example of an attribute which may vary. The memory provides one 16 bit data word for each pixel in a dual 100 x 160 array. Array scanning is sequential in some uniform pattern. The memory keeps track of addresses by counting master timing clock pulses while in the SCAN mode. The address count is reset to zero when a maximum address specified in the program word is reached. (The address count may also be set to zero by pulsing the secondary timing synchronization line).

Other features such as special timing or count sequencing information may also be incorporated in the program word. The specific length and content of the program word are to be defined during the design effort in cooperation with NASA.

To insert a program word into the memory the ENTER PROGRAM mode is established. Given this action the PROGRAM I/O line will be enabled to accept the program word in a bit serial format as clocked in by the timing signals.

The VERIFY PROGRAM mode allows the stored program word to be transmitted in a bit serial format back out on the PROGRAM I/O line, again under control of the timing signals.

Memory operation in conjunction with a sensor takes place in the SCAN mode. Address incrementation occurs in response to the timing signal. Data from the sensor and associated detection electronics are presented to the memory as word serial/bit parallel four bit binary words. If the data is nonzero, the memory must read the 16 bit word at the current address count, add the 4 bit word to the 16 bit word, and store the resultant sum at the same address.

The timing information necessary to control the SCAN mode is derived from the timing signals. The timing signals are comprised of a master clock pulse train of some frequency higher than the pixel rate and a supplemental synchronization input to be used as necessary to coordinate operations between the sensor and the memory. It is visualized that the external timing signals drive a count down chain inside the SIM. Internal waveforms derived from these counters generate all the control signals necessary for operation of the memory in synchronism with the sensor scan.

Frequency and waveform restrictions for the timing signals are to be defined during the design effort. If it can be shown to be advantageous, additional external timing signals may be specified by the designer.

In the OUTPUT mode the SIM is to provide a word serial/bit serial output of the storage contents on the DATA GNT line. The data is clocked out by an internal signal derived by counting down the external timing signals. It may be advantageous to output the internal clock signal along with the data to communicate when the data is valid. This point should be resolved with NASA during the design effort.

The SIM must be capable of verifying the operational status of its functional parts. An on-board processor will be available during a space flight to perform diagnostics. The memory must be equipped with a ROM self-test program that can be monitored and directed by the processor. The memory designer is to identify which functional areas of the memory should be tested, and is to develop an appropriate test sequence. The sequence is to be initiated by placing the memory in the TEST mode. The test will be advanced in response to the timing signals. Results may appear on the DATA OUT line or at the optional TEST PORT. The program word may be used to supplement specification of a test subroutine.

The intent of this functional description is to ensure that the SIM has sufficient flexibility to be used with different types of sensors. The designer is not restricted as to how the internal structure of the memory is to be implemented provided all design goals are met.

3.2 Characteristics. The performance, physical characteristics, and reliability requirement for a space qualified version of the sensor instrument memory are stated in Table 2. The design analysis is to demonstrate that these objectives can be met. The SIM breadboard is to comply with table 2 to the extent specified below.

3.2.1 Performance. The SIM breadboard is to provide storage for 32,000 words of 16 bits. The module is to be partitioned into two sections sufficiently independent to comply with the reliability objectives of Table 2. The module shall accept data at rates up to  $3 \times 10^6$  words/sec where the input words contain 4 parallel bits. The output data rate is to be defined during the design task with NASA approval.

The error rate objective is to be better than  $10^{-11}$  errors per data bit processed. It is not intended that this parameter be measured, and it should not be confused with component failure. NASA's intent is that the design analysis should examine the signal-to-noise ratios at critical points within the system to ensure that degradation below this objective does not occur.

The SIM breadboard should comply with the power dissipation objectives of Table 2. Power in some memory organizations will be a function of the incoming nonzero data rate. Power is specified at specific data rates, and is to be averaged over one frame time. A frame time is defined as the time required to cycle entirely through the memory from address zero to the maximum address and jump return to address zero.

Waveform risetimes, pulse widths, voltage amplitudes, and timing restrictions on all data and control signals are to be established during the design. Power sources will be the responsibility of NASA. The required voltages, polarities, current levels, and regulation requirements are to be established during the design.

3.2.2 Physical Characteristics. The SIM breadboard is to be used in a laboratory environment. It should be sufficiently rugged to allow normal handling, and should be arranged to allow convenient access to parts for test and/or repair. The unit should be suitable for resting on a workbench. No form factor or dimensional limitations are imposed.

Table 2. SENSOR INSTRUMENT MEMORY CHARACTERISTICS

Characteristic	Specification
Storage Capacity	2 sections of 16,000 words
Word Size	16 data bits/word
Data Rate	$3 \times 10^6$ words/sec
Error Rate	$10^{-11}$ errors/data bit
Standby Power	10 Watts @ 0 Hz data rate
Average Power	10 Watts @ 300 KHz data rate
Peak Power	30 Watts @ 3 MHz data rate
Operating Temperature	-10°C to +40°C
Storage Temperature	-55°C to +70°C
Volume	16 liters
Mass	3 Kg
Reliability	95% probability of success
Mission Time	1 year @ 35% duty cycle
Failure Definition	1 section must be functional

3.3 Design and Construction. Cost should be the primary consideration in selection of hardware and components for the breadboard. Commercial parts and practices are acceptable. All electronic components must, however, be identified as being capable of being qualified for space flight. The organization of the hardware should reflect basic safety considerations, and should consider how the equipment will be used in the laboratory.

3.4 Documentation. The contractor shall provide a functional description of the SIM breadboard with a clear statement of all operating sequences and interface requirements. An overall logic diagram shall be provided which shows the internal partitioning of functions to circuit boards and interconnection wiring. Each circuit board shall have documentation which identifies all components and specifies pin connections. Computer wiring lists are acceptable. A complete parts list with vendor identification is required. The contractor shall provide a description of the self-test capability of the module which identifies all test points and describes the test sequence.

3.5 Logistics. Not applicable.

3.6 Precedence. In the design of the sensor instrument memory module certain trade-off situations will be found to exist. Data rate requirements and reliability objectives must be achieved. Low cost is a major objective. If cost can be reduced at the expense of power, volume, or mass, NASA will consider such alternatives.

#### 4. QUALITY ASSURANCE PROVISIONS

4.1 General. Before delivery of the breadboard the contractor shall demonstrate to NASA personnel that the unit does operate properly at the required data rate and power levels.

4.1.1 Responsibility for Tests. The contractor is responsible for establishing a working demonstration of the breadboard being driven by the simplified controller. Measurements using external test equipment should confirm that performance goals have been achieved.

#### 5. PREPARATION FOR DELIVERY

5.1 Packaging. The data and equipment delivery items shall be packaged for shipment as specified in the contract.

Appendix B

Program Statement of Work

The SOW (statement of work) contained herein is included for the sake of completeness. It sets forth the original directives prescribed by NASA for the Camera Memory Study for LST program which led to this report.

1.0 SCOPE

The purpose of this study is to survey memory technologies capable of being developed and configured in such a manner that they can operate as data storage media for such detectors having limited internal storage time as the Charge Coupled Device (CCD) and Silicon Intensified Target (SIT) type cameras during space missions. The results of the study will be in the form of a report stating general characteristics of different techniques, showing detailed comparisons of technologies, and describing in detail why other techniques reviewed were not recommended. The information obtained from this study will be used as a guide for establishing specifications for a spacecraft memory to be used as part of a camera system having an associated data processor unit. The duration of this study shall be 6 months.

2.0 GENERAL

The intent of this study is to be able to define a data storage technology potentially capable of storing data from an imaging device (e.g., Charge Coupled Device (CCD) or from a Silicon Intensified Target (SIT) tube). The storage medium specified shall be capable of being addressable by a data processing unit which forms part of the camera design. The time frame of interest is for breadboard units for test and evaluation of 1976, and a flight unit for 1980.

3.0 APPROACH

The approach adopted shall involve an extensive literature survey, making visits to key personnel in many companies and incorporating information made available by NASA. These data shall be analyzed and trade-off studies shall be conducted to define qualitatively those techniques best suited to work as an integral part of the imaging system. Some flexibility needs to be included in the study as the data requirements, image tube development, and the overall camera system concept are more fully defined. Care must be taken to consider the impact of the technologies on system and subsystem design and to assess the performance advantages to be gained versus the cost of the different systems. The recommended memory approach is to have a breadboard memory of conceptual design expressing 1976 state-of-the-art, not necessarily present day state-of-the-art.

4.0 MEMORY INTERFACE

4.1 Sensor

The memory unit shall operate with an input signal originating from the following types of imaging sensors.

4.1.1 Solid state charge coupled device (CCD or ICCD). The ICCD refers to a developmental device incorporating a CCD operating in an Electron Bombardment Induced Conductivity mode.

4.1.2 SIT Tube

4.1.3 Others, including photomultipliers, diode arrays, infrared bolometers, far-uv linear array detectors, (e.g.; chevron plates plus resistive strips for read-out).

4.2 Processor

The memory unit shall be able to work with either a special processor which can do arithmetic manipulation of data or with a General Purpose Computer. The memory unit will be addressed in some relation to the detector scan format. Both continuous serial readout and co-addition of consecutive frames are possible operational modes.

5.0 MEMORY GUIDELINES

5.1 Physical (Size/Weight)

$1.6 \times 10^4 \text{ CM}^3/5\text{Kg.}$

5.2 Capacity

At least  $10^7$  bits.

5.3 Access

Serial access is anticipated. Parallel access to memory sub-sections via a high speed buffer interface is also permitted.

5.4 Power

Of the order of 10 watts, up to 50 watts during data burst modes.

5.5 Data Rate

$10^7$  bits/second anticipated.

5.6 Reliability

2 years minimum.

5.7 Environmental

Memory shall survive shuttle launch and return and low earth orbit environments.

6.0 STUDY REQUIREMENT

As a minimum this study shall:

- 6.1 Survey memory devices capable of operating with imaging devices. Estimate development schedule and cost for each memory system.
- 6.2 Analyze operations of memory with image device and data processor unit.
- 6.3 Develop specifications for a recommended design of a memory system which operates with an imaging tube and data processor, which will enable a breadboard unit to be developed by 1976, and a flight unit by 1980.
- 6.4 Analysis priority shall be as follows:
  - (1) Cost
  - (2) Reliability
  - (3) Power
  - (4) Physical (size/weight)

7.0 DOCUMENTATION RESULTS

- 7.1 Monthly Letter Progress Reports shall be prepared and delivered to NASA. Ten (10) copies shall be provided.
- 7.2 Final Reports describing the work done, results obtained and recommendations shall be prepared and delivered to NASA one month after completion of all tasks. Ten (10) copies shall be provided.

## Appendix C

### Unsuitable Memory Technologies

The information presented herein consists of a series of concise reviews of memory technologies which are found to be unsuitable for use as the data storage media for cameras deployed on space missions. Its purpose is to comment on the reasons for rejecting these technologies.

## MEMORY TECHNOLOGIES REJECTED FOR THE LST APPLICATION

During various stages of the memory technology survey, decisions are made that specific technologies are not suitable for use in the camera memory application. It is to be emphasized that this study is focused on one application. Rejection of a technology has no implications as to its utility in other applications, or in other timeframes. Screening decisions are based on the original study criteria of table 2.1. The more definitive, individual specifications for systems A & B did not exist at the time the preliminary technology screening was performed. No doubt some of the rejected technologies might be capable of meeting system A requirements. This should not be a major issue, however, since the technology decisions are ultimately focused on the long term needs of spacecraft memories.

### DRUM

Magnetic drums with read/write heads located on prepositioned single tracks are used in ground based systems as secondary storage units. Access times on the order of 8 milliseconds to records containing on the order of  $10^7$  bits are provided. The electro-mechanical nature of this storage precludes its consideration for the LST mission.

### DISC

Moving head magnetic disc systems are used as the major on-line secondary storage for ground based computer systems. The need to position the read/write head leads to access times on the order of 250 milliseconds. The electro-mechanical nature of the system and its obvious timing problems eliminates this technology from further consideration.

## TAPE

Space qualified magnetic tape recorders have been developed. These units are expensive and have proven to be a reliability problem. Serial data organization and low data rates make camera memory application unlikely. The tape recorder should be reserved for large ( $\sim 10^9$  bit) storage applications which can tolerate low data and reliability. The electromechanical nature of recorders eliminates them from serious consideration.

## CORE

Ferrite core has long been the standard means of implementing computer main memory. Only recently has it been seriously challenged on a cost basis by the semiconductor technologies. One of the primary difficulties with the core technology is that its bit packing density parameters are insufficient to permit a core memory to meet the camera memory volume, mass, and power objectives. Furthermore, cost would be higher than with semiconductor alternatives and the reliability goals would be very difficult to meet.

## WIRE.

Plated wire is a relatively mature technology with potential cost advantages over core. Because of early problems, the production volume necessary to achieve low cost never materialized. It has been used primarily in military and aerospace applications. Compared to core, plated wire offers speed, power reduction, NDRO (nondestructive readout), and radiation resistance. Plated 5 mil wire can not be considered a serious contender for the camera memory application because of its high cost and poor volume and mass densities. The major development in plated wire

technology is the miniwire. This small 2.5 mil diameter wire reduces bit drive current requirements and facilitates increasing bit densities within a plane and decreasing interplane spacings.

Univac is active in the development of 2.5 mil wire systems and has produced and delivered to RADC one  $10^7$  bit memory. The design was oriented toward MIL-E-5400 and MIL-E-16400. If these units go into volume production, the price could be 2¢/bit. Nonrecurring costs associated with flight qualification would, of course, increase the price. During the course of the technology survey, Robert White, the project engineer for this product, was interviewed at Univac Park in St. Paul, Minnesota. Mr. White described the nature of the technology, proposed a specific configuration for the camera memory applications, and provided a brief summary of the characteristics of a plated wire type of camera memory (reproduced below). Very impressive density numbers result from this data.

#### CAMERA MEMORY CHARACTERISTICS

Capacity	- 262 Kwords
Word Length	- 16 bits + parity
Data Rate	- $5 \times 10^6$ words/second
Latency	- 1-10 microseconds
Power	- 25 Watts average
Volume	- 400 cubic inches (6.6 liters)
Mass	- 25 pounds (11.4 kilograms)
Organization	- random access or sequential in Four word blocks
Environmental	- MIL-E-5400, MIL-E-16400
Temperature	- $0^{\circ}\text{C}$ to $50^{\circ}\text{C}$ operating $-55^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ standby

Prior to the interview, Mr. White had received a brief summary of the camera memory requirements as they were understood at that time. (This was prior to firming up the system A and B specifications). Some aspects

of the requirements were incompletely communicated, and as a result his proposed configuration does not match the need. The discrepancy is related to the data rate and the power estimate. The proposed memory has an 800 nanosecond read cycle and requires 1600 nanosecond for a read/modify/write cycle. Mr. White interpreted the 5 MHz word rate as implying only a read or write. Thus a 128 bit word is required instead of the proposed 64 bit word. This adversely affects the power. If the data rate requirement is increased to 10 MHz as in System B, the power rises still higher.

White made a rough prediction of the system failure rate. He compiled a parts list and added up the component failure rates. The non-redundant total failure rate was 25,830 fits. He could offer no comments on how much improvement might be achieved by redundancy. At a later date the data provided by Univac was evaluated. It is clear that this class of memory is a significant improvement in the plated wire art. In the context of the camera memory requirements, several difficulties exist. In particular, the mass density, power density, and cost do not meet objectives. From the existing data it is not possible to draw a definite conclusion as to whether the System B reliability could be met.

#### CFM

From time-to-time, various developments have been undertaken to realize a planar format for the plated wire type of memory. These magnetic film approaches store and retrieve information by domain rotation in an anisotropic media as in plated wire. They differ from plated wire in fabrication processes and equipment requirements. The motivation for planar film approaches is potential cost and size savings.

Generally the planar film developments have encountered serious problems in reduction to practice. Many different firms have embraced particular schemes, and have performed exploratory R&D. Phillips, IBM, Laboratory for Electronics, and others have reported some work. Closed flux memory (CFM) is the name given to the planar approach now being pursued by the Ampex Corporation under U.S. Navy funding. To establish the status of the effort, Dr. Malcolm Barlow of the Ampex Advanced Technology Division in Redwood City, California was contacted by telephone. Dr. Barlow is the project manager responsible for setting up a closed flux array pilot production line.

As Dr. Barlow described it, CFM production begins with an aluminum substrate covered by an insulating kapton film. The array is formed by plating layers of magnetic film and copper, and by photomasking and etching. At least 5 layers are involved. He has produced some arrays which contain defects. In his opinion a year or two years of further work will be required to debug and mature the fabrication process.

The item currently being produced by Ampex is a  $274 \times 274$  array at a density of  $5000 \text{ bits/in}^2$ . All of the bit positions are not useful in terms of being communicated to the external computer system. The plane provides 2048 words of 36 bits, or 73,728 useful bits. Dr. Barlow indicated that an early estimate made at Ampex was that 2 planes with drive and sense electronics could be packaged in a  $4" \times 4" \times 1/3"$  volume. This is  $1687 \text{ bits/cm}^3$  and about  $1000 \text{ bits/gram}$ . Dr. Barlow expects to improve the plane bit density to  $10,000 \text{ bits/in}^2$  eventually. The planar lines near an aluminum substrate form low impedance ( $\approx 40\Omega$ ) transmission lines. Drive currents at 40 mA to 60 mA are required. Write cycle times of 150 nanoseconds and read cycle times of 100 nanoseconds appear practical.

The 2 plane 4096 word module is expected to dissipate 10 Watts. This is  $6.78 \times 10^{-5}$  Watts per bit.

CFM does not seem to be practical for the camera memory application from both the time frame and the probable economic viability of the effort. Dr. Barlow's estimate of one-to-two years to mature the fabrication sequence is probably optimistic; but more important, it is only part of job of preparing working memory systems. Additional time will be necessary to define the packaging and electrical design of systems. Then time will be required to prove reliability. The economic viability of the effort has to be questioned on the basis of competition from nonvolatile MNOS RAM developments. If the feasibility studies now being performed for the MX version of the Minuteman missile show positive results, the motivation for CFM development would be greatly reduced. Since NASA does not want to undertake component development it would be an unwarranted risk to embrace CFM.

#### OFM

The oligatonic film memory (OFM) technology has been under development at Univac for several years. This approach to bulk storage is another planar equivalent to plated wire. The media is a very thin ( $\approx 100\text{\AA}$ ) anisotropic film. Oligatonic memories were included in this study on the strength of very impressive density numbers and vocal claims of maturity.

To verify the status of the technology, Mr. Ernest J. Torok, the Univac Oligatonic project engineer in St. Paul, was interviewed on the telephone. Mr. Torok gave the following parameters for a proposed system including power supplies:

Capacity -  $1.5 \times 10^7$  bits  
Volume - 1.3 cubic feet (3.68 liters)  
Power - 100 Watts  
Cost - 0.5¢/bit (in production)

In response to the RPI camera memory requirement, Mr. Torok said that the Oligatonic film approach would have difficulty meeting the 10 Watt average power and the 5000 gram objectives. He feels that the fundamental problems of the OFM technology have, however, been resolved. A partially populated system containing 8000 working bits was delivered to NASA Huntsville several years back. The purpose of that system was to demonstrate the feasibility of all elements of a memory system. Since that time, work has continued under Univac IR&D sponsorship.

From Mr. Torok's comments it was concluded that the oligatonic film approach lacks the necessary economic drivers and maturity required for the camera memory. A  $10^7$  bit OFM system would dissipate about 100 Watts - i.e., approximately the same as the  $1.5 \times 10^7$  Watts per bit. The volumetric density claimed is about 400 bits per  $\text{cm}^3$ . If one assumes a packaging density similar to plated wire, the mass density is probably about 200 bits/gram. These numbers are much more pessimistic than those reported in the early 70's by other investigators. Mr. Torok made the point that the densities for small memories are dominated by the peripheral circuit overhead. Previous OFM estimates used a  $10^9$  memory as the basis for computing densities, so that may account for the difference.

#### CROSSTIE

The crosstie memory development is still primarily concerned with definition of the phenomena and materials characteristics important

to memory operation. It will not be available in a timeframe compatible with the camera memory.

Crosstie is based on the motion of magnetic walls in thin films of magnetic materials. L. J. Schwee, et.al., at NOL claim 20 MHz data rates at  $10^6$  bits/inch<sup>2</sup>. Optical readout is presently used. Projections of much higher speeds and bit densities have been made. A successful development could provide a high speed block oriented memory systems.

#### DYNABIT

Dynabit storage is a domain wall motion controlled shift register. It has been under development by Hughes, and at least at one time, was sponsored by ECOM. The maximum shift rate is about 250 KHz. Its cost has been estimated at 0.1-to-1.0 cent per bit. Volumetric and mass densities are about the same as ferrite core. This technology is not suitable for use as a camera memory because of the slow shift rate and poor densities. It does not appear to have adequate economic drivers or technological maturity.

#### DOT

Domain tip (DOT) has been under development by Cambridge Memories of Newton, Massachusetts. This approach involves storage of information in a moving pattern of magnetic domains. Domain motion is constrained to specific channels 1.5 mils wide. The channels are formed as regions of low coercivity in an otherwise high coercivity continuous film of magnetic material.

In many ways the technology shares the attributes of the magnetic bubble approach, but it has significantly less potential. Like bubbles, DOT involves no mechanical motion to access information. Shift register

structures controlled by a rotating field are employed. The designs preferred by Cambridge Memories use control conductor patterns crossing the channels to block the inchworm type motion of the domains. For practical reasons involving the field coil drive and signal to noise tradeoffs, the shift rate is limited to 60 KHz.

This latter point is critical for the camera memory application. In fact, some misleading information about DOT data rates has appeared in the literature. R. J. Spain, et.al. of Cambridge Memories described a  $2.5 \times 10^6$  bit memory which used a 60 KHz shift rate. By multiplexing, the memory was able to provide a 240 KHz rate for 18 bit words. The system dissipated 250 Watts at the maximum data rate, and it was said that power dissipation was nearly linear with data rate. This design used two planes which contained a total of 72 shift registers running at 60 KHz. To reach a 10 MHz data rate, about 80 planes would be required with all shift registers ( $36 \times 80 = 2880$ ) brought out in parallel. The power dissipation would be on the order of 10,000 Watts. In short, DOT is not practical for use where high speed and low power are required.

The demonstrated bit density level on a substrate is about 6000 bits/in<sup>2</sup>. Magnetic bubble devices are already over 1,000,000 bits/in<sup>2</sup>. Many companies are active in bubble development. Only Cambridge Memories is pursuing the DOT approach in the U.S. From the standpoint of NASA's requirement for clear economic drivers for the camera memory technology, DOT seems marginal. Its direct competition will be bubbles, and it shows little promise of meeting bubble performance or density.

## P-MOS

P-channel metal oxide semiconductor (P-MOS) memory technology is most expeditiously evaluated from the context of a comparison with N-channel MOS. P-MOS is the oldest and most mature MOS technology. It is, however, being replaced in RAM applications by N-MOS because of fundamental differences in transistor properties. N-MOS promises to have both cost and performance advantages over comparable P-MOS. For this reason, N-MOS is a more desirable alternative and P-MOS is eliminated from serious consideration.

## CMOS

Complementary metal oxide semiconductor (CMOS) technology makes use of both N-channel and P-channel transistors. As a result, it is a more complex technology than either P-MOS or N-MOS alone. Memory cells in CMOS devices use 8 transistors as compared to 1 to 3 in N-MOS and P-MOS designs. Low dc power is the major advantage of CMOS. CMOS is rejected for the camera memory application because of its inherently low bit density compared to alternate MOS technologies. At any given state of development, larger capacity chips will be available with standard MOS than with CMOS. The resultant reliability and cost impact for  $10^7$  bit systems is significant.

## SOS

Silicon-on-sapphire (SOS) technology does not constitute a stand-alone approach to memory device production. SOS processing is combined with a major device fabrication technique, such as CMOS or MNOS, to secure dielectric isolation (as opposed to junction isolation) of the individual active elements. Its major asset is very high radiation resistance and rapid recovery from high radiation exposure. The largest

memory chip presently available is a 1024 bit CMOS/SOS RAM. Use of SOS based memory chips is counter indicated for the camera memory due to low bit density, high cost per bit (resulting from low yield); and still evolving fabrication processes.

#### MNOS/CCD

Nonvolatile storage capabilities can be provided in charge coupled device memory structures by introducing nitride memory cells adjacent to the CCD register. This MNOS/CCD compounded technology exhibits the traits of both its forebearers, but is in an immature stage of development. It is, therefore, not considered to be a viable candidate at this time for the LST camera memory application.

#### I<sup>2</sup>L

Integrated-injection-logic (I<sup>2</sup>L) is a relatively new bipolar technology receiving a high level of interest throughout the industry. Its major attributes, compared to standard bipolar technology, are simpler processing requiring no epitaxial layer, the exclusion of isolation diffusions to provide higher bit packing densities, and a lower (and variable) speed-power product. A number of major semiconductor houses are heavily involved in investigating I<sup>2</sup>L devices, and at least one commercial product (a 4 bit microprocessor from TI) has been announced. No memory products have as yet been announced, however, and the technology is still too immature to be a serious contender for the camera memory application.

#### BIPOLAR

Bipolar integrated circuit technology has been used for some time to manufacture memories. When compared to MOS memories these devices

exhibit high speed, high power, low bit density, and high cost per bit. Recent advances in the technology show promise of improving density through the elimination of isolation walls and simplification of structures. It does not appear that these improvements will overcome the advantages of MOS within the LST timeframe (and more probably never). Bipolar memory should be used where its high performance offers system advantage. In the camera memory application, MOS performance is adequate, therefore the higher cost and power of bipolar is an unacceptable alternative.

### OVONIC

Amorphous semiconductor devices are inherently slow write memories. Present day circuits have limitations as to how many writing operations can be performed before device characteristics are altered. Because of the read-mostly nature of the technology and its high power dissipation, it is rejected for the camera memory application.

### MAS

Metal Alumina Semiconductor (MAS) devices store data by holding charge within the alumina film. Charge can readily be injected electronically, and a large shift in gate threshold results. It is difficult to remove the charge, however. As a result MAS devices have only been produced for use as read only memories.

The Nippon Electric Company has been marketing several MAS devices since the early 70's. The NEC America Inc. office in New York City will provide technical descriptions of the device structure. A paper by Nakanuma, et.al. (undated and with no indication of having been published) describes the NEC transistor structure. The devices are N-channel enhance-

ment mode. The gate structure consists of 1200-to-2500Å of aluminum oxide. The substrate is 3 cm P-type silicon. Trapped charge can be removed by X-ray radiation. The structure is too slow for use in the camera memory.

#### FAME

A ferroacoustic memory element (FAME) employs wire as a substrate for a magnetostrictive material. The General Dynamic FAME used beryllium copper wire plated with an isotropic magnetostrictive material. Several wires were bonded to a ceramic transducer. The transducer propagates strain pulses down the wire. In the local region of the strain, the switching threshold of the magnetostrictive material is altered. The wire is used to write or sense by a sequence of time coincident pulses.

Storage density is reported to be limited by demagnetizing effects. No more than 50 bits/inch of wire is expected. Large strain amplitudes are necessary, and rather complex transducer arrangements are used. One working model had 5 inch wires and a data rate of 8 MHz. The FAME approach features a high data rate, but in other respects doesn't appear attractive for the camera memory application. Volume and mass density are inadequate. Because of the large amount of connections, reliability is questionable.

#### SONISCAN

Magnetostrictive thin film deposited on glass or quartz can be used to store information. An acoustical wave is used to scan the surface of memory strips and modify local magnetic properties such that a coincident electric pulse can write in data. An acoustical wave also causes a temporary flux change in local regions which depends on the original state in those regions, and thus allows a nondestructive readout.

The design and fabrication of practical Soniscan systems seems to be a complex materials and processing problem. Some small prototypes have been built. Some efforts at defining a production process for memory planes has been carried out. Work was performed at Sylvania, and later at Microsonics. The U.S. Navy sponsored these efforts. Currently the Navy has discontinued the program because of the probable development costs associated with achieving a low cost production process.

#### SAW

Acoustic wave delay line type memories have been realized in three forms: the wire delay line, the bulk delay line, and the surface wave delay line (SAW). All are volatile and require that the data be continuously recirculated. Bit packing density is a direct function of bit processing rate dwell time. Power consumption is high, and the memories are heavy. Environmental resistance is questionable. This class of memory is not being actively pursued and seems wholly unsuited for  $10^7$  bit systems.

#### MENTOR

Ferroelectric memory technology is still rather immature. Material characteristics do not readily lend themselves to realization of the memory element. No defined switching level exists, hysteresis loss heating is severe, fatigue effects exist, and in some cases shelf life problems exist. In theory the memory element should store information by changing its state of polarization on application of an electric field. This could result in nonvolatile high density memory systems.

A small company, Technovation, is working toward realization of ferroelectric memory arrays. They call the memory device MENTOR, and report that prototypes have been produced. The ferroelectric material

is  $\text{KNO}_3$ . Cycle times on the order of 100 nanoseconds are possible. Techno-  
vation is seeking funding to continue the development. Other development  
efforts are underway in large companies. However, the general lack of  
maturity of these efforts precludes serious consideration for the camera  
memory application.

#### OBAM

The optical beam addressed memory (OBAM) category is very broad,  
and encompasses designs with widely different features. Generally all of  
these approaches offer the potential of extremely high bit storage densities.  
The major development trend seems to be on the use of laser beams for  
addressing. Typically four basic subsystems are involved: a light source,  
a storage medium, an access system, and an optical subsystem.

Optical memory subsystems are complex and are for the most  
part in an early development stage. This hardware is costly and can be  
economically justified only for large memories. A frequently mentioned  
objective is the terrabit ( $10^{13}$ ) memory system. The technology is simply  
not for a relatively small  $10^7$  bit camera memory.

#### EBAM

Electron beam addressed memory (EBAM) devices are of historical  
importance to the development of computer systems. Many variations of  
this type of storage have been used. Among the more important forms were  
the Williams tube, the barrier grid tube, the holding-gun tube, and the  
Selectron. Prior to the development of the magnetic core, probably the  
most widely used form of storage was the Williams tube. These early  
systems had a limited life time and suffered from many manufacturing  
problems.

Recently new interest has been shown in storage tubes. J. Kelly, et.al., at Stanford Research Institute have proposed an EBAM system based on tubes capable of storing  $4 \times 10^6$  bits. (The old Williams tube capacity was on the order of 1000 bits). The proposed SRI system would store 64 megabits in 16 tubes. Access time to a word would be 3 microseconds. Kelly claims bit densities of  $450 \text{ bits/cm}^3$ . Writing rate per tube would be 1 Mbit/sec, and the reading rate would be 10 Mbits/sec. The cost projection is 0.02¢/bit for a commercial system, and 0.07¢/bit for a military system. General Electric and Microbit Corporation are also doing work with this type of storage.

#### JEM

A number of magnetic and electric effects which could be used to construct memories have been observed in metals cooled to the superconductivity point. The principal draw back of these approaches is the cost and size of the refrigeration equipment. Temperatures below  $4^{\circ}\text{K}$  are required. The reliability and power penalty associated with cooling equipment would probably exceed the camera memory goals without even considering the memory circuitry at all.

Josephson junction effect memory (JEM) cells have been devised to write and nondestructively sense flux trapped in a superconducting loop. The Josephson tunneling junction responds typically in  $10^{-11}$  seconds and requires about  $10^{-18}$  joules per operation. These parameters are of interest for use in building future high speed super computers, but are not particularly relevant to the camera memory requirements. The work is still in the research stage. The open literature contains reports of various experimental devices to prove the feasibility of basic concepts. Fully decoded memory arrays are not likely to be available for some time.

## Appendix D

### Westinghouse MNOS BORAM 6001

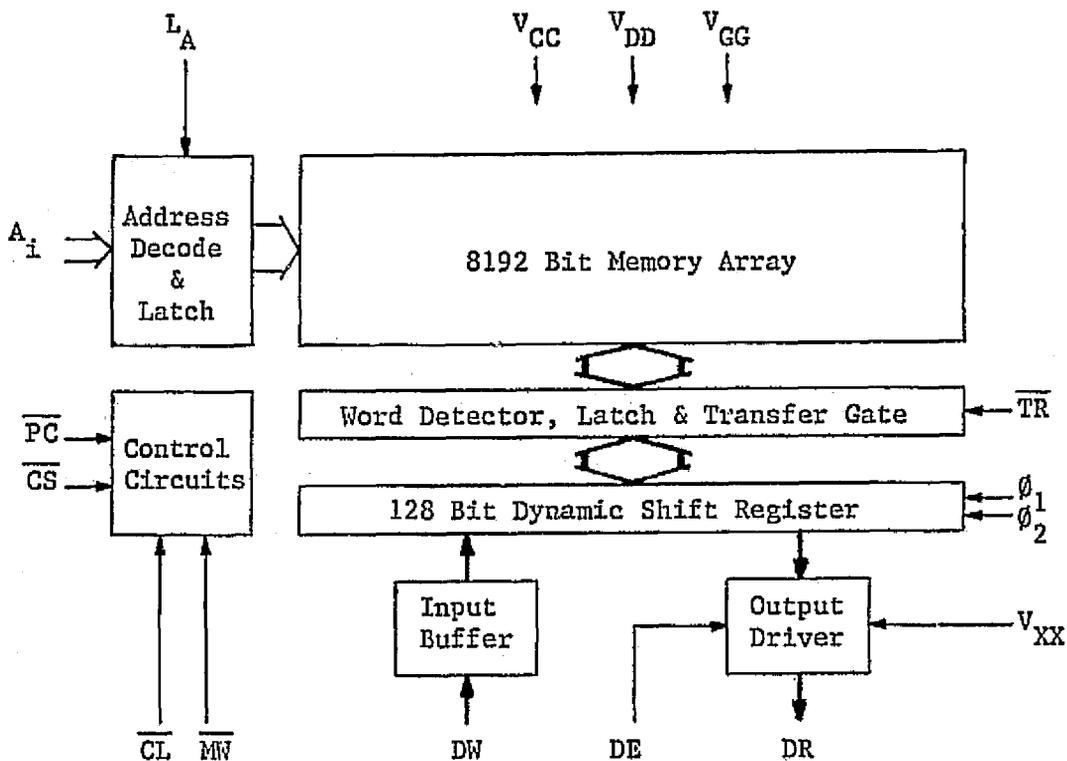
The material presented herein is a discussion of the nonvolatile MNOS type of memory chip that is recommended for spacecraft storage units of greater than  $10^6$  bits. Also included is a description of the MNOS micro-circuit packaging concept which has been employed successfully in diverse applications.

## BORAM 6001 MNOS MEMORY CHIP AND MICROCIRCUIT

The BORAM 6001 device is a block oriented 8192 bit memory chip. Its manufacturing process is a variation of proven P-channel metal gate technology. Reliability and producibility are enhanced by the conservative design rules established for the layout. A major feature of the die is the small size of the memory cell. The simplicity of the memory transistor allows a cell area of  $0.5 \text{ mils}^2$  without violating design rules. BORAM 6001 is intended for use in computer secondary storage. Typical systems will range in size from  $10^6$ -to- $10^8$  bits. The chip design emphasizes those features important to such applications. On chip power dissipation is minimized. Ratioless dynamic on chip peripheral circuitry is used wherever possible. Addressing is oriented toward blocks of 128 characters or words. Single chips form a bit slice of a block. Both clearing and writing are performed on a single block basis.

Figure 1 shows the functional organization of the BORAM 6001 chip. Preliminary performance specifications for the 6001 are shown in Table 1. The device contains a fully decoded 64 word by 128 bit random access memory and a 128 bit, two phase dynamic ratioless shift register. All input and output data is handled serially via the shift register. The memory array and the shift register may operate independently.

Internal to the chip the shift register is arranged as two interleaved registers. The net result is that the external data rate is two times the shift rate. As shift rates of 6 MHz have been observed over the operating temperature range for present day BORAM chips, it is expected that 12 MHz data rates can be maintained with the BORAM 6001. Considerations



$A_i$  - Address Inputs A0 to A5

$L_A$  - Latch Address Strobe

$\overline{PC}$  - Precharge Control

$\overline{CS}$  - Chip Select

$\overline{CL}$  - Clear

$\overline{MW}$  - Memory Write

DE - Data Enable (3rd state)

DR - Read Data Output

$V_{XX}$  - Output Stage Return Voltage Level

$\phi_1, \phi_2$  - Clock Inputs

$\overline{TR}$  - Transfer Control

$V_{CC}, V_{DD}, V_{GG}$  - Power Supplies

Figure 1. BORAM 6001 Chip Block Diagram

Table 1. Westinghouse BORAM 6001 MNOS Chip Specification

Characteristic	Parameter Value
Bits/Chip	8192
Organization	[ 64 rows [ 128 bits/row
Data I/O	[ 1 in and 1 out [ 128 bit shift register
Data Rate	2 times clock rate
Max Clock Rate	6 MHz
Clock Amplitudes	12 volts ( $2\phi$ )
Clock Line Capacitance	130pf ( $\phi_1$ and $\phi_2$ )
Transfer Line Capacitance	30pf
Address Latch Line Capacitance	20pf
Chip Select Line Capacitance	40pf
All Other Input Capacitance	4pf
Power (5 MHz data rate)	50mW

associated with clock driver limitations, though, make operation at a 5 MHz data rate (2.5 MHz shift rate) desirable for most memory applications.

The read-modify-write cycle waveforms for the memory chip appear in Figure 2. The cycle begins after the 6 bit address is latched. The rising edge of signal LA (latch address) determines when the address is captured. The address signals are free to change at all other items.

A precharge signal ( $\overline{PC}$ ) controls initial conditions within the RAM portion of the chip. While  $\overline{PC}$  is low, certain nodes within the device are clamped at specified voltage levels. When  $\overline{PC}$  goes high the clamps are removed and the RAM executes a read operation. A delay of about 5 microseconds is required to complete the read. The 128 bit word will then be held in the combination word detector, latch, and transfer gate. Application of a transfer signal ( $\overline{TR}$ ) causes a parallel transfer of the 128 bit word into the shift register. After the transfer signal returns to the high state, the shift register may begin operation.

The register will shift out one bit for possible modification by an external data processing circuit upon application of the first ( $\phi_1$ ) clock phase pulse. After being processed through the external circuitry, the data bit will be routed to the input terminal of the BORAM shift register. Upon application of the second ( $\phi_2$ ) clock phase pulse a new data bit will leave the register for modification, and the old (or modified) data bit will enter the register. This process continues until all of the bits have been processed. While the shift register is active, the latched addressed location in the RAM is being cleared. The control ( $\overline{CL}$ ) goes negative immediately after the read transfer is complete. Before the shifting operation is complete, the clear signal will be removed.

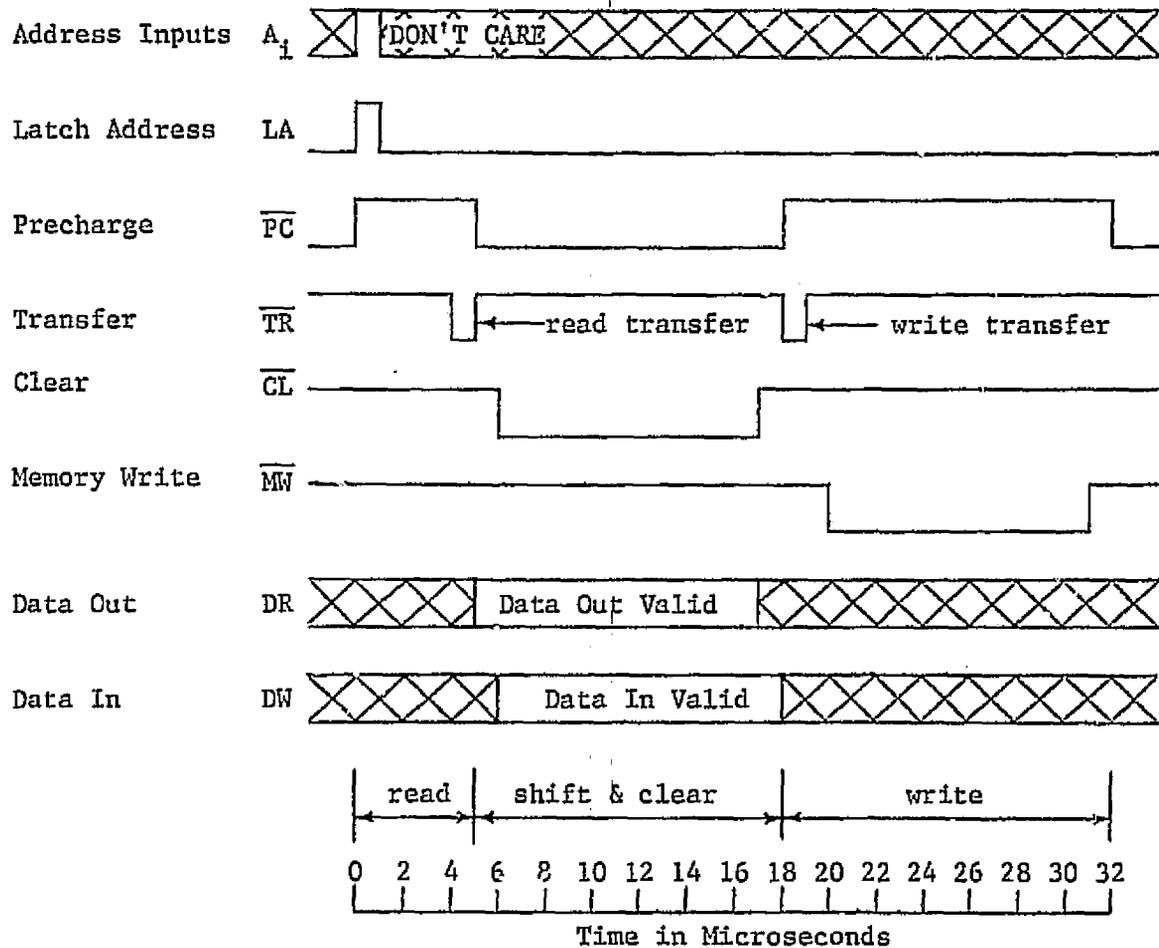


Figure 2. BORAM 6001 Read-Modify-Write Cycle Waveforms

Once the data in the register is properly positioned a write transfer may be initiated. The precharge signal goes positive to unclamp the circuitry in the combined detector and latch. The transfer pulse is applied in proper combination with the clock phase voltages, and the contents of the shift register force the state of the detector-latch circuit. The transfer pulse is now removed and the write operation is initiated. Signal  $\overline{MW}$  (memory write) controls the write.

The data output terminal of the BORAM chip is TTL compatible and provides three state operation. The output terminal will be in the high impedance state whenever the chip select ( $\overline{CS}$ ) is high or the data enable (DE) is low. This latter feature is important in that the write and read operations can be performed without tying up the output data bus.

BORAM 6001 devices are designed specifically for use in hybrid circuits. Figure 3 is a photograph of a prior BORAM microcircuit. The 6001 device will be packaged similarly. The microcircuit contains 16 chips (131,072 bits). It is the basic building block for BORAM memory modules. Figure 4 shows the functional organization of the microcircuit. Four chips are operated as a unit to service four different input and output data bus lines. Each group of four is controlled by separate chip select ( $\overline{CS}$ ) and clock lines. All other device terminals are common for all 16 chips.

BORAM memory microcircuits will soon be produced for Department of Defense applications. They form building blocks which will be common to many diverse systems manufactured by Westinghouse. The microcircuit has been configured with reliability and producibility as primary concerns. Each chip is accessible for testing. Every package will be subject to environmental tests and high temperature burn-in.

D-9

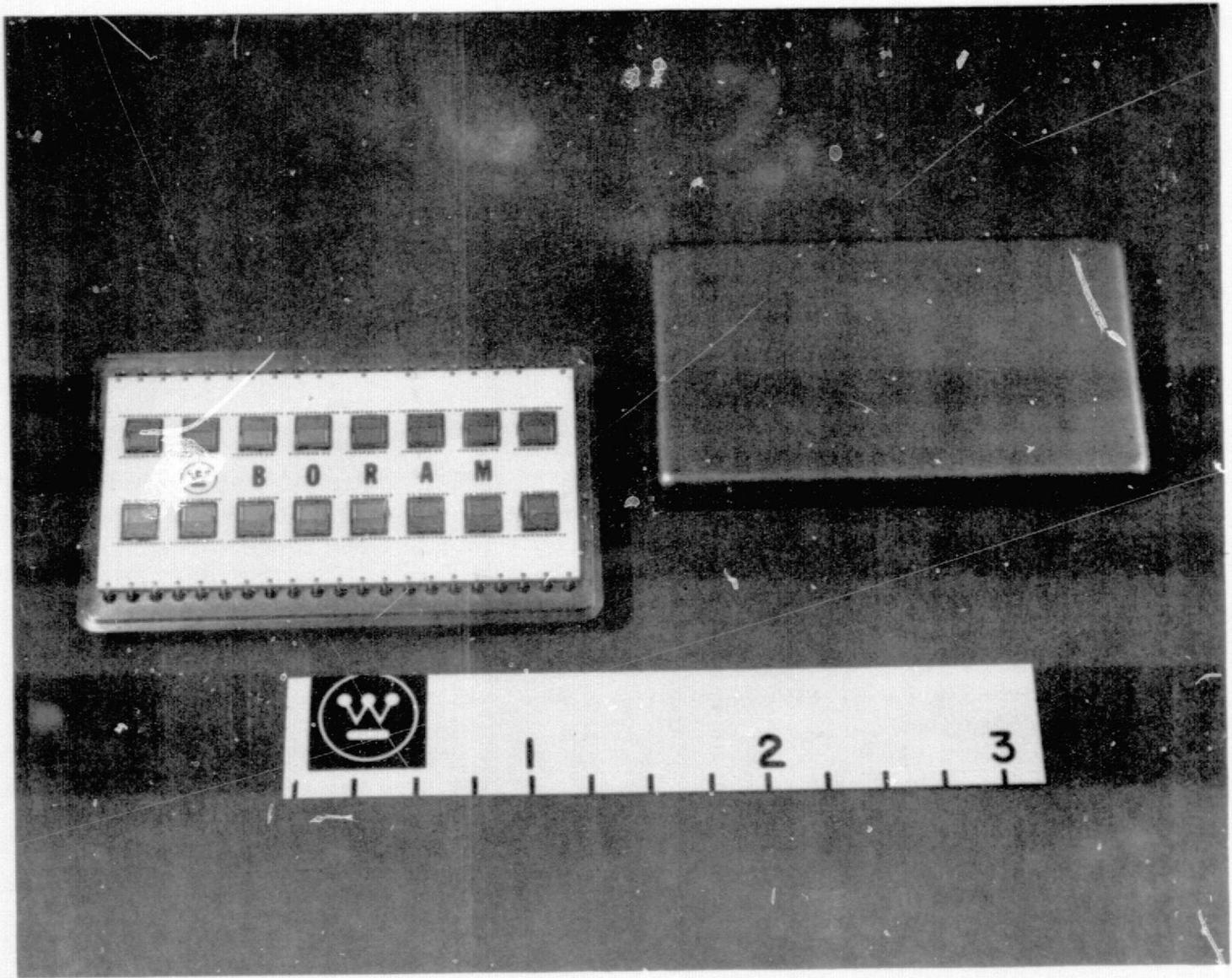


Figure 3. BORAM Microcircuit Physical Package

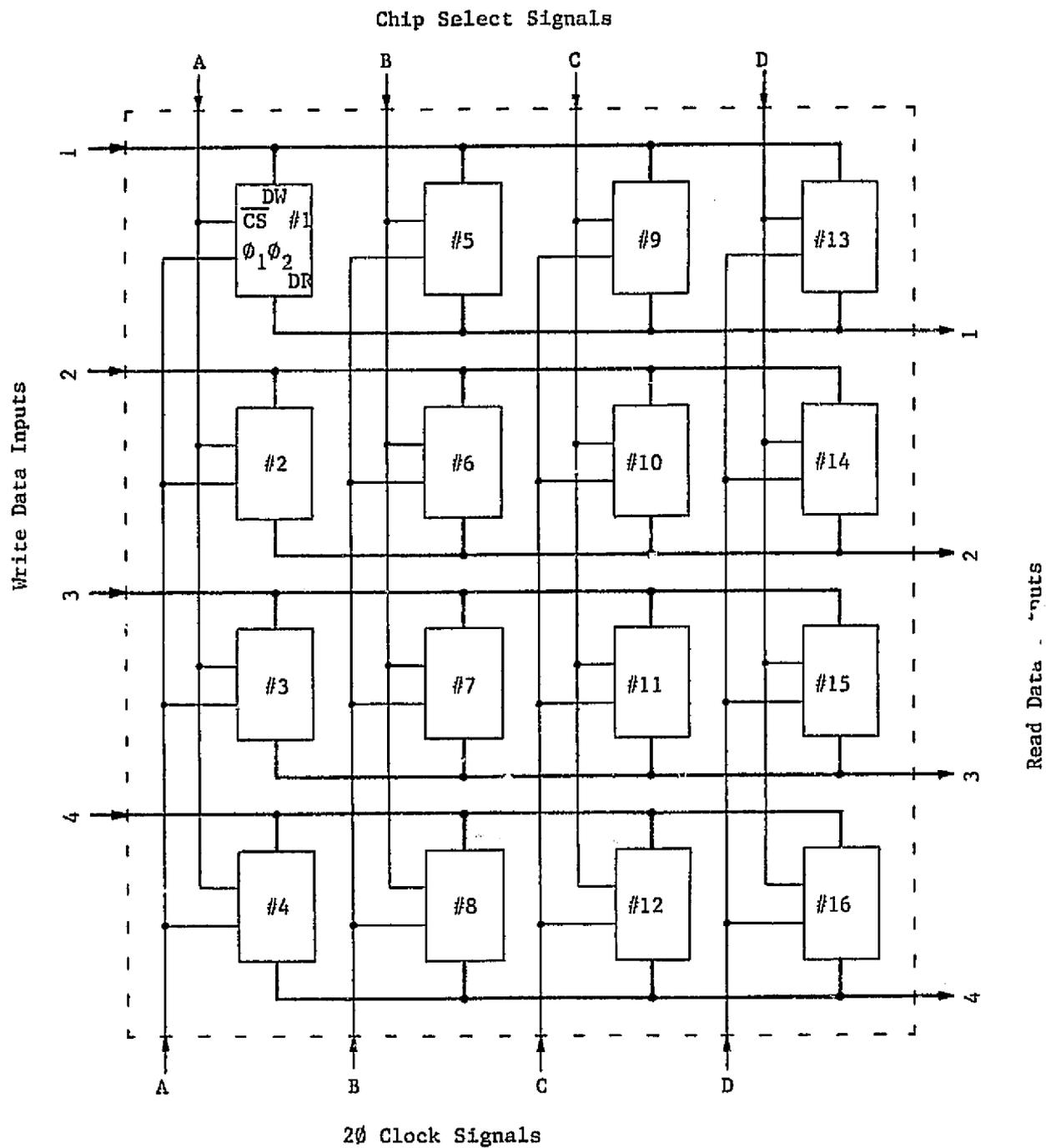


Figure 4. MNOS Microcircuit Functional Diagram

## GLOSSARY

### Abbreviations

A/D	-	analog-to-digital (converter)
AMD	-	Advanced Micro Devices
AMI	-	American Microsystems Incorporated
AMS	-	Advanced Memory Systems
BIOB	-	Bilateral Input and Output Bus (Register)
Bipolar	-	minority carrier controlled transistor
BNR	-	Bell Northern Research
BORAM	-	block organized RAM
BOSAM	-	block organized SAM
Bubble	-	cylindrical magnetic domain
CCD	-	charge coupled device
CFM	-	closed flux memory
CMOS	-	complementary MOS
Core	-	ferrite core technology
CPFF	-	cost plus fixed fee (contract)
Crosstie	-	contiguous domain wall structure
Disc	-	planar disc storage medium
DOT	-	domain tip propagation logic
dri	-	data refresh interval (subscript)
Daum	-	cylindrical drum storage medium
EAROM	-	electrically alterable ROM
EBAM	-	electron beam addressed memory (storage tube)
ECOM	-	U.S. Army Electronics Command
ELSEG	-	elementary segment (storage/failure unit)
EREX	-	error exorcism (shrinking memory)
FAME	-	ferroacoustic memory
IBM	-	International Business Machines
ICCD	-	intensified CCD (photosensor)
I <sup>2</sup> L	-	integrated injection logic (bipolar)
I/O	-	input-output
IR	-	infra-red
ISB	-	intermediate significant bit

## Abbreviations

JEM	-	Josephson tunneling effect memory
LSB	-	least significant bit
LST	-	large space telescope
MAS	-	metal alumina semiconductor
Mentor	-	ferroelectric thin film memory
MIL	-	Microsystems International Limited
MIL.	-	military (standard, specification, etc.)
MNOS	-	nitride interfaced MOS
MOS	-	metal oxide semiconductor
MSB	-	most significant bit
MTBF	-	mean time between failure
N-MOS	-	N-channel MOS
NOL	-	U.S. Navy Ordnance Laboratories
NRL	-	U.S. Navy Research Laboratories
OBAM	-	optical beam addressed memory
OFM	-	digatomic thin film memory
OVONIC	-	Ovoshinsky amorphous semiconductor
P-MOS	-	P-channel MOS
RAM	-	random accessed memory
RCA	-	Radio Corporation of America
RMM	-	read mostly memory
RMW	-	read-modify-write (cycle)
ROM	-	read only memory
SAM	-	serially accessed memory
SAW	-	surface acoustic wave
SECUR	-	single error correction (encoding)
SIM	-	sensor (or scientific) instrument memory
SIP	-	sensor (or scientific) instrument package
SISO	-	serial input and serial output (register)
SIT	-	silicon intensified target (imaging tube)
Soliscan	-	magnetostrictive thin film memory
SOS	-	silicon-on-sapphire (technology)
SOW	-	statement of work

### Abbreviations

Tape	-	maumetic tape recorder
TI	-	Texas Instruments
UV	-	ultra-violet
Wire	-	plated wire technology
WORAM	-	word organized RAM
WOSAM	-	word organized SAM
1T	-	one transistor (storage cell)
3T	-	three transistor (storage cell)

### Conversion Factors

1 inch	=	2.54 cm
1 mil	=	$10^{-3}$ inch
1Å	=	$10^{-10}$ meter
1 inch <sup>2</sup>	=	645.2 μm <sup>2</sup>
1 inch <sup>3</sup>	=	16.39 cm <sup>3</sup>
1 liter	=	$10^3$ cm <sup>3</sup>
1 oz	=	28.35 gram
1 lb	=	0.4536 Kg
0°C	=	273.15° Kelvin
[temp] <sup>o</sup> F	=	(9/5) [temp] <sup>o</sup> C + 32

### Prefix Units

T	-	tera	-	$10^{12}$
G	-	giga	-	$10^9$
M	-	mega	-	$10^6$
K	-	kilo	-	$10^3$
c	-	centi	-	$10^{-2}$
m	-	milli	-	$10^{-3}$
μ	-	micro	-	$10^{-6}$
η	-	nana	-	$10^{-9}$
p	-	pico	-	$10^{-12}$
f	-	femto	-	$10^{-15}$

## Terminology

access time	-	(on word or bit basis) delay from request to execution
active	-	denotes device with power supplied (not necessarily dynamically active)
adder	-	performs numerical summation of two binary numbers
average power	-	dissipation occurring at 1/10th maximum data rate
bilateral	-	signal flow can proceed in either direction
bipolar	-	minority carrier integrated circuit device
bit	-	binary digit
bit parallel	-	word bits processed concurrently
bit serial	-	data bits occur in sequential order
block	-	multiple group of words or bits
Boksenberg Camera	-	a photosensor system used to detect discrete photoevents
byte	-	8 bits, in this report (no universal definition)
camera memory	-	storage media for data from spacecraft photodetectors
capacity	-	quantity of data (bits or words) that storage media can hold
cell	-	discrete LSI memory element site
cycle time	-	period to complete assigned sequence of operations
data rate	-	frequency of occurrence of photoevents
dormant	-	denotes device electrically inactive (all power removed)
dynamic	-	volatile storage media requiring AC (and DC) power for data retention
error rate	-	fractional number of faulty bits occurring per bit processed
failure	-	discontinuation of or deviation from prescribed operation
fit	-	1 failure in $10^9$ device hours
hard error	-	a nonrecoverable bit error, caused by a device failure
latency time	-	(on block basis) delay from request to start of access
LST-1	-	first LST to be launched about 1980
LST-2	-	second LST to be launched about 1982
mission time	-	duration of life-cycle projection for system (spacecraft)
mode	-	prescribed operating sequence of memory
mortality	-	condition under which system is considered useless (dead)

## Terminology

multiplex	-	process of time sharing parallel signals on a single channel
nonredundant	-	structure contains no mechanisms performing same functions
nonvolatile	-	storage media which retains data upon power loss
overhead burden	-	degradation in memory density parameters introduced by peripheral circuitry
parallel	-	words or bits accessed in same time period
peak power	-	dissipation occurring at maximum data rate
peripheral circuitry	-	section of memory containing control electronics
photoelectron	-	free charge carrier in detector, released by input of a photon
photon event	-	generation of photoelectrons by impinging photon (quanta)
pixel	-	picture element
program word	-	group of bits used to specify memory operational sequences
radiation hardened	-	resistant to ionizing radiation damage
random	-	words or bits accessible selectively in any order
read/write	-	control line (signal) selection of read or write operations
redundancy	-	denotes presence of mechanisms capable of identical functions
refresh	-	process of replenishing decayed charge in dynamic cell
reliability	-	probability of proper operation at specific point in life-cycle
scan rate	-	frequency of sampling photodetector pixels
sector	-	storage sub-division
self-test	-	operation of checking functional status of system components
sequential	-	words or bits in time contiguous progression
serial	-	(same as sequential)
simplex	-	(same as nonredundant)
soft error	-	a transitory bit error, recoverable by rereading
spare	-	extra devices carried along to replace failed units
static	-	volatile storage media requiring only DC power for data retention

## Terminology

- storage - media for recording desired information
- storage array - section of memory containing data recording media
- System A - LST-1 camera memory
- System B - LST-2 camera memory
- tri-state - high impedance capability added to binary gate
- unipolar - majority carrier integrated circuit device
- vector - storage address space
- volatile - storage media which loses data upon power loss
- word - storage capacity assigned to each pixel
- word serial - data words occur in sequential order

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