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PLATED WIRE RANDOM ACCESS MEMORIES

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June 1975
FINAL REPORT FOR PERIOD
June 1974 - June 1975

Prepared for
GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland 20771
FINAL REPORT

PLATED WIRE RANDOM ACCESS MEMORIES

June 1975
for period
June 1974 - June 1975

Contract No. NAS 5-20576
for
GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland 20771

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8201 E. McDOWELL ROAD, SCOTTSDALE, ARIZ. 85252
REPORT NO. 4601-400
TOTAL PAGES 218
EFFECTIVE PAGES:
1 thru iii
1 thru 34

ATTACHMENTS:
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ATTACHMENT I: ACCEPTANCE TEST PROCEDURE (35 Pages)
ATTACHMENT II: ACCEPTANCE TEST DATA SHEETS S/N 103 (35 Pages)
ATTACHMENT III: ACCEPTANCE TEST DATA SHEETS S/N 104 (35 Pages)
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M
This Final Report documents the work done under NASA Contract NAS-5-20576 by Motorola, Inc., Government Electronics Division for the Goddard Space Flight Center, Greenbelt, Maryland. The work performed under the subject contract entailed the construction and testing of a 4096-words by 18-bits Random Access, NDRO-Plated Wire Memory. Four memory units were delivered to Goddard. This report gives the performance requirements, construction, and test history of the units along with a complete technical and functional description. The report covers the period from June 1974 through June 1975.
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<td>5</td>
<td>Simplified Memory Drive and Sense Diagram</td>
<td>17</td>
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<td>6</td>
<td>Word-Line Selection Matrix</td>
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<td>7</td>
<td>Sequencer, Logic Diagram</td>
<td>20</td>
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<tr>
<td>8</td>
<td>System Timing, Write Operation</td>
<td>21</td>
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<td>9</td>
<td>System Timing, Read Operation</td>
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<td>10</td>
<td>Four-Channel Sense Amplifier, Functional Diagram</td>
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<td>Delay Circuit, Functional Diagram</td>
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<td>12</td>
<td>Custom Package and Layout</td>
<td>27</td>
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<td>13</td>
<td>Word-Line Selection Matrix, Functional Diagram</td>
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<td>14</td>
<td>Digit Driver, Functional Diagram</td>
<td>29</td>
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<td>15</td>
<td>Power Switch +5V/-6V</td>
<td>30</td>
</tr>
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<td>16</td>
<td>Power Switch +5V/+5V</td>
<td>30</td>
</tr>
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<td>17</td>
<td>Tunnel Structure Construction</td>
<td>32</td>
</tr>
<tr>
<td>18</td>
<td>Memory Plane Construction</td>
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SECTION 1
INTRODUCTION AND OVERALL PROGRAM SUMMARY

1. INTRODUCTION

This Final Engineering Report documents the overall activity and history of the work performed by Motorola Inc., Government Electronics Division, Scottsdale, Arizona for the Goddard Space Flight Center, Greenbelt, Maryland, under NASA Contract No. NAS 5-20576. The report is submitted in accordance with the requirements of Specifications 73-15079 modified June 1974 and the addendum dated May 1974, and covers the period from June 1974 through June 1975.

1.1 PROGRAM SUMMARY

The work performed under the subject contract entailed the construction and testing of a 4096-word by 18-bit Random Access, NDRO-Plated Wire Memory.

The primary design parameters, in order of importance, were:

- High reliability
- Low power
- Volume
- Weight

Four memory units, serial no. 103, 104, 105, and 106 were delivered.

1.2 RESULTS ATTAINED

The memory units were subjected to comprehensive functional and environmental testing at the end-item level to verify conformance with the specified requirements.

A comparison of the memory unit's most significant physical and performance characteristics versus the specified requirements is shown in Table 1.
<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Contract Reference</th>
<th>Specified</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Volume</td>
<td>73-15079</td>
<td>160 in³</td>
<td>158.5 in³</td>
</tr>
<tr>
<td>Weight</td>
<td>73-15079</td>
<td>5.8 Pounds</td>
<td>5.640 pounds (SN103)</td>
</tr>
<tr>
<td></td>
<td>Mod 6/20/74</td>
<td></td>
<td>5.562 pounds (SN104)</td>
</tr>
<tr>
<td></td>
<td>Mod 6/20/74</td>
<td></td>
<td>5.594 pounds (SN105)</td>
</tr>
<tr>
<td></td>
<td>Mod 6/20/74</td>
<td></td>
<td>5.580 pounds (SN106)</td>
</tr>
<tr>
<td>Power</td>
<td>73-15079</td>
<td>7 watts</td>
<td>5.963 watts max (SN103)</td>
</tr>
<tr>
<td>Operate</td>
<td>Mod 6/20/74</td>
<td></td>
<td>5.914 watts max (SN104)</td>
</tr>
<tr>
<td></td>
<td>Mod 6/20/74</td>
<td></td>
<td>5.324 watts max (SN105)</td>
</tr>
<tr>
<td></td>
<td>Mod 6/20/74</td>
<td></td>
<td>5.687 watts max (SN106)</td>
</tr>
<tr>
<td>Power</td>
<td>73-15079</td>
<td>170 milliwatts</td>
<td>149 milliwatts max (SN103)</td>
</tr>
<tr>
<td>Standby</td>
<td></td>
<td></td>
<td>147 milliwatts max (SN104)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>139 milliwatts max (SN105)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>147 milliwatts max (SN106)</td>
</tr>
<tr>
<td>Voltage</td>
<td>73-15079</td>
<td>±5% on all</td>
<td>±5% on all</td>
</tr>
<tr>
<td>Tolerance</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Rate</td>
<td>73-15079</td>
<td>500 kHz</td>
<td>600 kHz</td>
</tr>
<tr>
<td>Access Time</td>
<td>73-15079</td>
<td>500 nanoseconds</td>
<td>&lt;500 nanoseconds</td>
</tr>
<tr>
<td>Operating Temp.</td>
<td>73-15079</td>
<td>-40°C to +85°C</td>
<td>Tested from -40°C to +85°C</td>
</tr>
<tr>
<td>Operating Vacuum</td>
<td>73-15079</td>
<td>One atm. to 10⁻⁵</td>
<td>Tested from one atm. to 10⁻⁵</td>
</tr>
<tr>
<td></td>
<td>Mod 6/20/74</td>
<td>mm Hg modified</td>
<td>mm Hg modified for test purposes.</td>
</tr>
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</table>
Table 1. Memory Performance Versus Specified Requirements (Contd)

<table>
<thead>
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<th>Characteristic</th>
<th>Contract Reference</th>
<th>Specified</th>
<th>Measured</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Vibration</td>
<td>73-15079 Mod 6/20/74</td>
<td>Sinusoidal</td>
<td>Tested at specified levels</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5.25 Hz-.33 in da</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>25-110 Hz-10g Peak</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>110-2000 Hz-5g Peak</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Peak Two octaves/minute</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Random</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15 Hz,.0004 g^2/Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>15-70 Hz,</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Linear Increase</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>70-100 Hz,</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.138 g^2/Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>100-400 Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Linear Decrease</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>400-2000 Hz,</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.0089 g^2/Hz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Two min/axis</td>
<td></td>
</tr>
<tr>
<td>Operating Shock</td>
<td>73-15079</td>
<td>Two shock pulses of 30g for 6 and</td>
<td>Tested at specified levels</td>
</tr>
<tr>
<td></td>
<td></td>
<td>12 milliseconds in three axis</td>
<td></td>
</tr>
</tbody>
</table>
SECTION 2
HISTORICAL PROGRAM SUMMARY

2. PROGRAM HISTORY

The design modification, construction, and test history, as related to the hardware requirements of this contract, is summarized in this section.

Four low-power random access spacecraft memories were constructed, tested, and delivered under this contract. The memories were constructed using the same basic design as units SN101 and SN102, previously delivered under contract no. NAS5-23163, with slight modifications. The word current generator was changed from a hybrid circuit to a discrete circuit which required a new layout of the timing and control board. The housing material was changed from aluminum to magnesium and the mu-metal magnetic shielding was removed to reduce the overall weight of each unit.

The initial contract was for three memory units with an option for two follow-on units. On 9/23/74 the contract was modified to exercise the option on the fourth memory unit and revise delivery schedule due to repair of a memory unit previously delivered under contract no. NAS 5-23163 which had been subjected to over temperature at GSFC.

The summarization is in chronological order from date of contract award to date of final delivery of the memory units.

2.1 SERIAL NUMBER 103

Assembly was completed and system testing began in January 1975. On 2/6/75 GSFC reported they had found a wire bond problem while performing construction analysis on the single digit driver hybrid circuits. Construction analysis at Motorola confirmed the problem and traced the cause to contamination of the gold plating on the single digit driver package. New packages were procured, tested for gold purity, and new single digit driver hybrids were constructed. The new single digit driver hybrids were installed in March 1975 and system test resumed.
Several minor design modifications were recommended to GSFC in April 1975 to improve waveform timing tolerances due to capacitance differences with the new Timing and Control board layout and to reduce power consumption. These modifications were approved by GSFC and incorporated in all units.

The unit was acceptance tested and shipped to GSFC on May 13, 1975.

2.2 SERIAL NUMBER 104

Assembly was completed and system testing began in April 1975. Due to bit errors during stack test and system test Serial Number 105 advanced ahead of SN104. Acceptance testing was completed on June 9, 1975 and shipped to GSFC.

2.3 SERIAL NUMBER 105

Assembly was completed and system testing began in May 1975. During acceptance test three failures occurred. GSFC Malfunction Reports were written and submitted to GSFC.

The first failure was a marginal level bit error which occurred during worst case pattern testing at \(-40^\circ C\) and was corrected by replacing a wire pair. Reference GSFC MRF No. D07898.

The second failure was again a marginal level bit error which occurred during worst case pattern testing. This error occurred during the intermediate temperature test after the \(-40^\circ C\) testing had been completed. The error was corrected by replacing a wire pair. Reference GSFC MRF No. D07899.

The third failure also occurred at cold temperature. This time a complete digit pair was bad due to a film of flux on one of the connector pins. Reference GSFC MRF No. D078900. The connector pins were cleaned and the unit confidence tested at cold temperature. Temperature testing per the acceptance test procedure was repeated and the unit shipped to GSFC on May 30, 1975.
2.4 SERIAL NUMBER 106

Assembly was completed and system testing began in May 1975. The unit failed cold temperature test due to an unsoldered pin on I/C U5 on the Timing and Control Board. GSFC Malfunction Report No. D09085 was written and submitted to GSFC. Acceptance testing was completed and the unit was shipped to GSFC on June 26, 1975.
Figure 1. 4K x 18 Bit Plated Wire Memory System

Figure 2. 4K x 18 Bit Plated Wire Integral Assembly
SECTION 3
TECHNICAL DESCRIPTION

3. DESCRIPTION

The memory unit is shown in Figures 1 and 2. The unit is identified as Motorola Part Number 01-P13701D002. Serial Numbers 103, 104, 105 and 106 were fabricated, tested & delivered.

3.1 SYSTEM CONFIGURATION

Motorola Drawing Numbers 01-P13701D, 15-P13745D, and 15-13746D (included in the engineering drawing package submitted to GSFC) completely define the end-item package in terms of size, mounting pattern, etc. The external connector pin assignments are as given in Table 2. The weight of each delivered unit was <5.8 pounds.

3.2 ELECTRICAL INTERFACE

Connectors J1 and J2 are Deutsch, Type 75020-442P, as modified and supplied by GSFC. The total memory interface is comprised of the following (Refer to Figure 3 Memory System Electrical Interface):

- 18 Input Data Lines (to memory)
- 16 Input Address Lines (to memory)
- 18 Output Data Lines (from memory)
- 1 Initiate Line (to memory)
- 1 Read/Write Select Line (to memory)
- 1 Read Complete Line (from memory)
- 2 Thermistor Sensor Lines (from memory)
- 7 Lines for -6.1V (to memory - all lines common internally)
- 5 Lines for +5.0V (to memory - all lines common internally)
- 12 Lines for Power and Signal Return (all lines common internally)
Figure 3. Memory System Electrical Interface
All signal inputs and outputs are to, or from, TTL Series 54 Standard logic devices. All inputs present one unit load. There is no internal loading on any of the output signal lines. The 18 data output lines and the read complete line are driven from open collector logic elements whose output transistor is normally in the OFF state.

The electrical interface characteristics of the delivered unit are as follows. On all signal inputs, a logic ONE is defined as the most positive voltage level, with respect to the return. On all signal outputs, a logic ONE is defined as the high impedance state. All time relationships are defined from the 50 percent points of the respective signals. Transition times (where applicable) are as specified for TTL Series 54 Standard logic with loading as applied. Stability is defined as being above the minimum logic ONE level or below the maximum logic ZERO level.

Memory Capacity: 4096 words of 18 bits each (73,728 bits total).

Access: Random by word via 12-bit input address. Also provides for addressing by memory unit via four-bit bank address. All bank address bits must be at a logic ONE for access.

Access Time: 500 nanoseconds, maximum, from leading edge of Initiate signal.

Read Cycle Time: 1.20 microseconds, maximum, from leading edge of Initiate signal.

Write Cycle Time: 1.00 microseconds, maximum, from leading edge of Initiate signal.

Operate Rate: 0 to 600k operations per second, minimum, with any read/write ratio.

Initiate Signal: Active level = logic ONE. Minimum pulse width = 50 nanoseconds. Maximum pulse width = 450 nanoseconds.

Read/Write Select: Read = logic ONE. Write = logic ZERO. Must be stable from leading edge of Initiate signal to end of read or write cycle.

Bank Address Lines: Must be stable from leading edge of Initiate pulse to end of Read or Write cycle.

Word Address Lines: Must be stable from leading edge of Initiate to end of cycle time.
<table>
<thead>
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<th>Pin No.</th>
<th>Function</th>
<th>Pin No.</th>
<th>Function</th>
</tr>
</thead>
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<tr>
<td>J1-1A</td>
<td>Address Bit 2⁰</td>
<td>J2-1A</td>
<td>Data Input Bit 2⁰</td>
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<tr>
<td>-1B</td>
<td>Address Bit 2¹</td>
<td>-1B</td>
<td>Data Input Bit 2¹</td>
</tr>
<tr>
<td>-1C</td>
<td>Address Bit 2²</td>
<td>-1C</td>
<td>Data Input Bit 2²</td>
</tr>
<tr>
<td>-1D</td>
<td>Address Bit 2³</td>
<td>-1D</td>
<td>Data Input Bit 2³</td>
</tr>
<tr>
<td>-1E</td>
<td>Address Bit 2⁴</td>
<td>-1E</td>
<td>Data Input Bit 2⁴</td>
</tr>
<tr>
<td>-1F</td>
<td>Address Bit 2⁵</td>
<td>-1F</td>
<td>Data Input Bit 2⁵</td>
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<tr>
<td>-1G</td>
<td>Address Bit 2⁶</td>
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<td>Data Input Bit 2⁶</td>
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<td>-1H</td>
<td>Return</td>
<td>-1H</td>
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<tr>
<td>-1J</td>
<td>Read/Write Control</td>
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<td>Data Input Bit 2⁸</td>
</tr>
<tr>
<td>-1K</td>
<td>Return</td>
<td>-1K</td>
<td>Data Input Bit 2⁹</td>
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<td>-1L</td>
<td>Return</td>
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<td>Data Input Bit 2¹⁰</td>
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<td>-1M</td>
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<td>-1N</td>
<td>Initiate Command</td>
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<td>Data Input Bit 2¹³</td>
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<td>-2A</td>
<td>Address Bit 2⁷</td>
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<td>Data Input Bit 2¹⁴</td>
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<td>-2B</td>
<td>Address Bit 2⁸</td>
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Table 2 External Connector Pin Assignments (Contd)

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<th>Function</th>
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</thead>
<tbody>
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<td>J2-2P</td>
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<tr>
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<td>-3A</td>
<td>Data Output Bit 2^10</td>
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<td>Bank Address Bit 3</td>
<td>-3B</td>
<td>Data Output Bit 2^11</td>
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<tr>
<td>-3C</td>
<td>+5.0V</td>
<td>-3C</td>
<td>Data Output Bit 2^12</td>
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<td>-3D</td>
<td>Data Output Bit 2^13</td>
</tr>
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<td>-3E</td>
<td>Data Output Bit 2^14</td>
</tr>
<tr>
<td>-3F</td>
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<td>-3F</td>
<td>Data Output Bit 2^15</td>
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<tr>
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<tr>
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<tr>
<td>-3K</td>
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</tr>
<tr>
<td>-3L</td>
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<td>Return</td>
</tr>
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<td>Return</td>
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</tr>
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<td>Return</td>
</tr>
<tr>
<td>-3P</td>
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<td>-3P</td>
<td>Return</td>
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</table>

**Input Data Lines:** For write operations, must be stable from leading edge of Initiate to end of cycle time. For read operations, may be any level within TTL logic limits.

**Read Complete Line:** Presents high impedance (20k minimum) in quiescent state. Goes active (i.e. low impedance) at end of access time (maximum of 500 nanoseconds following leading edge of Initiate signal). Remains at active level for minimum of 250 nanoseconds and maximum of 450 nanoseconds. Will sink minimum of 10 mA at 0.3V in active state.

**Data Output Lines:** Presents high impedance state (20k minimum) in quiescent state. Goes active (i.e. low impedance) prior to or in coincidence with the leading edge of Read Complete signal and remains active for minimum of 150 nanoseconds following trailing edge of Read Complete signal and maximum of 750 nanoseconds. Will sink minimum of 10 mA at 0.3 V in active state.
3.2.1 Power Source Requirements

The memory unit operates from power sources of +5.0V and -6.1V. Requirements imposed on these power sources by the memory are as follow (all measurements made at connector terminals):

**+5.0V:**

Regulation: ±5%

Average Standby Current: **12.2 mA**, worst-case.

Average Operate Current: 795 mA, worst-case at operate rate of 500k operations per second and read/write ratio of one.

Standby Power: 64.1 milliwatts maximum at +5.25V.

Operate Power: **4.171 watts**, maximum, at +5.25V and at operate rate of 500 kHz with a read/write ratio of one.

**-6.1V:**

Regulation: ±5%

Average Standby Current: **14.5 mA**, worst-case.

Average Operate Current: 280 mA, worst-case at operate rate of 500k operations per second and read/write ratio of one.

Standby Power: 92.8 milliwatts, maximum, at -6.40 volts.

Operate Power: **1.792 watts**, maximum, at -6.40 volts and at operate rate of 500 kHz with read/write ratio of one.

3.2.2 Thermistor Characteristics

The thermistor is mounted at the approximate center of the unit. It is a YSI Type 44006 precision element with a nominal impedance of 10k ohms at +25°C. The resistance versus temperature characteristic is given in Table 3.
Table 3. Thermistor Resistance Versus Temperature

<table>
<thead>
<tr>
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<tr>
<td>-70</td>
<td>3296</td>
</tr>
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<td>210</td>
<td>470.1</td>
</tr>
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</table>

RESISTANCE VERSUS TEMPERATURE 80°C to -150°C
3.3 FUNCTIONAL DESCRIPTION

3.3.1 Memory Organization

The memory is organized into 1024 memory words of 72 bits each (expandable to 96 bits). Each memory word therefore comprises four 18-bit external data words. Figure 4 is a block diagram of the memory organization. The memory stack itself is packaged on eight identical printed wiring, glass-epoxy substrates, with 128 two-turn word lines on each board, for a total of 1024.

Each word-line wraps twice around 144 plated wires, with the corresponding wires in each of the eight boards connected in series. At the far end, each pair of adjacent wires is shorted together, forming seventy-two pairs, with each pair traversing between all 1024 word-lines. The opposite ends of each pair terminate at the input of a differential sense amplifier. The outputs of a bi-directional digit driver current source is also connected to each pair of wires at the same end as the sense terminations. A specific bit storage location is formed at the crossover points of a particular word line and a pair of plated wires.

Using two wires for each bit storage (i.e., two crossovers) allows a differential implementation for information sensing, virtually eliminating common-mode noise problems and increasing the signal outputs at any given word current level, thus permitting operation at lower word currents than would have been required with a single crossover-per-bit implementation.

A memory word consists of the 72 bits under a single word line on a particular memory stack board. A particular data word address uniquely locates an 18-bit data word by identifying a word line and a group of 18 sense amplifier channels or 18 digit driver current sources.

The only electronics packaged as part of the memory stack is associated with word line selection. The rest of the electronics is packaged on three similar board assemblies.

3.3.2 Word-Line Selection and Drive

Figures 5 and 6 show the word current selection and drive method. Word-line addressing is accomplished through a two-level tree of transistor switches. The first level steers the word current to one of 64 unique areas of the stack. The second level steers the word current into one of 16 word lines in the particular word group addressed through the first level. Both levels are packaged on the memory stack boards.
Figure 4. Overall Functional Block Diagram
Figure 5.  Simplified Memory Drive and Sense Diagram
Figure 6. Word-Line Selection Matrix
The data word address is decoded in the sequencer, using SNC 5445 Binary-to-Decimal Decoders. Address bits $2^2$, $2^3$, $2^6$ through $2^9$ are decoded into 1-of-64 and identify the word group. Bits $2^0$, $2^1$, $2^4$ and $2^5$ are decoded into 1-of-16 and identify the word line within a group. Bits $2^{10}$ and $2^{11}$ identify a particular data word location (1-of-4) along the addressed word line. The apparent anomaly in sequence of the bits allocated for identification of word group and word line is a result of test considerations. With the switching matrix implementation used in the system, the address bit allocation defined above will identify adjacent word lines across a plane when the address sequences in a straight binary code.

Since only one end of each word-line is actively switched (with the opposite end returned to ground) only the addressed word-line has any voltage applied to it (with reference to the quiescent level). Thus, current flow in the stack resulting from charge transfer to/from stray capacitance is minimized and stack charge "restoration" is not necessary. The resulting design is significantly less complex, faster and more noise-free.

A transformer is used for coupling between the word current generator and the word line selection matrix to negate the need for a third, high-voltage power input. The transformer also provides some additional measure of noise reduction.

3.3.3 Control and Sequencing

The memory design does not use a discrete internal clock. Instead, memory sequences are generated from a series of programmable delays. A diagram of the sequencer logic is shown in Figure 7. Each delay is programmable, independent of any other delay. (The actual programming is accomplished by selection of discrete component values). Thus, timing sequences can be optimized for performance and power consumption.

Power to all but a minimum of control logic is switched off between memory cycles. The delay circuit is designed to come up in a normalized state when power is applied.

When an Initiate signal occurs, the power switch is turned on. If the signal is of longer duration than delay $\tau_A$ (approximately 35 nanoseconds), then the Initiate Override signal is actuated, locking the memory in the operate mode until the read or write cycle is completed.

Power to the digit drivers, sense amplifiers, and associated logic is also controlled, through the sequencer. The corresponding power switches are physically located on the digit electronics board assemblies.

Delays $\tau_B$ through $\tau_E$ are activated for a write cycle. Delays $\tau_B$ and $\tau_D$ set the width of the two phases of digit current and $\tau_C$ sets the separation between the two phases. Delay $\tau_E$ controls the duration of the word current. The $\phi_1$ and $\phi_2$ digit current controls for one of the four possible data words are activated, depending on the states of address bits $2^{10}$ and $2^{11}$.
Delays $\tau_F$ through $\tau_I$ are activated during a read cycle. Delay $\tau_F$ starts the word current after power start-up transients have had an opportunity to dissipate. A pick-off from the word current level is delayed by $\tau_G$ and used as the read strobe, which clocks the sense amplifier outputs into the output data buffer register. Delays $\tau_H$ and $\tau_I$ set the duration of the read complete and the post-read data hold periods, respectively.

### 3.3.4 Write Operation

The memory timing for a write cycle is shown in Figure 8. For proper operation, the address, data and read/write control signals must be stable prior to the leading edge of the initiate command and must remain stable until the write cycle has been completed.

When an initiate command pulse occurs in the presence of a low (or ground) level on the read/write control line, power to the sequencer and to the write electronics is turned on. A low impedance path is connected from the word current generator to a particular word line (through the word line selection matrix) as identified by address bits $2^0$ through $2^9$. A group of 18 digit driver current sources is then energized for $\phi_1$ current. The particular current sources are identified by address bits $2^{10}$ and $2^{11}$. The polarity of current (i.e. direction along the plated wire element) from any current source is controlled by the logic level of the data input to that current source. The $\phi_1$ digit current is then terminated and $\phi_2$ current enabled. The two phases are of equal amplitude and duration. This balanced current implementation precludes any hysteresis build-up due to an unequal history of data "one" and "zero" writes.

Figure 8. System Timing, Write Operation
The word current generator is energized early enough that the terminating transition of the word current can be made to occur during the time when $\phi_2$ digit current is at full amplitude. Data is "written into" the wire when the word current terminates in the presence of digit current.

At the end of the $\phi_2$ digit current, the write cycle is complete and internal system power is turned off. A write cycle, from the leading edge of the initiate command to turn-off of system power, requires approximately 750 nanoseconds.

3.3.5 Read Operation

The memory timing for a read cycle is shown in Figure 9. For proper operation, the address and read/write control lines must be stable prior to the leading edge of the initiate command and must remain stable until completion of the read cycle.

When the initiate command pulse occurs in coincidence with a high level on the read/write control line, power to the sequencer and the read electronics is turned on. A low impedance path is again connected to the addressed word line through the word line selection matrix. A group of 18 sense amplifier channels are selected, as identified by address bits $2^{10}$ and $2^{11}$.

After any transients generated in the sense amplifiers have had a chance to settle out, the word current generator is energized. Signals are induced in the plated wires during the word current transients and are amplified by the sense amplifiers. The leading edge transient of the word current is controlled to effect the widest useable "window" in the sense amplifier output. The amplifier outputs are used as steering inputs to buffer storage registers. The polarity depends on the state of the information previously 'written into' the plated wire.

The information "read out" during the turn-on transient of the word current is clocked into the buffer register by the strobe. The strobe is generated by a level detector in the current generator. This minimizes possible uncertainties in strobe position.

The read-complete signal is initiated when the data is clocked into the buffer register. It is maintained for a minimum of 250 nanoseconds and a maximum of 450 nanoseconds. Output data is maintained in the buffer register for at least 150 nanoseconds after termination of the read complete signal. At the end of this time the read cycle is complete and internal power is switched off.

The data and read complete sources are Series 54 open collector logic elements. A low impedance (i.e., output transistor on) denotes the active level for the read complete line and a logic zero on the data lines. The only time the low impedance condition will exist on a data line is during the actual read-out of a bit 0.

3.4 ELECTRICAL PARTS

High-Rel, screened parts were used in construction of the memory. Six pieces of each electronic device were submitted to GSFC for evaluation.
3.4.1 Logic Circuits

Series 54 TTL integrated circuit logic elements were used throughout the memory. These were procured per vendor High-Rel specification SNC which is MIL-STD-883, Class B.

3.4.2 Discrete Parts

Two types of established reliability resistors were used in the memory; the RCRXXG Composition and the RNR55C metal film. The RCRXXG were procured to S failure-rate levels and the RNR55C were procured to R failure-rate levels.

Three types of capacitors were used; the CSR 13 style established reliability tantalum with failure rate of R or lower, the CKR06 style, established reliability ceramic with failure rate of R or lower, and the CM series cap per MIL-C-5/18 with additional screening. Transistors and diodes were either purchased as JAN TX parts or screened to JAN TX equivalent per the documents indicated in the parts control list.
3.4.3 Transformer

A single rf transformer was used in the memory for coupling the word current from the generator to the memory stack. The transformer was fabricated in-house to the requirements of MIL-C-15305, Type LT6K, with temperature cycling per MIL-STD-202, Method 102, Condition C, except 10 cycles at \(-55^\circ\text{C}\).

3.4.4 Sense Amplifier

The four-channel sense amplifier (SC 12200 FB2) is shown in Figure 10. The input terminating resistors are external to the package.

3.4.5 Hybrid Circuits

Six different hybrids are used in the memory. These are custom circuits manufactured in-house and screened to meet the requirements of this program. Each of these circuits is described briefly in the following paragraphs.

3.4.5.1 Delay Circuit

The delay circuit is shown, functionally, in Figure 11. Only the high-to-low transition at the input is delayed at the output, with both the true and complement outputs available. The delay is adjustable from a minimum of approximately 25 nanoseconds to a maximum of several microseconds.

3.4.5.2 Word-Line Selection Circuits

The word-line selection circuits are shown in Figures 12 and 13. A particular switch is closed by grounding the corresponding selection input. The first and second level switches are packaged together. A particular package contains one first level switch and two banks of four second level switches each. Each of four second level selection inputs controls one switch in each bank. A single selection input controls the first level switch. The pin-outs are configured so that a first level switch can be connected to a second level bank in a different package, as well as to a bank in its own package.

3.4.5.3 Digit Driver

The digit driver is shown in Figure 14. Basically, it consists of two current sources with steering such that, depending on the logic inputs, one of the sources may be enabled to conduct current through the load in a particular direction. The \(T_1\) and \(T_2\) inputs denote successive time periods for the two opposite phases of digit current. The \(D\) and \(\bar{D}\) inputs denote the true and complement levels of an input data bit. If \(D\) is true, then current will flow in the direction indicated during \(T_1\) and in the opposite direction during \(T_2\). The current flow would be opposite if \(\bar{D}\) were true.
Figure 10. Four-Channel Sense Amplifier, Functional Diagram
3.4.5.4 Power Switches

Two types of power switches are used in the memory. One type provides two independently controlled logic level (i.e., +5.0 V) outputs from the primary +5 V input. The other type provides two sets of +5.0 V and -6.1 V outputs from the corresponding inputs. Each set is controlled independently. The switches themselves consume no power when in the OFF state. The switches perform no regulation. They are shown functionally in Figures 15 and 16.

3.5 MECHANICAL DESIGN

3.5.1 Stack Design

The plated wire memory stack used in the LP RASM used a standard Motorola plane design for spaceborne memories developed to high reliability, quality assurance, and workmanship standards. The primary design goal of the stack was simplicity of fabrication combined with high reliability. The number of solder joints and plated through holes are minimized to accomplish this end. The stack consists of eight planes arranged and interconnected to meet the specific requirements of the LP RASM. Specific details of stack construction are described below.
Figure 12. Custom Package and Layout
Figure 13. Word-Line Selection Matrix, Functional Diagram
Figure 14. Digit Driver, Functional Diagram
Figure 15. Power Switch +5V/-6V

Figure 13. Power Switch +5V/+5V
The tunnel structure, the heart of the memory plane, contains the word lines and the plated wire which stores the bits of data. The plated wires are installed in 0.007 diameter tunnels on 0.025 centers in a polyimide-FEP tunnel matt. The tunnel matt is constructed by forming the FEP (between the polyimide film) around dummy wires at controlled temperature, pressure and wire tension. After complete assembly processing the dummy wires are removed and the plated wire is installed in the tunnel.

Word lines of etched copper on glass epoxy board are laminated to each side of the tunnel matt so that they are perpendicular to the tunnels (plated wire). The word lines are double turn (twice around the wires per line). Their mechanical configuration is 0.010 wide conductor, an intervening 0.005 space and another 0.010 conductor, all on repetitive 0.050 centers. Plated-thru holes at each end of the tunnel matt creates the double turn word lines.

Each carrier structure contains 64 word lines and 100 bit lines (Plated wire tunnel pairs). To provide the desired storage capacity for the LP RASM only 72 tunnel pairs are populated (plated wire installed).

Keepers, of high magnetic permeability and processed with extreme care, are bonded to the outer surface of the glass epoxy board which support the word lines to contain the word line field and shield against external magnetic fields. The tunnel matt and word lines are carefully fabricated and then laminated into a subassembly using multilayer printed wiring board techniques. The keepers are then laminated using similar techniques. A cross section of the tunnel structure is shown in Figure 17.

The memory plane is fabricated by laminating two tunnel structures to each side of a motherboard. The motherboard is a two-sided printed wiring board which has a ground plane laminated in the center. The input and return for the matrix is tracked to the edge of the board where pc board interconnect is used to interface with the plane. Two tunnel structures per plane provide 128 word x 72 bit capacity. Installation of the 8 word-drive flat packs per side, by lap soldering, completes the memory plane subassembly. Memory plane construction is shown in Figure 18.

The memory stack consists of eight memory planes electrically and mechanically integrated into one unit to provide 1024 words x 72 bits of storage. The digit lines of each plane are interconnected with flat flexible circuitry bonded to the motherboard which permits the stack to be opened as necessary during assembly and rework. The plated wire is formed like a "hairpin" and installed into the top and bottom carrier structure (similar to a trombone slide). The two ends of the plated wire are lap soldered directly to the conductor of the interconnecting flex cable. This approach for installing the plated wire minimizes the number of solder joints required while providing the required stress relief.

PC board interconnect with miniature connectors (see Figure 2) is used to interconnect common word drive signals from plane to plane and carry all digit and word signals to the electronics. The use of printed circuitry interconnect provides controlled impedance and line characteristics. The connectors allow the stack to be connected/disconnected from the electronics with minimum effort.
During assembly, spacers are installed at each tie-down location on the planes to precisely position the planes relative to each other in the stack. The tie-downs are located to provide maximum stability under dynamic conditions.

3.5.2 System Packaging

The 4k x 18 bit Low Power Random Access Spacecraft Memory developed by Motorola consisted of a 1k by 72 plated wire stack, two digit drive/sense electronics boards and a timing/control/word drive board, all contained in an aluminum or magnesium housing.

The concept of stacking the electronics boards in the same manner as the planes was used in the complete memory package. The timing/control/word drive board is located on top of the plated wire stack while the two digit drive/sense boards are located below the plated wire stack. This arrangement eliminates interference between signals as the digit line interconnects leave the plated wire stack in one direction while the word lines go the other direction.
The size of the memory plane (i.e., number of word lines, digit lines, required structural mounting and word drive matrix area) determine the "plan view" size of the system package. The basic plane size is 8.05" long x 4.38" wide and contains 8 tie-down screws. The electronics boards have the same mounting tie-down locations and length as the plane but are 5.0" wide.

Mechanically, each of the electronic boards are essentially identical. Each consists of a printed wiring board to which flat pack integrated circuits (Motorola plated wire hybrids or conventional logic) are lap soldered and a few discrete components are mounted. The digit boards contain the digit drivers, sense amplifiers, data input buffers and data output registers. The third board contains the timing and control logic and the transistor word drive select electronics.

After the boards are assembled, a thin conformal coating is applied to the board assembly. This coating provides protection in a high humidity environment, protection against shorting across components and a vibration damping effect on the boards. This provides an encapsulated assembly that is easily disassembled for servicing or repair.

Flat flexible cable is used for interconnecting between board assemblies. The flex interconnect is arranged so the plated wire stack and printed wiring boards can be assembled in the system stack (described previously) or opened out to provide access for testing or troubleshooting of the boards, the stack or the system. The connection to the external connector is a conventional hard wire harness.

The plated wire stack and electronics boards are assembled by stacking them into a single unit and installing them in a housing. Spacers are provided between the boards and the stack at the tie down locations to position them with respect to each other. Eight special high-strength screws pass through the spacers and secure the system in the housing.

The system assembly is contained in a single protective housing which was machined from AZ 31B magnesium material and shipped to GSFC for gold plating. The memory housing is 8.6" long x 6.3" wide x 2.9" high (exclusive of mounting flanges and connectors) establishing a volume of 157 cubic inches. The system has a total weight of 5.80 pounds.

3.5.3 Materials

Motorola’s basic memory system design uses materials that meet the requirements of high reliability spaceborne hardware, particularly in the area of environment, outgassing and compatibility with other materials in the spacecraft. Materials are used that were approved on the Mariner '71 subsystems which Motorola designed and fabricated and have since been proven by the success of the mission. These materials were also used on the two memories previously delivered to GSFC under contract No. NAS 5-23163 with the exception of an adhesive used in the fabrication of the memory planes which was changed to facilitate manufacturing. This adhesive has been tested and approved for use by GSFC.
SECTION 4
TESTING

4. GENERAL

Comprehensive testing was performed on the memory and its subassemblies at each level of assembly.

4.1 SYSTEM LEVEL TESTING

Acceptance tests were conducted at the system level. Acceptance testing included complete functional tests at temperature extremes of +85°C and -40°C. The acceptance test procedure and test data records are included as an Appendix. Acceptance ambient temperature functional tests were repeated after environmental testing.

Environmental testing consisted of both sine and random vibration, shock, and vacuum (to \(10^{-5}\) mm Hg). The memory unit was continuously exercised with a worst case pattern during all environmental testing.

4.2 MEMORY STACK TESTING

A 100 percent on-line test was performed on the plated-wire during manufacture under relatively severe test patterns and word/digit current variations.

In addition to the on-line wire test, the memory stack was subjected to comprehensive worst case test patterns at the stack level using an EII 8500 computer controlled stack tester. Tests performed include adverse history being hard written in 1000 times and then the opposite polarity being written one time and immediately read out. Also adjacent bits are written into 10,000 times at the opposite polarity of the bit under test and then the bit under test is read out to test the effects of adjacent bit disturbs.

Any wire which did not meet the minimum output level requirements was replaced and the unit retested.

4.3 HYBRID CIRCUIT SCREENING

All hybrid microcircuits used in the memory were subjected to extensive, 100-percent screening to criteria based on MIL-STD-883 criteria. In addition to comprehensive electrical tests at temperature extremes, these tests included pre- and visual inspection, centrifuge, operational vibration, stabilization bake, thermal cycling, power aging, and leak testing.
ATTACHMENT I

ACCEPTANCE TEST PROCEDURES
LOW POWER RANDOM ACCESS
SPACECRAFT MEMORY
PART NO. 01-P13701D
(35 PAGES)
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<td>2.</td>
<td>REFERENCE INFORMATION</td>
<td>3</td>
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<td>12.</td>
<td>FINAL FUNCTIONAL TESTS</td>
<td>30</td>
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</tbody>
</table>
1. **SCOPE**

This procedure and the test data sheet (12-P11216B) define the unit acceptance requirements for the Low Power Random Access Spacecraft Memory, Motorola Part No. 01-P13701D, manufactured under Contract No. NAS 5-23163.

2. **REFERENCE INFORMATION**

2.1 **SPECIFICATIONS APPLICABLE**

- **S-562-P-24** Low Power Random Access Spacecraft Memory.
- **12-P13721D** Test Data Record
- **12-P11173B** Motorola Plated Wire Memory Tester Operating Manual.

2.2 **DEFINITIONS**

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>UP position on DATA and ADDRESS switches. DATA and ADDRESS lamps ON</td>
</tr>
<tr>
<td>0</td>
<td>DOWN position on DATA and ADDRESS switches. DATA and ADDRESS lamps OFF</td>
</tr>
<tr>
<td>Tester</td>
<td>Motorola Plated Wire Memory Tester</td>
</tr>
<tr>
<td>MSB</td>
<td>Most Significant Bit</td>
</tr>
<tr>
<td>LSB</td>
<td>Least Significant Bit</td>
</tr>
<tr>
<td>Error Lamps</td>
<td>Lamp ON indicates ERROR present.</td>
</tr>
</tbody>
</table>
3. TEST EQUIPMENT AND ENVIRONMENTAL REQUIREMENTS

3.1 TEST EQUIPMENT

The calibrated test equipment listed below, or its equivalent, will be required to perform this test procedure. Any equipment used as an equivalent to that listed below shall be recorded in the data sheet.

### STANDARD TEST EQUIPMENT

<table>
<thead>
<tr>
<th>ITEM</th>
<th>MANUFACTURER</th>
<th>MODEL OR TYPE</th>
<th>ACCURACY</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC Milliammeter</td>
<td>Hewlett Packard</td>
<td>428B</td>
<td>0-10 Amp.</td>
</tr>
<tr>
<td>Oscilloscope</td>
<td>Tektronix</td>
<td>585</td>
<td>50ns/cm</td>
</tr>
<tr>
<td>Scope Plug-In</td>
<td>Tektronix</td>
<td>82</td>
<td>Tr 1.5ns</td>
</tr>
<tr>
<td>Digital Voltmeter</td>
<td>Hewlett-Packard</td>
<td>3440A</td>
<td>Accuracy ± .05% of reading</td>
</tr>
<tr>
<td>Counter</td>
<td>CMC</td>
<td>727BN</td>
<td>0.1% ± 1/2 LSB</td>
</tr>
<tr>
<td>DC Multifunction Unit</td>
<td>Hewlett-Packard</td>
<td>3444A</td>
<td>0-999.9 ma.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0-9.999 megohms</td>
</tr>
<tr>
<td>Oven</td>
<td>Wyle</td>
<td>CO-106-1800</td>
<td>-100°F to +500°F</td>
</tr>
<tr>
<td>Power Supplies</td>
<td>Precision Design Inc</td>
<td>5015-A</td>
<td>0-50V, 1.5 Amp.</td>
</tr>
<tr>
<td>Power Supplies</td>
<td>Precision Design Inc</td>
<td>5015-S</td>
<td>0-50V, 1.5 Amp.</td>
</tr>
<tr>
<td>Pulse Generator</td>
<td>EH</td>
<td>139B</td>
<td>10Hz to 50MHz</td>
</tr>
</tbody>
</table>
**NON-STANDARD TEST EQUIPMENT**
(NO CALIBRATION REQUIRED)

Motorola Plated Wire Memory Tester 01-P11170B001

**NOTE:**
The Motorola Plated Wire Memory Tester supplies inputs to the memory under test from SN5400 series logic and presents a single unit load of SN5400 logic on the memory output lines.

Motorola Tester Interface Box T-5909

**NOTE:**
The Interface Box puts a 51 ohm resistor in series with all of the signals going to the memory and provides a 1K pull-up resistor to signals coming back from the memory.

**ENVIRONMENTAL TEST EQUIPMENT**

<table>
<thead>
<tr>
<th>ITEM</th>
<th>MANUFACTURER</th>
<th>MODEL NO.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vibration Tester</td>
<td>LING</td>
<td>275</td>
</tr>
<tr>
<td>Vacuum Chamber</td>
<td>NRC</td>
<td>2707</td>
</tr>
<tr>
<td>Shock Tester</td>
<td>MRL</td>
<td>2424</td>
</tr>
<tr>
<td>Vibration Test Fixture</td>
<td>MOT</td>
<td>—</td>
</tr>
</tbody>
</table>

**3.2 TEST CONDITIONS**

Unless otherwise specified all tests shall be performed under the following conditions.

**3.2.1 Power Supply Voltage**

The unit specified to be tested shall operate from the following DC source voltages:

- $+5.0V \pm 5\%$
- $-6.1V \pm 5\%$
3.2.2 Ambient Temperature
The unit shall be tested in a laboratory area having a temperature of +25 ± 10°C (77 ± 18°F).

3.2.3 Ambient Humidity
Normal laboratory ambient, not to exceed 90%.

3.2.4 Ambient Atmospheric Pressure
Normal laboratory ambient.

3.2.5 Stabilization Period
The test equipment shall not be used to conduct tests until after a minimum warm-up period of 15 minutes.

4. TEST SCHEDULE
The testing to be performed on each memory unit is as follows:

1. Physical Characteristics (Weight and Dimensions).
3. Operational Tests at Temperature Extremes.
4. Operational Vacuum Tests
5. Operational Vibration Tests
6. Operational Shock Tests
7. Final Functional Tests

Tests 3 through 6 may be performed in any sequence.
TEST RECORDS

5.1 TEST LOG

The Test Log shall be used to record the history of the memory, starting from the first system test. The log shall reference all testing, rework and idle time for the particular memory unit.

5.2 DATA RECORD

All test results shall be recorded in the Test Data Record, Motorola Document No. 12-P13721D.

6. PHYSICAL CHARACTERISTICS

6.1 WEIGHT

Place the LP RASM on the scale and read and record, in the data sheet, the weight of the memory, in pounds.

6.2 DIMENSIONS

Measure and record, in the data sheet, the outside dimensions as shown in Figure 1. Compute and record, in the data sheet, the memory volume by multiplying dimension W by dimension H by dimension D. \((V = W \times H \times D)\).

7. INITIAL FUNCTIONAL TESTS

7.1 INTERCONNECTION

Record connector mate/demate history according to IUE connector log requirements.

At the Interface Box, set memory power to OFF. Connect the unit under test as shown in Figure 2, except that the Interface Box will not be connected to the Plated Wire Memory Tester. The
connections are all labeled on the Interface Box.

Turn the coarse voltage controls fully counterclockwise and turn on power to all electrical test equipment.

Using the scope, adjust the Pulse Generator for $+3 \pm 0.1V$ positive pulses of $450 \pm 10$ nanosecond duration (at the 50 percent points) at a $500 \pm 1.0$ KHz rep rate. (Use the counter to adjust the rep rate). The pulse generator output must be terminated in 50 ohms and connected to the tester when making these adjustments.

Normal precaution shall be taken to ensure that the equipment is not dropped or damaged in any way while it is being handled, or while the connectors are being engaged.

7.2 PRELIMINARY CONTROL SETTINGS

Set the Tester and Interface Box controls as follows and maintain these control settings unless otherwise directed in the individual tests.

<table>
<thead>
<tr>
<th>CONTROL</th>
<th>SETTING</th>
</tr>
</thead>
<tbody>
<tr>
<td>TESTER</td>
<td></td>
</tr>
<tr>
<td>BD1-BD4 (24 Switches)</td>
<td>Up</td>
</tr>
<tr>
<td>Tape Reader Power</td>
<td>Light Off</td>
</tr>
<tr>
<td>Run-Off-Rewind Switch</td>
<td>OFF</td>
</tr>
<tr>
<td>Tester Power</td>
<td>Light On</td>
</tr>
<tr>
<td>Address Switches</td>
<td>Down</td>
</tr>
</tbody>
</table>
CONTROL

TESTER (Cont.)

<table>
<thead>
<tr>
<th>CONTROL</th>
<th>SETTING</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Switches</td>
<td>UP</td>
</tr>
<tr>
<td>READ/WRITE</td>
<td>WRITE</td>
</tr>
<tr>
<td>Word Length</td>
<td>24</td>
</tr>
<tr>
<td>READ 1/ READ 7 Switch</td>
<td>READ 1</td>
</tr>
<tr>
<td>Address Pattern</td>
<td>SEQ.</td>
</tr>
<tr>
<td>Data Pattern</td>
<td>MAN</td>
</tr>
<tr>
<td>Frequency</td>
<td>EXT.</td>
</tr>
</tbody>
</table>

INTERFACE BOX

<table>
<thead>
<tr>
<th>INTERFACE BOX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory Select Switches</td>
</tr>
<tr>
<td>Input Current Switch</td>
</tr>
<tr>
<td>Output Pullup Resistor</td>
</tr>
<tr>
<td>WC Switch</td>
</tr>
<tr>
<td>Initiate Pulse Switch</td>
</tr>
<tr>
<td>WC2 Switch</td>
</tr>
<tr>
<td>Memory Power</td>
</tr>
</tbody>
</table>

7.3 INITIAL POWER SUPPLY CONDITIONS

Using the DVM, adjust the three supplies as follows:

- +5V to Interface Box: +5.0V ± 0.1V
- +5V to Memory: +5.0 ± 0.1V
- -6.1V to Memory: -6.1 ± 0.1V
Set the motor selection switches to measure current and leave them in this position. Disconnect the output side of all three power supplies from the Interface Box.

All subsequent mention of +5V in the procedure refers to memory power unless otherwise specified.

7.4 CHASSIS ISOLATION

Using the digital ohmmeter verify that the impedance between the memory chassis and ground test point on the interface box is ≥ 9 megohms. Record the results in the Data Sheet.

7.5 INPUT SIGNAL LOADING

7.5.1 Connect the two +5V supplies to the Interface Box. (If the Interface Box supply overloads, reset it by turning its power off and back on).

7.5.2 Remove the jumper wire from the INT PULSE test point. Connect the digital ammeter between the INT PULSE and INT PULSE SW test points. Momentarily turn the MEMORY POWER switch to ON and measure and record the current. Set the INT PULSE switch to the +2.4V position. Momentarily set the memory power switch to ON and again measure and record the current. Disconnect the ammeter and connect the jumper wire between the INT PULSE and INT PULSE SW test points.

7.5.3 Replace the jumper from the MEMORY SELECT 1 test point to the MEMORY SELECT 1 SWITCH test point with the digital ammeter. Momentarily set MEMORY POWER to ON and measure and record the current. Set the MEMORY SELECT 1 SWITCH to the GND position.
Momentarily set MEMORY POWER to ON and measure and record the current.

Disconnect the ammeter and replace the jumper wire. Set the MEMORY SELECT 1 SWITCH back to the +2.4V position.

Repeat paragraph 7.5.3 for MEMORY SELECT 2, MEMORY SELECT 3, and MEMORY SELECT 4.

Connect the ammeter from the READ/WRITE test point to the INPUT CURRENT SWITCH test point. Set the Initiate Pulse Switch to 2.4V. Momentarily set the memory power switch to ON. Measure and record the current. Move the INPUT CURRENT SWITCH to the +2.4V position. Momentarily set the MEMORY POWER switch to ON and measure and record the current. Return the INPUT CURRENT SWITCH to the GND position.

Connect the ammeter between the ADDRESS BIT 20 and the INPUT CURRENT test points. Momentarily set the MEMORY POWER switch to the ON position and measure and record the current.

Set the INPUT CURRENT SWITCH to the +2.4V position. Momentarily set the MEMORY POWER switch to the ON position and measure and record the current. Set the INPUT CURRENT SWITCH back to the GND position.

Repeat the above two measurements at each of the 12 address bit test points. Connect a jumper between the R/W and GND test points. Repeat the above two measurements at each of the 18 DI test points (i.e. with the ammeter conn. between a DI test point and the INPUT CURRENT test point).
Verify that the MEMORY POWER switch is OFF. Remove the jumper from the R/W test point and install the jumper from the INT PULSE test point back in its original position.

7.6
VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS.

7.6.1 Connect the Interface Box to the tester. Connect the -6.1V power supply to the Interface Box. At the tester, depress the STOP and RESET pushbuttons. Set the initiate pulse SW to pulse position.

7.6.2 Turn the MEMORY POWER switch ON and push the START button on the tester. The tester will write a "1" in all data bits in all 4096 addresses one time and stop.

7.6.3 Set the READ/WRITE switch on the tester to the READ position. Push the tester START button. Using the Dual Trace of the oscilloscope, measure and record in the data sheet the voltage at the READ COMPLETE test point 150 ns after the leading edge of the pulse at the INITIATE PULSE test point. The voltage shall be ≤100 mv. Disregard errors.

(The road complete output for this test and the data outputs for the next test are terminated with a 1K resistor to GND).

7.6.4 Measure and record in the data sheet the voltage at each of the 18 data output lines that occurs 500 ns after the leading edge of the Initiate Pulse. The voltage shall be ≤100 mv. Push the tester stop button. Set the OUTPUT PULLUP RESISTOR switch to the +5V position.
7.7 POWER CONSUMPTION

7.7.1 Using the DVM, adjust the +5V and -6.1V memory power supplies to +5.0 ± 0.1V and -6.1 ± 0.1V, respectively. Record the voltages.

Using the 428B milliammeter, measure and record the current from the +5V memory supply. Compute and record the +5V power.

7.7.2 Using the milliammeter, measure and record the current to the -6.1V supply. Compute and record the -6.1V power.

7.7.3 Compute and record the total Memory Idle Power.

7.7.4 Set the DATA PATTERN switch to SEQ. and momentarily depress the RESET and START buttons. The tester should be cycling through memory addresses.

7.7.5 Repeat 7.7.1.

7.7.6 Repeat 7.7.2.

7.7.7 Compute and Record the Total Active Power. Momentarily depress the tester stop pushbutton.

7.8 READ COMPLETE TIMING

7.8.1 Connect the oscilloscope as follows; trigger input jack to the INITIATE PULSE test point, channel A voltage probe to the INITIATE PULSE test point and the channel B voltage probe to the READ COMPLETE test point.

7.8.2 Set the DATA PATTERN switch to MAN, READ/WRITE switch to READ, and tester BD1 switch 0 to the up position.

7.8.3 Depress and release the RESET button, then the START button.

7.8.4 Synchronize the oscilloscope on the leading edge of the initiate pulse.
7.8.5 The read complete pulse shall be a negative pulse and shall be generated 500 nanoseconds maximum after the leading edge of the initiate pulse and the duration shall be 250 ns minimum and 450 ns maximum. (All timing relationships shall be measured at the 50% points). Record the pulse delay and duration in the data sheet.

7.8.6 Momentarily depress the STOP button and set the READ/WRITE switch to WRITE. Set all data switches to the down position. Depress and release the RESET button, then the START button. Set the READ/WRITE switch to READ and momentarily depress the START switch.

7.8.7 Connect the scope channel A voltage probe to the first data output line test point (DO-0). The high-to-low transition on the data output line shall occur prior to (or in coincidence with) the leading edge of the read complete pulse. The low-to-high transition of the data output line shall occur no earlier than 150 nanoseconds following the trailing edge of the read complete pulse. (All timing relationships shall be measured at the 50 percent points). Record the results.

7.8.8 Repeat the measurements of 7.8.7 at each of the remaining 17 data output line test points. Record the results.

7.9 SYSTEM FUNCTIONAL TESTS

7.9.1 Depress and release the RESET button. Set the ADDRESS PATTERN switch to SEQ. Adjust the pulse generator frequency to 600 ± 1.0 KHz.

Set the DATA PATTERN switch to SEQ.
7.9.2 Depress and release the START button. The tester will then begin cycling through all memory locations. It steps to the first address, writes a "0", reads a "0", writes a "1" and reads a "1" in all bits in that address word, then steps to the next address, etc. The tester continues this cycle unless an error occurs. Test for 2 minutes and record any errors. Depress the STOP button.

7.9.3 Set the READ 1/READ 7 Switch to the READ 7 position. The READ 7 mode causes the tester to write a "0", read a "0" seven times, write a "1", and read a "1" seven times in each memory location.

7.9.4 Depress and release the START button. The Tester will continue to cycle unless an error occurs. Test for 2 minutes and record any errors.

7.9.5 Depress and release the STOP button. Set the DATA PATTERN switch to MAN and the READ/WRITE switch to WRITE. Set all DATA switches to the DOWN position.

7.9.6 Depress and release the RESET button and then the START button.

7.9.7 Set all DATA switches to the UP position.

7.9.8 Depress and release the RESET button and then the START button.

7.9.9 Set the READ/WRITE switch to READ. Depress and release the RESET button.
7.9.10  Depress and release the START button. Test for one minute. Record any errors.
7.9.11  Depress and release the STOP button.
7.9.12  Set the READ/WRITE switch to WRITE.
7.9.13  Set all DATA switches to the DOWN position. Depress and release the RESET button.
7.9.14  Depress and release the START button. The memory will cycle thru all 4096 addresses one time and stop.
7.9.15  Set the READ/WRITE switch to READ. Depress and release the RESET button.
7.9.16  Depress and release the START button. Run for one minute. Record any errors.
7.9.17  Depress and release the STOP button.
7.10 RANDOM ACCESS CAPABILITY

7.10.1 Set the READ/WRITE switch to WRITE and the ADDRESS PATTERN switch to MAN.

7.10.2 Select an address at random with the ADDRESS switches.

7.10.3 Set the DATA switches in a random pattern. Depress and release the RESET button.

7.10.4 Depress and release the START button. The selected data will be written into the selected address.

7.10.5 Depress and release the Stop button. Set the READ/WRITE switch to READ.

7.10.6 Depress and release the START button. The data in this address location will be read out. If an error occurs, note this in the data sheet.

7.10.7 The operator should select 3 other addresses at random, repeating steps 7.10.2 through 7.10.6 to verify the random access capability.

7.11 NON-VOLATILITY TEST

7.11.1 Set the ADDRESS PATTERN switch to SEQ and the DATA PATTERN switch to MAN.

7.11.2 Set the DATA switches to a random pattern. Depress and release the RESET button. Set the READ/WRITE switch to WRITE.

7.11.3 Depress and release the START button. The tester will run through all 4096 addresses one time and then stop. Set the READ/ WRITE switch to READ.

7.11.4 Turn memory power to OFF.
7.11.5 Depress and release the RESET button.

7.11.6 Turn memory power to ON.

7.11.7 Depress and release the START button. If any errors occur, record them on the data sheet. If no errors occur, no words were disturbed when the power was interrupted.

7.11.8 Depress and release the STOP button.

7.11.9 Repeat 7.11.4 through 7.11.8 four times. Record any errors.

7.12 MEMORY SELECT TEST

7.12.1 Set the ADDRESS PATTERN switch to SEQ and the DATA PATTERN switch to SEQ. Set the No. 0 switch on BD1 to the down position.

7.12.2 Set the MEMORY SELECT switches to 0000.

7.12.3 Depress and release the RESET button, then the START button. The tester should indicate an error at the first address. Record this address on the data sheet.

7.12.4 Repeat 7.12.3 with the memory select switches set to 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110.

7.12.5 Set the MEMORY SELECT switches to 1111.

7.12.6 Set the No. 0 switch on BD1 to the UP position. Depress and release the RESET button, then the START button. Allow the tester to run for 2 minutes. Record any errors. Depress and release the STOP button.
7.13 WORST CASE PATTERN TEST

7.13.1 Set the DATA PATTERN switch and the ADDRESS PATTERN switch to WCl. Turn the WC switch ON. Depress and release the STOP and RESET buttons.

7.13.2 Depress and release the START button. The tester will execute the following sequence:

A. Write a "1" in every bit of every word $2^{10}$ times.
B. Write a "0" once in every bit of every word under an even numbered word line in the stack.
C. Write a "1" in every bit of every word under an odd numbered word line and read the previously written "0" in every bit of every word under an even numbered word line until the operator sequences to the next group or until an error is detected. The READ light is lit during this cycle.

NOTE: If any error lights are ON when cycle C starts, disregard them and depress RESET one time prior to starting the one minute count. This applies to all worst-case pattern tests.

Run in cycle C for two minutes. Record any errors on the data sheet.

7.13.3 Press and release the WCl SEQ button. The tester will execute the preceding sequence, except "even" and "odd" are interchanged. The WC$^0$ and WC$^1$ lights will indicate the second WCl group is under test. Record any errors.
7.13.4 Repeat 7.13.3 for WC1 groups 3 and 4 in which "1" and "0" are interchanged. Record any errors on the data sheet.
Depress and release the STOP button. Turn the MEMORY POWER to OFF.

8. TEMPERATURE TEST
The temperature tests shall be conducted under normal laboratory conditions, with the exception of temperature.

8.1 TEST SETUP
Place the unit in the temperature chamber and establish the test setup as shown in Figure 3.

8.2 LOW TEMPERATURE
Place the memory unit in a plastic bag and seal the chamber.

8.2.1 Decrease the chamber ambient temperature to -40°C ± 3°C. When the chamber has reached this temperature, note the time.

8.2.2 Beginning 150 minutes after the chamber temperature has reached -40°C, measure and record the thermistor resistance at 10 minute intervals. At each measurement, except the first one, calculate the percent change from the previous reading. When the change is less than 5 percent turn off the chamber and proceed to paragraph 8.2.3.

8.2.3 Depress the START button. The memory shall run without error for 2 minutes. Depress the STOP button and record the results.
Turn on the chamber and set the +5V supply to 5.25V ± 0.2V and the -6.1V supply to -6.40 ± 0.02V. Measure and record the power supply volt and the standby power (paragraphs 7.7.1 through 7.7.3, except do not readjust the voltages). Set the READ 1/READ 7 Switch to READ 1.

Adjust the pulse generator frequency to 500 ± 1.0 KHz. Set the DATA PATTERN and ADDRESS PATTERN switches to SEQ. Push the START pushbutton. Measure and record, in the data sheet, the operating power (paragraphs 7.7.5 through 7.7.7, except adjust the voltages to +5.25 ± 0.02V and -6.40 ± 0.02V).

Adjust the pulse generator frequency to 600 ± 1.0 KHz. Set the READ 1/READ 7 Switch to READ 7. Set the +5V supply to +4.75 ± 0.02V and the -6.1V supply to -5.80 ± 0.02V. Turn off the chamber and push the RESET pushbutton. The memory shall run without error for two minutes. Depress the STOP button. Record the results in the data sheet. Set the READ 1/READ 7 Switch to READ 1. Push the START button and readjust the voltages to 4.75 and -5.8. Push STOP.

Turn on the chamber and allow it to cool for 5 minutes. Then turn off the chamber and proceed to paragraph 8.2.8.

Repeat paragraph 7.13.1 through 7.13.4.

Set the MEMORY POWER switch to ON. Depress and release the START button. Using the DVM, adjust the memory power supplies to +5.25 ± 0.02V and -6.40 ± 0.02V. Depress the STOP button.

Turn on the chamber and allow it to cool for 5 minutes. Then turn off the chamber and proceed to paragraph 8.2.11.
8.2.11 Repeat paragraphs 7.13.1 through 7.13.4.

8.3 INTERMEDIATE TEMPERATURE TEST
Set the chamber HEAT SELECTOR to the 375W position and the temperature to +85°C. Record the time.

8.3.1 Push the Reset and START buttons. Using the DVM, adjust the memory power supplies to +5.0 ± 0.2V and -6.1V ± 0.02V. Depress the STOP button.

8.3.2 At 10 minute intervals record the thermistor resistance and repeat paragraphs 7.13.1 thru 7.13.4 except that each test will be run for 1 minute.

NOTE: When the thermistor indicates the internal temperature of the MEMORY is between 0°C and 15°C open the chamber and remove the plastic bag from the memory. Reseal the chamber.

Testing may be discontinued when the THERMISTOR indicates +75°C.

8.3.3 When the chamber temperature reaches +85°C ± 3°C record the time on the data sheet.

8.4 HIGH TEMPERATURE
Beginning 50 minutes after the temperature chamber has reached 85°C measure and record the thermistor resistance at 10 minute intervals.
8.4 (cont.)
At each measurement except the first one calculate the percentage change from the previous reading. When the change is less than 5 percent, proceed to paragraph 8.4.1.

8.4.1 Set the ADDRESS PATTERN and DATA PATTERN switches to SEQ. Turn the MEMORY POWER to ON. Using the DVM, adjust the memory power supplies to $+5.25 \pm 0.01V$ and $-6.40 \pm 0.02V$. Measure and record the power supply voltage, current and standby (idle) power (paragraphs 7.7.1 through 7.7.3, except do not readjust the voltages). Set the READ 1/READ 7 Switch to READ 7.

8.4.2 Depress the START button. The memory shall run without error for 2 minutes. Record the results. Set the READ 1/READ 7 Switch to READ 1.

8.4.3 Adjust the pulse generator frequency to $500 \pm 1.0$ KHz. Measure and record the operating power (paragraphs 7.7.5 through 7.7.7, except adjust the voltages to $+5.25 \pm 0.02V$ and $-6.40 \pm 0.02V$). Depress the STOP button. Adjust the pulse generator frequency to $600 \pm 1.0$ KHz.

8.4.4 Repeat paragraphs 7.13.1 through 7.13.4.

8.4.5 Set the MEMORY POWER switch to ON. Depress and release the START button. Using the DVM, adjust the memory power supplies to $+4.75 \pm 0.02V$ and $-5.80 \pm 0.02V$. Depress the STOP button.

8.4.6 Repeat paragraphs 7.13.1 through 7.13.4.
8.4.7 Set the MEMORY POWER switch to ON.
Set the +5V supply to 5.0V ± .02 and the -6.1V and to -6.1 ± .02V. Set the DATA PATTERN switch to MAN and the ADDRESS PATTERN switch to SEQ. Set the READ/WRITE switch to WRITE. Select a random pattern and push the START pushbutton. The tester will write the data once in each of the 4096 addresses and stop. Set the READ/WRITE switch to READ and push the START pushbutton. The memory shall run without error. After 2 minutes, push the STOP button. Record the results. Set MEMORY POWER to OFF.

9. VACUUM TEST

9.1 SETUP

9.1.1 Verify that the MEMORY POWER switch on the Interface Box is in the OFF position. Turn the voltage controls fully counterclockwise on all three power supplies. Connect the equipment as shown in Figure 3. Turn on power to all memory associated test equipment.
9.1.2 Set the Tester and Interface Box controls as follows and maintain these control settings unless otherwise directed in the individual tests.

**CONTROL**

<table>
<thead>
<tr>
<th>TESTER</th>
</tr>
</thead>
<tbody>
<tr>
<td>BD1-BD4 (24 Switches)</td>
</tr>
<tr>
<td>Tape-Reader Power</td>
</tr>
<tr>
<td>Run-OFF-Rewind Switch</td>
</tr>
<tr>
<td>Tester Power</td>
</tr>
<tr>
<td>ADDRESS Switches</td>
</tr>
<tr>
<td>DATA Switches</td>
</tr>
<tr>
<td>READ/WRITE</td>
</tr>
<tr>
<td>WORD LENGTH</td>
</tr>
<tr>
<td>READ 1/READ 7 Switch</td>
</tr>
<tr>
<td>ADDRESS PATTERN</td>
</tr>
<tr>
<td>DATA PATTERN</td>
</tr>
<tr>
<td>FREQUENCY</td>
</tr>
</tbody>
</table>

**INTERFACE BOX**

| MEMORY SELECT SWITCHES | All 2.4V |
| INPUT CURRENT SWITCH | GND |
| OUTPUT PULLUP RESISTOR | 15V |
| INITIATE PULSE SWITCH | PULSE |
| WC2 SWITCH | OFF |
| WC SWITCH | OFF |
| MEMORY POWER | OFF |
9.1.3 Push the STOP button. Turn on all three power supplies. Using the DVM, adjust the Interface Box supply to +5.0 ± 0.1V. Set the memory supplies to approximately +5V and -6V. Set the MEMORY POWER switch to ON. Using the DVM, adjust the memory supplies to +5.0 ± 0.1V and -6.1 ± 0.1V. Set the memory power switch to OFF.

9.1.4 Using the scope, adjust the Pulse Generator for +3.0 ± 0.1V positive pulses of 450 ± 10 nanoseconds duration (measured at the 50% points). Using the counter, adjust the rep rate to 600 ± 1.0 KHz. The pulse generator must be terminated in 50 ohms and connected to the tester when making these adjustments. Just prior to starting the environmental test, proceed to the next applicable paragraph.

9.2 TEST

Push the tester STOP and RESET pushbuttons. Turn the MEMORY POWER ON and push the START pushbutton on the tester. The tester will write a "0", read a "0" seven times in all data bits, write a "1", read a "1" seven times in all bits, step to the next address and repeat the same sequence. The tester will keep cycling until an error occurs. Record any bit errors. Proceed immediately to paragraph 9.2.1.
9.2.1 While monitoring the tester for errors, start the vacuum chamber pump and pump the air out of the vacuum chamber at a rate such that the pressure inside the chamber drops to 7 mmHg in less than five minutes. Record any errors.

9.2.2 Continue pumping the chamber until the pressure $10^{-5}$ mmHg. In order to reach this pressure, the test may last several hours. Therefore, one hour after the test has started, the memory and tester may be turned off by pushing the STOP pushbutton on the tester, turning the MEMORY POWER OFF and turning the TESTER POWER OFF. After the chamber has reached $10^{-5}$ mmHg, test the memory as outlined in paragraph 7.13. Record any errors. Push the memory STOP pushbutton, turn the MEMORY POWER OFF, turn the TESTER POWER OFF and return the memory to one atmosphere pressure.

10. VIBRATION TEST

The following vibration tests are to be performed in three mutually perpendicular axes. The tests include sine sweep and random vibration, and the levels to be used are described below in the individual tests. These levels are inputs to the base or mounting bracket of the unit under test. The unit shall be functionally tested during the vibration testing to insure correct operation. Prior to performing the random vibration a spectral analysis of the tester input shall be performed to insure that the random vibration input is within the specified limits. The analysis
shall be plotted and the data sheet kept as part of the test data. For information only, an accelerometer shall be mounted on the top surface of the housing while testing the X and Z axes. Plot the output from this accelerometer and file as part of the test data.

10.1 SINE SWEEP TEST

10.1.1 Verify that the MEMORY POWER switch is in the OFF position. Turn the coarse voltage controls fully counterclockwise on all three power supplies.

Connect the equipment as shown in Figure 3 and turn on power to all memory associated test equipment.


Mount the memory unit on the shake table so as to be vibrated in the vertical (Y) axis as shown in Figure 4. (The axis order may be varied for convenience).

10.1.2 Push the STOP and RESET buttons. Turn the MEMORY POWER ON.

Perform a sine sweep over the frequency range of 5-2000 Hz at the levels listed below:

<table>
<thead>
<tr>
<th>FREQUENCY RANGE</th>
<th>TEST LEVEL</th>
</tr>
</thead>
<tbody>
<tr>
<td>5-25 Hz</td>
<td>0.33 in DA</td>
</tr>
<tr>
<td>24-110 Hz</td>
<td>10G PEAK</td>
</tr>
<tr>
<td>110-2000 Hz</td>
<td>5g PEAK</td>
</tr>
</tbody>
</table>

The sweep rate is to be 2 octaves per minute. During the sweep, repeatedly perform the tests of paragraph 7.13. Record any bit errors in the Qual Test Data Sheet. Push the STOP button.
10.2 RANDOM VIBRATION

10.2.1 Perform the spectral analysis specified in paragraph 10. While applying the following random vibration input, repeatedly perform the tests of paragraph 7.13.

<table>
<thead>
<tr>
<th>FREQUENCY RANGE</th>
<th>TEST LEVEL</th>
<th>TOLERANCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>15 Hz</td>
<td>.0044g²/Hz</td>
<td>± 3db</td>
</tr>
<tr>
<td>15-70 Hz</td>
<td>LINEAR INCREASE</td>
<td>Log-Log Plot</td>
</tr>
<tr>
<td>70-100 Hz</td>
<td>.138 g²/Hz</td>
<td>± 3db</td>
</tr>
<tr>
<td>100-400 Hz</td>
<td>LINEAR DECREASE</td>
<td>Log-Log Plot</td>
</tr>
<tr>
<td>400-2000 Hz</td>
<td>.0089 g²/Hz</td>
<td>± 3db</td>
</tr>
</tbody>
</table>

The test time is to be 2 minutes per axis.

Record any errors in the Data Record.

10.22 Repeat paragraph 10.1.2 and 10.2, in the two other mutually perpendicular axes as shown in Figure 4. Push the STOP button. Turn the MEMORY POWER OFF and then turn the TESTER POWER OFF.

11. SHOCK TEST

Two shocks in each direction shall be applied along the three mutually perpendicular axes of the LP RASM (total of 6 shocks).

11.1 SETUP

Verify that the MEMORY POWER switch is in the OFF position. Turn the coarse voltage controls fully counterclockwise on all three power supplies. Connect the equipment as shown in Figure 3 and apply power to all memory associated test equipment. Set the controls as shown in para. 9.1.2 and perform para. 9.1.3 and 9.1.4. Mount the LP RASM on the shock table so as to apply...
the shock in the vertical (Y) axis as shown in Figure 5. (The axes order may be varied for convenience).

11.2 TEST

11.2.1 Push the STOP and RESET buttons. Turn the MEMORY POWER ON and push the START button. The tester is now testing the LP RASM for bit errors. Apply a half sine shock pulse of 30 g's for a duration of 6 milliseconds. Record any bit errors. Push the STOP button.

11.2.2 Push the RESET and START buttons. Apply a half sine shock pulse of 30 g's for a duration of 12 milliseconds. Record any bit errors.

11.2.3 Repeat para. 11.2.1 and 11.2.2 for each of the other two directions as shown in Figure 5. Push the STOP button. Turn the MEMORY POWER OFF and then turn the TESTER POWER OFF.

12. FINAL FUNCTIONAL TESTS

To insure that the memory is still operating properly, perform all the tests of paragraph 7. Record the data.
FIGURE 2. TEST SET UP
FIGURE 3. TEST SET UP
VERTICAL
(Y) AXIS

HORIZONTAL
(X) AXIS

LONGITUDINAL
(Z) AXIS

ACCELEROMETER
FOR X AXIS

ACCELEROMETER
FOR Y AXIS

ACCELEROMETER
FOR Z AXIS

FIGURE 4. VIBRATION AXES
Initial Release

Incorporated changes prior, to First Usage

Change -6.9V to -6.1V

Change 6000mw to 7000mw, pages 10, 17, 19, 30. Change weight from 6.0 to 6.5 pounds, page 2.

Add weight 5.8 pounds for magnesium chassis MCO S7835.

Revised per MCO S7845

S/N 103

MOTOROLA INC.
Government Electronics Division
8201 EAST McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

ACCEPTANCE TEST DATA SHEET,
LOW POWER RANDOM ACCESS SPACE-CRAFT MEMORY, PART NO. 01-P13701D

SIZE
A
94990
12-P13721D

MFG
PROJ 4339
NO. 4601

CONTR NASS-23163
NO. NASS-20576

RELEASE
NOTICE

APPROVED DATE
1-2-73 H. Tweed

APPROVED DATE

SCALE

SHEET 1 OF 35
1. **SCOPE**

   This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

2. **REFERENCE INFORMATION**

2.1 **SPECIFICATIONS APPLICABLE**

   - **S-562-P-24**
     - Low Power Random Access Spacecraft Memory
   - **12-P13722D**
     - Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. **TEST DATA**

   Unit S/N **103**
   
   Start Date of Tests **4/28/75**
   
   Tested by **[Signature]**

4. **PHYSICAL CHARACTERISTICS**

4.1 **WEIGHT**

   Weight of LP-RASM = **5.640** pounds
   
   6.5 pounds (aluminum)
   5.8 pounds (magnesium)
S/N 103

Date of Test 4/28/25
Tested By B-144

6.2 DIMENSIONS

H = 2.896 inches
M = 8.960 inches
W = 8.630 inches
D = 6.328 inches
MD = 6.929 inches

V = H x W x D = 158.0 inches³

≤ 160 inches³
7.4 CHASSIS ISOLATION

Impedance \[ \geq 9 \text{ megohms} \]

7.5 INPUT SIGNAL LOADING

7.5.2 Current from INITIATE PULSE to Gnd \(1.15\) ma \(\leq 2\) ma
Current from 2.4V to INITIATE PULSE \(3.13\) \(\mu\)a \(\leq 20\) \(\mu\)a

7.5.3 Current from MEM SEL 1 to Gnd \(1.14\) ma \(\leq 2\) ma
Current from 2.4V to MEM SEL 1 \(2.49\) \(\mu\)a \(\leq 20\) \(\mu\)a

7.5.4 Current from MEM SEL 2 to Gnd \(1.14\) ma \(\leq 2\) ma
Current from 2.4V to MEM SEL 2 \(3.46\) \(\mu\)a \(\leq 20\) \(\mu\)a
Current from MEM SEL 3 to Gnd \(1.14\) ma \(\leq 2\) ma
Current from 2.4V to MEL SEL 3 \(3.42\) \(\mu\)a \(\leq 20\) \(\mu\)a

7.5.5 Current from MEM SEL 4 to Gnd \(1.14\) ma \(\leq 2\) ma
Current from 2.4V to MEM SEL 4 \(2.49\) \(\mu\)a \(\leq 20\) \(\mu\)a

7.5.6 Current from READ/WRITE to Gnd \(0.856\) ma \(\leq 2\) ma
Current from 2.4V to READ/WRITE \(856\) \(4.9\) \(\mu\)A \(\leq 20\) \(\mu\)a

7.5.6 Current from ADDRESS 2\(^0\) to Gnd \(0.87\) ma \(\leq 2\) ma
Current from 2.4V to ADDRESS 2\(^0\) \(5.28\) \(\mu\)a \(\leq 20\) \(\mu\)a
Current from ADDRESS 2\(^1\) to Gnd \(0.875\) \(\text{ma}\)  
Current from 2.4V to ADDRESS 2\(^1\) \(50.6\) \(\mu\text{a}\)  
Current from ADDRESS 2\(^2\) to Gnd \(0.945\) \(\text{ma}\)  
Current from 2.4V to ADDRESS 2\(^2\) \(5.68\) \(\mu\text{a}\)  
Current from ADDRESS 2\(^3\) to Gnd \(0.882\) \(\text{ma}\)  
Current from 2.4V to ADDRESS 2\(^3\) \(5.36\) \(\mu\text{a}\)  
Current from ADDRESS 2\(^4\) to Gnd \(0.934\) \(\text{ma}\)  
Current from 2.4V to ADDRESS 2\(^4\) \(6.1\) \(\mu\text{a}\)
<table>
<thead>
<tr>
<th>Current from ADDRESS</th>
<th>Current from 2.4V</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>2⁵ to Gnd</td>
<td>2⁵</td>
<td></td>
</tr>
<tr>
<td>0.884 ma</td>
<td>4.73 μA</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td></td>
<td></td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>2⁶ to Gnd</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.870 ma</td>
<td></td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td></td>
<td></td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>2⁷ to Gnd</td>
<td>2⁷</td>
<td></td>
</tr>
<tr>
<td>0.962 ma</td>
<td>5.62 μA</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td></td>
<td></td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>2⁸ to Gnd</td>
<td>2⁸</td>
<td></td>
</tr>
<tr>
<td>0.993 ma</td>
<td>1.99 μA</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td></td>
<td></td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>2⁹ to Gnd</td>
<td>2⁹</td>
<td></td>
</tr>
<tr>
<td>0.967 ma</td>
<td>1.09 μA</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td></td>
<td></td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>2¹⁰ to Gnd</td>
<td>2¹⁰</td>
<td></td>
</tr>
<tr>
<td>0.852 ma</td>
<td>5.46 μA</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td></td>
<td></td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>2¹¹ to Gnd</td>
<td>2¹¹</td>
<td></td>
</tr>
<tr>
<td>0.855 ma</td>
<td>5.42 μA</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td></td>
<td></td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>DATA IN BIT 0 to Gnd</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.056 ma</td>
<td></td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td></td>
<td></td>
<td>≤ 20 μA</td>
</tr>
</tbody>
</table>

Current from 2.4V to DATA IN BIT 0 1.056 μA  ≤ 2 ma
Current from 2.4V to DATA IN BIT 0 7.96 μA  ≤ 20 μA
S/N 103  Date of Test 4/28/75
Tested By B. J. F.

Current from DATA IN BIT 1 to Gnd 1.04 ma
Current from 2.4V to DATA IN BIT 1 8.12 µa

Current from DATA IN BIT 2 to Gnd 1.06 ma
Current from 2.4V to DATA IN BIT 2 7.45 µa

Current from DATA IN BIT 3 to Gnd 9.96 ma
Current from 2.4V to DATA IN BIT 3 8.77 µa

Current from DATA IN BIT 4 to Gnd 1.00 ma
Current from 2.4V to DATA IN BIT 4 8.62 µa

Current from DATA IN BIT 5 to Gnd 1.024 ma
Current from 2.4V to DATA IN BIT 5 8.72 µa

Current from DATA IN BIT 6 to Gnd 1.05 ma
Current from 2.4V to DATA IN BIT 6 7.0 µa

Current from DATA IN BIT 7 to Gnd 1.04 ma
Current from 2.4V to DATA IN BIT 7 7.53 µa

Current from DATA IN BIT 8 to Gnd 1.04 ma
Current from 2.4V to DATA IN BIT 8 7.54 µa

Current from DATA IN BIT 9 to Gnd 9.65 ma
Current from 2.4V to DATA IN BIT 9 3.06 µa

Limits

≤ 2 ma
≤ 20 µa
Current from DATA IN BIT 10 to Gnd 1.969 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 10 3.11 µa ≤ 20 µa
Current from DATA IN BIT 11 to Gnd 0.972 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 11 2.92 µa ≤ 20 µa
Current from DATA IN BIT 12 to Gnd 806 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 12 7.23 µa ≤ 20 µa
Current from DATA IN BIT 13 to Gnd 515 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 14 7.47 µa ≤ 20 µa
Current from DATA IN BIT 14 to Gnd 840 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 14 8.02 µa ≤ 20 µa
Current from DATA IN BIT 15 to Gnd 1.950 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 15 4.97 µa ≤ 20 µa
Current from DATA IN BIT 16 to Gnd 922 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 17 5.03 µa ≤ 20 µa
Current from DATA IN BIT 17 to Gnd 929 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 17 5.13 µa ≤ 20 µa
### Verification of Open Collector on Output Signals

#### 7.6

**S/N**: 102

**Date of Test**: 4/24/75

**Tested By**: [Signature]

<table>
<thead>
<tr>
<th>Voltage Bit</th>
<th>Voltage (mv)</th>
<th>Limit (mv)</th>
</tr>
</thead>
<tbody>
<tr>
<td>7.6.3 READ COMPLETE</td>
<td>70</td>
<td>≤ 100</td>
</tr>
<tr>
<td>7.6.4 DATA OUT BIT 0</td>
<td>10</td>
<td>≤ 100</td>
</tr>
<tr>
<td>DATA OUT BIT 1</td>
<td>10</td>
<td>≤ 100</td>
</tr>
<tr>
<td>DATA OUT BIT 2</td>
<td>0</td>
<td>≤ 100</td>
</tr>
<tr>
<td>DATA OUT BIT 3</td>
<td>-10</td>
<td>≤ 100</td>
</tr>
<tr>
<td>DATA OUT BIT 4</td>
<td>-10</td>
<td>≤ 100</td>
</tr>
<tr>
<td>DATA OUT BIT 5</td>
<td>-10</td>
<td>≤ 100</td>
</tr>
<tr>
<td>DATA OUT BIT 6</td>
<td>-10</td>
<td>≤ 100</td>
</tr>
<tr>
<td>DATA OUT BIT 7</td>
<td>-20</td>
<td>≤ 100</td>
</tr>
<tr>
<td>DATA OUT BIT 8</td>
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<td>≤ 100</td>
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<tr>
<td>DATA OUT BIT 9</td>
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<td>≤ 100</td>
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<tr>
<td>DATA OUT BIT 10</td>
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<td>DATA OUT BIT 11</td>
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<td>DATA OUT BIT 12</td>
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<tr>
<td>DATA OUT BIT 13</td>
<td>0</td>
<td>≤ 100</td>
</tr>
<tr>
<td>DATA OUT BIT 14</td>
<td>20</td>
<td>≤ 100</td>
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<tr>
<td>DATA OUT BIT 15</td>
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<td>≤ 100</td>
</tr>
<tr>
<td>DATA OUT BIT 16</td>
<td>-20</td>
<td>≤ 100</td>
</tr>
<tr>
<td>DATA OUT BIT 17</td>
<td>-10</td>
<td>≤ 100</td>
</tr>
</tbody>
</table>
7.7 POWER CONSUMPTION (25°C)

7.7.1 Memory +5V Voltage 4.993 Volts
Memory -6.1V Voltage 6.102 Volts
+5V Current 10.3 ma
+5V Power 51.5 mw

7.7.2 Memory -6.1V Current 4.7 ma
Memory -6.1V Power 8.7 mw

7.7.3 Total Memory Idle Power 3.34 mw 80.2

7.7.5 Memory +5V Voltage 5.006 Volts
Memory -6.1V Voltage 6.101 Volts
+5V Current 6.95 ma
+5V Power 347.5 mw

7.7.6 Memory -6.1V Current 240 ma
Memory -6.1V Power 1464 mw

7.7.7 Total Active Power 4939 mw

7.8 READ COMPLETE TIMING

7.8.5 Delay 410 ns
Duration 330 ns

500 ns max.
250 ns min
450 ns max.
Date of Test 4/29/75
Tested by B.100

READ COMPLETE/DATA OUTPUT TIMING

<table>
<thead>
<tr>
<th>Test</th>
<th>Result</th>
<th>Action</th>
<th>Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DO-0</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-1</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-2</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-3</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-4</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-5</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-6</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-7</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-8</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-9</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-10</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-11</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-12</td>
<td>OK</td>
<td>REJECT</td>
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</tr>
<tr>
<td>DO-13</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-14</td>
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<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-15</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-16</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
<tr>
<td>DO-17</td>
<td>OK</td>
<td>REJECT</td>
<td></td>
</tr>
</tbody>
</table>

LIMITS

REFER TO TEST PROC.
7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?
No
Yes Address Bits 0 errors

7.9.4 Did an error occur?
No
Yes Address Bits 0 errors

7.9.10 Did an error occur?
No
Yes Address Bits 0 errors

7.9.16 Did an error occur?
No
Yes Address Bits 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?
No
Yes Address Bits 0 errors

7.10.7 Did an error occur?
a) No
Yes Address Bits 0 errors
S/N 103

Date of Test 4/28/75
Tested By

b) No
Yes __________ Address ________ Bits ________ 0 errors

No ______

Limits

S/N 103

b) No
Yes __________ Address ________ Bits ________ 0 errors

No ______

7.11 NON-VOLATILITY TEST

Did an error occur?

7.11.7 No

7.11.9 Yes __________ Address ________ Bits ________ 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal)

7.12.4 Address 0001 0000 (Octal)
0001 0000 (Octal)
0010 0000 (Octal)
0011 0000 (Octal)
0100 0000 (Octal)
0101 0000 (Octal)
0110 0000 (Octal)
0111 0000 (Octal)
1000 0000 (Octal)
1001 0000 (Octal)
1010 0000 (Octal)
S/N 103  Date of Test 4/28/75
Tested By 8/60

Address 1011 c000 (Octal)  Limits 0000
1100 c000 (Octal) 0000
1101 c000 (Octal) 0000
1110 c000 (Octal) 0000

7.12.6 Did an error occur?
No /
Yes — Address —— Bits —— 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?
No /
Yes — Address —— Bits —— 0 errors

7.13.3 Did an error occur?
No /
Yes — Address —— Bits —— 0 errors
S/N 103

Date of Test 4/17/77
Tested By B. J. O.

7.13.4
a) Did an error occur?

No

Yes Address Bit 0 errors

b) Did an error occur?

No

Yes Address Bit 0 errors
8. TEMPERATURE TEST

8.2.1 TIME 5:57

8.2.2 LOW TEMPERATURE

THERMISTOR RESISTANCE

150 MINUTES 222.3 K OHMS
160 MINUTES 222.7 K OHMS % CHANGE 1.2%
170 MINUTES K OHMS % CHANGE
180 MINUTES K OHMS % CHANGE
190 MINUTES K OHMS % CHANGE

8.2.3 DID AN ERROR OCCUR?

NO ✓

8.2.4 -6.1 V VOLTAGE 4.900 VOLTS +5 V VOLTAGE 5.257 VOLTS
-6.1 V CURRENT 14.3 ma +5 V CURRENT 12.9 ma
-6.1 V POWER 91.52 mw +5 V POWER 57.26 mw

TOTAL MEMORY IDLE POWER 148.28 mw 170 mw MAX

8.2.5 -6.1 V VOLTAGE 6.402 VOLTS +5 V VOLTAGE 5.25 VOLTS
-6.1 V CURRENT 263 ma +5 V CURRENT 760 ma
-6.1 V POWER 1,683 mw +5 V POWER 3,675 mw

TOTAL MEMORY OPERATING POWER 5,358 mw 7,000 mw MAX
S/N 103

DATE OF TEST 4/29/75

TESTED BY

LIMITS

8.2.6  DID AN ERROR OCCUR?

NO /

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

8.2.8  WC a) DID AN ERROR OCCUR?

NO /

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

WC b) DID AN ERROR OCCUR?

NO /

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO /

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

WC d) DID AN ERROR OCCUR?

NO /

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

8.2.6 II WC a) DID AN ERROR OCCUR?

NO /

YES ___ ADDRESS ___ BIT ___ 0 ERRORS

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Government Electronics Division
8201 EAST McDOWELL ROAD
SCOTTSDALE, ARIZONA 85257

SIZE CODE IDENT NO. DWG NO.
A 94990 12-P13721D

SCALE REVISION SHEET

AV-2-B-199H-100A-2/4 DWG FORMAT
**8.2.9 (Cont.)**

WC b) DID AN ERROR OCCUR?

<table>
<thead>
<tr>
<th>NO</th>
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<tr>
<td></td>
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</table>

**ADDRESS BIT**

---

WC c) DID AN ERROR OCCUR?

<table>
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<tr>
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**ADDRESS BIT**

---

WC d) DID AN ERROR OCCUR?

<table>
<thead>
<tr>
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<tbody>
<tr>
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**ADDRESS BIT**

---

**8.3 INTERMEDIATE TEMPERATURE TEST**

**TIME**: 7:43

**8.3.2 TIME**

<table>
<thead>
<tr>
<th>TIME</th>
<th>THERMISTOR READING</th>
<th>OHMS</th>
<th>ERRORS</th>
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<tbody>
<tr>
<td>4.45</td>
<td>126.8</td>
<td>K</td>
<td>YES</td>
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<tr>
<td>9.55</td>
<td>89.6</td>
<td>K</td>
<td>YES</td>
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<tr>
<td>10.25</td>
<td>8.7</td>
<td>K</td>
<td>YES</td>
</tr>
<tr>
<td>10.25</td>
<td>89.6</td>
<td>K</td>
<td>YES</td>
</tr>
<tr>
<td>10.35</td>
<td>9.3</td>
<td>K</td>
<td>YES</td>
</tr>
<tr>
<td>10.45</td>
<td>5.7</td>
<td>K</td>
<td>YES</td>
</tr>
<tr>
<td>11.05</td>
<td>4.3</td>
<td>K</td>
<td>YES</td>
</tr>
<tr>
<td>11.15</td>
<td>2.7</td>
<td>K</td>
<td>YES</td>
</tr>
</tbody>
</table>

**DID ANY ERROR OCCUR?**

---

**ERRORS**

8.3.3  
TIME 10:54

8.4.1  
50 MINUTES 1.408 K OHMS
80 MINUTES 1.408 K OHMS % CHANGE 0
90 MINUTES --- K OHMS % CHANGE
170 80 MINUTES K OHMS % CHANGE
90 MINUTES --- K OHMS % CHANGE

8.4.1  
-6.1 V VOLTAGE 4.403 VOLTS +5 V VOLTAGE 5.252 VOLTS
-6.1 V CURRENT 6.3 ma +5 V CURRENT 12.2 ma
-6.1 V POWER 40.3 mw +5 V POWER 64.1 mw
TOTAL MEMORY IDLE POWER 104.4 mw 170 mw MAX

8.4.2  
DID AN ERROR OCCUR?
NO ☑
YES ADDRESS ___ BIT ____ 0 ERRORS

8.4.3  
-6.1 V VOLTAGE 6.400 VOLTS +5 V VOLTAGE 5.247 VOLTS
-6.1 V CURRENT 280 ma +5 V VOLTAGE 795 ma
-6.1 V POWER 1772 mw +5 V POWER 4171 mw
TOTAL MEMORY OPERATING POWER 5963 mw 7000 mw MAX

8.4.4  
wc a) DID AN ERROR OCCUR?
NO ☑
YES ADDRESS ___ BIT ____ 0 ERRORS
8.4.4 (Cont.)

YES □ ADDRESS _____ BIT _____ O ERRORS
NO ✓

WC b) DID AN ERROR OCCUR?

LIMITS

WC c) DID AN ERROR OCCUR?

DID AN ERROR OCCUR?

NO ✓

YES ADDRESS _____ BIT _____ O ERRORS

MC b) DID AN ERROR OCCUR?

NO ✓

YES ADDRESS _____ BIT _____ O ERRORS

WC d) DID AN ERROR OCCUR?

NO ✓

YES ADDRESS _____ BIT _____ O ERRORS

8.4.6 WC a) DID AN ERROR OCCUR?

NO ✓

YES ADDRESS _____ BIT _____ O ERRORS

WC b) DID AN ERROR OCCUR?

NO ✓

YES ADDRESS _____ BIT _____ O ERRORS

WC c) DID AN ERROR OCCUR?

NO ✓

YES ADDRESS _____ BIT _____ O ERRORS

WC d) DID AN ERROR OCCUR?

NO ✓

YES ADDRESS _____ BIT _____ O ERRORS

8.4.7 DID AN ERROR OCCUR?

NO ✓

YES ADDRESS _____ BIT _____ O ERRORS
## VACUUM TEST

9.2 Did Any Bit Errors Occur?

<table>
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<tr>
<th>No</th>
<th>V</th>
<th>Address</th>
<th>Bits</th>
<th>0 Errors</th>
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### Fast Decompression

<table>
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<th>5/5/75</th>
<th>Tested by</th>
<th>B. Junt</th>
</tr>
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Did Any Bit Errors Occur?

<table>
<thead>
<tr>
<th>No</th>
<th>V</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Address</th>
<th>Bits</th>
<th>0 Errors</th>
</tr>
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</table>

### Hard Vacuum

<table>
<thead>
<tr>
<th>Date</th>
<th>5/5/75</th>
<th>Tested by</th>
<th>B. Junt</th>
</tr>
</thead>
</table>

Did Any Bit Errors Occur?

<table>
<thead>
<tr>
<th>No</th>
<th>V</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Address</th>
<th>Bits</th>
<th>0 Errors</th>
</tr>
</thead>
</table>

## VIBRATION TEST

10. SINE SWEEP

Axis X - Did Any Bit Errors Occur?

<table>
<thead>
<tr>
<th>No</th>
<th>V</th>
<th>Freq</th>
<th>Address</th>
<th>Bits</th>
<th>0 Errors</th>
</tr>
</thead>
</table>


S/N 103  

Date of Test 5/6/75  
Tested by

Axis Y - Did Any Bit Error Occur?  

No ___  
Yes ___  Freq _____ Address ____  Bits _____  0 Errors

Axis Z - Did Any Bit Errors Occur?  

No ___  
Yes ___  Freq _____ Address ____  Bits _____  0 Errors

RANDOM VIBRATION  

Axis X - Did Any Bit Errors Occur?  

No ___  
Yes ___  Freq _____ Address ____  Bits _____  0 Errors

Axis Y - Did Any Bit Errors Occur?  

No ___  
Yes ___  Freq _____ Address ____  Bits _____  0 Errors

Axis Z - Did Any Bit Errors Occur?  

No ___  
Yes ___  Freq _____ Address ____  Bits _____  0 Errors

SHOCK TEST  

Date 5/8/75  
Tested By

6 MILISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?  

No ___  
Yes _____  Address _______  Bits _______  0 Errors

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SCOTTSDALE, ARIZONA 85252  

SIZE CODE IDENT NO. DWG NO.  
A 94990 12-P13721D  

SCALE REVISION SHEET
Z Direction - Did Any Bit Errors Occur?

No

Yes  Address  Bits  0 Errors

X Direction - Did Any Bit Errors Occur?

No

Yes  Address  Bits  0 Errors

12 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No

Yes  Address  Bits  0 Errors

Z Direction - Did Any Bit Errors Occur?

No

Yes  Address  Bits  0 Errors

X Direction - Did Any Bit Errors Occur?

No

Yes  Address  Bits  0 Errors

MAY 8-1975
7.4 CHASSIS ISOLATION
Impedance $\geq 10$

7.5 INPUT SIGNAL LOADING

7.5.2 Current from INITIATE PULSE to Gnd 1.164 ma $\leq 2$ ma
Current from 2.4V to INITIATE PULSE $2.57 \mu$A $\leq 20 \mu$A

7.5.3 Current from MEM SEL 1 to Gnd 1.167 ma $\leq 2$ ma
Current from 2.4V to MEM SEL 1 $2.52 \mu$A $\leq 20 \mu$A

7.5.4 Current from MEM SEL 2 to Gnd 1.166 ma $\leq 2$ ma
Current from 2.4V to MEM SEL 2 $3.59 \mu$A $\leq 20 \mu$A
Current from MEM SEL 3 to Gnd 1.165 ma $\leq 2$ ma
Current from 2.4V to MEM SEL 3 $3.54 \mu$A $\leq 20 \mu$A

7.5.5 Current from MEM SEL 4 to Gnd 1.163 ma $\leq 2$ ma
Current from 2.4V to MEM SEL 4 $2.56 \mu$A $\leq 20 \mu$A

7.5.6 Current from READ/WRITE to Gnd 6.1877 ma $\leq 2$ ma
Current from 2.4V to READ/WRITE $5.13 \mu$A $\leq 20 \mu$A

7.5.6 Current from ADDRESS 20 to Gnd 0.83 ma $\leq 2$ ma
Current from 2.4V to ADDRESS 20 $5.47 \mu$A $\leq 20 \mu$A
S/N 103

Date of Test 5-9-75
Tested By

Limits

Current from ADDRESS 1 to Gnd 0.876 ma

≤ 2 ma

Current from 2.4V to ADDRESS 1 5.22 µa

≤ 20 µa

Current from ADDRESS 2 to Gnd 0.967 ma

≤ 2 ma

Current from 2.4V to ADDRESS 2 5.87 µa

≤ 20 µa

Current from ADDRESS 3 to Gnd 504 ma

≤ 2 ma

Current from 2.4V to ADDRESS 3 5.57 µa

≤ 20 µa

Current from ADDRESS 4 to Gnd 0.958 ma

≤ 2 ma

Current from 2.4V to ADDRESS 4 6.33 µa

≤ 20 µa

W. W. Heffernan
5-9-75
<table>
<thead>
<tr>
<th>Description</th>
<th>Current</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current from ADDRESS 2⁵ to Gnd</td>
<td>0.905 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2⁵</td>
<td>4.92 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Current from ADDRESS 2⁶ to Gnd</td>
<td>0.891 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2⁶</td>
<td>5.19 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Current from ADDRESS 2⁷ to Gnd</td>
<td>0.886 ma</td>
<td>≤ 2 ma</td>
</tr>
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<td>Current from 2.4V to ADDRESS 2⁷</td>
<td>5.85 μA</td>
<td>≤ 20 μA</td>
</tr>
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<td>Current from ADDRESS 2⁸ to Gnd</td>
<td>1.016 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2⁸</td>
<td>1.02 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Current from ADDRESS 2⁹ to Gnd</td>
<td>1.991 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2⁹</td>
<td>1.11 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Current from ADDRESS 2¹⁰ to Gnd</td>
<td>1.873 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2¹⁰</td>
<td>5.60 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Current from ADDRESS 2¹¹ to Gnd</td>
<td>0.876 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2¹¹</td>
<td>5.57 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Current from DATA IN BIT 0 to Gnd</td>
<td>1.08 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 0</td>
<td>5.21 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Bit</td>
<td>Current from DATA IN to Gnd</td>
<td>Current from 2.4V to DATA IN</td>
</tr>
<tr>
<td>--------</td>
<td>-----------------------------</td>
<td>-----------------------------</td>
</tr>
<tr>
<td>1</td>
<td>1.06 mA</td>
<td>8.37 μA</td>
</tr>
<tr>
<td>2</td>
<td>1.08 mA</td>
<td>7.66 μA</td>
</tr>
<tr>
<td>3</td>
<td>1.02 mA</td>
<td>8.97 μA</td>
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<td>4</td>
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<td>8.96 μA</td>
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<td>6</td>
<td>1.08 mA</td>
<td>8.18 μA</td>
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<td>7</td>
<td>1.07 mA</td>
<td>7.90 μA</td>
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<tr>
<td>8</td>
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<td>7.77 μA</td>
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<tr>
<td>9</td>
<td>1.98 mA</td>
<td>3.16 μA</td>
</tr>
</tbody>
</table>
Current from DATA IN BIT 10 to Gnd: \(0.991\) ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 10: \(3.21\) μA ≤ 20 μA

Current from DATA IN BIT 11 to Gnd: \(0.995\) ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 11: \(2.99\) μA ≤ 20 μA

Current from DATA IN BIT 12 to Gnd: \(0.826\) ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 12: \(7.44\) μA ≤ 20 μA

Current from DATA IN BIT 13 to Gnd: \(0.835\) ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 13: \(7.67\) μA ≤ 20 μA

Current from DATA IN BIT 14 to Gnd: \(0.860\) ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 14: \(8.21\) μA ≤ 20 μA

Current from DATA IN BIT 15 to Gnd: \(0.974\) ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 15: \(5.10\) μA ≤ 20 μA

Current from DATA IN BIT 16 to Gnd: \(0.945\) ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 16: \(5.20\) μA ≤ 20 μA

Current from DATA IN BIT 17 to Gnd: \(0.956\) ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 17: \(5.32\) μA ≤ 20 μA
7.6

VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS

7.6.3 READ COMPLETE voltage 20 mv 

Limit

7.6.4 DATA OUT BIT 0 voltage 25 mv 
DATA OUT BIT 1 voltage 20 mv 
DATA OUT BIT 2 voltage 20 mv 
DATA OUT BIT 3 voltage 10 mv 
DATA OUT BIT 4 voltage 10 mv 
DATA OUT BIT 5 voltage 10 mv 
DATA OUT BIT 6 voltage 0 mv 
DATA OUT BIT 7 voltage 0 mv 
DATA OUT BIT 8 voltage 0 mv 
DATA OUT BIT 9 voltage 10 mv 
DATA OUT BIT 10 voltage 25 mv 
DATA OUT BIT 11 voltage 30 mv 
DATA OUT BIT 12 voltage 25 mv 
DATA OUT BIT 13 voltage 30 mv 
DATA OUT BIT 14 voltage 30 mv 
DATA OUT BIT 15 voltage 40 mv 
DATA OUT BIT 16 voltage 25 mv 
DATA OUT BIT 17 voltage 30 mv 

\[ \text{Limit} \leq 100 \text{ mv} \]
7.7 POWER CONSUMPTION (25°C)

7.7.1 Memory +5V Voltage \(5.011\) Volts
Memory -6.1V voltage \(6.103\) Volts
+5V Current \(10.5\) ma
+5V Power \(52.615\) mw

7.7.2 Memory -6.1V Current \(4.9\) ma
Memory -6.1V Power \(29.904\) mw

7.7.3 Total Memory Idle Power \(82.54\) mw

7.7.5 Memory +5V Voltage \(5.002\) Volts
Memory -6.1V Voltage \(6.100\) Volts
+5V Current \(6.90\) ma
+5V Power \(3451.0\) mw

7.7.6 Memory -6.1V Current \(238\) ma
Memory -6.1V Power \(1451.8\) mw

7.7.7 Total Active Power \(4902.8\) mw

7.8 READ COMPLETE TIMING

7.8.5 Delay \(410\) ns
Duration \(340\) ns

Date of Test 5-9-75
Tested By

Limits

170 mw max

7000 mw max.
### READ COMPLETE/DATA OUTPUT TIMING

<table>
<thead>
<tr>
<th>DO</th>
<th>Status</th>
<th>Remarks</th>
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<td>DO-17</td>
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</table>
7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?
No
Yes Address Bits 0 errors

7.9.4 Did an error occur?
No
Yes Address Bits 0 errors

7.9.10 Did an error occur?
No
Yes Address Bits 0 errors

7.9.16 Did an error occur?
No
Yes Address Bits 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?
No
Yes Address Bits 0 errors

7.10.7 Did an error occur?
a) No
Yes Address Bits 0 errors
S/N 103

Date of Test 5-9-75

Tested By

Limits

b) No

Yes Address ______ Bits ______ 0 errors

c) No

Yes Address ______ Bits ______ 0 errors

7.11 NON-VOLATILITY TEST

7.11.7 Did an error occur?

&

7.11.9 No

Yes Address ______ Bits ______ 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal) 0000

7.12.4 Address 0001 0000 (Octal) 0000

0010 0000 (Octal) 0000

0011 0000 (Octal) 0000

0100 0000 (Octal) 0000

0101 0000 (Octal) 0000

0110 0000 (Octal) 0000

0111 0000 (Octal) 0000

1000 0000 (Octal) 0000

1001 0000 (Octal) 0000

1010 0000 (Octal) 0000
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<th>Limits</th>
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<td>1011</td>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>1100</td>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>1101</td>
<td>0000</td>
<td>0000</td>
</tr>
<tr>
<td>1110</td>
<td>0000</td>
<td>0000</td>
</tr>
</tbody>
</table>

**7.12.6 Did an error occur?**
- No ✓

**7.13 WORST CASE PATTERN TEST**

**7.13.2 Did an error occur?**
- No ✓

**7.13.3 Did an error occur?**
- No ✓
7.13.4

a) Did an error occur?
   No ✓
   Yes __ Address ___ Bit ___ 
   0 errors

b) Did an error occur?
   No ✓
   Yes __ Address ___ Bit ___ 
   0 errors
<table>
<thead>
<tr>
<th>TIME</th>
<th>PRESSURE (mm Hg A)</th>
<th>REMARKS</th>
</tr>
</thead>
<tbody>
<tr>
<td>1021</td>
<td>7.7</td>
<td>START TO HIGH VACUUM</td>
</tr>
<tr>
<td>1050</td>
<td>1.4 x 10^{-5}</td>
<td></td>
</tr>
<tr>
<td>1100</td>
<td>3.1 x 10^{-5}</td>
<td></td>
</tr>
<tr>
<td>1130</td>
<td>2 x 10^{-5}</td>
<td></td>
</tr>
<tr>
<td>1160</td>
<td>1.3 x 10^{-5}</td>
<td></td>
</tr>
<tr>
<td>1230</td>
<td>1 x 10^{-5}</td>
<td></td>
</tr>
<tr>
<td>1300</td>
<td>1.7 x 10^{-6}</td>
<td>VENT TO AMB.</td>
</tr>
<tr>
<td>1330</td>
<td>9.8 x 10^{-6}</td>
<td>OPEN BELL DAK-END TEST</td>
</tr>
<tr>
<td>1340</td>
<td>8.1 x 10^{-6}</td>
<td></td>
</tr>
</tbody>
</table>
### Shock Test (Drop)

**Project:** 4601-1400  
**Date:** 5-8-73

<table>
<thead>
<tr>
<th>Sheet</th>
<th>1</th>
<th>of</th>
<th>1</th>
</tr>
</thead>
</table>

**W.O. No.:** 3040  
**Control No.:** 11  
**Unit:** P.W.1

<table>
<thead>
<tr>
<th>Serial No.</th>
<th>123</th>
</tr>
</thead>
</table>

**Operator:** A  
**Observer:** A

**Vibration Mounts:**

- **No. of Drops per Face:** 500  
- **Total No. of Drops:** 6  
- **Acceleration:** 7.0 G's  
- **Pulse Duration:** 6.5/12 ms

**Spec Details:** 12-2/13

<table>
<thead>
<tr>
<th>Drop Height</th>
<th>7.6 x 5/4 in.</th>
</tr>
</thead>
</table>

**Programmer Pressure:** 1/4 P.S.I.

**Type of Wave Shape:** 1/8

**Bandpass Filter:**
- Low FR. Hz: 4.3/0 Hz  
- High FR. Hz: 4.3/0 Hz

**Remarks:** 3 drops, 1 side, 3 holes, 1/2" holes

- Pads: 13 x .012 in.  
- 2 - 1/2 x .012 in.  
- 3 - 1/4 x .012 in.  
- 1 - 1/4 x .012 in.  

<table>
<thead>
<tr>
<th>Item No.</th>
<th>Part No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>MIL-2359</td>
<td>3/4 in. plate (B)</td>
</tr>
<tr>
<td>2</td>
<td>MIL-2356</td>
<td>3/4 in. plate (B)</td>
</tr>
<tr>
<td>3</td>
<td>MIL-2358</td>
<td>3/4 in. plate (B)</td>
</tr>
</tbody>
</table>

| Axis | Face | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|------|------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|----|----|----|----|
| A    |      | 1 |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
|      |      |   | 1 |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| B    |      | 1 |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |
|      |      |   | 1 |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |
| C    |      | 1 |   |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |    |
|      |      |   | 1 |   |   |   |   |   |   |   |    |    |    |    |    |    |    |    |    |    |    |    |

**Test Complete**
### VIBRATION TEST

**Project:** 4661-400  
**Unit:** PLATED WIRE MEMORY  
**Control No.:** 01-02  
**W.O. No.:** 3041  
**Operator:** O. Smith  
**Observer:** L. Gouldin  
**Cycle Time:** 15 TO 2K Hz

### Table

| Run No. | Time Start | Time Stop | Accum VIB. Time | Unit Ser. No. | Displacement Inches D.A. | Acceleration: RMS G's  
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1757</td>
<td>1759</td>
<td>2 min</td>
<td>103</td>
<td>NA</td>
<td>5.61</td>
</tr>
<tr>
<td>2</td>
<td>1901</td>
<td>1901</td>
<td>20 sec</td>
<td>103</td>
<td>NA</td>
<td>5.61</td>
</tr>
<tr>
<td>3</td>
<td>1938</td>
<td>1958</td>
<td>20 sec</td>
<td>103</td>
<td>NA</td>
<td>5.61</td>
</tr>
<tr>
<td>4</td>
<td>1994</td>
<td>1994</td>
<td>4 sec</td>
<td>103</td>
<td>0.33&quot;, 5.61</td>
<td>Shaped Random Noise</td>
</tr>
<tr>
<td>X</td>
<td>2111</td>
<td>2113</td>
<td>2 min</td>
<td>103</td>
<td>NA</td>
<td>5.61</td>
</tr>
<tr>
<td>5</td>
<td>2119</td>
<td>2123</td>
<td>4.21 sec</td>
<td>163</td>
<td>0.33&quot;, 5.61</td>
<td>Shaped Random Noise</td>
</tr>
<tr>
<td>6</td>
<td>2148</td>
<td>2148</td>
<td>10 sec</td>
<td>103</td>
<td>0.33&quot;, 5.61</td>
<td>Shaped Random Noise</td>
</tr>
<tr>
<td>7</td>
<td>2248</td>
<td>2152</td>
<td>4.21 sec</td>
<td>163</td>
<td>0.33&quot;, 5.61</td>
<td>Shaped Random Noise</td>
</tr>
<tr>
<td>8</td>
<td>2257</td>
<td>2259</td>
<td>2 min</td>
<td>103</td>
<td>NA</td>
<td>5.61</td>
</tr>
</tbody>
</table>

**Remarks:** END TEST
PROJECT 4601-100  UNIT Wire Memory SER. NO. 103

X AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1.5 Hz SCAN RATE 1.125 Hz AVG. TIME 10 SECONDS
2.0 Hz SCAN RATE 2.25 Hz AVG. TIME 10 SECONDS
3.20 Hz SCAN RATE 3.5 Hz AVG. TIME 10 SECONDS
4.50 Hz SCAN RATE 4.25 Hz AVG. TIME 10 SECONDS

FREQ. RANGE 1.15-20 Hz MOTOROLA SPECIFICATION NO.

1.5-20 Hz COTG. 160/160/160/160
30-100
100-2K

VIBRATION DATE 5-6-75
DATE ANALYZED 5-6-75

W O. Smit

VIBRATION TOLERANCE LEVEL SHOWN

REMARKS

X

Frequency (Hz)

10 20 30 40 50 60 70 80 90 100

ORIGINAL PAGE IS OF POOR QUALITY
Plated

PROJECT 4601-100 UNITWIRE MEMORY  SER. NO. 103

X AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1.5 HZ SCAN RATE 125 HZ AVG. TIME 1.10 SECONDS
210 HZ SCAN RATE 225 HZ AVG. TIME 2.10 SECONDS
320 HZ SCAN RATE 3.5 HZ AVG. TIME 3.10 SECONDS
450 HZ SCAN RATE 425 HZ AVG. TIME 4.10 SECONDS

FREQ. RANGE 1. 15-20 HZ MOTOROLA SPECIFICATION NO.
2. 20-40 HZ CUSTOMER SPECIFICATION NO.
3. 40-100 Hz
4. 100-20 Hz

VIBRATION DATE 6-6-75
DATE ANALYZED 6-6-75 BY O. Smith
VIBRATION TOLERANCE LEVEL N/A
REMARKS response, accelerometer on top of unit

ORIGINAL PAGE OF POOR QUALITY
FILTER B.W.  
1. 500 Hz SCAN RATE 1.25 Hz AVG. TIME 1.10 Sec.  
2. 200 Hz SCAN RATE 2.25 Hz AVG. TIME 2.10 Sec.  
3. 20 Hz SCAN RATE 3.5 Hz AVG. TIME 3.10 Sec.  
4. 50 Hz SCAN RATE 4.25 Hz AVG. TIME 4.10 Sec.  

FREQ. RANGE 115-20 Hz MOTOROLA SPECIFICATION NO.  
220-400 Hz CUSTOMER SPECIFICATION NO.  

VIBRATION DATE 5-6-75  
DATE ANALYZED 5-6-75  
VIBRATION LEVEL ShOWN  
O. Smith  

REMARKS  

Frequency (Hz)  

Power Spectral Density (c^2/Hz)
Plated
PROJECT 4601-400 UNIT WIRE MEMORY SER. NO. 103

Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1.5 HZ SCAN RATE 1.125 HZ A-G. TIME 1.10 SECONDS

1.20 HZ SCAN RATE 0.51 A-G. TIME 10 SECONDS

0.50 HZ SCAN RATE 1.20 A-G. TIME 10 SECONDS

FREQ. RANGE 0.15-20 HZ大陸

2.10 HZ 40 HZ 60 HZ 80 HZ 100 HZ 1.10 HZ 1.20 HZ 1.50 HZ

0.15-20 HZ 20-40 HZ 40-100 HZ 100-2K HZ 2K-5K HZ 5-6.25 HZ 6.25-7.5 HZ 7.5-10 HZ N/A

By G. Smith
response accelerometer on top of unit

Frequency (Hz)
**Plated Wire**

**Project:** 460-400 Unit Memory  
**SER. No.:** 103

**X**  
**AXIS FREQ RANGE:** 5-2 KHZ

**PLOTTER CAL.**  
**FREQ:** x  
**V. 10 DB/IN.**

**ACCELERATION:** 10^-5  
**PKGS. DISPLACED:** 33"  
**DA**

**VIBRATION DATE:** 5-6-75  
**BY:** C. Saucy

**REMARKS:** ACCEL ON TOP OF UNIT VS INPUT

**Motorola Specification No.:** LINC

**Customer Specification No.:** T/E IN PLOT VS SERVO

**FREQUENCY IN CYCLES PER SECOND**

- **T=1**
ATTACHMENT III

ACCEPTANCE TEST DATA SHEET,
LOW POWER RANDOM ACCESS SP
SPACECRAFT MEMORY
PART NO. 12-P13721D
DRAWING NO. 12-P13721D
SERIAL NUMBER 104
(35 PAGES)
<table>
<thead>
<tr>
<th>APPLICATION</th>
<th>REVISIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>NEXT ASSEMBLY</td>
<td>LETTER DESCRIPTION</td>
</tr>
<tr>
<td>X1</td>
<td>Initial Release</td>
</tr>
<tr>
<td>X2</td>
<td>Incorporated changes prior to First Usage</td>
</tr>
<tr>
<td>X3</td>
<td>Change -6.9V to -6.1V</td>
</tr>
<tr>
<td>X4</td>
<td>Change 6000 mw to 7000 mw, pages 10, 17, 19, 30. Change weight from 6.0 to 6.5 pounds, page 2.</td>
</tr>
<tr>
<td>X5</td>
<td>Add weight 5.8 pounds for magnesium chassis MCO S7835.</td>
</tr>
<tr>
<td>X6</td>
<td>Revised per MCO S7845</td>
</tr>
</tbody>
</table>

**SN 104**
1. **SCOPE**

This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

2. **REFERENCE INFORMATION**

2.1 **SPECIFICATIONS APPLICABLE**

<table>
<thead>
<tr>
<th>Specification</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>S-562-P 24</td>
<td>Low Power Random Access Spacecraft Memory</td>
</tr>
<tr>
<td>12-P13722D</td>
<td>Acceptance Test Procedure, Low Power Random Access Spacecraft Memory</td>
</tr>
</tbody>
</table>

3. **TEST DATA**

<table>
<thead>
<tr>
<th>Unit S/N</th>
<th>Start Date of Tests</th>
<th>Tested by</th>
</tr>
</thead>
<tbody>
<tr>
<td>104</td>
<td>5/28/75</td>
<td></td>
</tr>
</tbody>
</table>

**ATP PARA. NO.**

3.1 **EQUIVALENT TEST EQUIPMENT**

- DC Milliammeter H.P 426A 0-1A
- Digital Voltmeter Fluke 8120A (Multimeter)
- Counter HP 5245L

4. **PHYSICAL CHARACTERISTICS**

6.1 **WEIGHT**

Weight of LP-RASM = 5.562 Pounds

Limit

- 6.5 pounds (aluminum)
- 5.8 pounds (magnesium)
S/N 104  
Date of Test 5/24/75  
Tested By  

6.2 DIMENSIONS  

H = 2.835 inches  
W = 6.630 inches  
MW = 0.955 inches  
D = 7.322 inches  
MD = 6.207.64 inches  

V = H x W x D = 157.64 inches³  ≤ 160 inches³
7.4 CHASSIS ISOLATION

Impedance: 2.9 meg ohms

Limit: ≥ 9 megohms

7.5 INPUT SIGNAL LOADING

7.5.2 Current from INITIATE PULSE to Gnd: 1.405 mA ≤ 2 mA
Current from 2.4V to INITIATE PULSE: 1.40 μA ≤ 20 μA

7.5.3 Current from MEM SEL 1 to Gnd: 1.403 mA ≤ 2 mA
Current from 2.4V to MEM SEL 1: 1.04 μA ≤ 20 μA

7.5.4 Current from MEM SEL 2 to Gnd: 1.407 mA ≤ 2 mA
Current from 2.4V to MEM SEL 2: 1.41 μA ≤ 20 μA
Current from MEM SEL 3 to Gnd: 1.408 mA ≤ 2 mA
Current from 2.4V to MEM SEL 3: 1.42 μA ≤ 20 μA
Current from MEM SEL 4 to Gnd: 1.401 mA ≤ 2 mA
Current from 2.4V to MEM SEL 4: 1.02 μA ≤ 20 μA

7.5.5 Current from READ/WRITE to Gnd: 1.008 mA ≤ 2 mA
Current from 2.4V to READ/WRITE: 1.30 μA ≤ 20 μA

7.5.6 Current from ADDRESS 2⁰ to Gnd: 0.912 mA ≤ 2 mA
Current from 2.4V to ADDRESS 2⁰: 0.562 μA ≤ 20 μA
S/N 104  
Date of Test 5/28/75  
Tested By [Signature]

Current from ADDRESS 1 to Gnd 0.916 ma  
Limits  
≤ 2 ma

Current from 2.4V to ADDRESS 1 0.017 μa  
≤ 20 μa

Current from ADDRESS 2 to Gnd 0.985 ma  
≤ 2 ma

Current from 2.4V to ADDRESS 2 7.06 μa  
≤ 20 μa

Current from ADDRESS 3 to Gnd 0.916 ma  
≤ 2 ma

Current from 2.4V to ADDRESS 3 7.80 μa  
≤ 20 μa

Current from ADDRESS 4 to Gnd 0.965 ma  
≤ 2 ma

Current from 2.4V to ADDRESS 4 8.22 μa  
≤ 20 μa

[Company Information]
Current from ADDRESS $2^5$ to Gnd $0.906 \text{ ma}$
Current from 2.4V to ADDRESS $2^5$ $5.67 \mu\text{a}$

Current from ADDRESS $2^6$ to Gnd $0.901 \text{ ma}$
Current from 2.4V to ADDRESS $2^6$ $5.79 \mu\text{a}$

Current from ADDRESS $2^7$ to Gnd $0.973 \text{ ma}$
Current from 2.4V to ADDRESS $2^7$ $6.82 \mu\text{a}$

Current from ADDRESS $2^8$ to Gnd $0.946 \text{ ma}$
Current from 2.4V to ADDRESS $2^8$ $1.44 \mu\text{a}$

Current from ADDRESS $2^9$ to Gnd $0.935 \text{ ma}$
Current from 2.4V to ADDRESS $2^9$ $1.14 \mu\text{a}$

Current from ADDRESS $2^{10}$ to Gnd $1.006 \text{ ma}$
Current from 2.4V to ADDRESS $2^{10}$ $1.32 \mu\text{a}$

Current from ADDRESS $2^{11}$ to Gnd $1.008 \text{ ma}$
Current from 2.4V to ADDRESS $2^{11}$ $1.36 \mu\text{a}$

Current from DATA IN BIT 0 to Gnd $1.061 \text{ ma}$
Current from 2.4V to DATA IN BIT 0 $7.59 \mu\text{a}$
<table>
<thead>
<tr>
<th>Current from DATA IN BIT</th>
<th>Value</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 to Gnd</td>
<td></td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 1</td>
<td></td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>2 to Gnd</td>
<td></td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 2</td>
<td></td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>3 to Gnd</td>
<td></td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 3</td>
<td></td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>4 to Gnd</td>
<td></td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 4</td>
<td></td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>5 to Gnd</td>
<td></td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 5</td>
<td></td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>6 to Gnd</td>
<td></td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 6</td>
<td></td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>7 to Gnd</td>
<td></td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 7</td>
<td></td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>8 to Gnd</td>
<td></td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 8</td>
<td></td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>9 to Gnd</td>
<td></td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to DATA IN BIT 9</td>
<td></td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Description</td>
<td>Current</td>
<td>Limit</td>
</tr>
<tr>
<td>--------------------------------------------------</td>
<td>---------</td>
<td>-------</td>
</tr>
<tr>
<td>Current from DATA IN BIT 10 to Gnd</td>
<td>0.999 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 10</td>
<td>9.31 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Current from DATA IN BIT 11 to Gnd</td>
<td>1.003 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 11</td>
<td>8.41 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Current from DATA IN BIT 12 to Gnd</td>
<td>1.053 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 12</td>
<td>9.86 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Current from DATA IN BIT 13 to Gnd</td>
<td>1.054 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 14</td>
<td>9.53 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Current from DATA IN BIT 14 to Gnd</td>
<td>1.070 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 14</td>
<td>9.27 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Current from DATA IN BIT 15 to Gnd</td>
<td>1.056 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 15</td>
<td>6.31 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Current from DATA IN BIT 16 to Gnd</td>
<td>1.040 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 17</td>
<td>6.43 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Current from DATA IN BIT 17 to Gnd</td>
<td>1.062 ma</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 17</td>
<td>7.57 μA</td>
<td>≤ 20 μA</td>
</tr>
</tbody>
</table>
### VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS

#### 7.6.3 READ COMPLETE voltage
- Value: 50 mv
- Limit: ≤ 100 mv

#### 7.6.4 DATA OUT BIT 0 voltage
- Value: 20 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 1 voltage
- Value: 20 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 2 voltage
- Value: 10 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 3 voltage
- Value: 20 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 4 voltage
- Value: 10 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 5 voltage
- Value: 0 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 6 voltage
- Value: 10 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 7 voltage
- Value: 0 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 8 voltage
- Value: 0 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 9 voltage
- Value: 20 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 10 voltage
- Value: 20 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 11 voltage
- Value: 20 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 12 voltage
- Value: 10 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 13 voltage
- Value: 25 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 14 voltage
- Value: 40 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 15 voltage
- Value: 10 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 16 voltage
- Value: 10 mv
- Limit: ≤ 100 mv

#### DATA OUT BIT 17 voltage
- Value: 10 mv
- Limit: ≤ 100 mv
7.7 POWER CONSUMPTION (25°C)

7.7.1 Memory +5V Voltage 5.005 Volts
Memory -6.1V Voltage 6.103 Volts
+5V Current 10.1 ma
+5V Power 50.5505 mw

7.7.2 Memory -6.1V Current 3.15 ma
Memory -6.1V Power 19.22445 mw

7.7.3 Total Memory Idle Power 69.77475 mw 170 mw max

7.7.5 Memory +5V Voltage 5.001 Volts
Memory -6.1V Voltage 6.105 Volts
+5V Current 6.65 ma
+5V Power 3325.665 mw

7.7.6 Memory -6.1V Current 2.25 ma
Memory -6.1V Power 1373.625 mw

7.7.7 Total Active Power 4699.290 mw 7000 mw max.

7.8 READ COMPLETE TIMING

7.8.5 Delay 395 ns 500 ns max.
Duration 320 ns 250 ns min 450 ns max.
### READ COMPLETE/DATA OUTPUT TIMING

<table>
<thead>
<tr>
<th>DO</th>
<th>Status</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>DO-0</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-1</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-2</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-3</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-4</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-5</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-6</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-7</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-8</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-9</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-10</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-11</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-12</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-13</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-14</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-15</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-16</td>
<td>OK</td>
<td>REJECT</td>
</tr>
<tr>
<td>DO-17</td>
<td>OK</td>
<td>REJECT</td>
</tr>
</tbody>
</table>

**Limitations:**

Refer to test proc.
S/N 104

Date of Test 5/28/75

Tested By

Limits

7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?
No
Yes __ Address ___ Bits ___ 0 errors

7.9.4 Did an error occur?
No
Yes __ Address ___ Bits ___ 0 errors

7.9.10 Did an error occur?
No
Yes __ Address ___ Bits ___ 0 errors

7.9.16 Did an error occur?
No
Yes __ Address ___ Bits ___ 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?
No
Yes __ Address ___ Bits ___ 0 errors

7.10.7 Did an error occur?
a) No
Yes __ Address ___ Bits ___ 0 errors
b) No  
   Yes ______ Address ______ Bits ______ 0 errors

c) No  
   Yes ______ Address ______ Bits ______ 0 errors

7.11  NON-VOLATILITY TEST

7.11.7  Did an error occur?

 &

7.11.9  No  
   Yes ______ Address ______ Bits ______ 0 errors

7.12  MEMORY SELECT TEST

7.12.3  Address 0000 (Octal) 0000

7.12.4  Address 0001 0000 (Octal) 0000
        0010 0000 (Octal) 0000
        0011 0000 (Octal) 0000
        0100 0000 (Octal) 0000
        0101 0000 (Octal) 0000
        0110 0000 (Octal) 0000
        0111 0000 (Octal) 0000
        1000 0000 (Octal) 0000
        1001 0000 (Octal) 0000
        1010 0000 (Octal) 0000
S/N 104

Date of Test 5/28/75

Tested By

Limits

Address 1011 0000 (Octal) 0000
1100 0000 (Octal) 0000
1101 0000 (Octal) 0000
1110 0000 (Octal) 0000

7.12.6 Did an error occur?
No X
Yes Address Bits 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?
No X
Yes Address Bits 0 errors

7.13.3 Did an error occur?
No X
Yes Address Bits 0 errors
7.13.4

a) Did an error occur?
   No  
   Yes ___ Address ___ Bit ___  0 errors

b) Did an error occur?
   No  
   Yes ___ Address ___ Bit ___  0 errors
8. TEMPERATURE TEST

8.2.1 TIME 7:00

8.2.2 LOW TEMPERATURE

THERMISTOR RESISTANCE

<table>
<thead>
<tr>
<th>TIME</th>
<th>LIMITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>150 MINUTES</td>
<td>200 K OHMS</td>
</tr>
<tr>
<td>160 MINUTES</td>
<td>204 K OHMS % CHANGE 2%</td>
</tr>
<tr>
<td>170 MINUTES</td>
<td>K OHMS % CHANGE</td>
</tr>
<tr>
<td>180 MINUTES</td>
<td>K OHMS % CHANGE</td>
</tr>
<tr>
<td>190 MINUTES</td>
<td>K OHMS % CHANGE</td>
</tr>
</tbody>
</table>

8.2.3 DID AN ERROR OCCUR?

| NO | X |

YES ADDRESS BITS 0 ERRORS

8.2.4 -6.1 V VOLTAGE 6.404 VOLTS +5 V VOLTAGE 5.249 VOLTS

-6.1 V CURRENT 14.0 ma +5 V CURRENT 10.8 ma

-6.1 V POWER 89.656 mw +5 V POWER 56.672 mw

TOTAL MEMORY IDLE POWER 146.345 mw 170 mw MAX

8.2.5 -6.1 V VOLTAGE 6.404 VOLTS +5 V VOLTAGE 5.249 VOLTS

-6.1 V CURRENT 25.4 ma +5 V CURRENT 4.85 ma

-6.1 V POWER 162.957 mw +5 V POWER 345.345 mw

TOTAL MEMORY OPERATING POWER 522.479 mw 7000 mw MAX
8.2.6 DID AN ERROR OCCUR?

No X

Yes ___ ADDRESS _____ BIT _____ 0 ERRORS

8.2.8 WC a) DID AN ERROR OCCUR?

No X

Yes ___ ADDRESS _____ BIT _____ 0 ERRORS

WC b) DID AN ERROR OCCUR?

No X

Yes ___ ADDRESS _____ BIT _____ 0 ERRORS

WC c) DID AN ERROR OCCUR?

No X

Yes ___ ADDRESS _____ BIT _____ 0 ERRORS

WC d) DID AN ERROR OCCUR?

No X

Yes ___ ADDRESS _____ BIT _____ 0 ERRORS

8.2.11 WC a) DID AN ERROR OCCUR?

No X

Yes ___ ADDRESS _____ BIT _____ 0 ERRORS
**8.2.11** (Cont.)

**WC b) DID AN ERROR OCCUR?**

<table>
<thead>
<tr>
<th>NO</th>
<th>ADDRESS</th>
<th>BIT</th>
<th>O ERRORS</th>
</tr>
</thead>
<tbody>
<tr>
<td>YES</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**WC c) DID AN ERROR OCCUR?**

<table>
<thead>
<tr>
<th>NO</th>
<th>ADDRESS</th>
<th>BIT</th>
<th>O ERRORS</th>
</tr>
</thead>
<tbody>
<tr>
<td>YES</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**WC d) DID AN ERROR OCCUR?**

<table>
<thead>
<tr>
<th>NO</th>
<th>ADDRESS</th>
<th>BIT</th>
<th>O ERRORS</th>
</tr>
</thead>
<tbody>
<tr>
<td>YES</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**8.3** INTERMEDIATE TEMPERATURE TEST

**TIME** 10:16

<table>
<thead>
<tr>
<th>TIME</th>
<th>THERMISTOR READING</th>
<th>DID ANY ERROR OCCUR?</th>
<th>O ERRORS</th>
</tr>
</thead>
<tbody>
<tr>
<td>10:24</td>
<td>13.6 K</td>
<td>X</td>
<td>YES</td>
</tr>
<tr>
<td>10:36</td>
<td>2.21 G</td>
<td>X</td>
<td>YES</td>
</tr>
<tr>
<td>11:46</td>
<td>3.47 G</td>
<td>X</td>
<td>YES</td>
</tr>
<tr>
<td>11:56</td>
<td>1.7 G</td>
<td>X</td>
<td>YES</td>
</tr>
<tr>
<td>11:57</td>
<td>2.17 G</td>
<td>X</td>
<td>YES</td>
</tr>
<tr>
<td>11:58</td>
<td>4.64 G</td>
<td>X</td>
<td>YES</td>
</tr>
<tr>
<td>11:59</td>
<td>3.41 G</td>
<td>X</td>
<td>YES</td>
</tr>
<tr>
<td>12:00</td>
<td>2.87 G</td>
<td>X</td>
<td>YES</td>
</tr>
<tr>
<td>12:01</td>
<td>2.69 G</td>
<td>X</td>
<td>YES</td>
</tr>
<tr>
<td>12:02</td>
<td>1.71 G</td>
<td>X</td>
<td>YES</td>
</tr>
</tbody>
</table>
S/N 104

DATE OF TEST 5/29/75

TESTED BY

8.3.3 TIME 11:30

8.4

50 MINUTES ——— K OHMS

60 MINUTES ——— K OHMS % CHANGE

70 MINUTES ——— K OHMS % CHANGE

80 MINUTES 1.51 K OHMS % CHANGE

90 MINUTES 1.61 K OHMS % CHANGE

8.4.1

-6.1 V VOLTAGE 6.1403 VOLTS +5 V VOLTAGE 5.256 VOLTS

-6.1 V CURRENT 7.1 ma. +5 V CURRENT 12.0 ma

-6.1 V POWER 45.443 mw +5 V POWER 63.022 mw

TOTAL MEMORY IDLE POWER 103.533 mw 170 mw MAX

8.4.2 DID AN ERROR OCCUR?

NO

YES ADDRESS BIT 0 ERRORS

8.4.3

-6.1 V VOLTAGE 6.400 VOLTS +5 V VOLTAGE 5.258 VOLTS

-6.1 V CURRENT 2.75 ma. +5 V VOLTAGE 790 ma

-6.1 V POWER 750.2 mw 1760 +5 V POWER 453.62 mw 4153.1%

TOTAL MEMORY OPERATING POWER 7000 mw MAX

8.4.4 DID AN ERROR OCCUR?

NO

YES ADDRESS BIT 0 ERRORS

8.4.5

-6.1 V VOLTAGE 6.410 VOLTS +5 V VOLTAGE 5.258 VOLTS

-6.1 V CURRENT 2.75 ma. +5 V VOLTAGE 790 ma

-6.1 V POWER 750.2 mw 1760 +5 V POWER 453.62 mw 4153.1%

TOTAL MEMORY OPERATING POWER 7000 mw MAX

8.4.6 DID AN ERROR OCCUR?

NO

YES ADDRESS BIT 0 ERRORS

MOTOROLA INC.

Government Electronics Division

8301 EAST McDOWELL ROAD

SCOTTSDALE, ARIZONA 85257

SIZE CODE IDENT NO. DWG NO. 12-P13721D

SCALE REVISION SHEET 19
8.4.4 (Cont.)

WC b) Did an error occur?
No
Yes

WC c) Did an error occur?
No
Yes

WC d) Did an error occur?
No
Yes

8.4.6
WC a) Did an error occur?
No
Yes

WC b) Did an error occur?
No
Yes

WC c) Did an error occur?
No
Yes

WC d) Did an error occur?
No
Yes

8.4.7 Did an error occur?
No
Yes
9. VACUUM TEST

9.2 Did Any Bit Errors Occur?

No

Yes Address ________ Bits ________ 0 Errors

9.2.1 Fast Decompression

Date 6-3-75

Tested by

Did Any Bit Errors Occur?

No

Yes Address ________ Bits ________ 0 Errors

9.2.2 Hard Vacuum

Date 6-3-75

Tested by

Did Any Bit Errors Occur?

No

Yes Address ________ Bits ________ 0 Errors

10. VIBRATION TEST

Date 6-5-75

Tested by

SINE SWEEP

Axis X - Did Any Bit Errors Occur?

No

Yes Freq Address ________ Bits ________ 0 Errors
### Axis Y - Did Any Bit Error Occur?

<table>
<thead>
<tr>
<th>No</th>
<th>Freq</th>
<th>Address</th>
<th>Bits</th>
<th>0 Errors</th>
</tr>
</thead>
</table>

### Axis Z - Did Any Bit Errors Occur?

<table>
<thead>
<tr>
<th>No</th>
<th>Freq</th>
<th>Address</th>
<th>Bits</th>
<th>0 Errors</th>
</tr>
</thead>
</table>

#### RANDOM VIBRATION

### Axis X - Did Any Bit Errors Occur?

<table>
<thead>
<tr>
<th>No</th>
<th>Freq</th>
<th>Address</th>
<th>Bits</th>
<th>0 Errors</th>
</tr>
</thead>
</table>

### Axis Y - Did Any Bit Errors Occur?

<table>
<thead>
<tr>
<th>No</th>
<th>Freq</th>
<th>Address</th>
<th>Bits</th>
<th>0 Errors</th>
</tr>
</thead>
</table>

### Axis Z - Did Any Bit Errors Occur?

<table>
<thead>
<tr>
<th>No</th>
<th>Freq</th>
<th>Address</th>
<th>Bits</th>
<th>0 Errors</th>
</tr>
</thead>
</table>

#### SHOCK TEST

1. **Date:** 5-30-75
2. **Tested By:**

6 MILISECOND DURATION SHOCK

<table>
<thead>
<tr>
<th>Y Direction - Did Any Bit Errors Occur?</th>
<th>No</th>
<th>Address</th>
<th>Bits</th>
<th>0 Errors</th>
</tr>
</thead>
</table>

---

**MOTOROLA INC.**

Government Electronics Division

8701 E. McDowell Road
Scottsdale, Arizona 85252

**SIZE** | **CODE IDENT NO.** | **DWG NO.**
---|---|---
A | 94990 | 12-P13721D

**SCALE** | **REVISION** | **SHEET**
---|---|---
A | | 22
Z Direction - Did Any Bit Errors Occur?

No

Yes ______ Address _______ Bits _______ 0 Errors

X Direction - Did Any Bit Errors Occur?

No

Yes ______ Address _______ Bits _______ 0 Errors

12 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No

Yes ______ Address _______ Bits _______ 0 Errors

Z Direction - Did Any Bit Errors Occur?

No

Yes ______ Address _______ Bits _______ 0 Errors

X Direction - Did Any Bit Errors Occur?

No

Yes ______ Address _______ Bits _______ 0 Errors

MOTOROLA INC.

Government Electronics Division

8201 E. McDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

SIZE CODE IDENT NO. DWG NO.
A 94990 12-P13721D

SCALE REVISION SHEET 23
7.4 CHASSIS ISOLATION

Impedance \( \geq 9 \) mho

7.5 INPUT SIGNAL LOADING

7.5.2 Current from INITIATE PULSE to Gnd \( 1.38 \) ma
Current from 2.4V to INITIATE PULSE \( 1.31 \) \( \mu \)A

7.5.3 Current from MEM SEL 1 to Gnd \( 1.38 \) ma
Current from 2.4V to MEM SEL 1 \( 1.97 \) \( \mu \)A

7.5.4 Current from MEM SEL 2 to Gnd \( 1.39 \) ma
Current from 2.4V to MEM SEL 2 \( 1.36 \) \( \mu \)A

7.5.5 Current from READ/WRITE to Gnd \( 1.002 \) ma
Current from 2.4V to READ/WRITE \( 1.26 \) \( \mu \)A

7.5.6 Current from ADDRESS \( 2^0 \) to Gnd \( 0.99 \) ma
Current from 2.4V to ADDRESS \( 2^0 \) \( 6.34 \) \( \mu \)A
S/N 104

Date of Test 6/6/75

Tested By

Limits

Current from ADDRESS 2¹ to Gnd .90 ma ≤ 2 ma
Current from 2.4V to ADDRESS 2¹ 5.93 µa ≤ 20 µa
Current from ADDRESS 2² to Gnd .97 ma ≤ 2 ma
Current from 2.4V to ADDRESS 2² 6.76 µa ≤ 20 µa
Current from ADDRESS 2³ to Gnd .90 ma ≤ 2 ma
Current from 2.4V to ADDRESS 2³ 7.40 µa ≤ 20 µa
Current from ADDRESS 2⁴ to Gnd .98 ma ≤ 2 ma
Current from 2.4V to ADDRESS 2⁴ 7.83 µa ≤ 20 µa
<table>
<thead>
<tr>
<th>Address</th>
<th>Current</th>
<th>Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>25 to Gnd</td>
<td>0.89 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>2.4V to 25</td>
<td>5.42 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>6 to Gnd</td>
<td>0.89 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>2.4V to 6</td>
<td>5.52 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>7 to Gnd</td>
<td>0.96 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>2.4V to 7</td>
<td>6.53 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>8 to Gnd</td>
<td>0.93 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>2.4V to 8</td>
<td>1.10 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>9 to Gnd</td>
<td>0.92 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>2.4V to 9</td>
<td>1.09 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>10 to Gnd</td>
<td>0.97 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>2.4V to 10</td>
<td>1.27 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>11 to Gnd</td>
<td>0.97 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>2.4V to 11</td>
<td>1.30 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>DATA IN Bit 0 to Gnd</td>
<td>1.04 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>2.4V to DATA IN Bit 0</td>
<td>106 μA</td>
<td>≤ 20 μA</td>
</tr>
<tr>
<td>Current from DATA IN BIT 1 to Gnd</td>
<td>1.06 mA</td>
<td>( \leq 2 ) mA</td>
</tr>
<tr>
<td>----------------------------------</td>
<td>---------</td>
<td>-----------------</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 1</td>
<td>7.32 ( \mu )A</td>
<td>( \leq 20 \mu )A</td>
</tr>
<tr>
<td>Current from DATA IN BIT 2 to Gnd</td>
<td>1.06 mA</td>
<td>( \leq 2 ) mA</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 2</td>
<td>0.71 ( \mu )A</td>
<td>( \leq 20 \mu )A</td>
</tr>
<tr>
<td>Current from DATA IN BIT 3 to Gnd</td>
<td>1.03 mA</td>
<td>( \leq 2 ) mA</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 3</td>
<td>9.22 ( \mu )A</td>
<td>( \leq 20 \mu )A</td>
</tr>
<tr>
<td>Current from DATA IN BIT 4 to Gnd</td>
<td>1.02 mA</td>
<td>( \leq 2 ) mA</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 4</td>
<td>9.16 ( \mu )A</td>
<td>( \leq 20 \mu )A</td>
</tr>
<tr>
<td>Current from DATA IN BIT 5 to Gnd</td>
<td>1.04 mA</td>
<td>( \leq 2 ) mA</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 5</td>
<td>8.97 ( \mu )A</td>
<td>( \leq 20 \mu )A</td>
</tr>
<tr>
<td>Current from DATA IN BIT 6 to Gnd</td>
<td>1.06 mA</td>
<td>( \leq 2 ) mA</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 6</td>
<td>7.65 ( \mu )A</td>
<td>( \leq 20 \mu )A</td>
</tr>
<tr>
<td>Current from DATA IN BIT 7 to Gnd</td>
<td>1.04 mA</td>
<td>( \leq 2 ) mA</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 7</td>
<td>7.31 ( \mu )A</td>
<td>( \leq 20 \mu )A</td>
</tr>
<tr>
<td>Current from DATA IN BIT 8 to Gnd</td>
<td>1.03 mA</td>
<td>( \leq 2 ) mA</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 8</td>
<td>7.73 ( \mu )A</td>
<td>( \leq 20 \mu )A</td>
</tr>
<tr>
<td>Current from DATA IN BIT 9 to Gnd</td>
<td>0.97 mA</td>
<td>( \leq 2 ) mA</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 9</td>
<td>8.09 ( \mu )A</td>
<td>( \leq 20 \mu )A</td>
</tr>
</tbody>
</table>
Current from DATA IN BIT 10 to Gnd $0.98 \text{ ma}$
Current from 2.4V to DATA IN BIT 10 $8.89 \mu\text{a}$

Current from DATA IN BIT 11 to Gnd $0.99 \text{ ma}$
Current from 2.4V to DATA IN BIT 11 $8.05 \mu\text{a}$

Current from DATA IN BIT 12 to Gnd $1.04 \text{ ma}$
Current from 2.4V to DATA IN BIT 12 $9.43 \mu\text{a}$

Current from DATA IN BIT 13 to Gnd $1.04 \text{ ma}$
Current from 2.4V to DATA IN BIT 14 $9.12 \mu\text{a}$

Current from DATA IN BIT 14 to Gnd $1.05 \text{ ma}$
Current from 2.4V to DATA IN BIT 14 $9.93 \mu\text{a}$

Current from DATA IN BIT 15 to Gnd $1.06 \text{ ma}$
Current from 2.4V to DATA IN BIT 15 $6.09 \mu\text{a}$

Current from DATA IN BIT 16 to Gnd $1.03 \text{ ma}$
Current from 2.4V to DATA IN BIT 17 $6.16 \mu\text{a}$

Current from DATA IN BIT 17 to Gnd $1.05 \text{ ma}$
Current from 2.4V to DATA IN BIT 17 $7.24 \mu\text{a}$

**Limits**

$\leq 2 \text{ ma}$

$\leq 20 \mu\text{a}$
### VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS

#### 7.6.3 READ COMPLETE voltage

<table>
<thead>
<tr>
<th>Voltage (mv)</th>
<th>Limit (mv)</th>
</tr>
</thead>
<tbody>
<tr>
<td>68</td>
<td>≤ 100</td>
</tr>
</tbody>
</table>

#### 7.6.4 DATA OUT BIT 0 voltage

<table>
<thead>
<tr>
<th>Voltage (mv)</th>
<th>Limit (mv)</th>
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</thead>
<tbody>
<tr>
<td>40</td>
<td>≤ 100</td>
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</tbody>
</table>

#### 7.6.4 DATA OUT BIT 1 voltage

<table>
<thead>
<tr>
<th>Voltage (mv)</th>
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</thead>
<tbody>
<tr>
<td>40</td>
<td>≤ 100</td>
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</tbody>
</table>

#### 7.6.4 DATA OUT BIT 2 voltage

<table>
<thead>
<tr>
<th>Voltage (mv)</th>
<th>Limit (mv)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>≤ 100</td>
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#### 7.6.4 DATA OUT BIT 3 voltage

<table>
<thead>
<tr>
<th>Voltage (mv)</th>
<th>Limit (mv)</th>
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</thead>
<tbody>
<tr>
<td>30</td>
<td>≤ 100</td>
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#### 7.6.4 DATA OUT BIT 4 voltage

<table>
<thead>
<tr>
<th>Voltage (mv)</th>
<th>Limit (mv)</th>
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<tbody>
<tr>
<td>25</td>
<td>≤ 100</td>
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#### 7.6.4 DATA OUT BIT 5 voltage

<table>
<thead>
<tr>
<th>Voltage (mv)</th>
<th>Limit (mv)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>≤ 100</td>
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</table>

#### 7.6.4 DATA OUT BIT 6 voltage

<table>
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<tr>
<th>Voltage (mv)</th>
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</thead>
<tbody>
<tr>
<td>2</td>
<td>≤ 100</td>
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</tbody>
</table>

#### 7.6.4 DATA OUT BIT 7 voltage

<table>
<thead>
<tr>
<th>Voltage (mv)</th>
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</tr>
</thead>
<tbody>
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<td>≤ 100</td>
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</tbody>
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#### 7.6.4 DATA OUT BIT 8 voltage

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<th>Voltage (mv)</th>
<th>Limit (mv)</th>
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</thead>
<tbody>
<tr>
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<td>≤ 100</td>
</tr>
</tbody>
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#### 7.6.4 DATA OUT BIT 9 voltage

<table>
<thead>
<tr>
<th>Voltage (mv)</th>
<th>Limit (mv)</th>
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</thead>
<tbody>
<tr>
<td>2</td>
<td>≤ 100</td>
</tr>
</tbody>
</table>

#### 7.6.4 DATA OUT BIT 10 voltage

<table>
<thead>
<tr>
<th>Voltage (mv)</th>
<th>Limit (mv)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>≤ 100</td>
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</tbody>
</table>

#### 7.6.4 DATA OUT BIT 11 voltage

<table>
<thead>
<tr>
<th>Voltage (mv)</th>
<th>Limit (mv)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>≤ 100</td>
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</table>

#### 7.6.4 DATA OUT BIT 12 voltage

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<th>Voltage (mv)</th>
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</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>≤ 100</td>
</tr>
</tbody>
</table>

#### 7.6.4 DATA OUT BIT 13 voltage

<table>
<thead>
<tr>
<th>Voltage (mv)</th>
<th>Limit (mv)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>≤ 100</td>
</tr>
</tbody>
</table>

#### 7.6.4 DATA OUT BIT 14 voltage

<table>
<thead>
<tr>
<th>Voltage (mv)</th>
<th>Limit (mv)</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>≤ 100</td>
</tr>
</tbody>
</table>

#### 7.6.4 DATA OUT BIT 15 voltage

<table>
<thead>
<tr>
<th>Voltage (mv)</th>
<th>Limit (mv)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>≤ 100</td>
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</tbody>
</table>

#### 7.6.4 DATA OUT BIT 16 voltage

<table>
<thead>
<tr>
<th>Voltage (mv)</th>
<th>Limit (mv)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>≤ 100</td>
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</tbody>
</table>

#### 7.6.4 DATA OUT BIT 17 voltage

<table>
<thead>
<tr>
<th>Voltage (mv)</th>
<th>Limit (mv)</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>≤ 100</td>
</tr>
</tbody>
</table>
7.7 POWER CONSUMPTION (25°C)

7.7.1 Memory +5V Voltage 5.008 Volts
Memory -6.1V voltage -6.016 Volts
+5V Current 10.1 ma
+5V Power 50.6 mw

7.7.2 Memory -6.1V Current 3.1 ma
Memory -6.1V Power 18.7 mw

7.7.3 Total Memory Idle Power 69.3 mw

7.7.5 Memory +5V Voltage 5.009 Volts
Memory -6.1V Voltage -6.109 Volts
+5V Current 650 ma
+5V Power 3255.9 mw

7.7.6 Memory -6.1V Current 220 ma
Memory -6.1V Power 1344.0 mw

7.7.7 Total Active Power 4599.9 mw

7.8 READ COMPLETE TIMING

7.8.5 Delay 390 ns
Duration 320 ns
<table>
<thead>
<tr>
<th>S/N</th>
<th>Date of Test</th>
</tr>
</thead>
<tbody>
<tr>
<td>104</td>
<td>6/6/75</td>
</tr>
</tbody>
</table>

**Tested by** [Signature]

---

### READ COMPLETE/DATA OUTPUT TIMING

<table>
<thead>
<tr>
<th>DO</th>
<th>Status</th>
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<tbody>
<tr>
<td>DO-0</td>
<td>OK REJECT</td>
</tr>
<tr>
<td>DO-1</td>
<td>OK REJECT</td>
</tr>
<tr>
<td>DO-2</td>
<td>OK REJECT</td>
</tr>
<tr>
<td>DO-3</td>
<td>OK REJECT</td>
</tr>
<tr>
<td>DO-4</td>
<td>OK REJECT</td>
</tr>
<tr>
<td>DO-5</td>
<td>OK REJECT</td>
</tr>
<tr>
<td>DO-6</td>
<td>OK REJECT</td>
</tr>
<tr>
<td>DO-7</td>
<td>OK REJECT</td>
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<tr>
<td>DO-8</td>
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<td>DO-11</td>
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<td>DO-12</td>
<td>OK REJECT</td>
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<tr>
<td>DO-13</td>
<td>OK REJECT</td>
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<td>DO-14</td>
<td>OK REJECT</td>
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<tr>
<td>DO-15</td>
<td>OK REJECT</td>
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<tr>
<td>DO-16</td>
<td>OK REJECT</td>
</tr>
<tr>
<td>DO-17</td>
<td>OK REJECT</td>
</tr>
</tbody>
</table>

**Limits**

**Refer to Test Proc.**
7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?
No  X
Yes ___ Address ___ Bits ______ 0 errors

7.9.4 Did an error occur?
No  X
Yes ___ Address ___ Bits ______ 0 errors

7.9.10 Did an error occur?
No  X
Yes ___ Address ___ Bits ______ 0 errors

7.9.16 Did an error occur?
No  X
Yes ___ Address ___ Bits ______ 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?
No  X
Yes ___ Address ___ Bits ______ 0 errors

7.10.7 Did an error occur?
a) No  X
   Yes ___ Address ___ Bits ______ 0 errors
S/N 104

Date of Test 6/6/75
Tested By

Limits

b) No 

Yes Address Bits 0 errors

c) No 

Yes Address Bits 0 errors

7.11 NON-VOLATILITY TEST

7.11.7 Did an error occur?

&

7.11.9 No 

Yes Address Bits 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal) 0000

7.12.4 Address 0001 0000 (Octal) 0000

0010 0000 (Octal) 0000

0011 0000 (Octal) 0000

0100 0000 (Octal) 0000

0101 0000 (Octal) 0000

0110 0000 (Octal) 0000

0111 0000 (Octal) 0000

1000 0000 (Octal) 0000

1001 0000 (Octal) 0000

1010 0000 (Octal) 0000
S/N 104

Address 1011 0000 (Octal)
       1100 0000 (Octal)
       1101 0000 (Octal)
       1110 0000 (Octal)

7.12.6 Did an error occur?
   No ☒
   Yes ☐ Address ☐ Bits ☐ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?
   No ☒
   Yes ☐ Address ☐ Bits ☐ 0 errors

7.13.3 Did an error occur?
   No ☒
   Yes ☐ Address ☐ Bits ☐ 0 errors
7.13.4 a) Did an error occur?
   No X
   Yes Address Bit 0 errors

b) Did an error occur?
   No X
   Yes Address Bit 0 errors
PROJECT 4601-400 UNIT P-W Memory SER. NO. 104

X&Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1.25 Hz SCAN RATE 1.25 Hz AVG. TIME 10 SECONDS
2.10 Hz SCAN RATE 2.25 Hz AVG. TIME 20 SECONDS
3.50 Hz SCAN RATE 3.50 Hz AVG. TIME 10 SECONDS
4.20 Hz SCAN RATE 2.25 Hz AVG. TIME 10 SECONDS

FREQ. RANGE 1) 15-20 dB 20-40 dB 3) 40-100 dB 4) 100-2K Hz

VIBRATION DATE 5 June 1975
DATE ANALYZED 5 June 1975 Pete Martin

REMARKS dB as shown

PRECEDED PAGE BLANK NOT FILMED ORIGINAL PAGE IS OF POOR QUALITY
PROJECT 4601-400 UNIT P-W Memory SER. NO. 104

X&Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1.5 Hz SCAN RATE 1.25 Hz AVG. TIME 10 SECONDS
2.10 Hz SCAN RATE 2.25 Hz AVG. TIME 210 SECONDS
3.20 Hz SCAN RATE 3.25 Hz AVG. TIME 310 SECONDS
4.50 Hz SCAN RATE 1.25 Hz AVG. TIME 410 SECONDS

FREQ. RANGE:
1. 15-20 Hz DATA POINT 5 AVERAGE NO.
2. 20-40 Hz CONTEXT SHAPE DATA POINT 5
3. 40-100 Hz CONTEXT SHAPE DATA POINT 5
4. 100-2 KHz CONTEXT SHAPE DATA POINT 5

VIBRATION DATE: 5 June 1975
DUTY ANALYSIS: 5 June 1975
PETE MARTIN

REMARKS:
13 dB as shown.
PROJECT 4601-400 UNIT P-W Memory SER. NO. 104

Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1.5 HZ SCAN RATE 1..125 AVG. TIME 10 SECONDS
2.10 HZ SCAN RATE 2.25 HZ AVG. TIME 210 SECONDS
3.20 HZ SCAN RATE 3.5 HZ AVG. TIME 310 SECONDS
4.50 HZ SCAN RATE 4.5 HZ AVG. TIME 410 SECONDS

FREQUENCY RANGE 1-500 HZ
MOTOROLA SPECIFICATION NO.

VIBRATION DATE 3 June 1975
DATA ANALYST 5 June 1975 Pete Martin
VIBRATION TO ENCAPSULATE LEVEL NA
RELAX Response of top cover

Power Spectral Density (g²/Hz)

Frequency (Hz)
### Vibration Test

**Date:** 5 June 75  
**Project:** 4601-400  
**Unit:** Potted Wire Memory  
**Control No.:** 01-02  
**W.O. No.:** 3041  
**Operator:** Pete Martian  
**Observer:** Lee Stulden  
**Cycle Time:** 4.5 min  
**Freq.:** 5 to 2000 Hz  
**Remarks:**

<table>
<thead>
<tr>
<th>Axis</th>
<th>Run No.</th>
<th>Time Start</th>
<th>Time Stop</th>
<th>Vibration Time</th>
<th>Unit No.</th>
<th>Displacement Inches D.A.</th>
<th>Acceleration X RMS</th>
<th>Acceleration X PK</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Z</td>
<td>12:34</td>
<td>13:46</td>
<td>2 min</td>
<td>104</td>
<td>NA</td>
<td>5.615 G</td>
<td>5.6 G RMS</td>
<td></td>
<td>shaped random</td>
</tr>
<tr>
<td>Z</td>
<td>13:09</td>
<td>13:14</td>
<td>4.3 min</td>
<td>104</td>
<td>.33</td>
<td>10.05</td>
<td>75 G RMS</td>
<td></td>
<td>sine sweep 5-110-2KHz</td>
</tr>
<tr>
<td>X</td>
<td>13:20</td>
<td>13:25</td>
<td>4.3 min</td>
<td>104</td>
<td>.33</td>
<td>10.05</td>
<td>75 G RMS</td>
<td></td>
<td>sine sweep 5-110-2KHz</td>
</tr>
<tr>
<td>Y</td>
<td>13:27</td>
<td>13:34</td>
<td>2 min</td>
<td>104</td>
<td>NA</td>
<td>5.615 G</td>
<td>5.6 G RMS</td>
<td></td>
<td>shaped random</td>
</tr>
<tr>
<td>X</td>
<td>14:17</td>
<td>14:47</td>
<td>2 min</td>
<td>104</td>
<td>NA</td>
<td>5.615 G</td>
<td>5.6 G RMS</td>
<td></td>
<td>shaped random</td>
</tr>
<tr>
<td>Y</td>
<td>14:42</td>
<td>14:53</td>
<td>4.3 min</td>
<td>104</td>
<td>.33</td>
<td>10.05</td>
<td>75 G RMS</td>
<td></td>
<td>sine sweep 5-110-2KHz</td>
</tr>
<tr>
<td>TIME</td>
<td>PRESSURE (mm Hg A)</td>
<td>Remarks</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1:50</td>
<td>Pt 42</td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>2:53</td>
<td>7 MMH</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6:10</td>
<td>6.3 x 10⁻⁵</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9:30</td>
<td>3 x 10⁻⁵</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10:00</td>
<td>2 x 10⁻⁵</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10:30</td>
<td>1.4 x 10⁻⁵</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11:00</td>
<td>1.1 x 10⁻⁵</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11:15</td>
<td>4.9 x 10⁻⁶</td>
<td>END TEST</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11:20</td>
<td>0.9 x 10⁻⁶</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>
SHOCK TEST
(DROP)

PROJECT 4101-400
DATE 5-30-75

TYPE OF TEST
☑ MODULAR IMPACT
☐ FREE FALL DROP

SHEET 1 OF 1
W.O. NO. 3040
CONTROL NO. 11
UNIT P W. M.

SERIAL NO. 104
OPERATOR Lee M.
OBSERVER Lee F. Johnson

VIBRATION MOUNTS none

NO. OF DROPS PER FACE 2
TOTAL NO. OF DROPS 6

ACCELERATION 30 G'S
PULSE DURATION 6.12 MS

SPEC DETAILS 12-P13722 D

DROP HEIGHT 12 X 14 X IN.
PROGRAMMER PRESSURE NA P.S.I.

TYPE OF WAVESHAPE Half sine
BANDPASS FILTER 2 LOY FR. Hz
3 TO HIGH FR. Hz

REMARKS 3 degrees 6 ms 3 degrees at 12 ms

PAD AND PLATE CONFIGURATION

<table>
<thead>
<tr>
<th>ITEM</th>
<th>PART NO.</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>14RL2357</td>
<td>o'hem plate</td>
</tr>
<tr>
<td>2</td>
<td>14RL2756</td>
<td>1&quot; red gum</td>
</tr>
<tr>
<td>3</td>
<td>14RL2357</td>
<td>o'hem plate</td>
</tr>
</tbody>
</table>

Axis for 12 ms:

1-8 x 1/4 plastic
2-8 x 4/14 in
3-8 x 4/14 in
3-1 blue channel
1-1 1/4 in open

AXIS FACE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
2 / / / / / / / / / / / / / / / / / / / / / / / / / / / / / / / C
1 / / / / / / / / / / / / / / / / / / / / / / / / / / / / / / / D
2 / / / / / / / / / / / / / / / / / / / / / / / / / / / / / / / E

test complete
ATTACHMENT IV

ACCEPTANCE TEST DATA SHEET
LOW POWER RANDOM ACCESS
SPACECRAFT MEMORY
PART NO. 12-P13721D
SERIAL NUMBER 105
(35 PAGES)
<table>
<thead>
<tr>
<th>APPLICATION</th>
<th>REVISIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>XT ASSEMBLY</td>
<td>USED ON</td>
</tr>
<tr>
<td></td>
<td>LTHR</td>
</tr>
<tr>
<td></td>
<td>DESCRIPTION</td>
</tr>
<tr>
<td>X1</td>
<td>Initial Release</td>
</tr>
<tr>
<td>X2</td>
<td>Incorporated changes prior to First Usage</td>
</tr>
<tr>
<td>X3</td>
<td>Change -6.9V to -6.1V</td>
</tr>
<tr>
<td>X4</td>
<td>Change 6000mw to 7000mw, pages 10, 17, 19, 30, Change weight from 6.0 to 6.5 pounds, page 2.</td>
</tr>
<tr>
<td>X5</td>
<td>Add weight 5.8 pounds for magnesium chassis MCO S7835.</td>
</tr>
<tr>
<td>X6</td>
<td>Revised per MCO S7845</td>
</tr>
</tbody>
</table>

*ASTERISK INDICATES DATA WHICH IS NONMANDATORY - FOR INFORMATION ONLY.*

**APPLICATION**

- Initial Release
- Incorporated changes prior to First Usage
- Change -6.9V to -6.1V
- Change 6000mw to 7000mw, pages 10, 17, 19, 30, Change weight from 6.0 to 6.5 pounds, page 2.
- Add weight 5.8 pounds for magnesium chassis MCO S7835.
- Revised per MCO S7845

**REV STATUS**

- REV: 1
- SHEET: 1
- SHEETS: 1

**MATERIAL:**

- CONTR: NAS5-23163
- NO: NAS5-20576

**ACCEPTANCE TEST DATA SHEET,**

LOW POWER RANDOM ACCESS SPACECRAFT MEMORY, PART NO. 01-P13701D

**Scale:** SHEET 1 OF 35
1. **SCOPE**

This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

2. **REFERENCE INFORMATION**

3. **SPECIFICATIONS APPLICABLE**

   2.1 Low Power Random Access Spacecraft Memory

   12-P13722D Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. **TEST DATA**

   Unit S/N 105

   Start Date of Tests 5/15/75

   Tested by

4. **EQUIVALENT TEST EQUIPMENT**

   DC milliammeter HP 428A 0-1A

   Digital voltmeter Fluke 8120A (Multimeter)

   Counter HP 5245

4. **PHYSICAL CHARACTERISTICS**

6.1 **WEIGHT**

   Weight of LP-RASM $5.594$ Pounds

   Limit

   6.5 pounds (aluminum)

   5.8 pounds (magnesium)
6.2 DIMENSIONS

\[ H = 2.905 \text{ inches} \]
\[ m = 6.927 \text{ inches} \]
\[ w = 6.322 \text{ inches} \]
\[ d = 8.960 \text{ inches} \]
\[ O = 8.630 \text{ inches} \]

\[ V = H \times W \times X \times D = 158.5 \text{ inches}^3 \]

\[ \leq 160 \text{ inches}^3 \]
7.4 CHASSIS ISOLATION

Impedance: \( \geq 9 \text{ mega} \)

Limit

7.5 INPUT SIGNAL LOADING

7.5.2 Current from INITIATE PULSE to Gnd: 1.09 ma \( \leq 2 \text{ ma} \)
Current from 2.4V to INITIATE PULSE: 88 \( \mu \text{a} \) \( \leq 20 \mu \text{a} \)

7.5.3 Current from MEM SEL 1 to Gnd: 1.105 ma \( \leq 2 \text{ ma} \)
Current from 2.4V to MEM SEL 1: 61 \( \mu \text{a} \) \( \leq 20 \mu \text{a} \)

7.5.4 Current from MEM SEL 2 to Gnd: 1.09 ma \( \leq 2 \text{ ma} \)
Current from 2.4V to MEM SEL 2: 82 \( \mu \text{a} \) \( \leq 20 \mu \text{a} \)
Current from MEM SEL 3 to Gnd: 1.105 ma \( \leq 2 \text{ ma} \)
Current from 2.4V to MEM SEL 3: 82 \( \mu \text{a} \) \( \leq 20 \mu \text{a} \)

7.5.5 Current from READ/WRITE to Gnd: 1.14 ma \( \leq 2 \text{ ma} \)
Current from 2.4V to READ/WRITE: 154 \( \mu \text{a} \) \( \leq 20 \mu \text{a} \)

7.5.6 Current from ADDRESS 2 to Gnd: 2.39 ma \( \leq 2 \text{ ma} \)
Current from 2.4V to ADDRESS 2: 5.78 \( \mu \text{a} \) \( \leq 20 \mu \text{a} \)
S/N 105

Date of Test 5/5/75

Tested By

Limits

Current from ADDRESS 1 to Gnd .942 mA ≤ 2 mA
Current from 2.4V to ADDRESS 1 5.33 μA ≤ 20 μA
Current from ADDRESS 2 to Gnd 1.017 mA ≤ 2 mA
Current from 2.4V to ADDRESS 2 6.35 μA ≤ 20 μA
Current from ADDRESS 3 to Gnd .940 mA ≤ 2 mA
Current from 2.4V to ADDRESS 3 6.74 μA ≤ 20 μA
Current from ADDRESS 4 to Gnd .994 mA ≤ 2 mA
Current from 2.4V to ADDRESS 4 7.51 μA ≤ 20 μA
<table>
<thead>
<tr>
<th>Current</th>
<th>Limits</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current from ADDRESS 2⁵ to Gnd</td>
<td>2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2⁵</td>
<td>20 μA</td>
</tr>
<tr>
<td>Current from ADDRESS 2⁶ to Gnd</td>
<td>2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2⁵</td>
<td>20 μA</td>
</tr>
<tr>
<td>Current from ADDRESS 2⁷ to Gnd</td>
<td>2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2⁷</td>
<td>20 μA</td>
</tr>
<tr>
<td>Current from ADDRESS 2⁸ to Gnd</td>
<td>2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2⁸</td>
<td>20 μA</td>
</tr>
<tr>
<td>Current from ADDRESS 2⁹ to Gnd</td>
<td>2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2⁹</td>
<td>20 μA</td>
</tr>
<tr>
<td>Current from ADDRESS 2¹⁰ to Gnd</td>
<td>2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2¹⁰</td>
<td>20 μA</td>
</tr>
<tr>
<td>Current from ADDRESS 2¹¹ to Gnd</td>
<td>2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2¹¹</td>
<td>20 μA</td>
</tr>
<tr>
<td>Current from DATA IN BIT 0 to Gnd</td>
<td>2 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 0</td>
<td>20 μA</td>
</tr>
<tr>
<td>Current from DATA IN BIT 1 to Gnd</td>
<td>1.037 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 1</td>
<td>6.85 μa</td>
</tr>
<tr>
<td>Current from DATA IN BIT 2 to Gnd</td>
<td>1.052 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 2</td>
<td>2.09 μa</td>
</tr>
<tr>
<td>Current from DATA IN BIT 3 to Gnd</td>
<td>1.029 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 3</td>
<td>8.20 μa</td>
</tr>
<tr>
<td>Current from DATA IN BIT 4 to Gnd</td>
<td>1.011 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 4</td>
<td>7.20 μa</td>
</tr>
<tr>
<td>Current from DATA IN BIT 5 to Gnd</td>
<td>1.048 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 5</td>
<td>7.45 μa</td>
</tr>
<tr>
<td>Current from DATA IN BIT 6 to Gnd</td>
<td>1.016 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 6</td>
<td>5.48 μa</td>
</tr>
<tr>
<td>Current from DATA IN BIT 7 to Gnd</td>
<td>0.992 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 7</td>
<td>5.51 μa</td>
</tr>
<tr>
<td>Current from DATA IN BIT 8 to Gnd</td>
<td>0.996 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 8</td>
<td>5.83 μa</td>
</tr>
<tr>
<td>Current from DATA IN BIT 9 to Gnd</td>
<td>0.970 ma</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 9</td>
<td>6.02 μa</td>
</tr>
</tbody>
</table>
Current from DATA IN BIT 10 to Gnd 0.971 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 10 6.01 μa ≤ 20 μa
Current from DATA IN BIT 11 to Gnd 0.980 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 11 6.04 μa ≤ 20 μa
Current from DATA IN BIT 12 to Gnd 0.990 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 12 5.60 μa ≤ 20 μa
Current from DATA IN BIT 13 to Gnd 0.991 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 14 5.64 μa ≤ 20 μa
Current from DATA IN BIT 14 to Gnd 0.995 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 14 5.36 μa ≤ 20 μa
Current from DATA IN BIT 15 to Gnd 0.884 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 15 4.17 μa ≤ 20 μa
Current from DATA IN BIT 16 to Gnd 0.874 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 17 4.66 μa ≤ 20 μa
Current from DATA IN BIT 17 to Gnd 0.877 ma ≤ 2 ma
Current from 2.4V to DATA IN BIT 17 4.77 μa ≤ 20 μa

Limits
## VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS

### 7.6.3 READ COMPLETE voltage

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>20.0</td>
<td>≤ 100 mv</td>
</tr>
</tbody>
</table>

### 7.6.4 DATA OUT BIT 0 voltage

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.0</td>
<td>≤ 100 mv</td>
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</tbody>
</table>

### DATA OUT BIT 1 voltage

<table>
<thead>
<tr>
<th>Voltage</th>
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</thead>
<tbody>
<tr>
<td>10.0</td>
<td>≤ 100 mv</td>
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</tbody>
</table>

### DATA OUT BIT 2 voltage

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<tr>
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</table>

### DATA OUT BIT 3 voltage

<table>
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<tr>
<th>Voltage</th>
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</thead>
<tbody>
<tr>
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<td>≤ 100 mv</td>
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</table>

### DATA OUT BIT 4 voltage

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<tr>
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<tbody>
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</table>

### DATA OUT BIT 5 voltage

<table>
<thead>
<tr>
<th>Voltage</th>
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</tr>
</thead>
<tbody>
<tr>
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<td>≤ 100 mv</td>
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</table>

### DATA OUT BIT 6 voltage

<table>
<thead>
<tr>
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<tbody>
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<td>≤ 100 mv</td>
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</tbody>
</table>

### DATA OUT BIT 7 voltage

<table>
<thead>
<tr>
<th>Voltage</th>
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<tbody>
<tr>
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<td>≤ 100 mv</td>
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</table>

### DATA OUT BIT 8 voltage

<table>
<thead>
<tr>
<th>Voltage</th>
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</thead>
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<td>≤ 100 mv</td>
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</tbody>
</table>

### DATA OUT BIT 9 voltage

<table>
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<tr>
<th>Voltage</th>
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</thead>
<tbody>
<tr>
<td>20.0</td>
<td>≤ 100 mv</td>
</tr>
</tbody>
</table>

### DATA OUT BIT 10 voltage

<table>
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<th>Voltage</th>
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</tr>
</thead>
<tbody>
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<td>15.0</td>
<td>≤ 100 mv</td>
</tr>
</tbody>
</table>

### DATA OUT BIT 11 voltage

<table>
<thead>
<tr>
<th>Voltage</th>
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</thead>
<tbody>
<tr>
<td>20.0</td>
<td>≤ 100 mv</td>
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</tbody>
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### DATA OUT BIT 12 voltage

<table>
<thead>
<tr>
<th>Voltage</th>
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</thead>
<tbody>
<tr>
<td>20.0</td>
<td>≤ 100 mv</td>
</tr>
</tbody>
</table>

### DATA OUT BIT 13 voltage

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>20.0</td>
<td>≤ 100 mv</td>
</tr>
</tbody>
</table>

### DATA OUT BIT 14 voltage

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>20.5</td>
<td>≤ 100 mv</td>
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</table>

### DATA OUT BIT 15 voltage

<table>
<thead>
<tr>
<th>Voltage</th>
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</tr>
</thead>
<tbody>
<tr>
<td>15.0</td>
<td>≤ 100 mv</td>
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</table>

### DATA OUT BIT 16 voltage

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>25.0</td>
<td>≤ 100 mv</td>
</tr>
</tbody>
</table>

### DATA OUT BIT 17 voltage

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>25.0</td>
<td>≤ 100 mv</td>
</tr>
<tr>
<td>Section</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>-------------</td>
</tr>
<tr>
<td>7.7</td>
<td>POWER CONSUMPTION (25°C)</td>
</tr>
<tr>
<td>7.7.1</td>
<td>Memory +5V Voltage</td>
</tr>
<tr>
<td></td>
<td>Memory -6.1V Voltage</td>
</tr>
<tr>
<td></td>
<td>+5V Current</td>
</tr>
<tr>
<td></td>
<td>+5V Power</td>
</tr>
<tr>
<td>7.7.3</td>
<td>Memory -6.1V Current</td>
</tr>
<tr>
<td></td>
<td>Memory -6.1V Power</td>
</tr>
<tr>
<td>7.7.5</td>
<td>Memory +5V Voltage</td>
</tr>
<tr>
<td></td>
<td>Memory -6.1V Voltage</td>
</tr>
<tr>
<td></td>
<td>+5V Current</td>
</tr>
<tr>
<td></td>
<td>+5V Power</td>
</tr>
<tr>
<td>7.7.6</td>
<td>Memory -6.1V Current</td>
</tr>
<tr>
<td></td>
<td>Memory -6.1V Power</td>
</tr>
<tr>
<td>7.7.7</td>
<td>Total Active Power</td>
</tr>
<tr>
<td></td>
<td>Total Memory Idle Power</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>7.8</td>
<td>READ COMPLETE TIMING</td>
</tr>
<tr>
<td>7.8.5</td>
<td>Delay</td>
</tr>
<tr>
<td></td>
<td>Duration</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:** The page includes a table of electrical specifications and timing data for a device tested on 5/15/75. The testing was conducted by a technician and the data is within the specified limits.
<table>
<thead>
<tr>
<th>Test No.</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>DO-1</td>
<td>OK</td>
</tr>
<tr>
<td>DO-2</td>
<td>OK</td>
</tr>
<tr>
<td>DO-3</td>
<td>OK</td>
</tr>
<tr>
<td>DO-4</td>
<td>OK</td>
</tr>
<tr>
<td>DO-5</td>
<td>OK</td>
</tr>
<tr>
<td>DO-6</td>
<td>OK</td>
</tr>
<tr>
<td>DO-7</td>
<td>OK</td>
</tr>
<tr>
<td>DO-8</td>
<td>OK</td>
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<tr>
<td>DO-9</td>
<td>OK</td>
</tr>
<tr>
<td>DO-10</td>
<td>OK</td>
</tr>
<tr>
<td>DO-11</td>
<td>OK</td>
</tr>
<tr>
<td>DO-12</td>
<td>OK</td>
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<tr>
<td>DO-13</td>
<td>OK</td>
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<td>DO-14</td>
<td>OK</td>
</tr>
<tr>
<td>DO-15</td>
<td>OK</td>
</tr>
<tr>
<td>DO-16</td>
<td>OK</td>
</tr>
</tbody>
</table>

Date of Test: 5/15/75
7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?
No √
Yes ___ Address ___ Bits ___ 0 errors

7.9.4 Did an error occur?
No √
Yes ___ Address ___ Bits ___ 0 errors

7.9.10 Did an error occur?
No √
Yes ___ Address ___ Bits ___ 0 errors

7.9.16 Did an error occur?
No √
Yes ___ Address ___ Bits ___ 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?
No √
Yes ___ Address ___ Bits ___ 0 errors

7.10.7 Did an error occur?
a) No √
Yes ___ Address ___ Bits ___ 0 errors
b) No 
Yes Address ___ Bits ___ 0 errors

c) No 
Yes Address ___ Bits ___ 0 errors

7.11 NON-VOLATILITY TEST

7.11.7 Did an error occur?
No 

7.11.9 Yes Address ___ Bits ___ 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address ___ (Octal) 0000

7.12.4 Address 0001 ___ (Octal) 0000
  0010 ___ (Octal) 0000
  0011 ___ (Octal) 0000
  0100 ___ (Octal) 0000
  0101 ___ (Octal) 0000
  0110 ___ (Octal) 0000
  0111 ___ (Octal) 0000
  1000 ___ (Octal) 0000
  1001 ___ (Octal) 0000
  1010 ___ (Octal) 0000
S/N 105

Date of Test 5/15/75
Tested By

Address 1011 (Octal) 0000
1100 (Octal) 0000
1101 (Octal) 0000
1110 (Octal) 0000

7.12.6 Did an error occur?
No ✓
Yes Address Bits 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?
No ✓
Yes Address Bits 0 errors

7.13.3 Did an error occur?
No ✓
Yes Address Bits 0 errors
S/N 105

Date of Test 5/15/75
Tested By

7.13.4

a) Did an error occur?
No ✓
Yes Address Bit 0 errors

b) Did an error occur?
No ✓
Yes Address Bit 0 errors
S/N 105

DATE OF TEST 5/24/75
TESTED BY

8. TEMPERATURE TEST

8.2.1 TIME 6:30

8.2.2 LOW TEMPERATURE

THERMISTOR RESISTANCE
150 MINUTES 221.2 K OHMS
160 MINUTES 221.5 K OHMS % CHANGE
170 MINUTES K OHMS % CHANGE
180 MINUTES K OHMS % CHANGE
190 MINUTES K OHMS % CHANGE

8.2.3 DID AN ERROR OCCUR?

NO X

YES _______ ADDRESS _______ BITS _______ 0 ERRORS

8.2.4 -6.1 V VOLTAGE 6.405 VOLTS +5 V VOLTAGE 5.255 VOLTS
-6.1 V CURRENT 12.8 ma +5 V CURRENT 10.3 ma
-6.1 V POWER 51.99 mw +5 V POWER 59.13 mw

TOTAL MEMORY IDLE POWER 136.12 mw 170 mw MAX

8.2.5 -6.1 V VOLTAGE 6.401 VOLTS +5 V VOLTAGE 5.250 VOLTS
-6.1 V CURRENT 24 ma 240 +5 V CURRENT 660 ma 670
-6.1 V POWER 1537 mw +5 V POWER 3518 mw

TOTAL MEMORY OPERATING POWER 5055 mw 7000 mw MAX

MOTOROLA INC.
Government Electronics Division

SIZE CODE IDENT NO. DWG NO.
A 94990 12-P13721D

SCALE REVISION SHEET 16
8.2.6 DID AN ERROR OCCUR?

NO

YES ADDRESS BIT 0 ERRORS

8.2.8

WC a) DID AN ERROR OCCUR?

NO

YES ADDRESS BIT 0 ERRORS

WC b) DID AN ERROR OCCUR?

NO

YES ADDRESS BIT 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO

YES ADDRESS BIT 0 ERRORS

WC d) DID AN ERROR OCCUR?

NO

YES ADDRESS BIT 0 ERRORS

8.2.11

WC a) DID AN ERROR OCCUR?

NO

YES ADDRESS BIT 0 ERRORS
### 8.2.11 (Cont.)

**WC b) DID AN ERROR OCCUR?**

<table>
<thead>
<tr>
<th>Address</th>
<th>Bit</th>
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</thead>
<tbody>
<tr>
<td>NO</td>
<td>X</td>
</tr>
</tbody>
</table>

**WC c) DID AN ERROR OCCUR?**

<table>
<thead>
<tr>
<th>Address</th>
<th>Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>NO</td>
<td>X</td>
</tr>
</tbody>
</table>

**WC d) DID AN ERROR OCCUR?**

<table>
<thead>
<tr>
<th>Address</th>
<th>Bit</th>
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</thead>
<tbody>
<tr>
<td>YES</td>
<td></td>
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</table>

#### 8.3 INTERMEDIATE TEMPERATURE TEST

**TIME 10:45**

#### 8.3.2 TIME THERMISTOR READING. DID ANY ERROR OCCUR?

<table>
<thead>
<tr>
<th>Time</th>
<th>Thermistor Reading</th>
<th>Did Any Error Occur?</th>
</tr>
</thead>
<tbody>
<tr>
<td>10:55</td>
<td>125 K OHMS</td>
<td>NO</td>
</tr>
<tr>
<td>10:55</td>
<td>K OHMS</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td></td>
<td>YES</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 ERRORS</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
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*MOTOROLA INC.*

Government Electronics Division

8701 EAST McDOWELL ROAD
SCOTTSDALE, ARIZONA 85257

SIZE | CODE IDENT NO. | DWG NO. |
-----|----------------|---------|
A    | 94990          | 12-P13721D |

SCALE | REVISION | SHEET |
-----|----------|------|
8/N 105

DATE OF TEST 5/25/75

TESTED BY

8.3.3 TIME 11:3D

8.4

50 MINUTES _______ K OHMS
60 MINUTES 1.506 K OHMS % CHANGE
70 MINUTES 1.472 K OHMS % CHANGE
80 MINUTES 1.443 K OHMS % CHANGE
90 MINUTES _______ K OHMS % CHANGE

8.4.1

-6.1 V VOLTAGE -6.402 VOLTS +5 V VOLTAGE 5.250 VOLTS
-6.1 V CURRENT 6.4 ma +5 V CURRENT 11.8 ma
-6.1 V POWER 40.9724 mw +5 V POWER 61.75 mw

TOTAL MEMORY IDLE POWER 102.9228 mw 170 mw MAX

8.4.2

DID AN ERROR OCCUR?

NO X

YES ADDRESS ________ BIT ________ O ERRORS

8.4.3

-6.1 V VOLTAGE 6.406 VOLTS +5 V VOLTAGE 5.25 VOLTS
-6.1 V CURRENT 255 ma +5 V VOLTAGE 760 ma
-6.1 V POWER 1633.53 mw +5 V POWER 3990.6 mw

TOTAL MEMORY OPERATING POWER 5323.53 mw 7000 mw MAX

8.4.4 WC a) DID AN ERROR OCCUR?

NO X

YES ADDRESS ________ BIT ________ O ERRORS
8.4.4 (Cont.)

WC b) DID AN ERROR OCCUR?

NO

YES ______ ADDRESS _______ BIT _______ 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO

YES ______ ADDRESS _______ BIT _______ 0 ERRORS

WC d) DID AN ERROR OCCUR?

NO

YES ______ ADDRESS _______ BIT _______ 0 ERRORS

8.4.6

WC a) DID AN ERROR OCCUR?

NO

YES ______ ADDRESS _______ BIT _______ 0 ERRORS

WC b) DID AN ERROR OCCUR?

NO

YES ______ ADDRESS _______ BIT _______ 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO

YES ______ ADDRESS _______ BIT _______ 0 ERRORS

WC d) DID AN ERROR OCCUR?

NO

YES ______ ADDRESS _______ BIT _______ 0 ERRORS

8.4.7

DID AN ERROR OCCUR?

NO

YES ______ ADDRESS _______ BIT _______ 0 ERRORS
S/N 195

Date of Test 5/19/75
Tested by

9. VACUUM TEST

Did Any Bit Errors Occur?
No

Yes Address Bits 0 Errors

9.2 Fast Decompression

Date 5/19/75
Tested by

Did Any Bit Errors Occur?
No

Yes Address Bits 0 Errors

9.2.1

9.2.2 Hard Vacuum

Date 5/19/75
Tested by

Did Any Bit Errors Occur?
No

Yes Address Bits 0 Errors

10. VIBRATION TEST

Date 5/21/75
Tested by

SINE SWEEP

Axis X - Did Any Bit Errors Occur?
No

Yes ___________ Freq ______ Address ________ Bits ___________ 0 Errors
Axis Y - Did Any Bit Error Occur?

No

Yes ___ Freq _____ Address _____ Bits _____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No

Yes ___ Freq _____ Address _____ Bits _____ 0 Errors

RANDOM VIBRATION

Axis X - Did Any Bit Errors Occur?

No

Yes ___ Freq _____ Address _____ Bits _____ 0 Errors

Axis Y - Did Any Bit Errors Occur?

No

Yes ___ Freq _____ Address _____ Bits _____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No

Yes ___ Freq _____ Address _____ Bits _____ 0 Errors

11. SHOCK TEST

Date 5/21/75  Tested By

6 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No

Yes ___ Address _____ Bits _____ 0 Errors
Z Direction - Did Any Bit Errors Occur?

No

Yes Address _______ Bits _______ 0 Errors

X Direction - Did Any Bit Errors Occur?

No

Yes Address _______ Bits _______ 0 Errors

12 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No

Yes Address _______ Bits _______ 0 Errors

Z Direction - Did Any Bit Errors Occur?

No

Yes Address _______ Bits _______ 0 Errors

X Direction - Did Any Bit Errors Occur?

No

Yes Address _______ Bits _______ 0 Errors
7.4 CHASSIS ISOLATION
Impedance \( \geq 9 \text{megohms} \)

7.5 INPUT SIGNAL LOADING

7.5.2 Current from INITIATE PULSE to Gnd \( \frac{1.104}{\text{ma}} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to INITIATE PULSE \( \frac{90}{\mu\text{a}} \) \( \leq 20 \mu\text{a} \)

7.5.3 Current from MEM SEL 1 to Gnd \( \frac{1.102}{\text{ma}} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to MEM SEL 1 \( \frac{61}{\mu\text{a}} \) \( \leq 20 \mu\text{a} \)

7.5.4 Current from MEM SEL 2 to Gnd \( \frac{1.105}{\text{ma}} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to MEM SEL 2 \( \frac{83}{\mu\text{a}} \) \( \leq 20 \mu\text{a} \)
Current from MEM SEL 3 to Gnd \( \frac{1.105}{\text{ma}} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to MEM SEL 3 \( \frac{83}{\mu\text{a}} \) \( \leq 20 \mu\text{a} \)

7.5.5 Current from MEM SEL 4 to Gnd \( \frac{1.102}{\text{ma}} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to MEM SEL 4 \( \frac{61}{\mu\text{a}} \) \( \leq 20 \mu\text{a} \)

7.5.6 Current from READ/WRITE to Gnd \( \frac{905}{\text{ma}} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to READ/WRITE \( \frac{159}{\mu\text{a}} \) \( \leq 20 \mu\text{a} \)

Current from ADDRESS 2\(^{0}\) to Gnd \( \frac{931}{\text{ma}} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to ADDRESS 2\(^{0}\) \( \frac{5.85}{\mu\text{a}} \) \( \leq 20 \mu\text{a} \)
Current from ADDRESS 2\(^1\) to Gnd \(0.932\) \(\text{ma}\) ≤ 2 \(\text{ma}\)
Current from 2.4V to ADDRESS 2\(^1\) \(5.42\ \mu\text{a}\) ≤ 20 \(\mu\text{a}\)
Current from ADDRESS 2\(^2\) to Gnd \(1.009\) \(\text{ma}\) ≤ 2 \(\text{ma}\)
Current from 2.4V to ADDRESS 2\(^2\) \(6.44\ \mu\text{a}\) ≤ 20 \(\mu\text{a}\)
Current from ADDRESS 2\(^3\) to Gnd \(0.932\) \(\text{ma}\) ≤ 2 \(\text{ma}\)
Current from 2.4V to ADDRESS 2\(^3\) \(6.92\ \mu\text{a}\) ≤ 20 \(\mu\text{a}\)
Current from ADDRESS 2\(^4\) to Gnd \(0.966\) \(\text{ma}\) ≤ 2 \(\text{ma}\)
Current from 2.4V to ADDRESS 2\(^4\) \(7.61\ \mu\text{a}\) ≤ 20 \(\mu\text{a}\)
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<th>Address Range</th>
<th>Current (mA)</th>
<th>Limit</th>
</tr>
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<td>ADDRESS 2^5 to Gnd</td>
<td>0.935</td>
<td>≤ 2 ma</td>
</tr>
<tr>
<td>2.4V to ADDRESS 2^5</td>
<td>6.12</td>
<td>≤ 20μA</td>
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<td>≤ 20μA</td>
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<td>1.030</td>
<td>≤ 2 ma</td>
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<td>≤ 20μA</td>
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<tr>
<td>ADDRESS 2^9 to Gnd</td>
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<tr>
<td>ADDRESS 2^11 to Gnd</td>
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<td>≤ 20μA</td>
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<td>6.07 μA</td>
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<td>0.983 mA</td>
<td>≤ 2 mA</td>
</tr>
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<td>Current from 2.4V to DATA IN BIT 12</td>
<td>5.65 μA</td>
<td>≤ 20 μA</td>
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<td>Current from DATA IN BIT 13 to Gnd</td>
<td>0.984 mA</td>
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<td>Current from 2.4V to DATA IN BIT 13</td>
<td>5.69 μA</td>
<td>≤ 20 μA</td>
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<td>Current from DATA IN BIT 14 to Gnd</td>
<td>0.989 mA</td>
<td>≤ 2 mA</td>
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<td>Current from 2.4V to DATA IN BIT 14</td>
<td>5.41 μA</td>
<td>≤ 20 μA</td>
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<td>Current from DATA IN BIT 15 to Gnd</td>
<td>0.977 mA</td>
<td>≤ 2 mA</td>
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<td>Current from 2.4V to DATA IN BIT 15</td>
<td>4.22 μA</td>
<td>≤ 20 μA</td>
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<tr>
<td>Current from DATA IN BIT 16 to Gnd</td>
<td>0.868 mA</td>
<td>≤ 2 mA</td>
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<td>Current from 2.4V to DATA IN BIT 16</td>
<td>1.70 μA</td>
<td>≤ 20 μA</td>
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<td>Current from DATA IN BIT 17 to Gnd</td>
<td>0.873 mA</td>
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<tr>
<td>Current from 2.4V to DATA IN BIT 17</td>
<td>4.50 μA</td>
<td>≤ 20 μA</td>
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</table>
7.6 VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS

7.6.3 READ COMPLETE voltage

- READ COMPLETE voltage 50 mv ≤ 100 mv

7.6.4 DATA OUT BIT 0 voltage

- DATA OUT BIT 0 voltage 20 mv ≤ 100 mv
- DATA OUT BIT 1 voltage 0 mv ≤ 100 mv
- DATA OUT BIT 2 voltage 0 mv ≤ 100 mv
- DATA OUT BIT 3 voltage 0 mv ≤ 100 mv
- DATA OUT BIT 4 voltage 10 mv ≤ 100 mv
- DATA OUT BIT 5 voltage 10 mv ≤ 100 mv
- DATA OUT BIT 6 voltage 5 mv ≤ 100 mv
- DATA OUT BIT 7 voltage 0 mv ≤ 100 mv
- DATA OUT BIT 8 voltage 0 mv ≤ 100 mv
- DATA OUT BIT 9 voltage 15 mv ≤ 100 mv
- DATA OUT BIT 10 voltage 10 mv ≤ 100 mv
- DATA OUT BIT 11 voltage 15 mv ≤ 100 mv
- DATA OUT BIT 12 voltage 15 mv ≤ 100 mv
- DATA OUT BIT 13 voltage 15 mv ≤ 100 mv
- DATA OUT BIT 14 voltage 15 mv ≤ 100 mv
- DATA OUT BIT 15 voltage 10 mv ≤ 100 mv
- DATA OUT BIT 16 voltage 5 mv ≤ 100 mv
- DATA OUT BIT 17 voltage 10 mv ≤ 100 mv
7.7 POWER CONSUMPTION (25°C)

7.7.1 Memory +5V Voltage 5.000 Volts
Memory -6.1V voltage 6.102 Volts
+5V Current 10.1 ma
+5V Power 50.5 mw

7.7.2 Memory -6.1V Current 6.102 ma
Memory -6.1V Power 19.5264 mw

7.7.3 Total Memory Idle Power 70.02 mw

7.7.5 Memory +5V Voltage 5.001 Volts
Memory -6.1V Voltage 6.107 Volts
+5V Current 6.70 ma
+5V Power 3350.47 mw

7.7.6 Memory -6.1V Current 2.15 ma
Memory -6.1V Power 1313.005 mw

7.7.7 Total Active Power 663.675 mw

7.8 READ COMPLETE TIMING

7.8.5 Delay 405 ns
Duration 330 ns

Date of Test 5-27-75
Tested By

8/N _`^. Date of Test
Tested By -'

Limits

7.7.1 Memory +5V Voltage 5.000 Volts
Memory -6.1V voltage 6.102 Volts
+5V Current 10.1 ma
+5V Power 50.5 mw

7.7.2 Memory -6.1V Current 6.102 ma
Memory -6.1V Power 19.5264 mw

7.7.3 Total Memory Idle Power 70.02 mw

7.7.5 Memory +5V Voltage 5.001 Volts
Memory -6.1V Voltage 6.107 Volts
+5V Current 6.70 ma
+5V Power 3350.47 mw

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Tested By

Limits

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+5V Current 10.1 ma
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7.7.5 Memory +5V Voltage 5.001 Volts
Memory -6.1V Voltage 6.107 Volts
+5V Current 6.70 ma
+5V Power 3350.47 mw

7.7.6 Memory -6.1V Current 2.15 ma
Memory -6.1V Power 1313.005 mw

7.7.7 Total Active Power 663.675 mw

7.8 READ COMPLETE TIMING

7.8.5 Delay 405 ns
Duration 330 ns

Date of Test 5-27-75
Tested By

Limits
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**Limits**

Refer to test proc.
7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?
No X
Yes Address Bits 0 errors

7.9.4 Did an error occur?
No X
Yes Address Bits 0 errors

7.9.10 Did an error occur?
No X
Yes Address Bits 0 errors

7.9.16 Did an error occur?
No X
Yes Address Bits 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?
No
Yes Address Bits 0 errors

7.10.7 Did an error occur?
a) No X
Yes Address Bits 0 errors
b) No [X]

Yes

Address

Bits

0 errors

c) No [X]

Yes

Address

Bits

0 errors

7.11 NON-VOLATILITY TEST

7.11.7 Did an error occur?

No [X]

Yes

Address

Bits

0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal) 0000

7.12.4 Address 0001 0000 (Octal) 0000

0010 0000 (Octal) 0000

0011 0000 (Octal) 0000

0100 0000 (Octal) 0000

0101 0000 (Octal) 0000

0110 0000 (Octal) 0000

0111 0000 (Octal) 0000

1000 0000 (Octal) 0000

1001 0000 (Octal) 0000

1010 0000 (Octal) 0000
S/N 105

Date of Test 5/27/75
Tested By

Limits

Address 1011 000 (Octal) 0000
1100 0000 (Octal) 0000
1101 0000 (Octal) 0000
1110 0000 (Octal) 0000

7.12.6 Did an error occur?
No X
Yes Address Bits 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?
No X
Yes Address Bits 0 errors

7.13.3 Did an error occur?
No X
Yes Address Bits 0 errors
7.13.4 a) Did an error occur?

No [X]  Yes Address ____ Bit ____  0 errors

b) Did an error occur?

No [X]  Yes Address ____ Bit ____  0 errors
SHOCK TEST (DROP)

PROJECT 4601-400
DATE 5-16-75
SHEET 1 OF 1
NO. 30412
CONTROL NO. 11
LOT PLASTIC WIRE MEMORY
SERIAL NO. 105
OPERATOR Joe T
OBSERVER Joe T
VIBRATION MOUNTS
D. OF DROPS PER PAGE 6, TOTAL NO. OF DROPS 6
ACCELERATION 30 G's
PULSE DURATION 1.4 12 MS
SPEC DETAILS 13-51372 20

FEMALE HEIGHT 1 7 / 8 IN.
PROGRAMMER PRESSURE 1/4 A P.S.I.
TYPE OF WAVESHAPE SINE
BANDPASS FILTER 2 LOW FR. Hz
\[ \frac{9}{300} \text{ HIGH FR. Hz} \]
REMARKS 3 drops + 6 ms of 3 drops + 12 ms
Pad for 12 ms one 1-8x8x\( \frac{1}{4} \) plastic
2-8x8x\( \frac{1}{4} \) metal
3-8x8x\( \frac{1}{4} \) metal
3-1" blue cloth
1-1" blue open

PAD AND PLATE CONFIGURATION

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<th>PART NO.</th>
<th>DESCRIPTION</th>
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<tr>
<td>2</td>
<td>MOL 2776</td>
<td>1&quot; red open (B)</td>
</tr>
<tr>
<td>3</td>
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START PUMPING

NEAR TO ATM
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<td>0.33</td>
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PROJECT 4601-400 UNIT P-W Memory SER. NO 105

X & Z AXIS  SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1-5 HZ SCAN RATE 1.125 HZ AVG. TIME 1.10 SECONDS
210 HZ SCAN RATE 2.50 HZ AVG. TIME 2.10 SECONDS
320 HZ SCAN RATE 3.50 HZ AVG. TIME 3.10 SECONDS
490 HZ SCAN RATE 4.25 HZ AVG. TIME 4.10 SECONDS

VIBRATION DATE 21 May 75
DATE ANALYZED 21 May 75
PETE MARTIN
VIBRATION TOLERANCE LINE as shown +3 dB

REMARKS Input accelerometer

Frequency (Hz)
PROJECT 4601-400 UNIT P-W Memory SER. NO. 105

Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W.
1.5 HZ SCAN RATE 1.25 HZ AVG. TIME 1.10 SECONDS
2.10 HZ SCAN RATE 2.25 HZ AVG. TIME 2.10 SECONDS
3.20 HZ SCAN RATE 5.25 HZ AVG. TIME 3.10 SECONDS
4.50 HZ SCAN RATE 25 HZ AVG. TIME 4.10 SECONDS

FREQUENCY 1.15-20 HZ MOTOR KNOB TAKE-OFF NO.
2.20-40 HZ CUSTOM KNOB TAKE-OFF NO.
3.40-100 HZ
4.100-2K HZ

VIBRATION RATE 21 May 75
DATE ANALYZED 21 May 75 BY Pete Martin
VIBRATION TESTER N/A

REMARKS Response accelerometer on top of housing

ORIGINAL PAGE OF POOR QUALITY
PROJECT 4601-400 UNIT P-W Memory SER. NO. 105

Y AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1. 5 Hz SCAN RATE 1.125 Hz AVG. TIME 1.10 SECONDS
2. 10 Hz SCAN RATE 2.25 Hz AVG. TIME 2.10 SECONDS
3. 20 Hz SCAN RATE 3.5 Hz AVG. TIME 3.10 SECONDS
4. 50 Hz SCAN RATE 11.25 Hz AVG. TIME 4.10 SECONDS

FREQUENCY SCALE 15-20 Hz NOT DETERMINED
20-40 Hz CUSTOM SCALE
40-100 Hz
100-2K Hz

VIBRATION DATE 21-May-75
DATE ANALYZED 21-May-75
VIBRATION LEVEL as shown -13 dB

REMARKS Input accelerometer
ATTACHMENT V

ACCEPTANCE TEST DATA SHEET
LOW POWER RANDOM ACCESS
SPACECRAFT MEMORY
PART NO. 01-P13701D
DRAWING NO. 12-P13721D
SERIAL NUMBER 106

(35 PAGES)
<table>
<thead>
<tr>
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<tr>
<td>LTR</td>
<td>DESCRIPTION</td>
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<tr>
<td>X1</td>
<td>Initial Release</td>
</tr>
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<td>X2</td>
<td>Incorporated changes prior to First Usage</td>
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<tr>
<td>X3</td>
<td>Change -6.9V to -6.1V</td>
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<tr>
<td>X4</td>
<td>Change 6000mw to 7000mw, pages 10, 17, 19, 30. Change weight from 3.0 to 6.5 pounds, page 2.</td>
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<tr>
<td>X5</td>
<td>Add weight 5.8 pounds for magnesium chassis MCO S7835. Revised per MCO S7845</td>
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**SN106**

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**FOR ASSOCIATED LISTS SEE**

**INTERPRET DRAWING IN ACCORDANCE WITH STANDARDS PRESCRIBED BY**

**MOTOROLA INC.**

8201 EAST MCDOWELL ROAD
SCOTTSDALE, ARIZONA 85252

**ACCEPTANCE TEST DATA SHEET,**
LOW POWER RANDOM ACCESS SPACE-RAFT MEMORY, PART NO. 01-P13701D

**SCALE**

**SUMMARY OF REVISIONS**

- Rev X1: Initial Release
- Rev X2: Incorporated changes prior to First Usage
- Rev X3: Change -6.9V to -6.1V
- Rev X4: Change 6000mw to 7000mw, pages 10, 17, 19, 30. Change weight from 3.0 to 6.5 pounds, page 2.
- Rev X5: Add weight 5.8 pounds for magnesium chassis MCO S7835. Revised per MCO S7845.
1. **SCOPE**

   This test data sheet is to be used to record data as required by the Acceptance Test Procedure for the Low Power Random Access Spacecraft Memory.

2. **REFERENCE INFORMATION**

2.1 **SPECIFICATIONS APPLICABLE**

   - S-562-P-24 Low Power Random Access Spacecraft Memory
   - 12-P13722D Acceptance Test Procedure, Low Power Random Access Spacecraft Memory

3. **TEST DATA**

   Unit S/N 1060 Start Date of Tests 6-17-75
   Tested by [Signature]

4. **PHYSICAL CHARACTERISTICS**

   6.1 **WEIGHT**

   Weight of LP-RASM - 5.58 Pounds
   6.5 pounds (aluminum)
   5.8 pounds (magnesium)
S/N 1016

Date of Test 6-17-75
Tested By

6.2 DIMENSIONS

- H = 29.03 inches
- W = 8.633 inches
- MW = 8.944 inches
- D = 6.320 inches
- ND = 6.971 inches

V = H X W X D = 158.4 inches³ ≤ 160 inches³
7.4 CHASSIS ISOLATION

Impedance $\geq 10 \, \text{M} $

Limit $\geq 9 \, \text{megohms}$

7.5 INPUT SIGNAL LOADING

7.5.2 Current from INITIATE PULSE to Gnd $1.15 \, \text{ma}$ $\leq 2 \, \text{ma}$

Current from 2.4V to INITIATE PULSE $95 \, \text{µa}$ $\leq 20 \, \text{µa}$

7.5.3 Current from MEM SEL 1 to Gnd $1.15 \, \text{ma}$ $\leq 2 \, \text{ma}$

Current from 2.4V to MEM SEL 1 $70 \, \text{µa}$ $\leq 20 \, \text{µa}$

7.5.4 Current from MEM SEL 2 to Gnd $1.16 \, \text{ma}$ $\leq 2 \, \text{ma}$

Current from 2.4V to MEM SEL 2 $96 \, \text{µa}$ $\leq 20 \, \text{µa}$

Current from MEM SEL 3 to Gnd $1.16 \, \text{ma}$ $\leq 2 \, \text{ma}$

Current from 2.4V to MEM SEL 3 $98 \, \text{µa}$ $\leq 20 \, \text{µa}$

Current from MEM SEL 4 to Gnd $1.15 \, \text{ma}$ $\leq 2 \, \text{ma}$

Current from 2.4V to MEM SEL 4 $70 \, \text{µa}$ $\leq 20 \, \text{µa}$

7.5.5 Current from READ/WRITE to Gnd $96 \, \text{µa}$ $\leq 2 \, \text{ma}$

Current from 2.4V to READ/WRITE $202 \, \text{µa}$ $\leq 20 \, \text{µa}$

7.5.6 Current from ADDRESS 0 to Gnd $94 \, \text{µa}$ $\leq 2 \, \text{ma}$

Current from 2.4V to ADDRESS 0 $7.04 \, \text{µa}$ $\leq 20 \, \text{µa}$
S/N 106  
Date of Test 06-17-75  
Tested By [Signature]  

Current from ADDRESS 2¹ to Gnd  \( \frac{0.94}{A} \) ma  
Current from 2.4V to ADDRESS 2¹  \( \frac{6.52}{A} \) \( \mu A \)  
Current from ADDRESS 2² to Gnd  \( \frac{1.03}{A} \) ma  
Current from 2.4V to ADDRESS 2²  \( \frac{7.62}{A} \) \( \mu A \)  
Current from ADDRESS 2³ to Gnd  \( \frac{0.96}{A} \) ma  
Current from 2.4V to ADDRESS 2³  \( \frac{9.04}{A} \) \( \mu A \)  
Current from ADDRESS 2⁴ to Gnd  \( \frac{0.99}{A} \) ma  
Current from 2.4V to ADDRESS 2⁴  \( \frac{9.36}{A} \) \( \mu A \)  

Limits  
\( \leq 2 \text{ ma} \)  
\( \leq 20 \mu A \)  
\( \leq 2 \text{ ma} \)  
\( \leq 20 \mu A \)  
\( \leq 2 \text{ ma} \)  
\( \leq 20 \mu A \)  
\( \leq 2 \text{ ma} \)  
\( \leq 20 \mu A \)  

MOTOROLA INC.  
Government Electronics Division  
8301 E. McDOWELL ROAD  
SCOTTSDALE, ARIZONA 85252  

SIZE | CODE IDENT NO. | DWG NO.  
---|---|---  
A | 94990 | 12-P13721D  

SCALE | REVISION | SHEET  
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<td>DATA IN BIT 0</td>
<td>$5.09\ \text{µA}$</td>
<td>$\leq 20\ \text{µA}$</td>
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</table>
Current from DATA IN BIT 1 to Gnd  \( 0.96 \) ma \( \leq 2 \) ma
Current from 2.4V to DATA IN BIT 1  \( 5.06 \) \( \mu \)a \( \leq 20 \) \( \mu \)a
Current from DATA IN BIT 2 to Gnd  \( 0.99 \) ma \( \leq 2 \) ma
Current from 2.4V to DATA IN BIT 2  \( 4.65 \) \( \mu \)a \( \leq 20 \) \( \mu \)a
Current from DATA IN BIT 3 to Gnd  \( 0.94 \) ma \( \leq 2 \) ma
Current from 2.4V to DATA IN BIT 3  \( 4.84 \) \( \mu \)a \( \leq 20 \) \( \mu \)a
Current from DATA IN BIT 4 to Gnd  \( 0.94 \) ma \( \leq 2 \) ma
Current from 2.4V to DATA IN BIT 4  \( 4.65 \) \( \mu \)a \( \leq 20 \) \( \mu \)a
Current from DATA IN BIT 5 to Gnd  \( 0.95 \) ma \( \leq 2 \) ma
Current from 2.4V to DATA IN BIT 5  \( 4.60 \) \( \mu \)a \( \leq 20 \) \( \mu \)a
Current from DATA IN BIT 6 to Gnd  \( 0.92 \) ma \( \leq 2 \) ma
Current from 2.4V to DATA IN BIT 6  \( 5.97 \) \( \mu \)a \( \leq 20 \) \( \mu \)a
Current from DATA IN BIT 7 to Gnd  \( 0.89 \) ma \( \leq 2 \) ma
Current from 2.4V to DATA IN BIT 7  \( 5.80 \) \( \mu \)a \( \leq 20 \) \( \mu \)a
Current from DATA IN BIT 8 to Gnd  \( 0.91 \) ma \( \leq 2 \) ma
Current from 2.4V to DATA IN BIT 8  \( 6.26 \) \( \mu \)a \( \leq 20 \) \( \mu \)a
Current from DATA IN BIT 9 to Gnd  \( 0.99 \) ma \( \leq 2 \) ma
Current from 2.4V to DATA IN BIT 9  \( 7.39 \) \( \mu \)a \( \leq 20 \) \( \mu \)a
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<tr>
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<td>6.52 µA</td>
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<td>Current from DATA IN BIT 11 to Gnd</td>
<td>1.07 mA</td>
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<td>Current from 2.4V to DATA IN BIT 11</td>
<td>6.51 µA</td>
<td>≤ 20 µA</td>
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<td>Current from 2.4V to DATA IN BIT 12</td>
<td>6.02 µA</td>
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<tr>
<td>Current from DATA IN BIT 13 to Gnd</td>
<td>0.95 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 13</td>
<td>6.11 µA</td>
<td>≤ 20 µA</td>
</tr>
<tr>
<td>Current from DATA IN BIT 14 to Gnd</td>
<td>0.96 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 14</td>
<td>6.03 µA</td>
<td>≤ 20 µA</td>
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<td>Current from DATA IN BIT 15 to Gnd</td>
<td>0.98 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 15</td>
<td>6.54 µA</td>
<td>≤ 20 µA</td>
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<td>Current from DATA IN BIT 16 to Gnd</td>
<td>0.96 mA</td>
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<td>0.96 mA</td>
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<tr>
<td>Current from 2.4V to DATA IN BIT 17</td>
<td>6.95 µA</td>
<td>≤ 20 µA</td>
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</table>
7.6 VERIFICATION OF OPEN COLLECTOR ON OUTPUT SIGNALS

### 7.6.3 READ COMPLETE voltage

- **voltage : 10 mv**
- **Limit : ≤ 100 mv**

### 7.6.4 DATA OUT BIT 0 voltage

- **voltage : 30 mv**
- **Limit : ≤ 100 mv**

- **voltage : 20 mv**
- **Limit : ≤ 100 mv**

- **voltage : 20 mv**
- **Limit : ≤ 100 mv**

- **voltage : 10 mv**
- **Limit : ≤ 100 mv**

- **voltage : 30 mv**
- **Limit : ≤ 100 mv**

- **voltage : 25 mv**
- **Limit : ≤ 100 mv**

- **voltage : 30 mv**
- **Limit : ≤ 100 mv**

- **voltage : 10 mv**
- **Limit : ≤ 100 mv**

- **voltage : 20 mv**
- **Limit : ≤ 100 mv**

- **voltage : 30 mv**
- **Limit : ≤ 100 mv**

- **voltage : 30 mv**
- **Limit : ≤ 100 mv**

- **voltage : 40 mv**
- **Limit : ≤ 100 mv**

- **voltage : 40 mv**
- **Limit : ≤ 100 mv**

- **voltage : 30 mv**
- **Limit : ≤ 100 mv**

- **voltage : 40 mv**
- **Limit : ≤ 100 mv**
### 7.7 Power Consumption (25°C)

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory +5V Voltage</td>
<td>5.003 Volts</td>
</tr>
<tr>
<td>Memory -5V Voltage</td>
<td>6.100 Volts</td>
</tr>
<tr>
<td>+5V Current</td>
<td>10.0 ma</td>
</tr>
<tr>
<td>+5V Power</td>
<td>50.03 mw</td>
</tr>
<tr>
<td>Memory -6.1V Current</td>
<td>3.2 ma</td>
</tr>
<tr>
<td>Memory -6.1V Power</td>
<td>19.52 mw</td>
</tr>
<tr>
<td>Total Memory Idle Power</td>
<td>69.55 mw</td>
</tr>
<tr>
<td>Memory +5V Voltage</td>
<td>5.000 Volts</td>
</tr>
<tr>
<td>Memory -5V Voltage</td>
<td>6.101 Volts</td>
</tr>
<tr>
<td>+5V Current</td>
<td>6.70 ma</td>
</tr>
<tr>
<td>+5V Power</td>
<td>3350 mw</td>
</tr>
<tr>
<td>Memory -6.1V Current</td>
<td>2.86 ma</td>
</tr>
<tr>
<td>Memory -6.1V Power</td>
<td>14.91 mw</td>
</tr>
<tr>
<td>Total Active Power</td>
<td>4841 mw</td>
</tr>
<tr>
<td>READ COMPLETE TIMING</td>
<td></td>
</tr>
<tr>
<td>Delay</td>
<td>410 ns</td>
</tr>
<tr>
<td>Duration</td>
<td>310 ns</td>
</tr>
<tr>
<td>7.8.5</td>
<td></td>
</tr>
<tr>
<td>Delay</td>
<td>410 ns</td>
</tr>
<tr>
<td>Duration</td>
<td>310 ns</td>
</tr>
</tbody>
</table>

- 7.7.1 Memory +5V Voltage: 5.003 Volts
- 7.7.1 Memory -5V Voltage: 6.100 Volts
- 7.7.1 +5V Current: 10.0 ma
- 7.7.1 +5V Power: 50.03 mw
- 7.7.1 Memory -6.1V Current: 3.2 ma
- 7.7.1 Memory -6.1V Power: 19.52 mw
- 7.7.3 Total Memory Idle Power: 69.55 mw
- 7.7.5 Memory +5V Voltage: 5.000 Volts
- 7.7.5 Memory -5V Voltage: 6.101 Volts
- 7.7.5 +5V Current: 6.70 ma
- 7.7.5 +5V Power: 3350 mw
- 7.7.6 Memory -6.1V Current: 2.86 ma
- 7.7.6 Memory -6.1V Power: 14.91 mw
- 7.7.7 Total Active Power: 4841 mw
- 7.8 READ COMPLETE TIMING
- 7.8.5 Delay: 410 ns
- 7.8.5 Duration: 310 ns

**Limits**

- 7.7.3 Total Memory Idle Power: 170 mw max.
- 7.7.7 Total Active Power: 7000 mw max.
- 7.8.5 Delay: 500 ns max.
- 7.8.5 Duration: 250 ns min
- 450 ns max.
Date of Test 06-17-75
Tested by

7.8.7 & 7.8.8

READ COMPLETE/DATA OUTPUT TIMING

<table>
<thead>
<tr>
<th>DO</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>DO-0</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-1</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-2</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-3</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-4</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-5</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-6</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-7</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-8</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-9</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-10</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-11</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-12</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-13</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-14</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-15</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-16</td>
<td>OK ✓</td>
</tr>
<tr>
<td>DO-17</td>
<td>OK ✓</td>
</tr>
</tbody>
</table>

LIMITS

REJECT

REFER TO TEST PROC.
S/N 106

Date of Test 06-17-75
Tested By

7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?
No
Yes  Address  Bits  0 errors

7.9.4 Did an error occur?
No
Yes  Address  Bits  0 errors

7.9.10 Did an error occur?
No
Yes  Address  Bits  0 errors

7.9.16 Did an error occur?
No
Yes  Address  Bits  0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?
No
Yes  Address  Bits  0 errors

7.10.7 Did an error occur?
a) No
Yes  Address  Bits  0 errors
S/N 106

Date of Test: 06.17.75
Tested By: ____________________

b) No ✓
   Yes __________ Address _______ Bits _______ 0 errors

c) No ✓
   Yes __________ Address _______ Bits _______ 0 errors

7.11 NON-VOLATILITY TEST

7.11.7 Did an error occur?
   & No ✓
   Yes __________ Address _______ Bits _______ 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal).
   0000

7.12.4 Address 0001 (Octal) 0000
   0100 (Octal) 0000
   0110 (Octal) 0000
   0111 (Octal) 0000
   1000 (Octal) 0000
   1001 (Octal) 0000
   1010 (Octal) 0000
S/N 106

Date of Test 06-17-75
Tested By

Address 1011 0000 (Octal) 0000
1100 0000 (Octal) 0000
1101 0000 (Octal) 0000
1110 0000 (Octal) 0000

7.12.6 Did an error occur?
No
Yes ___ Address ___ Bits ___ 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?
No
Yes ___ Address ___ Bits ___ 0 errors

7.13.3 Did an error occur?
No
Yes ___ Address ___ Bits ___ 0 errors
7.13.4 a) Did an error occur?
   No ✔
   Yes __ Address ___ Bit ___ 0 errors

b) Did an error occur?
   No ✔
   Yes __ Address ___ Bit ___ 0 errors
8. TEMPERATURE TEST

8.2.1 TIME 0705

8.2.2 LOW TEMPERATURE

THERMISTOR RESISTANCE

150 MINUTES 213 K OHMS
160 MINUTES 216 K OHMS % CHANGE 1.34%
170 MINUTES 219 K OHMS % CHANGE
180 MINUTES K OHMS % CHANGE
190 MINUTES K OHMS % CHANGE

8.2.3 DID AN ERROR OCCUR?

NO ✓
YES ADDRESS BITS 0 ERRORS

8.2.4 -6.1 V VOLTAGE 6.40 VOLTS +5 V VOLTAGE 5.24 VOLTS
-6.1 V CURRENT 14.5 ma +5 V CURRENT 10.2 ma
-6.1 V POWER 92.82 mw +5 V POWER 53.57 mw

TOTAL MEMORY IDLE POWER 146.4 mw

8.2.5 -6.1 V VOLTAGE 6.401 VOLTS +5 V VOLTAGE 5.256 VOLTS
-6.1 V CURRENT 255 ma +5 V CURRENT 680 ma
-6.1 V POWER 1632 mw +5 V POWER 35.24 mw

TOTAL MEMORY OPERATING POWER 52.06 mw

7000 mw MAX
8/N 106

DATE OF TEST 06-24-75
TESTED BY

LIMITS

8.2.6 DID AN ERROR OCCUR?

NO ✓

YES __ ADDRESS ___ BIT ___ 0 ERRORS

8.2.8 WC a) DID AN ERROR OCCUR?

NO ✓

YES __ ADDRESS ___ BIT ___ 0 ERRORS

WC b) DID AN ERROR OCCUR?

NO ✓

YES __ ADDRESS ___ BIT ___ 0 ERRORS

WC c) DID AN ERROR OCCUR?

NO ✓

YES __ ADDRESS ___ BIT ___ 0 ERRORS

WC d) DID AN ERROR OCCUR?

NO ✓

YES __ ADDRESS ___ BIT ___ 0 ERRORS

8.2.9 WC a) DID AN ERROR OCCUR?

NO ✓

YES __ ADDRESS ___ BIT ___ 0 ERRORS
8.2.9 (Cont.)

WC b) DID AN ERROR OCCUR?

<table>
<thead>
<tr>
<th>NO</th>
<th>ADDRESS</th>
<th>BIT</th>
<th>0 ERRORS</th>
</tr>
</thead>
<tbody>
<tr>
<td>YES</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

WC c) DID AN ERROR OCCUR?

<table>
<thead>
<tr>
<th>NO</th>
<th>ADDRESS</th>
<th>BIT</th>
<th>0 ERRORS</th>
</tr>
</thead>
<tbody>
<tr>
<td>YES</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

WC d) DID AN ERROR OCCUR?

<table>
<thead>
<tr>
<th>NO</th>
<th>ADDRESS</th>
<th>BIT</th>
<th>0 ERRORS</th>
</tr>
</thead>
<tbody>
<tr>
<td>YES</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

8.3 INTERMEDIATE TEMPERATURE TEST

TIME: 10:37

8.3.2

<table>
<thead>
<tr>
<th>TIME</th>
<th>THERMISTOR READING</th>
<th>DID ANY ERROR OCCUR?</th>
</tr>
</thead>
<tbody>
<tr>
<td>10:47</td>
<td>140 K OHMS</td>
<td>NO &amp; YES</td>
</tr>
<tr>
<td>10:47</td>
<td>145 K OHMS</td>
<td>NO &amp; YES</td>
</tr>
<tr>
<td>10:47</td>
<td>146 K OHMS</td>
<td>NO &amp; YES</td>
</tr>
<tr>
<td>10:47</td>
<td>147 K OHMS</td>
<td>NO &amp; YES</td>
</tr>
<tr>
<td>10:47</td>
<td>148 K OHMS</td>
<td>NO &amp; YES</td>
</tr>
</tbody>
</table>

MOTOROLA INC.
Government Electronics Division

AV-2-B-199H-100A-2/4 DWG FORMAT
8.3.3  
TIME 11:20

8.4  
50 MINUTES 1.601 K OHMS
60 MINUTES 1.510 K OHMS % CHANGE 5.1%
70 MINUTES 1.450 K OHMS % CHANGE 4.0%
80 MINUTES 1.333 K OHMS % CHANGE 3.2%
90 MINUTES K OHMS % CHANGE

8.4.1
-6.1 V VOLTAGE 6.407 VOLTS +5 V VOLTAGE 5.251 VOLTS
-6.1 V CURRENT 8.0 ma +5 V CURRENT 11.5 ma
-6.1 V POWER 52.21 mw +5 V POWER 60.38 mw
TOTAL MEMORY IDLE POWER 112.59 mw 170 mw MAX

8.4.2 DID AN ERROR OCCUR?
NO
YES ADDRESS ___ BIT ___ 0 ERRORS

8.4.3
-6.1 V VOLTAGE 6.407 VOLTS +5 V VOLTAGE 5.250 VOLTS
-6.1 V CURRENT 265 ma +5 V VOLTAGE 260 ma
-6.1 V POWER 1696.5 mw +5 V POWER 3990 mw
TOTAL MEMORY OPERATING POWER 5686.5 mw 7000 mw MAX

8.4.4 WC a) DID AN ERROR OCCUR?
NO
YES ADDRESS ___ BIT ___ 0 ERRORS

MOTOROLA INC.
Government Electronics Division
A 94990 12-P13721D
SIZE CODE IDENT NO. DWG NO.
8.4.4 (Cont.)

WC b) DID AN ERROR OCCUR?

NO

YES

ADDRESS

BIT

0 ERRORS

WC c) DID AN ERROR OCCUR?

NO

YES

ADDRESS

BIT

0 ERRORS

WC d) DID AN ERROR OCCUR?

NO

YES

ADDRESS

BIT

0 ERRORS

8.4.6

WC a) DID AN ERROR OCCUR?

NO

YES

ADDRESS

BIT

0 ERRORS

WC b) DID AN ERROR OCCUR?

NO

YES

ADDRESS

BIT

0 ERRORS

WC c) DID AN ERROR OCCUR?

NO

YES

ADDRESS

BIT

0 ERRORS

WC d) DID AN ERROR OCCUR?

NO

YES

ADDRESS

BIT

0 ERRORS

8.4.7

DID AN ERROR OCCUR?

NO

YES

ADDRESS

BIT

0 ERRORS
S/N 104  

Date of Test 6-16-75
Tested by

9. VACUUM TEST

9.2 Did Any Bit Errors Occur?

No

Yes Address Bits 0 Errors

9.2.1 Fast Decompression

Date 6-16-75 Tested by

Did Any Bit Errors Occur?

No

Yes Address Bits 0 Errors

9.2.2 Hard Vacuum

Date 6-16-75 Tested by

Did Any Bit Errors Occur?

No

Yes Address Bits 0 Errors

10. VIBRATION TEST

Date 5-21-75 Tested by

SINE SWEEP

Axis X - Did Any Bit Errors Occur?

No

Yes Freq Address Bits 0 Errors
S/N 106

Date of Test 6-24-75
Tested by

Axis Y - Did Any Bit Error Occur?

Limits

No

Yes __ Freq _____ Address _____ Bits _____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No

Yes __ Freq _____ Address _____ Bits _____ 0 Errors

RANDOM VIBRATION

Axis X - Did Any Bit Errors Occur?

No

Yes __ Freq _____ Address _____ Bits _____ 0 Errors

Axis Y - Did Any Bit Errors Occur?

No

Yes __ Freq _____ Address _____ Bits _____ 0 Errors

Axis Z - Did Any Bit Errors Occur?

No

Yes __ Freq _____ Address _____ Bits _____ 0 Errors

11. SHOCK TEST

Date 6-18-75  Tested By

6 MILISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?

No

Yes _____ Address _____ Bits _____ 0 Errors
Z Direction - Did Any Bit Errors Occur?
No
Yes __ Address _____ Bits ______ 0 Errors

X Direction - Did Any Bit Errors Occur?
No
Yes __ Address _____ Bits ______ 0 Errors

12 MILLISECOND DURATION SHOCK

Y Direction - Did Any Bit Errors Occur?
No
Yes __ Address _____ Bits ______ 0 Errors

Z Direction - Did Any Bit Errors Occur?
No
Yes __ Address _____ Bits ______ 0 Errors

X Direction - Did Any Bit Errors Occur?
No
Yes __ Address _____ Bits ______ 0 Errors
7.4 CHASSIS ISOLATION

Impedance  

Limit

> 10 meg Ω

≥ 9 megohms

7.5 INPUT SIGNAL LOADING

7.5.2 Current from INITIATE PULSE to Gnd  

Current from 2.4V to INITIATE PULSE  

≤ 2 mA

≤ 20 μA

7.5.3 Current from MEM SEL 1 to Gnd  

Current from 2.4V to MEM SEL 1  

≤ 2 mA

≤ 20 μA

7.5.4 Current from MEM SEL 2 to Gnd  

Current from 2.4V to MEM SEL 2  

≤ 2 mA

≤ 20 μA

7.5.5 Current from READ/WRITE to Gnd  

Current from 2.4V to READ/WRITE  

≤ 2 mA

≤ 20 μA

7.5.6 Current from ADDRESS 2 to Gnd  

Current from 2.4V to ADDRESS 2  

≤ 2 mA

≤ 20 μA
Current from ADDRESS $2^1$ to Gnd $0.94$ ma  
Current from 2.4V to ADDRESS $2^1$ $6.47$ $\mu$A  
Current from ADDRESS $2^2$ to Gnd $1.02$ ma  
Current from 2.4V to ADDRESS $2^2$ $7.59$ $\mu$A  
Current from ADDRESS $2^3$ to Gnd $1.95$ ma  
Current from 2.4V to ADDRESS $2^3$ $8.96$ $\mu$A  
Current from ADDRESS $2^4$ to Gnd $1.98$ ma  
Current from 2.4V to ADDRESS $2^4$ $9.25$ $\mu$A  

**Limits**  
$\leq 2$ ma  
$\leq 20$ $\mu$A
<table>
<thead>
<tr>
<th>Current</th>
<th>Address</th>
<th>Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current from ADDRESS 2(^5) to Gnd</td>
<td>0.84 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2(^5)</td>
<td>4.90 µA</td>
<td>≤ 20 µA</td>
</tr>
<tr>
<td>Current from ADDRESS 2(^6) to Gnd</td>
<td>0.91 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2(^5)</td>
<td>6.07 µA</td>
<td>≤ 20 µA</td>
</tr>
<tr>
<td>Current from ADDRESS 2(^7) to Gnd</td>
<td>1.64 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2(^7)</td>
<td>10.81 µA</td>
<td>≤ 20 µA</td>
</tr>
<tr>
<td>Current from ADDRESS 2(^8) to Gnd</td>
<td>1.88 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2(^8)</td>
<td>4.47 µA</td>
<td>≤ 20 µA</td>
</tr>
<tr>
<td>Current from ADDRESS 2(^9) to Gnd</td>
<td>1.93 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2(^9)</td>
<td>3.41 µA</td>
<td>≤ 20 µA</td>
</tr>
<tr>
<td>Current from ADDRESS 2(^{10}) to Gnd</td>
<td>1.89 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2(^{10})</td>
<td>11.64 µA</td>
<td>≤ 20 µA</td>
</tr>
<tr>
<td>Current from ADDRESS 2(^{11}) to Gnd</td>
<td>1.88 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>Current from 2.4V to ADDRESS 2(^{11})</td>
<td>9.25 µA</td>
<td>≤ 20 µA</td>
</tr>
<tr>
<td>Current from DATA IN BIT 0 to Gnd</td>
<td>0.89 mA</td>
<td>≤ 2 mA</td>
</tr>
<tr>
<td>Current from 2.4V to DATA IN BIT 0</td>
<td>5.05 µA</td>
<td>≤ 20 µA</td>
</tr>
<tr>
<td>Bit</td>
<td>Current from DATA IN BIT to Gnd</td>
<td>Current from 2.4V to DATA IN BIT</td>
</tr>
<tr>
<td>-----</td>
<td>---------------------------------</td>
<td>----------------------------------</td>
</tr>
<tr>
<td>1</td>
<td>0.90 ma</td>
<td>0.084 μA</td>
</tr>
<tr>
<td>2</td>
<td>0.69 ma</td>
<td>0.462 μA</td>
</tr>
<tr>
<td>3</td>
<td>0.94 ma</td>
<td>0.482 μA</td>
</tr>
<tr>
<td>4</td>
<td>0.94 ma</td>
<td>0.463 μA</td>
</tr>
<tr>
<td>5</td>
<td>0.94 ma</td>
<td>0.468 μA</td>
</tr>
<tr>
<td>6</td>
<td>0.92 ma</td>
<td>0.592 μA</td>
</tr>
<tr>
<td>7</td>
<td>0.98 ma</td>
<td>0.576 μA</td>
</tr>
<tr>
<td>8</td>
<td>0.90 ma</td>
<td>0.620 μA</td>
</tr>
<tr>
<td>9</td>
<td>0.99 ma</td>
<td>0.762 μA</td>
</tr>
</tbody>
</table>
Current from DATA IN BIT 10 to Gnd \( \frac{9.7}{\text{ma}} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to DATA IN BIT 10 \( \frac{6.43}{\mu\text{a}} \) \( \leq 20\mu\text{a} \)

Current from DATA IN BIT 11 to Gnd \( \frac{1.01}{\text{ma}} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to DATA IN BIT 11 \( \frac{6.44}{\mu\text{a}} \) \( \leq 20\mu\text{a} \)

Current from DATA IN BIT 12 to Gnd \( \frac{9.5}{\text{ma}} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to DATA IN BIT 12 \( \frac{5.98}{\mu\text{a}} \) \( \leq 20\mu\text{a} \)

Current from DATA IN BIT 13 to Gnd \( \frac{9.5}{\text{ma}} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to DATA IN BIT 14 \( \frac{6.07}{\mu\text{a}} \) \( \leq 20\mu\text{a} \)

Current from DATA IN BIT 14 to Gnd \( \frac{9.5}{\text{ma}} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to DATA IN BIT 14 \( \frac{6.00}{\mu\text{a}} \) \( \leq 20\mu\text{a} \)

Current from DATA IN BIT 15 to Gnd \( \frac{9.5}{\text{ma}} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to DATA IN BIT 15 \( \frac{6.50}{\mu\text{a}} \) \( \leq 20\mu\text{a} \)

Current from DATA IN BIT 16 to Gnd \( \frac{9.5}{\text{ma}} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to DATA IN BIT 17 \( \frac{7.06}{\mu\text{a}} \) \( \leq 20\mu\text{a} \)

Current from DATA IN BIT 17 to Gnd \( \frac{9.5}{\text{ma}} \) \( \leq 2 \text{ ma} \)
Current from 2.4V to DATA IN BIT 17 \( \frac{6.92}{\mu\text{a}} \) \( \leq 20\mu\text{a} \)
## Verification of Open Collector on Output Signals

**7.6.3 Read Complete Voltage**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Voltage (mv)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>15</td>
</tr>
</tbody>
</table>

Limit: 100 mv

**7.6.4 Data Out Bit Voltages**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Voltage (mv)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>10</td>
</tr>
<tr>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
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<td>16</td>
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Limit: 100 mv
7.7 POWER CONSUMPTION (25°C)

7.7.1 Memory +5V Voltage +5.006 Volts
Memory -6.1V voltage -6.103 Volts
+5V Current 10 ma
+5V Power 50.06 mw

7.7.2 Memory -6.1V Current 3.3 ma
Memory -6.1V Power 20.13 mw

7.7.3 Total Memory Idle Power 70.19 mw
170 mw max

7.7.5 Memory +5V Voltage +5.007 Volts
Memory -6.1V Voltage -6.105 Volts
+5V Current 67.0 ma
+5V Power 3354.69 mw

7.7.6 Memory -6.1V Current 230 ma
Memory -6.1V Power 1404.15 mw

7.7.7 Total Active Power 4758.84 mw
7000 mw max.

7.8 READ COMPLETE TIMING

7.8.5 Delay 390 ns
Duration 320 ns
500 ns max.
250 ns min
450 ns max.
## READ COMPLETE/DATA OUTPUT TIMING

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<td>DO-17</td>
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### LIMITS

REFER TO TEST PROC.
7.9 SYSTEM FUNCTIONAL TEST

7.9.2 Did an error occur?
No ☑ Yes ___ Address ___ Bits ___ 0 errors

7.9.4 Did an error occur?
No ☑ Yes ___ Address ___ Bits ___ 0 errors

7.9.10 Did an error occur?
No ☑ Yes ___ Address ___ Bits ___ 0 errors

7.9.16 Did an error occur?
No ☑ Yes ___ Address ___ Bits ___ 0 errors

7.10 RANDOM ACCESS CAPABILITY

7.10.6 Did an error occur?
No ☑ Yes ___ Address ___ Bits ___ 0 errors

7.10.7 Did an error occur?
a) No ☑ Yes ___ Address ___ Bits ___ 0 errors
S/W X 0 6

Date of Test Tested By

Limits

106

b) No

Yes Address Bits 0 errors

c) No

Yes Address Bits 0 errors

7.11 NON-VOLATILITY TEST

7.11.7 Did an error occur?

No

Yes Address Bits 0 errors

7.12 MEMORY SELECT TEST

7.12.3 Address 0000 (Octal)

7.12.4 Address 0001 0000 (Octal)

0010 0000 (Octal)

0011 0000 (Octal)

0100 0000 (Octal)

0101 0000 (Octal)

0110 0000 (Octal)

0111 0000 (Octal)

1000 0000 (Octal)

1001 0000 (Octal)

1010 0000 (Octal)

MOTOLLA INC.
Government Electronics Division

SIZE CODE IDENT NO. Dwg NO.
A 94990

12-P13721D
S/N 106

Date of Test 6/5/75

Tested By

Limits

Address 1011 0000 (Octal) 0000
1100 0000 (Octal) 0000
1101 0000 (Octal) 0000
1110 0000 (Octal) 0000

7.12.6 Did an error occur?
No
Yes Address Bits 0 errors

7.13 WORST CASE PATTERN TEST

7.13.2 Did an error occur?
No
Yes Address Bits 0 errors

7.13.3 Did an error occur?
No
Yes Address Bits 0 errors
7.13.4

a) Did an error occur?
No
Yes ___ Address ___ Bit ___ 0 errors

b) Did an error occur?
No
Yes ___ Address ___ Bit ___ 0 errors
### Vibration Test

**Date:** 24-75  
**Project:** 464-400  
**Unit:** P/U Auxiliary  
**Control No.:** 01-02  
**W.O. No.:** 30-41  
**Operator:** [Signature]  
**Observer:** [Signature]  
**Cycle Time:** 1 min  
**Freq.:** 15 to 2 kHz  
**Random SHAPE:**

#### Spec Details:

12-0137221

#### Axis Table:

<table>
<thead>
<tr>
<th>Run No.</th>
<th>Time Start</th>
<th>Time Stop</th>
<th>Accumulated Vib. Time</th>
<th>Unit Ser. No.</th>
<th>Displacement</th>
<th>Acceleration</th>
<th>Remarks</th>
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<tr>
<td>1</td>
<td>T2.25 min</td>
<td>T2.227 min</td>
<td>106</td>
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<td>5.61</td>
<td>RESPONSE ACC = 6.15 G RMS</td>
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<td>T2.35 min</td>
<td>T2.411 min</td>
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<td>.33</td>
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<td>10-5</td>
<td>20-35</td>
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<td>3</td>
<td>15.20</td>
<td>15.34</td>
<td>106</td>
<td>.33</td>
<td></td>
<td>10-5</td>
<td>20-35</td>
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<td>T3.402 min</td>
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<td>RESPONSE ACC = 5.9 R M S</td>
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<td>20-35</td>
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<td>.33</td>
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</table>

**End Test**
PROJECT: 4601-400  P/W Memory  SER. NO. 106

X&Z AXIS  SAMPLE (LOOP) TIME  10 SECONDS

FILTER B.W. 1.5 HZ SCAN RATE 1.25 HZ AVG. TIME 10 SECONDS
2.10 HZ SCAN RATE 2.25 HZ AVG. TIME 10 SECONDS
3.20 HZ SCAN RATE 3.5 HZ AVG. TIME 10 SECONDS
4.50 HZ SCAN RATE 4.25 HZ AVG. TIME 10 SECONDS

FREQ. RANGE 1.15-20 HZ  MOTOROLA SPECIFICATION NO.
2.20-40 HZ  CUSTOMER SPECIFICATION NO.
3.20-100 HZ
4.100-2K HZ

VIBRATION DATE 6-24-75
DATE ANALYZE 6-23-75  CV. O. Smith
VIBRATION TOLERANCE LEVEL SHOWN

REMARKS

ORIGINAL PAGE 1
OF POOR QUALITY
PROJECT 4601-400 UNIT P/N Memory SER. NO. 106

X... AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1.25 Hz SCAN RATE 1.25 Hz A.G. TIME 1.10 SECONDS
2.25 Hz SCAN RATE 3.25 Hz A.G. TIME 2.10 SECONDS
3.75 Hz SCAN RATE 3.75 Hz A.G. TIME 3.10 SECONDS
4.50 Hz SCAN RATE 4.25 Hz A.G. TIME 4.10 SECONDS

FREQ. RANGE 15-20 Hz MOTOR SIGNAL GATING NO.

VIBRATION DATE 6-24-75

DATE ANALYZED 6-24-75 BY O. Smith

VIBRATION TOLERANCE LEVEL N/A

REMARKS X axis response

Power Spectral Density (g^2/Hz)

Frequency (Hz)
Varnings:
FILTER B.W. 1. 50Hz SCAN RATE 1.25Hz AVG. TIME 1.10 SECONDS
2. 1.0Hz SCAN RATE 2.25Hz AVG. TIME 2.10 SECONDS
3. 2.0Hz SCAN RATE 2.25Hz AVG. TIME 3.10 SECONDS
4. 5.0Hz SCAN RATE 2.25Hz AVG. TIME 4.10 SECONDS
FREQ. RANGE 1. 15-20 Hz 2. 20-40 Hz 3. 40-100 Hz 4. 100-2000 Hz
MOTOROLA SPECIFICATION NO. 106
CUSTOMER SPECIFICATION NO.
VIBRATION DATE 6-24-75
DATE ANALYZED
VIBRATION TOLERANCE LEVEL shown
REMARKS

Frequency (Hz)
PROJECT 4601-400  P/W Memory  SER. NO. 106
UNIT X&Z AXIS SAMPLE (LOOP) TIME 10 SECONDS

FILTER B.W. 1.5 HZ SCAN RATE 1.125 HZ AVG. TIME 10 SECONDS
2.0 HZ SCAN RATE 2.25 HZ AVG. TIME 10 SECONDS
3.2 HZ SCAN RATE 3.5 HZ AVG. TIME 10 SECONDS
4.5 HZ SCAN RATE 4.25 HZ AVG. TIME 10 SECONDS

FREQ. RANGE 1.15-20 HZ MOTOROLA SPECIFICATION NO.
2.20-40 HZ CUSTOMER SPECIFICATION NO.
3.40-100 HZ
4.100-2K Hz

VIBRATION DATE 6-24-75
DATE ANALYZED 6-21-75 BY O. Smith
VIBRATION TOLERANCE [LEVEL] SHOWN

REMARKS

Power Spectral Density (g^2/Hz)

Frequency (Hz)
### HIGH VACUUM TEST

- **Unit**: Plated Wire
- **Project**: 4601-400
- **Serial**: 106
- **Operator**: Joe Mollere
- **Observer**: Lee Goulden

<table>
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<th>PRESSURE (mm Hg A)</th>
<th>REMARKS</th>
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<td>VENT TO ATM. END TEST</td>
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**REMARKS**

- START TO H. VAC
- END TEST
**SHOCK TEST**

(DROP)

---

**PROJECT**

4601-400

**DATE**

18 June 75

**SHEET**

1 of 1

**W.O. NO.**

3040

**CONTROL NO.**

Altered Wire Memory

**SERIAL NO.**

106

**OPERATOR**

Cathy Martin

**OBSERVER**

Kee Louden

**VIBRATION MOUNTS**

NONE

**NO. OF DROPS PER DROP**

6

**TOTAL NO. OF DROPS**

C

**ACCELERATION**

30 G's

**PULSE DURATION**

6.412 MS

**SPEC DETAILS**

P137220 as received by Motorola from Kee Louden dated 6-18-75

---

**DROP HEIGHT**

3/4 + 3 1/4 IN.

**PROGRAMMER PRESSURE**

N/1 P.S.I.

**TYPE OF WAVESHAPE**

Low Sine

**BANDPASS FILTER**

4300 LOW FR. Hz

**REMARKS**

3 drops at 6MS and 3 drops at 12MS

---

**PAD AND PLATE CONFIGURATION**

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<td>1'' red open B</td>
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<tr>
<td>MRL235Y</td>
<td>Alum plate B</td>
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<td>Plastic</td>
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<td>Red line</td>
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<td>Red line</td>
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<td>1'' blue closed</td>
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<tr>
<td>1'' blue open</td>
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**AXIS**

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