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STICAP
A LINEAR CIRCUIT ANALYSIS PROGRAM WITH STIFF SYSTEMS CAPABILITY
Volume II - User's Manual

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ABSTRACT

STICAP (Stiff Circuit Analysis Program) is a FORTRAN IV, Version 2.3, computer program written for the CDC-6400-6600 computer series and SCOPE 3.0 operating system. It provides the circuit analyst a tool for automatically computing the transient responses and frequency responses of large linear time invariant networks, both stiff and non-stiff. The circuit description and user's program input language is engineer-oriented, making simple the task of using the program.

Three volumes of documentation are available for the STICAP program; a theory manual, a user's manual, and a system's programmers manual. Volume I describes the engineering theories underlying STICAP and gives further references to the literature. Volume II, the user's manual, explains user interaction with the program and gives results of typical circuit design applications. Volume III depicts the program structure from a system's programmers viewpoint and contains flow charts and other software documentation.

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CHAPTER I

GENERAL PROGRAM DESCRIPTION

1.0 INTRODUCTION

The program STICAP - Stiff Circuit Analysis Program - was developed by personnel of the School of Engineering, Old Dominion University, Norfolk, Virginia, 1970-1971, under contract NAS1-9434-25. This program package represents the merging into one diversified computer aided network design program the capabilities of the existing programs CORNAP,[1] for linear circuit analysis; Gear's ALGORITHM 407 - DIFSUB,[2] for numerical integration of stiff ordinary differential equations; and a somewhat specialized matrix solution technique for obtaining time domain circuit response.

The composite program thus consists of three separate component programs, or modes of operation, each with some advantages over the others, in different circumstances. The CORNAP mode consists of the circuit analysis programs and capabilities of the original program CORNAP. In the Gear and Matrix modes the circuit translation routines of the program CORNAP are employed to obtain the state variable differential equations of the circuit, but different techniques for solving these equations are used. The functions and limitations of the various modes are described in the sequel.

The program STICAP is written in the FORTRAN IV, version 2.3 language. It is machine compatible with the CDC 6400-6600 computer series and runs under the SCOPE 3.0 operating system. It is segmented

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[1]Developed by Dr. Christopher Pottle, Cornell University, Ithaca, N.Y.

[2]Developed by Dr. C. W. Gear, University of Illinois, Urbana, Illinois

in overlays of 70K or less using the SCOPE OVERLAY capability. All I/O is accomplished using standard I/O files. The I/O files are equivalenced so that File 5 is used for input and File 6 for output. No other files are used by this program.

1.1 PROGRAM FUNCTIONS AND CAPACITY

This program has the capability of obtaining, at the option of the user, certain combinations of the following quantities: state variable equations, transfer functions, frequency and time responses, of an n-port linear active time invariant network.

The starting point for the program's analysis is a user oriented circuit description stated in terms of circuit branch elements and circuit nodes. The largest network configuration of these elements accepted by the program may be determined as follows. Let E be the number of energy storage elements; I the number of inputs; N the number of outputs; R the number of resistors; and C the number of controlled sources present in the network. The maximum number of elements of each type are governed by the constraints

$$E + I \leq 30,$$

$$E + N \leq 30,$$

$$R + C \leq 28.$$

In the Gear and Matrix modes the additional constraints

$$I \leq 10, \; N \leq 10$$

are imposed.

1.2 PROGRAM SELECT OPTIONS

The user may select one of the following mutually exclusive modes of operation: the CORNAP mode, the GEAR mode, or the matrix

mode. The first of these, the CORNAP mode, embodies the network analysis capabilities of the original program CORNAP, with choice suppression of certain print features, such as the printing of state equations and transfer functions. This program mode translates a circuit description from user language in terms of circuit nodes and branch elements to a mathematical description in terms of the state variable differential equations and algebraic state-output equations of the circuit. The option is provided for subsequent calculation of transfer functions, zeroes of transmission, and frequency or time response of the circuit.

The Gear mode may be used to perform time response calculations only. Here the circuit equations are generated by the CORNAP subroutines, and either stiffly stable implicit linear multistep methods or the non-stiff Adam's integration techniques may be selected for numerical integration of the state equations. In this mode a maximum of ten independent sources may be simultaneously used to drive the network, and up to ten simultaneous outputs may be requested. The full power of the FORTRAN language may be employed to describe the mathematical equations governing the behavior of the independent sources, or the user may wish to write his own program for input of sampled data.

Finally, the matrix mode may also be used for performing time response calculations, employing the circuit equations generated by CORNAP subroutines. The solution of these equations is obtained by means of a matrix technique which avoids a numerical integration. The technique is computationally rapid, but it is applicable only in

the case of linear time invariant systems whose eigenvalues are not closely-grouped, and which are forced by sinusoidal, cosinusoidal, or step function inputs. Only a limited number of such inputs are allowed. The circuit may be driven by a maximum of ten simultaneous independent sources, and a maximum of ten outputs may be requested.

1.2 NETWORK ACCEPTIBILITY

This program package will perform the complete analysis of any lumped, linear time invariant network, whether stiff or non-stiff. The elements making up the network may be of the following types:

1) ordinary two-terminal passive circuit elements - resistance, inductance, and capacitance;
2) mutual inductance and capacitance;
3) the four two-terminal controlled sources (voltage/current controlled voltage/current sources).

Two port active and nonreciprocal elements such as negative impedance convercers, ideal transformers and gyrators can be made up of the one port elements described above. Inputs are defined by attaching independent voltage and current sources to the network. Unity coupled transformers (or even n-port inductors with a semidefinite inductance matrix) can be handled by the procedure, as can all resistive networks

1.4 SOURCE DERIVATIVES

Source derivatives will occur in the state variable equations describing a circuit whenever a voltage source is connected in a loop containing only capacitors and other voltage sources, or a current source is connected in a cut set containing only inductors and other

current sources. Although the state variable equations describing passive circuits may contain only the first derivative of circuit inputs, the equations describing active circuits may contain any number of input derivatives. An active circuit whose state variable equation contains a second derivative is shown in Figure 1. The state variable and output equations for this circuit are

$$\frac{dV_{c3}}{dt} = -.5V_{c3} + .5\,\frac{d^2V_1}{dt^2}$$

$$V_0 = V_{c3} \quad \frac{d^2V_1}{dt^2}$$

The CORNAP mode will not compute time domain responses for circuits with input derivatives in the state output equations. The GEAR and MATRIX modes allow only a first derivative of the circuit inputs in the state variable equations as long as no input derivatives occur in the output equations. In this case the state variable equations and the output equations would be of the form

$$\dot{\underline{X}} = \underset{\sim}{A}\underline{X} + \underset{\sim}{B}\underline{u} + \underset{\sim}{B}_1\dot{\underline{u}}$$

$$\underline{Y} = \underset{\sim}{C}\underline{X} + \underset{\sim}{D}\underline{u}$$

A second choice of state variables

$$\underline{\sigma} = \underline{X} + \underset{\sim}{B}_1\underline{u}$$

would then be made transforming the original state variable and output equation into

$$\dot{\underline{\sigma}} = \underset{\sim}{A}\underline{\sigma} + (\underset{\sim}{B} + \underset{\sim}{A}\underset{\sim}{B}_1)\underline{u}$$

$$\underline{Y} = \underset{\sim}{C}\underline{X} + (\underset{\sim}{D} + \underset{\sim}{C}\underset{\sim}{B}_1)\underline{u}$$

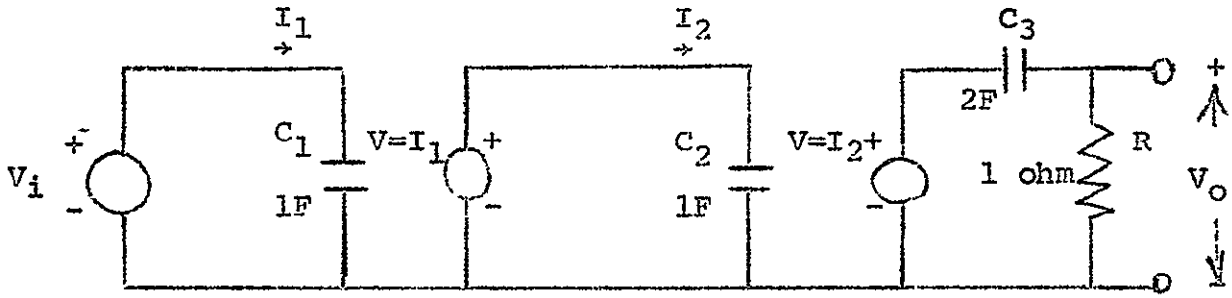

Figure 1

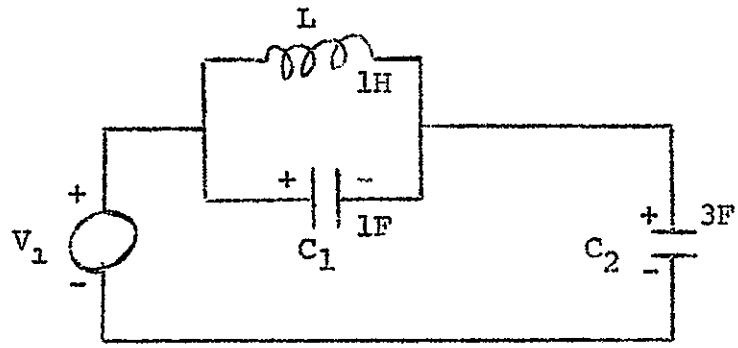

Figure 2

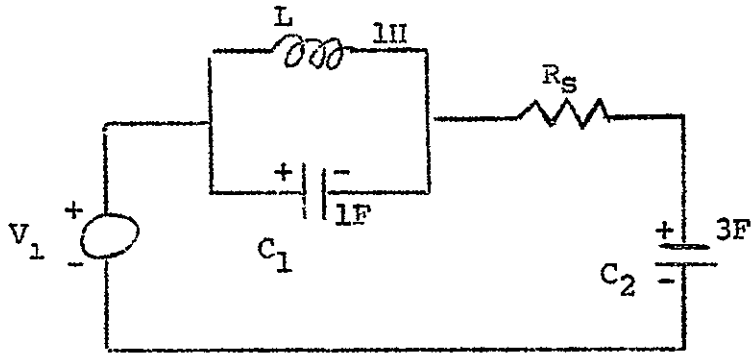

Figure 3

where no input derivatives occur. For example, consider the circuit in Figure 2. The state variable equations for this circuit are

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_{c1}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -\frac{1}{4} & 0 \end{bmatrix} \begin{bmatrix} i_L \\ V_{c1} \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{3}{4} \end{bmatrix} \frac{dV_1}{dt}$$

Whether an input derivative occurs in the output equations depends upon the choice of the outputs. If V_{c3} were chosen as the output, the output equation would be

$$V_{c2} = [0 \; -1] \begin{bmatrix} i_L \\ V_{c1} \end{bmatrix} + V_1$$

For the GEAR and the MATRIX mode, these equations would then be transformed into the equivalent form

$$\begin{bmatrix} \frac{dq_1}{dt} \\ \frac{dq_2}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -\frac{1}{4} & 0 \end{bmatrix} \begin{bmatrix} q_1 \\ q_2 \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{3}{4} \end{bmatrix} V_1$$

$$V_{c2} = [0 \; - 1] \begin{bmatrix} q_1 \\ q_2 \end{bmatrix} + \frac{1}{4} V_1$$

If, however, i_{c_1} were chosen as the circuit output, the output equation would be

$$i_{c1} = \left(-\frac{1}{4}, 0\right) \begin{bmatrix} i_L \\ V_{c1} \end{bmatrix} + \frac{3}{4} \frac{dV_1}{dt}$$

and no solution would be attempted by any of the three solution modes.

Care should be taken when describing the inputs to a circuit with input derivatives. Due to the fact that inductor currents and

capacitor voltages cannot change instantaneously, inputs to these types of circuits must not be allowed to have jump discontinuities. Moreover, the initial conditions of the circuit must be chosen such that the circuit at time $t = 0^+$ obeys Kirchhoff's voltage and current laws. For example, if the circuit in Figure 2 were to be driven with the voltage source

$$V_1 = \cos(t)$$

the initial capacitor voltages must be chosen such that

$$V_{c1}(0) + V_{c2}(0) = V_1(0) = 1.$$

In that the initial conditions of a circuit are chosen to be zero for impulse and step calculations, neither the GEAR nor the MATRIX mode will calculate the step or the impulse response of a circuit whose solution equations contain input derivatives.

The source derivatives can be eliminated from the solution equations by including the internal resistance of the voltage sources and the parallel conductances of the current sources. Thus, if the internal resistance R_s of the voltage source in Figure 2 were included in the circuit description as shown in Figure 3, the state variable and output equations would become

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_{c1}}{dt} \\ \frac{dV_{c2}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ -1 & -\frac{1}{R_s} & -\frac{1}{R_s} \\ 0 & -\frac{1}{R_s} & -\frac{1}{R_s} \end{bmatrix} \begin{bmatrix} i_L \\ V_{c1} \\ V_{c2} \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{R_s} \\ \frac{1}{R_s} \end{bmatrix} V_1$$

$$\begin{bmatrix} V_{c2} \\ i_{c2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ 0 & -\frac{1}{R_s} & -\frac{1}{R_s} \end{bmatrix} \begin{bmatrix} i_L \\ V_{c1} \\ V_{c2} \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{R_s} \end{bmatrix} V_1 .$$

CHAPTER II

CIRCUIT DESCRIPTION AND MODE SELECTION

2.0 OVERVIEW OF CARD INPUT DECK SETUP

In this chapter the manner in which the user describes his circuit to the program STICAP will be discussed. As a means of introduction an illustration of the overall deck setup of the cards which must be prepared is indicated by Figure 1.

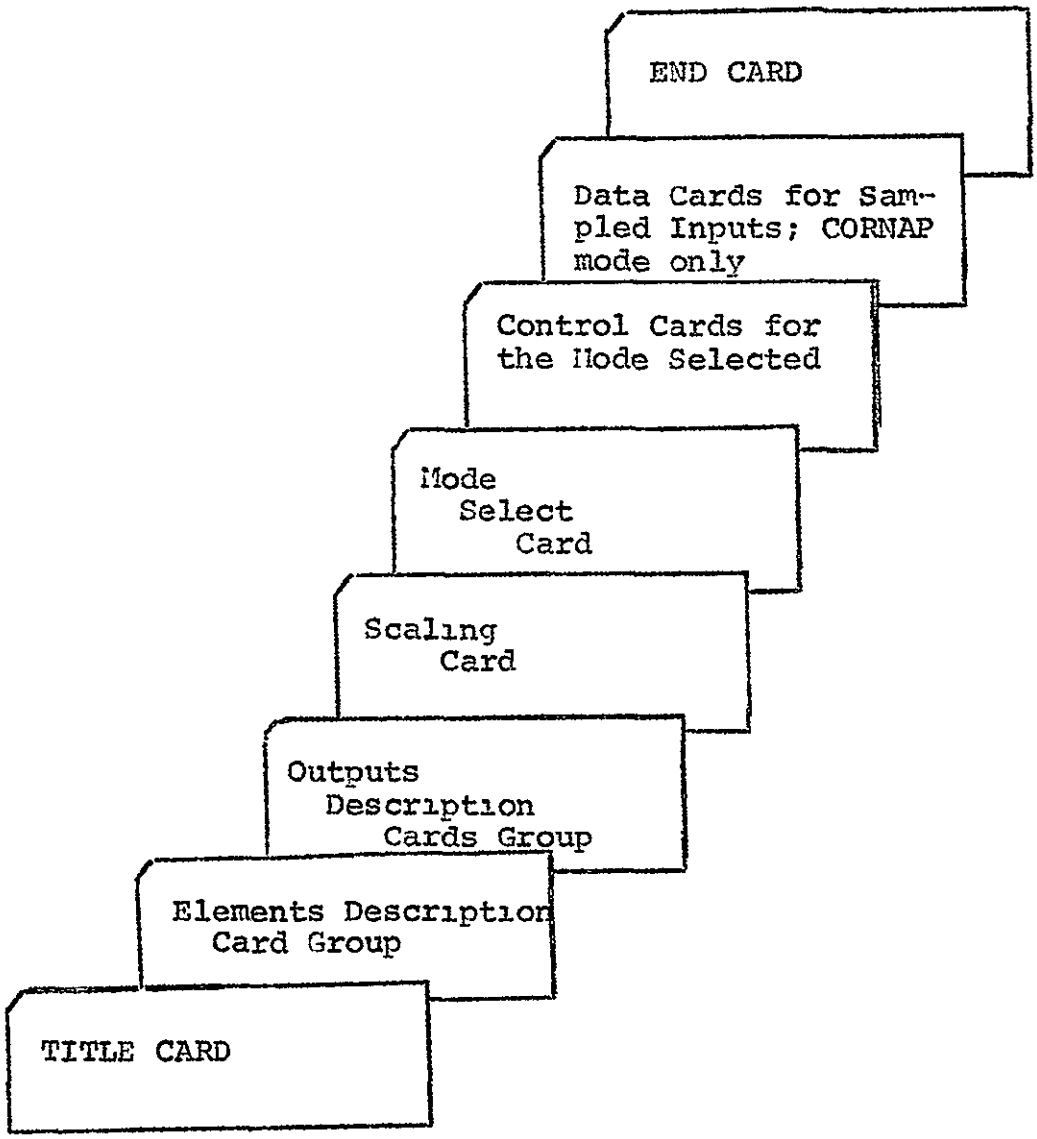

Figure 1 - Overview of Deck Setup

The contents of the title card are printed out verbatim at the head of each section of the output, and serve as a means of identification to the user. As such, the user has complete freedom in

specifying the contents of this card. The elements description card group is used to specify the interconnections between nodes and branches of the circuit. The outputs card group is used to specify the circuit currents and voltages desired as outputs by the user. The scaling card specifies the manner in which the circuit is to be scaled for computational purposes. The mode select card determines which of the Gear, CORNAP or Matrix modes is to be selected for analysis. A different group of control cards is needed, depending upon which mode is selected. These cards specify the output options selected and contain information needed by the numerical integration and analysis routines. In the CORNAP mode only, a series of card groups consisting of a control card followed by sampled input data cards may sometimes appear. An end card is always present, regardless of mode.

2.1 ELEMENTS DESCRIPTION CARD GROUP

The first card in the group is a header card

```
*  ELEMENTS
```

containing an asterisk in column one. The word "ELEMENTS" may appear anywhere on the card (data fields whose length and starting position on the card may be arbitrarily selected by the user are said to be free form data).

All elements description cards are free form. One card must be prepared for each circuit element. Card format for passive elements or independent sources is

```
NAME N1 N2 VALUE,
```

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and for independent sources is

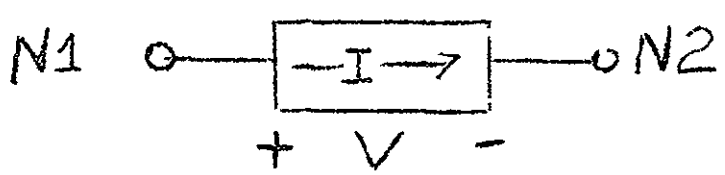
- NAME N1 N2 VALUE*NAME2.

NAME, N1, N2, and VALUE must be separated by at least one blank. The asterisk between VALUE and NAME2 need not be present.

NAME is the user's name for the circuit element. This name may be a maximum of four characters long. The first letter of the element name is used to specify the element type as indicated:

First Letter	Element Type
V	Voltage source
I	Current source
R	Resistor
L	Inductor
C	Capacitor
K	Coefficient of Coupling
M	Mutual inductance or Capacitance

For non-mutual elements N1 and N2 are the node numbers (two digit integers) of the nodes between which the element is connected. The circuit nodes should be ordered compactly from zero (00), although the failure to do so is non-fatal. Node 00 should be the reference node, or ground. The maximum number of nodes is 64. N1 is given a positive reference with respect to N2.



For mutual elements N1 and N2 are the element names of the two element

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involved.

For dependent sources NAME2 is the name of the controlling element, with a V or an I prefixed as the first letter of the name, to indicate respectively the occurrences of a voltage controlled or current controlled element.

A feature not normally employed by the average user is the following. By placing the word "TREE" after the description of the element, as in

NAME N1 N2 VALUE TREE,

a capacitor may be forced into the proper tree. An inductor may similarly be forced into the cotree by placing the word "COTREE" there, i.e.,

NAME N1 N2 VALUE COTREE.

VALUE is the value of the element or strength of the source. Negative values are permissible. Zero values are also allowed for inductors and capacitors and may be used to define fictitious branches for output or control purposes. No entry need be given for independent sources. VALUE may be any integer, decimal, or floating point number with a maximum of 15 digits in the mantissa, and where magnitude is in the range 10^{-290} to 10^{+290}.

2.2 OUTPUTS DESCRIPTION CARDS GROUP

The element currents and voltages selected by the user as circuit outputs are indicated by this card group. The header card, free form except for the asterisk in column one, has the format:

* OUTPUTS

The output cards, ordered in any fashion, are of one of the forms

VNAME

or INAME,

depending upon whether the voltage across or current through the element with this element name is desired. Here NAME is the name of a circuit element given in the elements description card group. One card must be prepared for each desired output.

2.3 SCALING CARDS GROUP

The scaling cards, in free format, are preceded by a header card with an asterisk in column one

* SCALING

followed by one or both of the cards

FREQUENCY = VALUE1

and IMPEDANCE = VALUE2.

VALUE1 and VALUE2 represent respectively the frequency (rad/sec) and impedance level (ohms) about which the network is designed to operate. These numbers, ideally, are used as scale factors to scale the network to operate around 1 rad/sec and a 1 ohm impedance level. A scaling factor several magnitudes away from its proper value can be computationally critical; hence some attention should be paid to determining scale factors which cause scaled element values to bracket the value unity* The scaling values may be integer, decimal, or floating point, as specified in section (2.1).

The scaling cards group may be omitted, but if so the user should be careful to use a consistent set of units for the circuit. Most standard texts on network theory include a section on circuit

---

*See Appendix I for further discussion of scaling.

scaling, and the concept should be understood by the user before attempting to design with STICAP.

If the scaling option is chosen, the Gear and Matrix mode output remains scaled by the same factors. In the CORNAP mode the choice of unscaling the output is present.

2.4 MODE SELECT CARD

Regardless of which mode is to be selected, the user's deck set-up is the same as is indicated by Figure 1, up to and including the scaling cards. Thereafter it changes with the individual mode. In this section the mode select cards and the control cards for each mode will be described.

The mode select cards are of the general form

*MODE NAME, OPTION, OPTION, OPTION.

The asterisk necessarily appears in column 1, followed by the mode name of the mode selected, and the options chosen. All data fields other than the asterisk may be free form, but must be delimited by commas. The omission of any option indicator results in the omission of that particular option. The options need not occur in any specific order on the mode select card.

The mode select cards for each mode, with all possible options present, are given below.

MODE NAME	OPTION INDICATORS
CORNAP MODE	STATE EQUATIONS, TRANSFER FUNCTIONS
GEAR MODE	STATE EQUATIONS, TRANSFER FUNCTIONS
MATRIX MODE	STATE EQUATIONS, TRANSFER FUNCTIONS, SOLUTION EQUATIONS

In all three modes the matrices of the state-input and state output equations

$$\bar{x}' = A\bar{x} + B\bar{u} + C_1\bar{u}' + B_2\bar{u}' + \ldots$$

$$\bar{y} = C\bar{x} + D\bar{u} + E_1\bar{u}' + D_2\bar{u}'' + \ldots$$

may be printed, using the option indicator "STATE EQUATIONS." However, if a higher order derivative than the first occurs in the state-input equations, or if any derivative at all occurs in the output equations, numerical integration of these equations cannot be performed, since no allowance is made for user input of source derivatives.

If the transfer functions indicator appears on the mode select card, the poles, zeroes, and gain constants of the transfer functions of each input-output pair are printed. In the matrix mode the network equations are presumedly solvable in closed form, and the exact solution equations may be printed by means of the third option indicator. This feature prints the solution equations governing the time domain behavior of the state variables. The combined output of these equations together with the matrices of the state output equations allows the user a complete closed form description of the solution.

Example 1

The following cards effect the same result, the choice of the Gear mode with its full options:

```
*    GEAR MODE,    TRANSFER FUNCTIONS   ,STATE EQUATIONS
*GEAR,  STATE,  TRANS  FER
*G,  STA,  TRA  N
*G    , TRA       , STA
```

The program reads only the first letter of the mode name and the first 3 letters of each option indicator. Errors in the mode name are fatal; those in options selection are merely indicated by error messages, with the indeterminate option omitted.

Example 2 - Fatal error in mode name.

```
*HEAR
```

Example 3 - Error diagnostics; MATRIX option chosen, contrary to desires of the user; print request ignored.

```
*HEAR    TRANSFER       (Comma omitted)
*HORNAP   ,T RANSFER    (Incorrect option indicator)
```

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CHAPTER III

CONTROL CARDS GEAR MODE

3.0 GENERAL MODE DESCRIPTION

The primary purpose of the Gear program mode is the obtaining of time domain circuit response for stiff circuits, using stiffly stable implicit linear multistep methods for performing the numerical integration. The response of non-stiff circuits may be obtained equally as well, since the option of choosing the Adam's linear multistep methods, suitable for non-stiff integration, is available. Since little extra effort is required to do so, the optional capability of obtaining the poles, zeroes, and gain constants for the transfer functions of each input output pair in the network is included. The time domain response of a circuit with up to ten simultaneous inputs or outputs may be obtained. The inputs may be described using the full power of the FORTRAN language, or the user may wish to write his own routine for inputting sampled data, as indicated in the description of the user routine USEFCN.* Thus the Gear mode is the most powerful general purpose analysis component. Its one possible drawback, as opposed to the CORNAP mode, is that the input waveforms cannot be changed without reprocessing the entire circuit, and it cannot be used for frequency response calculations.

The control cards for this mode will now be described (see Figure II).

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*Subroutine USEFCN is a user supplied routine which specifies the independent sources of the circuit, discussed at a later point.

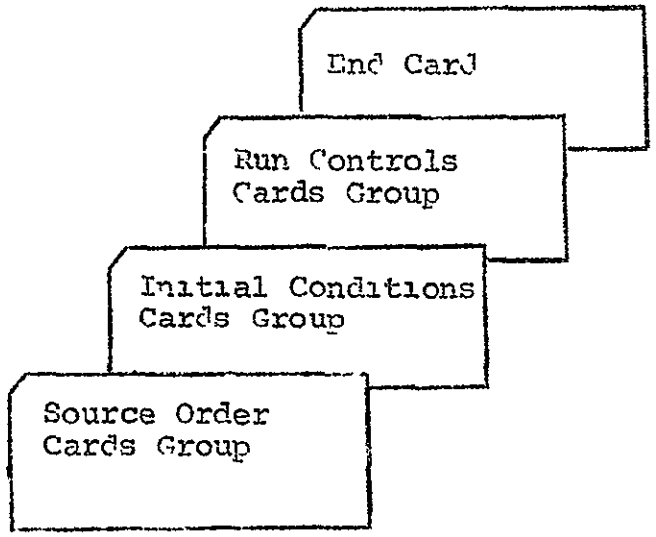


Figure II - Control Cards; Gear Mode

These control cards may be classed in the categories: source order cards, initial conditions cards, and run control cards. It is not essential that the ordering of the three card groups within the deck setup be as indicated by Figure II; however, this ordering should process fastest. Cards composing each individual group will now be described.

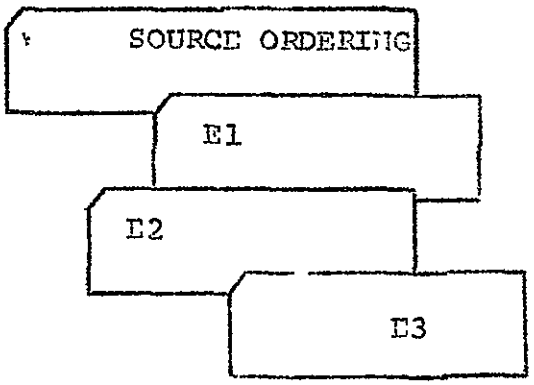
3.1 SOURCE ORDER CARDS GROUP

(a) Header card - The first card in this group contains an asterisk in column 1, followed by the words "SOURCE ORDERING," in free form.

(b) Source name cards - These cards must be ordered in the sequence that the values of the independent source functions U(1), U(2),...,U(N) are computed by the user-supplied routine USEFCN. The name of the corresponding independent source appears anywhere on the card. This name must be

the same as the name given this source on the circuit description cards.

Ex



The number of source names must be the same as the number of independent sources defined when describing the circuit, else the program is terminated. If the number of names does not agree with the number of functions defined in USEFCN as sources, the program is also terminated. If an impulse response is to be computed, only one independent source is involved; hence, only one source should be specified when describing the circuit.

The source names and the order these source values are computed is necessary in order to set up the proper correspondence between components of the source vector as computed by the user, and the order in which these sources appear ordered by the circuit translation program.

If only one source is defined in the circuit description, this card group need not be present.

3.2 INITIAL CONDITIONS CARD GROUP

(a) Header card - The first card in this group contains an

asterisk in column 1, followed by the words 'Initial Conditions,' in free form; i.e. no specific starting column for either word.

(b) Value cards - These cards may be ordered in any fashion and are also free form. Each card contains the name of a component of the state vector of the circuit, as well as its value, in the form

NAME = Value.

Here NAME is the same as the name specified on the circuit description cards, and 'Value has one of the formats

a) integer

b) decimal

c) exponential - exponent field of length 3.

The components of the state vector are the capacitor voltages and inductor currents of the circuit.

Examples -

C1 = .003

L2 = 2.E + 003

C2 = 3E - 003

C5 = 6

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If this card group is not present, it is assumed that the initial state is zero. Any state variable not assigned an initial value is assumed to have an initial value of zero.

3.3 RUN CONTROLS CARD GROUP

This card group supplies data needed by Gear's program, and allows selection of certain options. Individual cards in the

group are as follows:

(a) Header card - The first card in the group, which contains an asterisk in column 1, followed by the words "RUN CONTROLS," in free form.

(b) Integration control cards - These cards may be ordered in any fashion and are in free form. One card is required for each of the following items, if the item is selected as an option by the user:

1. Initial time - This is the lower limit of integration and the time at which the initial conditions are measured. This card need not be given if the initial time is zero. It will be of the form:

   INITIAL TIME = A

   where A is a floating point number.

2. Impulse or step response - The impulse or step response of the circuit is found if one of the following two cards is present:

   STEP RESPONSE

   IMPULSE RESPONSE

   Only one of these cards may be given. Note that USEFCN is not to be supplied by the user if the impulse or step response is to be calculated.

3. Print starting time - This card gives the value of time at which output printing is to begin. The card will be of the form:

   PRINT START = A

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where A is a floating point number. If this card is not given, printings will begin at the initial time.

4. Upper integration limit - The upper limit for the integration may be given by specifying the stop time or by specifying the number of time points printed. This card will be one of the two forms:

STOP TIME = A

POINTS PRINTED = N

where A is a floating point number and N is an integer number. If a stop time is given, interpolation is used to determine the values of the outputs at the stop time. If neither card is given, 100 time points will be printed.

5. Error controls - The value of EPS controls the accuracy of Gear's integration routines. The Euclidean norm of a vector whose Ith component is the single step error of the Ith state variable divided by the maximum value of the Ith state variable, must be less than this value. This card will be of the form

EPS = A

where A is a floating point number. If this card is not given, EPS is assumed to be 10^{-4}.

6. Integration method - An integration method suitable for stiff systems is normally used. A predictor-corrector Adam's integration method, however, may be chosen by including the following card:

ADAMS INTEGRATION

7. Print density - The number of integration steps between printings is given by this card and is of the form

OUTPUT DENSITY = N

where N is an integer. If not given, printings will take place after every third integration step.

8. Step size controls - The size of the integration step is controlled by the integration routine; however, the maximum step size, minimum step size, and initial step size may be specified by the user. These cards will be as follows:

HMAX = A

HMIN = A

HINIT = A

where A is a floating point number. If HMAX is not given, it is set to one tenth of the stop time minus the initial time, if the stop time was specified, and is unbounded otherwise. If HMIN is not given, it is set to zero. If HINIT is not given, it is set to 10^{-4}.

3.4 END CARD

The last card in the Gear input is an END card. The format is:

* END

with the asterisk in column 1.

3.5 USER SUPPLIED INPUT ROUTINE

The routine USEFCN is a subroutine which must be supplied by the user. The function of this routine is the following : Given a

specific time at which their values are needed by the integration routine, compute values U(I), I = 1,2,...N, N≤10 of the various independent sources and store them in an output source vector U.

This feature of STICAP supplies to the user two alternative capabilities: First, the independent sources may be defined in equation form, using the full power of the FORTRAN language. Second, values of the independent sources may be obtained by interpolation of data samples. This data could be supplied in tabular form, or be read in block by block at execution time.

The program STICAP has incorporated within it a skeleton USEFCN. This routine may be completed by addition of user supplied FORTRAN equation statements defining the independent source equations; or it may be replaced by a user supplied routine which at specified times computes by some means, such as indicated, the vector U of source values. Assuming STICAP resides on a data cell, this routine could be caused to replace the resident USEFCN routine prior to execution, by means of a CUTOUT card, or whatever UPDATE facilities are available.

It is essential that the source values in the USEFCN output vector be ordered in the same sequence in which the names of the independent sources occur on the user's SOURCE ORDERING cards. We emphasize that errors in this ordering <u>cannot be detected</u> by STICAP, and result in a grossly misleading circuit analysis.

<u>Sources defined by FORTRAN equations</u>

If there are N independent sources, the user supplies N statements of the form

```
U(1) = F1(T)
U(2) = F2(T)
```

Here T is a dummy argument whose value, when supplied by STICAP, specifies the time at which a vector of source values is required. The FI(T), I = 1,2,...,N, are FORTRAN equation statements defining the sources as a function of the dummy time variable T. The ordering of the values of U(I) is identical to the order in which the names of the sources occur on the source order cards.

The skeleton USEFCN contains the statements below:

```
      SUBROUTINE USEFCN (T,U)
      DIMENSION U(10)
      COMMON/RUN/SKIP (13), INPUT
      IF (INPUT.EQ.1) GO TO 10
      U(1) = 1.0
      GO TO 20

   10 U(1) = 0.0

   20 CONTINUE
      RETURN
      END
```

The FORTRAN equation defining statements produced by the user are to replace all statements starting with the COMMON statement and ending with statement number 20. These statements may be replaced using whatever UPDATE facilities are convenient.

Source Values Obtained by Interpolation

The circuit designer may wish to supply an interpolation routine which obtains the independent source values from tabular data defined within itself, or from data samples read in at execution time. If so, the onus is on the user to determine the necessary data density and precision of the interpolation scheme required in order to provide accurate intermediate values. Here it should be kept in mind that data values needed by Gear's integration scheme are not uniformly spaced, nor do they necessarily occur in a time sequence

which is ordered in terms of increasing time. Hence data points as much as one plot point (print increment) behind the current time point may next be required.

If this USEFCN option is chosen, the user's program size must be compatible with overlay sizes of the main program. The user written routine may be inserted in the program replacing the above listed USEFCN using whatever UPDATE facilities are convenient to the user. Any data cards read by this routine should follow the END card in the deck setup indicated by Figure I, Chapter II. If the data is read from tape, the tape cannot be defined as logical unit #5 or #6. The program card in the main overlay should be modified to include this tape number.

CHAPTER IV

CONTROL CARDS, MATRIX MODE

4.0 GENERAL MODE DESCRIPTION

The Matrix program mode provides a rapid means for obtaining time domain circuit response, for circuits with inputs restricted to the class of linear combinations of sinusoidal, cosinusoidal, step and impulse functions. Stiffness of the circuit does not affect the analysis, but rather the grouping of eigenvalues of the system matrix. Such eigenvalues should not be too closely grouped together, or computational error may become a problem. The optional capability of obtaining the poles, zeroes and gain constants for the transfer functions of each input-output pair in the network is included. Input waveforms may not be changed without reprocessing the entire circuit, and no frequency response calculations may be performed.

The control card deck setup for this mode is similar to that of the Gear mode (see Figure III). It is not necessary that the ordering of the card groups conform to the one given, however, this ordering should process most rapidly.

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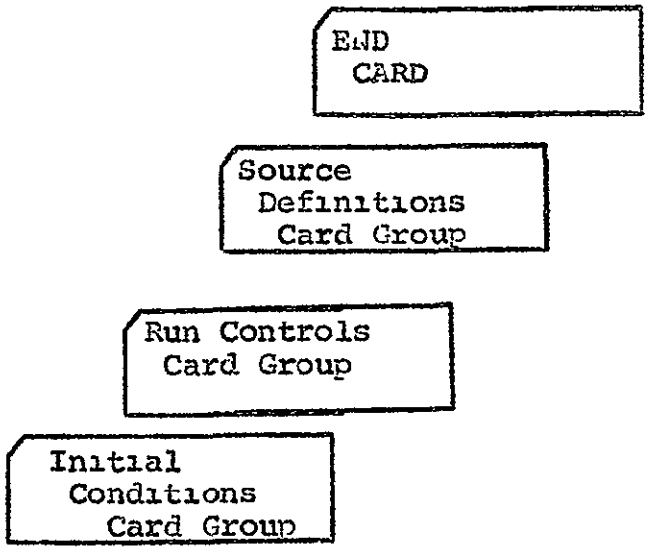

Figure III - Control Cards; Matrix Mode

The composition of each card group will now be given.

4.1 INITIAL CONDITIONS CARD GROUP

The cards needed in this group are the same as those of the Gear mode initial condition's description (see section III.3.2). This card group is not required if all initial conditions are zero, as in impulse response calculations.

4.2 RUN CONTROLS CARD GROUP

Individual cards in this group are as follows:

(a) Header Card - The first card in the group, which contains an asterisk in column one, followed by the words "RUN CONTROLS", in free form.

(b) Run Controls Cards - These cards may be ordered in any fashion, and may be punched in free form. One card must be present for each of the following options desired by the user:

1. <u>Initial time</u> - the lower limit of integration, and time at which initial conditions must be measured. Card format is

   INITIAL TIME = A

   where A is a floating point number. The initial time is assumed zero if this card is omitted.

2. <u>Response type</u> - the impulse or step response (with a step of amplitude 1) is calculated if one of the following format statements is present:

   STEP RESPONSE

   IMPULSE RESPONSE

If neither card is present, a source definition card group specifying the network inputs is mandatory.

3. Print starting time - Contains the time value at which output printing is to begin. Card format is

PRINT START = A

where A is a floating point number. If this card is omitted, printing begins at the initial time.

4. Upper limit of integration - May be specified by a stop time or number of points to be printed. Card format is one of the following:

STOP TIME = A

POINTS PRINTED = N

where A is floating point format and N is integer. If neither card is present, 100 time values of the outputs will be printed.

5. Print density - The plot increment between print points is specified in the format

PLOT INCREMENT = A

where A is floating point format.

4.3 SOURCE DEFINITIONS CARD GROUP

This card group consists of a header card followed by a source definition card for each driving source. The beader card contains an asterisk in column one, followed by the words "SOURCE DEFINITIONS CARD GROUP", in free form. A maximum of ten independent driving sources is permitted. Each source must be specified by a card (or cards) punched free form in the following format

NAME = F1(T) + F2(T) + ... + FM(T).

Here NAME is the name of an independent source specified when describing the circuit. The right member of the equation statement is a sum of functions FI(T), $I \leq 20$, where each FI(T) may have one of the forms

```
A
A*IMP
A*SIN(B*T)
A*SIN(B*T+C)
A*COS(B*T)
A*COS(B*T+C)
```

where A, B, C are free format floating point numbers.

The first form indicates a step function of amplitude specified by A, with jump at the initial time t_o; the second on impulse function $A\delta(t-t_o)$, the delta function of amplitude A. All other forms indicate sines and cosines of amplitude A, frequency f, $2\pi f=B$, and phase C. The asterisks indicating multiplication need not appear. A source description may be continued on additional cards by placing a dollar sign $ in column 1 of each continuation card, as long as each FI(T) is completely described on one card. No more than 20 FI(T) may compose one source; a sinusoid or cosinusoid with non-zero phase is considered as two functions, for purposes of counting.

4.4 END CARD

The end of the source definitions card group, and matrix input, is signalled by a card with an asterisk in column 1, of the form

```
* END.
```

CHAPTER V

CONTROL CARDS; CORNAP MODE

5.0 GENERAL MODE DESCRIPTION

The CORNAP mode embodies the capabilities of the original program CORNAP. This program mode may be used to obtain transfer functions, zeroes of transmission, and frequency or time response of the network. Assuming a network characterized by multiple independent driving sources and/or multiple output ports, the user may obtain, for each input-output pair, the preceding quantities. Furthermore, it is not necessary to reprocess the circuit description in order to obtain the outputs at a fixed port which occur when a different input port is used to drive the circuit. The same is true if it is desired to alter the wave form at a fixed port. Unfortunately, no capability is provided for computing a superposition of the outputs at a single port, assuming it were desired to drive a network with several simultaneous inputs. However, both the Gear and Matrix modes have this capability. For time domain analysis, step response, impulse response, or transient response with a sampled data driving input may be obtained. In all cases it is assumed that the initial state is zero. However, in both of the other modes, the initial state vector may be selected arbitrarily, in these instances for which such choice might be desirable.

5.1 CONTROL CARDS; DATA CARDS

The cards following the mode select card (see Fig. 1; Chapter II) needed to complete the user's deck setup for the CORNAP mode will be described in this section. These cards are <u>not</u> free format; information appears in a specific data field in a specific form. These

cards control the calculation and printing of time and frequency response data. In reading the card format description given below, it would be advantageous to keep in mind the following items: In the circuit description for the CORNAP mode, the network may be described as having multiple input ports and multiple output ports; the circuit translation routines then yield the proper set of state and state output equations for such a network. However, in the actual computation of circuit response, the responses are available in terms of input-output pairs; i.e., the response to a single input-single output linear time invariant system is computed. The CORNAP mode does not compute a summed response at a single output port for a circuit excited by several simultaneous inputs. Responses may be obtained for all possible input-output pairs, without reprocessing the circuit.

The control cards are prepared in the format below. However, if only state equations and transfer functions are desired, the cards now to be described may be omitted.

Any number of these cards may be present, in any order. If sampled data input is desired, one of these cards must be present for each individual desired input, with the data samples immediately following, as described below.

Col. 1

This column contains a character which defines the type of response desired:

F - frequency response

T - time response.

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Cols. 3-6

These columns contain either the name* of an input-defining independent source or are blank. Responses with this element as input are calculated if a name appears here; responses with each and every independent source as input are generated if the field is left blank. The field must not be left blank, for sampled data time response. Similar columns for output are cols. 33-36.

Cols. 8-9

Frequency Response

These columns contain a two-digit integer giving the number of decades of the frequency variable to be covered by a frequency response calculation if a logarithmic scale for frequency is chosen. Blanks in these columns indicate a linear scale is desired.

Cols. 10-12

A three-digit integer in these columns give the number of frequency or time points to be printed. For a logarithmic frequency scale, this number gives the number of points per decade.

Cols. 14-31

The increment in frequency or time between printed responses appears in these columns as a string of digits containing a decimal point. Exponential notation (1.5E -04 = 0.00015) may be used provided the exponent part is right-justified in the field (cols. 28-31).

Cols. 33-36

These columns contain either the name* of an element defined in

*left justified

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the outputs description (without the appended V or I) as determining an output port or are blank. Responses with this element as output are calculated if a name appears here; responses at each and every defined output are generated if the field is left blank.

Col. 38

Any nonblank character in this column will cause response calculations to remain scaled by the factors given previously. These scale factors will be used to "unnormalize" the calculations if this column is left blank.

Col. 41

Frequency response

A nonblank character in this column will cause the frequency scale to be in radians/sec. A blank in this column indicates the frequency scale is to be in Hz.

Time response

A blank in this column indicates the impulse and step response of the network are to be calculated; a nonblank character causes an external sampled input signal to be used as input. At present the samples of these signals are entered 6 to a card, each occupying 12 columns (cols. 1-12, 13-24,...,61-72), in the same way as the time increment between printouts was entered. As many input signals must be entered as inputs were defined in cols. 3-6 The first sample of an input signal must begin a new card. These cards follow immediately the time response control card now under discussion.

Cols. 44-61

Frequency response

The first (lowest) frequency at which a response is desired should be entered in these columns in the same way as the frequency increment between printouts was entered.

Time response

An integration step size may be entered in these columns, whose value governs the numerical integration producing the time response. If omitted, a step size guaranteeing roughly six-figure accuracy of the resulting response will be used. If present, either this or the next smallest step size which evenly divides the print interval will be used. If the response to external sampled input is requested, the sampling interval of the external signal must appear in these columns, and the print interval must be a multiple (≥ 2) of it.

5.2 END CARD

The last card in the input contains an asterisk in column one and has the free form format otherwise as indicated,

* END.

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CHAPTER VI

EXAMPLES OF USE

6.0 A PULSE FORMING NETWORK

A circuit consisting of two twin-tee networks connected by a negative impedance converter is indicated by Figure 4. STICAP input cards which might be used to analyze this circuit are indicated below. The node numbering in the elements cards group agrees with that given in the figure. A zero-valued capacitor CZ is used to establish a branch at the output across which the output voltage is available. First employed by Pottle in the original CORNAP program, this circuit is a realization by Antreich and Gleissner[3] of an optimum pulse forming filter proposed by Jess and Schussler.[4] The filter should have at most a one percent step response overshoot and a one percent stop band frequency response.

6.1 GEAR MODE ANALYSIS; USEFCN OPTION

The user's control cards needed to achieve an analysis of the previous circuit using the Gear integration routines are listed below in the order they would appear in the user's deck. In order to drive the network with the voltage source V_1 as a sinusoidal input the following CUTOUT cards were used to alter USEFCN:

```
CUTOUT   7700000   9700000
      U(1) = SIN(5.0*T)
```

---

[3]K. Antreich and E. Gleissner, "Uber die Realisierung von Impulsfiltern durch aktive RC-Netzwerke,' Arch. Elek. Ubertr., Vol. 19, 1965; pp. 309-316.

[4]J. Jess and H. W. Schussler, "On the Design of Pulse-Forming Networks," IEEE Trans., Vol. CT-12 (September 1965), pp. 393-399.

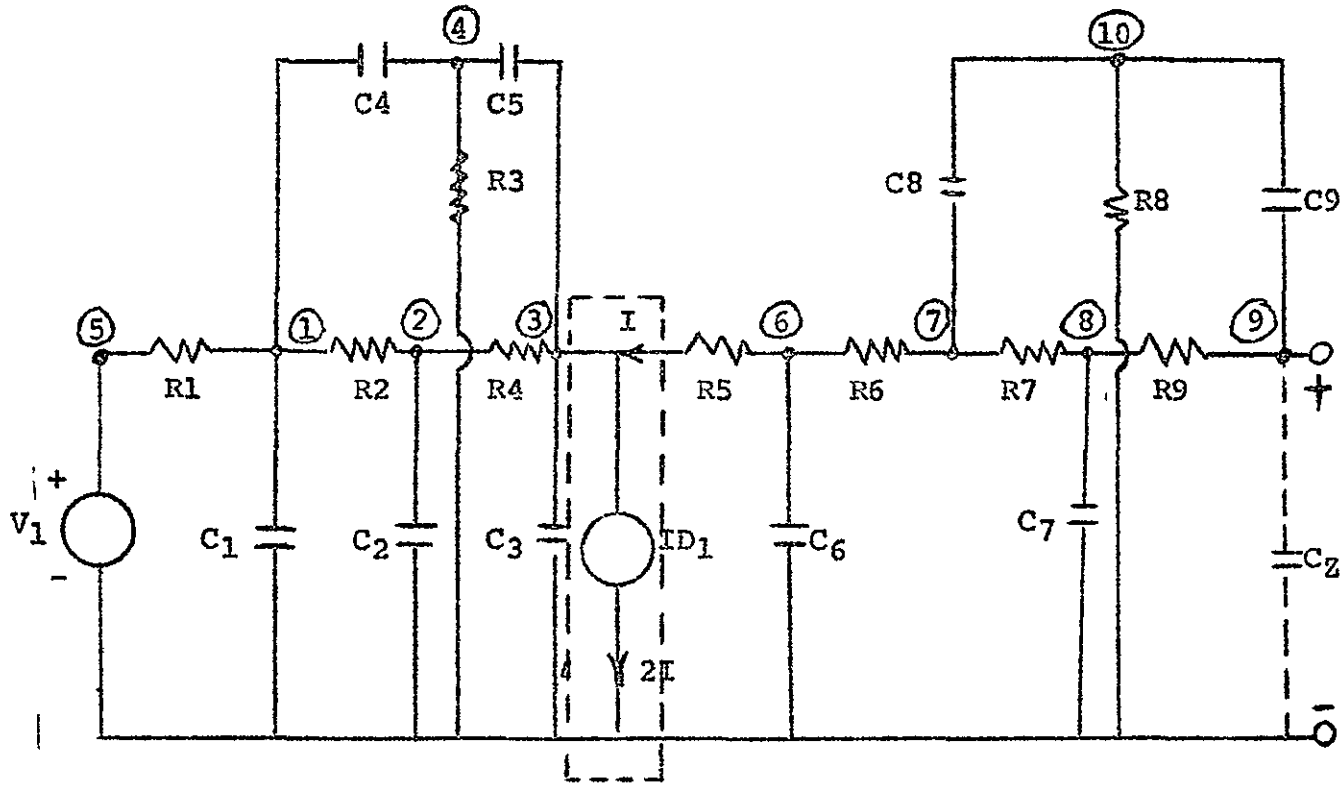


Fig. 4 Active RC Network of Antreich and Gleissner

Before exercising this option the above sequence numbers should be verified by obtaining a listing of the program. (The CUTOUT option may be a feature peculiar only to the Langley computer; if so, other methods of altering USEFCN needs be employed.)

The first card appearing below is the user's title card:

```
ANTREICH AND GLEISSNER - SCHUESSLER PULSE FORMING NETWORK
*ELEMENTS
R1                    5   1        1.0
R2                    1   2        3.118
R3                    4   0        3.121
R4                    2   3        2.86
R5                    3   6        0.9005
R6                    6   7        3.127
R7                    7   8        3.257
R8                   10   0        0.6412
R9                    8   9       11.21
C1                    1   0        2.211
C2                    2   0        0.749
C3                    3   0        9.809E-2
C4                    4   1        0.1713
C5                    4   3        0.1867
C6                    6   0        0.459
C7                    8   0        0.196
C8                   10   7        0.5972
C9                   10   9        0.1735
CZ                    9   0        0.0
V1                    5   0
ID1                   3   0       -2.0 IR5
*OUTPUTS
VCZ
*GEAR
*SOURCE ORDERING
V1
*RUN CONTROLS
STOP TIME = 20.0
OUTPUT DENSITY = 10
*END
```

Since the circuit is not stiff, this analysis could also be more efficiently achieved in the Gear mode by use of Adam's integration techniques. In this case the following card must be included in the RUN CONTROLS card group:

ADAMS INTEGRATION

Other cards controlling the integration step size and output data might also be prepared.

6.2 MATRIX MODE ANALYSIS; SOLUTION EQUATIONS PRINTED

The analysis of the sinusoidal driven pulse forming circuit by matrix mode routines may be achieved by using the same title card and elements cards as in section 4.1, with the remainder of the user's input control cards replaced by the following:

```
*OUTPUTS
 VCZ
*MATRIX, SO
*RUN CONTROLS
 STOP TIME = 20
 PLOT INCREMENT = 0.5
*SOURCE DEFINITIONS
 V1 = SIN (5.0*T)
*END
```

In this instance the closed form solution for VCZ as a function of time is also obtained.

6.3 CORNAP MODE ANALYSIS; SAMPLED DATA INPUT

A CORNAP mode analysis of the pulse forming network with a sinusoidal driver requires the same elements cards as in section 4.1; the remainder of these cards would be replaced by the following:

```
*OUTPUTS
 VCZ
```

*CORNAP, STATE EQNS, TRANSFER FCNS

Control Card (See below for contents)

DATA CARDS

*END

The contents of the nonblank columns of the control card might be:

Columns	Contents
1	T
3-4	V1
10-12	100
28-31	0.10
33-35	VCZ
41	X
58-61	0.01

The data cards contain, 6 samples per card in (perhaps) F 12.4 format, values of sin 5 t on the interval zero to ten seconds, at increments of 0.01 seconds. A smaller increment could be employed, in the interests of accuracy of the numerical integration. A chief encumbrance of this mode of analysis is the preparation of numerous sampled data cards necessary for an accurate numerical integration. The options exercised on the mode card effect printing of the state equations, transfer functions, poles and zeroes of the network.

6.4 SOME PROGRAM RESULTS

In Figure 5 we exhibit for the pulse forming circuit with sinusoidal driving function the voltage VCZ as a function of time, as obtained by execution of the STICAP program in the various modes, using the control cards of Sections 4.1, 4.2, 4.3. Figures 6 and 7 contain the corresponding results for the step and impulse responses of the pulse forming network. Output from the three modes appears

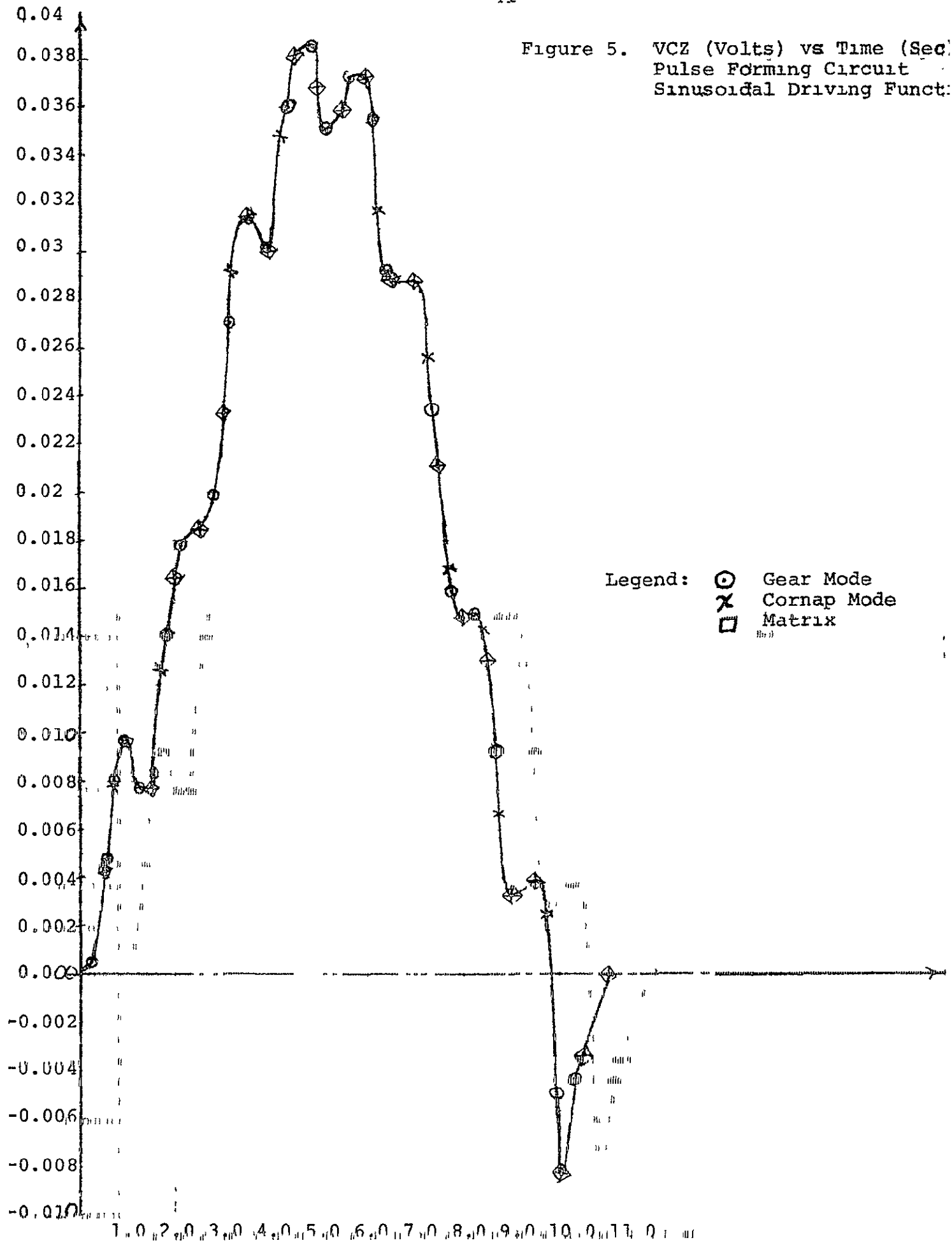


Figure 5. VCZ (Volts) vs Time (Sec)
Pulse Forming Circuit
Sinusoidal Driving Funct:

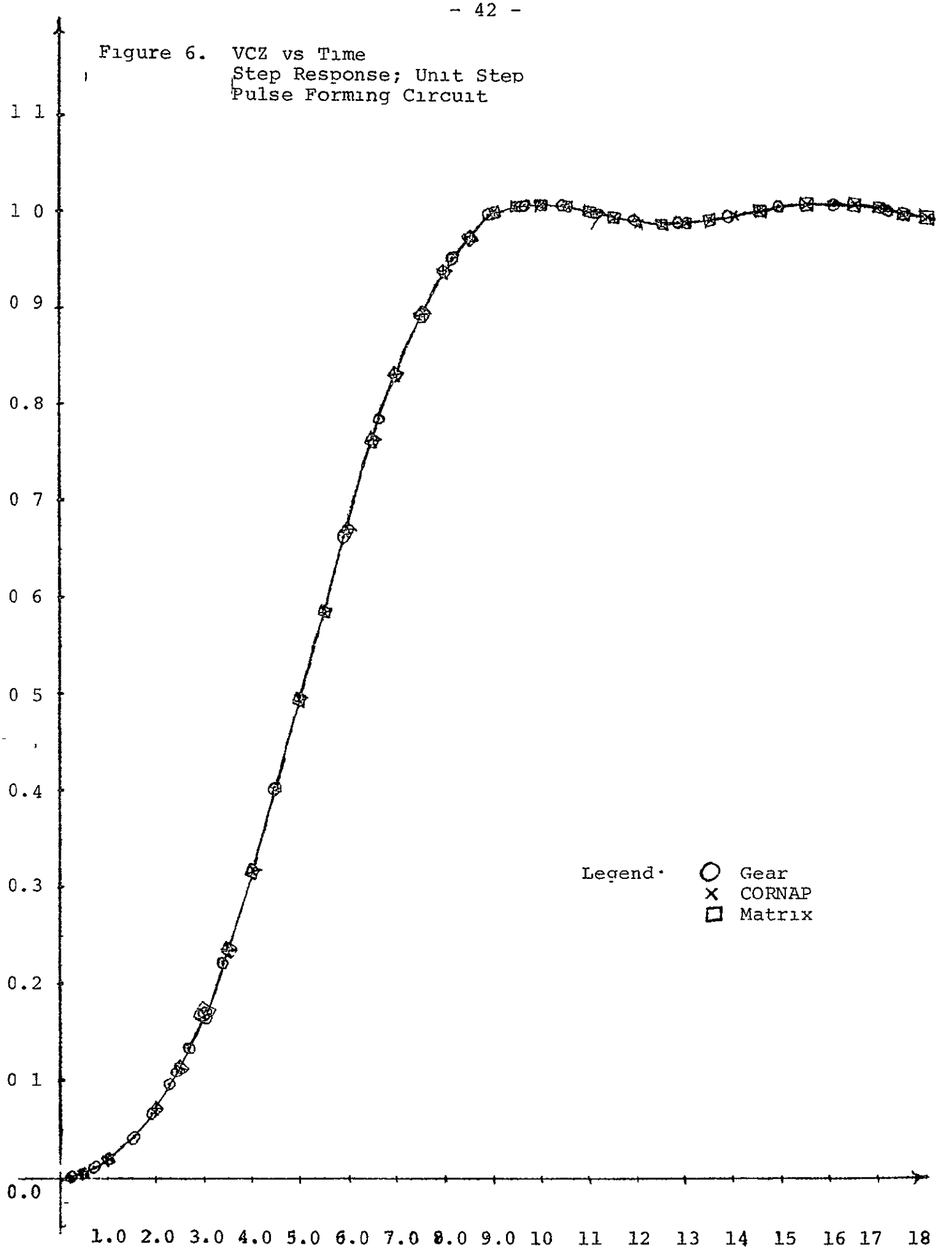
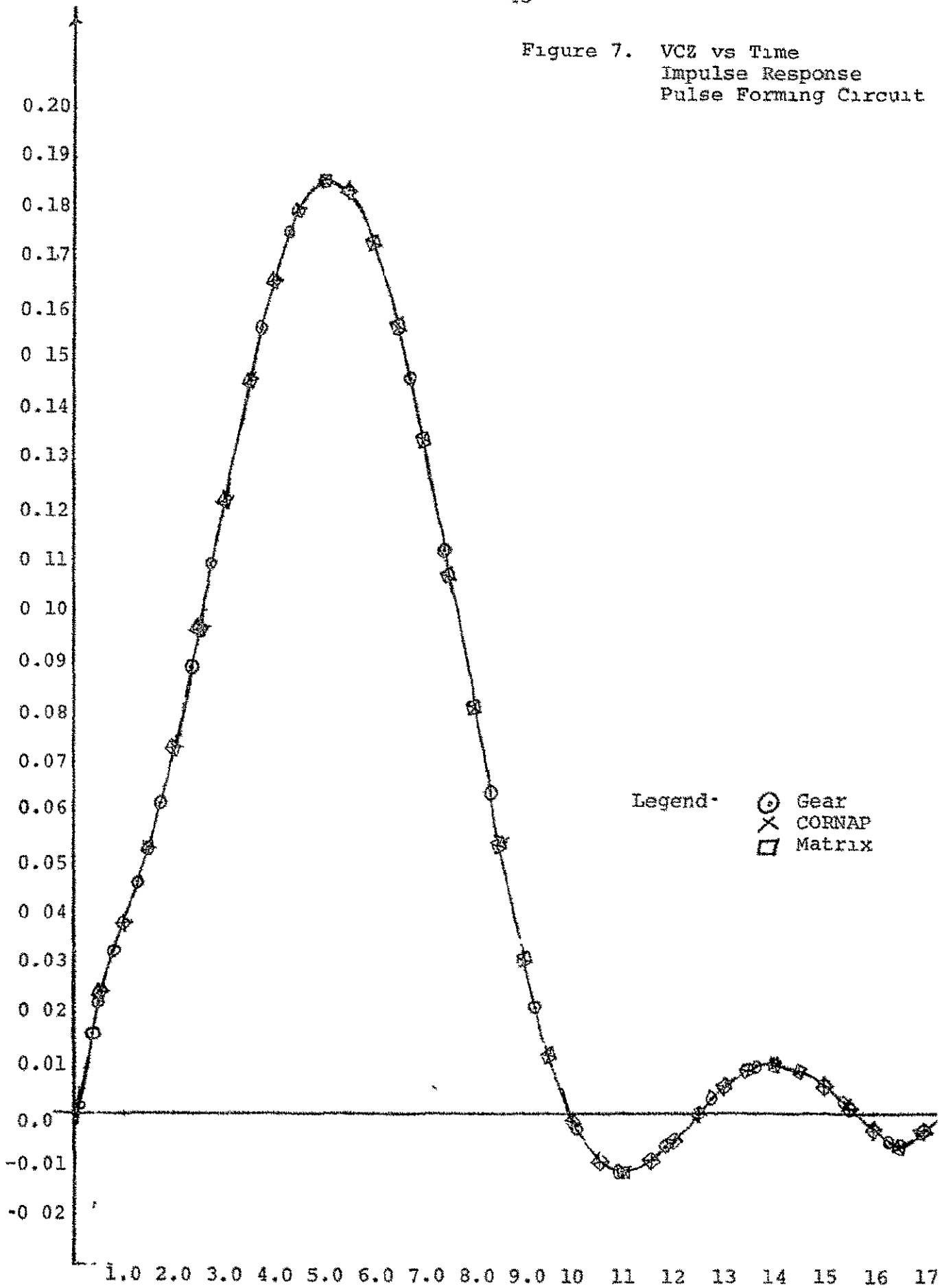


Figure 6. VCZ vs Time
Step Response; Unit Step
Pulse Forming Circuit

Figure 7. VCZ vs Time
Impulse Response
Pulse Forming Circuit



to be mutually consistent. However, at values of time for which the output voltage is nearly zero, the matrix mode printed results do not appear to have as many significant figures of accuracy as do the Gear mode results, suggesting loss of significant digits in this computational mode. The problem has not been thoroughly investigated to determine its significance.

6.5 A STIFF CIRCUIT

A stiff circuit which has caused problems in the first generation version of SCEPTRE[6] is exhibited in Figure 8. The node numbering indicated agrees with that used in preparing the control cards below. The system matrix for this network has the eigenvalues (poles of the system) $-.5 \pm 100i$, $-\frac{1}{10}$, -10.

The elements card group and some possible outputs for the network are:

```
* ELEMENTS

RS    1   2   1.0
R1    2   3   1.0
R2    2   5   1.0E + 4
C1    3   4   1.0E - 4
C2    5   6   1.0E - 2
L1    4   0   1.0
L2    6   0  10.0
V1    1   0

* OUTPUTS

VC1
VC2
IL1
IL2
```

[6] C. H. Cooke and E. Young, "Numerical Integration and Other Techniques for Computer Aided Network Design Programming," NASA CR-111837, January, 1971.

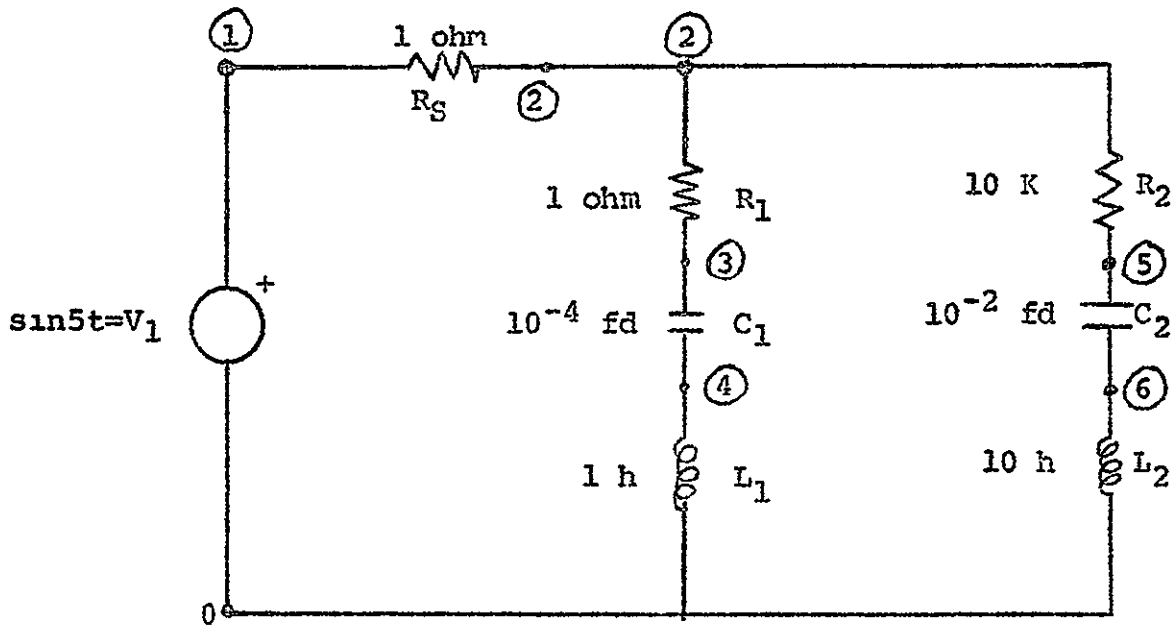


Figure 8. Typical Stiff Circuit

The Gear and Matrix modes were used to obtain time response for this stiff circuit, with the sinusoidal independent source

$$V1 = \sin 5\ t.$$

Plots of the output voltage across capacitor C1, VC1 versus time, appear in Figure 9.

In Figure 9(b) the data is plotted on a more microscopic scale, utilizing more data points, to illustrate the parasitic high frequency effects. These effects are most readily discernable in the first 0.5 seconds of time response. When such high frequency effects are of interest, many data points need be plotted, and the Gear integration routine should be restricted with a stepsize HMAX small enough to give an output data density sufficient for discernment of such effects. Whether or not a circuit is stiff may be detected by examining the poles of the network (eigenvalues of the system matrix), obtainable by use of the transfer functions option, available in all modes. Large magnitude left halfplane poles indicate a stiff circuit.

6.6 A CIRCUIT WITH SOURCE DERIVATIVES

A circuit characterized by source derivatives in the state equations (due to a loop containing only inductors and capacitors) appears in Figure 10. The elements cards and possible output cards are:

```
* ELEMENTS

L1    1   2   1.0
C1    1   2   1.0
C2    2   0   3.0
V1    1   0
```

Figure 9. VC1 (Volts) vs Time (Sec)
Stiff Circuit
Sinusoidal Driving Function

Legend: ⊙ Gear
× Matrix

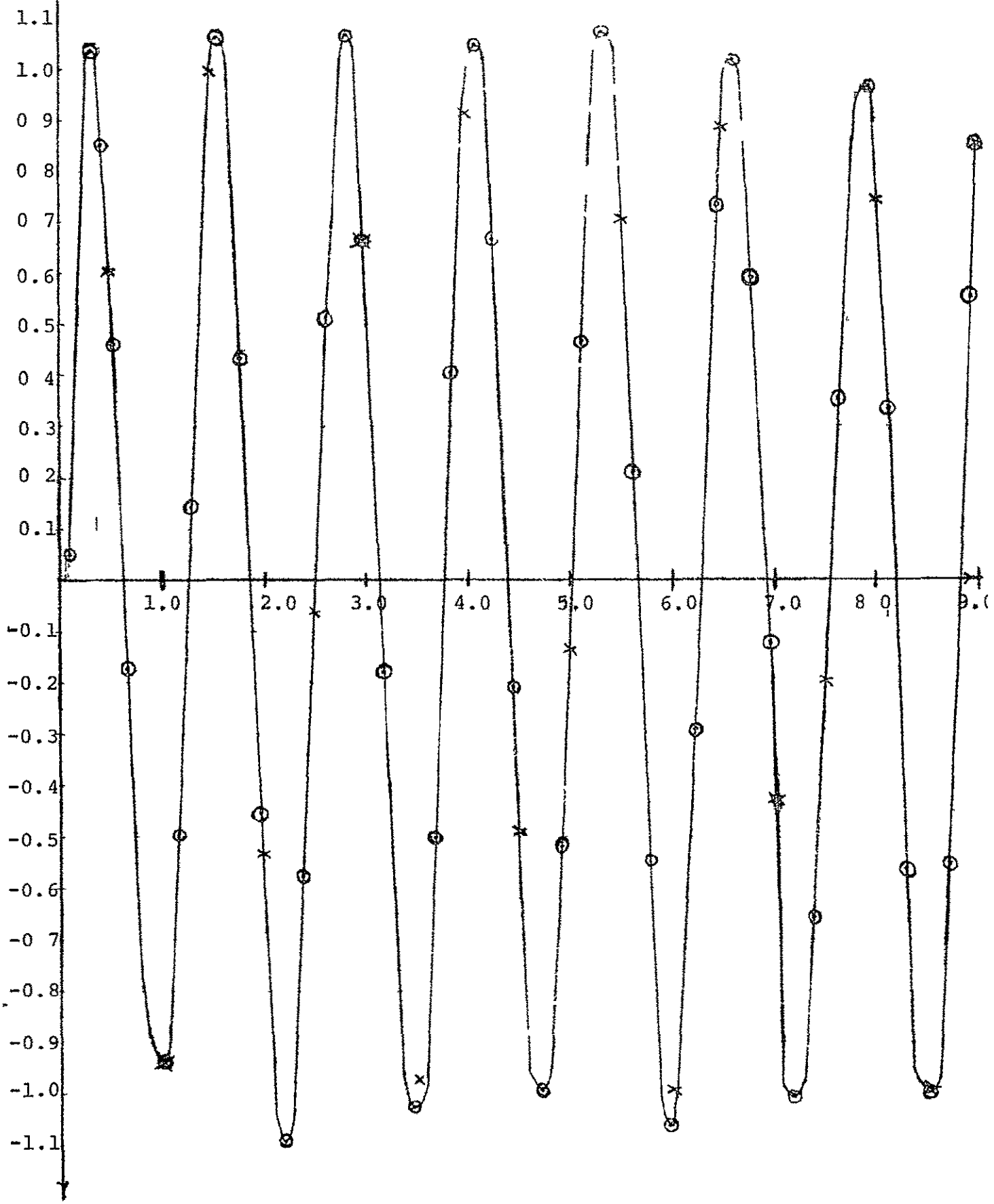
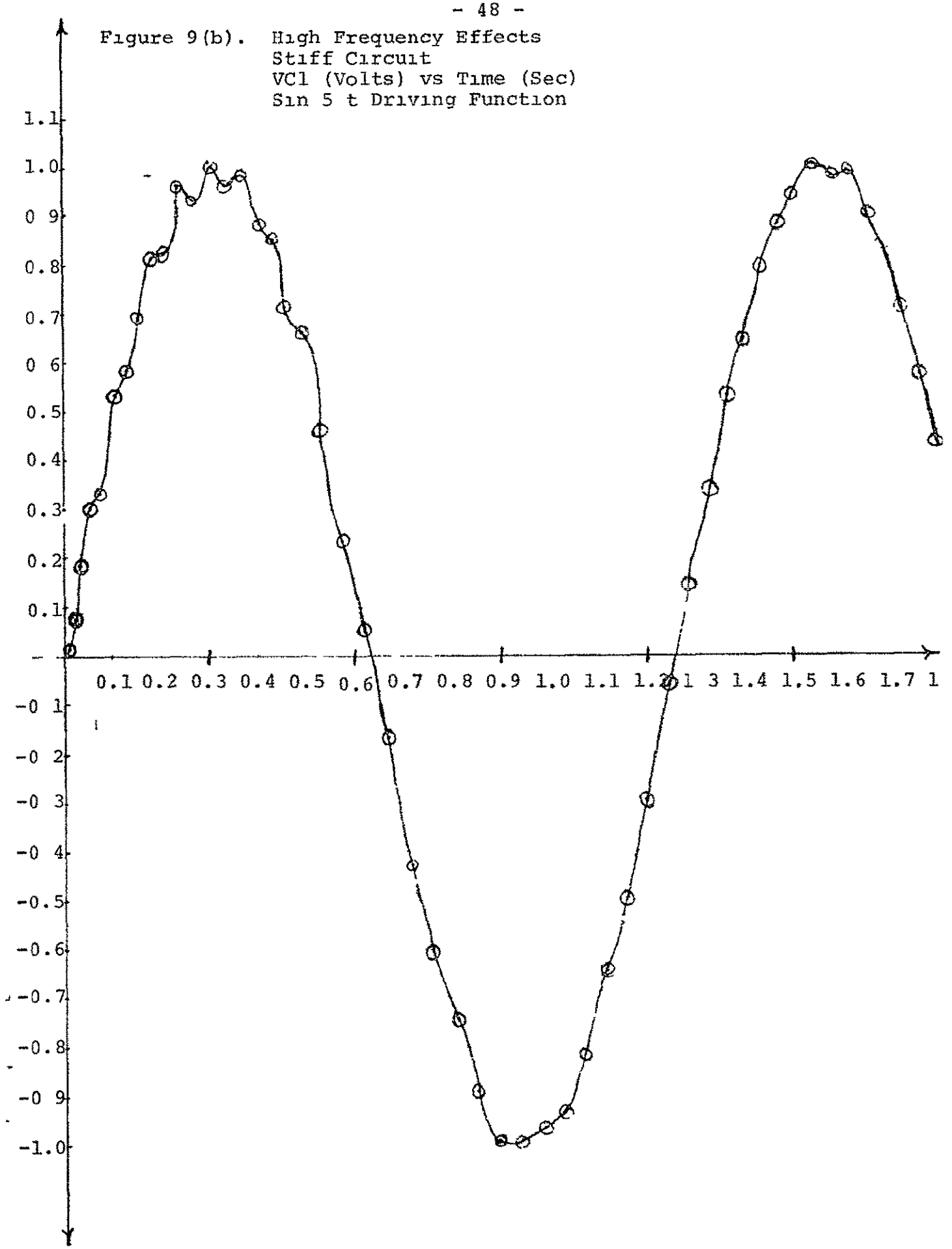
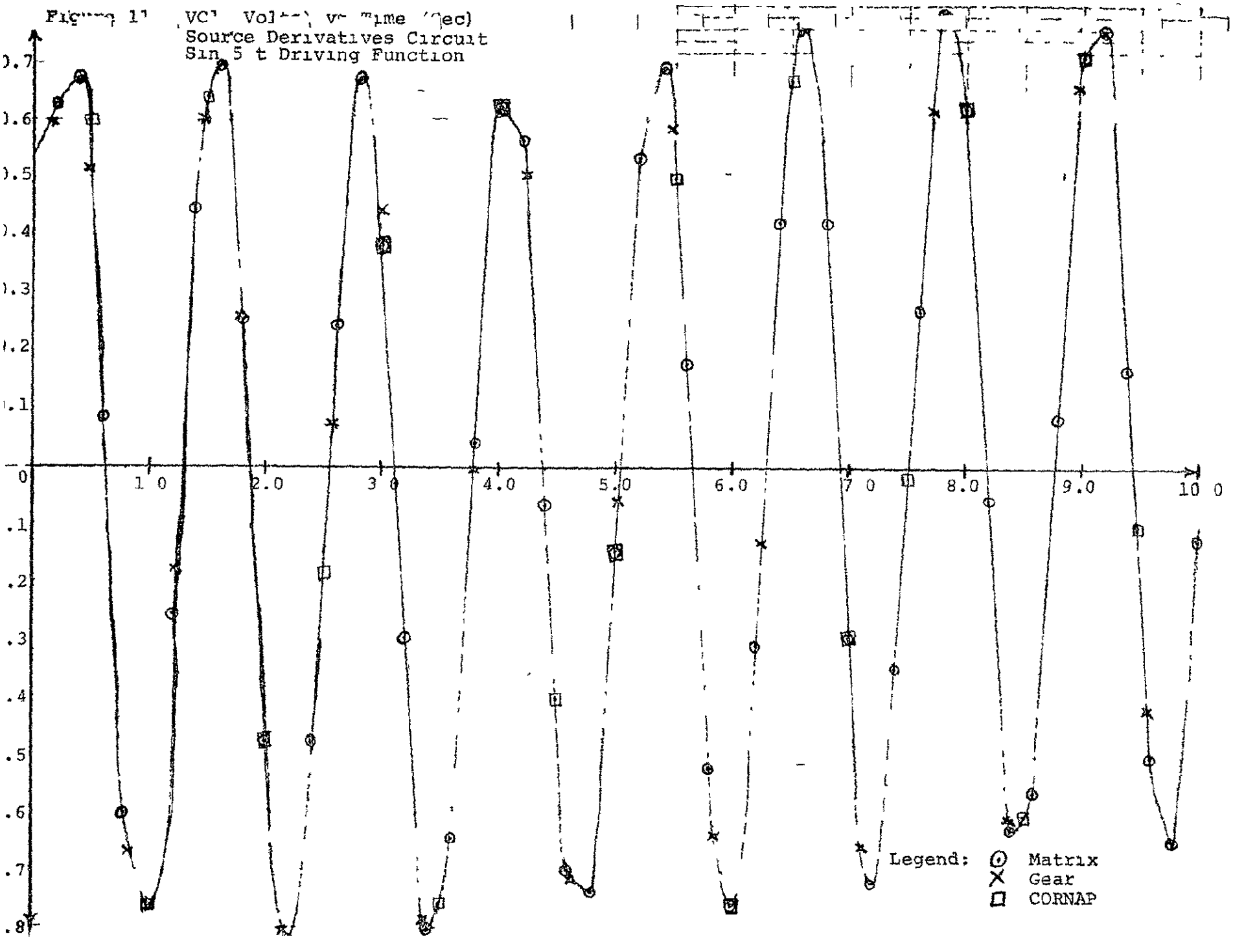


Figure 9(b). High Frequency Effects
Stiff Circuit
VC1 (Volts) vs Time (Sec)
Sin 5 t Driving Function




Source Derivatives Circuit
Sin 5 t Driving Function
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
9.0
10.0
.1
.2
.3
.4
.5
.6
.7
.8
Legend:
Matrix
Gear
CORNAP

```
* OUTPUTS

  VC1
  VC2
  IL1
```

Figure 11 depicts the output voltage VC1 resulting from the source V1 = sin 5 t.

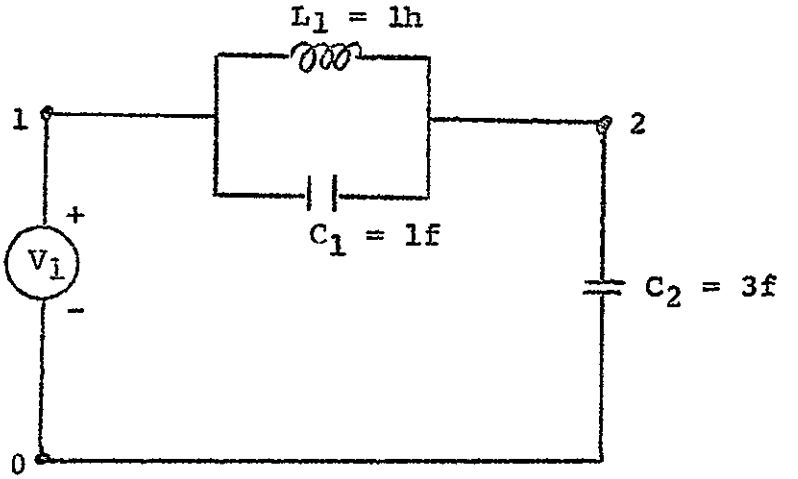


Figure 10. A Circuit Characterized by Source Derivatives in the Circuit Equations

6.7 OUTPUT LISTINGS

This section contains a program output listing for the pulse forming circuit previously discussed. The listing illustrates the manner in which the matrices of the state equations and state output equations, transfer functions, gain constants, zeroes and poles of the network are printed. This listing was obtained using the CORNAP

mode with the sinusoidal driving function sin 5 t. The page containing the comment

** The name VCZ does not appear on the output list **

is the result of misusing the CORNAP program. In specifying the program output, the voltage through CZ, the name VCZ was placed in columns 33-35 of the CORNAP control card (see page 40). However, these card columns should have contained the name CZ, the same name as was used in specifying this capacitor in the elements description, without the V appended when specifying the outputs by the outputs description card group.

```
ANTREICH AND GLEISSNER - SCHUESSLER PULSE FORMING NETWORK -64.10.10.S

ELEMENTS
 R1    5 1     1.0
 R2    1 2     3.118
 R3    4 0    3.121
 R4    2 3    2.86
 R5   3 6    0.9005
 R6   6 7    3.127
 R7   7 8    3.257
 R8   10 0    0.6412
 R9   8 9    11.21
 C1   1 0    2.211
 C2   2 0    0.749
 C3   3 0    9.809E-2
 C4   4 1    0.1713
 C5   4 3    0.1867
 C6   6 0    0.459
 C7   8 0    0.196
 C8   10 7    0.5972
 C9   10 9    0.1735
 CZ   9 0     0.0
 V1   5 0
 ID1   3 0    -2.0   IR5

OUTPUTS
 VCZ

THIS NETWORK HAS BEEN SCALED FOR COMPUTATION BY THE FOLLOWING FACTORS

 FREQUENCY 1.0000000E+00 RADIANS/SEC.     IMPEDANCE 1.0000000E+00 OHMS
```

ANTREICH AND GLEISSNER - SCHUESSLER PULSE FORMING NETWORK -64.10.10.S

THE (SCALED) ENTRIES OF THE A MATRIX ARE

STATE VARIABLES — STATE VARIABLES

	C1	C2	C3	C4
C1	-6.8815175E-01	2.1586769E-01	1.6062439E-01	-1.0318169E-01
C2	4.2819547E-01	-8.9501837E-01	4.6682290E-01	0.
C3	-1.2195434E+00	1.9684460E+00	4.1360312E+00	-9.4072197E-01
C4	-1.1721256E+00	9.1398415E-01	2.0732080E+00	-1.3317846E+00
C6	0.	0.	2.4193773E+00	0.
C7	0.	0.	0.	0.
C8	0.	0.	0.	0.
C9	0.	0.	0.	0.

	C6	C7	C8	C9
C1	-2.3444029E-01	0.	0.	0.
C2	0.	0.	0.	0.
C3	-6.0367692E+00	0.	0.	0.
C4	-3.0259631E+00	0.	0.	0.
C6	-3.0181875E+00	1.2131571E-01	-5.0480674E-01	2.7312178E-02
C7	2.8410159E-01	-1.6696064E+00	-1.0096212E+00	-3.7588360E-01
C8	-3.8758776E-01	-3.3135552E-01	-7.6048937E-01	4.1145689E-02
C9	7.2255271E-02	-4.2462931E-01	1.4162654E-01	-4.9400058E-01

THE (SCALED) ENTRIES OF THE B MATRIX ARE

STATE VARIABLES — SOURCE VARIABLES

	V1
C1	4.4291808E-01
C2	0.
C3	2.1111348E-01
C4	-1.2088804E-01
C6	0.
C7	0.
C8	0.
C9	0.

THE (SCALED) ENTRIES OF THE C MATRIX ARE

OUTPUT VARIABLES	STATE VARIABLES			
	C1	C2	C3	C4
V CZ	0.	0.	0.	0.
	C6	C7	C8	C9
V CZ	1.4053181E-01	1.7412359E-01	2.7545442E-01	-9.6079902E-01

THE (SCALED) ENTRIES OF THE D MATRIX ARE

OUTPUT VARIABLES	SOURCE VARIABLES
	V1
V CZ	0.

ANTREICH AND GLEISSNER - SCHUESSLER PULSE FORMING NETWORK -64.10.10.S

TRANSFER FUNCTION CRITICAL FREQUENCIES (SCALED)

OUTPUT VARIABLE - V CZ
SOURCE VARIABLE - V1

GAIN CONSTANT IS 7.1778470E-02

POLE POSITIONS			ZERO POSITIONS		
REAL PART	IMAGINARY PART	ORDER	REAL PART	IMAGINARY PART	ORDE
-4.4859094E-02	9.1549708E-01	1	-6.0964382E-06	1.2945752E+00	1
-3.6668814E-01	6.2457201E-01	1	-8.9500618E-01	0.	1
-8.9500618E-01	0.	1	-2.0220162E+00	0.	1
-2.0220161E+00	0.	1	1.9922384E-04	1.0199093E+00	1
-4.9054538E-01	2.0810336E-01	1			

THE NAME VCZ DOES NOT APPEAR ON THE OUTPUT LIST

(An Apparently Non-Fatal program Bug)

ANTREICH AND GLEISSNER - SCHUESSLER PULSE FORMING NETWORK -64.10.10.S

TRANSFER FUNCTION CRITICAL FREQUENCIES (SCALED)

OUTPUT VARIABLE - V CZ
SOURCE VARIABLE - V1

GAIN CONSTANT IS 7.177847CE-02

POLE POSITIONS			ZERO POSITIONS		
REAL PART	IMAGINARY PART	ORDER	REAL PART	IMAGINARY PART	ORI
-4.4659094E-02	9.1549708E-01	1	-6.0964382E-06	1.2945752E+00	
-3.6668814E-01	6.2457201E-01	1	-8.9500618E-01	0.	
-8.9500618E-01	0.	1	-2.0220162E+00	0.	
-2.0220161E+00	0.	1	1.9922384E-04	1.0199093E+00	
-4.9054538E-01	2.0810336E-01	1			

THIS NETWORK HAS BEEN SCALED FOR COMPUTATION BY THE FOLLOWING FACTORS
FREQUENCY 1.0000000E+00 RADIANS/SEC. IMPEDANCE 1.000000E+00 OHMS

UNSCALED TIME RESPONSE

INTEGRATION STEP SIZE 2.0000E-02 SEC
EXTERNAL INPUT SIGNAL SAMPLING INTERVAL 1.0000E-02 SEC

TIME	INPUT	OUTPUT (VCZ)
0.	0.	0.
1.0000E-01	4.7943E-01	5.6497E-05
2.0000E-01	8.4147E-01	4.1650E-04
3.0000E-01	9.9749E-01	1.2624E-03
4.0000E-01	9.0930E-01	2.6154E-03
5.0000E-01	5.9847E-01	4.3358E-03
6.0000E-01	1.4112E-01	6.1835E-03
7.0000E-01	-3.5078E-01	7.8467E-03
8.0000E-01	-7.5680E-01	9.0615E-03
9.0000E-01	-9.7753E-01	9.6622E-03
1.0000E+00	-9.5892E-01	9.6300E-03
1.1000E+00	-7.0554E-01	9.1015E-03
1.2000E+00	-2.7942E-01	8.3379E-03
1.3000E+00	2.1512E-01	7.6633E-03
1.4000E+00	6.5659E-01	7.3873E-03
1.5000E+00	9.3800E-01	7.7301E-03
1.6000E+00	9.8936E-01	8.7703E-03
1.7000E+00	7.9849E-01	1.0425E-02
1.8000E+00	4.1212E-01	1.2472E-02
1.9000E+00	-7.5151E-02	1.4601E-02

2.0000E+00	-5.4402E-01	1.6494E-02
2.1000E+00	-8.7970E-01	1.7898E-02
2.2000E+00	-9.9999E-01	1.8690E-02
2.3000E+00	-8.7545E-01	1.8902E-02
2.4000E+00	-5.3657E-01	1.8716E-02
2.5000E+00	-6.6322E-02	1.8419E-02
2.6000E+00	4.2017E-01	1.8326E-02
2.7000E+00	8.0378E-01	1.8709E-02
2.8000E+00	9.9061E-01	1.9723E-02
2.9000E+00	9.3490E-01	2.1371E-02
3.0000E+00	6.5029E-01	2.3500E-02
3.1000E+00	2.0647E-01	2.5837E-02
3.2000E+00	-2.8790E-01	2.8057E-02
3.3000E+00	-7.1179E-01	2.9859E-02
3.4000E+00	-9.6140E-01	3.1039E-02
3.5000E+00	-9.7563E-01	3.1539E-02
3.6000E+00	-7.5099E-01	3.1461E-02
3.7000E+00	-3.4248E-01	3.1040E-02
3.8000E+00	1.4988E-01	3.0586E-02
3.9000E+00	6.0554E-01	3.0407E-02
4.0000E+00	9.1295E-01	3.0732E-02
4.1000E+00	9.9683E-01	3.1656E-02
4.2000E+00	8.3666E-01	3.3115E-02
4.3000E+00	4.7164E-01	3.4899E-02
4.4000E+00	-8.8513E-03	3.6708E-02
4.5000E+00	-4.8717E-01	3.8219E-02
4.6000E+00	-8.4622E-01	3.9168E-02
4.7000E+00	-9.9808E-01	3.9414E-02
4.8000E+00	-9.0558E-01	3.8973E-02
4.9000E+00	-5.9136E-01	3.8013E-02
5.0000E+00	-1.3235E-01	3.6812E-02
5.1000E+00	3.5906E-01	3.5694E-02
5.2000E+00	7.6256E-01	3.4944E-02
5.3000E+00	9.7936E-01	3.4741E-02
5.4000E+00	9.5638E-01	3.5115E-02
5.5000E+00	6.9924E-01	3.5938E-02
5.6000E+00	2.7091E-01	3.6957E-02
5.7000E+00	-2.2376E-01	3.7854E-02
5.8000E+00	-6.6363E-01	3.8326E-02
5.9000E+00	-9.4103E-01	3.8159E-02
6.0000E+00	-9.6803E-01	3.7282E-02
6.1000E+00	-7.9313E-01	3.5781E-02
6.2000E+00	-4.0404E-01	3.3882E-02
6.3000E+00	8.3974E-02	3.1896E-02
6.4000E+00	5.5143E-01	3.0141E-02
6.5000E+00	8.8387E-01	2.8867E-02
6.6000E+00	9.9991E-01	2.8195E-02
6.7000E+00	8.7114E-01	2.8086E-02
6.8000E+00	5.2908E-01	2.8356E-02
6.9000E+00	5.7487E-02	2.8716E-02
7.0000E+00	-4.2818E-01	2.8846E-02

7.1000E+00	-8.0902E-01	2.8478E-02
7.2000E+00	-9.9178E-01	2.7455E-02
7.3000E+00	-9.3172E-01	2.5777E-02
7.4000E+00	-6.4354E-01	2.3597E-02
7.5000E+00	-1.9780E-01	2.1187E-02
7.6000E+00	2.9637E-01	1.8874E-02
7.7000E+00	7.1797E-01	1.6955E-02
7.8000E+00	9.6380E-01	1.5632E-02
7.9000E+00	9.7365E-01	1.4958E-02
8.0000E+00	7.4511E-01	1.4829E-02
8.1000E+00	3.3415E-01	1.5007E-02
8.2000E+00	-1.5862E-01	1.5182E-02
8.3000E+00	-6.1256E-01	1.5047E-02
8.4000E+00	-9.1652E-01	1.4375E-02
8.5000E+00	-9.9609E-01	1.3073E-02
8.6000E+00	-8.3177E-01	1.1209E-02
8.7000E+00	-4.6382E-01	8.9960E-03
8.8000E+00	1.7702E-02	6.7360E-03
8.9000E+00	4.9489E-01	4.7517E-03
9.0000E+00	8.5090E-01	3.3060E-03
9.1000E+00	9.9859E-01	2.5385E-03
9.2000E+00	9.0179E-01	2.4318E-03
9.3000E+00	5.8420E-01	2.8164E-03
9.4000E+00	1.2357E-01	3.4125E-03
9.5000E+00	-3.6731E-01	3.8991E-03
9.6000E+00	-7.6825E-01	3.9925E-03
9.7000E+00	-9.8111E-01	3.5167E-03
9.8000E+00	-9.5375E-01	2.4458E-03
9.9000E+00	-6.9288E-01	9.1146E-04
1.0000E+01	-2.6237E-01	-8.3001E-04

The next listing depicts Gear mode output for the pulse forming circuit when step response is requested. Observe that the input run controls cards used are listed as part of the output; as well as the elements and outputs card groups:

ANTREICH AND GLEISSNER - SCHUESSLER PULSE FORMING NETWORK - 64.10.10.S

ELEMENTS

R1	5	1	1.0
R2	1	2	3.118
R3	4	0	3.121
R4	2	3	2.86
R5	3	6	0.9005
R6	6	7	3.127
R7	7	8	3.257
R8	10	0	0.6412
R9	8	9	11.21
C1	1	0	2.211
C2	2	0	0.749
C3	3	0	9.809E-2
C4	4	1	0.1713
C5	4	3	0.1867
C6	6	0	0.459
C7	8	0	0.196
C8	10	7	0.5972
C9	10	9	0.1735
CZ	9	0	0.0
V1	5	0	
ID1	3	0	-2.0 IR5

OUTPUTS

VC7

THIS NETWORK HAS BEEN SCALED FOR COMPUTATION BY THE FOLLOWING FACTORS

FREQUENCY 1.0000000E+00 RADIANS/SEC. IMPEDANCE 1.0000000E+00 OHMS

ANTREICH AND GLEISSNER - SCHUESSLER PULSE FORMING NETWORK - 64.10.10.S

THE (SCALED) ENTRIES OF THE A MATRIX ARE

STATE VARIABLES — STATE VARIABLES

	C1	C2	C3	C4
C1	-6.8815175E-01	2.1586789E-01	1.6062439E-01	-1.0318169E-01
C2	4.2819547E-01	-8.9501837E-01	4.6682290E-01	0.
C3	-1.2195434E+00	1.9684460E+00	4.1360312E+00	-9.4072197E-01
C4	-1.1721256E+00	9.1398415E-01	2.0732080E+00	-1.3317846E+00
C6	0.	0.	2.4193773E+00	0.
C7	0.	0.	0.	0.
C8	0.	0.	0.	0.
C9	0.	0.	0.	0.

	C6	C7	C8	C9
C1	-2.3444029E-01	0.	0.	0.
C2	0.	0.	0.	0.
C3	-6.0367692E+00	0.	0.	0.
C4	-3.0259631E+00	0.	0.	0.
C6	-3.0181875E+00	1.2131571E-01	-5.0480674E-01	2.7312178E-02
C7	2.8410159E-01	-1.6696064E+00	-1.0096212E+00	-3.7588360E-01
C8	-3.8798776E-01	-3.3135592E-01	-7.6048937E-01	4.1145689E-02
C9	7.2255271E-02	-4.2462931E-01	1.4162654E-01	-4.9400058E-01

THE (SCALED) ENTRIES OF THE B MATRIX ARE

STATE VARIABLES — SOURCE VARIABLES

	V1
C1	4.4291808E-01
C2	0.
C3	2.1111348E-01
C4	-1.2088804E-01
C6	0.
C7	0.
C8	0.
C9	0.

THE (SCALED) ENTRIES OF THE C MATRIX ARE

OUTPUT VARIABLES	STATE VARIABLES			
	C1	C2	C3	C4
V CZ	0.	0.	0.	0.
	C6	C7	C8	C9
V CZ	1.4053181E-01	1.7412359E-01	2.7545442E-01	-9.6079902E-01

THE (SCALED) ENTRIES OF THE D MATRIX ARE

OUTPUT VARIABLES	SOURCE VARIABLES
	V1
V CZ	0.

ANTREICH AND GLEISSNER - SCHUESSLER PULSE FORMING NETWORK - 64.10.10.S

TRANSFER FUNCTION CRITICAL FREQUENCIES (SCALED)

OUTPUT VARIABLE - V CZ
SOURCE VARIABLE - V1

GAIN CONSTANT IS 7.1778470E-02

POLE POSITIONS			ZERO POSITIONS		
REAL PART	IMAGINARY PART	ORDER	REAL PART	IMAGINARY PART	ORDE
-4.4859094E-02	9.1549708E-01	1	-6.0964382E-06	1.2945752E+00	1
-3.6668814E-01	6.2457201E-01	1	-8.9500618E-01	0.	1
-8.9500618E-01	0.	1	-2.0220162E+00	0.	1
-2.0220161E+00	0.	1	1.9922384E-04	1.0199093E+00	1
-4.9054538E-01	2.0810336E-01	1			

```
RUN CONTROLS
    EPS =  1.00000E-04
    PRINT DENSITY =    3
    INITIAL TIME =  0.
    PRINT STARTING TIME =  0.
    HINIT =  1.00000E-04
    HMIN =  0.
    STIFF INTEGRATION
    HMAX =  2.00000E+00
    STOP TIME =  2.00000E+01
    STEP RESPONSE
```

ANTREICH AND GLEISSNER - SCHUESSLER PULSE FORMING NETWORK - 64.10.

TIME	VCZ
0.	0.
1.16104E-02	4.77371E-06
5.29586E-02	9.73736E-05
1.08541E-01	3.96535E-04
1.63856E-01	8.75283E-04
2.01737E-01	1.30866E-03
2.32724E-01	1.70884E-03
2.94326E-01	2.63862E-03
3.71274E-01	4.02903E-03
4.39755E-01	5.45897E-03
5.21930E-01	7.39103E-03
6.07320E-01	9.62659E-03
6.97008E-01	1.22051E-02
7.90698E-01	1.51354E-02
8.91607E-01	1.85520E-02
1.00403E+00	2.26723E-02
1.12576E+00	2.75131E-02
1.25278E+00	3.30028E-02
1.38207E+00	3.90803E-02
1.51220E+00	4.57345E-02
1.64242E+00	5.29751E-02
1.77235E+00	6.08256E-02
1.90175E+00	6.93096E-02
2.03054E+00	7.84550E-02
2.15877E+00	8.82939E-02
2.28659E+00	9.88619E-02
2.41874E+00	1.10616E-01
2.67497E+00	1.35886E-01
2.98950E+00	1.71482E-01
3.38514E+00	2.23322E-01
3.88472E+00	2.99058E-01
4.49258E+00	4.03297E-01
5.15459E+00	5.25062E-01
5.90588E+00	6.62236E-01
6.65718E+00	7.85670E-01
7.40847E+00	8.84920E-01
8.15977E+00	9.54262E-01
8.91106E+00	9.93620E-01
9.66236E+00	1.00816E+00
1.04137E+01	1.00656E+00

ANTREICH AND GLEISSNER - SCHUESSLER PULSE FORMING NETWORK - 64.10.10.S

TIME	VCZ
1.11650E+01	9.98394E-01
1.19850E+01	9.91100E-01
1.28393E+01	9.90609E-01
1.38611E+01	9.98443E-01
1.49667E+01	1.00782E+00
1.60722E+01	1.00871E+00
1.71777E+01	1.00088E+00
1.82832E+01	9.92583E-01
1.93887E+01	9.91795E-01
2.00000E+01	9.95055E-01

Solution Complete

```
08/17/71   LRC CM SCOPE 3.0  64COZ-131K 06/02/71C
15.08.16.TER1317.
15.08.17.JCB,1,3CC, 7000C.            A3031       R
15.08.17.HB105                     BLDG 12C2   CENT
15.08.17.USER.BAVUSO, SALVATORE J              0000
15.08.17.44430  15010
15.08.17.NCMAP.
15.08.17.FETCH(A3031,SPRZ01,BINARY)
15.08.23.TIME        BG ATTACH
15.09.09.TIME        EC ATTACH
15.09.28.END    FETCH
15.09.28.REWIND(CUTPUT)
15.09.30.BNFILE.
15.10.34.STOP
15.10.35.CPU     7.134427 SEC.
15.10.35.PPU   116.899840 SEC.
15.10.35.TL.   177 SEC.
15.10.35.DATE     08/17/71
16.07.15. TER1317.    215 LINES PRINTED. LP26
```

The next listing exhibits typical matrix mode output for the pulse forming circuit with the sin 5 t driver. Observe the form of the solution equation giving VCZ as a function of time. The notation

1.31040E-09EXP(-2.02202E + 00T) + ... etc.

is to be interpreted as

$$1.3104 \times 10^{-9}\ e^{-2.02202T},$$

where T is the time variable. The T appearing in sin and cosine arguments is also to be interpreted as the time variable, and not a portion of any floating point exponent which may precede it.

```
START OF OUTPUT FOR JOB NO. 1319.
ANTREICH AND GLEISSNER - SCHUESSLER PULSE FORMING NETWORK -64.10.10.
ELEMENTS
 R1   5 1    1.0
 R2   1 2    3.118
 R3   4 0    3.121
 R4   2 3    2.86
 R5   3 6    0.9005
 R6   6 7    3.127
 R7   7 8    3.257
 R8   10 0   0.6412
 R9   8 9    11.21
 C1   1 0    2.211
 C2   2 0    0.749
 C3   3 0    9.809E-2
 C4   4 1    0.1713
 C5   4 3    0.1867
 C6   6 0    0.453
 C7   8 0    0.196
 C8   10 7   0.5972
 C9   10 9   0.1735
 CZ   9 0    0.0
 V1   5 0
 TD1  3 0    -2.0  TR5
OUTPUTS
 VCZ
THIS NETWORK HAS BEEN SCALED FOR COMPUTATION BY THE FOLLOWING FACTOR

 FREQUENCY 1.000000E+00 RADIANS/SEC.    IMPEDANCE 1.000000E+00 OHM
ANTREICH AND GLEISSNER - SCHUESSLER PULSE FORMING NETWORK -64.10.10.
RUN CONTROLS
      INITIAL TIME =  0.
      PRINT STARTING TIME =  0.
      NUMBER OF POINTS PRINTED =    40
      PRINT INTERVAL =  5.000000E-01
      STOP TIME =  2.000000E+01
```

ORIGINAL PAGE IS
OF POOR QUALITY

ALL INITIAL CONDITIONS ZERO
SOURCE DEFINITIONS
V1
SINE FUNCTION MAGNITUDE 1.00000E+00 AND ANGULAL VELOCITY 5.000
ANTREICH AND GLEISSNER - SCHUESSLER PULSE FORMING NETWORK -64.10.10.S
THE FOLLOWING ARE THE CLOSED FORM SOLUTIONS

VC2 =

-2.06191E-03SIN(5.00000E+00T + 3.03285E-01)

+ 1.31040E-03EXP(-2.02902E+00T) -8.39908E-10EXP(-4.95006E-01T)

+ 4.37654E-01EXP(-4.90545E-01T)*SIN(2.08103E-01T + 6.19925E-02)
-1.26120E-01EXP(-3.06688E-01T)*SIN(6.24572E-01T + 2.44476E-01)
+ 4.36887E-03EXP(-4.48591E-02T)*SIN(9.15497E-01T + 1.50343E+00)

ANTREICH AND GLEISSNER - SCHUESSLER PULSE FORMING NETWORK -64.10.10.S

TIME	VC2
0.	2.03678E-16
5.00000E-01	-7.31303E-04
1.00000E+00	2.11766E-03
1.50000E+00	-2.06173E-03
2.00000E+00	2.14730E-03
2.50000E+00	-7.78797E-04
3.00000E+00	-3.39442E-04
3.50000E+00	2.21996E-03
4.00000E+00	-2.65757E-03
4.50000E+00	2.03823E-03
5.00000E+00	-6.08264E-04
5.50000E+00	-1.00302E-03
6.00000E+00	2.31243E-03
6.50000E+00	-2.64165E-03
7.00000E+00	1.32020E-03
7.50000E+00	-4.35053E-04
8.00000E+00	-1.72312E-03
8.50000E+00	2.39464E-03
9.00000E+00	-2.61410E-03
9.50000E+00	1.79370E-03
1.00000E+01	-2.53326E-04
1.05000E+01	-1.37723E-03
1.10000E+01	2.46664E-03
1.15000E+01	-2.57504E-03
1.20000E+01	1.65931E-03
1.25000E+01	-8.36545E-05
1.30000E+01	-1.52527E-03
1.35000E+01	2.52758E-03
1.40000E+01	-2.52463E-03
1.45000E+01	1.51761E-03
1.50000E+01	9.29641E-05
1.55000E+01	-1.66660E-03
1.60000E+01	2.57739E-03
1.65000E+01	-2.46311E-03

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1.70000E+01    1.36923E-03
1.75000E+01    2.69215E-04
1.80000E+01   -1.80059E-03
1.85000E+01    2.61585E-03
1.90000E+01   -2.39075E-03
1.95000E+01    1.21482E-03

10/26/71   LRC CDC SCOPE 3.0  6400Z-131K 09/01/71
15.10.44.TFR1319.
15.10.44.JOB,1,500, 70000.          A3031      R
15.10.44.HB105                   BLDG1202
15.10.44.USER.BAVUSO, SALVATORE J              0000
15.10.44.44430  15010
15.10.44.FETCH(A3031,SPRA05,SOURCE)
15.10.48.TIME        BG ATTACH
15.11.29.TIME        ED ATTACH
15.15.05.END    FETCH
15.15.06.BKSP,OUTPUT,2.
15.15.07.NOMAP.
15.15.07.RUN(S,,,SCFILE,DUM)
15.18.36.SETINDF.
15.18.37.LGO.
15.19.14.STOP
15.19.15.      0001085 O/S CALLS
15.19.15.CPU     94.899824 SEC.
15.19.15.PPU    142.544896 SEC.
15.19.15.TL.    237 SEC.
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APPENDIX I

CIRCUIT SCALING

Some basic concepts of the STICAP circuit scaling option will here be discussed. For further clarification one may consult Appendix C of the reference:

William D. Stanley, Transform Circuit Analysis for Engineering and Technology, Prentice-Hall, 1968.

The linearity of the circuits processable by STICAP allows the state-input and state-output equations to be algebraicly rearranged in the partitioned form:*

$$\frac{d}{dt}\begin{bmatrix} \bar{X}_v \\ \bar{X}_i \end{bmatrix} = \left[\begin{array}{c|c} A_1 & B_1 \\ \hline C_1 & D_1 \end{array}\right] \begin{bmatrix} \bar{X}_v \\ \bar{X}_i \end{bmatrix} + \left[\begin{array}{c|c} A_2 & B_2 \\ \hline C_2 & D_2 \end{array}\right] \begin{bmatrix} \bar{U}_v \\ \bar{U}_i \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} \bar{Y}_v \\ \bar{Y}_i \end{bmatrix} = \left[\begin{array}{c|c} A_3 & B_3 \\ \hline C_3 & D_3 \end{array}\right] \begin{bmatrix} \bar{X}_v \\ \bar{X}_i \end{bmatrix} + \left[\begin{array}{c|c} A_4 & B_4 \\ \hline C_4 & D_4 \end{array}\right] \begin{bmatrix} \bar{U}_v \\ \bar{U}_i \end{bmatrix} \quad (2)$$

Here the A, B, C, D subscripted quantities are constant matrices; and

$\bar{X}_{(\ )}$ is a time varying vector of state variables,

$\bar{U}_{(\ )}$ is a time varying vector of the independent voltage sources or current sources,

$\bar{Y}_{(\ )}$ is a time varying vector of user requested outputs.

Moreover, the "v' and "i" subscripts indicate respectively voltages and currents of the network.

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*For simplicity we consider only the case in which no source derivatives are present. This renegade circumstance may similarly be treated.

Frequency Scaling

User input of a frequency scaling factor

$$\text{FREQUENCY} = \omega, \ \omega \neq 1$$

effects on the time scale the change of variable

$$t = \lambda t', \ \lambda = \omega^{-1},$$

where t' is the scaled time variable.

The effect on the state-input equations is that state variables and independent sources are now measured in terms of the variable t', and the A, B, C, D matrices in the scaled quantities are now the old A, B, C, D matrices multiplied by λ. The form of the state-output equations does not change; however, the outputs are now expressed in terms of the scaled time variable t'.

As far as the user is concerned, the implications of using a frequency scaling factor are the following:

(i) Sampled data inputs and Fortran defined or otherwise user supplied input data must be expressed in terms of the scaled time variable t'.

(ii) Calculated time response outputs for which the unscale option is not (or cannot be) exercised are expressed in terms of the scaled time parameter t'.

(iii) User controls on the numerical integration routines must be specified in terms of t'; i.e. stop time, print increment, start time, etc.

(iv) Solution equations computed in the matrix mode will be expressed in terms of the time variable t'.

Impedance Scaling

Assume an input impedance scaling factor

$$\text{IMPEDANCE} = kz, \; kz \neq 1$$

is user supplied by means of the scaling option. In this instance the solution of equations (1) and (2), but with the B and C subscripte matrices of the state-input and state-output equations replaced as indicated below, is obtained.

$$\begin{aligned} B_{(\;)} &\longrightarrow \frac{1}{kz} B_{(\;)} \\ C_{(\;)} &\longrightarrow kz \; C_{(\;)} \end{aligned} \qquad (3)$$

The implications of impedance scaling as seen from the new form of the state and output equations is that scaled outputs and unscaled outputs are not simply related (linearly) except in the following cases:

(a) Only voltage sources

(i) Scaled time domain voltage outputs from STICAP are true outputs.

(ii) Scaled current outputs must be divided by kz to obtain the true output.

(iii) Initial conditions input to the program must, of course, be scaled, inversely to that scaling of (i), (ii).

(b) Only current sources

(i) Scaled time domain current outputs are true outputs.

(ii) Voltage outputs must be multiplied by kz to obtain true outputs.

(iii) Initial conditions input to the program must be scaled, inversely to that of (i) and (ii).

The case (a) corresponds mathematically to making on equations (1) and (2) the changes of variable

$$(\overline{X}_i) \text{ scaled} = kz\ \overline{X}_i$$

$$(\overline{Y}_i) \text{ scaled} = kz\ \overline{Y}_i$$

with no changes of variable on $\overline{X}_v$, $\overline{Y}_v$. In case (b) the corresponding changes of variable are

$$(\overline{X}_v) \text{ scaled} = \frac{1}{kz}\ \overline{X}_v$$

$$(\overline{Y}_v) \text{ scaled} = \frac{1}{kz}\ \overline{Y}_v.$$

For the mixed case Stanley suggests the combining of voltage and current sources to obtain sources all of one kind. If this is not considered feasible the alternate below is advocated.

For the mixed case the scaled equations produced by STICAP can alternately be obtained from the unscaled equations by either of the following changes of variable:

I. $(\overline{X}_v) \text{ scaled} = \frac{1}{kz}\ \overline{X}_v$

$(\overline{Y}_v) \text{ scaled} = \frac{1}{kz}\ \overline{Y}_v$

$(\overline{U}_v) \text{ scaled} = \frac{1}{kz}\ \overline{U}_v$

II. $(\overline{X}_i) \text{ scaled} = kz\overline{X}_i$

$(\overline{Y}_i) \text{ scaled} = kz\overline{Y}_i$

$(\overline{U}_i) \text{ scaled} = kz\overline{U}_i$

Thus the user may use the scaling option for the mixed case, provided he scales (one but not both of) his current or voltage sources input to the program, as well as the corresponding initial conditions. The outputs are then to be interpreted by referral to (one but not both of) the proper output scaling equations (see case I and II).