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FINAL REPORT
RADAR RANGE DATA SIGNAL ENHANCEMENT TRACKER

NAS 9-13739

23 April 1975

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Prepared for
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
JOHNSON SPACE CENTER
HOUSTON, TEXAS

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Prepared by
Subsystems Engineering and Analysis Department

TRW
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Approved by: H. B. Killen
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Project Manager

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1.0 INTRODUCTION

This report describes the design, fabrication, and performance characteristics of two digital data signal enhancement filters which are capable of being inserted between the Space Shuttle Navigation Sensor outputs and the guidance computer. Commonality of interfaces has been stressed so that the filters may be evaluated through operation with simulated sensors or with actual prototype sensor hardware.

The filters will provide both a smoothed range and range rate output. Different conceptual approaches are utilized for each filter. The first filter is based on a combination low pass nonrecursive filter and a cascaded simple average smoother for range and range rate, respectively. Filter number two is a tracking filter which is capable of following transient data of the type encountered during burn periods. A test simulator was also designed which generates typical shuttle navigation sensor data. Details of this design are included in the report.

The design approach taken for both filters was to implement the filters as microprocessors. The first filter design was implemented as a special purpose device. The only component lacking in this filter to make it a true microprocessor is an arithmetic logic unit capable of add, subtract, logical operations, etc. This unit does contain an accumulator.

The digital tracking filter was implemented as a true microprocessor. As a matter of interest, this unit could be programmed to perform the functions of the first filter as well as other filter concepts.

As presently programmed, the first filter is capable of smoothing over 1, 2, 3, and 4 second intervals with sample rates of 16, 8, 4, and 2 samples/sec, respectively. The output range rate word is computed based on the most recent range word and the seventeen previous range words. The smoothed range word is based on the most recent range word and the fifteen previous range words.

The second filter is programmed to smooth over 2, 4, 8, and 16 range words beginning with the most recent. Sample rates for any of the above options may be 2, 4, 8, and 16 samples/second. A smoothed range and range rate output are provided. Based on the computed range rate, both filters provide an update for the smoothed range word to correct for the time lag resulting from averaging over N words.

2.0 FILTER ANALYSIS

2.1 N-SAMPLE SMOOTHING FILTER

The N-sample filter is a discrete, linear, time invariant, non-recursive, finite memory, polynomial smoothing filter. A review of the literature indicates that considerable work has been devoted to analysis of this smoothing technique. This analysis exists largely through the efforts of R. B. Blackman[1] and J. D. Musa[2]. In this section, portions of this work are reviewed and applied to the problem at hand.

Consider the random process R(nT), where n is an integer and T is the sample period. The process can be thought of as comprising a signal component $\overline{R}(nT)$ and a noise component $\tilde{R}(nT)$. It is assumed that $\overline{R}(nT)$ can be satisfactorily approximated by an rth degree polynomial in nT, R(nT). Also, assume that $\tilde{R}(nT)$ is a random noise process that is wide sense stationary with respect to the sampling instants nT. This situation occurs in the tracking of a moving object whose true position could be represented as an rth degree polynomial and whose measured position includes a random error. For significant filtering action to be possible, it is necessary that

$$E[R(nT)] = 0 \tag{1}$$

and var $[R(nT)] = \text{var}[\tilde{R}(nT)] = \sigma_R 2$. That is, the signal must represent the d.c. component and noise is the time varying component over the time interval chosen for smoothing.

Let $\Phi_R(iT)$ represent the autocorrelation function of $\tilde{R}(nT)$, where i is an integer. A discrete polynomial smoother of the pth order and rth degree is a filter that operates on R(nT) in such a fashion that the output C(nT) and the input R(nT) are related by

$$E[C(nT)]^2 = R^{(p)}(nT + \tau) \tag{2}$$

for all n. The quantity τ represents prediction time. If τ is negative, the operation performed is interpolation and if τ is zero the operation represents smoothing. The superscript (p) denotes the "pth derivative of the estimate with respect to nT." Thus for p equal zero, the output represents position data; for p equal one the output represents velocity information, etc.

A linear, time-invariant smoother which is nonrecursive and has finite memory may be described in terms of the input-output relationship

$$C(nT) = \sum^{N-1} W(iT)\ R[(n-i)T] \tag{3}$$

where W(iT) is the weighting function. Note that W(iT) is defined only at a finite number of points, that it is independent of the input, and that it is invariant with the time nT. No previous values of the output appear in (3), therefore the smoother is nonrecursive. The variance ratio

$$\mu^2 = \frac{\sigma_C^2}{\sigma_R^2} \tag{4}$$

is a measure of the efficiency of the smoother. Since R(nT) was assumed wide-sense stationary, C(nT) is also wide-sense stationary. This follows from the time invariance of the smoother. Therefore μ^2 is not a function of time.

If $\tilde{R}(nT)$ has an autocorrelation function of arbitrary form, it may be shown using equations (1), (3), and (4) that

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$$\mu^2 = \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} W_i W_j \Phi_R[(i - j)T] \tag{5}$$

where $W_i = W(iT)$ and $W_j = W(jT)$. If the power density spectrum of the noise is white, the autocorrelation function, Φ, assumes the form of

$$\Phi_R[(i - j)T] = \begin{cases} 1 & i = j \\ 0 & i \neq j \end{cases} \tag{6}$$

and equation (5) becomes

$$\mu^2 = \sum_{i=0}^{N-1} W_i^2 \tag{7}$$

However, the noise of interest here is not necessarily uncorrelated from sample to sample. Musa has shown that correlated noise may be represented by the wide-sense Markov process as a first order approximation, or by a linear combination of such processes as a better approximation. Either the autocorrelation function or the power density spectrum may be approximated.

2.1.1 Wide-Sense Markov Noise Model

A wide-sense stationary, continuous random process will be called wide-sense Markov if it has the autocorrelation function

$$\Phi(\tau) = \exp(-\Omega\tau), \ \tau \geq 0. \tag{8}$$

A rigorous definition for wide-sense Markov noise may be found in Doob[3]. The quantity Ω is called the "noise bandwidth." By using the eveness

property of autocorrelation functions, equation (8) may be written as

$$\Phi(\tau) = \exp(-\Omega|\tau|). \tag{9}$$

For a discrete wide-sense Markov process with equally spaced samples, the autocorrelation function may be written as

$$\Phi(\tau) = \exp(-\Omega|\tau|)\ Cb_T(T), \tag{10}$$

where Cb_T is the comb function defined by

$$Cb_T(\tau) = \sum_{i=-\infty}^{+\infty} \delta(\tau - iT). \tag{11}$$

The power density spectrum obtained by Fourier transforming (11) is

$$S(f) = \frac{2\Omega}{(2\pi f)^2 + \Omega^2} * \frac{1}{T}\, Cb_{1/T}\ (f) \tag{12}$$

where the * indicates convolution.

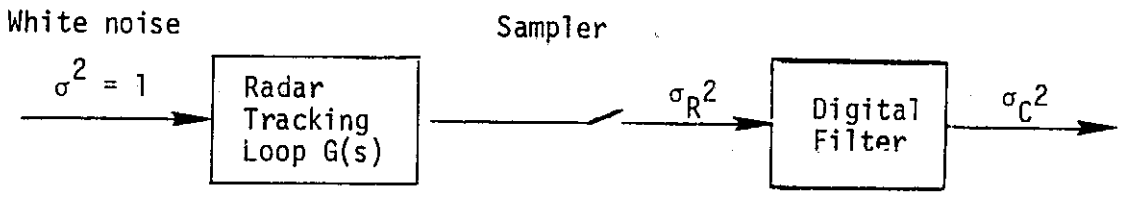
Using the wide-sense Markov noise model reduces (5) to

$$\mu^2 = \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} W_i\ W_j\ \alpha^{|i-j|} \tag{13}$$

where

$$\alpha = \exp(-\Omega T). \tag{14}$$

Applying this to the LM rendezvous radar, consider the system shown in Figure 1.



$$G(s) = \frac{24\,(s + 11.2)}{s^2 + 24.67s + 268.96}$$

Figure 1. LM Rendezvous Radar Tracking Loop Output With Smoothing Filter

White noise is filtered by the radar such that the normalized power density spectrum at the input to the sampler becomes

$$s(\omega) = \frac{G(j\omega)^{\,2}}{\sigma^2} \tag{15}$$

where

$$\sigma^2 = \frac{1}{2\pi}\int_{-\infty}^{\infty} |(Gj\omega)|^2 d\omega = 12.10 \tag{16}$$

The closed loop transfer function is given by

$$G(s) = \frac{24(s + 11.2)}{s^2 + 24.67s + 268.96} . \tag{17}$$

Using Equations (15), (16), and (17), the normalized noise spectral density at the radar output becomes

$$s(\omega) = 26.58 \frac{\omega^2 + 224.8}{\omega^4 + 60.7\omega^2 + 72339} \tag{18}$$

and is graphed in Figure 2 along with first and second approximations. The second approximation is given by

$$s(\omega) \simeq \sum_{v=1}^{3} A_v \frac{2v\Omega}{(v\Omega)^2 + \omega^2} \tag{19}$$

where $v\Omega$ is the half power point in each approximation.

An "optimum smoother" of the class being discussed has been investigated by Blackman. This specifies the filter whose weighting function yields the minimum possible value of μ^2. This work has been extended by Musa to include a linear combination of noise power inputs. The noise variance ratio of a linear discrete system for which the input noise power has been approximated may be expressed as

$$\mu^2 = \sum_{v} A_v \left[\frac{1 + e^{-v\Omega T}}{N - (N-2)e^{-v\Omega T}} \right] \tag{20}$$

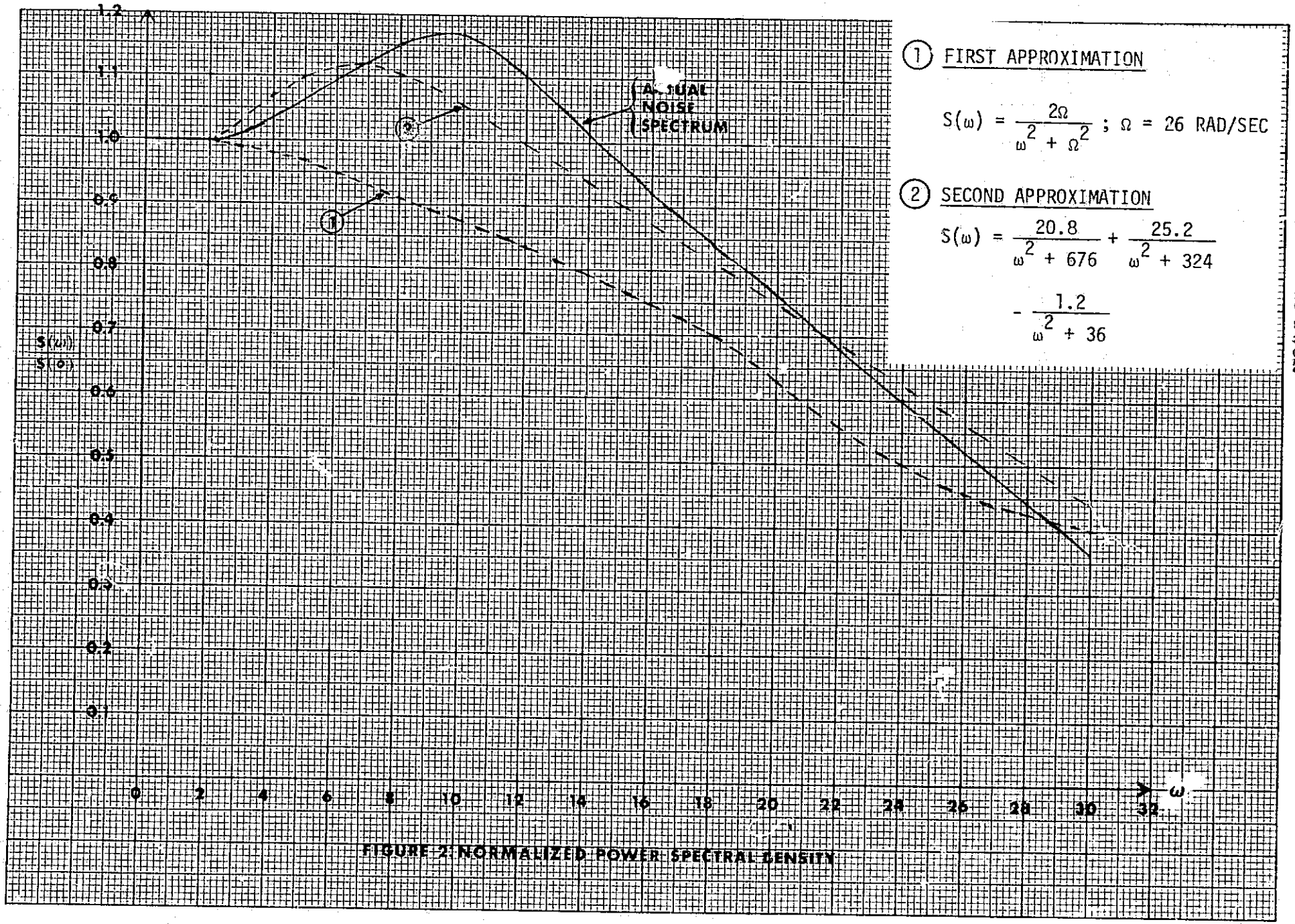


FIGURE 2: NORMALIZED POWER SPECTRAL DENSITY

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where N is the number of samples and T is the time between samples. Using this expression, the smoothing action of an N-sample averaging filter is graphed in Figure 3 for the LM rendezvous radar. The corresponding weighting function is given by

$$W_i = \begin{cases} \dfrac{1}{N - (N-2)\alpha} & (i = 0, N-1) \\[2ex] \dfrac{1 - \alpha}{N - (N-2)\alpha} & (i = 1, 2, ---, N-2) \end{cases} \tag{21}$$

and is shown in Figure 4.

Referring now to Equation (2), for p = 1. The filter output represents velocity information. The variance ratio for this case is given by

$$\mu^2 = \frac{1}{T^2} \frac{12\eta}{(N-1)\left\{ [1 + \eta(N-1)]\,[2 + \eta(N-1)] + [1 - \eta^2] \right\}} \tag{22}$$

where

$$\eta = \frac{1 - \alpha}{1 + \alpha} \tag{23}$$

The corresponding weighting function is

$$W_i = \begin{cases} \dfrac{3}{T} \dfrac{(1+\eta)[1+\eta(N-2)]}{(N-1)\left\{ [1+\eta(N-1)][2+\eta(N-1)] + [1-\eta^2] \right\}}, & (i = 0) \\[2ex] \dfrac{6}{T} \dfrac{\eta^2(N-1-2i)}{(N-1)\left\{ [1+\eta(N-1)][2+\eta(N-1)] + [1-\eta^2] \right\}}, & (i = 1,2,---,N-2) \\[2ex] \dfrac{-3}{T} \dfrac{(1+\eta)[1+\eta(N-2)]}{(N-1)\left\{ [1+\eta(N-1)][2+\eta(N-1)] + [1-\eta^2] \right\}}, & (i = N-1) \end{cases} \tag{24}$$

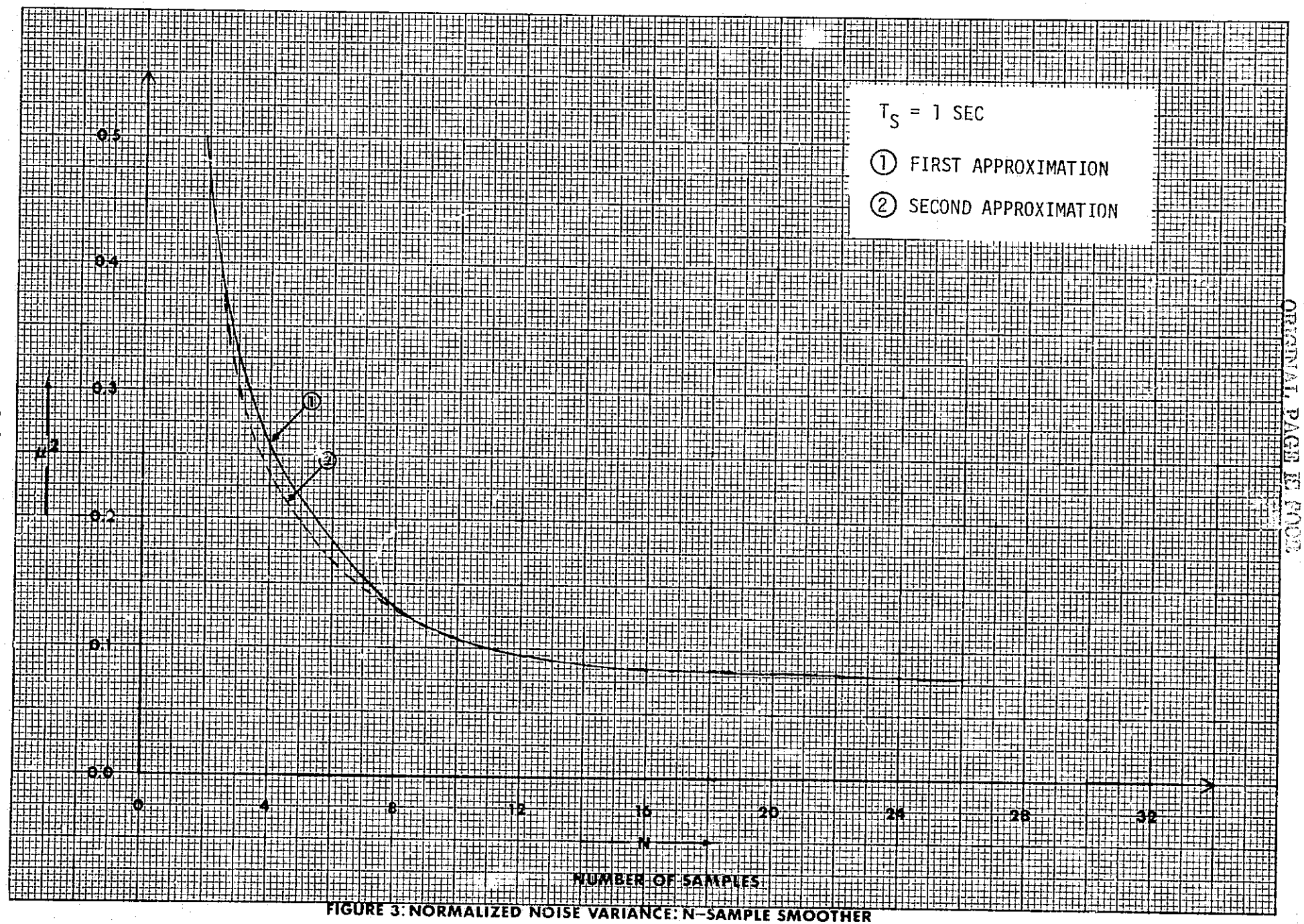

FIGURE 3: NORMALIZED NOISE VARIANCE: N-SAMPLE SMOOTHER

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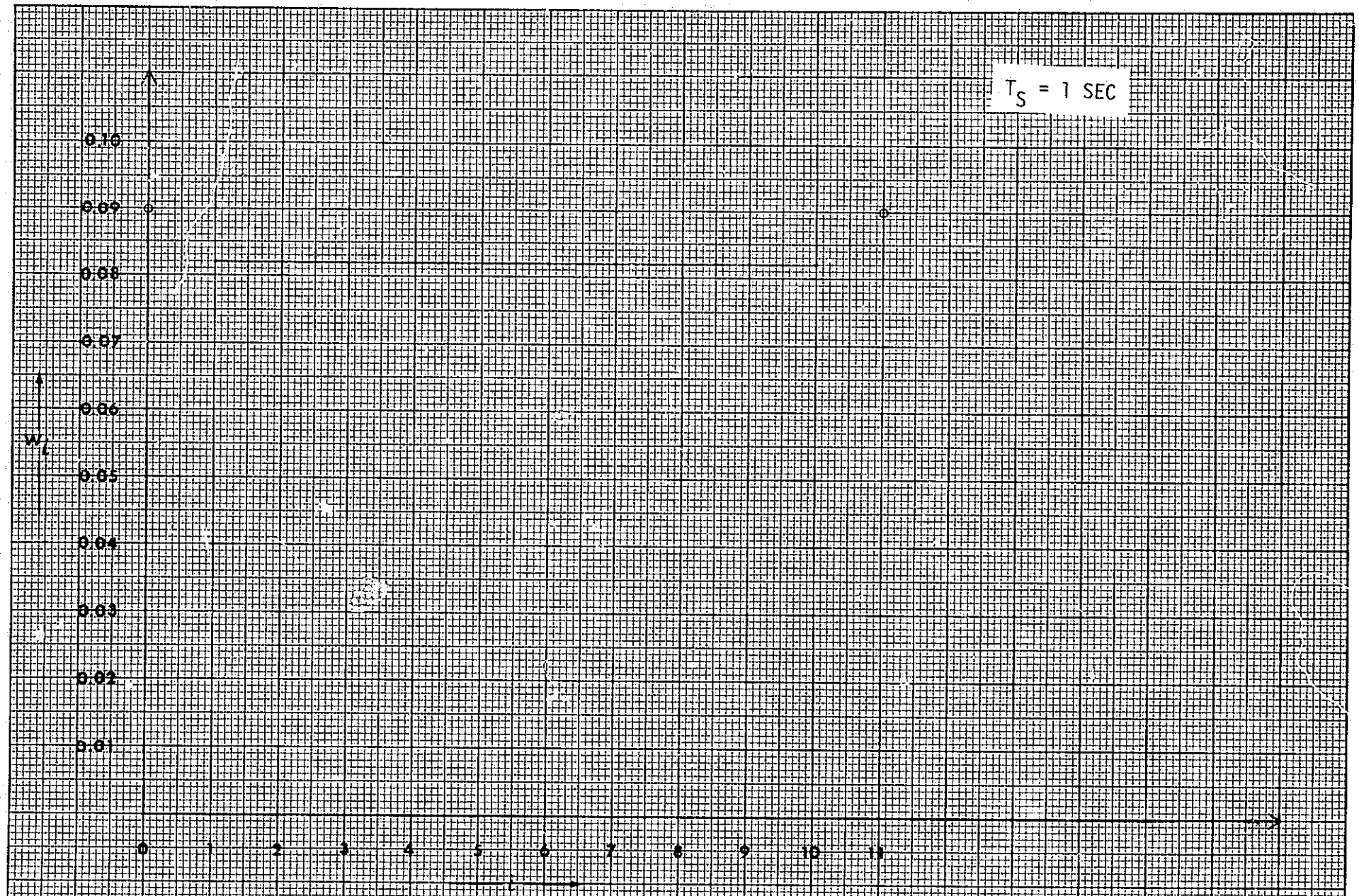

FIGURE 4. OPTIMUM WEIGHTING FUNCTION: N SAMPLE SMOOTHER

and both functions are plotted in Figures 5 and 6.

2.1.2 Cascaded Simple Averages Smoothers

The idea of obtaining a nonuniform weighting sequence of finite length by cascading uniform weighting sequences of shorter length originated with J. W. Tukey[4]. The overall weighting sequence is the multiple discrete convolution of the cascaded simple weighting sequences. For example, the convolution of the simple weighting sequence

$$\left\{12(1)\right\} = \left\{1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1\right\} \tag{25}$$

with the weighting sequence

$$\left\{6(1)\right\} = \left\{1, 1, 1, 1, 1, 1\right\} \tag{26}$$

is the weighting sequence

$$\left\{12(1)\right\} * \left\{(1)\right\} = \left\{1, 2, 3, 4, 5, 6, 6, 6, 6, 6, 6, 6, 5, 4, 3, 2, 1\right\}. \tag{27}$$

This technique was extended by Blackman to include a differencing operation. This results in a simplification of the procedure for obtaining velocity or acceleration information. For example if

$$\left\{\Delta\right\} = \left\{1, -1\right\}$$

then

$$\left\{\Delta\right\} * \left\{12(1)\right\} * \left\{6(1)\right\} = \left\{1, 1, 1, 1, 1, 1, 0, 0, 0, 0, 0, 0, -1, -1, -1, -1, -1, -1\right\}. \tag{29}$$

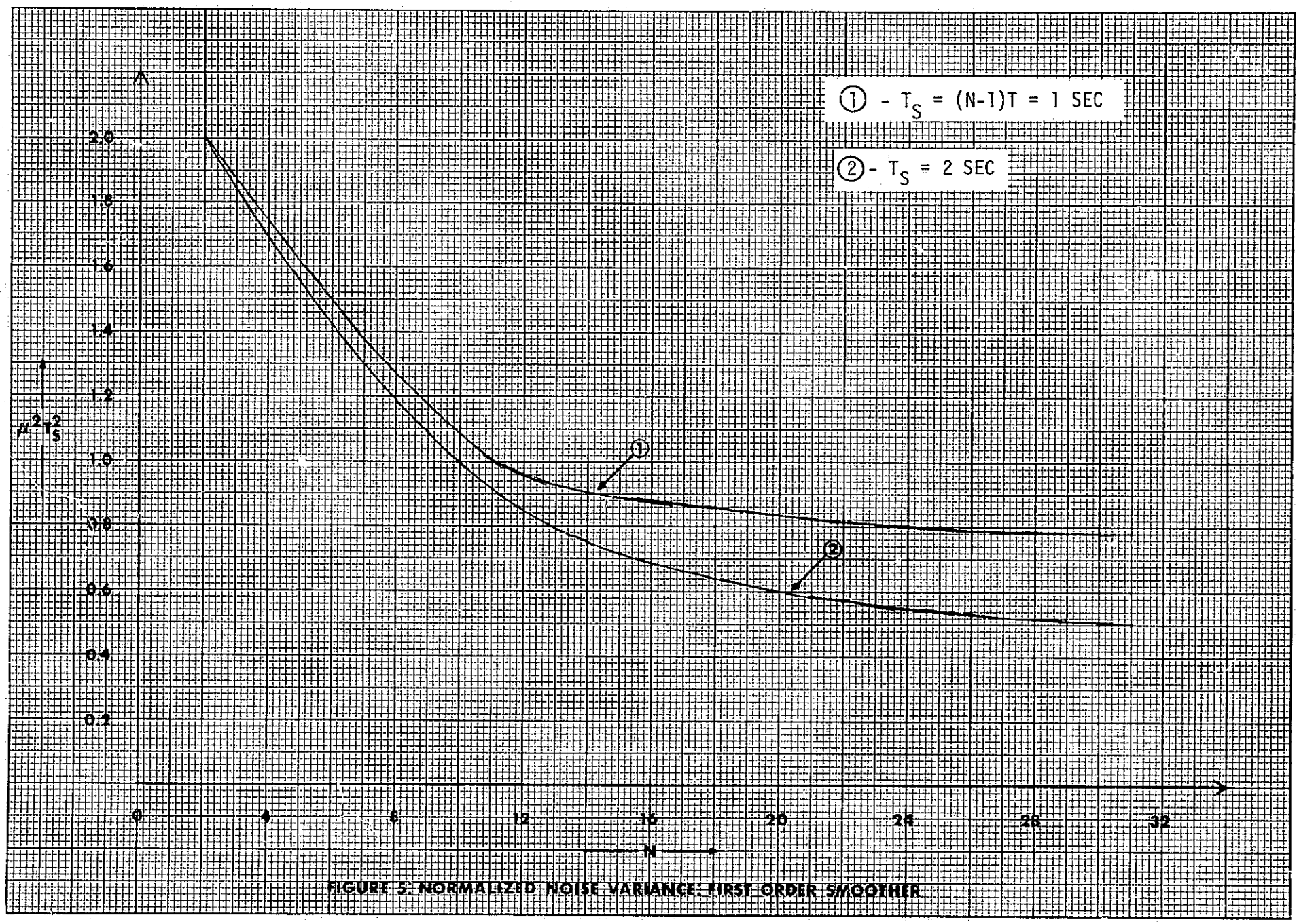

FIGURE 5. NORMALIZED NOISE VARIANCE: FIRST ORDER SMOOTHER

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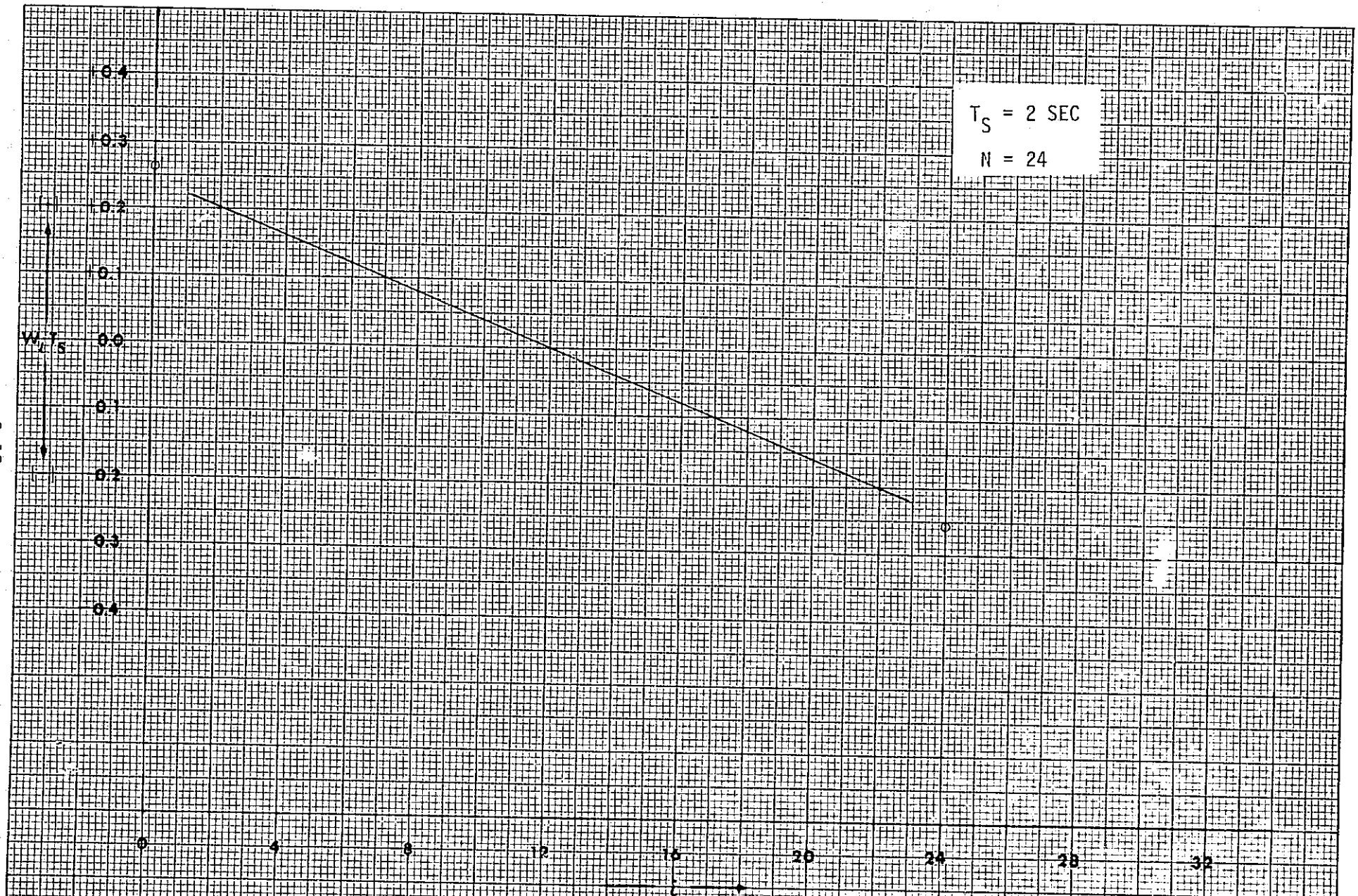

FIGURE 6: OPTIMUM WEIGHTING FUNCTION: FIRST ORDER SMOOTHER

This is equivalent to applying to the original time series a weighting sequence consisting of six consecutive ones, followed by six consecutive zeros, and followed in turn by six consecutive negative ones.

2.1.3 Smoothed First Differences

Consider the following procedure.

1.1 Keep the most recent $n_1 + 1$ terms of the original time series in store.

1.2 Generate each term of a second times series by taking the difference between the newest and oldest terms stored in 1.1 and dividing by n_1T. Keep the most recent n_2 terms of this series in store ($n_2 \leq n_1$).

1.3 Generate each term of the final output time series by summing the terms stored in 1.2 and dividing by n_2 (see top half of Figure 7).

Thus, the second time series represents moving simple averages of n_1 consecutive first differences and as such is a smoothed velocity. The whole scheme is equivalent to applying two moving simple averagings, in cascade, to the first differences of the original time series. In terms of Equation (29), the weighting sequence may be represented by

$$W_i = \frac{1}{n_1 n_2 T} \left\{ n_2(1),\ (n_1 - n_2),\ n_2(-1) \right\} . \qquad (30)$$

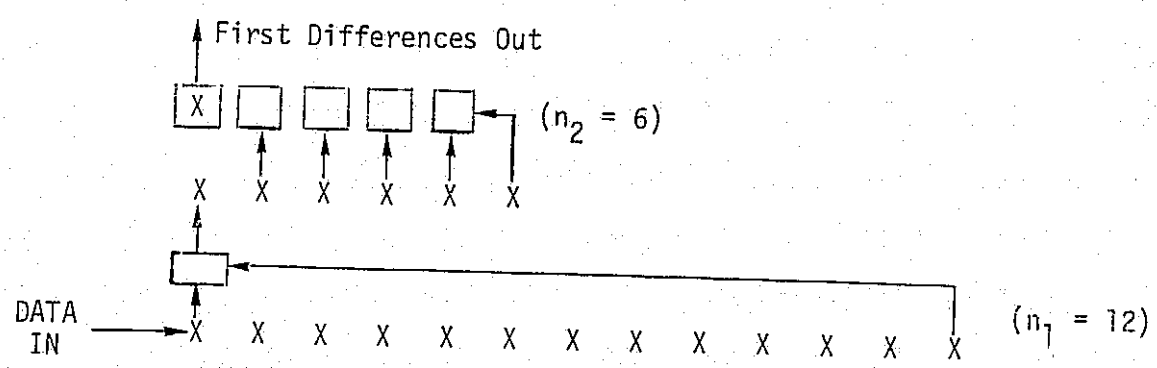

Figure 7. First Differences by Cascaded Simple Averaging

These smoothers are an approximation of the optimum smoothers discussed previously. The approximation for the first order smoother involves using only the values K, -K, and 0 for the weighting coefficients, where K is a constant. Referring to Figure 6, note that the optimum weighting function consists of a positive and negative triangle symmetrical about the middle of the time series. The approximation substitutes a rectangle of weight plus K for the first triangle followed by a weight of zero in the middle of the time series where the weights are small, and finally by a rectangle of weight minus K for the negative triangle. This technique reduces the amount of storage at the cost of a slight increase in μ^2.

The weighting functions of cascaded simple averaging smoothers for both the 0th and 1st order are as follows:

$$W_i = \frac{1}{N} \tag{31}$$

and

$$W_i = \begin{cases} \frac{4.5}{NT_s} & (0 \le i \le \frac{N}{3} - 1) \\ 0 & (\frac{N}{3} \le i \le \frac{2}{3}N - 1) \\ \frac{4.5}{NT_s} & (\frac{2}{3}N \le i \le N - 1) \end{cases} \quad . \tag{32}$$

Equation (32) is equivalent to Equation (30) where N is a multiple of 3. The weighting function for the first order smoother is plotted in Figure 8.

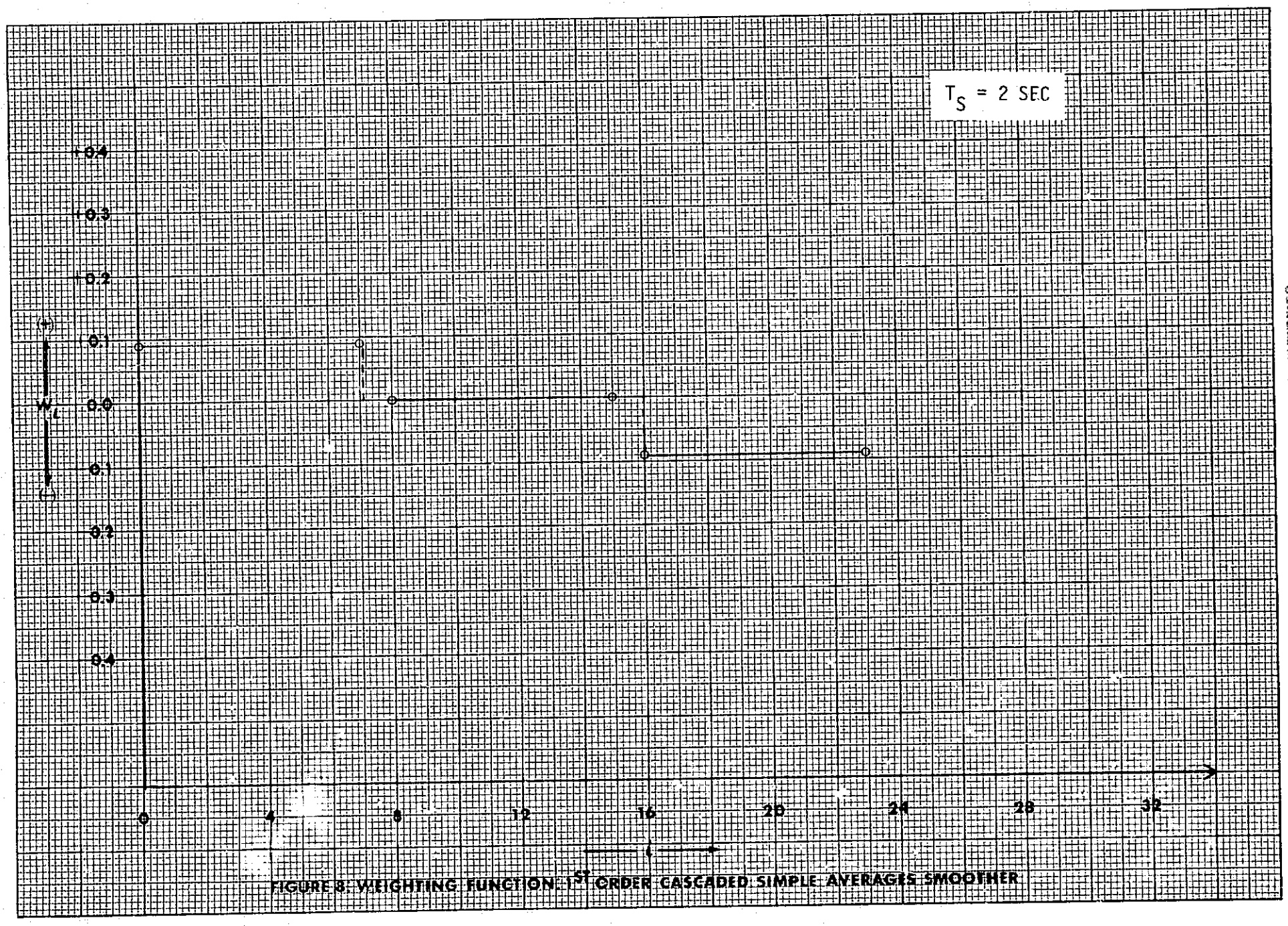

FIGURE 8. WEIGHTING FUNCTION: 1ST ORDER CASCADED SIMPLE AVERAGES SMOOTHER

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Variance ratios for the 0th and 1st order smoother, are respectively:

$$\mu^2 = \frac{1+\alpha}{N(1-\alpha)} + \frac{2\alpha(\alpha^N-1)}{[N(1-\alpha)]^2}$$

and

$$\mu^2 = 2\left(\frac{4.5}{T_s}\right)^2 \left(\frac{N-1}{N}\right)^2 \left\{\frac{1+\alpha}{3N(1-\alpha)} - \frac{\alpha(\alpha^N-2\alpha^{2N/3}-\alpha^{N/3}+2}{[N(1-\alpha)]^2}\right\} \tag{34}$$

These variance ratios are plotted in Figures 9 and 10.

The output noise variance ratio for white noise is given by

$$\mu^2 = \frac{27}{2\ N^3T^2} = 0.14. \tag{35}$$

The first order smoother was investigated for providing a smoothed range rate. Comparing Figures 5 and 10 it is evident that the first order cascaded averages smoother provides smoothing action which is identical for all practical purposes. For ease of implementation, it this design for the range rate smoother was selected.

It was desired to investigate the dynamic response of the range rate smoother under the shuttle functional requirement that range rate error be at most 0.3 fps. A computer program was written to evaluate the range rate error. Details of the program are contained in [5]. The simulations begin at a range of 10 nm with a closing rate of 30 fps. At 30 seconds into the run, a 20 second burn was initiated at a constant acceleration level of 0.5 fps. After the burn was complete, the runs were continued for an additional 20 seconds. The range rate error is plotted in Figure 11 for two sample rates. Note that the range

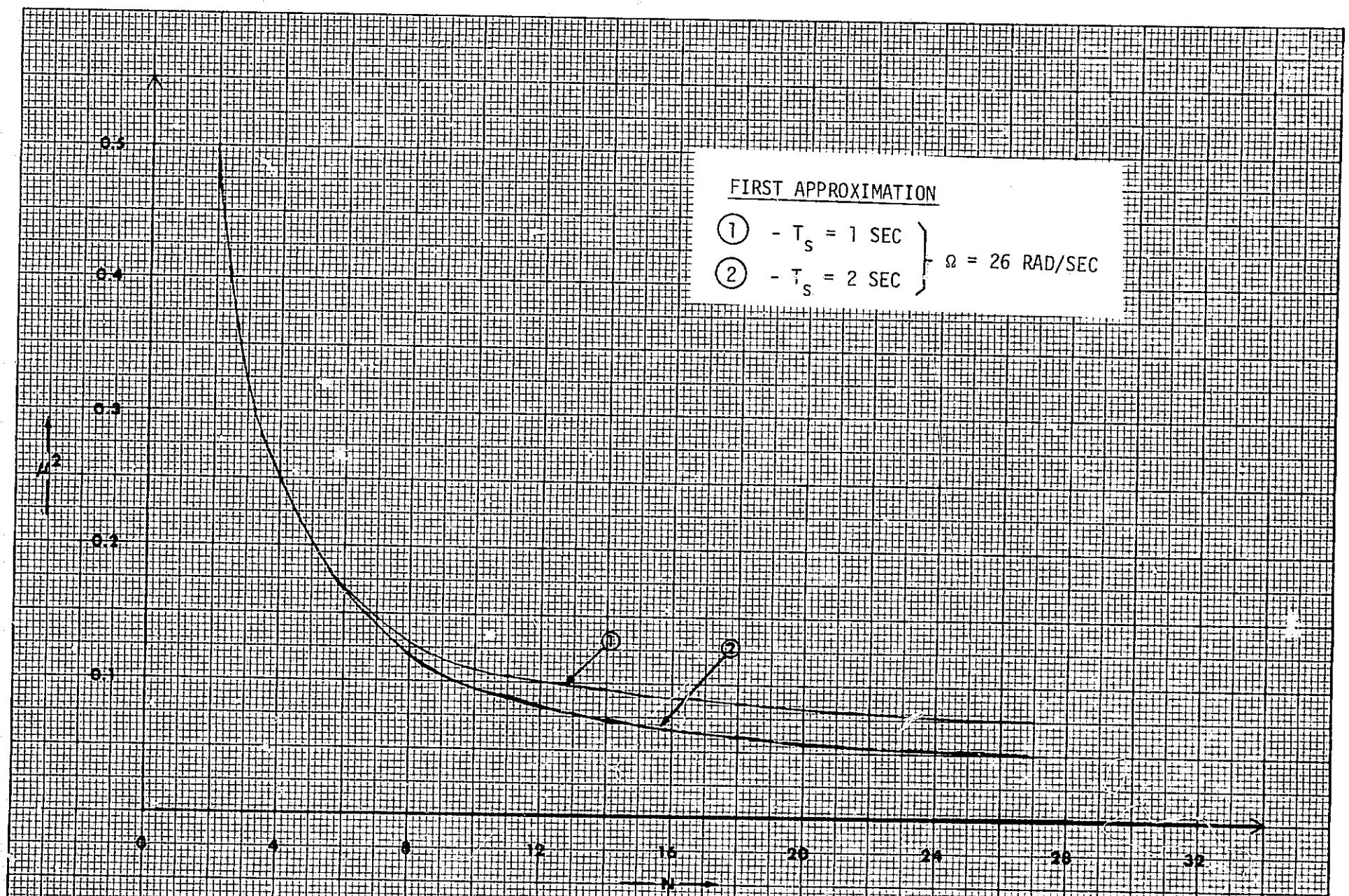

FIGURE 9: NOISE VARIANCE RATIO: 0TH ORDER SMOOTHER

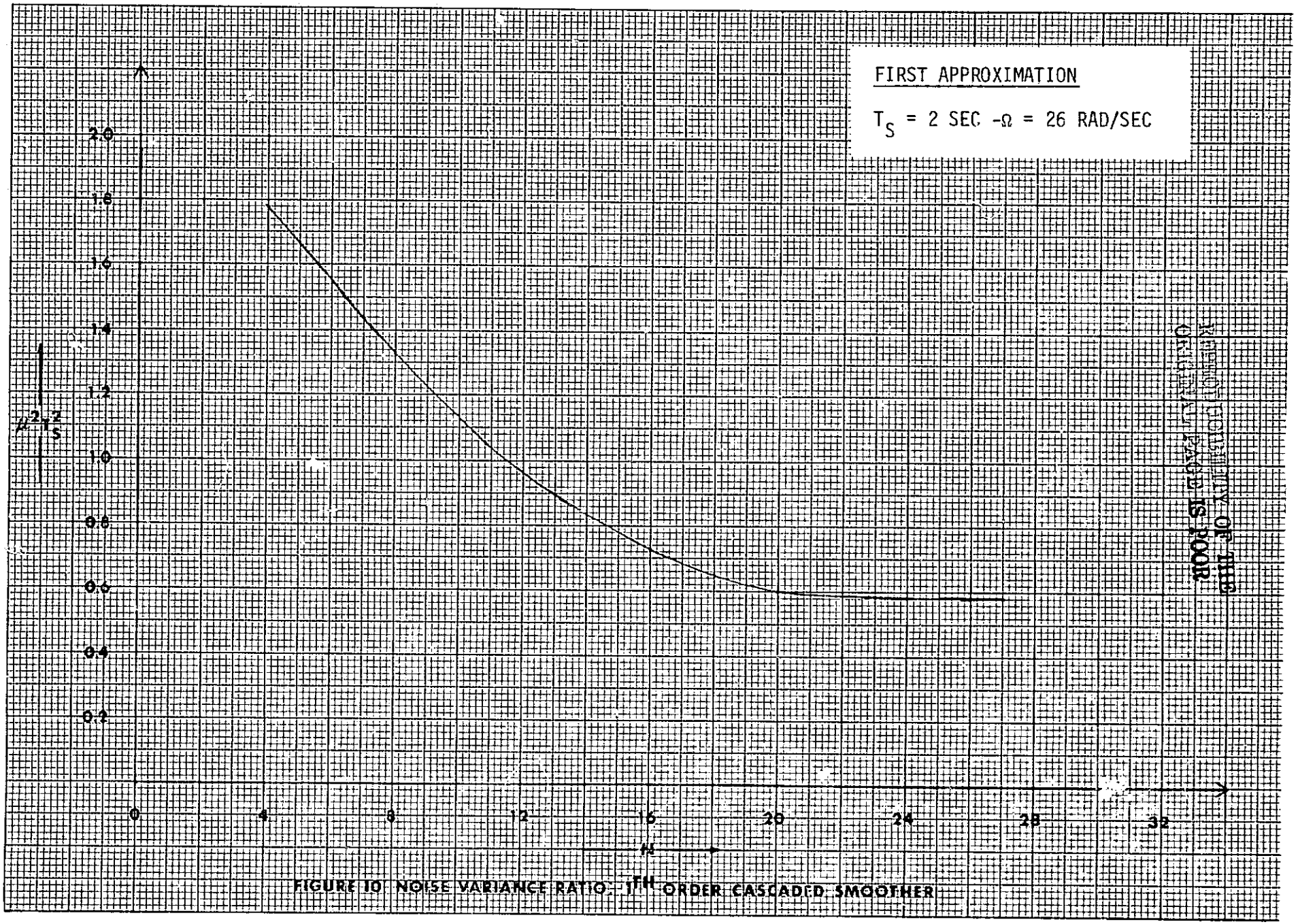

FIGURE 10 NOISE VARIANCE RATIO, 1TH ORDER CASCADED SMOOTHER

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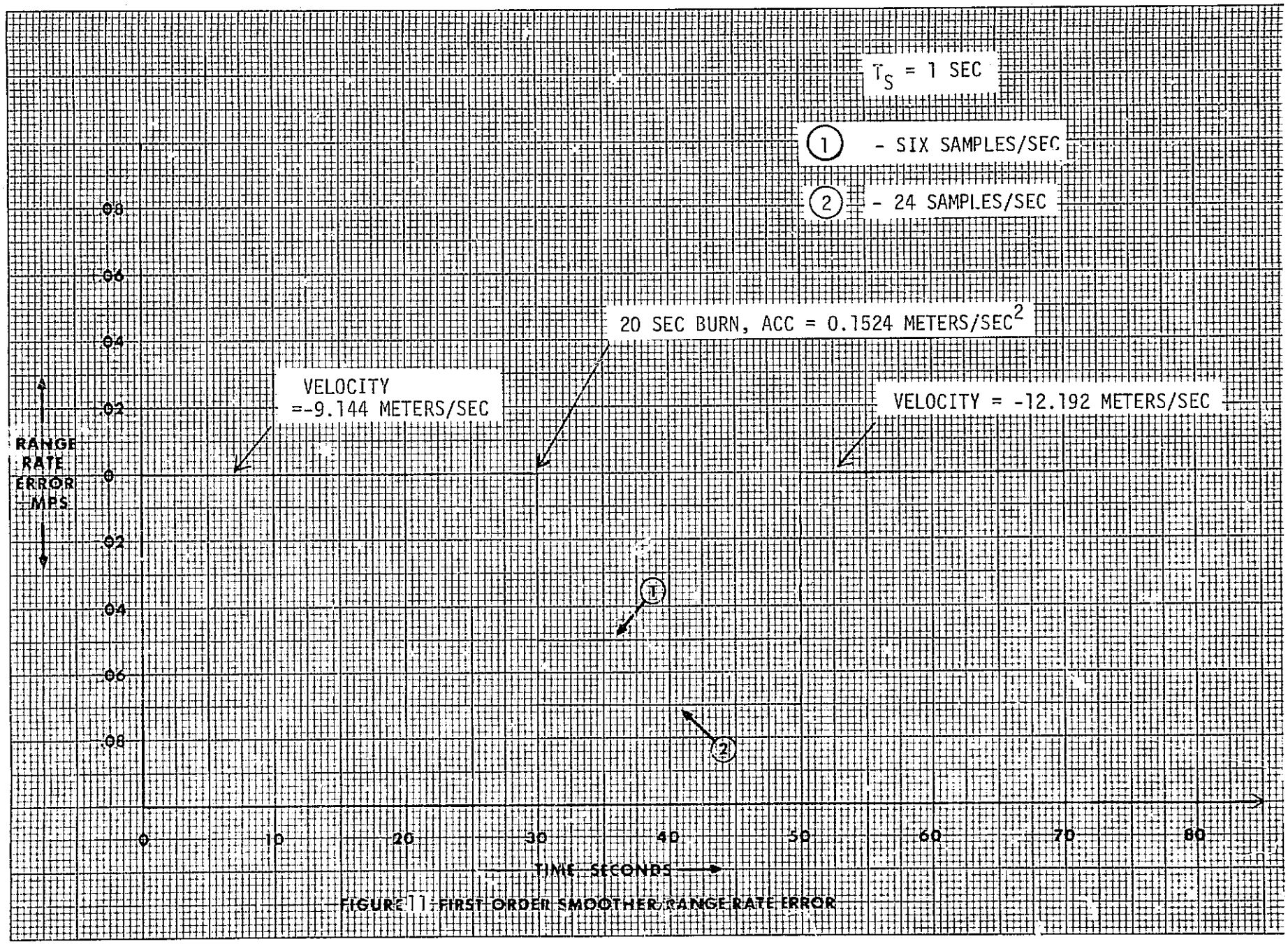

FIGURE 11 FIRST ORDER SMOOTHER RANGE RATE ERROR

rate error is on the order of 0.17 fps during the burn period and zero for constant velocity. The abrupt change from zero to a constant error occurs because in the simulation the burn period start and finish coincided with the one second sample time of the guidance computer. Referring to Figure 10, for a two second smoothing interval, the reduction in range rate error by filtering action may be expressed as

$$\sqrt{\frac{\sigma_{out}^2}{\sigma_{in}^2}} = \sqrt{.15} = 0.39. \tag{38}$$

That is, an input range rate error due to noise of 0.3 fps would be reduced to 0.12 fps.

2.4 DIGITAL TRACKING FILTER

The basic filter which was investigated for shuttle application is shown in Figure 12.

In this filter, the delay time, T, is provided by a holding register which is clocked one sample time later to compute a new difference for the error. The previously smoothed range word is added to the smoothed error to compute a new range word. Multiplying the smoothed error by an appropriate constant results in a smoothed range rate.

Two different designs for this filter were investigated in the initial analysis. In the first design, the smoothed error word consists of a running average which is used to update the output register each sample time. In the second design, the output register is updated after an N number of error words have been smoothed

Performance of the loop insofar as stability and tracking are concerned may be investigated by obtaining the overall closed loop transfer function. The set of difference equations which relate the closed loop input and output in the time domain are:

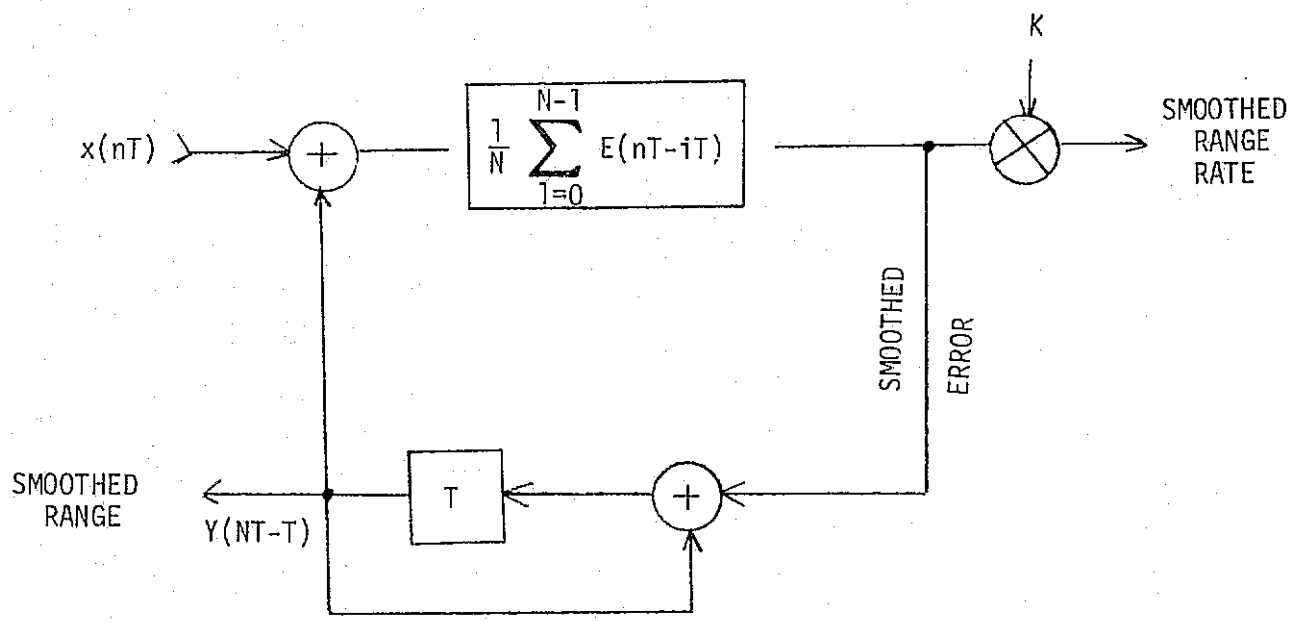

FIGURE 12. DIGITAL TRACKING FILTER

$$E(nT) = x(nT) - y(nT - T) \tag{39a}$$

and

$$y(nT) = y(nT - T) + \frac{1}{N}[E(nT) + E(nT - T) + E(nT - 2T) + \ldots E[nT - (N - 1)T] \quad . \tag{39b}$$

Taking the z-transform of these equations, the closed loop transfer function may be shown to be

$$\frac{y(z)}{x(z)} = \frac{1 + z^{-1} + z^{-2} + \ldots z^{-(N-1)}}{N - (N - 1)z^{-1} + z^{-2} + \ldots Z^{N}} \quad . \tag{40}$$

In this configuration the loop filter has been assumed to be a straight n-sample averaging device whose output updates the output register each sample time. Stability analysis proceeds directly by determining the pole locations in this expression. If any poles fall on or outside the unit circle in the z-plane the system is unstable. Performing this analysis yields the information that the loop is unstable if N equals five or greater. For N equal four, the poles are located very near the unit circle. This analysis was verified independently with a computer simulation. Details of this program are contained in [5]. Figure 13 illustrates a simulated loop response with a ramp input. This simulation data has been verified analytically by inserting the appropriate transform for x(z) into Equation (40) and inverting the resulting equation for y(z). Note that for N equal five, oscillations about the mean never decrease because two poles are located outside the unit circle.

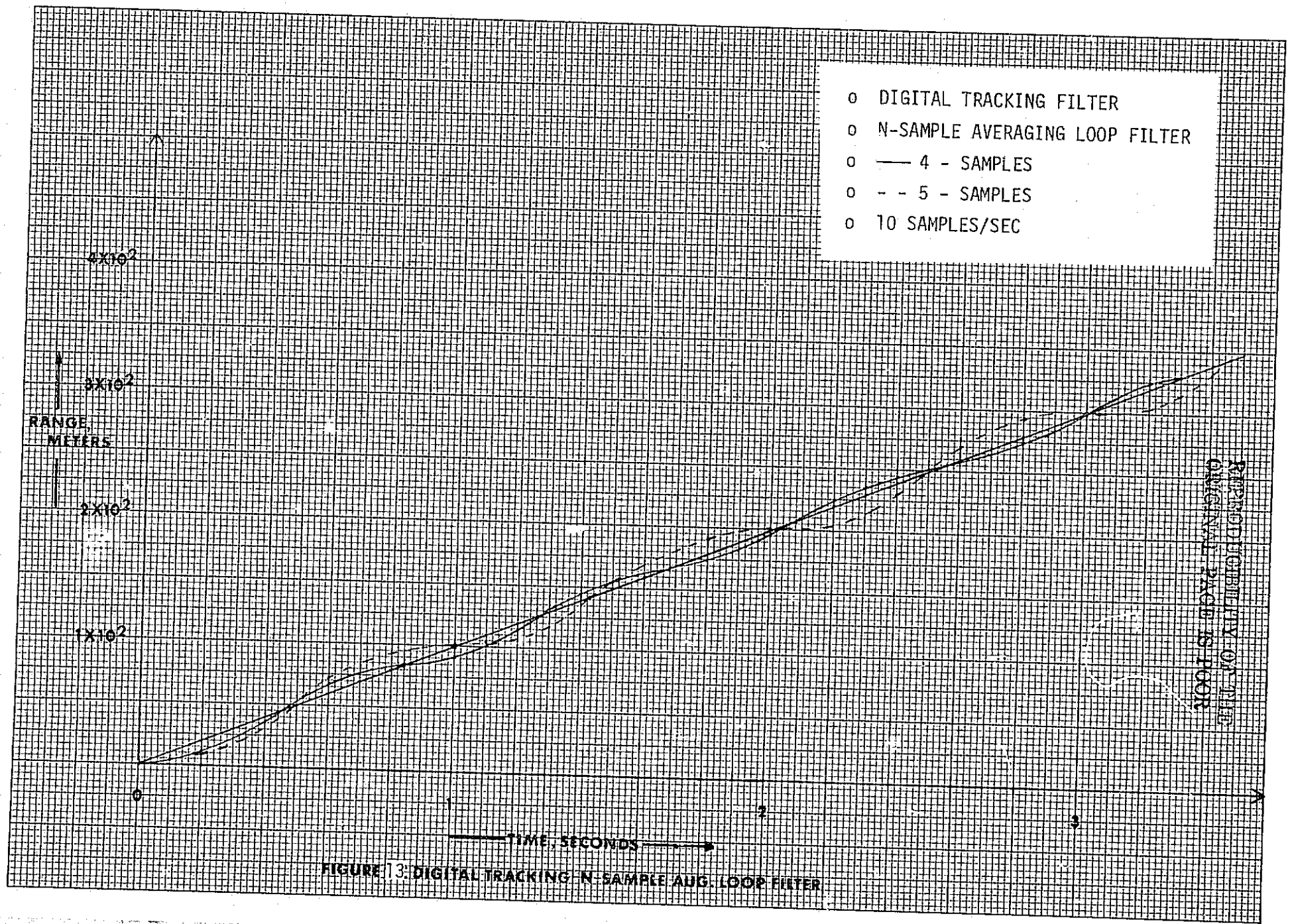

FIGURE 13: DIGITAL TRACKING N-SAMPLE AUG. LOOP FILTER

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The second version of this filter effectively employs a "skip sampler" inserted in the loop immediately preceeding the adder. This filter is illustrated in Figure 14. A correction factor is applied to the smoothed range external to the feedback loop to compensate for lag associated with the averaging action in the filter. Similarly a correction factor is applied external to the loop to insert the time base in the average error. This results in a smoothed range rate output. This filter was simulated and its range rate error is illustrated in Figure 15. Note that the range rate error is on the order of 0.5 fps. The large offset at the beginning of the run occurs because a large word was deliberately set into the smoothed range register at the start. These results, indicate that a digital tracking filter would be capable of producing high quality smoothed range and range rate data during vehicle acceleration.

The tracking filter which was implemented is basically the configuration shown in Figure 14. Since this basic filter produces an output only after smoothing over N data words a multiplexing technique was devised which effectively implements N filters in parallel. With this technique each adjacent filter smoothes over N data words which lags the previous set of N data words by one sample time. Thus, the filter presents a smoothed output word for each input word.

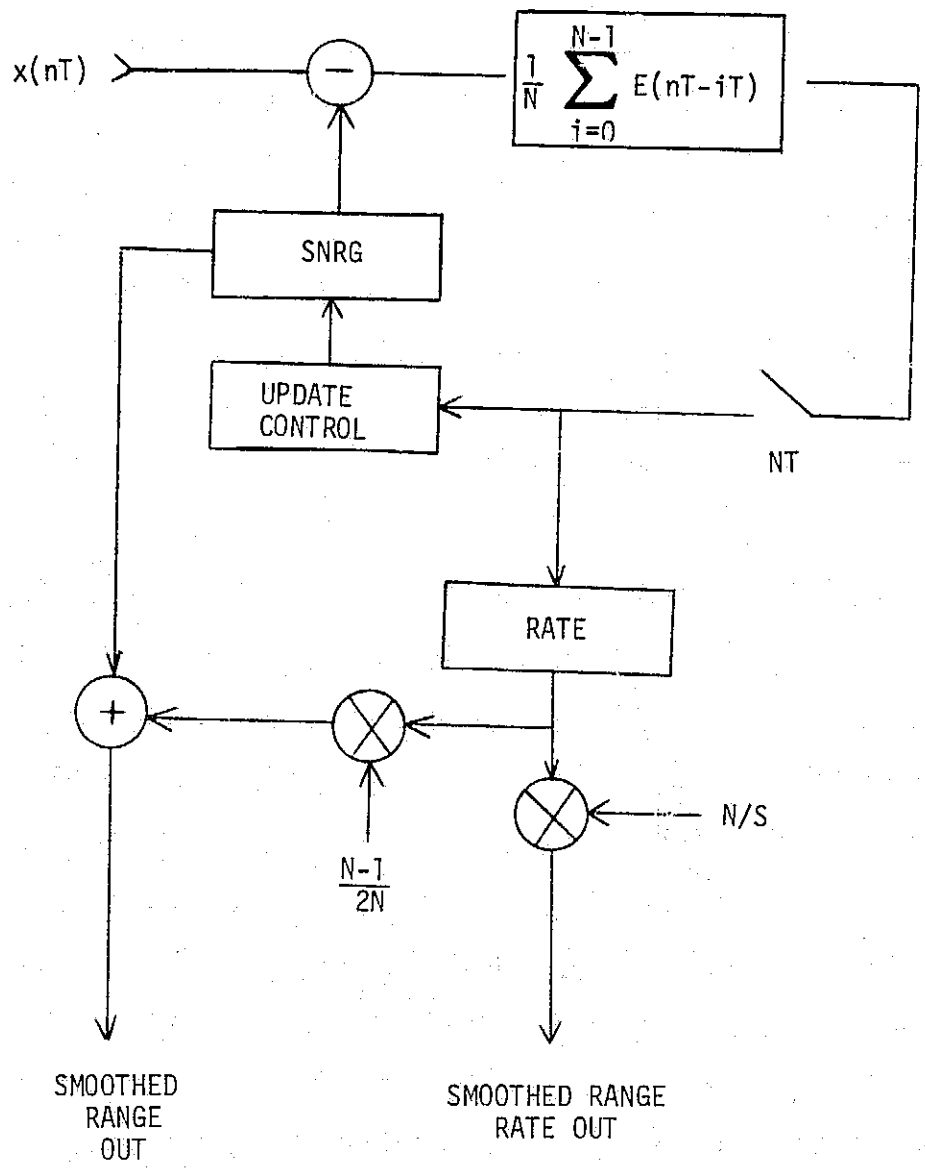

Figure 14. DIGITAL TRACKING FILTER - N-SAMPLE AVERAGING LOOP FILTER WITH SKIP SAMPLING

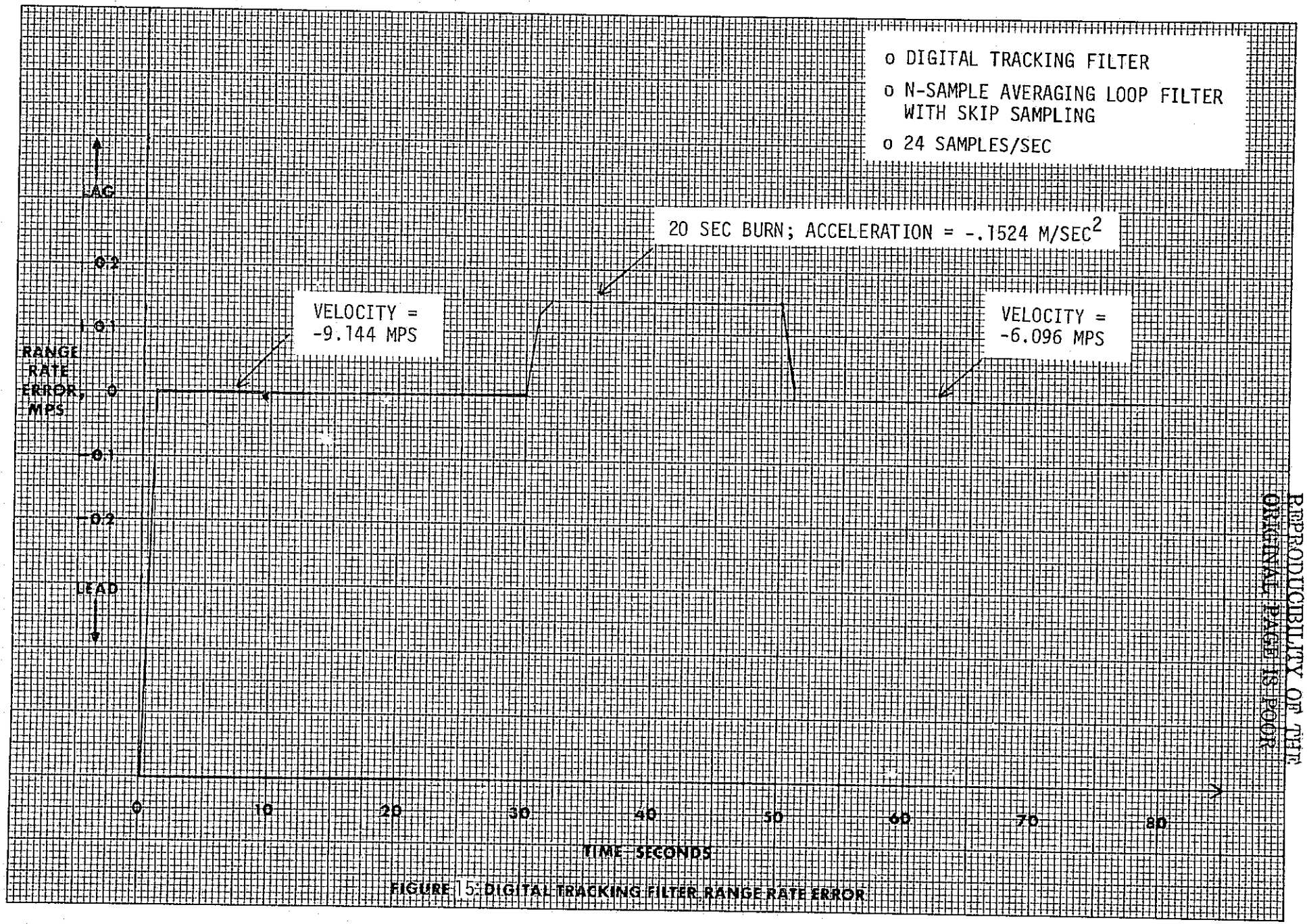

FIGURE 15. DIGITAL TRACKING FILTER RANGE RATE ERROR

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3.0 CASCADED AVERAGING FILTER DESIGN

3.1 FIRST CANDIDATE FILTER

The first candidate filter consists of a combination N-sample smoother which provides a smoothed range and a cascaded simple average smoother for providing range rate. A functional block diagram for the first filter is shown in Figure 16. During operation the smoothed range rate is computed immediately after the reception of a data word followed by the computation of the smoothed range word. The range rate computation implements Equation (32) and the smoothed range computation implements Equation (31).

Operation of the filter may be understood by referring to the filter architecture illustrated in Figure 17. As indicated, the principal components are input-output registers, a 32 word memory, and an arithmetic logic unit. A programmed algorithm using ROM's is utilized to direct functional operations of the various logic units and a data bus provides data communications between the various units.

The operational cycle begins when the filter raises the "data request" line. As soon as a "data ready" signal is received by the filter, the data request line is dropped and the data word entered into the input regester with subsequent storage into the memory. At this point the filter is preprogrammed to perform the following functional steps. The contents of the memory is scanned beginning with word #1 which is the most recent data word. This data word along with the previous five data words are summed together by the arithmetic logic unit which functions as an accumulator. Words 7 through 12 are read out of memory but are not added by the accumulator so that these words are effectively skipped. Beginning with word 13 the next six words are read out of memory and sequentially subtracted from the accumulated sum which represents the first six words. In the event that subtraction through zero occurs, provision is made in the algorithm for complementing so that the resulting difference in the arithmatic logic unit is represented as a magnitude. At this point appropriate division is accomplished to enter the weighting function. This function is pre-

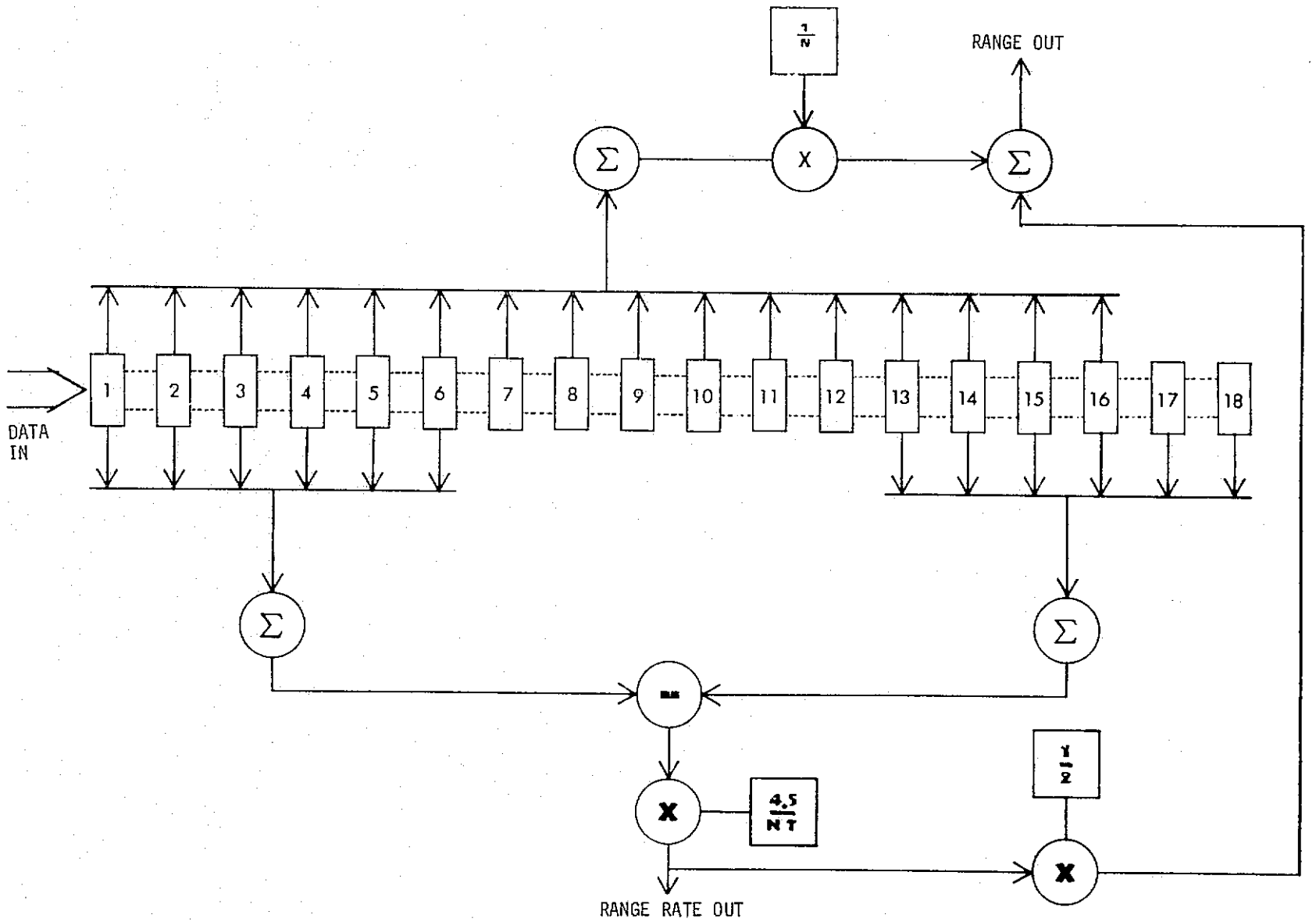

Figure 16. First Candidate Filter Functional Block Diagram

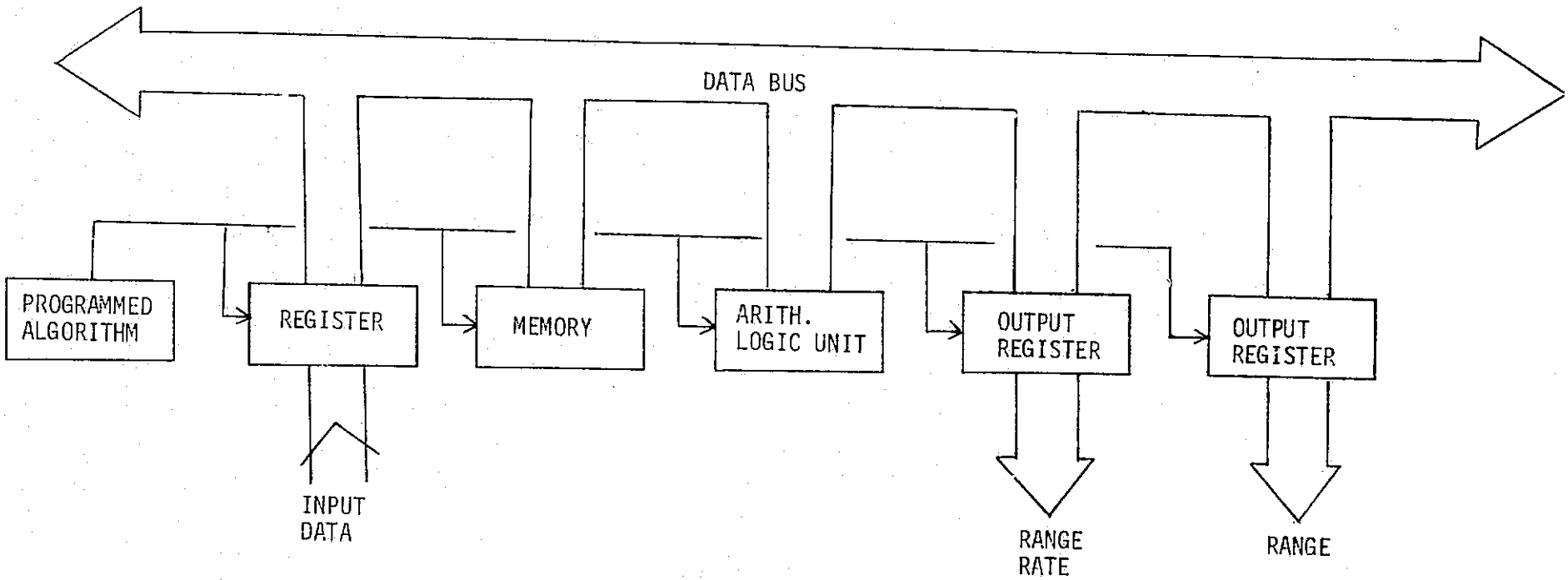

Figure 17. First Candidate Smoothing Filter Architecture

determined by the setting of the switch position on the front panel. The computed range rate is stored in the output range rate register and the range rate data ready line is pulsed. At this time, the range rate is also stored in a scratch pad memory location for later use in updating the smoothed range word.

The memory is connected as a carousel type such that after the eighteenth word, the pointer is automatically reset to word #1. A memory scan operation is begun and words #1 through #16 are summed by the arithmetic logic unit. Division by four is accomplished so that the average word is present in the accumulator. Since the smoothed word is delayed by eight sample times from the incoming data word, a correction factor equal to half the range rate is added or subtracted from the smoothed range word to update the computed range word. This is accomplished by retrieving the range rate word from the scratch pad memory location and either adding or subtracting depending on whether the range rate is increasing or decreasing. This word is stored in the output range register and the range data ready line is pulsed. This completes the operational cycle of the filter and it returns to the "idle" state until the next computation is initiated. A more detailed description of the filter's operation may be had by considering the algorithm which is programmed to operate the filter.

3.1.1 First Candidate Filter Algorithm

A flow diagram for the filter algorithm and its associated circuitry is shown in Figure 18 and 19, respectively. In Figure 19, the numbers in triangles serve to identify the ROM with the associated coding table. The coding which has been programmed in the ROM's is contained in Tables I through IV. Numbers in circles refer to physical layout of the circuit board.

Referring now to Figures 18 and 19, the filter remains in the "idle" state (step zero) until a "GO" signal is detected. The GO signal is derived from the filter's internal clock and has available repetition rates of 2, 4, 8, and 16 Hz depending on the switch setting on the fron panle. This

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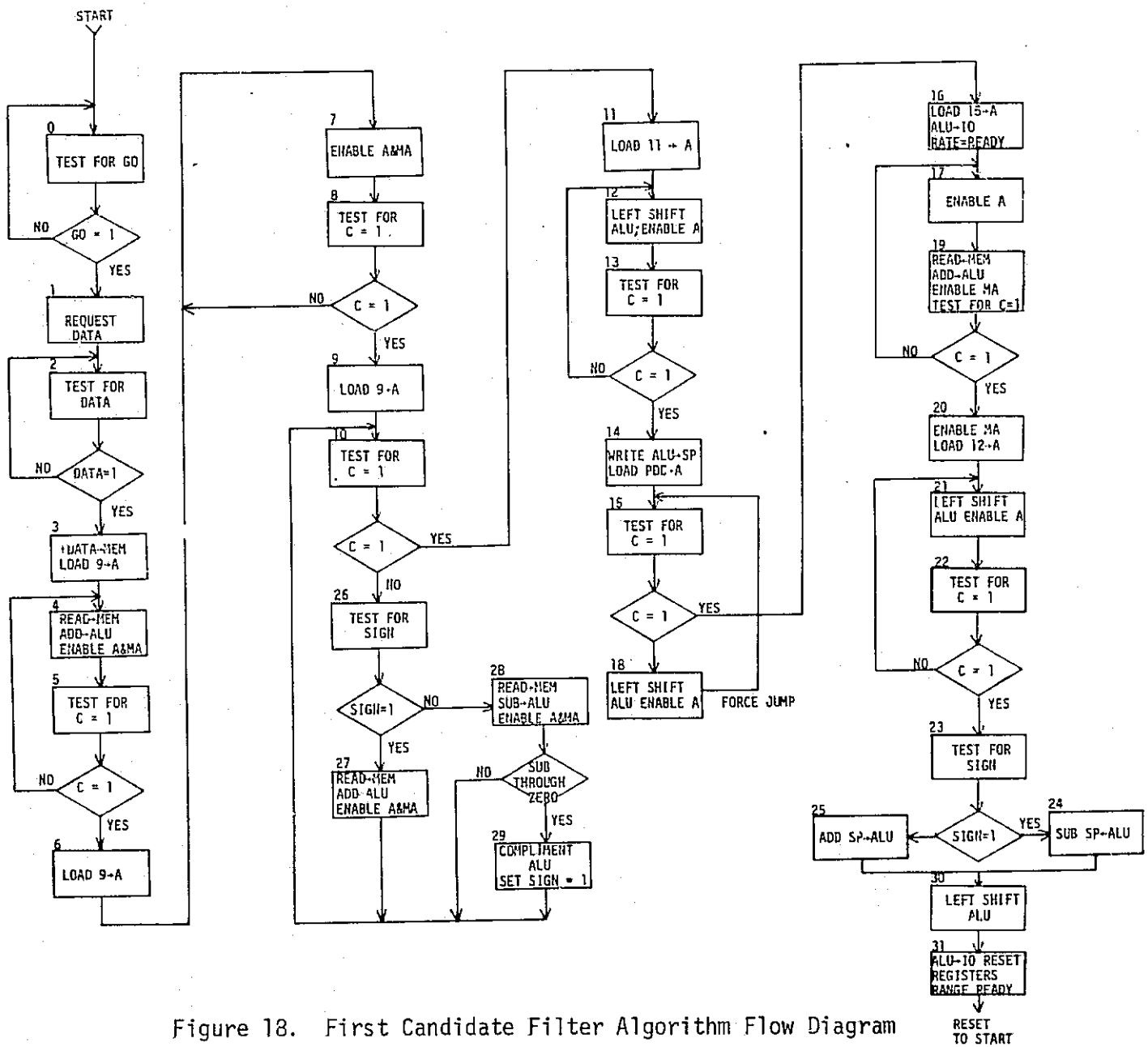

Figure 18. First Candidate Filter Algorithm Flow Diagram

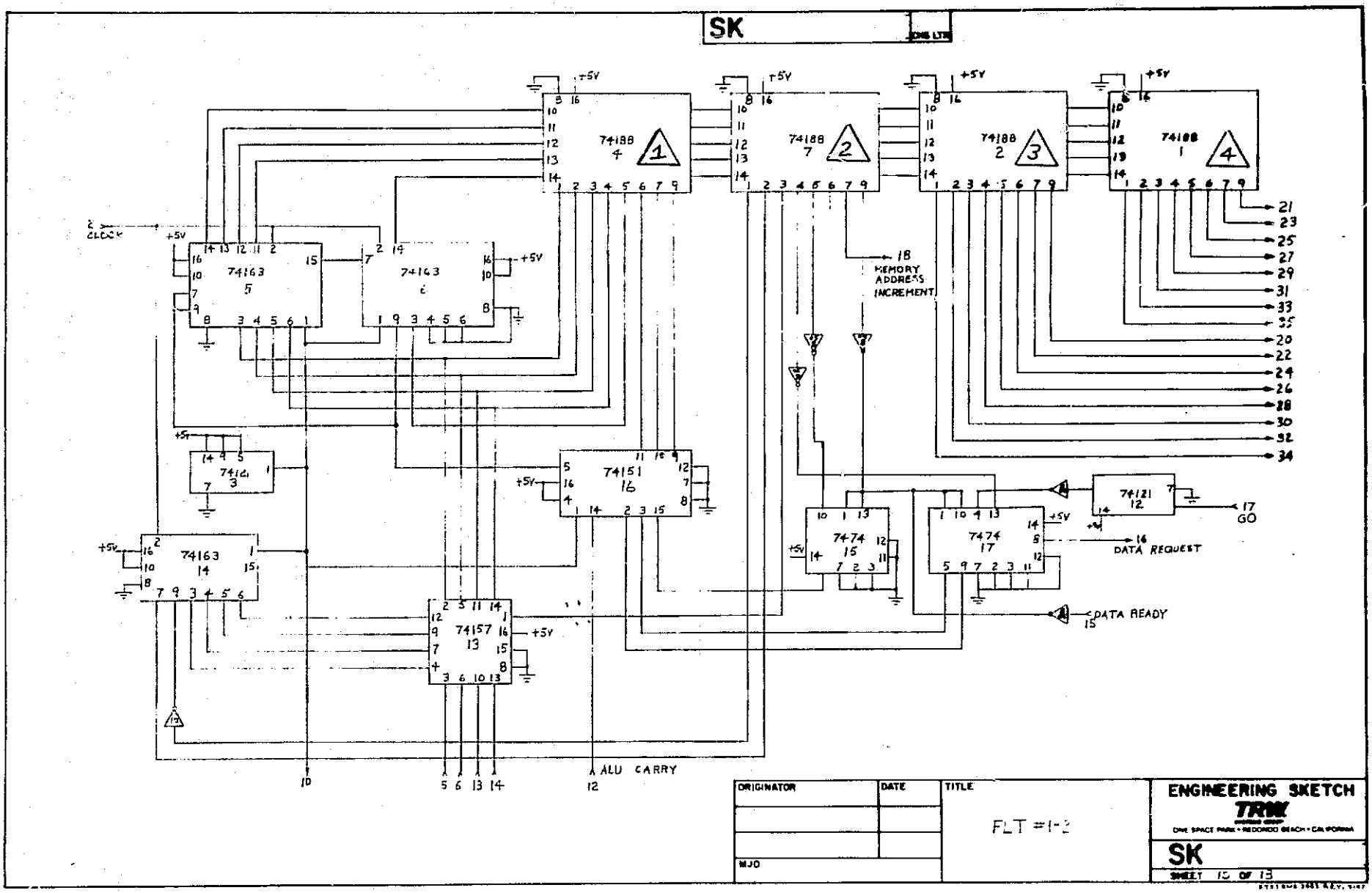

Figure 19. First Candidate Filter Control Circuitry

pulse sets the GO flip/flop (1/2 - 7474) so that Q equals a logic "1". Referring to Table I, ROM outputs O_5, O_6, and O_7 are coded for binary one which dials up position #2 on the 74151 multiplexer. The state of the GO F/F then appears at the "Y" output of the multiplexer. The presence of a logic "1" enables the 74163 counters so that the counters advance to step one on the next clock pulse. Alternatively, the presence of a zero at the "Y" output loads into the counters ROM outputs O_0 through O_4 which, from Table I, are all zero's for step zero.

After detection of the GO signal, the filter advances to state one and the data request line is raised. Referring to Table II, the data request output of ROM #2 becomes a logic "1" which is inverted so that the data request F/F is cleared, thus setting $\overline{Q}$ high. The filter then advances to step two and tests for data. In Table 1, ROM outputs O_5, O_6, and O_7 are seen to be set to binary two. This dials up the third output of the multiplexer which looks at the state of the data F/F. Upon receipt of a "data ready" from the simulator or navigation device, the data ready F/F is set such that Q equals logical "1". This result appears at the "Y" output and the ROM address counter advances the filter to state three on the next clock pulse and the remainder of the algorithm is executed.

Rather than continue with a step by step description of the operation of the algorithm implementation, only specific comments will be made about the function of the remaining components of the circuit.

Using the coding tables and the flow diagram any specific action of the circuit may be determined. The "A" counter is provided to enable the counter to perform the equivalent of a "DO LOOP". For example in step three, the 74157 which is essentially a two-pole switch routes the O_0 through O_4 outputs of ROM #1 to the input of the "A" counters. These ROM outputs are coded for a binary nine which is loaded into the counter. Next, note that in step four the memory is read which places the contents of current data memory location on the data bus and an add command is given

TABLE I

	T_{A_2}	T_{A_1}	T_{A_0}	A_4	A_3	A_2	A_1	A_0
	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
0	0	0	1	0	0	0	0	0
1	0	0	0	0	0	0	0	0
2	0	1	0	0	0	0	1	0
3	0	0	0	0	1	0	0	1
4	0	0	0	0	0	0	0	0
5	0	1	1	0	0	1	0	0
6	0	0	0	0	1	0	0	1
7	0	0	0	0	0	0	0	0
8	0	1	1	0	0	1	1	1
9	0	0	0	0	1	0	0	1
10	0	1	1	1	1	0	1	0
11	0	0	0	0	1	0	1	1
12	0	0	0	0	0	0	0	0
13	0	1	1	0	1	1	0	0
14	0	0	0	0	0	0	0	0
15	0	1	1	1	0	0	1	0
16	0	0	0	0	1	1	1	1
17	1	1	1	1	0	0	1	1
18	1	1	1	0	1	1	1	1
19	0	1	1	1	0	0	0	1
20	0	0	0	0	1	1	0	0
21	0	0	0	0	0	0	0	0
22	0	1	1	1	0	1	0	1
23	1	0	0	1	1	0	0	1
24	1	1	1	1	1	1	1	0
25	1	1	1	1	1	1	1	0
26	1	0	0	1	1	1	0	0
27	1	1	1	0	1	0	1	0
28	1	0	1	0	1	0	1	0
29	1	1	1	0	1	0	1	0
30	0	0	0	0	0	0	0	0
31	0	0	0	0	0	0	0	0

TABLE II

	LOAD "A" 0_0	INCREMENT "A" 0_1	PDC FUNCTION 0_2	DATA REQUEST 0_3	SET SIGN 0_4	INCREMENT "MEM" 0_5	SET COMP 0_6	RESET 0_7
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	0
2	0	0	0	0	0	0	0	0
3	1	0	0	0	0	0	0	0
4	0	1	0	0	0	1	1	0
5	0	0	0	0	0	0	0	0
6	1	0	0	0	0	0	0	0
7	0	1	0	0	0	1	1	0
8	0	0	0	0	0	0	0	0
9	1	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0
11	1	0	0	0	0	0	0	0
12	0	1	0	0	0	1	0	0
13	0	0	0	0	0	0	0	0
14	1	0	1	0	0	0	0	0
15	0	0	0	0	0	0	0	0
16	1	0	0	0	0	0	0	0
17	0	1	0	0	0	0	0	0
18	0	1	0	0	0	0	0	0
19	0	0	0	0	0	1	1	0
20	1	0	0	0	0	1	1	0
21	0	1	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0
23	0	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0
26	0	0	0	0	0	0	0	0
27	0	1	0	0	0	1	1	0
28	0	1	0	0	0	1	1	0
29	0	0	0	0	1	0	0	0
30	0	0	0	0	0	0	0	0
31	0	0	0	0	0	0	0	1

TABLE III

	ALU FUNCTIONS SELECT				RE (MEMORY)	M	INPUT LOAD	LOAD MEMORY
	S_3	S_2	S_1	S_0				
	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
0	0	0	0	0	1	0	1	1
1	0	0	0	0	1	0	1	1
2	0	0	0	0	1	0	1	1
3	0	0	0	0	1	0	0	0
4	0	1	1	0	0	1	1	1
5	0	0	0	0	1	0	1	1
6	0	0	0	0	1	0	1	1
7	0	0	0	0	1	0	1	1
8	0	0	0	0	1	0	1	1
9	0	0	0	0	1	0	1	1
10	0	0	0	0	1	0	1	1
11	0	0	0	0	1	0	1	1
12	0	0	0	0	1	0	1	1
13	0	0	0	0	1	0	1	1
14	0	0	0	0	1	0	1	0
15	0	0	0	0	1	0	1	1
16	0	0	0	0	1	0	1	1
17	0	0	0	0	1	0	1	1
18	0	0	0	0	1	0	1	1
19	0	1	1	0	0	1	1	1
20	0	0	0	0	1	0	1	1
21	0	0	0	0	1	0	1	1
22	0	0	0	0	1	0	1	1
23	0	0	0	0	1	0	1	1
24	1	0	0	1	0	1	1	1
25	0	1	1	0	0	1	1	1
26	0	0	0	0	1	0	1	1
27	0	1	1	0	0	1	1	1
28	1	0	0	1	0	1	1	1
29	1	1	1	1	1	0	1	1
30	0	0	0	0	1	0	1	1
31	0	0	0	0	1	0	1	1

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TABLE IV

	S.C. MEMORY SELECT	ALU OUTPUT	ALU OUT RATE RDY		ALU OUT RANGE RDY		ALU SHIFT	
			S_1	S_0	S_1	S_0	S_1	S_0
	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
0	0	1	0	0	0	0	1	1
1	0	1	0	0	0	0	1	1
2	0	1	0	0	0	0	1	1
3	0	1	0	0	0	0	1	1
4	0	1	0	0	0	0	0	0
5	0	1	0	0	0	0	1	1
6	0	1	0	0	0	0	1	1
7	0	1	0	0	0	0	1	1
8	0	1	0	0	0	0	1	1
9	0	1	0	0	0	0	1	1
10	0	1	0	0	0	0	1	1
11	0	1	0	0	0	0	1	1
12	0	1	0	0	0	0	1	0
13	0	1	0	0	0	0	1	1
14	1	0	0	0	0	0	1	1
15	0	1	0	0	0	0	1	1
16	0	0	1	1	0	0	1	1
17	0	1	0	0	0	0	1	1
18	0	1	0	0	0	0	1	0
19	0	1	0	0	0	0	0	0
20	0	1	0	0	0	0	1	1
21	0	1	0	0	0	0	1	0
22	0	1	0	0	0	0	1	1
23	0	1	0	0	0	0	1	1
24	1	1	0	0	0	0	0	0
25	1	1	0	0	0	0	0	0
26	0	1	0	0	0	0	1	1
27	0	1	0	0	0	0	0	0
28	0	1	0	0	0	0	0	0
29	0	1	0	0	0	0	1	1
30	0	1	0	0	0	0	1	0
31	0	0	0	0	1	1	1	1

to the arithmetic logic unit. These commands originate from ROM's #3 and 4 (see Tables II and IV). At the completion of step four the filter advances to step five and the multiplexer dials up the carry output of the "A" counter. For C = 0, the address for step four is loaded into the two ROM address counters and the filter skips back to step four. This iteration will be performed six times at which time the "A" counter has reached count #15 which raises the carry out line and the filter advances to step #6.

In Figure 19 note that one of the inputs to the multiplexer is the carry output of the arithmetic logic unit. When words 13 through 18 are being subtracted from the accumulated sum of words 1 through 6 subtraction through zero results in the complement of the difference word in the ALU. By "looking" at this carry during the subtract operation the filter detects this condition and complements the difference word so that the magnitude is contained in the ALU. At the same time the "SGN" F/F is set to denote that subtraction through zero has occurred. When the next word is read from memory the SGN = 1 condition directs the filter to simply add the magnitudes of the remaining six words.

3.1.2 First Candidate Filter Operation

The first candidate filter is capable of smoothing over 1, 2, 3, or 4 second intervals. Corresponding sample rates for each of these smoothing intervals are 16, 8, 4, and 2 samples/sec respectively. The different smoothing intervals may be selected by the rotary switch on the from panel. A "DATA" light is included on the front panel and remains in the on state while data is being transfered to the filter. In operation, after the filter is turned the correct smoothed words will be presented at the output after the first eighteen words. This number of data words are required to fill up the memory. For all subsequent operation, a correct smoothed data word will appear at the output for each input word.

3.1.3 First Candidate Filter Performance Data

Verification of the operating characteristics of the filter was made using noisy simulated data. Figures 20 and 21 are data plots for the 8

LSB's of input and output data. Noise was added to the 6 LSB's for both data runs. Since the same recorder was used for both input and output data, the data is not time synchronous but the smoothing properties of the filter are still apparent.

In Figure 20 the data input consisted of noise only and four data runs were made using the four available sampling rates with corresponding sampling time. Using a true RMS voltmeter, the ratio of input to output noise variance was determined to be on the order of 10:1. The data run in Figure 21 is for a noisy ramp input. The simulator was set so that the range word increased three bits per sample time.

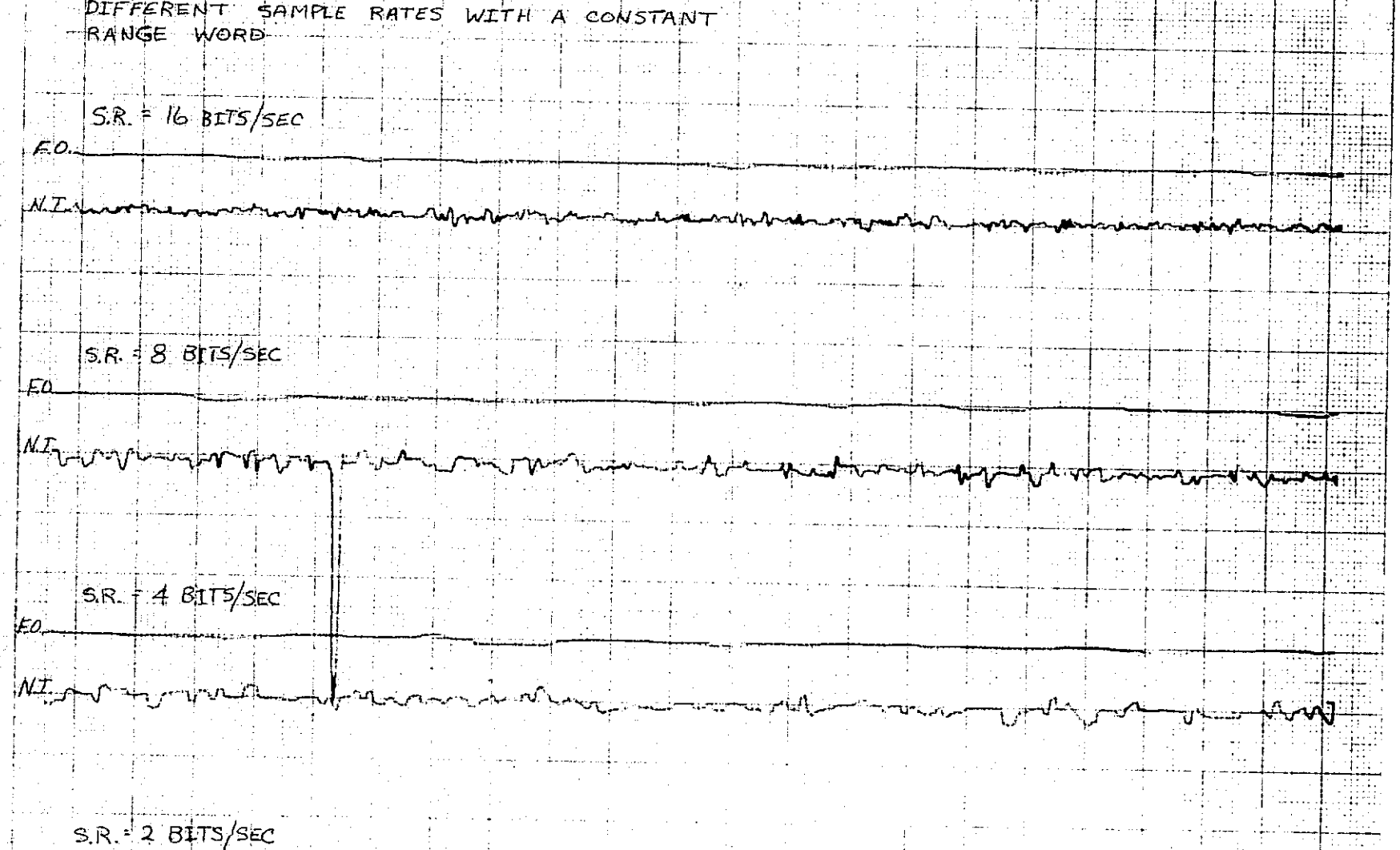

Figure 20. Noise with a Constant Range Word

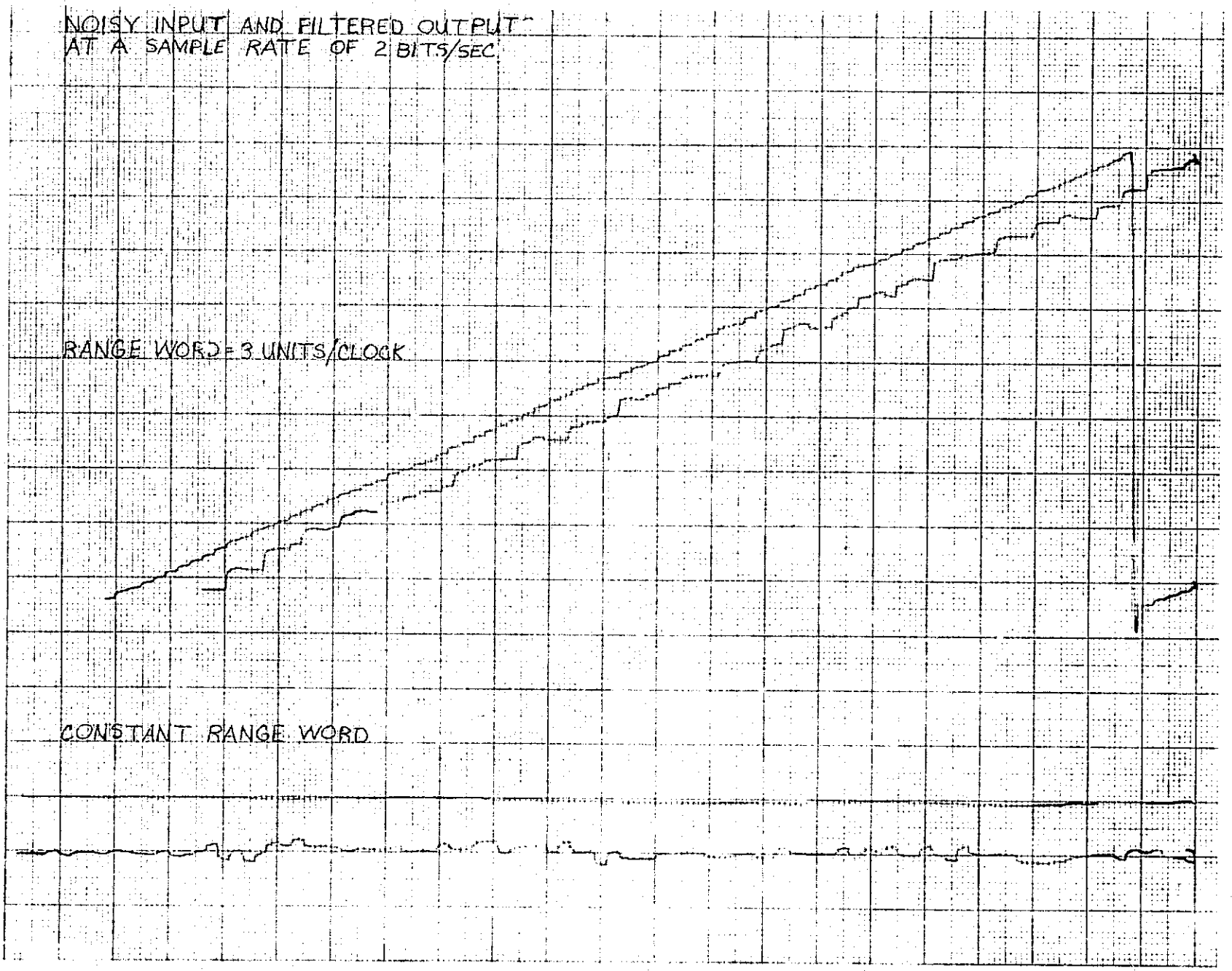

Figure 21. Noisy Input Ramp

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4.0 DIGITAL TRACKING FILTER DESIGN

4.1 SECOND CANDIDATE FILTER

The second candidate filter consists of a digital tracking filter which provides a smoothed range and range rate output. A functional block diagram for this filter is shown in Figure 14. As indicated previously, a multiplexing technique was devised which permits N of these filters to be effectively implemented in parallel. The number N is controlled by switch settings on the front panel and may have values of 2, 4, 8, or 16.

Operation of the filter may be understood by referring to the filter architecture illustrated in Figure 22. The principal components are input-output registers, two 32 word memories, and two arithmetic logic units. The memories are segmented into two blocks of sixteen words each. The memory units are identical with the exception that one memory board contains pull-up resistors for the data bus.

The "DATA & ERROR" memory stores incoming data words in one block of 16 words and error words are stored in the second block. In addition, this second block of memory is used as a "scratch pad." The range memory is used to store computed range words and is the unit which makes it possible to implement the N-parallel filter concept.

Two arithmetic logic units (ALU's) are contained in the design. ALU #1 is utilized strictly for performing addition, subtraction, and division. When computing error words, the results are stored in the error memory as a 15 bit error word with bit #16 (MSB) used as the word sign. When a negative word results, the carry is monitored such that the word is automatically complemented so that the magnitude plus sign is stored. When other add or subtract operations are performed all sixteen bits are used as data.

The second arithmetic logic unit is utilized is primarily as an accumulator which is also capable of left-shift and right-shift operations. Its primary use is to compute the average error word. The filter accomplishes this by scanning the error memory twice. On the first scan, ALU #2 sums up

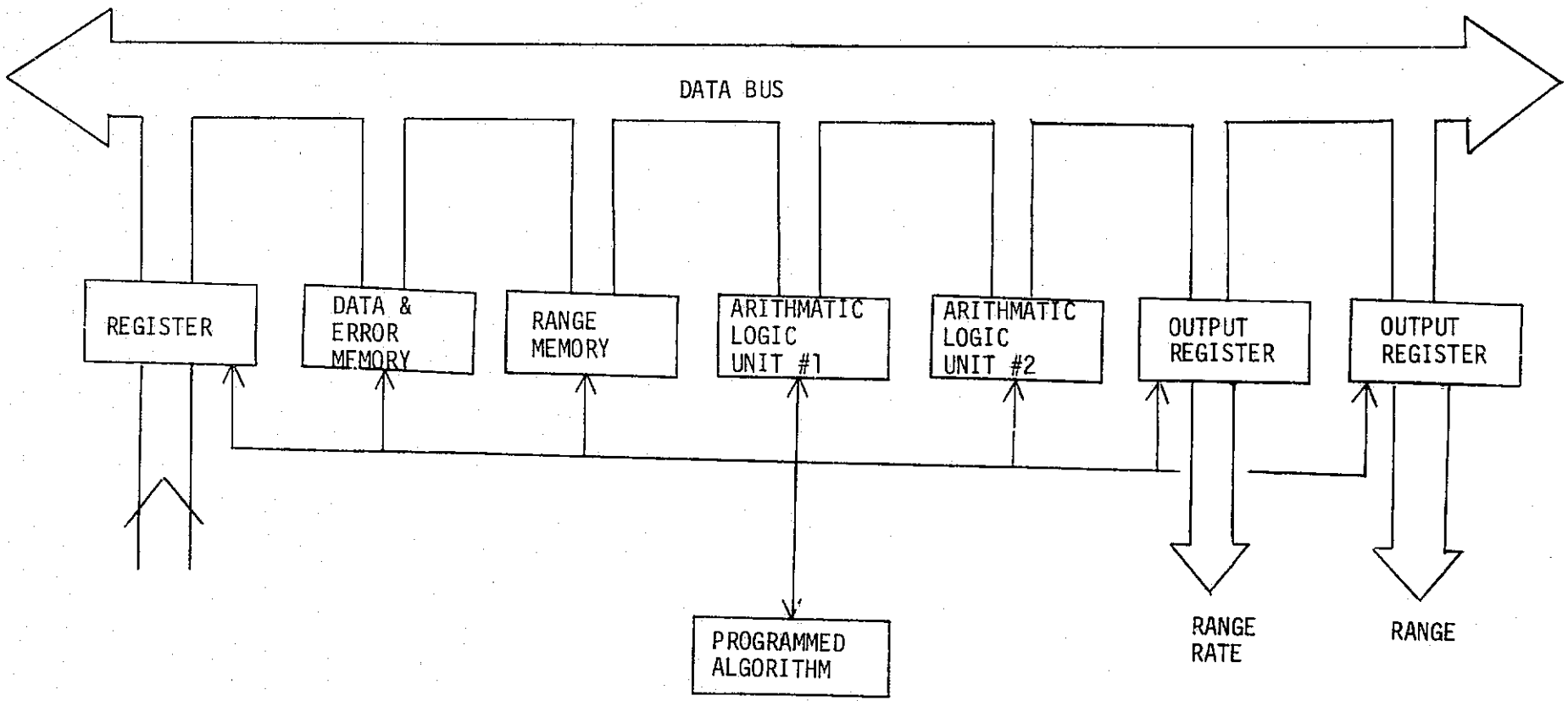

Figure 22. Second Candidate Smoothing Filter Architecture

all of the positive words. On the second pass, the negative words are sequentially subtracted from the accumulated sum. If subtraction through zero occurs, the contents of the accumulator are complemented and the remaining negative words are added to the complemented word. A more detailed understanding of the filter operation may be had by examining the filter algorithm.

4.1.1 Second Candidate Filter Algorithm

A flow diagram for the filter algorithm and its associated circuitry is shown in Figures 23 and 24 and the ROM codes are contained in Tables 5 through 10. Referring to the flow diagram, the operation for data request and data acknowledge is identical to the first filter. In step #3 the current data word is loaded into the input register and also into the data memory and the filter advances to step #4. The previously computed range word is read from the range memory and loaded into the input register on the ALU #1 board. The output of this register forms the "A" input to the 74181's. In steps 5 through 7 an iteration is performed which scans the data memory beginning with the most recent data word and the difference between each data word and the range word is computed. These "error" words are stored in the error memory. When this operation is completed, the address pointer for the data memory will again be at the starting point which is the most recent data word.

The address counter for the data memory is also used for the error memory. The "loop" starting with step #9 and ending with step #24 causes the error memory to be scanned. In this operation the word sign is examined and all of the positive error words are summed by ALU #2. The "loop" beginning with step #11 and ending with steps 28 or 30 subtracts the negative words from the accumulated sum. A complement operation is performed to facilitate subtraction through zero. At the conclusion of this operation, steps 13 or 14 perform a left-shift operation which divides the final sum in the accumulator to produce an error word which has been averaged over N words. This average error word has a value which is N times the range rate.

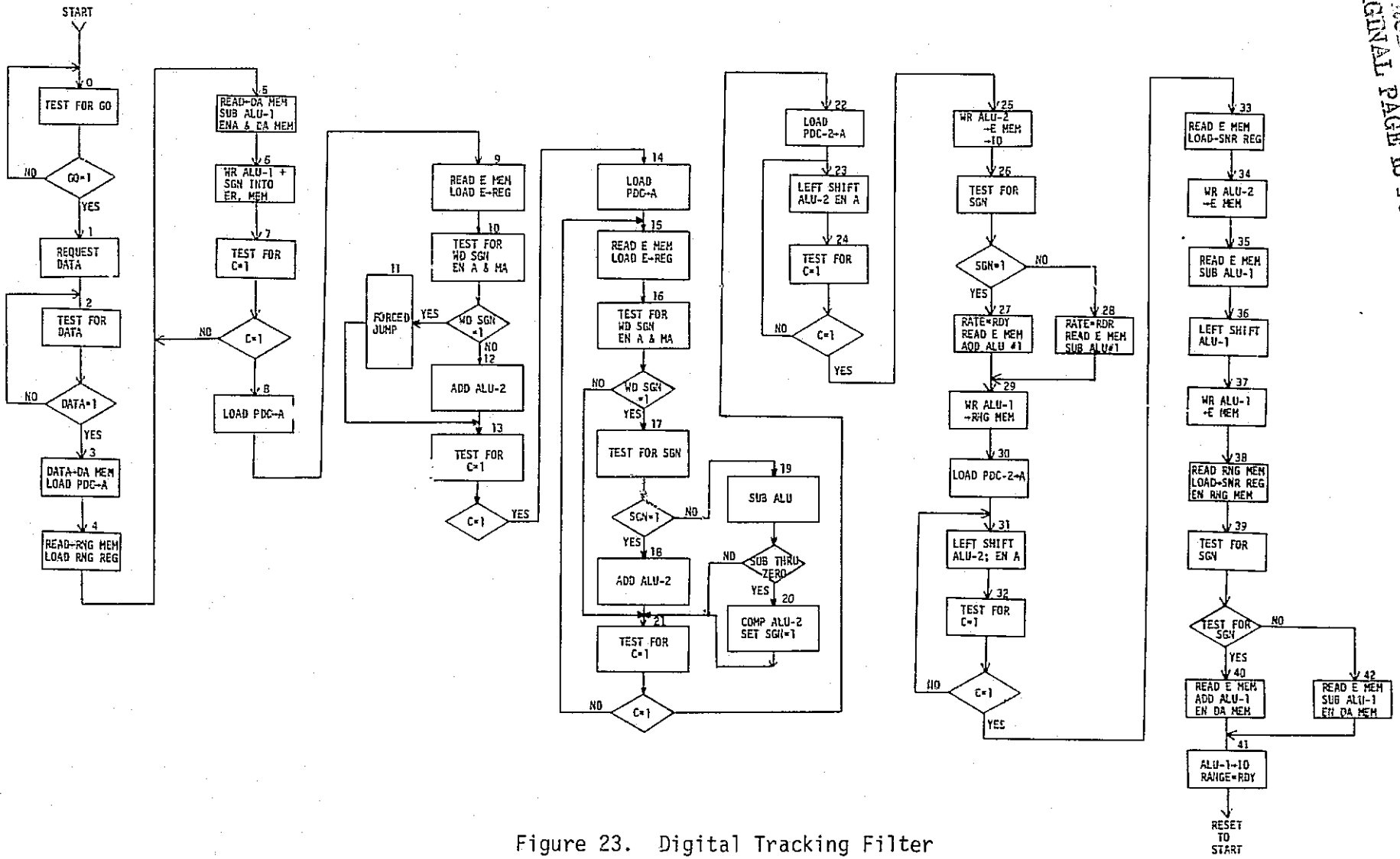

Figure 23. Digital Tracking Filter

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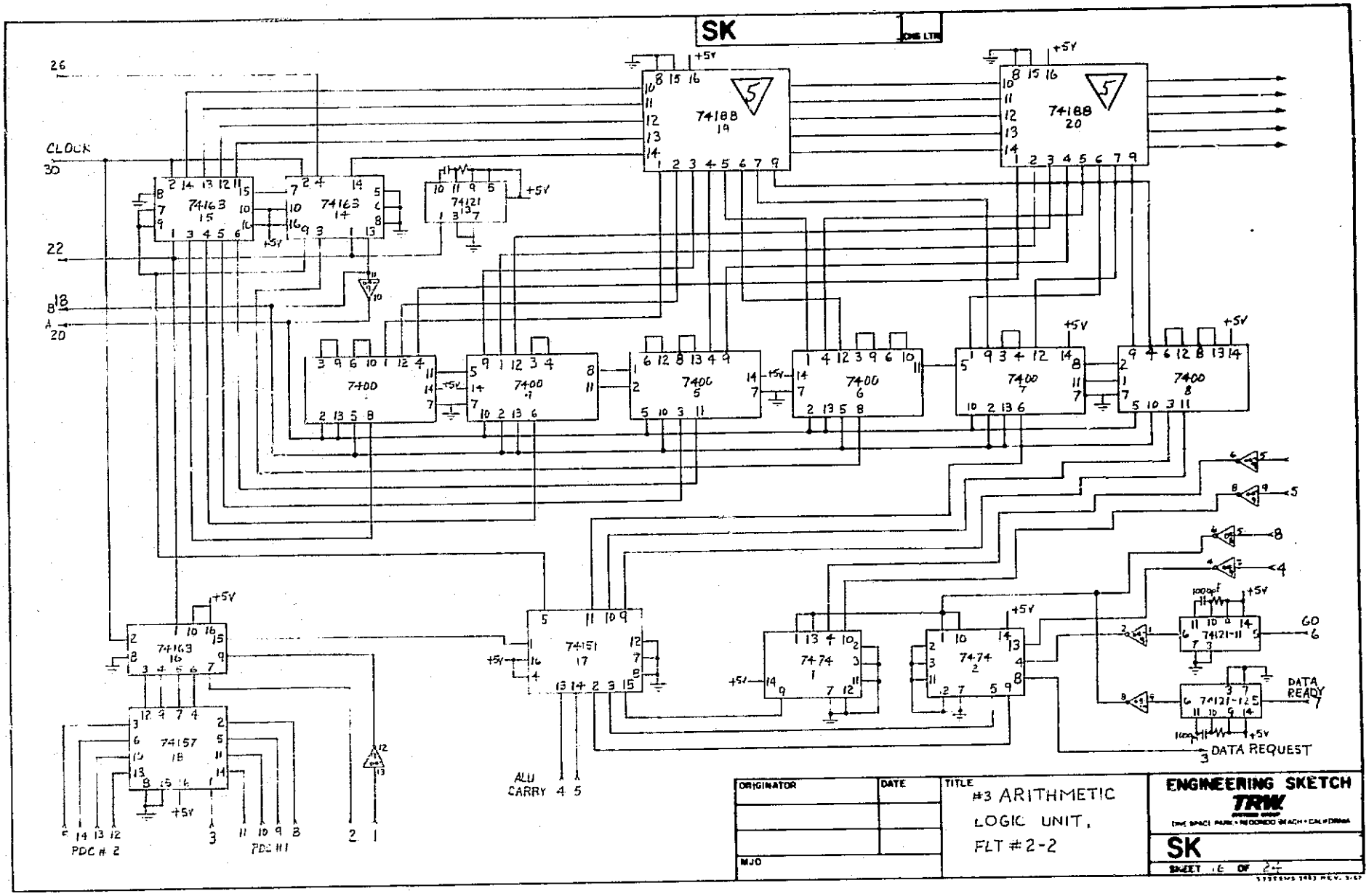

Figure 24. Second Candidate Filter Control Circuitry

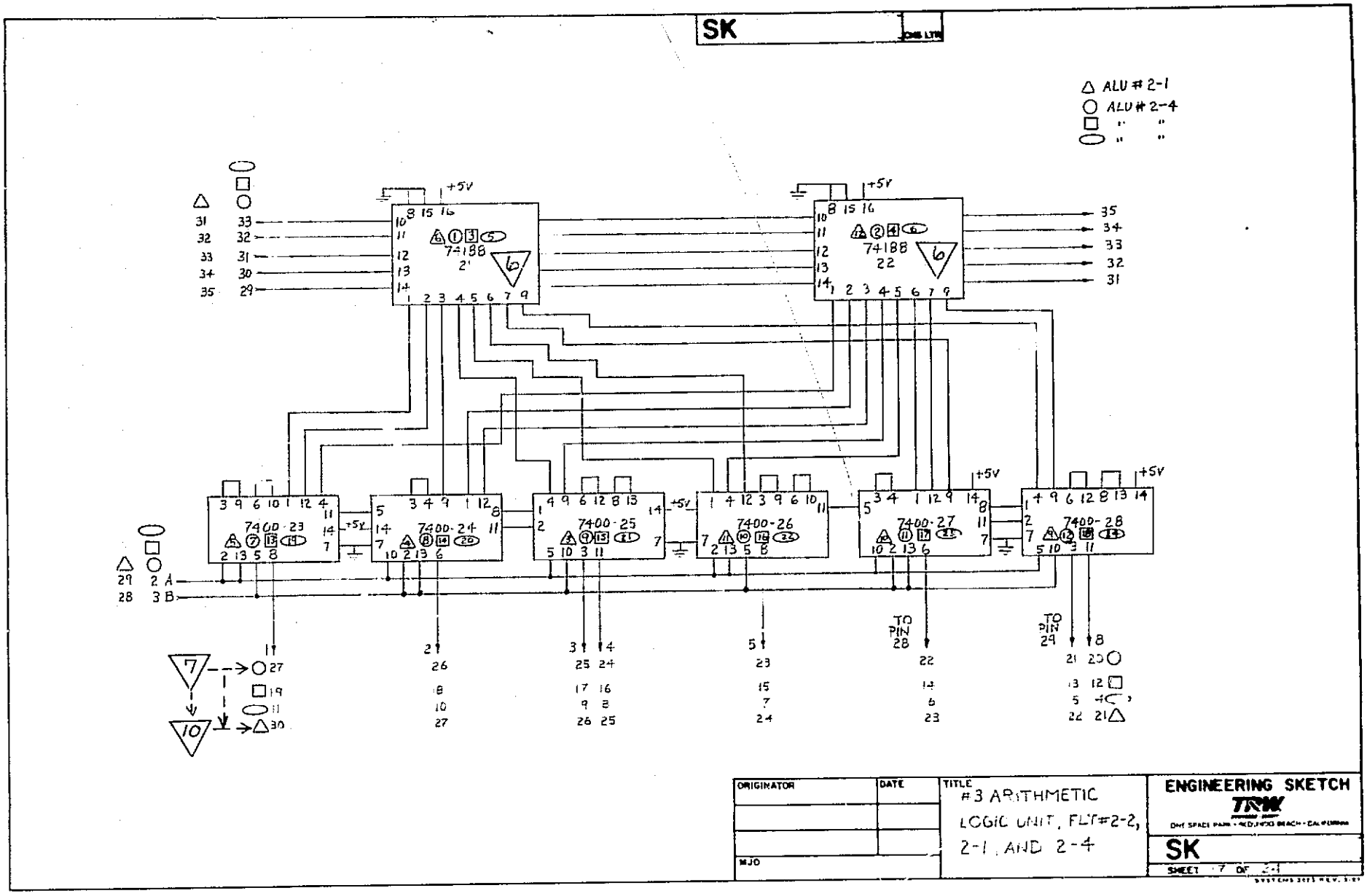

Figure 24a. Second Candidate Filter Control Circuitry

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TABLE V

	T_{A_L}	T_{A_1}	T_{A_0}	A_4	A_3	A_2	A_1	A_0
	0_7	0_6	0_5	0_4	0_3	0_2	0_1	0_0
0	0	0	1	0	0	0	0	0
1	0	0	0	0	0	0	0	0
2	0	1	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	0	0
6	0	0	0	0	0	0	0	0
7	0	1	1	0	0	1	0	1
8	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0
10	1	1	0	0	1	1	0	0
11	1	1	1	0	1	1	0	1
12	0	0	0	0	0	0	0	0
13	0	1	1	0	1	0	0	1
14	0	0	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0
16	1	1	0	1	0	1	0	1
17	1	0	0	1	0	0	1	1
18	1	1	1	1	0	1	0	1
19	1	0	1	1	0	1	0	1
20	0	0	0	0	0	0	0	0
21	0	1	1	0	1	1	1	1
22	0	0	0	0	0	0	0	0
23	0	0	0	0	0	0	0	0
24	0	1	1	1	0	1	1	1
25	0	0	0	0	0	0	0	0
26	1	0	0	1	1	1	0	0
27	1	1	1	1	1	1	0	1
28	0	0	0	0	0	0	0	0
29	0	0	0	0	0	0	0	0
30	0	0	0	0	0	0	0	0
31	0	0	0	0	0	0	0	0
32	0	1	1	1	1	1	1	1
33	0	0	0	0	0	0	0	0
34	0	0	0	0	0	0	0	0
35	0	0	0	0	0	0	0	0
36	0	0	0	0	0	0	0	0
37	0	0	0	0	0	0	0	0
38	0	0	0	0	0	0	0	0
39	1	0	0	0	1	0	0	1
40	0	0	0	0	0	0	0	0
41	0	0	0	0	0	0	0	0
42	1	1	1	0	0	0	0	0

TABLE VI

	RESET 0_7	INCRE. DA&E MEM 0_6	INCRE. RANGE MEM 0_5	SET SIGN 0_4	DATA REQUEST 0_3	PDC FUNCTION 0_2	INCRE "A" 0_1	LOAD "A" 0_0
0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	1
4	0	0	0	0	0	0	0	0
5	0	1	0	0	0	0	1	0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	1
9	0	0	0	0	0	0	0	0
10	0	1	0	0	0	0	1	0
11	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	1
15	0	0	0	0	0	0	0	0
16	0	1	0	0	0	0	1	0
17	0	0	0	0	0	0	0	0
18	0	0	0	0	0	0	0	0
19	0	0	0	0	0	0	0	0
20	0	0	0	1	0	0	0	0
21	0	0	0	0	0	0	0	0
22	0	0	0	0	0	1	0	1
23	0	0	0	0	0	0	1	0
24	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0
26	0	0	0	0	0	0	0	0
27	0	0	0	0	0	0	0	0
28	0	0	0	0	0	0	0	0
29	0	0	0	0	0	0	0	0
30	0	0	0	0	0	1	0	1
31	0	0	0	0	0	0	1	0
32	0	0	0	0	0	0	0	0
33	0	0	0	0	0	0	0	0
34	0	0	0	0	0	0	0	0
35	0	0	0	0	0	0	0	0
36	0	0	0	0	0	0	0	0
37	0	0	0	0	0	0	0	0
38	0	0	1	0	0	0	0	0
39	0	0	0	0	0	0	0	0
40	0	1	0	0	0	0	0	0
41	0	1	0	0	0	0	0	0
42	1	0	0	0	0	0	0	0

TABLE VII

	LOAD MEM 0_7	C.E. (DATA MEM) 0_6	C.E. (E. MEM) 0_5	C.E. (R. MEM) 0_4	INPUT LOAD 0_3	M_1 0_2	ALU-2 CLEAR 0_1	ALU-2 OUTPUT 0_0
0	1	1	1	1	1	0	1	1
1	1	1	1	1	1	0	0	1
2	1	1	1	1	1	0	0	1
3	0	0	1	1	0	0	0	1
4	1	1	1	0	1	0	0	1
5	1	0	1	1	1	1	0	1
6	0	1	0	1	1	0	0	1
7	1	1	1	1	1	0	0	1
8	1	1	1	1	1	0	0	1
9	1	1	0	1	1	0	0	1
10	1	1	1	1	1	0	0	1
11	1	1	1	1	1	0	0	1
12	1	1	1	1	1	0	0	1
13	1	1	1	1	1	0	0	1
14	1	1	1	1	1	0	0	1
15	1	1	0	1	1	0	0	1
16	1	1	1	1	1	0	0	1
17	1	1	1	1	1	0	0	1
18	1	1	1	1	1	0	0	1
19	1	1	1	1	1	0	0	1
20	1	1	1	1	1	0	0	1
21	1	1	1	1	1	0	0	1
22	1	1	1	1	1	0	0	1
23	1	1	1	1	1	0	0	1
24	1	1	1	1	1	0	0	1
25	0	1	0	1	1	0	0	0
26	1	1	1	1	1	0	0	1
27	1	1	0	1	1	1	0	1
28	1	1	0	1	1	1	0	1
29	0	1	1	0	1	0	0	1
30	1	1	1	1	1	0	0	1
31	1	1	1	1	1	0	0	1
32	1	1	1	1	1	0	0	1
33	1	1	0	1	1	0	0	1
34	0	1	0	1	1	0	0	0
35	1	1	0	1	1	1	0	1
36	1	1	1	1	1	0	0	1
37	0	1	0	1	1	0	0	1
38	1	1	1	0	1	0	0	1
39	1	1	1	1	1	0	0	1
40	1	1	0	1	1	1	0	1
41	1	1	0	1	1	1	0	1
42	1	1	1	1	1	0	0	1

TABLE VIII

	ALU-1 FUNCTION SELECT		ALU-1 SHIFT		RNG. REG. LOAD	RATE RDY IO	RNG RDY IO	ALU-1 OUTPUT
	S_3,S_0	S_2,S_1	S_1	S_0				
	0_7	0_6	0_5	0_4	0_3	0_2	0_1	0_0
0	0	0	1	1	0	0	0	1
1	0	0	1	1	0	0	0	1
2	0	0	1	1	0	0	0	1
3	0	0	1	1	0	0	0	1
4	0	0	1	1	1	0	0	1
5	1	0	0	0	0	0	0	1
6	0	0	1	1	0	0	0	0
7	0	0	1	1	0	0	0	1
8	0	0	1	1	0	0	0	1
9	0	0	1	1	0	0	0	1
10	0	0	1	1	0	0	0	1
11	0	0	1	1	0	0	0	1
12	0	0	1	1	0	0	0	1
13	0	0	1	1	0	0	0	1
14	0	0	1	1	0	0	0	1
15	0	0	1	1	0	0	0	1
14	0	0	1	1	0	0	0	1
17	0	0	1	1	0	0	0	1
18	1	0	1	1	0	0	0	1
19	0	0	1	1	0	0	0	1
20	0	0	1	1	0	0	0	1
21	0	0	1	1	0	0	0	1
22	0	0	1	1	0	0	0	1
23	0	0	1	1	0	0	0	1
24	0	0	1	1	0	0	0	1
25	0	0	1	1	0	0	0	1
26	0	0	1	1	0	0	0	1
27	0	1	0	0	0	0	0	1
28	1	0	0	0	0	0	0	1
29	0	0	1	1	0	0	0	0
30	0	0	1	1	0	0	0	1
31	0	0	1	1	0	0	0	1
32	0	0	1	1	0	0	0	1
33	0	0	1	1	1	0	0	1
34	0	0	1	1	0	0	0	1
35	1	0	0	0	0	0	0	1
36	0	0	1	0	0	0	0	1
37	0	0	1	1	0	0	0	0
38	0	0	1	1	1	0	0	1
39	0	0	1	1	0	0	0	0
40	0	1	0	0	0	0	0	1
41	1	0	0	0	0	0	0	1
42	0	0	1	1	0	0	1	0

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TABLE IX

	ALU-2 FUNCTION SELECT					ALU-2 SHIFT		E. REG. LOAD
	S_3	S_2	S_1	S_0	M	S_1	S_0	
	0_7	0_6	0_5	0_4	0_3	0_2	0_1	0_0
0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	1	1	0
2	0	0	0	0	0	1	1	0
3	0	0	0	0	0	1	1	0
4	0	0	0	0	0	1	1	0
5	0	0	0	0	0	1	1	0
6	0	0	0	0	0	1	1	0
7	0	0	0	0	0	1	1	0
8	0	0	0	0	0	1	1	0
9	0	0	0	0	0	1	1	1
10	0	0	0	0	0	1	1	0
11	0	0	0	0	0	1	1	0
12	0	1	1	0	1	0	0	0
13	0	0	0	0	0	1	1	0
14	0	0	0	0	0	1	1	0
15	0	0	0	0	0	1	1	1
16	0	0	0	0	0	1	1	0
17	0	0	0	0	0	1	1	0
18	0	1	1	0	1	0	0	0
19	1	0	0	1	1	0	0	0
20	1	1	1	1	0	0	0	0
21	0	0	0	0	0	1	1	0
22	0	0	0	0	0	1	1	0
23	0	0	0	0	0	1	0	0
24	0	0	0	0	0	1	1	0
25	0	0	0	0	0	1	1	0
26	0	0	0	0	0	1	1	0
27	0	0	0	0	0	1	1	0
28	0	0	0	0	0	1	1	0
29	0	0	0	0	0	1	1	0
30	0	0	0	0	0	1	1	0
31	0	0	0	0	0	1	0	0
32	0	0	0	0	0	1	1	0
33	0	0	0	0	0	1	1	0
34	0	0	0	0	0	1	1	0
35	0	0	0	0	0	1	1	0
36	0	0	0	0	0	1	1	0
37	0	0	0	0	0	1	1	0
38	0	0	0	0	0	1	1	0
39	0	0	0	0	0	1	1	0
40	0	0	0	0	0	1	1	0
41	0	0	0	0	0	1	1	0
42	0	0	0	0	0	1	1	0

TABLE X

	0_7	0_6	0_5	0_4	0_3	0_2	0_1	0_0
					2^6 - ALGO.	D_{16}/C_{n+4}	INVERT CONTROL	
0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
3	0	0	0	0	0	0	0	0
4	0	0	0	0	0	0	0	0
5	0	0	0	0	0	0	1	0
6	0	0	0	0	0	0	0	0
7	0	0	0	0	0	0	0	0
8	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0
10	0	0	0	0	0	0	0	0
11	0	0	0	0	0	0	0	0
12	0	0	0	0	0	0	0	0
13	0	0	0	0	0	0	0	0
14	0	0	0	0	0	0	0	0
15	0	0	0	0	0	0	0	0
16	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	0	0
18	0	0	0	0	0	0	0	0
19	0	0	0	0	0	0	0	0
20	0	0	0	0	0	0	0	0
21	0	0	0	0	0	0	0	0
21	0	0	0	0	0	0	0	0
22	0	0	0	0	0	0	0	0
23	0	0	0	0	0	0	0	0
24	0	0	0	0	0	0	0	0
25	0	0	0	0	0	0	0	0
26	0	0	0	0	0	0	0	0
27	0	0	0	0	0	1	0	0
28	0	0	0	0	0	1	0	0
29	0	0	0	0	0	0	0	0
30	0	0	0	0	0	0	0	0
31	0	0	0	0	0	0	0	0
32	0	0	0	0	0	0	0	0
33	0	0	0	0	0	0	0	0
34	0	0	0	0	0	0	0	0
35	0	0	0	0	0	1	0	0
36	0	0	0	0	0	0	0	0
37	0	0	0	0	0	0	0	0
38	0	0	0	0	0	0	0	0
39	0	0	0	0	1	0	0	0
40	0	0	0	0	1	1	0	0
41	0	0	0	0	0	1	0	0
42	0	0	0	0	0	0	0	0

In steps 17 and 18 this averaged error word is either added or subtracted from the current range word to produce the new range word. This word replaces the old range word in memory. Since the computed range word lags the actual range, a correction factor equal to N-1 x R/2 is added or subtracted from the computed value of range. The remaining steps in the algorithm perform this operation. In this process, steps 31 and 32 perform a divide by N operation which results in the actual range rate R.

In step 38, the range memory is enabled so that the pointer advances to the next memory location. The data and error memory pointer is advanced during step 40 or 41. These memory pointer advances effectively implement the N-parallel filter concept.

4.1.2 Second Candidate Filter Operation

The second candidate filter is capable of smoothing over 1, 2, 3, 4, or 8 second intervals. Control of the smoothing interval is accomplished by varying either the sample rate and/or the number of words N to be used for data smoothing. The sample rate and number of words are determined by switch settings of four rotary switches on the front panel. Sample rate control is determined by the setting of the first switch on the left and its position is independent of the position of the remaining three switches. The remaining three switches control the number of words N and must all be placed in the same position for correct filter operation.

In operation, the filter requires 2N input data words before it begins tracking. After this time, for a ramp input, the filter tracks exactly. For an abrupt step change in the input the filter will again require 2N input words to track the change. This characteristic is inherent in the algorithm. The filter is capable of processing error words of up to 15 bits. Thus extremely large input data words can be tracked in a time frame corresponding to 2N input words.

4.1.3 Second Candidate Filter Performance Data

Verification of the operating characteristics of the filter was made using simulated noisy data. Figure 25 contains data plots for the 8 LSB's of input and output data. Noise was added to the 6 LSB's for each data run. As was indicated previously, the data plots are not time synchronous.

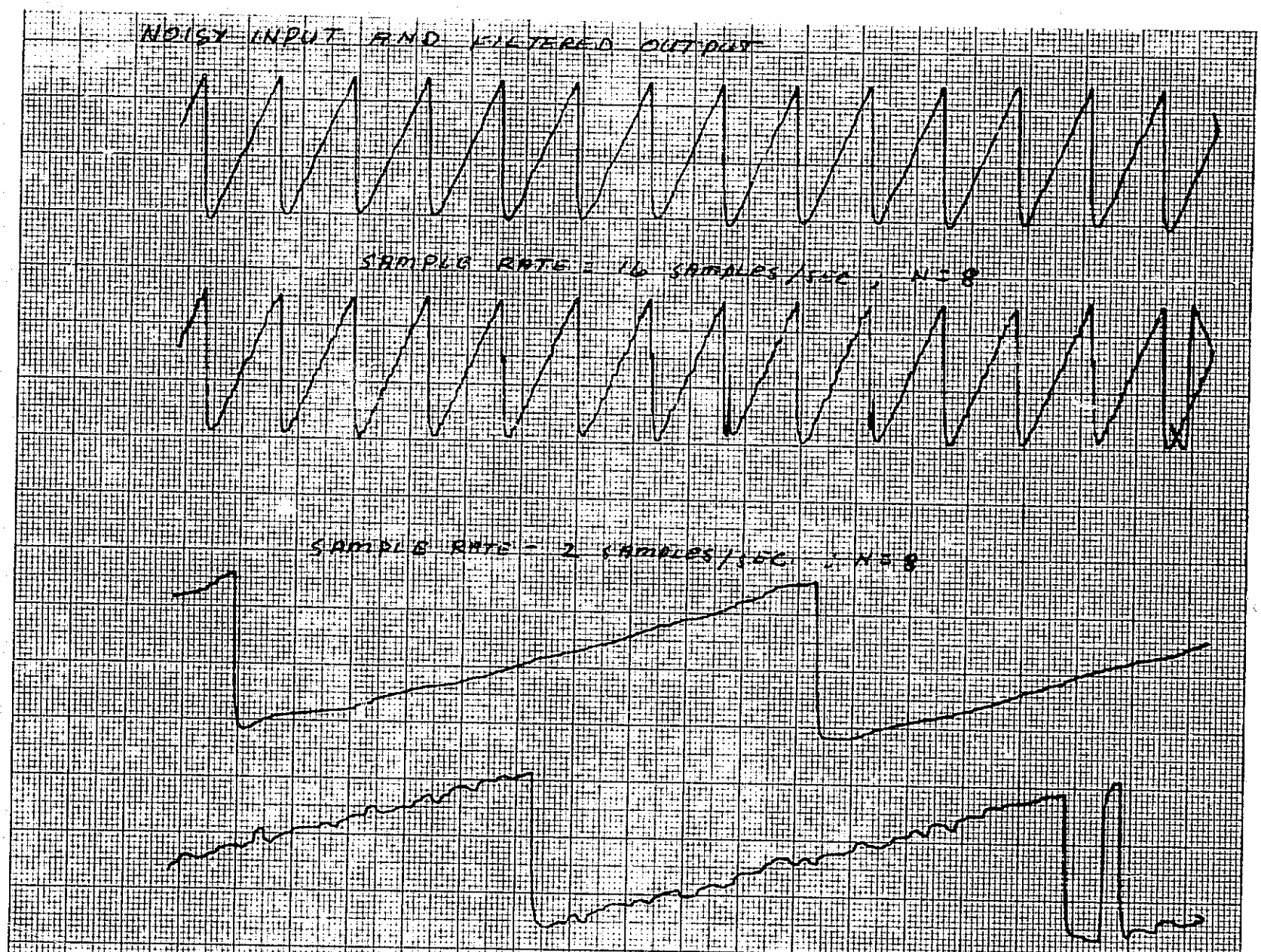

Figure 25. Noisy Input Ramp

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5.0 CONCLUSIONS AND RECOMMENDATIONS

Based on recommendations contained in [5], two different filter types were constructed and evaluated. The results of this evaluation indicates that both filters will result in input/output noise variance reduction on the order of 10:1. In addition, the tracking filter demonstrated the ability to track large (up to a 15 bit word) discontinuities in the input data. The filter will reacquire lock on a data input change consisting of a full 16 bit word at a slightly greater expense in time. A computer aided evaluation will be necessary in order to obtain complete filter performance data.

The implementation of both filters is based on extensive use of micro-programming techniques. Thus, the physical size, power requirements, and reliability of the filters may all be optimized by implementing the filters with commercially available microprocessor integrated circuits. The flow diagrams contained in this report may be implemented directly.

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5. France, H. M., Interim Report - Radar Range Data Signal Enhancement Tracker, TRW Report No. 2553-H004-R0-00, 12 April 1974.

APPENDIX A

TEST SIGNAL GENERATOR

A test signal generator was constructed to supply signals which can be used to evaluate the performance of the two filters. This signal generator supplies, under control of the filter under test, 16 bit range words which change at a rate determined by the setting of front panel switches. Provision is also made for adding random noise to the output digital words.

The overall operation of the test generator can be seen from an inspection of the block diagram of Figure A-1. The range words are generated in an accumulator which increments the range word by a fixed amount upon each receipt of a data sample request from the filter under test. These range words are added to the noise words which are provided by an A/D converter which converts filtered analog noise from an external random noise generator. The resulting noisy range words are placed in an output register where they are available as 16 bit parallel words for use as input data to the filter under test. Two D/A converters are also included to convert both the output range words of the test generator and the output words of the filter to permit analog evaluations of filter performance.

TEST GENERATOR OPERATION

Schematic diagrams for each circuit board in the test generator are shown in Figure A-2 through Figure A-5, as well as an overall interconnection plan as illustrated in Figure A-1.

MAIN ALU BOARD

The main ALU board provides the range word accumulator function. Four 74181 ALU's are connected to associated 74194 shift registers to form a 16 bit accumulator. The range word increment is set by the four switches S_2 through S_5 which are mounted on the front panel. The current range word appears on the output lines of the shift registers and is fed back as one input to the ALU's. The other ALU input is supplied by the range rate switches. When a clock pulse appears on the shift register clock line, the output of the ALU's is transferred to the range word output lines and

held until the next clock pulse. Initial clearing of the accumulator at power turn-on is provided by a one shot. Additional clearing of the accumulator is available from the front panel clear button which is connected so as to ground the clear line of all the shift registers.

A/D CONVERTER BOARD

This board contains an A/D converter for digitizing the output of the analog noise filter as well as facilities for adding the noise words to the output of the range word generator and for holding the resultant noisy data in an output register for use by the filter under test.

When a data request is received from the filter under test, a "start conversion" signal is given to the A/D converter by a one shot which is triggered by the data request. This one shot also clocks the range word accumulator causing it to increment the range word. The six bit noise word output of the A/D converter is added to the current range word in a binary adder formed by four 7483's. The output of the adder is latched in the 74194 output register by a clock pulse generated from the output of the "conversion complete" signal from the A/D converter. With appropriate delays, this same signal is used to clear the input register of the filter under test, to clear the data request flip/flop and to raise the data ready flag to the filter under test.

LOW PASS FILTER BOARD

An active low pass filter is used to filter the output of a random noise generate in order to simulate the low pass characteristic of the range tracking loop of a typical sensor. The active filter uses three operational amplifiers to develop a second order transfer function of the form

$$H(s) = \frac{1}{S^2 + 2\xi\omega_n S + \omega_n^2} \qquad (1)$$

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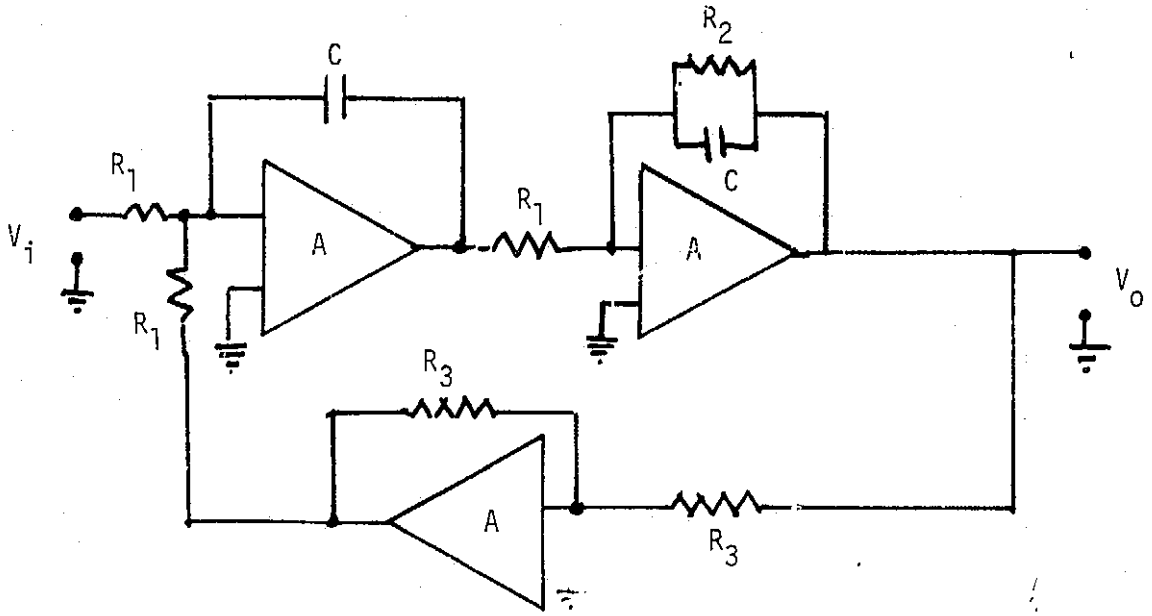
The following sketch shows the configuration used.



The transfer function is:

$$\frac{V_o(S)}{V_i(S)} = \frac{1}{S^2 + \frac{1}{R_2C} S + \frac{1}{R_1^2C^2}} \tag{2}$$

From Equation (1) it can be seen that the natural frequency, ω_n, and the damping factor, ξ, can be controlled independently by appropriate changes in R_1 and R_2. In particular, by comparing Equations (1) and (2):

$$\omega_n = \frac{1}{R_1C_1}$$

$$\xi = \frac{R_1}{2R_2} \tag{3}$$

The values selected for C, R_1 and R_2 in the test generator give $\omega_n = 62.5$ rad/sec. and $\xi = 0.67$. Other values are readily obtained by changing R_1 and R_2 appropriately.

D/A CONVERTER BOARD

It is often convenient to observe to the performance of the filter under test by means of an analog plot of the filtered and unfiltered range words. The D/A converter board contains two separate eight bit D/A converters for this purpose. Each converter is connected to the eight least significant bits of the range word being converted. Since the noise fluctuations are contained in the first six bits of the test words, conversion of the lower eight bits is sufficient to observe the behavior of the filter. If the generated range word is constantly increasing, the output of the D/A converter will reset itself after every change in range of 2^8 bits. The use of two converters permits simultaneous comparison of the filtered and unfiltered data.

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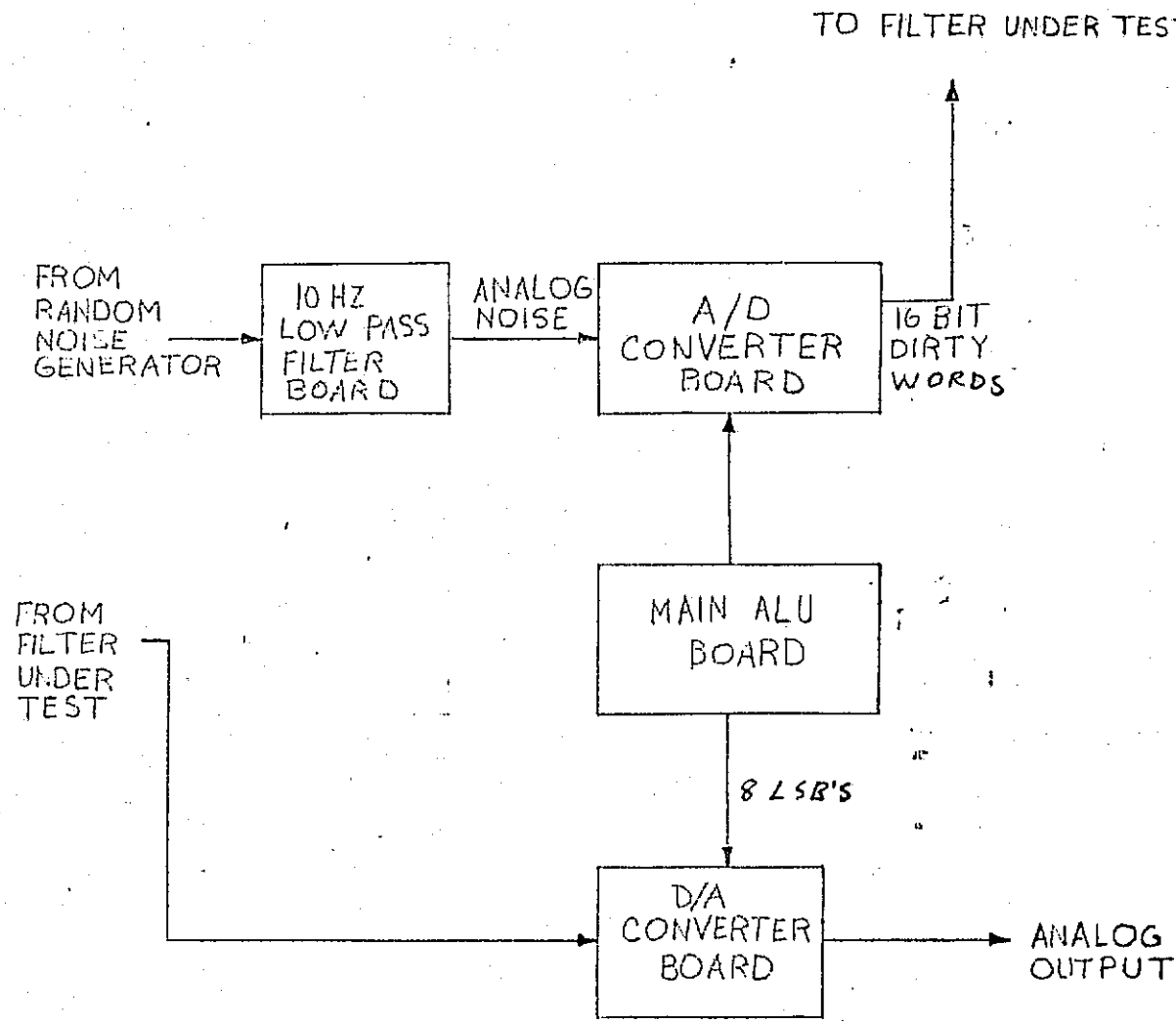

ORIGINATOR	DATE	TITLE
MJO		Figure A-1. Test Signal Generator Block Diagram

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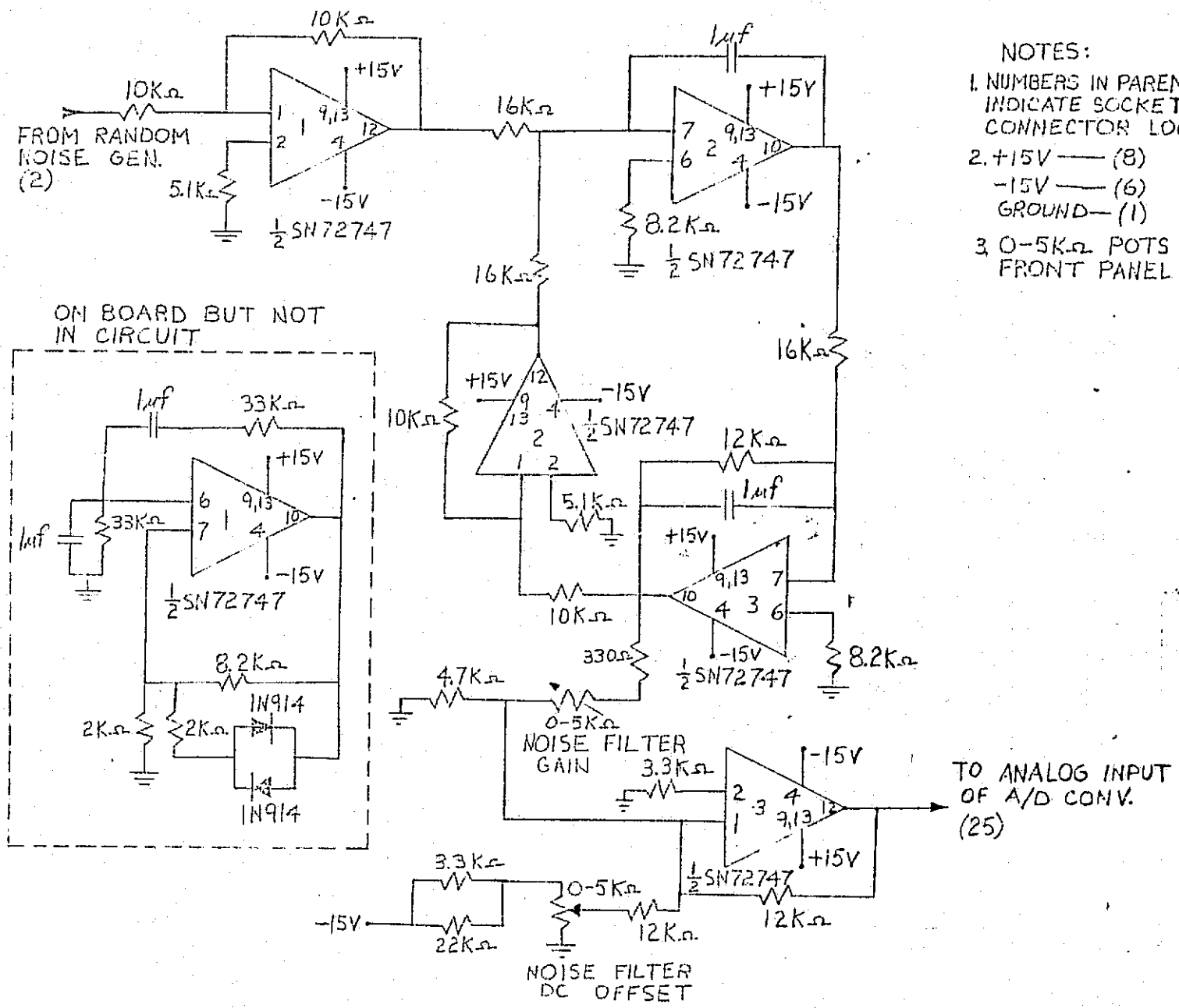


NOTES:

1. NUMBERS IN PARENTHESIS INDICATE SOCKET CONNECTOR LOCATION
2. +15V —— (8)
   -15V —— (6)
   GROUND — (1)
3. 0-5KΩ POTS ON FRONT PANEL

ORIGINATOR	DATE	TITLE
		Figure A-2. 10 Hz Low Pass Filter

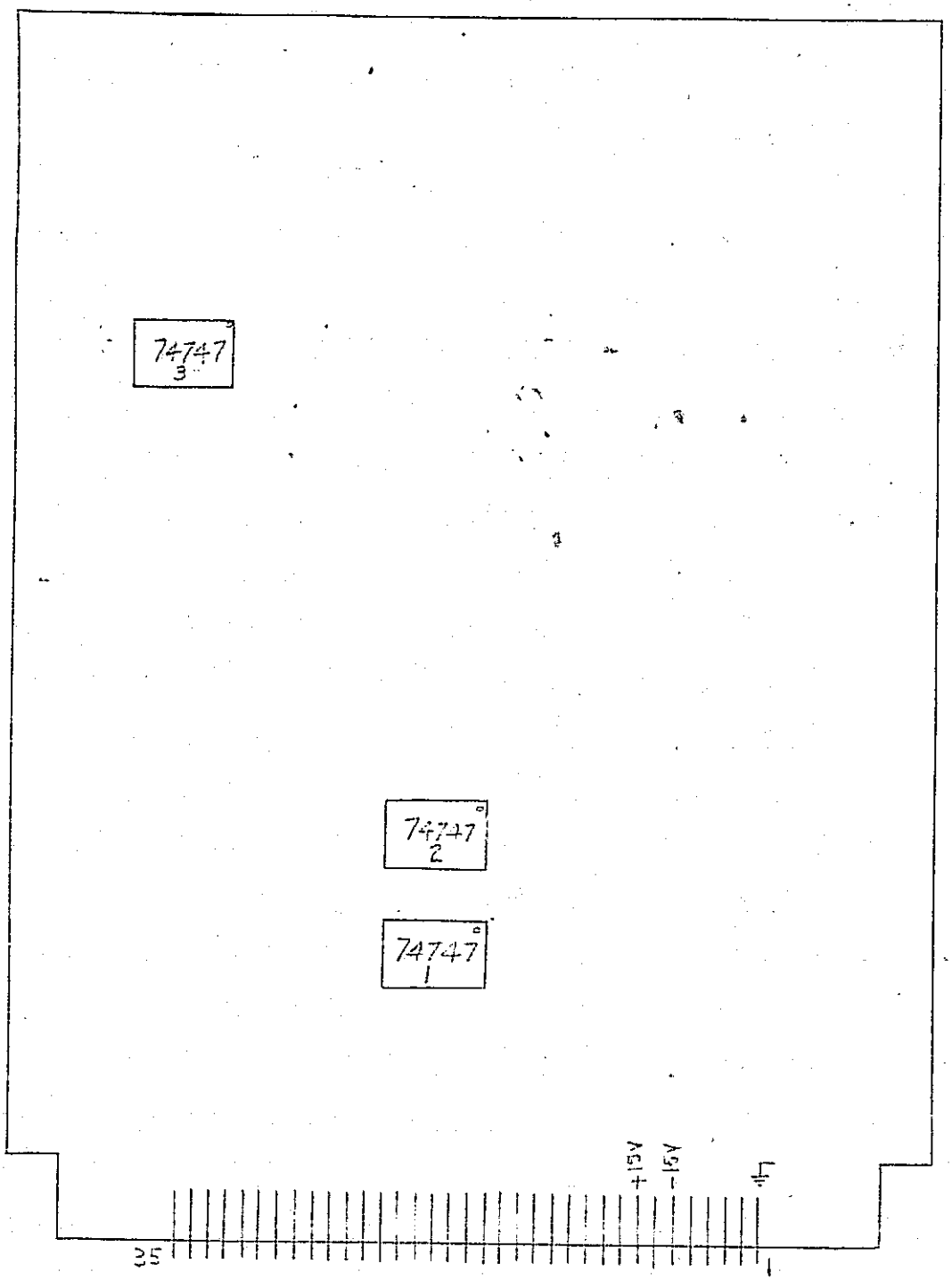
ENGINEERING SKETCH

SK

SHEET 2 OF 2

A-7

SYSTEMS 323 REV. 5-67



ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		Figure A-2a. 10 Hz Low Pass Filter Board	TRW
MJO			SK
			SHEET OF

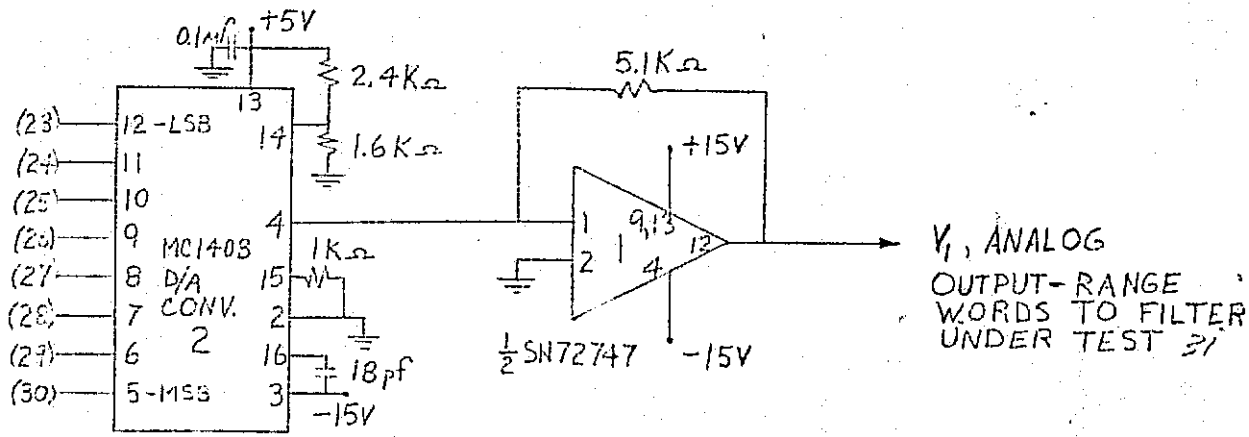
SK

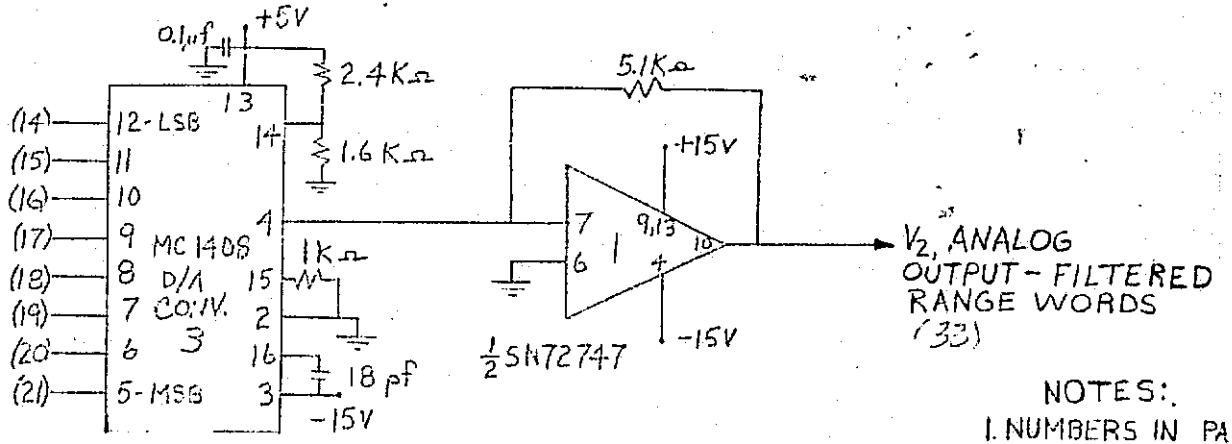
CHG LTR

SYSTEMS 5-3 REV. 5-67

SK

CHG LTR





NOTES:

1. NUMBERS IN PARENTHESIS INDICATE SOCKET CONNECTOR LOCATION
2. +5V —— (22)
   GROUND — (1)
   +15V —— (33)
   -15V —— 37
   GROUND FOR ±15V SUPPLY

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

ORIGINATOR	DATE	TITLE
MJO		Figure A-3. D/A Converter

ENGINEERING SKETCH

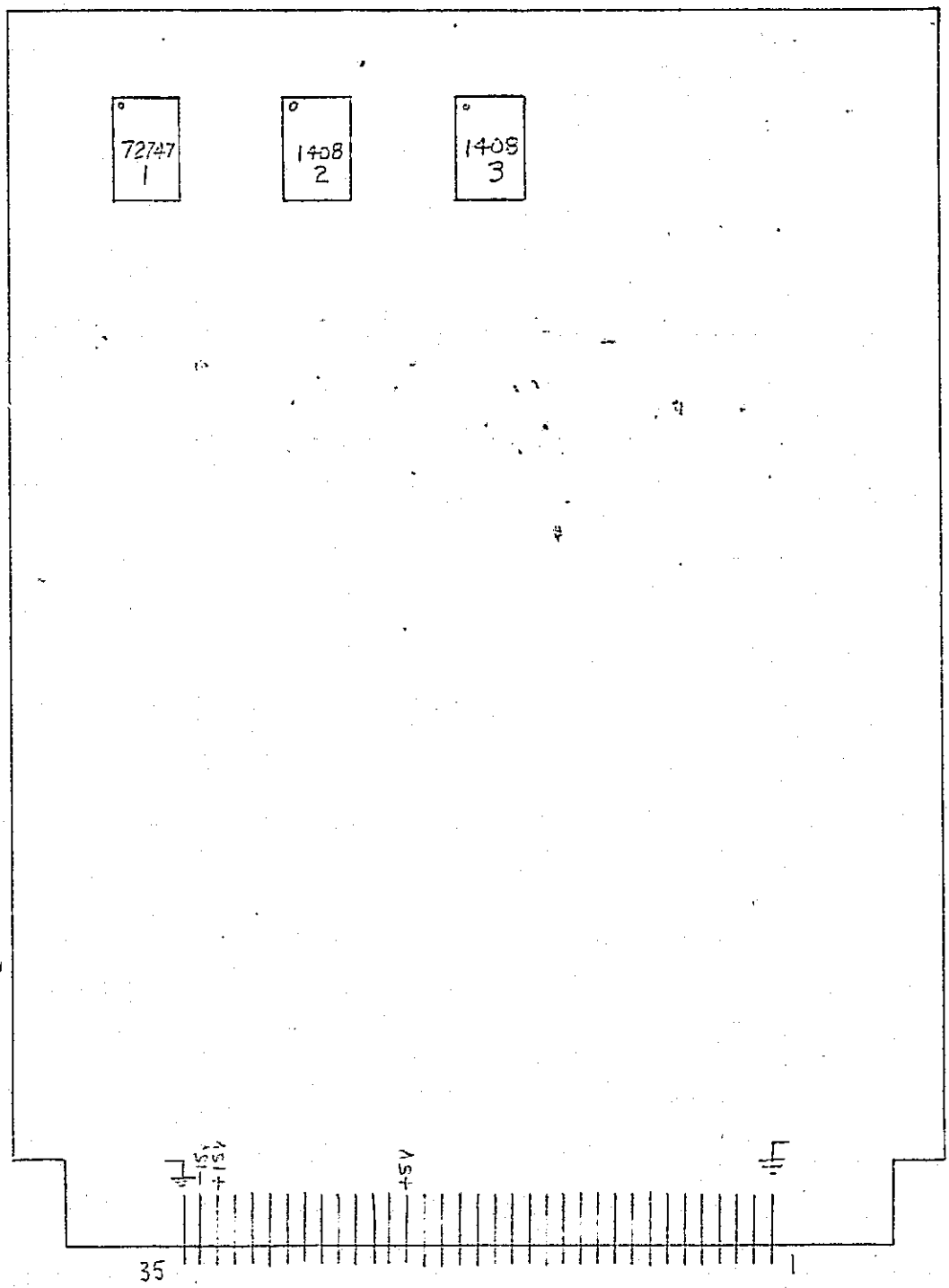
TRW

ONE SPACE PARK • REDONDO BEACH CALIFORNIA

SK

SHEET 3 OF 5

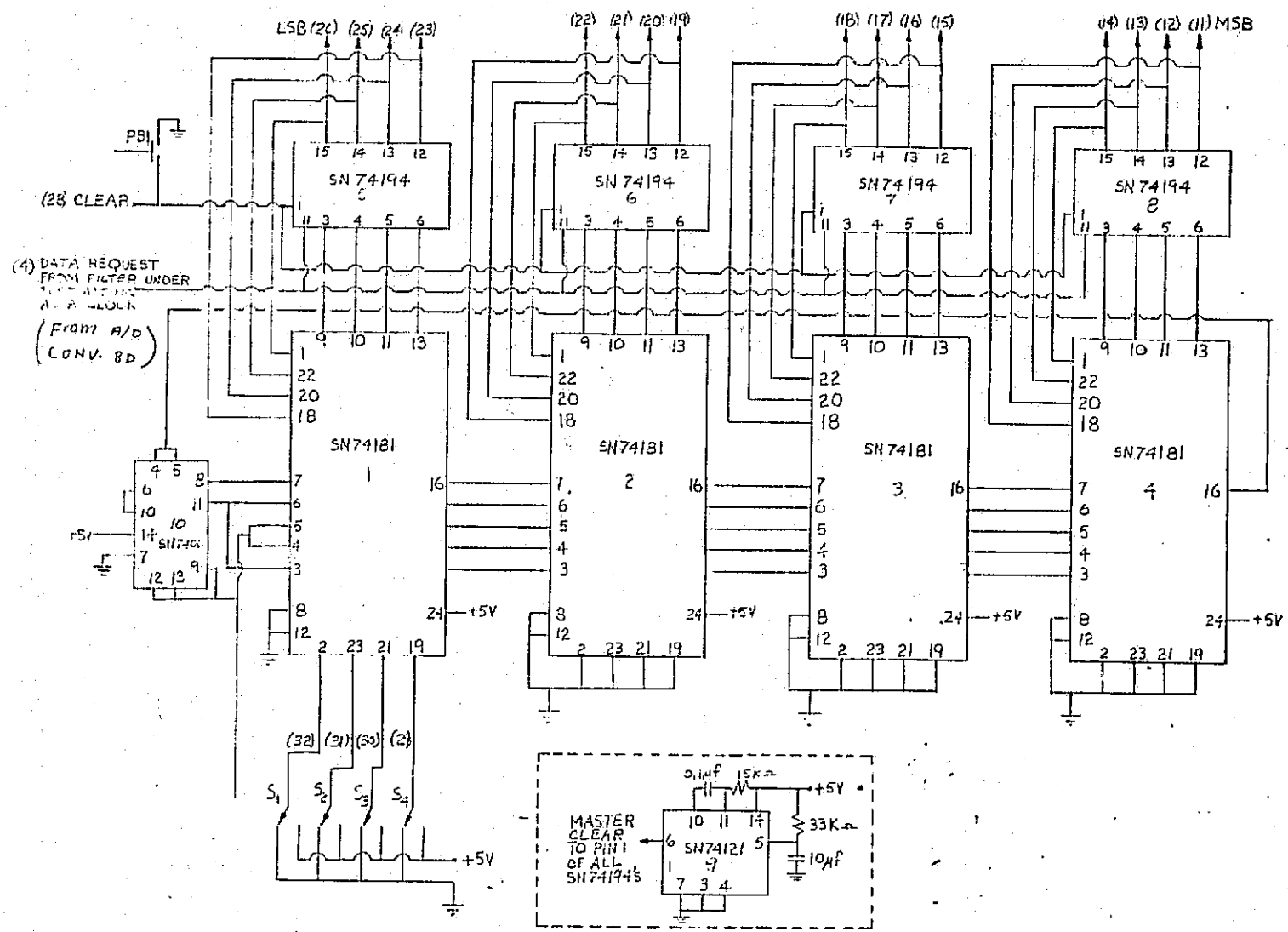
SYSTEMS 523 REV. 5-67



CHG LTR

SK

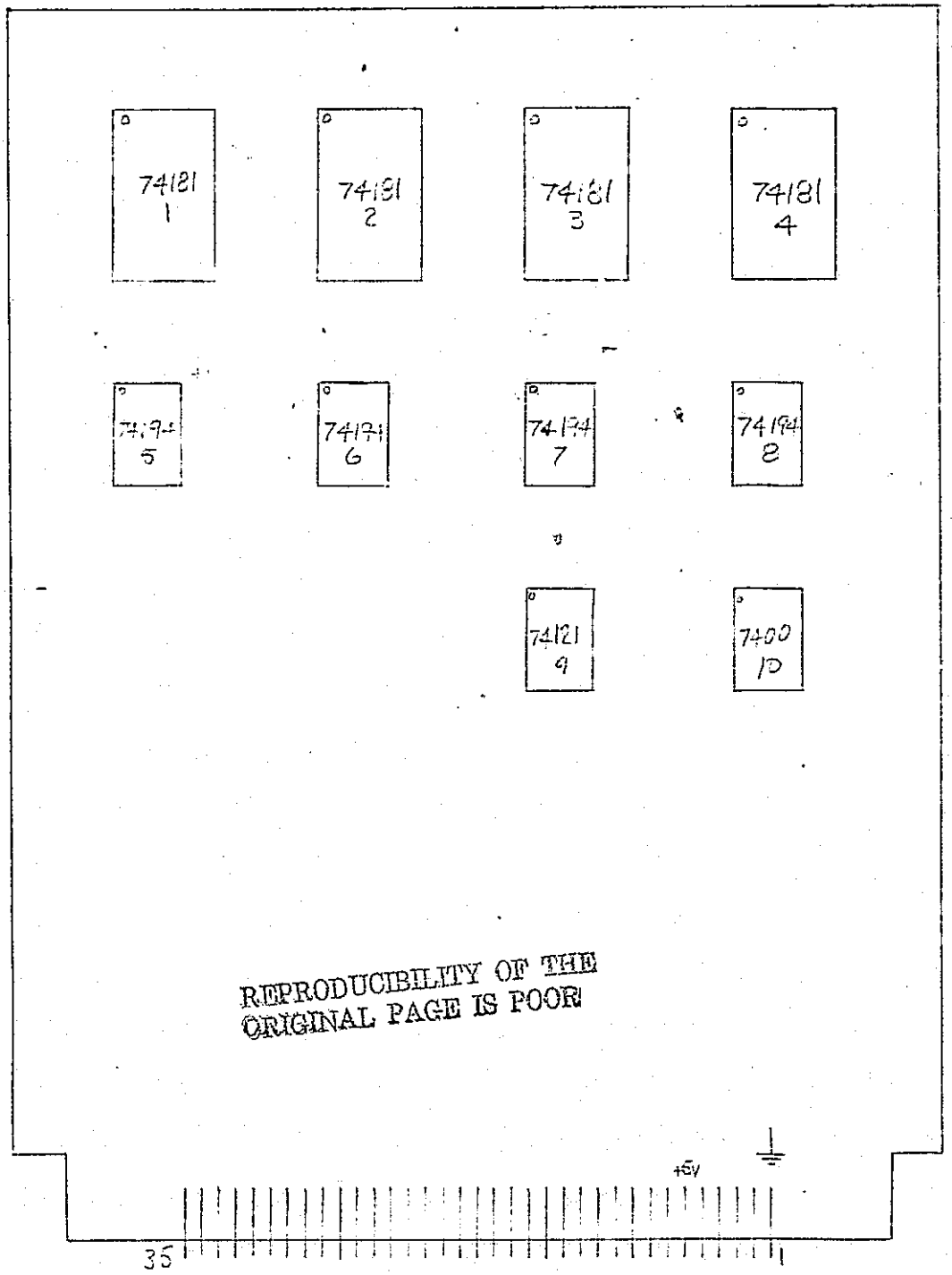
ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		Figure A-3a. D/A Converter Board	TRW ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
			SK
MJO			SHEET OF



NOTES:

1. ON ALL SN74194's PINS 2,7,8 CONNECTED TO GROUND; PINS 9,10, F16 TO +5V
2. NUMBERS IN PARENTHESIS INDICATE SOCKET CONNECTOR LOCATION
3. ALL SWITCHES ON FRONT PANEL.
4. GROUND — (1)
   +5V — (6)

ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH • CALIFORNIA
		Figure A-4. Main ALU	SK
MJO			SHEET 4 OF 5



REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

CHG LTR

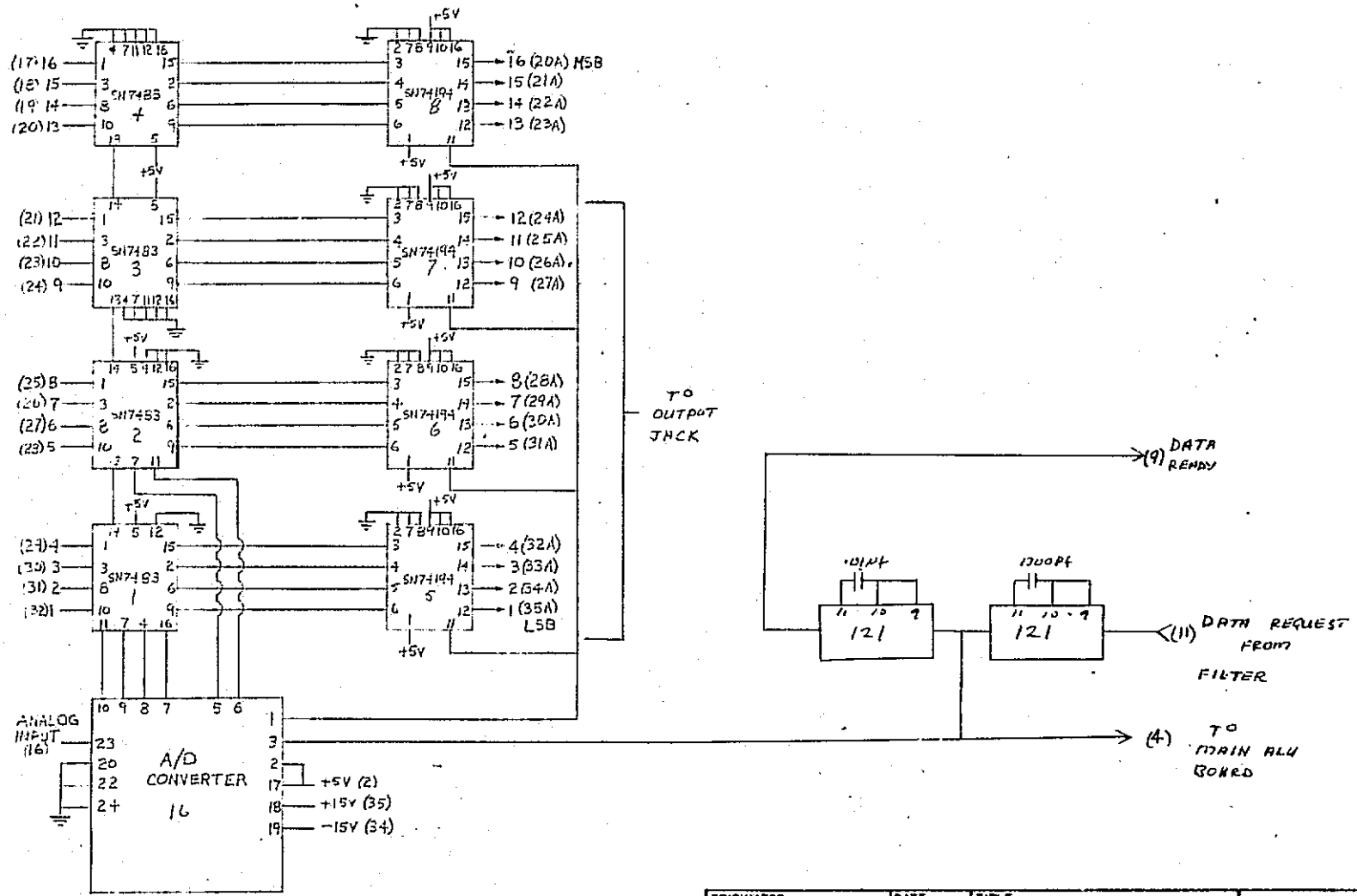
SK

ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		Figure A-4a. Main ALU Board	TRW ONE SPACE PARK • REDONDO BEACH CALIFORNIA
MJO			SK SHEET OF

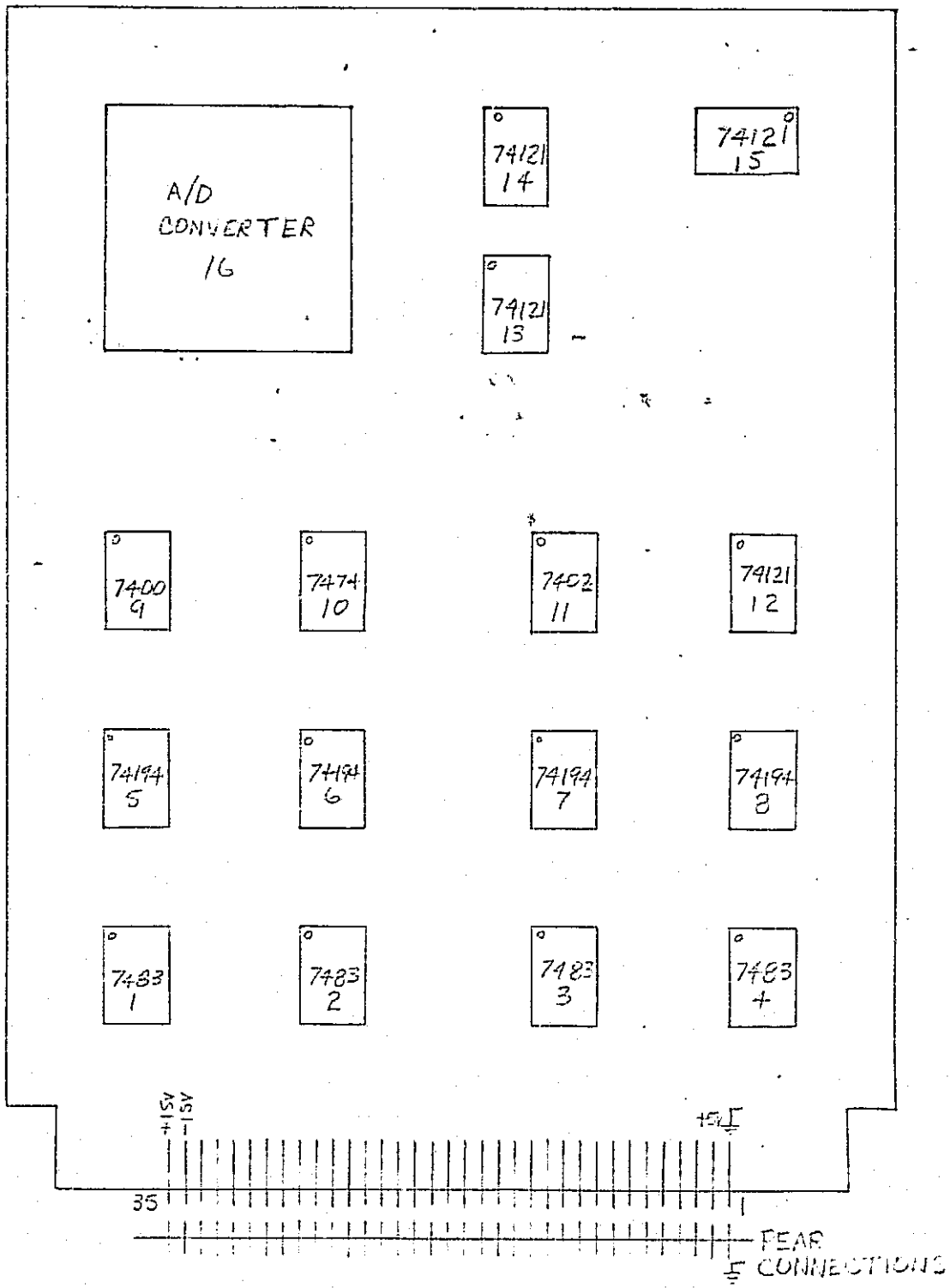
SYSTEMS 223 REV. 3-67

SK

CHG LTR



ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		Figure A-5. A/D Converter	TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH • CALIFORNIA
MJO			SK
			SHEET 5 OF 5



ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		Figure A-5a. A/D Converter Board	TRW ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
MJO			SK
			SHEET OF

SYSTEMS 523 REV. 5-67

APPENDIX B
CASCADED AVERAGING FILTER

J1

PIN NO.		FUNCTION
1	Parallel Input Data	-1 - MSB
2		-2
3		-3
4		-4
5		-5
6		-6
7		-7
8		-8
9		-9
10		-10
11		-11
12		-12
13		-13
14		-14
15		-15
16	Parallel Input Data	-16
17		
18		
19	Clock Out	
20		
21	Shift Left Serial Input	
22	Shift RT Serial Input	
23	Data Request	
24		
25	Data Ready	
26		
27	Clear	
28		
29	S0	
30		
31	S1	
32	6nd	
33		
34		

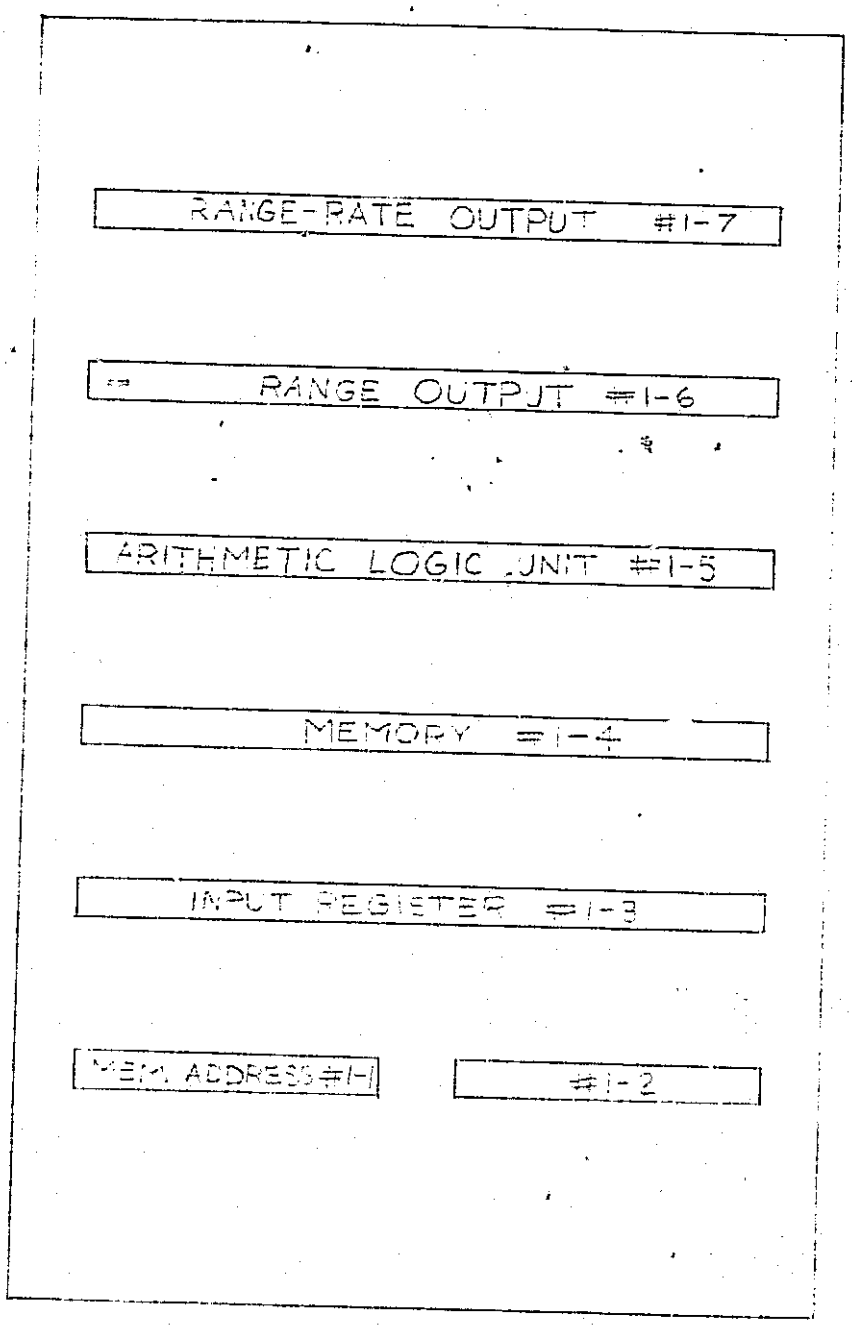
J2

PIN NO.		FUNCTION
1	Parallel Range Rate Out	-1 - LSB
2		
3		
4		
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16	Parallel Range Rate Out	-16 - MSB
17	Parallel Range Out	-1 - LSB
18		
19		
20		
21		
22		
23		
24		
25		
26		
27		
28		
29		
30		
31		
32	Parallel Range Out	-16 - MSB
33	Range Ready	
34	Range Rate Ready	

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

CHG LTR

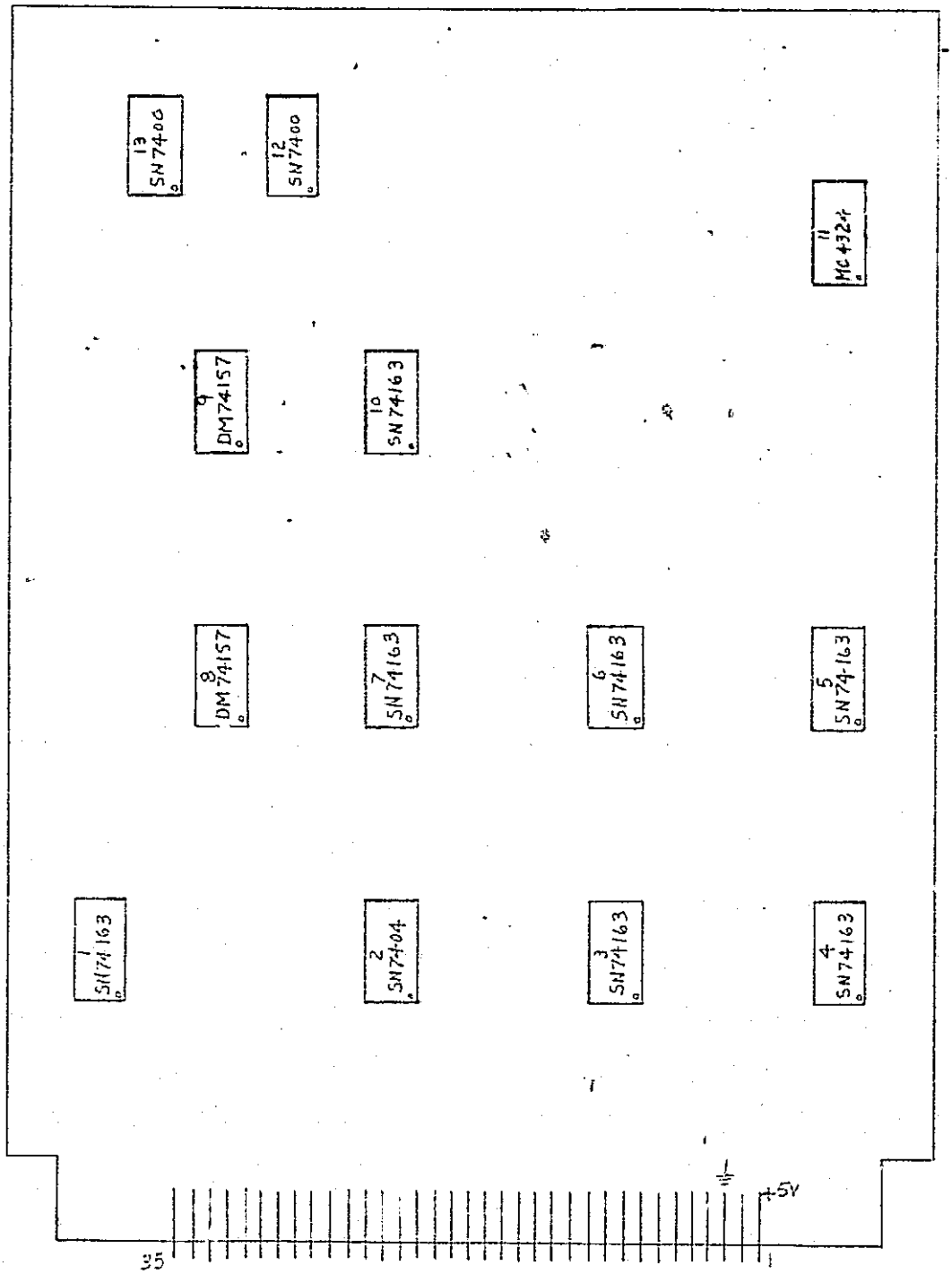
SK



REAR VIEW

ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		FILTER #1 FRONT LOCATION	TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
MJO			SK
			SHEET OF

SYSTEMS 523 REV. 5-67

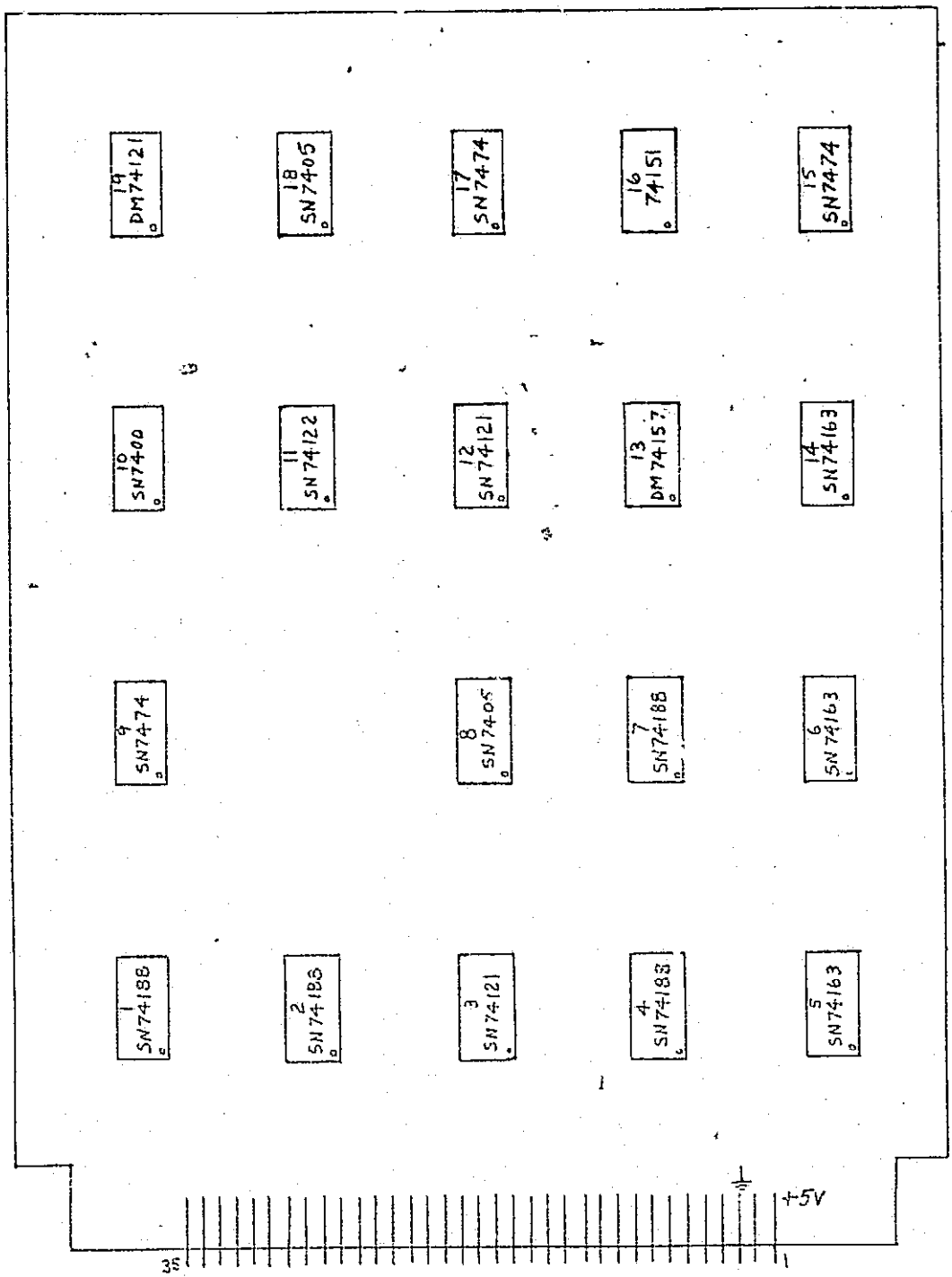


CHG LTR

SK

ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		MEMORY ADDRESS FLT # 1-1	TRW ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
			SK
MJO			SHEET OF

SYSTEMS 523 REV. 5-67

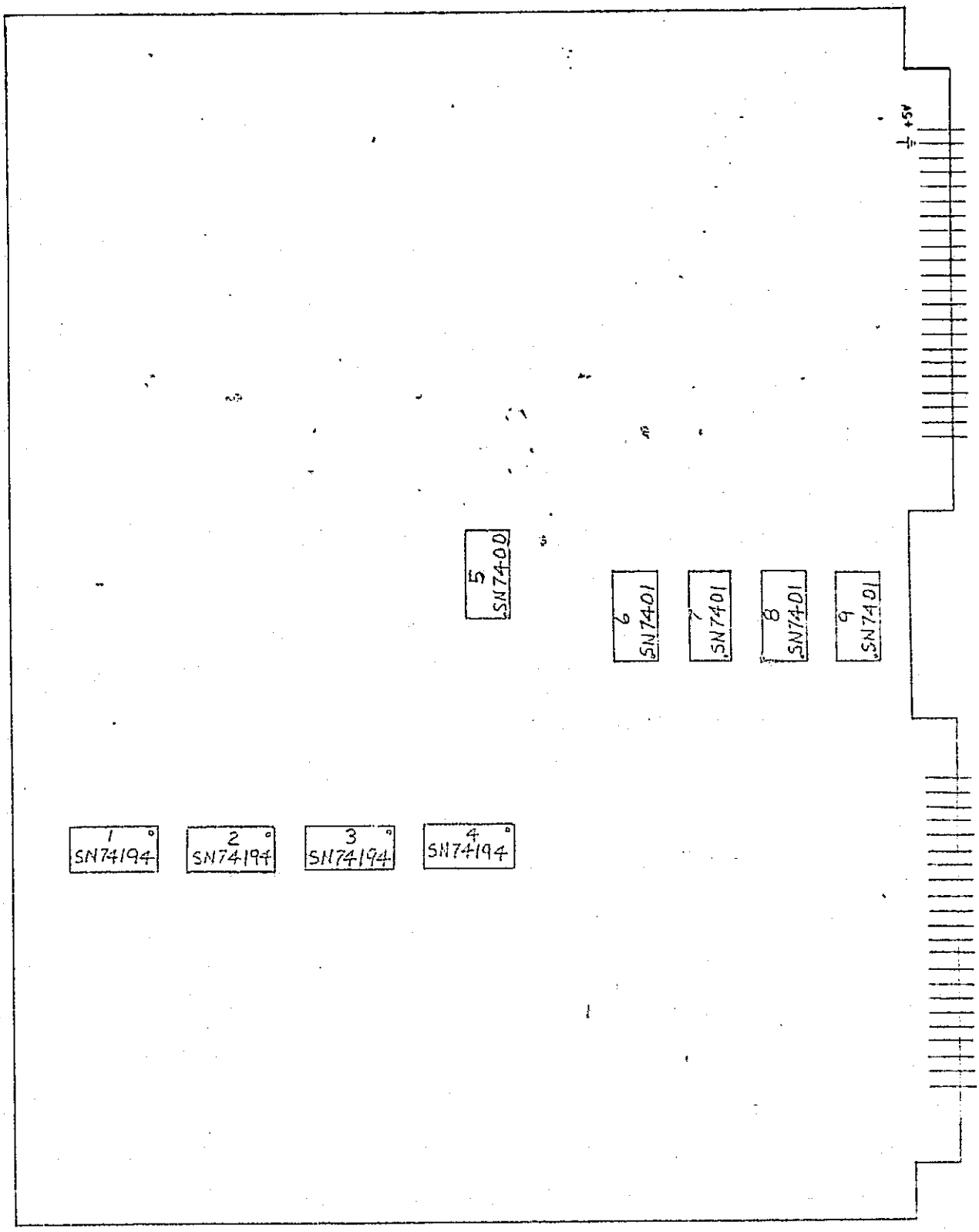


SK

CHG LTR

ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		FLT #1-2	TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
			SK
MJO			SHEET OF

SYSTEMS 523 REV. 5-67



CHG LTR

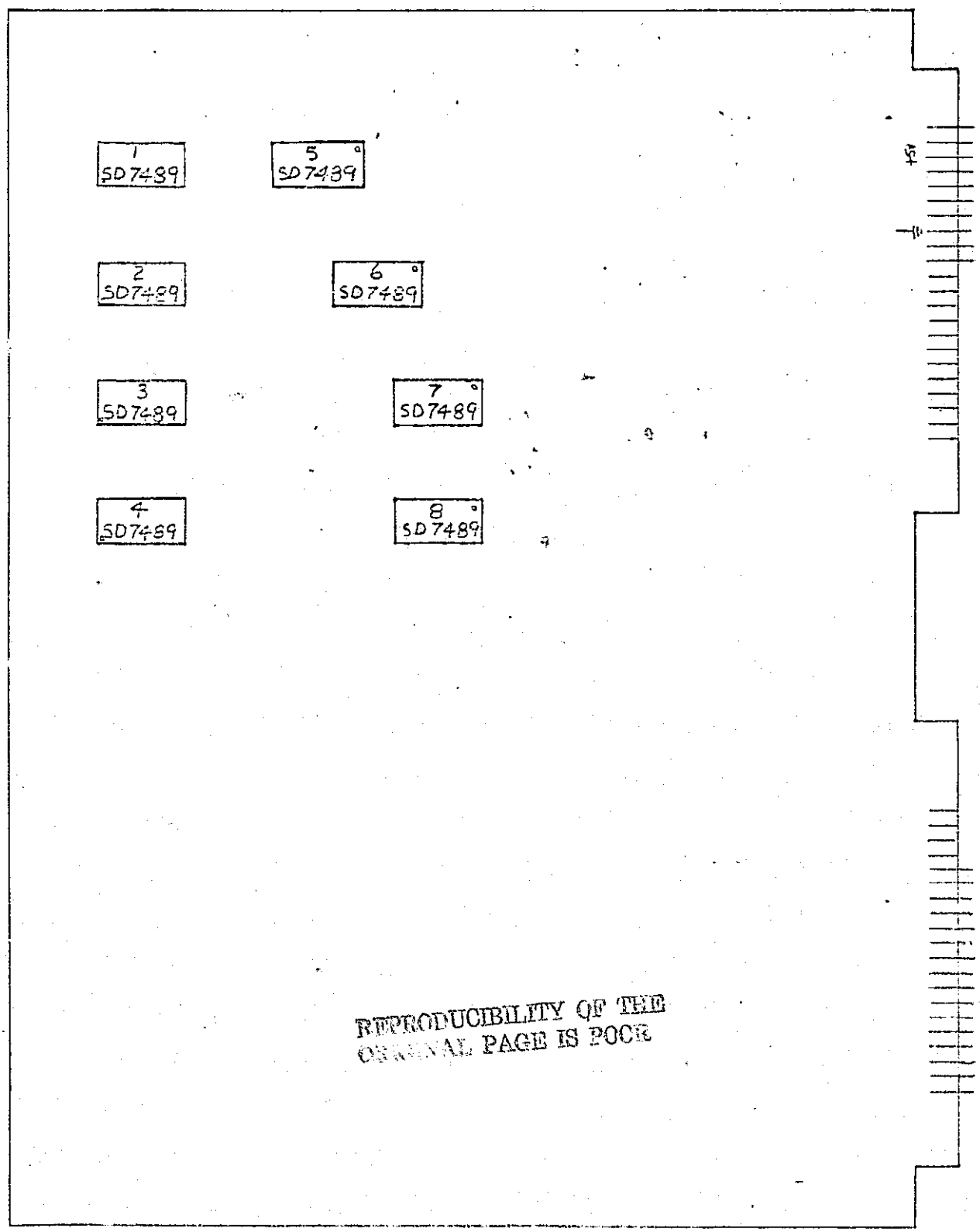
SK

ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		INPUT DATA REGISTER	TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
		FLT #1-3	SK
MOD			SHEET OF

SYSTEMS 323 REV. 5-67

CHG LTR

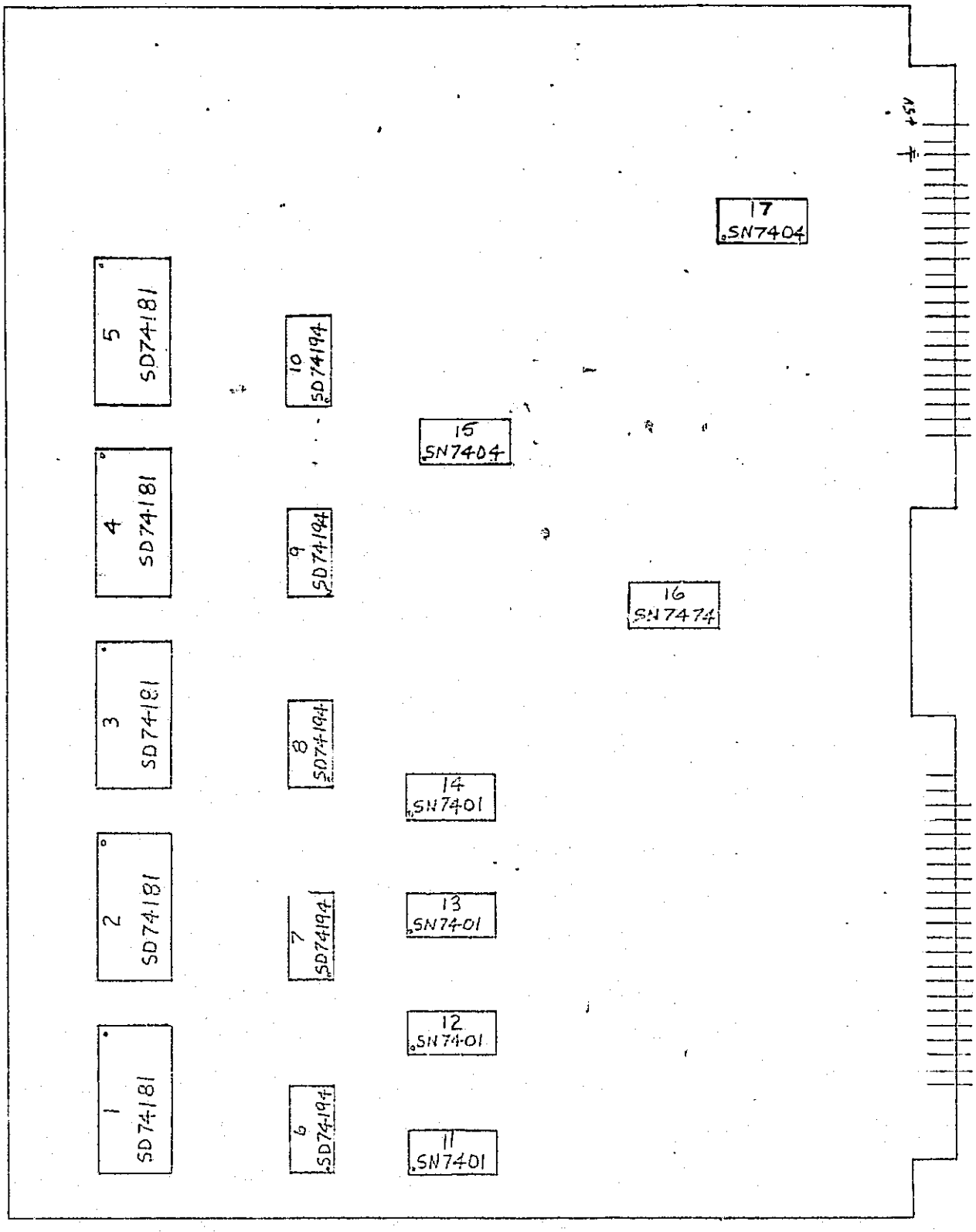
SK



REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		MEMORY	TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH CALIFORNIA
		FLT #1-4	SK
MJO			SHEET OF

SYSTEMS 523 REV. 5-67

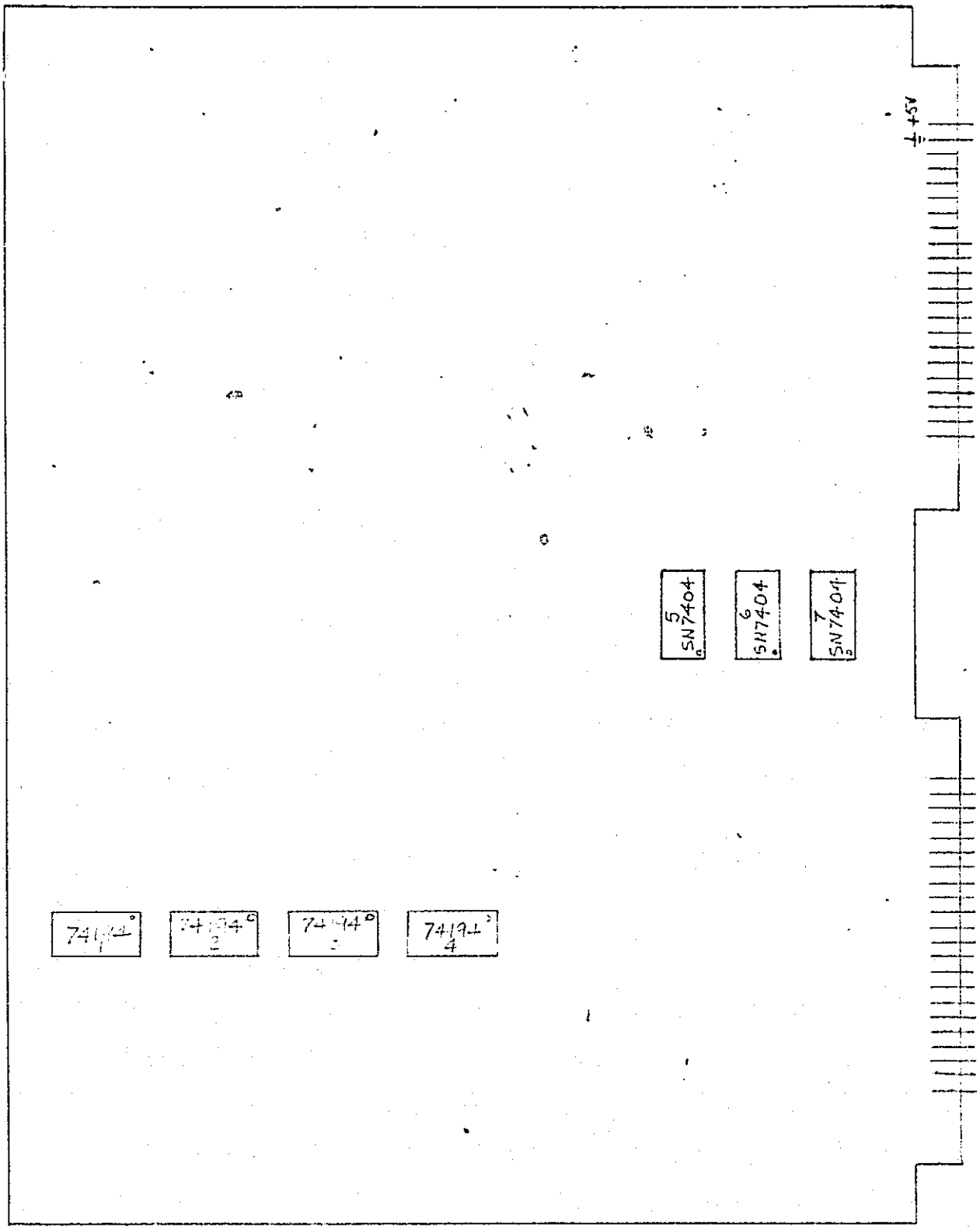


ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		ARITHMETIC LOGIC UNIT FLT # 1-5	TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
MJO			SK
			SHEET OF

SYSTEMS 523 REV. 5-67

CHG LTR

SK

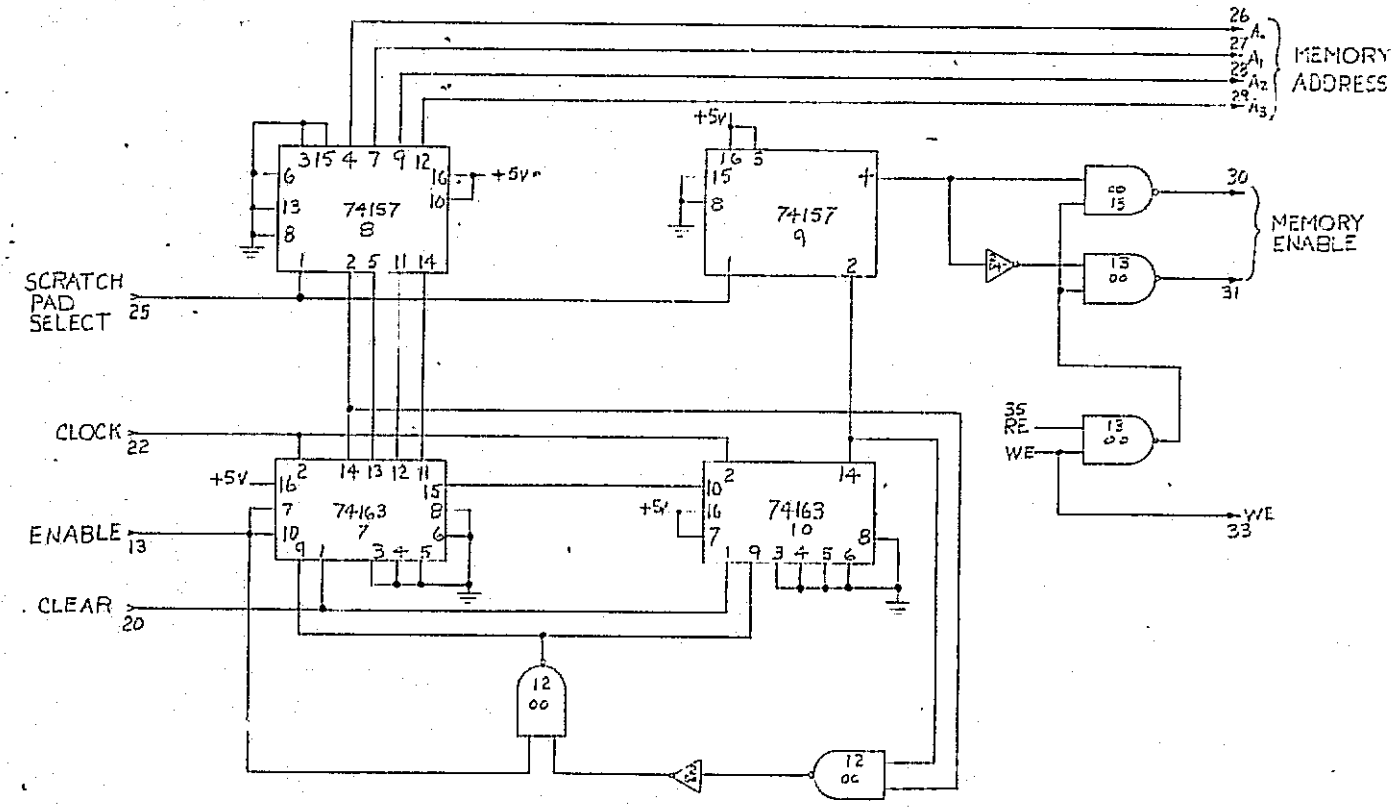


ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		FLT # 1-6 AND #1-7	TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
			SK
MJO			SHEET OF

SYSTEMS 523 REV. 5-67

SK

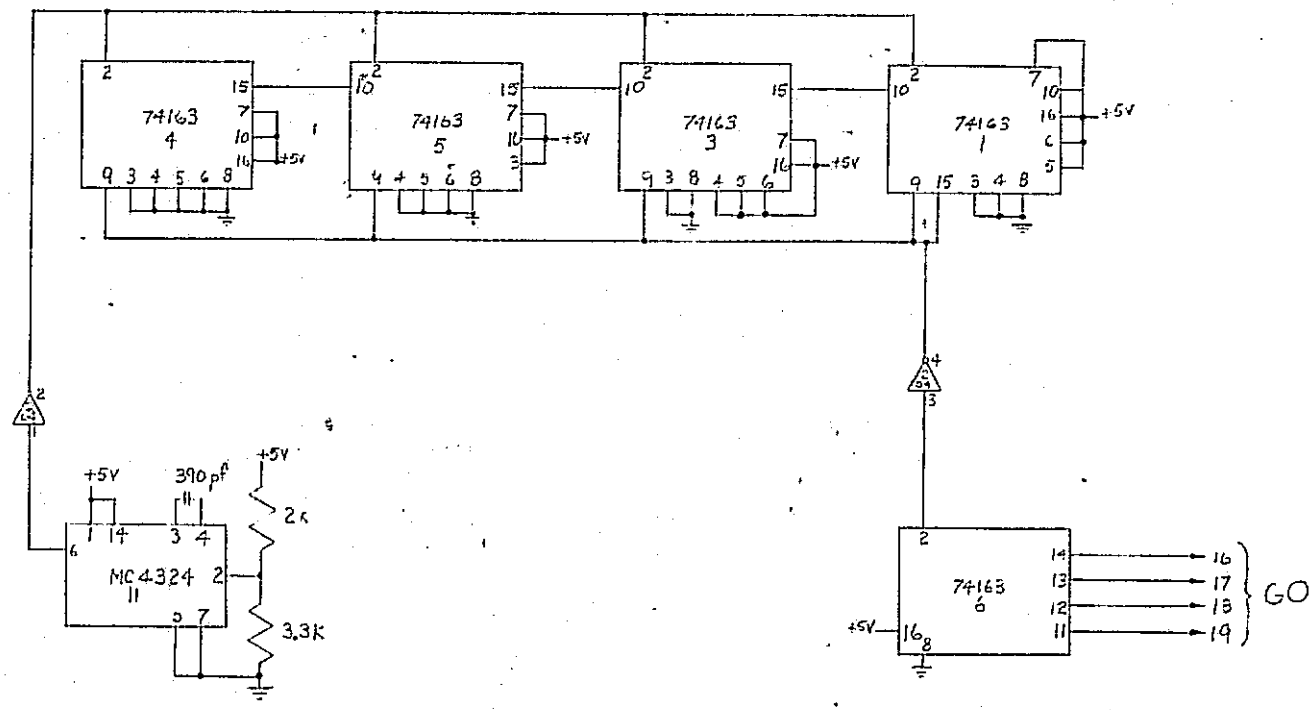
CHG LTR



ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		MEMORY ADDRESS FLT #1-1	TRW SYSTEMS GROUP DNL SPACE PARK • REDONDO BEACH • CALIFORNIA
MJO			SK
			SHEET 8 OF 12

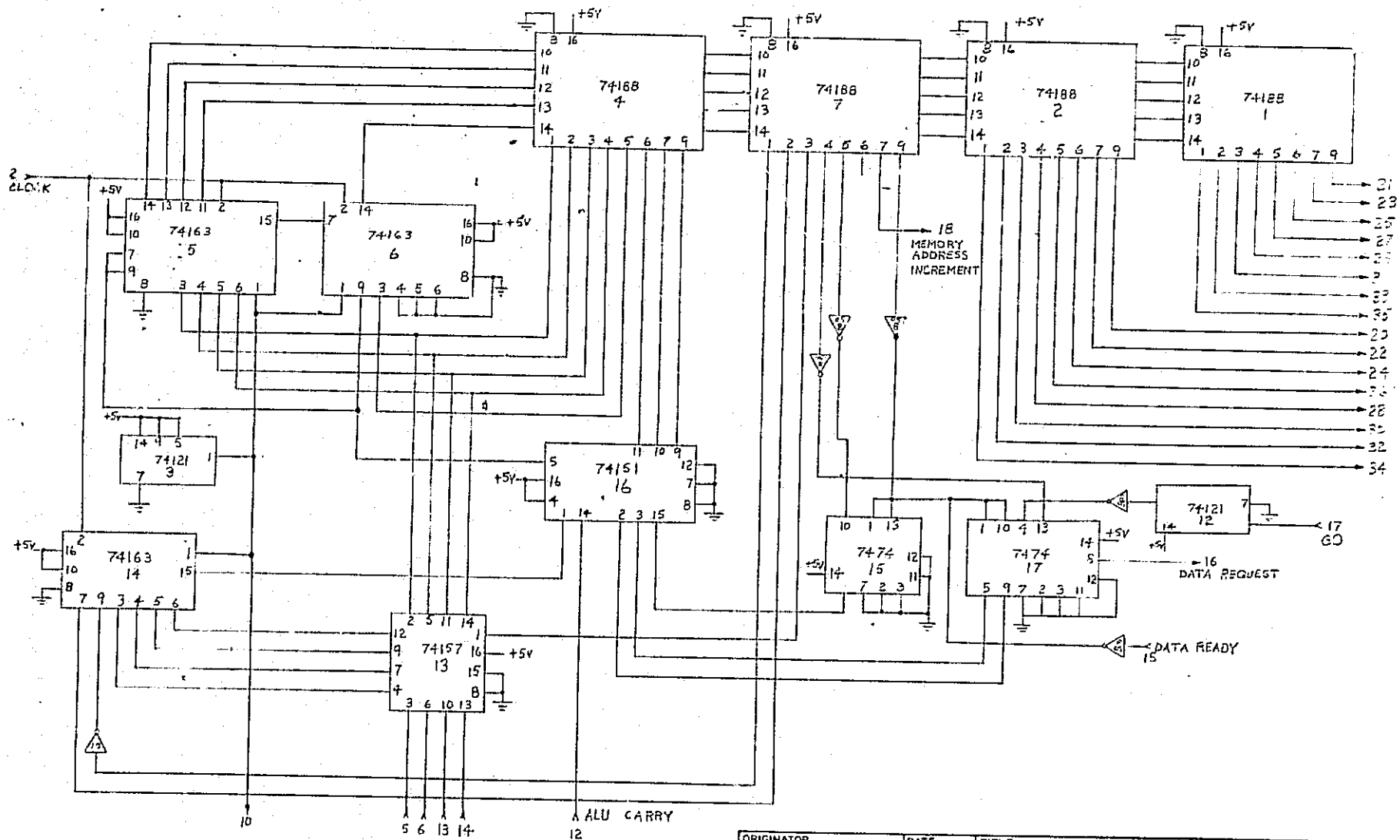
REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

SK | CHG LTR



ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		CLOCK CIRCUIT FLT # 1-1	TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH • CALIFORNIA
MJO			SK
			SHEET 9 OF 14

5733 LMS 3563 REV. 3-67



ORIGINATOR	DATE	TITLE
		FLT #1-2
MJO		

ENGINEERING SKETCH
TRW
ONE SPACE PARK • REDONDO BEACH • CALIFORNIA

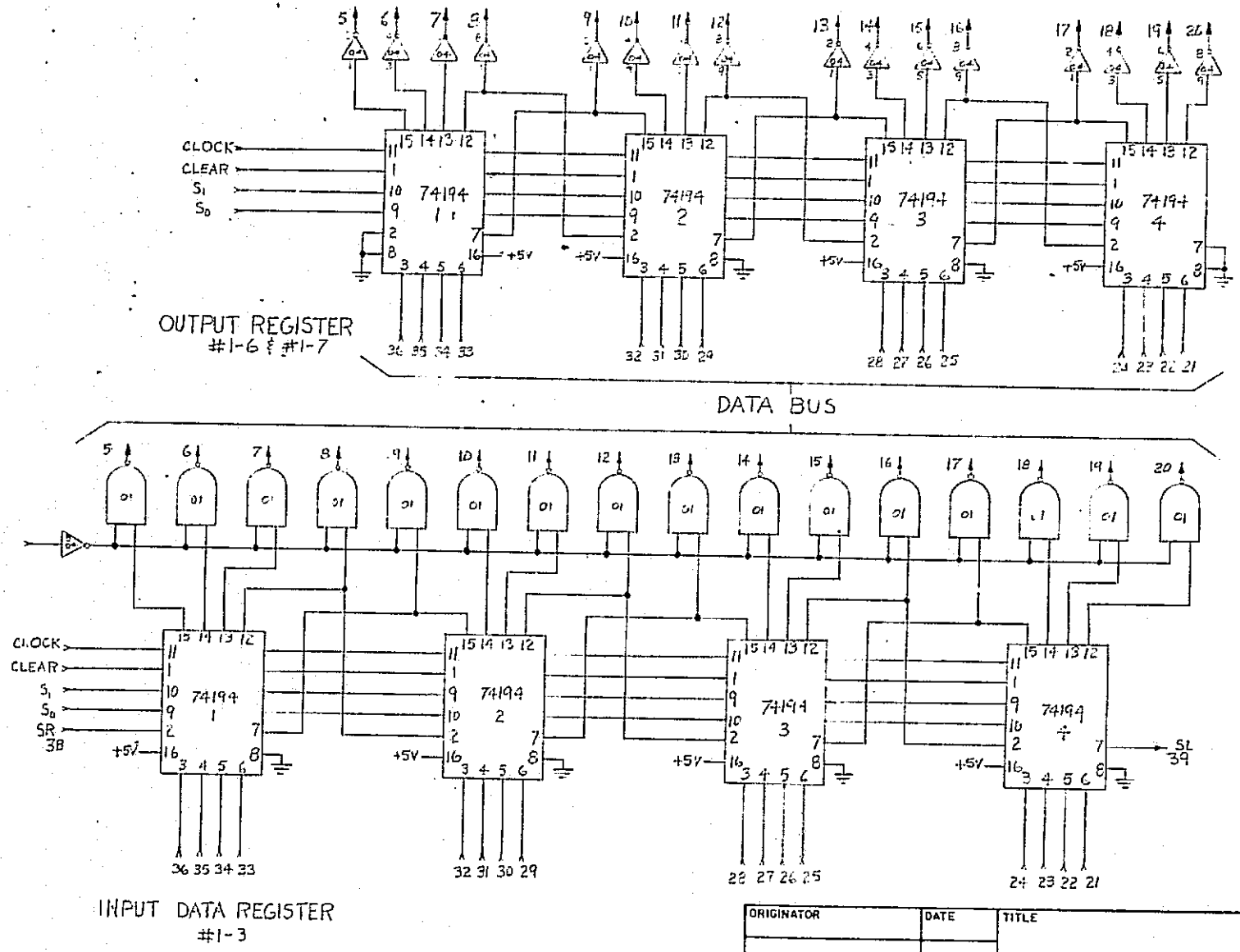
SK

SHEET 10 OF 12

SYSTEMS 3001 REV. 5-67

SK

CHG LTR

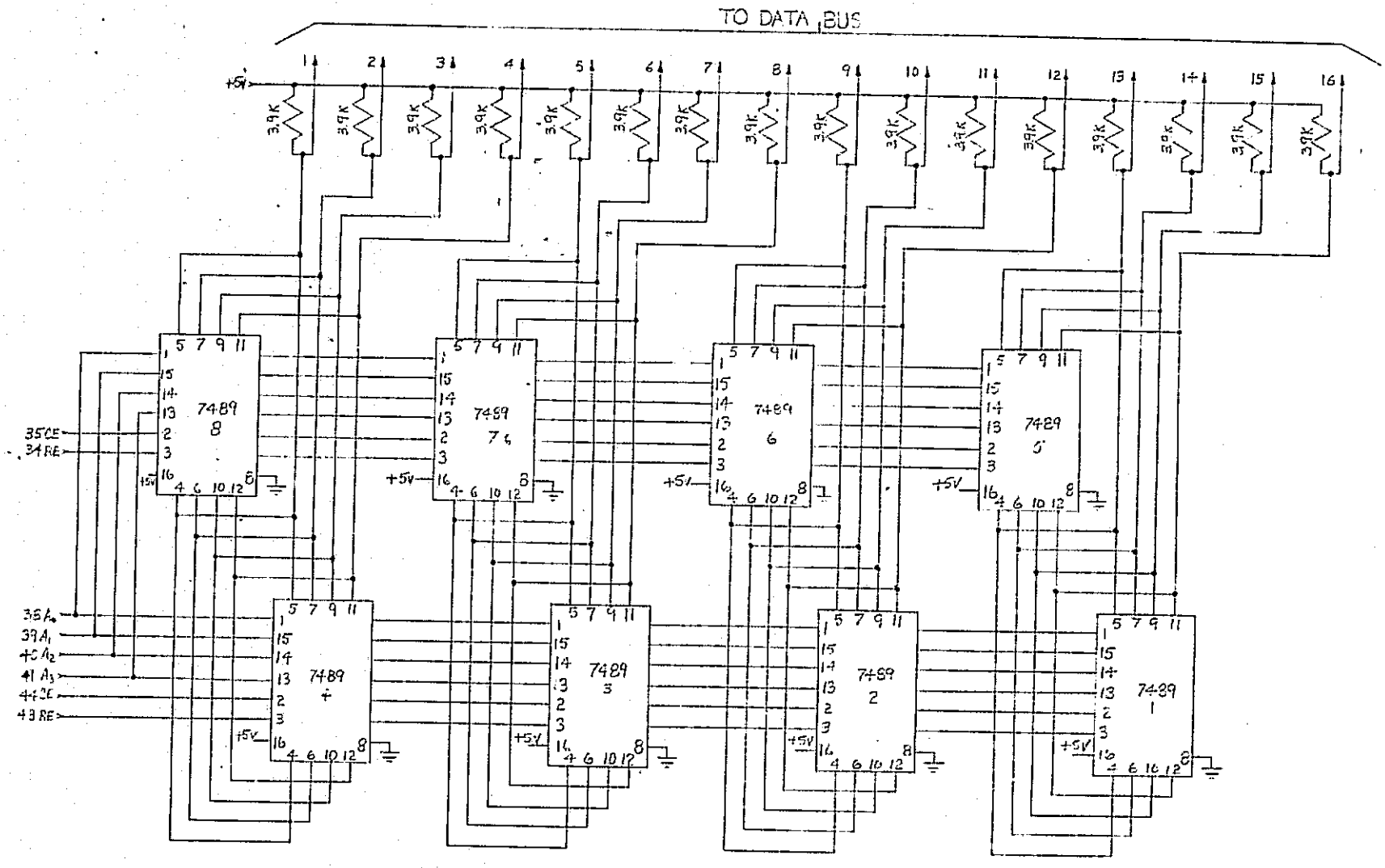


REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		DATA REGISTERS FLT #1-3, #1-6, & #1-7	TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH • CALIFORNIA
MJO			SK
			SHEET 11 OF 17

SK

CHG LTR



ORIGINATOR	DATE	TITLE
		MEMORY FLT #1-4
MJO		

B-15

ENGINEERING SKETCH

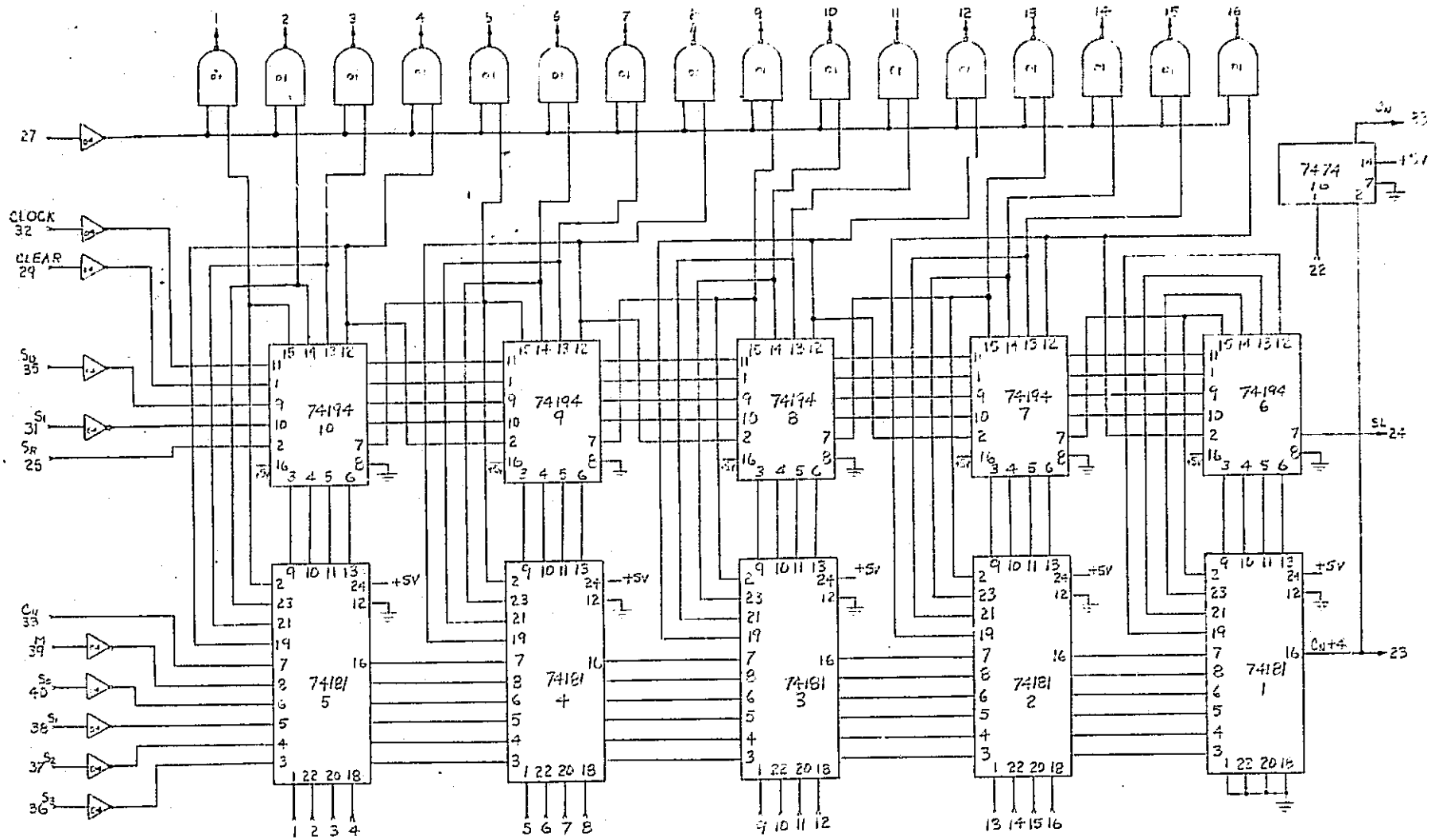
TRW

DNL SPACE PARK • REDONDO BEACH • CALIFORNIA

SK

SHEET 12 OF 18

SK | CHG LTR



ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		ARITHMETIC LOGIC UNIT, FLT #1-5	TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH • CALIFORNIA
MJO			SK
			SHEET - OF -

B-16

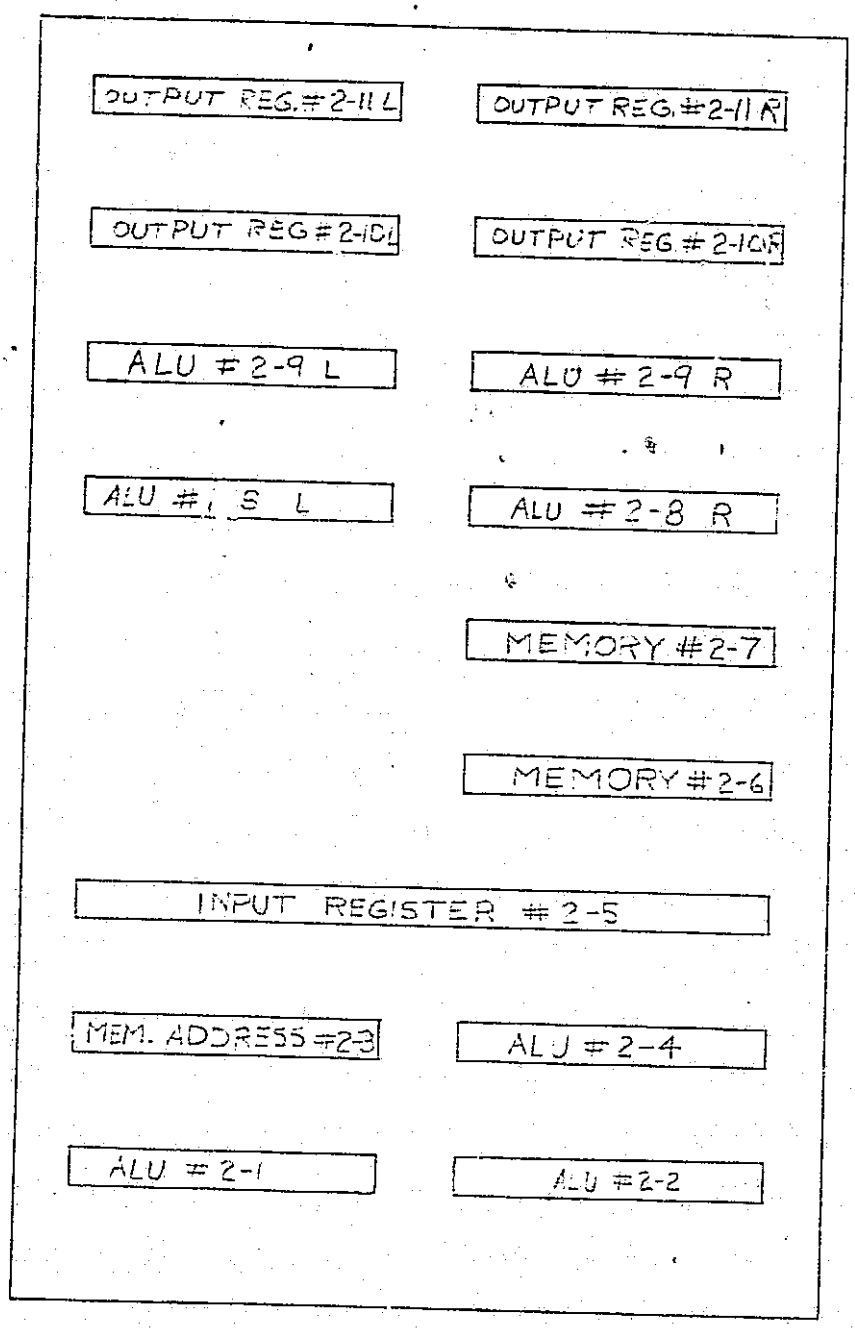
APPENDIX C
DIGITAL TRACKING FILTER

Pin functions are the same as J1 and J2 for the cascaded averaging filter (see Appendix B)

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

CHG LTR

SK



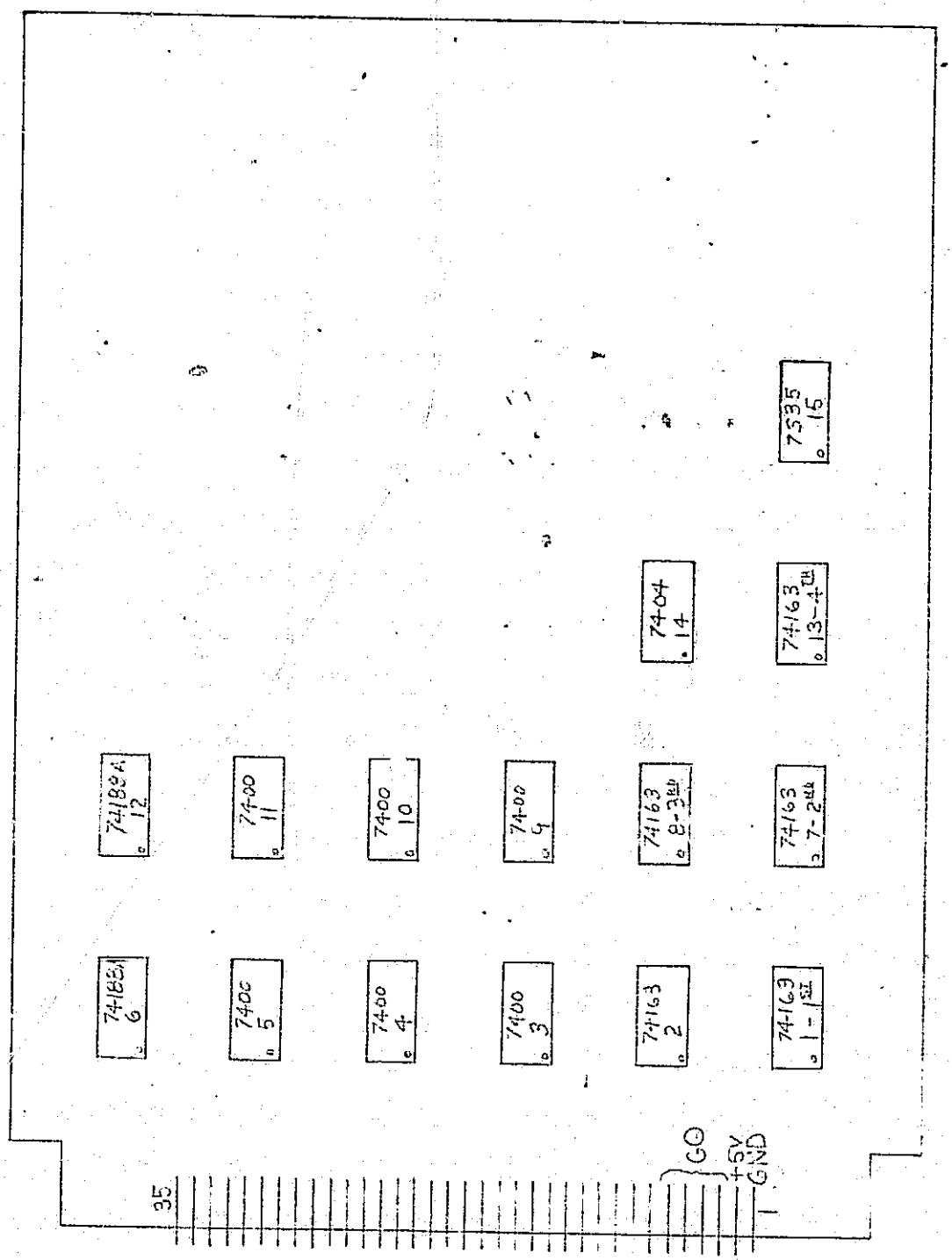
REAR VIEW

ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		FILTER #2 BOARD LOCATION	TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
MJO			SK
			SHEET OF

SYSTEMS 523 REV. 5-67

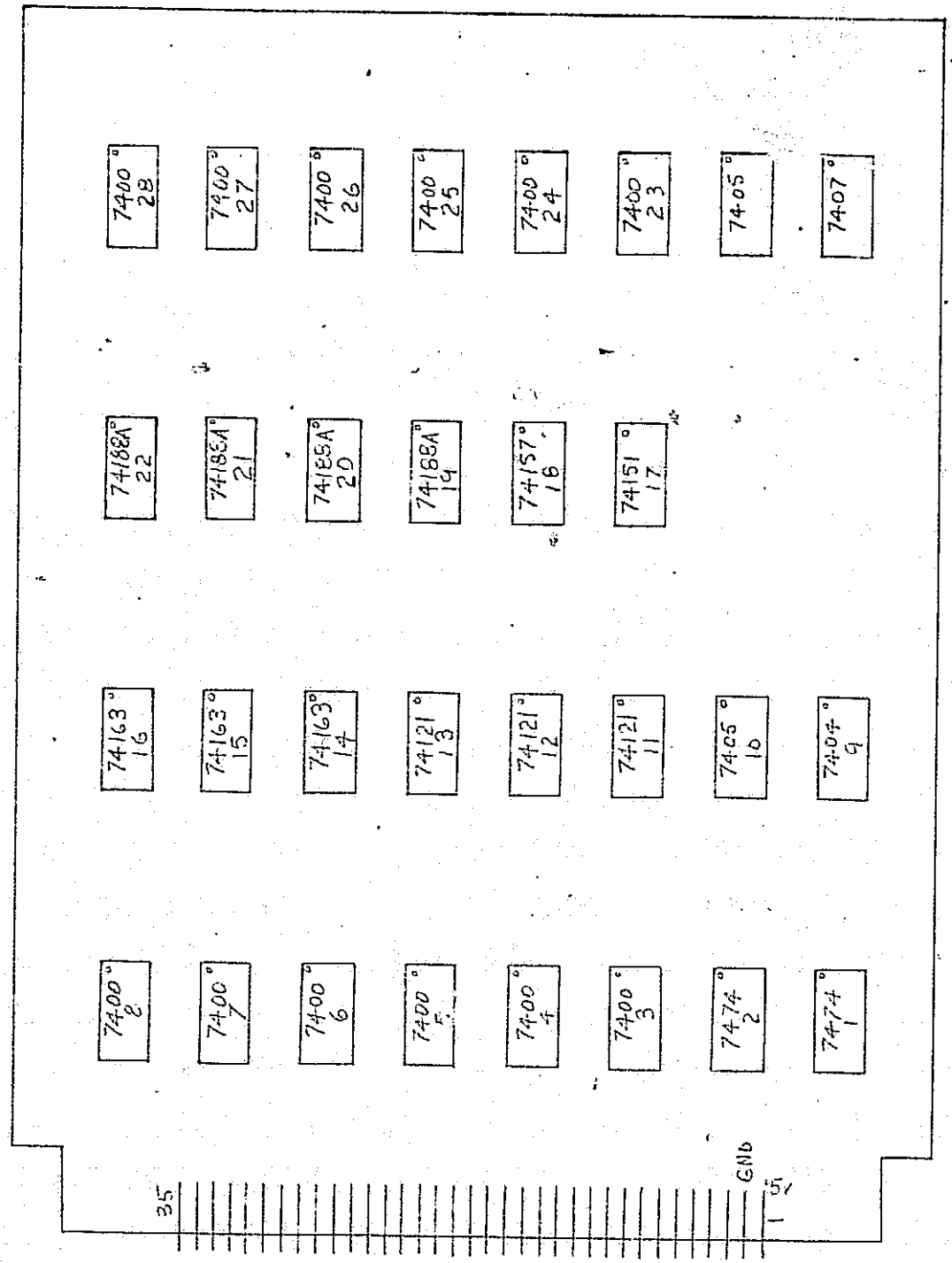
SK

CHG LTR



ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		ARITHMETIC LOGIC UNIT AND CLOCK CKT. FLT # 2-1	TRW ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
MJO			SK
			SHEET OF

SYSTEMS 523 REV. 5-67



ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		#3 ARITHMETIC LOGIC UNIT FLT #2-2	TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
MJO			SK
			SHEET OF

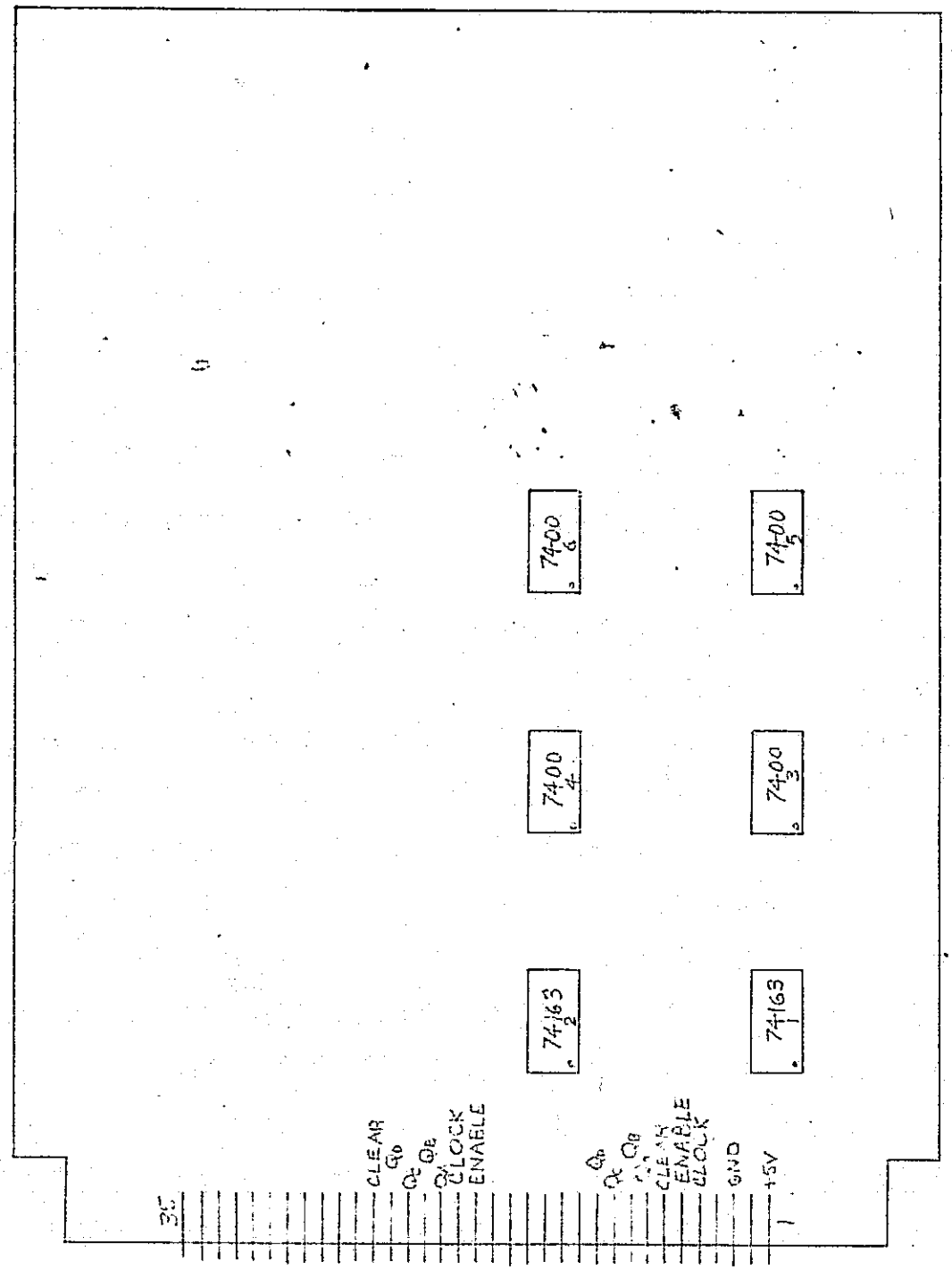
SK

CHG LTR

SYSTEMS 523 REV. 5-67

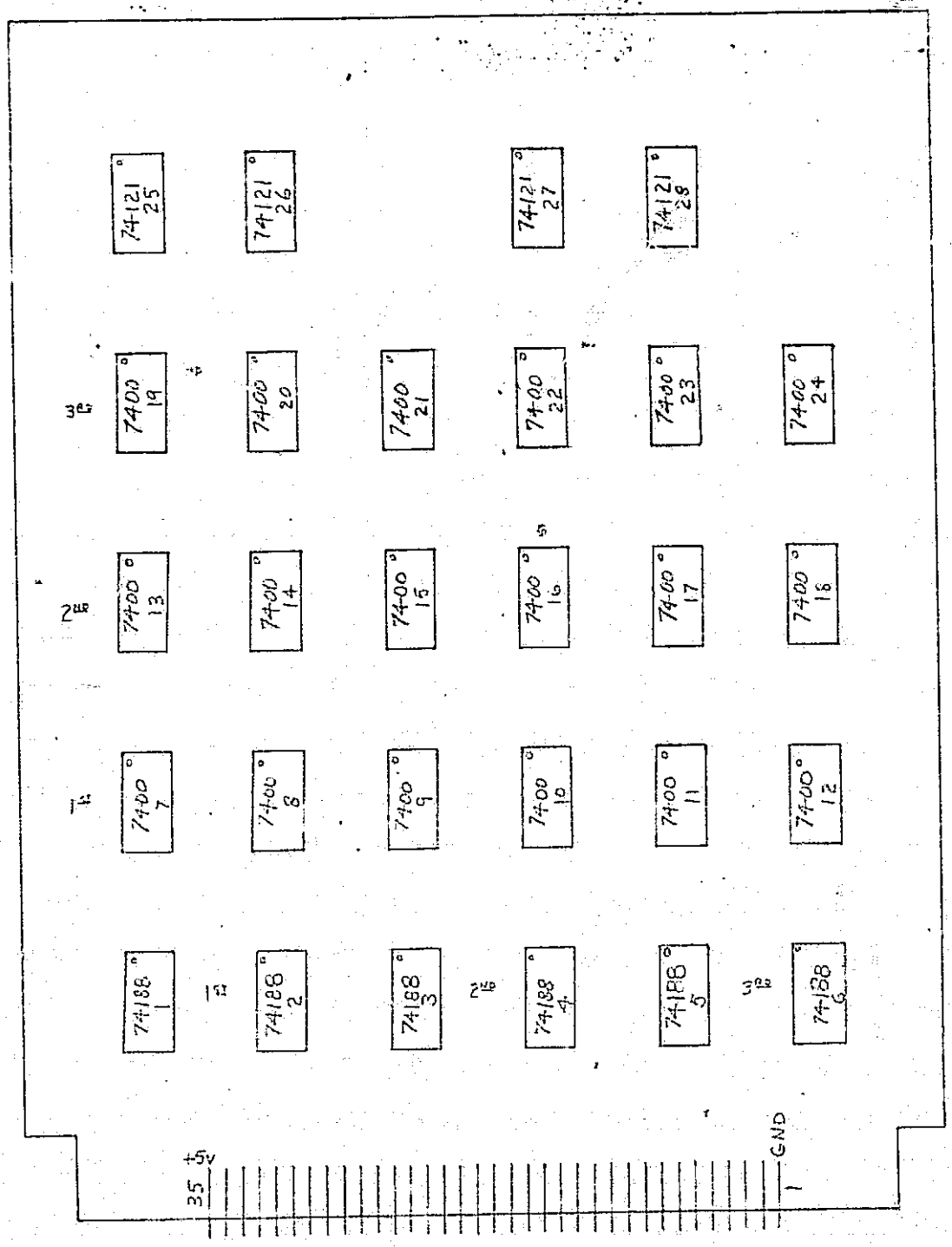
CHG LTR

SK



ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		DATA/ERROR MEM. ADD. AND RANGE MEM. FLT # 2-3	TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
MJO			SK
			SHEET OF

SYSTEMS 323 REV. 5-67



ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		ARITHMETIC LOGIC UNIT, FLT # 2-4	TRW SYSTEMS GROUP, ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
MJO			SK
			SHEET OF

SK

CHG LTR

SYSTEMS 523 REV. 5-67

REPRODUCIBILITY OF THE
ORIGINAL PAGE IS POOR

CHG LTR

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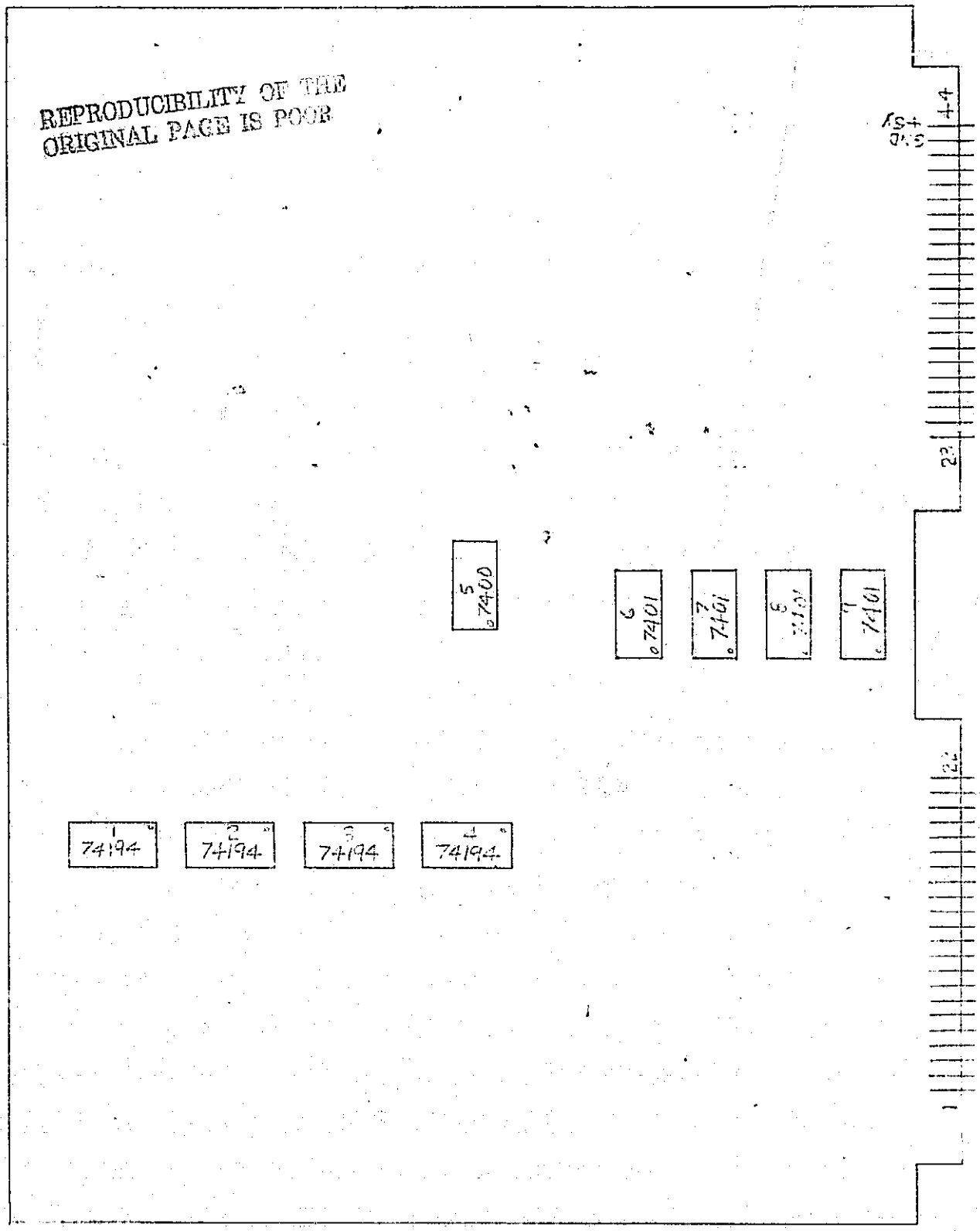
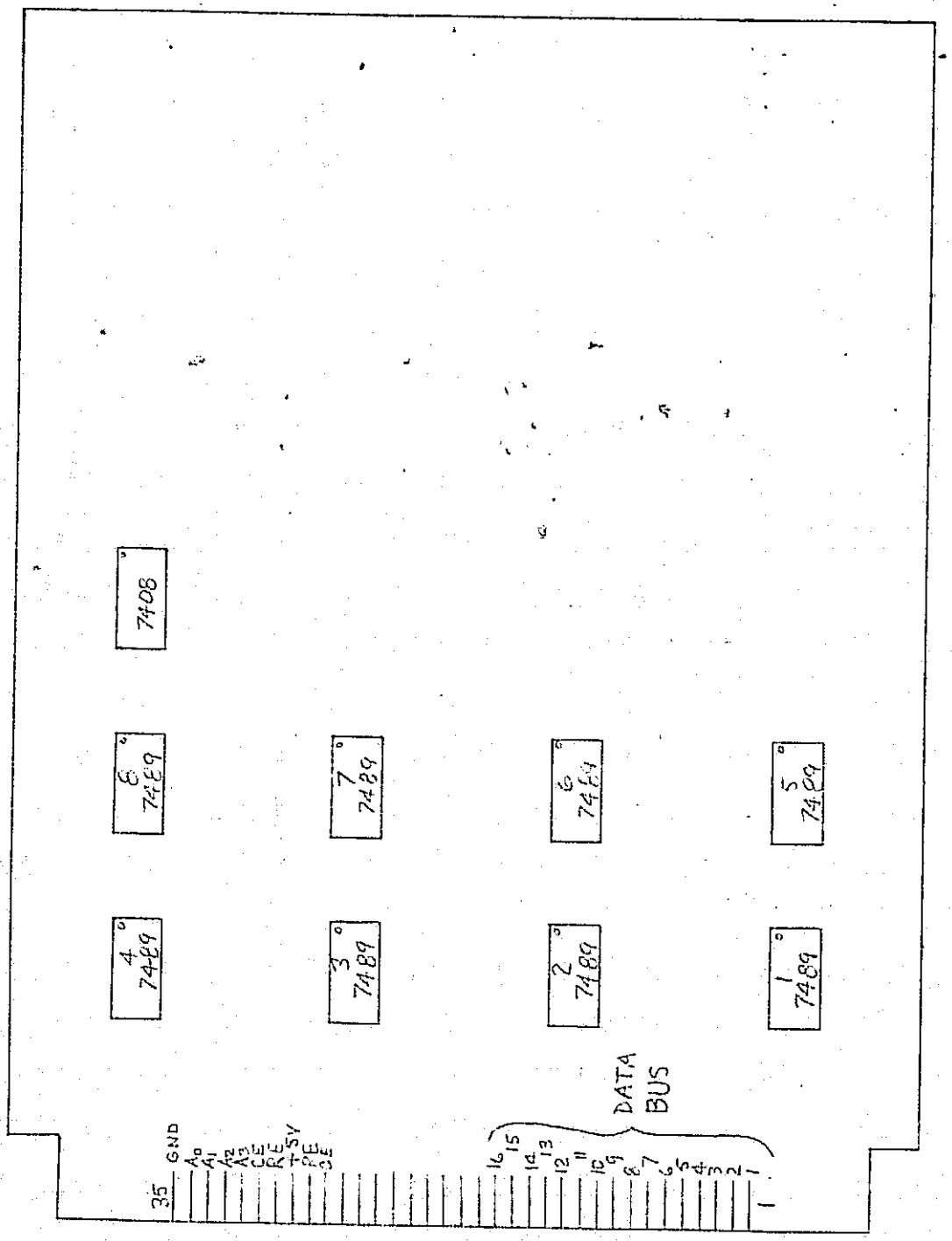


ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		INPUT DATA REGISTER	TRW
		FLT # 2-5	SK
MJO			SHEET OF

SYSTEMS 523 REV. 5-67



ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		MEMORY #2-6	TRW ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
MJO			SK
			SHEET OF

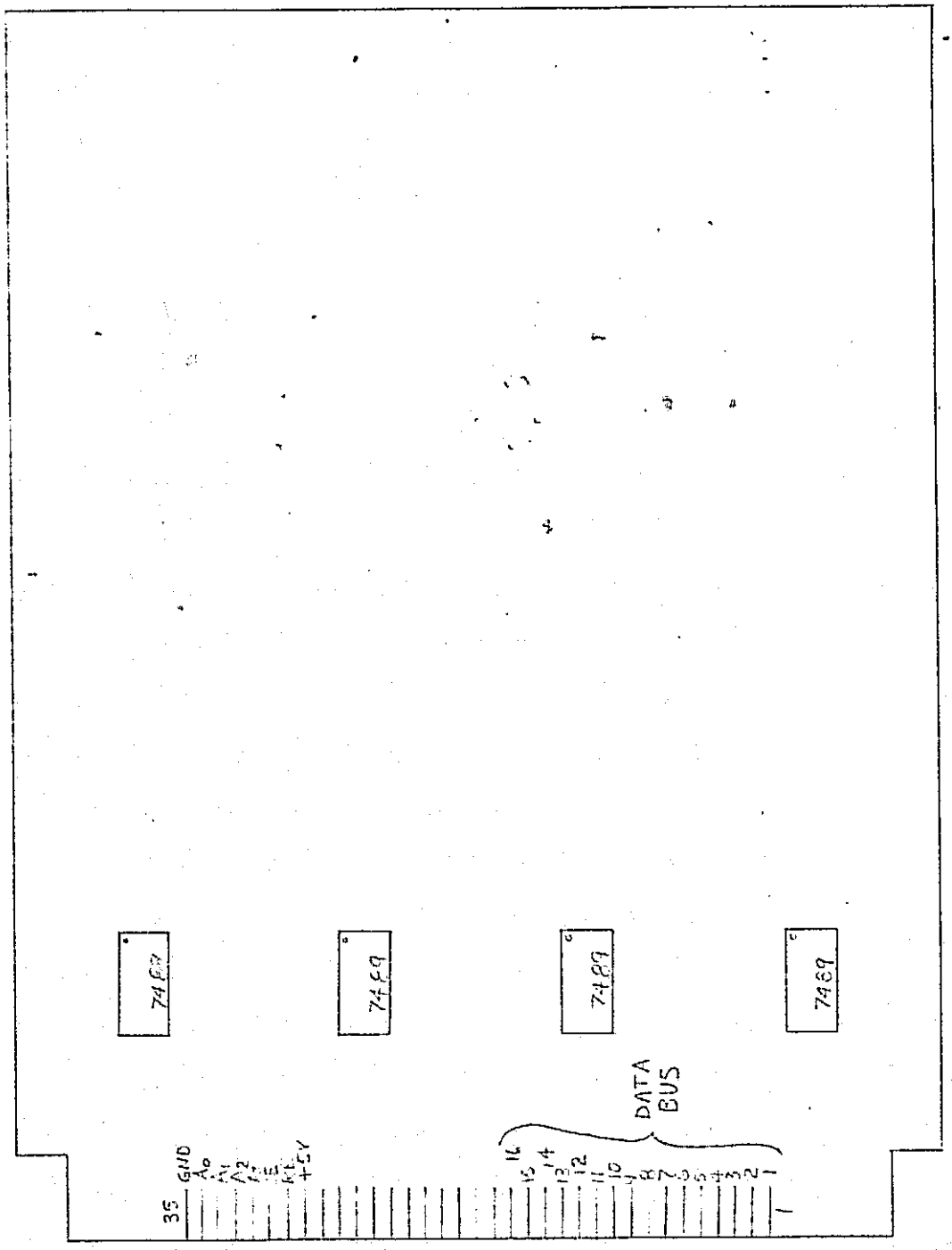
SYSTEMS 523 REV. 5-67

CHG LTR

SK

CHG LTR

SK

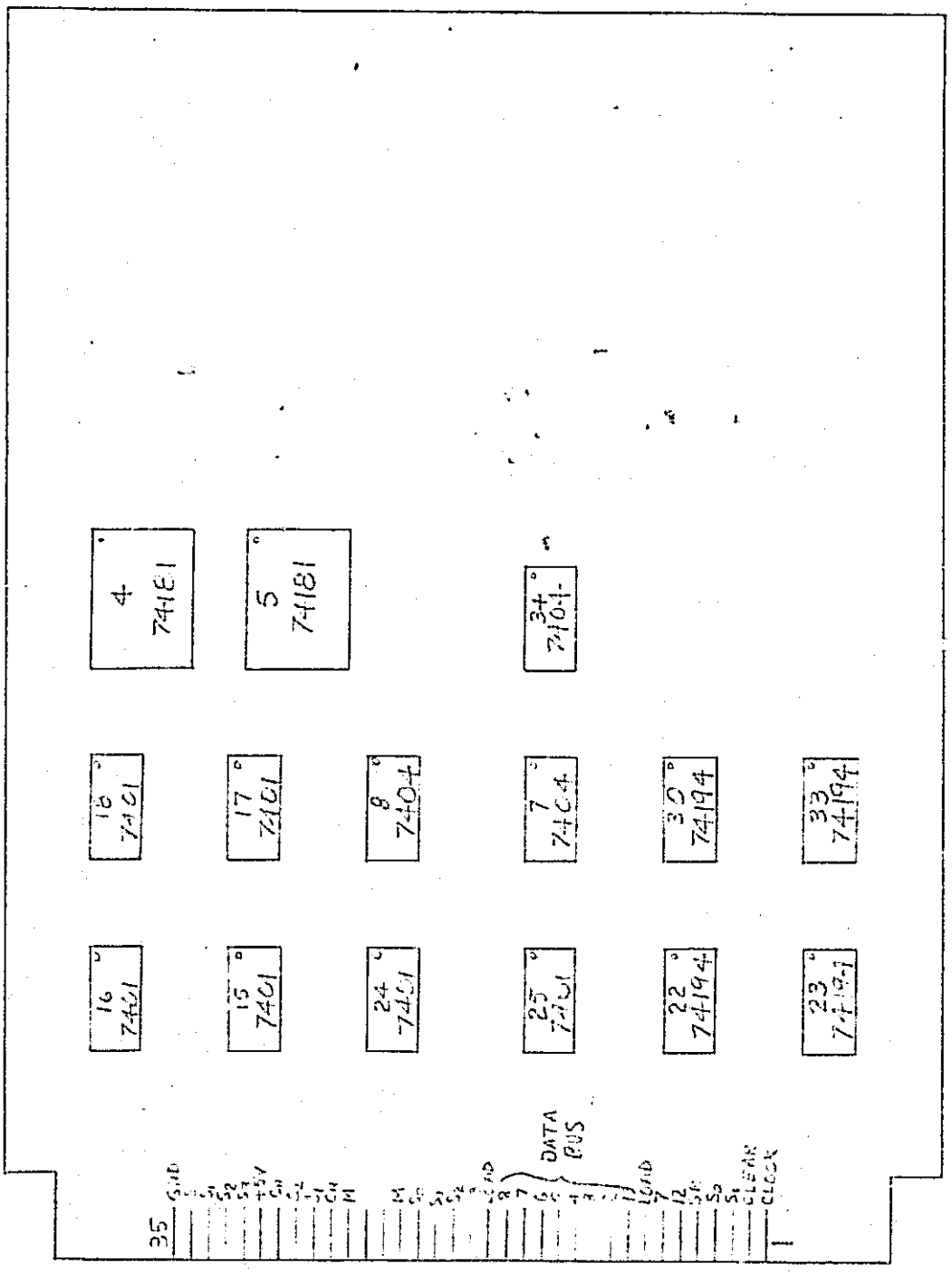


ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		MEMORY #2-7	TRW INC. ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
			SK
MJO			SHEET OF

SYSTEMS 523 REV. 5-67

CHG LTR

SK



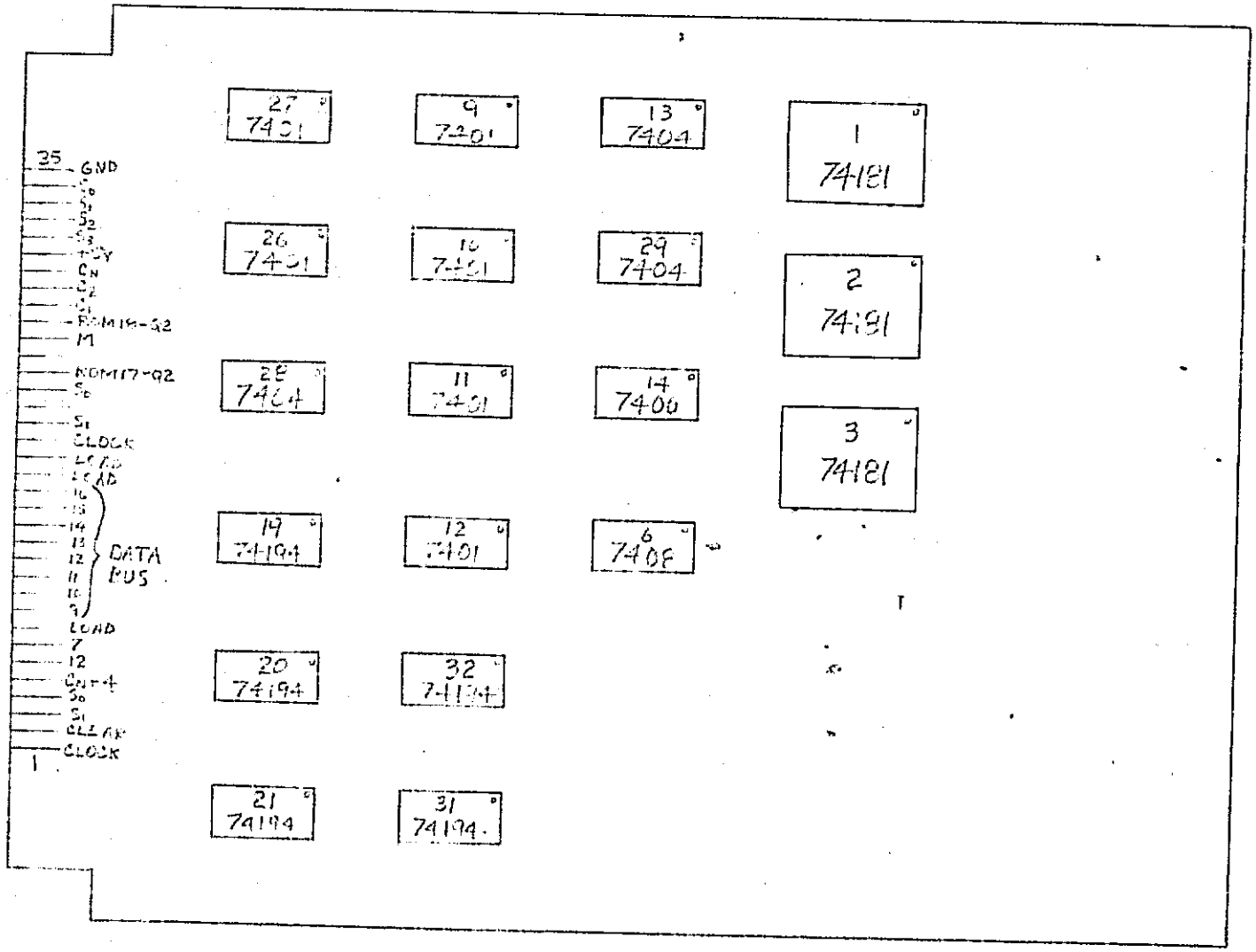
ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		ARITHMETIC LOGIC UNIT	TRW
		LEFT SIDE	ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
MJO			SK
			SHEET / OF

C-11

SYSTEMS 523 REV. 5-67

SK

CHG LTR



ORIGINATOR

MJO

DATE

TITLE

ENGINEERING SKETCH

TRW

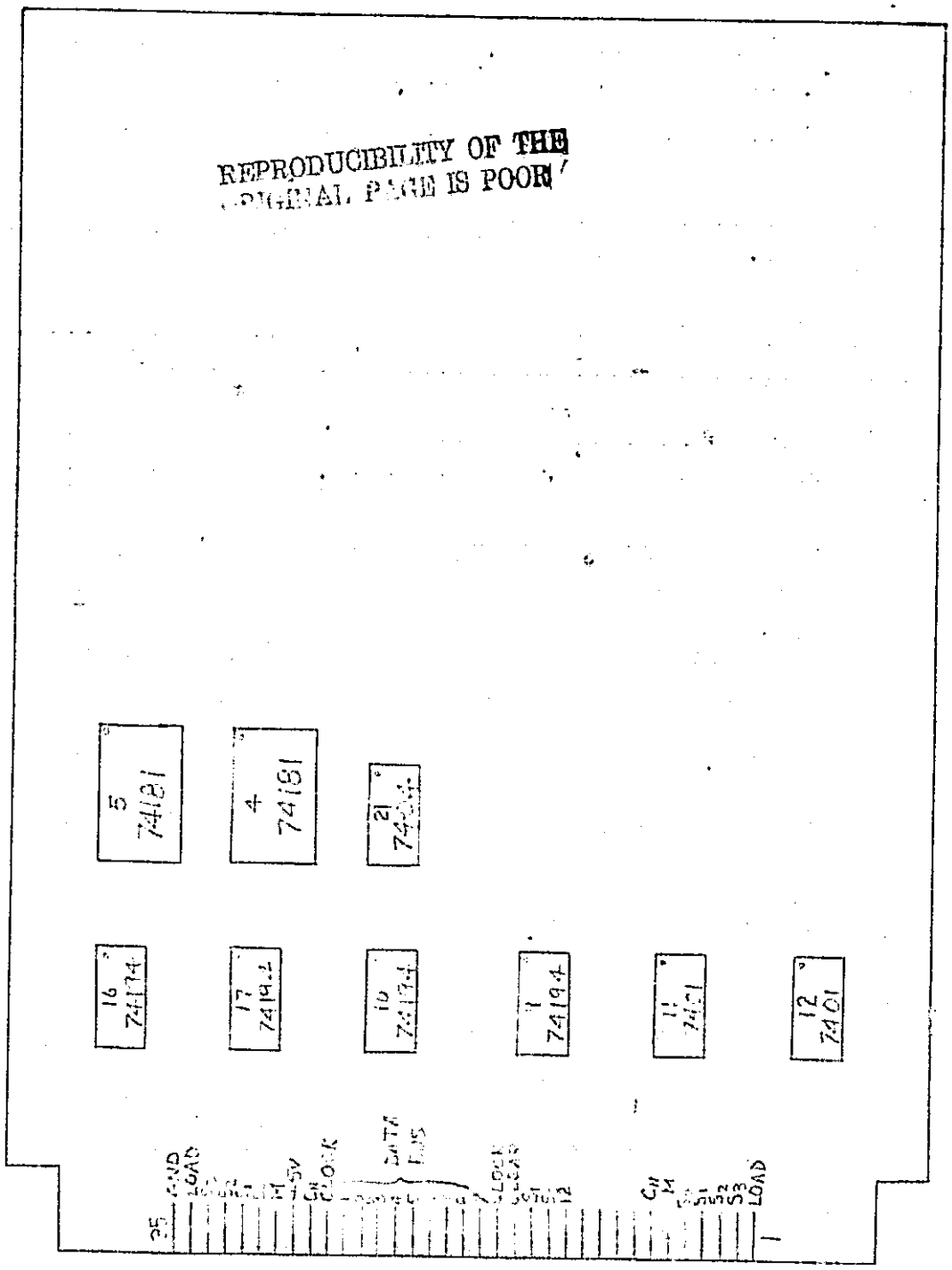
SK

SHEET OF

SYSTEMS 123 REV. 5-67

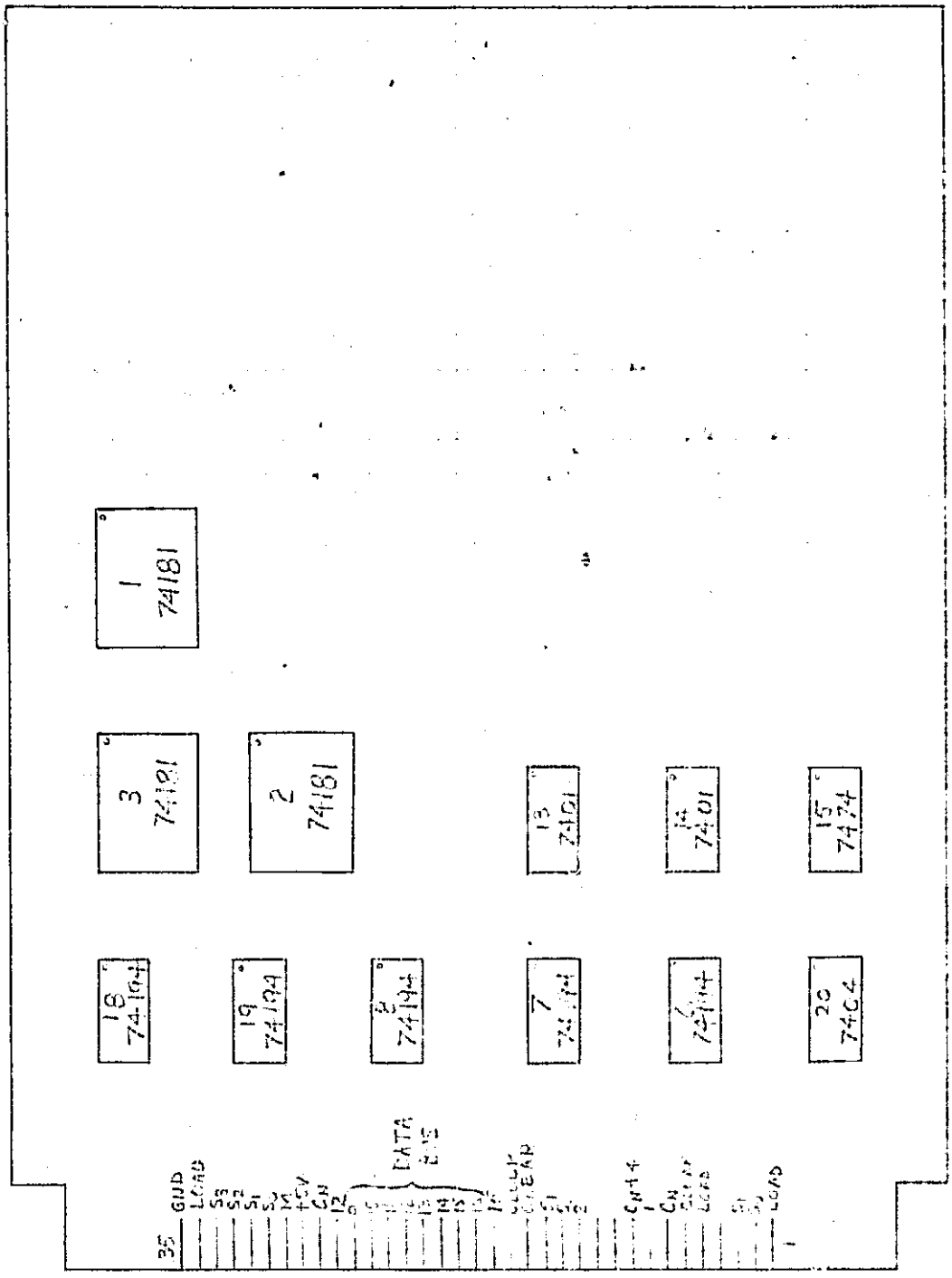
SK	REVISIONS			
	LTR	DESCRIPTION	DATE	APPROVED

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR



ENGINEERING SKETCH	TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA
ORIGINATOR / DATE	# ARITHMETIC LOGIC UNIT
MJO	SIZE A / CODE IDENT NO. 11982 / SK
	SCALE / SHEET 1 OF

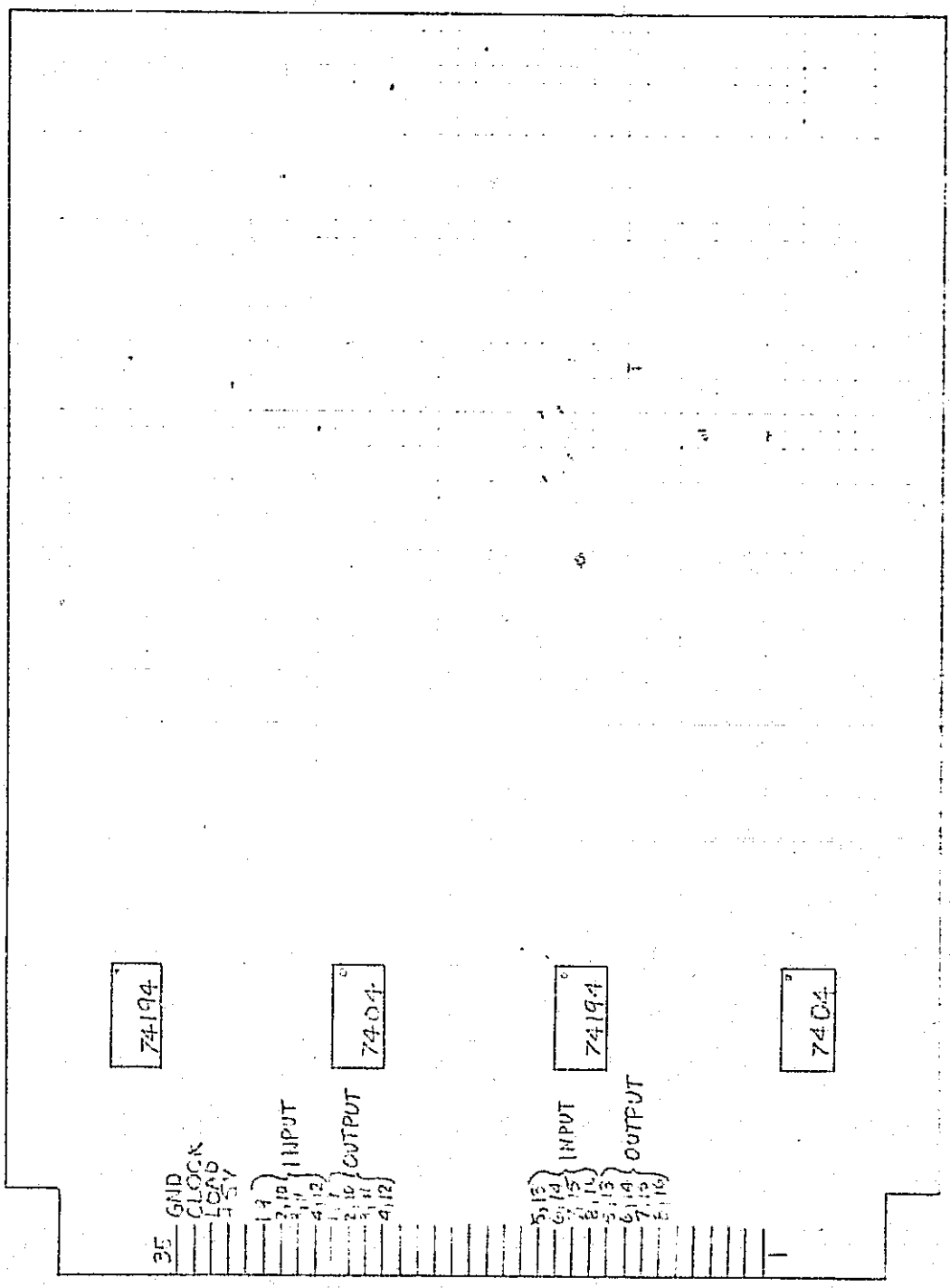
SK	REVISIONS			
	LTR	DESCRIPTION	DATE	APPROVED



ENGINEERING SKETCH		TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA		
ORIGINATOR	DATE	[illegible]		
		SIZE A	CODE IDENT NO. 11982	SK
MJO		SCALE		SHEET 1 OF

SYSTEMS 523 REV. 12-71

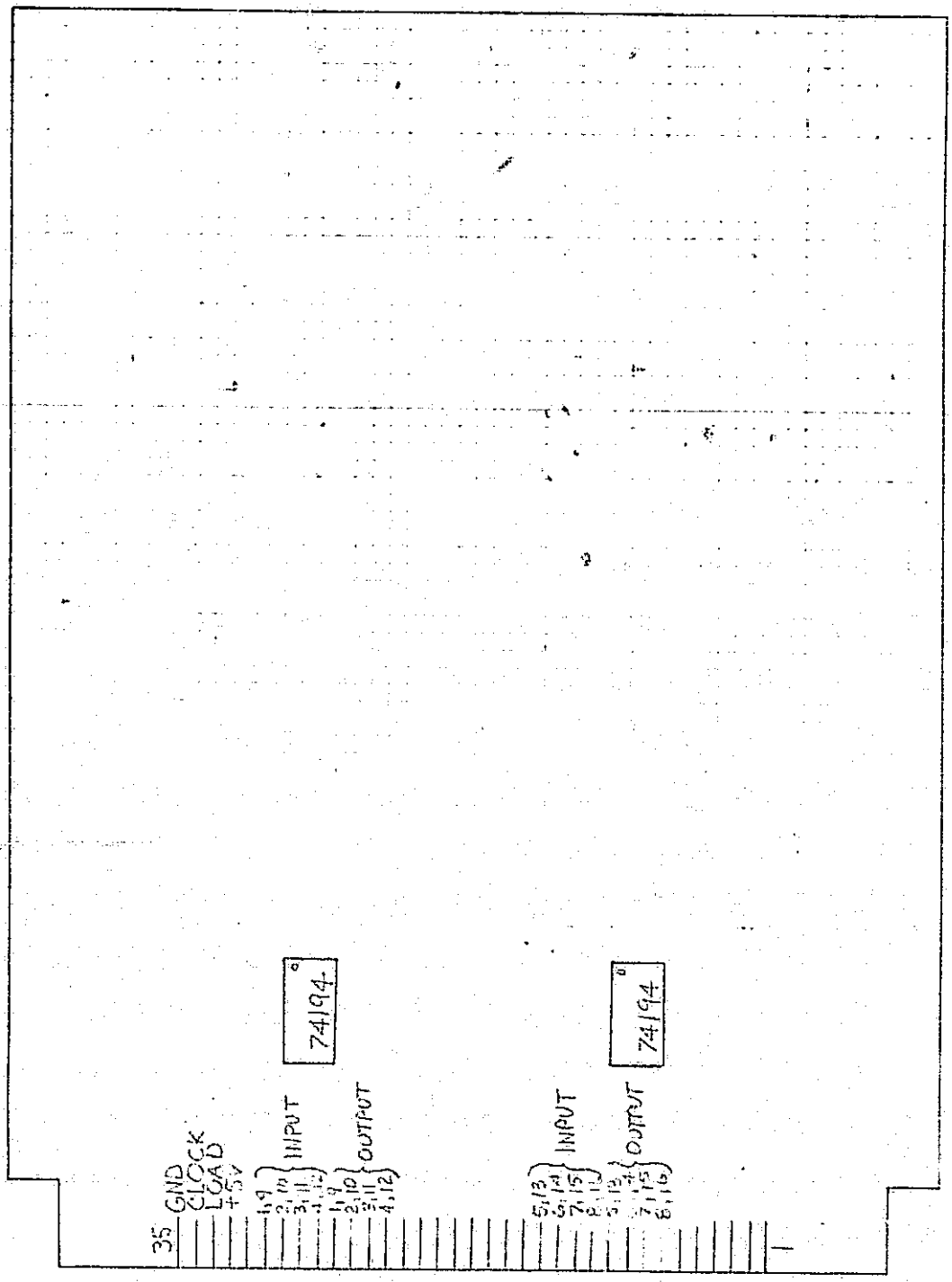
SK	REVISIONS			
	LTR	DESCRIPTION	DATE	APPROVED



ENGINEERING SKETCH		TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA		
ORIGINATOR	DATE	OUTPUT REGISTER #2-[illegible] LEFT [illegible]		
		SIZE A	CODE IDENT NO. 11982	SK
MJO		SCALE C-15		SHEET 1 OF

SYSTEMS 523 REV. 12-71

SK	REVISIONS			
	LTR	DESCRIPTION	DATE	APPROVED

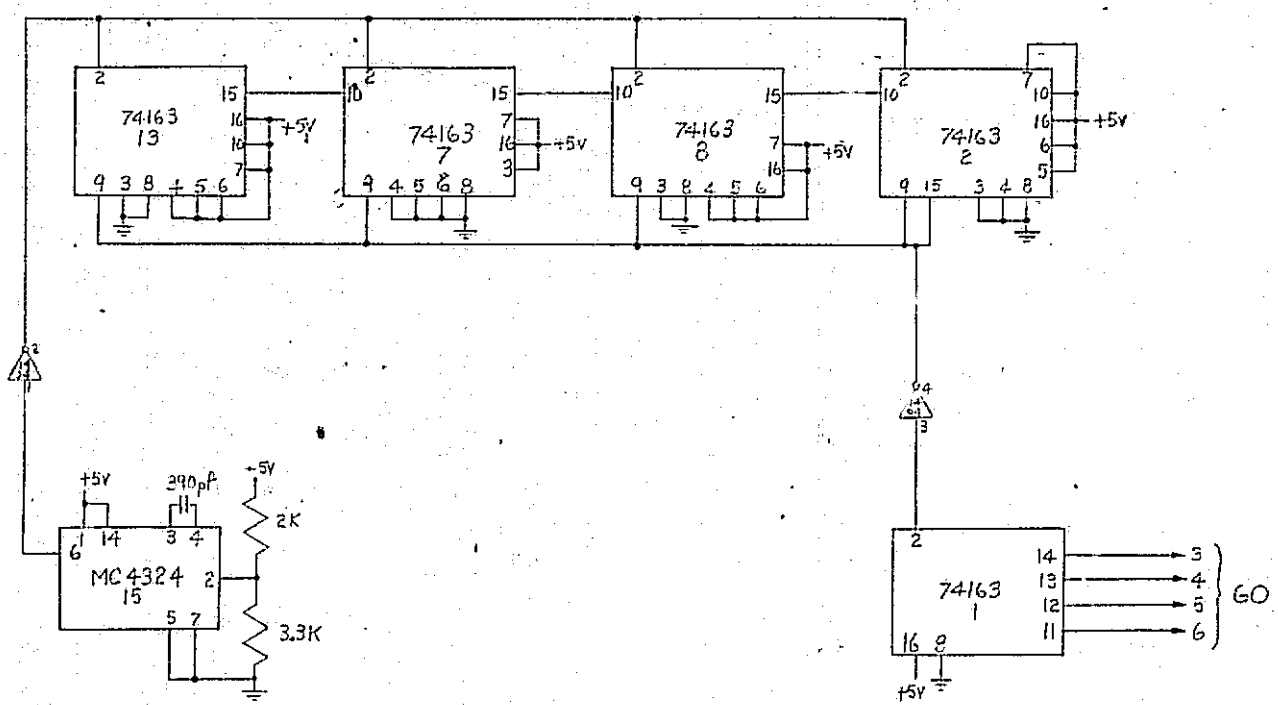


ENGINEERING SKETCH	TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH, CALIFORNIA		
ORIGINATOR / DATE	OUTPUT REGISTER # 2-11 LEFT & RIGHT SHIFT		
MJO	SIZE A	CODE IDENT NO. 11982	SK
	SCALE		SHEET 1 OF

SYSTEMS SC3 REV. 12-71

SK

CHG LTR



ORIGINATOR	DATE	TITLE
		CLOCK CIRCUIT FLT # 2-1
MJO		

ENGINEERING SKETCH

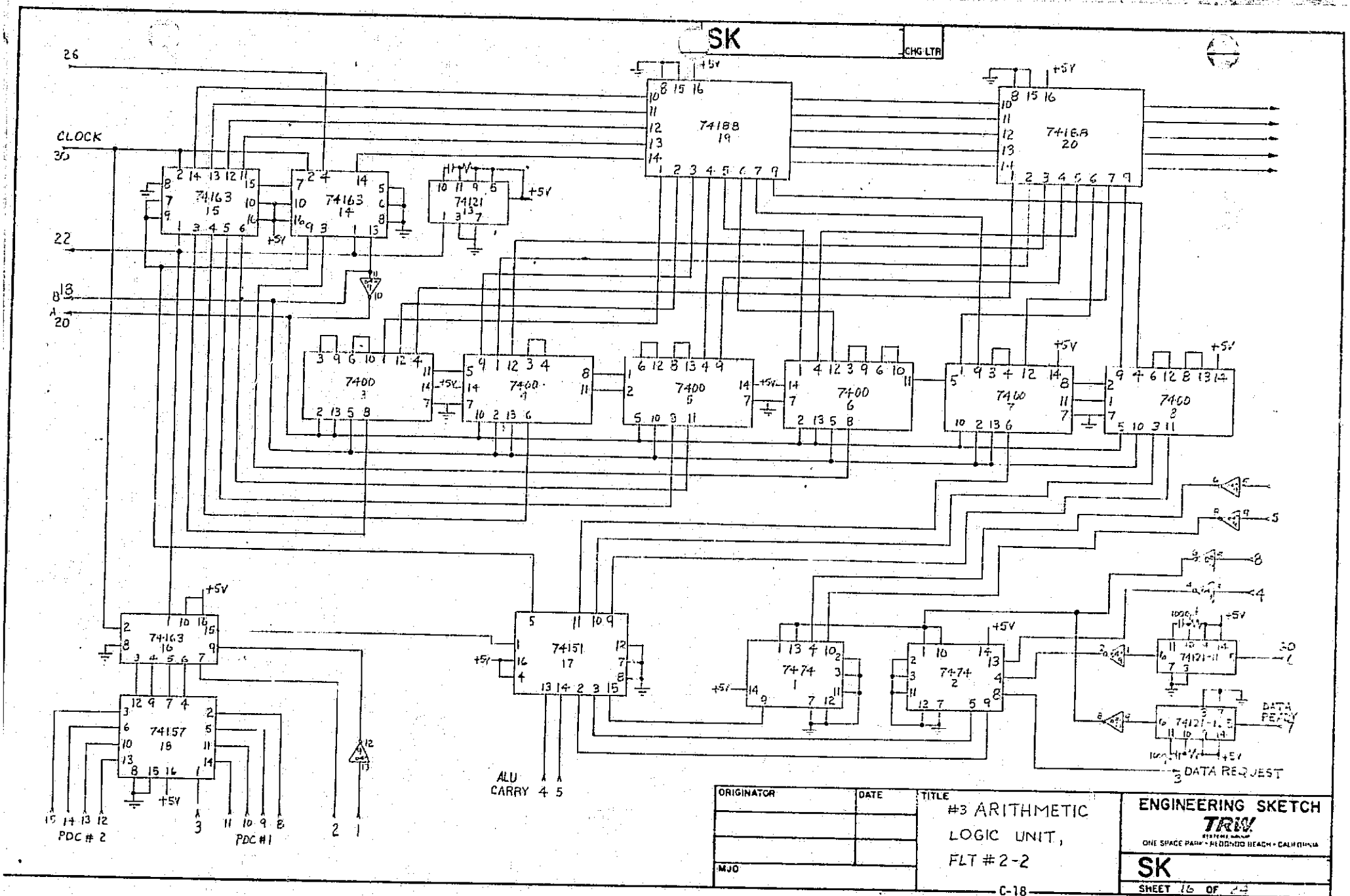
TRW SYSTEMS GROUP

ONE SPACE PARK • REDONDO BEACH • CALIFORNIA

SK

SHEET 15 OF 24

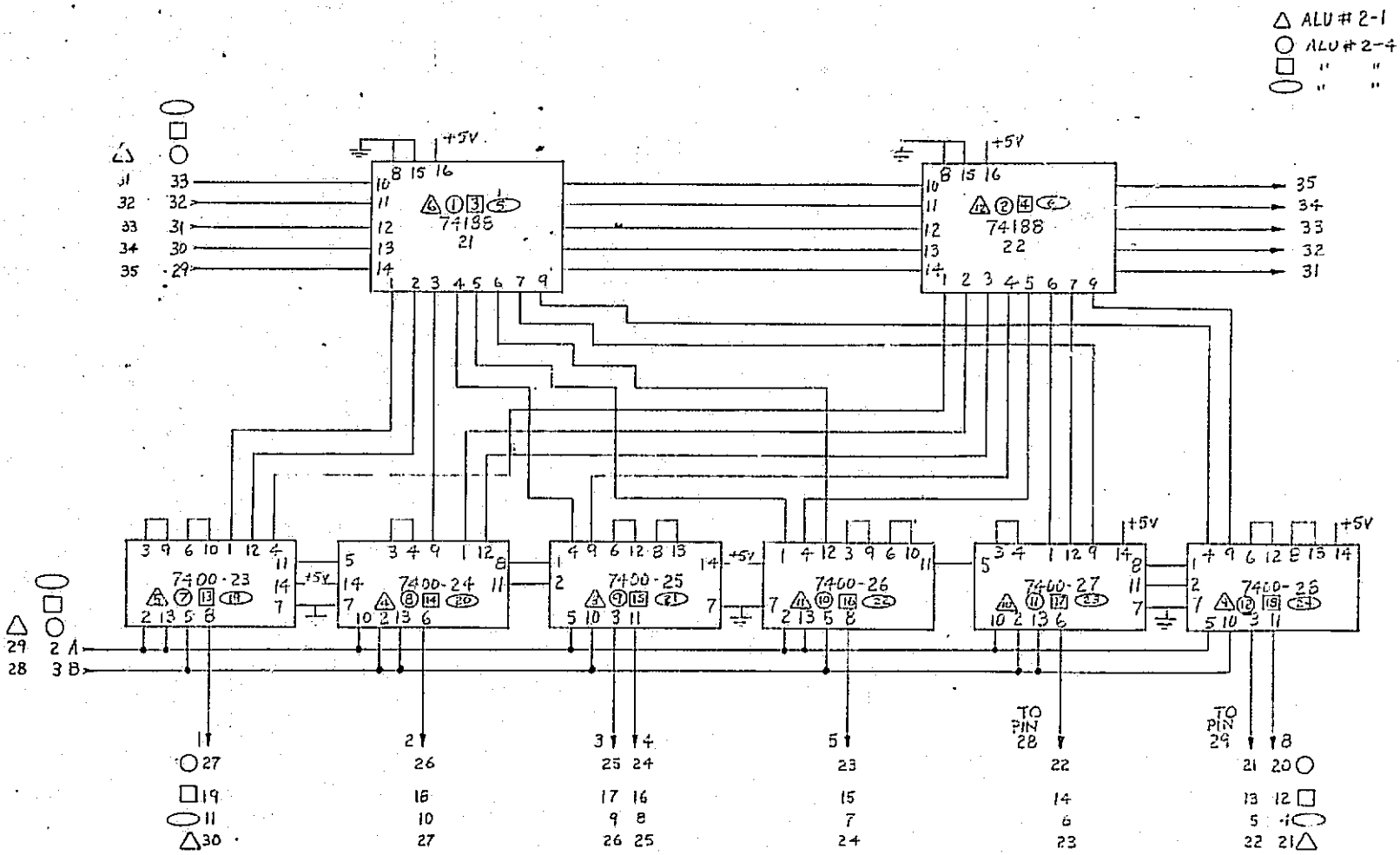
C-17



REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR

SK

CHG LTR



ORIGINATOR	DATE	TITLE
		#3 ARITHMETIC LOGIC UNIT, FLT#2-2, 2-1, AND 2-4
MJO		

ENGINEERING SKETCH

TRW SYSTEMS GROUP

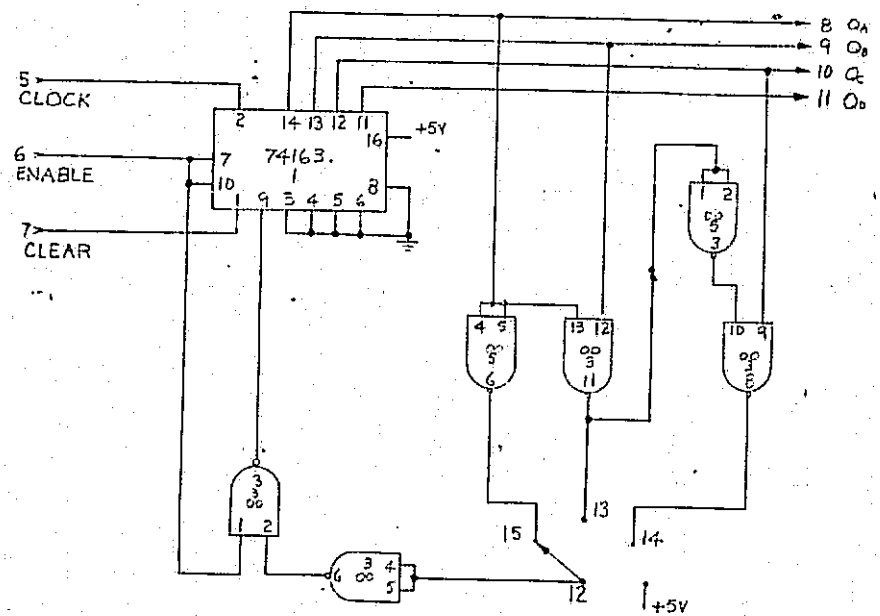
ONE SPACE PARK • REDONDO BEACH • CALIFORNIA

SK

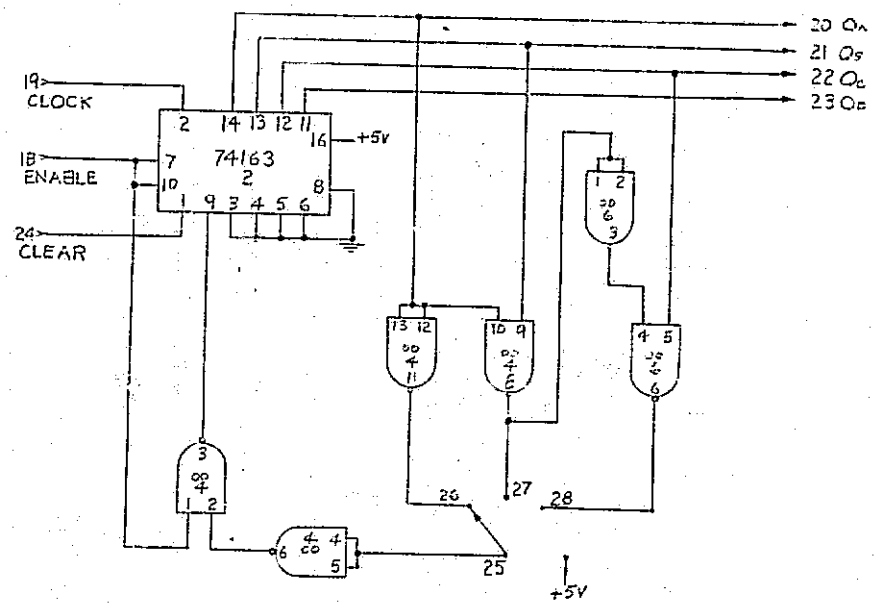
SHEET 17 OF 24

SK

CHG LTR



DATA & ERROR MEM. ADD.



RANGE MEM.

ORIGINATOR	DATE	TITLE
		DATA & ERROR MEM. ADDRESS AND RANGE MEM., FLT # 2-3
MJO		

ENGINEERING SKETCH

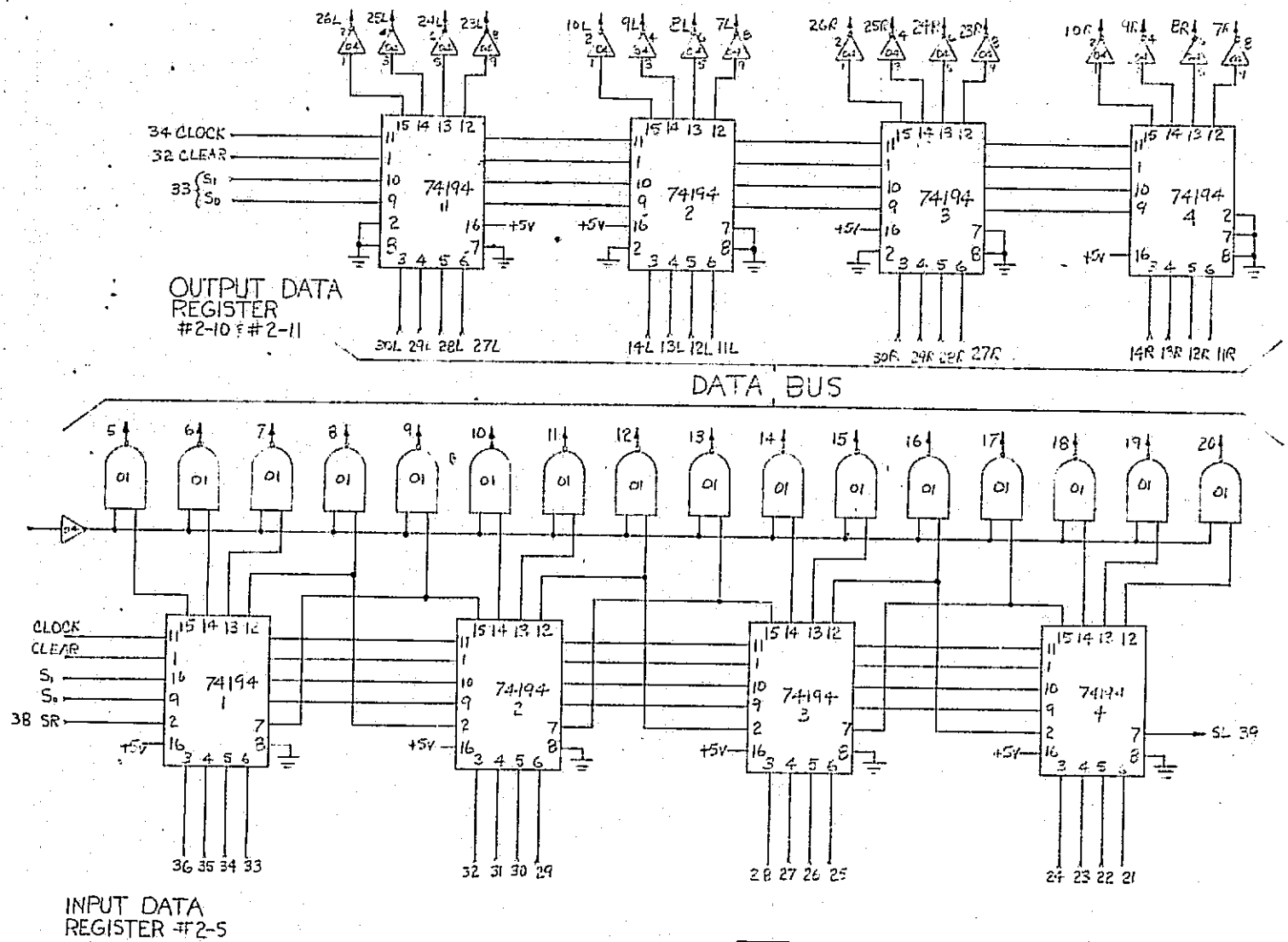
TRW SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH • CALIFORNIA

SK

SHEET 16 OF 16

SK

CHG LTR



ORIGINATOR	DATE	TITLE
		DATA REGISTERS
		FLT #2-5, #2-10 & #2-11
MJO		

C-21

ENGINEERING SKETCH

TRW

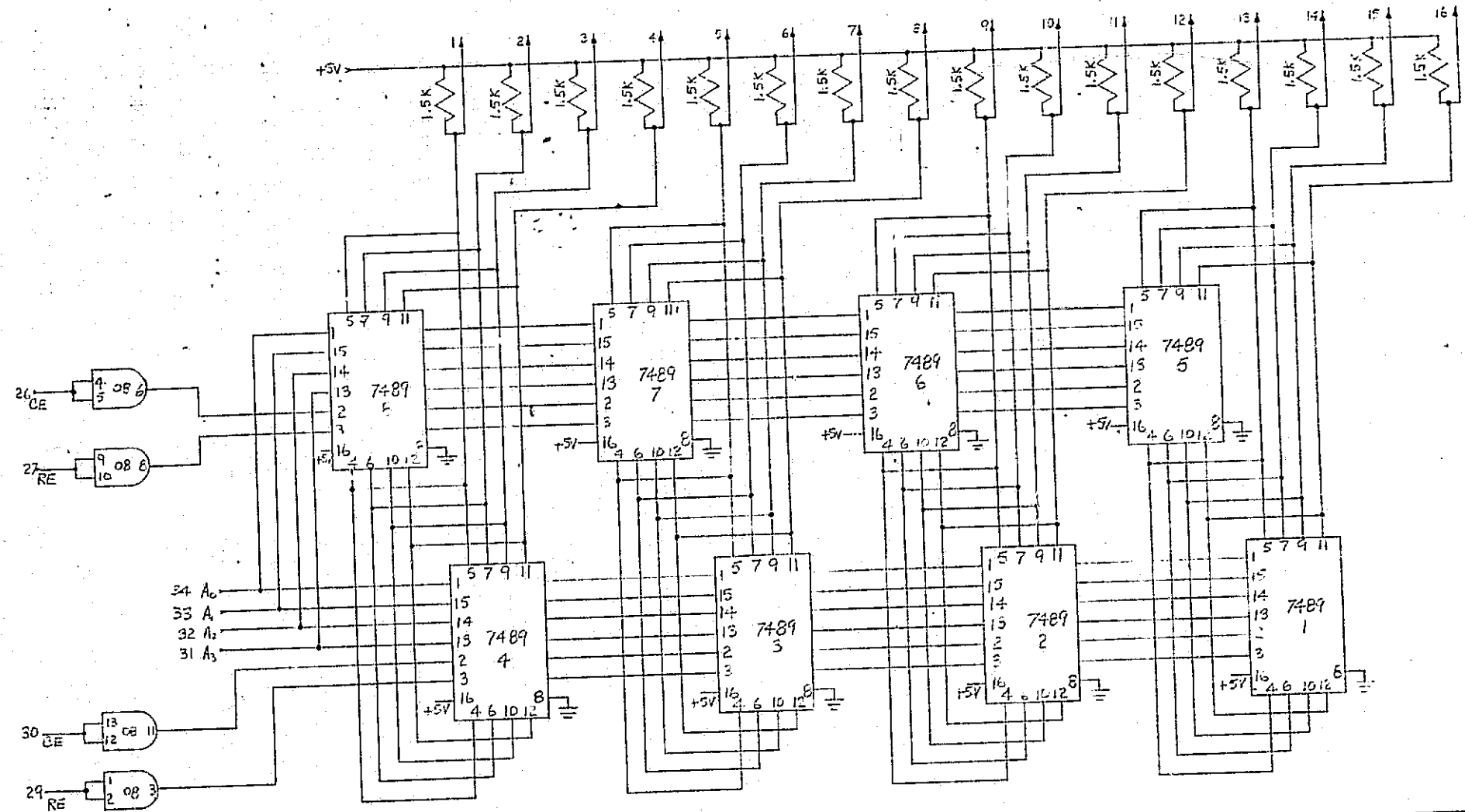
ONE SPACE PARK • REDONDO BEACH • CALIFORNIA

SK

SHEET 19 OF 24

SK

CHG LTR



ORIGINATOR	DATE	TITLE
		MEMORY # 2-6
MJO		

C-22

ENGINEERING SKETCH

TRW SYSTEMS GROUP

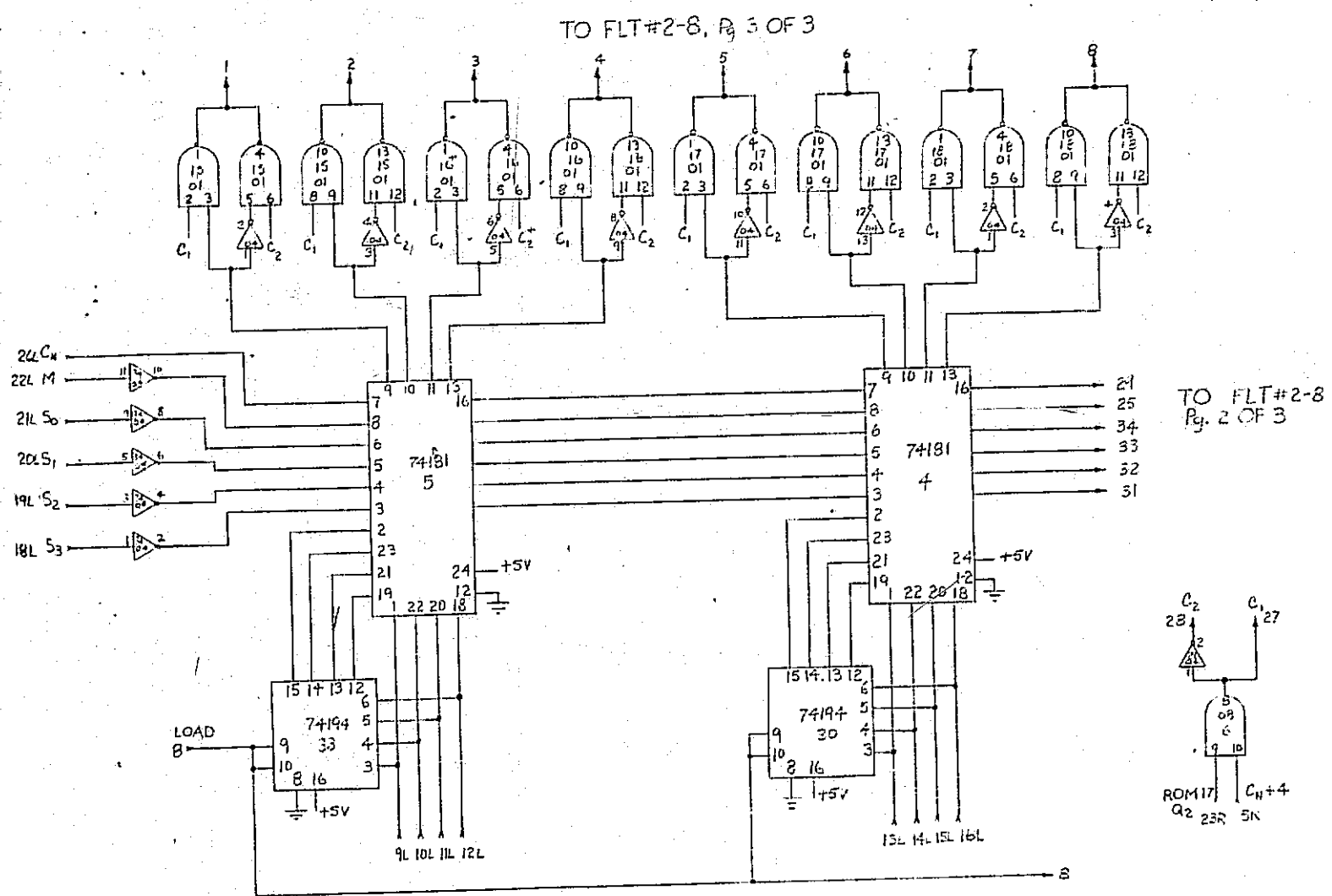
ONE SPACE PARK • REDONDO BEACH • CALIFORNIA

SK

SHEET 25 OF 34

SYSTEMS DEV. DIV.

SK | CHG LTR



ORIGINATOR	DATE	TITLE
		#1 ARITHMETIC LOGIC UNIT, FLT#2-8, Pg 1 of 3
MJO		

C-23

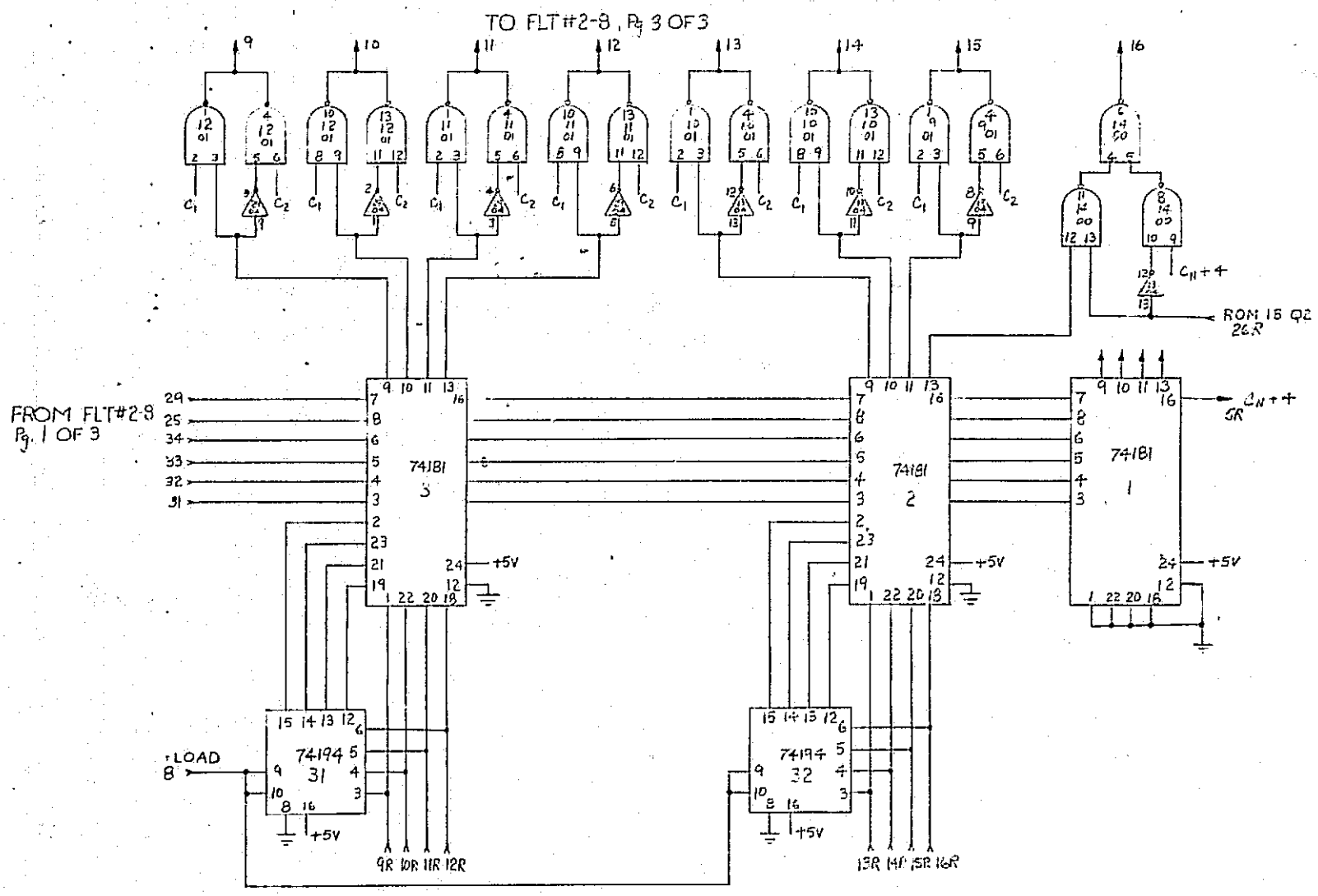
ENGINEERING SKETCH
TRW SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH • CALIFORNIA

SK

SHEET 21 OF 24

SK

CHG LTR



ORIGINATOR	DATE	TITLE
		#1 ARITHMETIC LOGIC UNIT FLT #2-8, Pg 2 of 3
M/O		

C-24

ENGINEERING SKETCH

TRW SYSTEMS GROUP

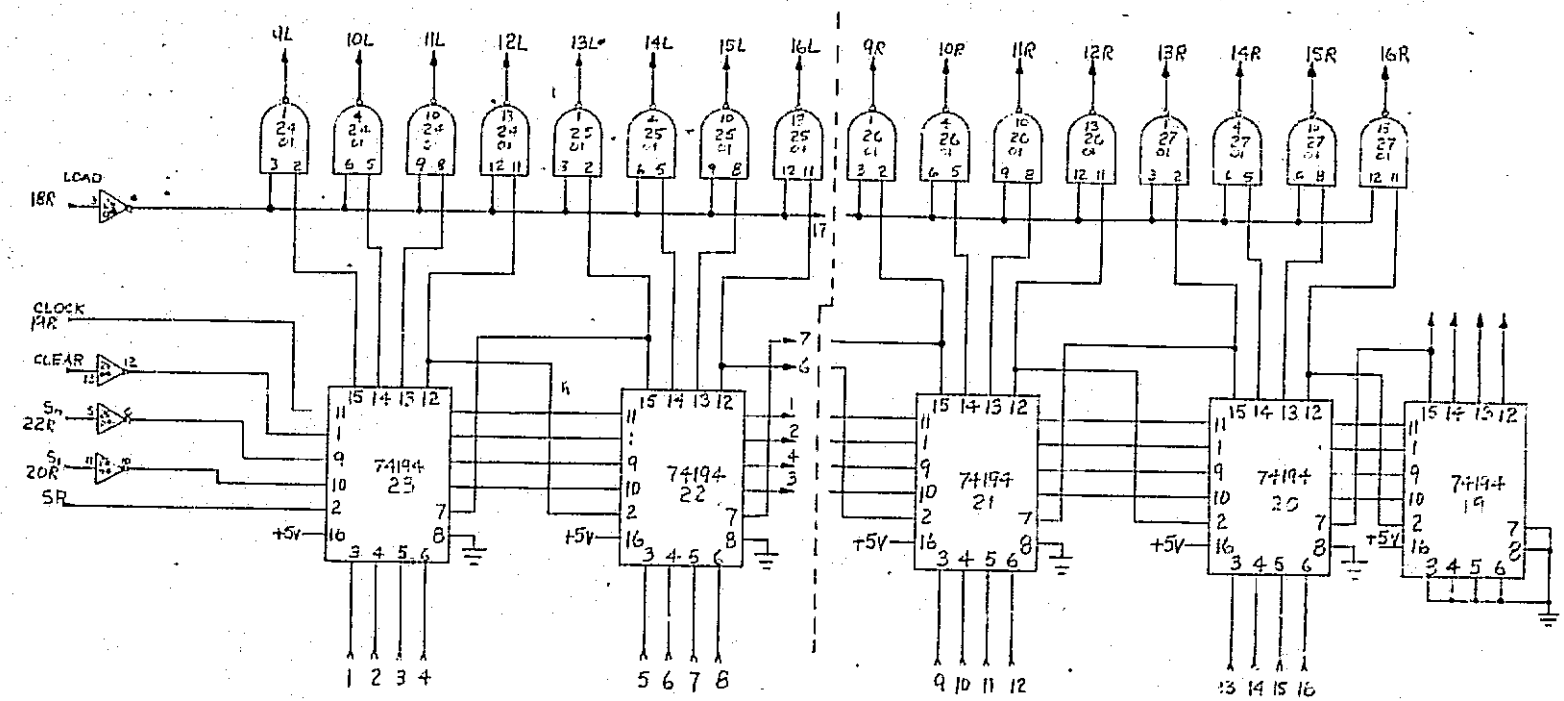
ONE SPACE PARK • REDONDO BEACH • CALIFORNIA

SK

SHEET 22 OF 24

SK

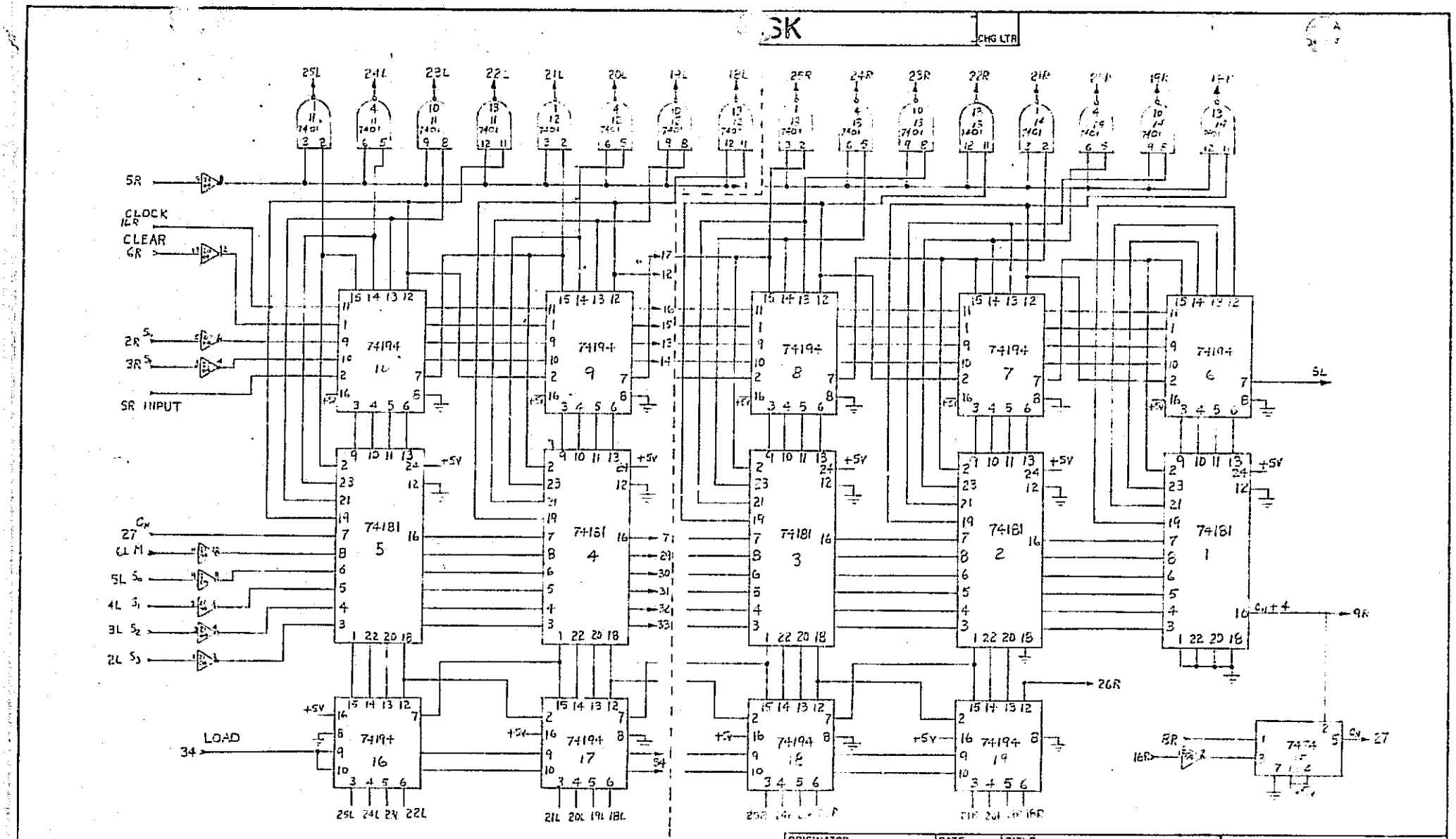
CHG LTR



FROM FLT #2-8
Pg 1 OF 3

FROM FLT #2-8
Pg. 2 OF 3

ORIGINATOR	DATE	TITLE	ENGINEERING SKETCH
		#1 ARITHMETIC LOGIC UNIT, FLT # 2-8, Pg 3 of 3	TRW SYSTEMS GROUP ONE SPACE PARK • REDONDO BEACH • CALIFORNIA
MJO			SK
			SHEET 25 OF 24



ORIGINATOR	DATE	TITLE
		#2 ARITHMETIC LOGIC UNIT FLT #2-9
MJO		

ENGINEERING SKETCH
TRW
SYSTEMS GROUP
ONE SPACE PARK • REDONDO BEACH • CALIFORNIA

SK

SHEET 24 OF 24