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NAS 9-14444

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10/31/75

Preliminary Redundancy Management/Multi-Flight Computer Modeling Analysis Final Report

3/26/75

Objectives

The objective of this task was to determine the effect of Multi-Flight Computer Operations and Update Blocks on the CPU utilization, elapsed times, and execution jitter of the ALT Flight Software (FSW). These objectives have been accomplished with results presented at the FSW ALT Preliminary Design Review.

Summary of Findings

Preliminary analysis indicates a total additional CPU cost of about 13% for the Approach and Landing Phase of ALT-10% for Update Blocks, 2.5% for GPC synchronization, and approximately 0.5% for MTU Redundancy Management. This figure does not include any Update Blocks for SM; however, the cost of these, if there are any, should be small relative to the 10% for GN&C Update Blocks.

Transport lag increased to an average of 15.9 ms (from 14.3 ms without these functions). Maximum transport lag increased to 18.5 ms (from 16.9). Critical input sampling jitter remained the same.

Detailed Findings

Update Blocks were added to the GN&C portion of the model as follows: 3 Update SVC's were added to the Fast Cycle Executive (1 at 25 Hz, 2 at 12.5 Hz), and 4 Update SVC's were added to the Mated/Drop Executive (all at 12.5 Hz) (see Reference 1). Excluding synchronization, the FCOS overhead for these 100 Updates/second was 2.5% ($\sim$250μsec each). The application processing within these blocks added 7.5% to the CPU utilization.

GPC Synchronization was performed for the following events: Update Blocks, Wait for Event, Satisfaction of an Event Wait (via SET or SIGNAL), Timer Interrupts, and I/O Input Completions for all devices except the PCMMU. This resulted in about 400 synchronizations/second at a total CPU cost of 2.5%. Information on when synchronization should be performed was obtained from Reference 2. Even if the number of sync points should double, synchronization costs would only rise to 5%.

MTU Redundancy Management costs were estimated to be about 0.5%. At a 12.5 Hz rate, this is about 400μsec per execution of the function. Since 12.5 Hz is the maximum rate at which MTU RM will be performed (nominal rate is 2 Hz) the cost per exeuction could double and the total cost would not exceed 1%.

The transport increase of 1.6 ms was caused as follows:

.62 ms application processing within an Update block
.25 ms FCOS processing for the Update block
.42 ms FCOS processing for 7 syncs
.30 ms misc time due to model variability

1.59 ms Total

Future Analysis

Future efforts in this area should include the following steps:

1) Obtain data on the usage of Update blocks by SM.

2) Improve the model of synchronization by charging a variable CPU cost based on the number of times the sync routine must loop waiting for other GPC's. Currently only an average time is charged.

3) As the design of MFC progresses, verify the points where synchronization must be performed and obtain a better estimate of the cost of the MTU RM function.

4) Add these functions to the baseline FSW model to be used in all future analysis.

References:

1. Informal information from W. Madden

2. Digital Development Memo #865, "Quantitative Analysis of GPC Synchronization Methods", from Charles Stark Draper Labs, Inc., dated 1/10/75.

DOWNLIST DATA STALENESS FEASIBILITY ANALYSIS

FINAL REPORT

May 23, 1975

PURPOSE

The purpose of this task was to determine the feasibility of using the Flight Software model to generate tables showing the staleness of the different downlist data items. This purpose has been accomplished.

SUMMARY OF RESULTS

The Flight Software model can be used to generate staleness information. The attached tables show the staleness distribution for six selected downlist data items in two different simulation runs. Staleness is relatively constant for those data items whose collection rate is an integral multiple of their downlist rate; for those data items which are collected and downlisted at non-integral rates (e.g. collected at 12.5HZ and downlisted at 5HZ), however, the staleness is quite variable from sample to sample. More detail is given below.

FINDINGS

The Flight Software model corresponding to the 2/17/75 Functional Design Specification was used for this study. The six data items used were collected via I/O requests from the Fast Cycle Executive and downlisted at rates of 12.5, 5, or 1HZ (see Table 1). Staleness for each downlist item was computed as the time between reading the data at the MDM and placing it in the downlist buffer.

Two simulation runs, each simulating 4 seconds of time, were made for the study. In the first run (results shown in Figures 1, 2, and 3), the CPU estimates given in the 2/17/75 FDS were used, creating an overload condition. However, since the Fast Cycle Executive and the Downlist are the two highest priority tasks, they were always able to complete processing before their next execution was scheduled. A second run, with all CPU estimates reduced by 50%, was made to investigate the effects of timing variations on the results. Results of this run are shown in Figures 4 and 5.

The timeline in Figure 1 shows the approximate times of gathering inputs and downlisting data for a 1/2 second period of the first run (full CPU estimates). The line above the time bar shows the active periods for the Fast Cycle Executive (periods from timer interrupts going off until CLOSE is issued) with the approximate times for gathering data via the three input requests. The line below the bar shows Downlist periods of activity with the approximate times of downlisting the various items. (Item D6 not shown because not downlisted in this period).

Figures 2 and 3 show the staleness information for the six data items in the first run (full CPU estimates); Figures 4 and 5 show the same information for the second run (reduced CPU estimates). Each graph shows staleness of data in milliseconds versus the number of samples in that range. Although there are some differences between the corresponding downlist items in the two runs, the general conclusions given below are valid for each run.

CONCLUSIONS

Two factors influence the variability of data staleness in the two runs. The first is that the Fast Cycle Executive performs much more work on odd execution cycles than on even. This causes the Downlist process to delay beginning its processing on its odd cycles until the Fast Cycle Exec finishes. A data item downlisted at a rate of every 1st, 3rd, 5th, ... execution of the Downlist process will thus alternate between rapid downlisting and waiting for the Fast Cycle Exec to finish. The data item 'Fwd Atch Pt Cap', (3rd graph in Figure 2) which is downlisted every fifth cycle of the Downlist process, demonstrates this effect.

The second factor influencing the variability of staleness, which has a much more significant effect, is the condition of downlisting at a rate not evenly divisible into the data collection rate (e.g. collect data at 12.5HZ and downlist at 5HZ). This creates a very large variability in the amount of staleness. The first and third graphs in Figures 3 and 5 demonstrate this effect.

Current efforts towards reducing the cost of Downlist will, if successful, permit a larger skew of the Downlist Process away from the Fast Cycle Executive (perhaps 25 ms); this will largely alleviate the staleness variability caused by the first factor mentioned above. No solution is apparent for the second factor mentioned, except for making the collection and downlisting rates compatible.

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Table 1 - Data Items Used for Staleness Computations

Downlist Item	Sample Rate, Source	Downlist Rate	Execution Cycles When Downlisted
D1 - Gyro Roll Rate	25HZ, GN&C Input #1	12.5HZ	1,3,5,7,9, ...
D2 - IMU IOR	12.5HZ, GN&C Input #3	12.5HZ	2,4,6,8,10, ...
D3 - Fwd Atch Pt Cap	25HZ, GN&C Input #2	5HZ	1,6,11,16, ...
D4 - GN IMU Fail	12.5HZ, GN&C Input #3	5HZ	3,8,13,18, ...
D5 - LH RHC Roll	25HZ, GN&C Input #1	1HZ	5,30,55, ...
D6 - IMU Plat Temp Ready	12.5HZ, GN&C Input #3	1HZ	15,40,65, ...

Figure 1. Downlist And Fast Cycle Exec - Periods Of Activity

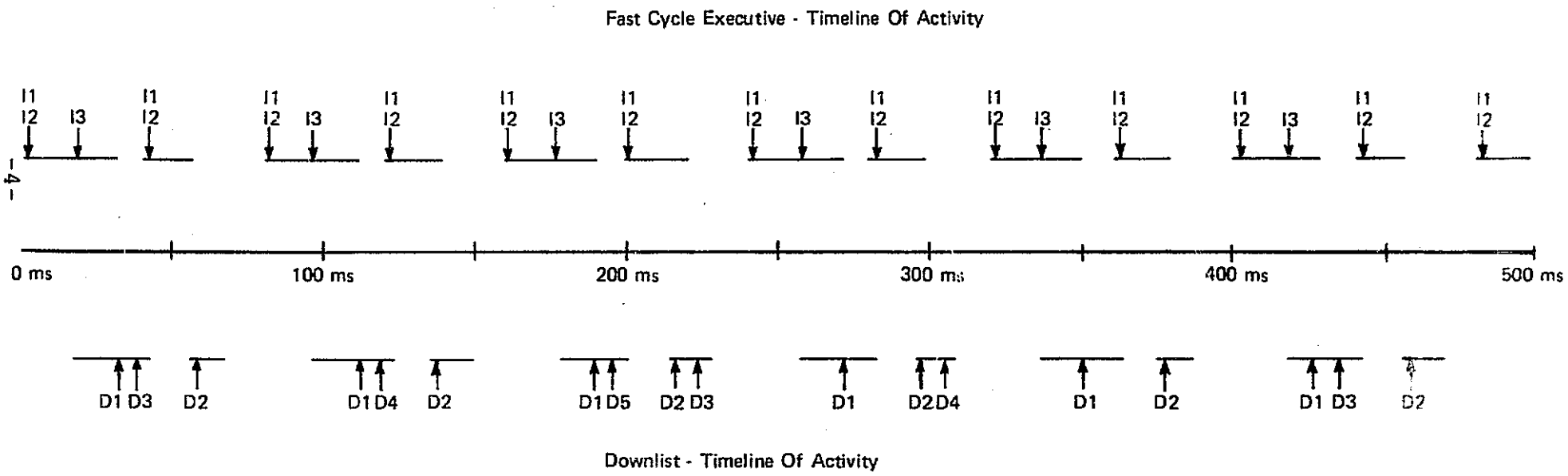
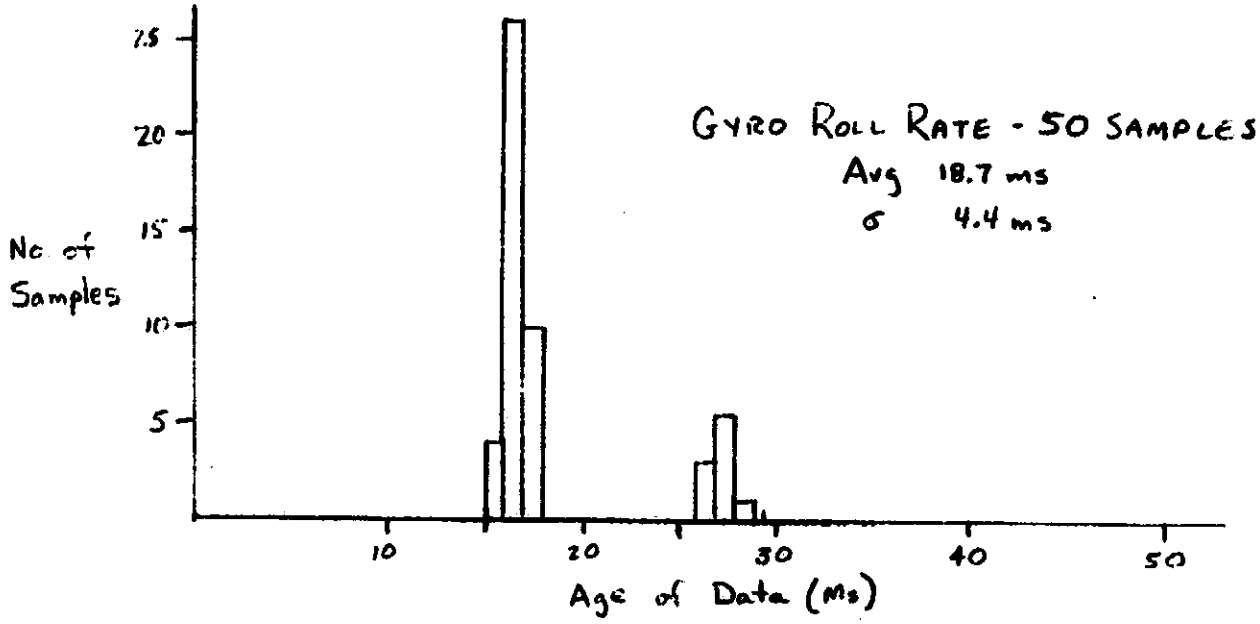


Figure 2

DATA [illegible] FULL CPU ESTIMATES



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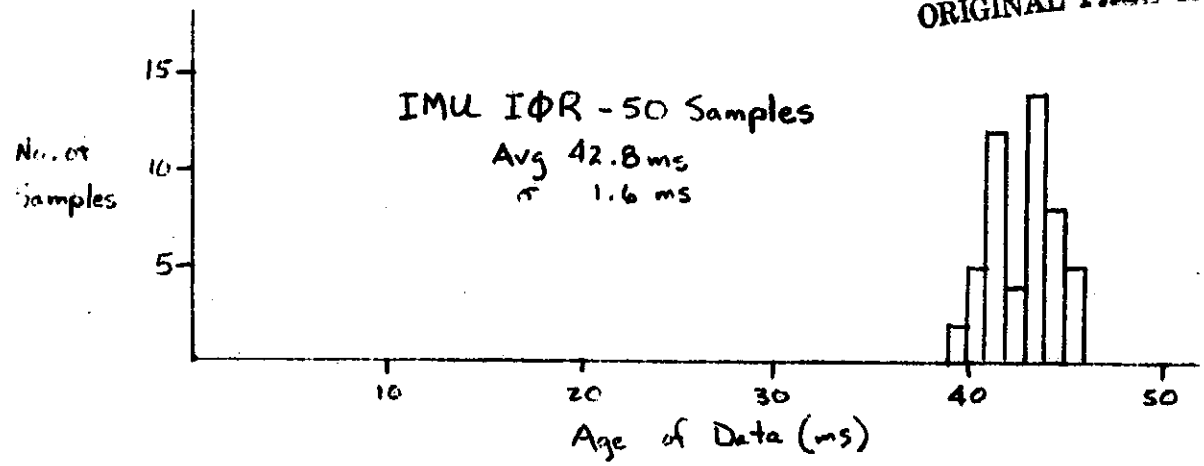


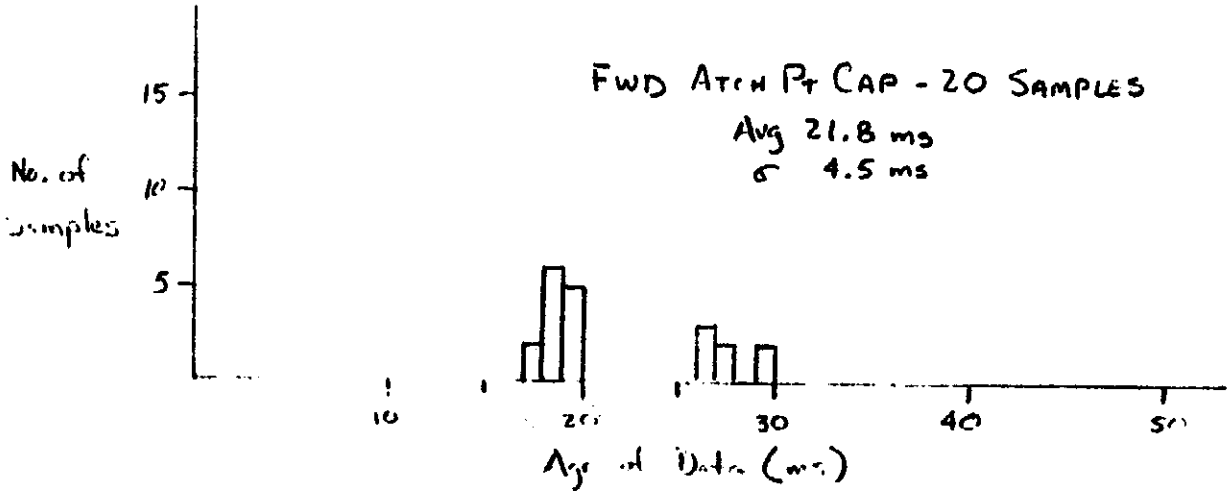
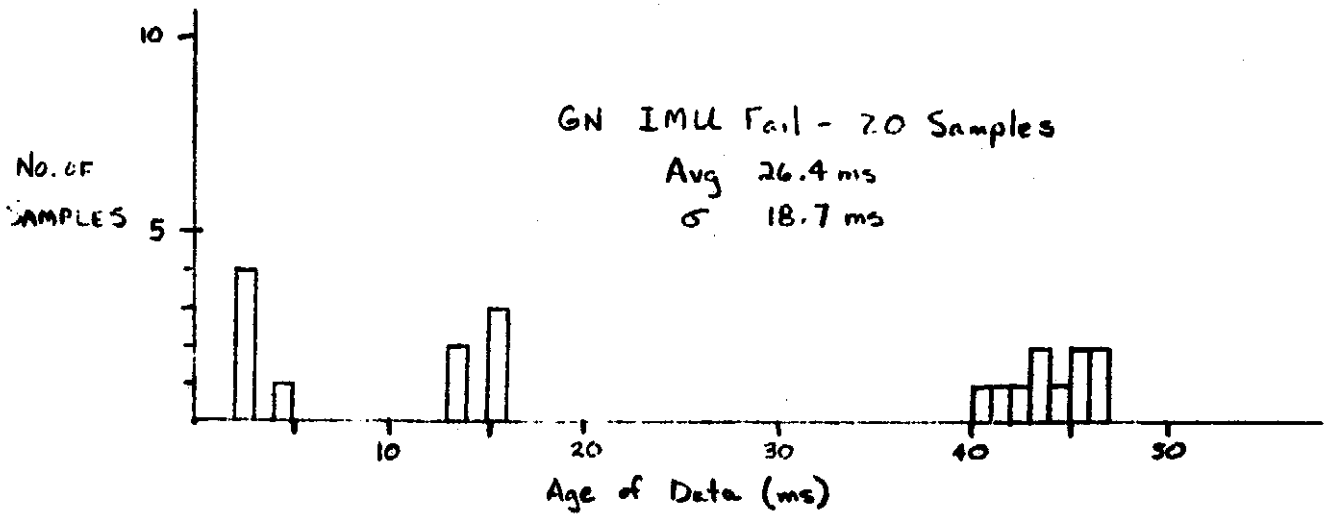
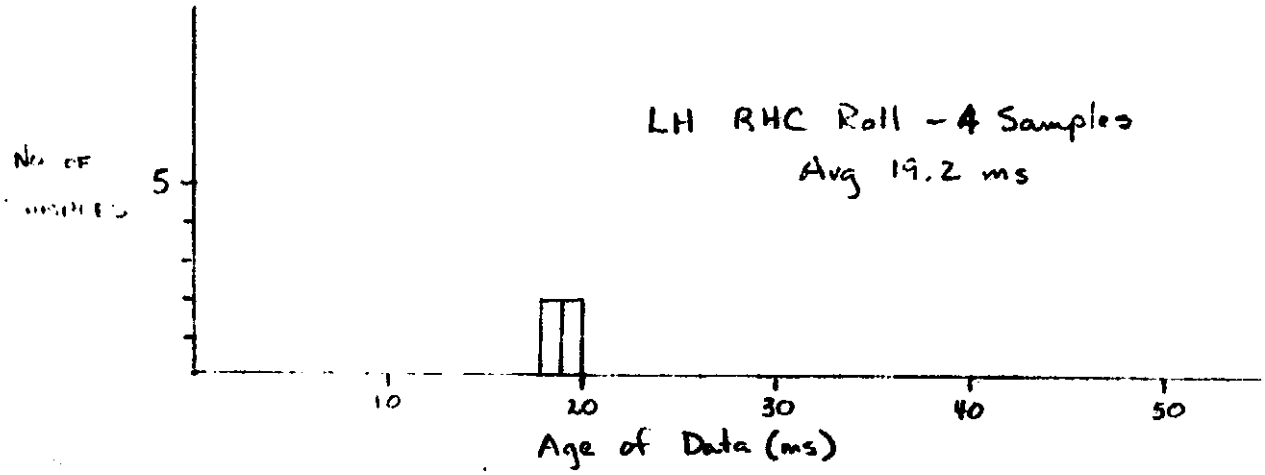


Figure 3

DATA [illegible] ESTIMATES





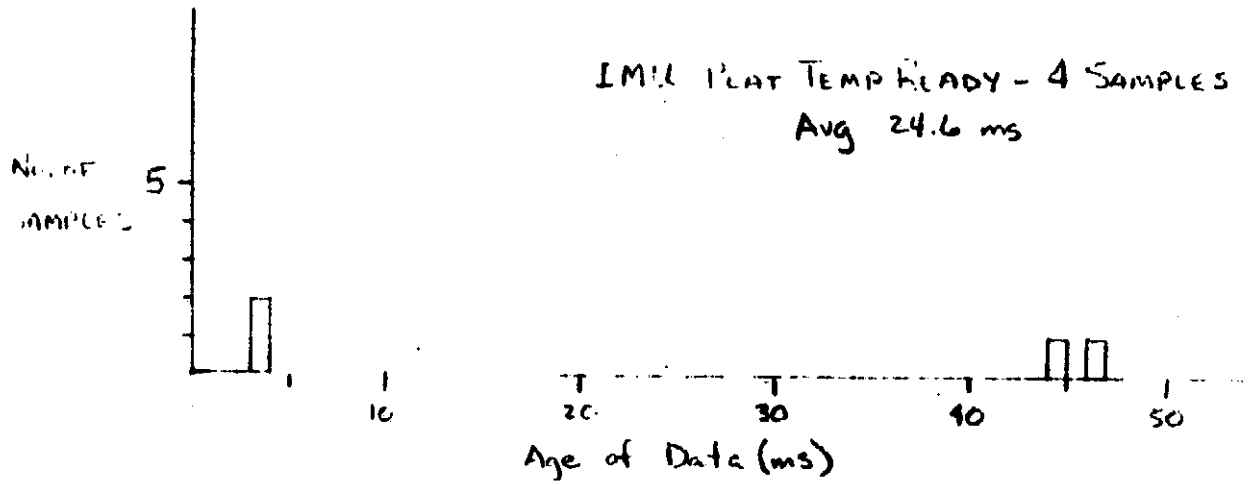
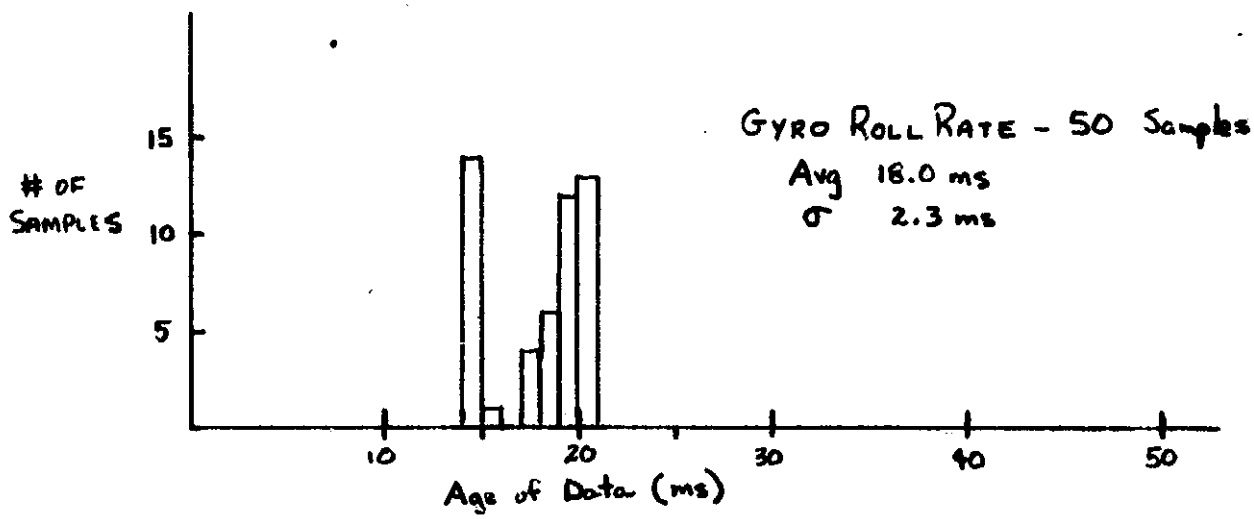
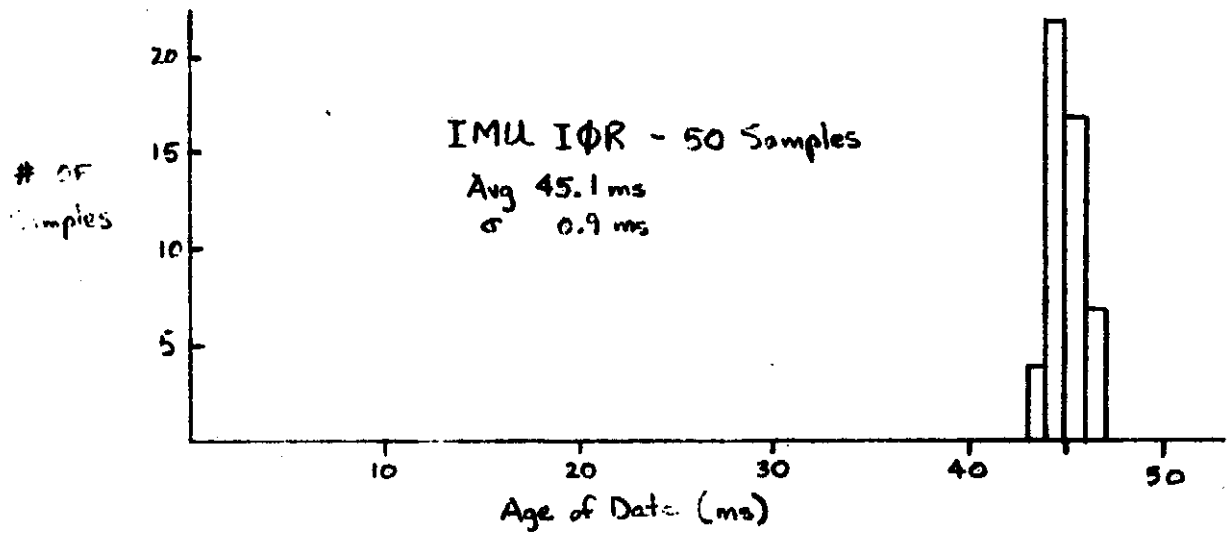


Figure 4

DATA STALENESS - ALL CPU ESTIMATES HALVED





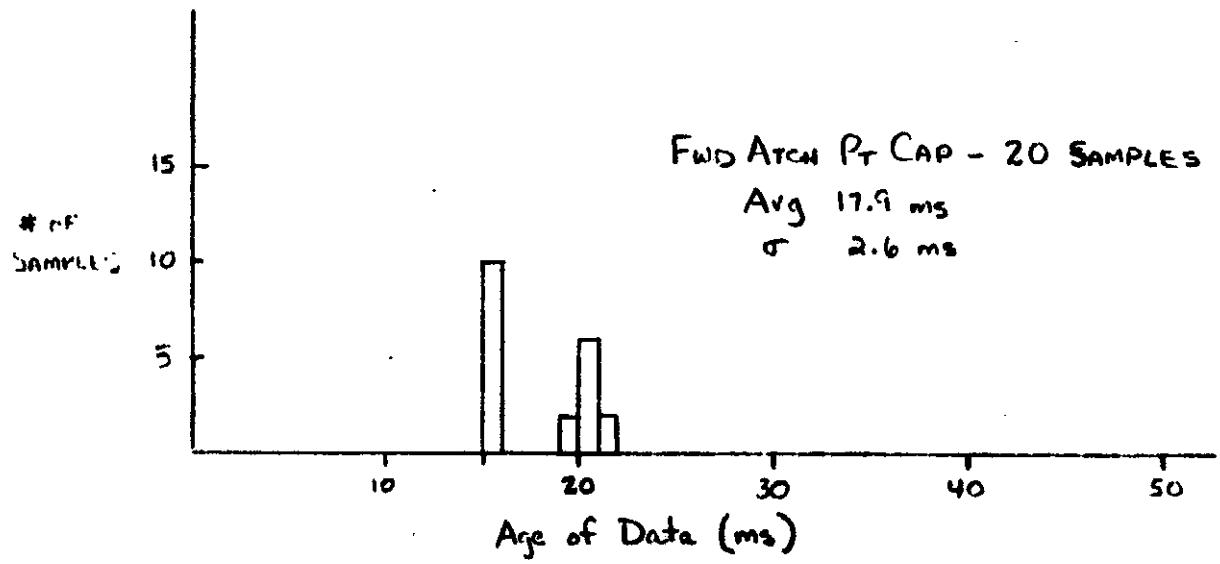
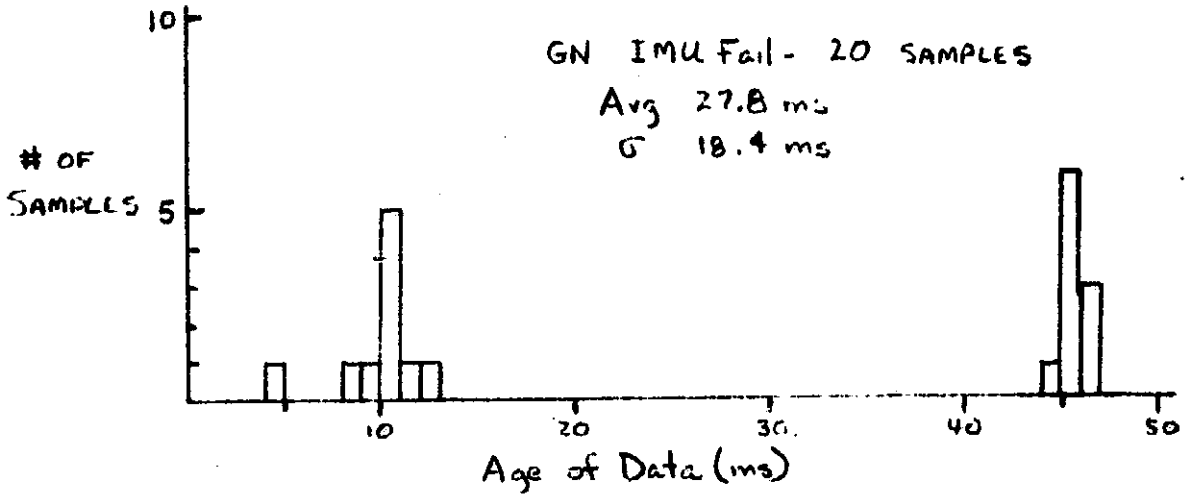


Figure 5

DATA TIMELINESS - ALL CPLL ESTIMATES HALVED



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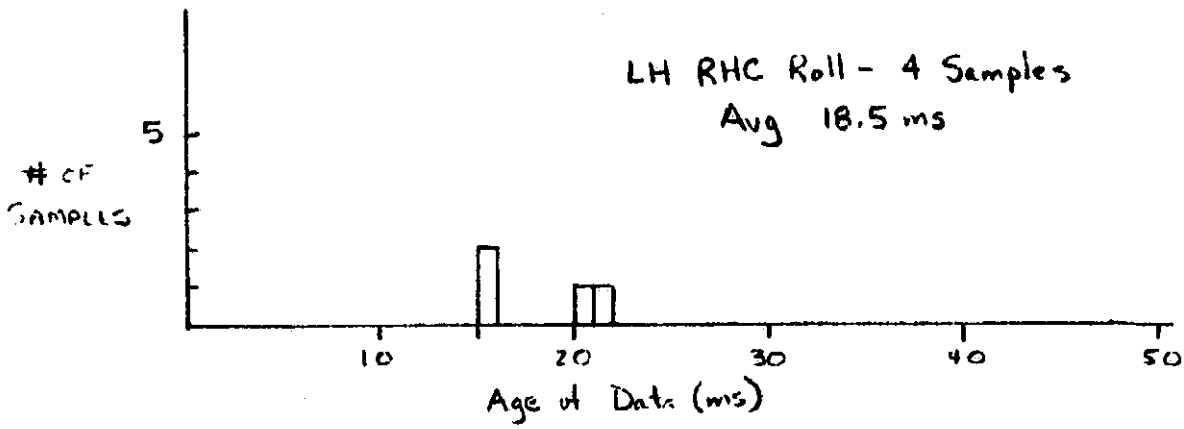

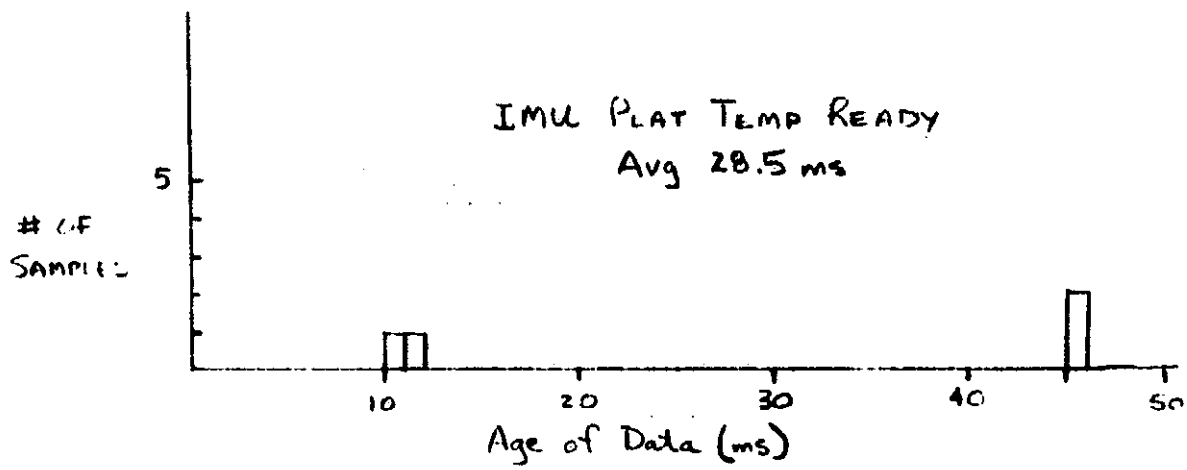

ADL2 PERFORMANCE ANALYSIS

FINAL REPORT

6/4/75

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PURPOSE AND SCOPE

The purpose of this study has been to evaluate the performance of the Flight Software ADL2 delivery. The scope of this task was limited to ADL2 cyclic functions, including the cyclic processing invoked by the IMU specialist function. GN&C was simulated in two flight control modes, manual direct and manual CAS.

OBJECTIVES

The objective of this study was to answer the following ADL2 performance questions:

1) What is the ADL2 CPU load?

2) Can all processes complete within the required cycle time?

3) What is transport lag and input sampling variation?

METHOD

All cyclic processes for ADL2 were modeled. In addition, the IMU Major Cycle Processor, which is a cyclic process invoked by the IMU specialist function, was modeled. Table 1 contains a profile of the ADL2 processes modeled. Crew inputs and demand response specialist functions were not modeled.

The inputs used in modeling UI and SM are provided in Appendix A. As in previous studies, the CPU estimates for Polling, Data Acquisition and PM Control include an assumed 15% HAL Overhead; the total CPU is moderately sensitive to this figure. Appendix B contains a breakdown of processing times for GN&C. Two cases were simulated: Case 1 had GN&C in manual CAS mode and Case 2 had GN&C in manual direct mode. The average CPU for the worst case processing load, cluster positioning, was used for the IMU Major Cycle processor. Appendix C contains the GN&C I/O profile modeled.

FINDINGS

CPU utilization for the ADL2 baseline case 1 with GN&C in manual CAS mode was 80.7% (Refer to Table 2). In a two-second simulation, one execution of the lowest priority process, IMU Major Cycle Processor, was missed because the elapsed time of its previous execution exceeded 320 ms. CPU utilization for the ADL2 baseline case 2 with GN&C in manual direct mode was 74.8% (Refer to Table 3). All processes were able to complete within their allotted time.

Table 1

Flight Computer Task Summary for ADL2

Process	Subsystem	Rate	Priority	IO Req per sec	# Waits/ Sec	# Implied Waits/Sec	#Sets, Resets
Fast Cycle Executive	GN&C	25HZ	250	175	25	25	62.5
Downlist	UI	25HZ	246	25		25	
IMU Minor Cycle Proc.	GN&C	25HZ	242		25		
Data Acquisition	SM	10HZ	234	10		10	2
MCDS Input (Polling)	UI	5HZ	230	10		10	
Preflight Executive	GN&C	12.5HZ	146		12.5		
Display Update	UI	1HZ	142	2		2	
PM Control	SM	2HZ	122		2		2
IMU Major Cycle Proc.	GN&C	3.125HZ	114				

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TABLE 2

CASE 1*

ADL2 CPU UTILIZATION

	APPL	FCOS	TOTAL
UI			
DISPLAY UPDATE	8.7	.5	9.2
POLLING	.7	1.0	1.7
DOWNLIST	11.9	3.6	15.5
UI TOTAL	21.3	5.1	26.4
SM			
DATA ACQUISITION	3.8	1.5	5.3
PM CONTROL	1.2	.2	1.4
SM TOTAL	5.0	1.7	6.7
GN&C			
FAST CYCLE EXEC*	17.2	12.9	30.1
IMU MINOR CYCLE PROC	8.4	1.7	10.1
PREFLIGHT EXEC	2.3	1.0	3.4
IMU MAJOR CYCLE PROC**	3.2	.3	3.5
GN&C TOTAL	31.1	15.9	47.0
MISC		.6	.6
TOTAL SYSTEM	57.4	23.3	80.7

*MANUAL CAS MODE

**ADJUSTED FOR 1 MISSED EXECUTION

TABLE 3

CASE 2*

ADL2 CPU UTILIZATION

	APPL	FCOS	TOTAL
UI			
DISPLAY UPDATE	8.7	.5	9.2
POLLING	.7	1.0	1.7
DOWNLIST	11.9	3.6	15.5
UI TOTAL	21.3	5.1	26.4
SM			
DATA ACQUISITION	3.8	1.4	5.2
PM CONTROL	1.2	.2	1.4
SM TOTAL	5.0	1.6	6.6
GN&C			
FAST CYCLE EXEC*	11.0	12.7	23.7
IMU MINOR CYCLE PROC	8.4	1.7	10.1
PREFLIGHT EXEC	2.3	1.1	3.4
IMU MAJOR CYCLE PROC	3.6	.3	3.9
GN&C TOTAL	25.3	15.8	41.1
MISC		.7	.7
TOTAL SYSTEM	51.6	23.2	74.8

*MANUAL DIRECT MODE

Transport lag was measured as the time data from Input 1 or 2 leaves the MDMs to the time Output 1 data arrives at the MDMs. The Fast Cycle Executive must perform 4.88 ms of transport lag processing in manual CAS mode and 2.3 ms of transport lag processing for manual direct mode. Transport lag for manual CAS mode, case 1, ranged from 10-21 ms and exceeded the required upper bound of 15 ms 22% of the time. Since manual direct mode requires 2.5 ms less transport lag processing, transport lag results for case 2 were better. The range was 7-16.6 ms and 2% of the cases exceeded 15 ms.

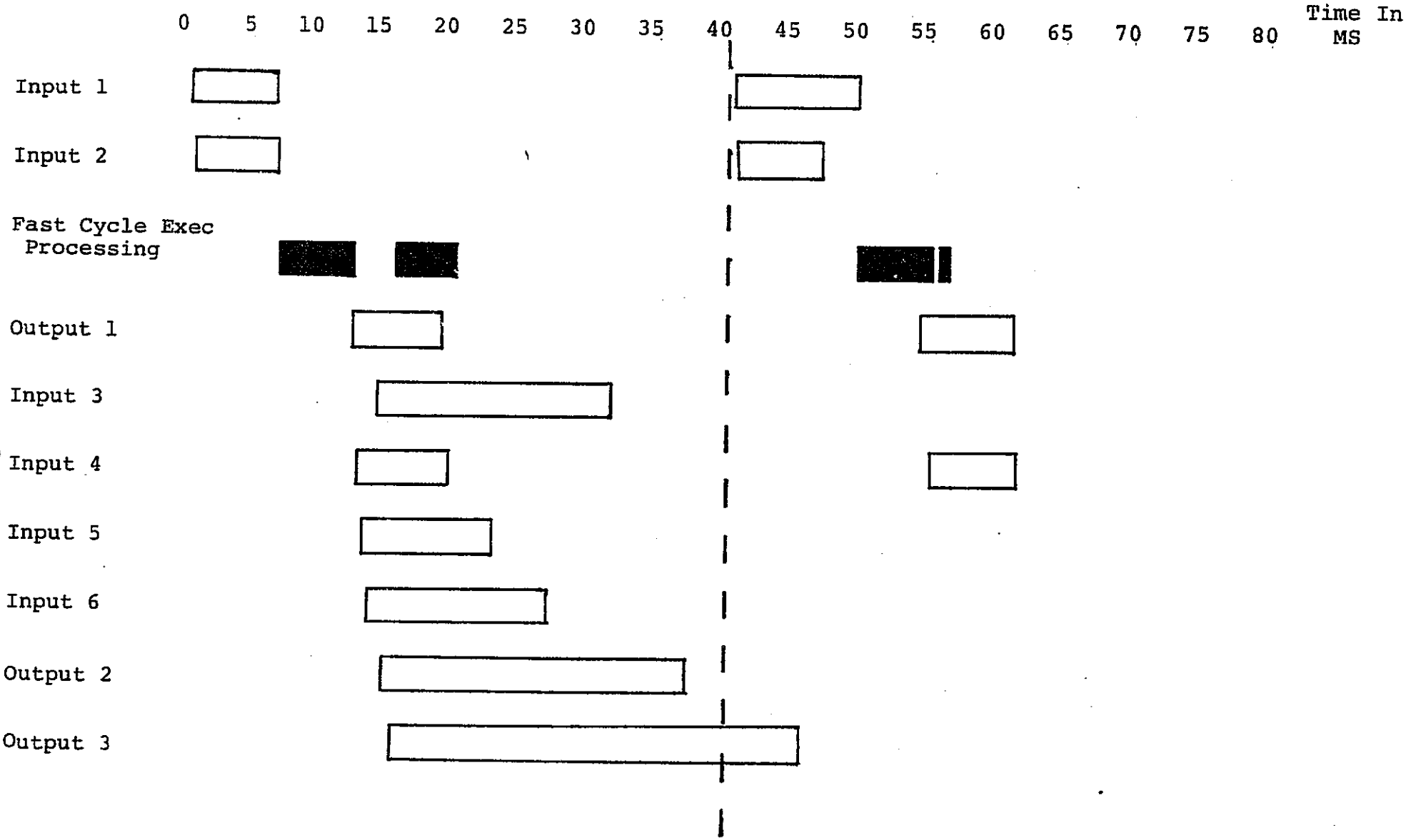
Sampling variations are defined as the variation from 40 ms of the difference in the times between succeeding samples of Input 1 data on the FF MDMs and Input 2 data on the FA MDMs. Sampling variation results for Input 1 showed that 78% of the samples exceeded .8 ms in manual CAS mode and 54% of the cases exceeded .8 ms in manual direct mode. The requirement is that not more than 4% can exceed .8 ms. The maximum sampling variation exceeded the required 4 ms upper limit in 24% of the samples for manual CAS mode and in 8% of the samples for manual direct mode. In manual CAS mode the sampling variation was as high as 9.4 ms and in manual direct mode it was as high as 6.4 ms. The sampling variation for the FA MDM (Input 2) meets requirements for both GN&C modes.

Factors that contribute to transport lag and sampling jitter are discussed in detail in the FSW ALT PDR Analysis Report. An additional contributing factor is that the ALT PROM chained input 3 is broken into 4 separate read requests, inputs 3, 4, 5 and 6, for ADL2. Although these requests are issued before the close of the Fast Cycle Executive, they are not complete before the start of the next minor cycle. Thus, on every even cycle Input 1 is delayed because the FF MDM is busy with I/O requests issued on the previous odd cycle. Figure 4, a profile of elapsed times for GN&C I/O requests, illustrates the contention for the FF MDMs.

The best way to eliminate this contention is to reduce the number of I/O transactions to the FF MDMs on the odd minor cycles. Since MSBLS data is not processed for ADL2, both cases were run with Input 6 (MSBLS) deleted. Without Input 6, transport lag and sample variation requirements were met for the manual direct mode. By deleting input 6 and by moving output 3 (DDU) to the even minor cycles, transport lag and sample variations were met for manual CAS mode. Refer to tables 5 and 6 for a summary of transport lag and sample variation results.

TABLE 4

GN&C I/O PROFILE FOR 2 AVERAGE MINOR CYCLES FROM CASE 1*



Elapsed time for I/O request; includes FCOS and IOP servicing of request, wait time for free BCEs and data transfer time.

Application Processing

*GN&C in manual CAS mode

TABLE 5

ADL2 TRANSPORT LAG RESULTS

CASE	AVG. T.L (MS)	RANGE OF T.L (MS)	% OF CASES GT 15MS
BASELINE MANUAL DIRECT MODE	10.4MS	7-16.6MS	2%
BASELINE MANUAL CAS MODE	13.5MS	10-21MS	22%
MANUAL DIRECT WITH INPUT 6 (MSBLS) DELETED	10MS	7.4-12.2MS	-
MANUAL CAS WITH INPUT 6 (MSBLS) DELETED	12.6MS	10.4-15.6MS	2%
MANUAL CAS WITH NO INPUT 6 AND OUTPUT 3 (DDU) MOVED TO EVEN CYCLE	12.3MS	10-14MS	-

TABLE 6

ADL2 SAMPLING VARIATION RESULTS

CASE	INPUT 1(FF)- % GT .8MS	INPUT 1(FF)- % GT 4MS	INPUT 1(FF)- MAX. JITTER	INPUT 2(FA)- % GT .8MS
BASELINE MANUAL DIRECT MODE	54%	8%	6.4MS	-
BASELINE MANUAL CAS MODE	78%	24%	9.4MS	-
MANUAL DIRECT MODE WITH INPUT 6(MSBLS) DELETED	4%	-	2.6MS	-
MANUAL CAS MODE WITH INPUT 6(MSBLS) DELETED	14%	-	3.8MS	-
MANUAL CAS WITH NO INPUT 6 AND OUTPUT 3 (DDU) MOVED TO EVEN CYCLE	2%	-	1MS	-

RESULTS AND RECOMMENDATIONS

CPU utilization for cyclic ADL2 processes is 80.7% for manual CAS mode and 74.8% for manual direct mode. With 80.7% CPU utilization the lowest priority process was not always able to complete within its cycle rate. If more accurate CPU estimates are desired, ADL2 CPU utilization should be resized when CPU estimates based on ICS processing times are available for Polling, Data Acquisition and PM Control.

If it is determined that CPU for ADL2 should be reduced, one way would be to implement the new Downlist design for ADL2. This design, consisting of executable tables, would reduce the 15.5% CPU cost for Downlist to 5.1%.

Although transport lag and sample variations requirements are not met for the ADL2 baseline, these requirements can be achieved by redistributing the 12.5 hz I/O requests for the FF MDM over the odd and even minor cycles, as described in Findings.

REFERENCES

Flight Software ALT PDR Analysis Report by K. L. Williams, 3/21/75.

APPENDIX A

SM INPUTS FOR ADL2

- BASED ON ESTIMATED INSTRUCTION COUNTS 2.5μ INSTRUCTION PLUS 15% HAL OVERHEAD

DATA ACQUISITION

- 1 PMU READ/CYCLE FOR AN AVERAGE OF 39 WORDS
- 387 16-BIT WORDS READ PER SECOND
- 66 INTERAPPLICATION WORDS READ PER SECOND

PM CONTROL

NO PRECONDITION, SPECIAL COMPUTATION OR LIGHT AND ALARM MANAGEMENT

FDA	MEASUREMENTS	SAMPLES
• SAMPLE RATES		
•• DISCRETE PARENTS	23 (114 DISCRETES)	46

- FAIL RATE

  1 GOING BAD PER FDA CYCLE

  1 GOING GOOD PER FDA CYCLE

DOWNLIST INPUTS

DOWNLIST (25HZ) - PROCESSING TIMES BASED ON HAL EXPANSION OF ASSEMBLY LANGUAGE INSTRUCTIONS X 2.5μ/INSTRUCTION

- THE NUMBER OF WORDS DOWNLISTED IS 1254 16-BIT WORDS PER SEC
- 3 RATE GROUPS 1/SEC, 5/SEC, 12.5/SEC
- THE NUMBER OF WORDS MOVED PER EXECUTION - 48
- NUMBER OF CONTIGUOUS DATA GROUPS PER EXECUTION - 40
- 1 PCMMU WRITE/CYCLE OF 128 WORDS; 3 CHAINED REQUESTS PER WRITE

UI INPUTS

DISPLAY UPDATE (1HZ) - PROCESSING TIMES BASED ON NUMBER OF CODED ASSEMBLY LANGUAGE INSTRUCTIONS X 2.5μ/INSTRUCTION

- 2 ACTIVE DEU'S
- DISPLAYS SUPPORTED:

  RM SENSORS AT 1HZ

  IMU CONTROL AT 1HZ

  SYSTEM SUMMARY AT 1HZ

  FCS/DED DISP AT 1HZ

DISPLAY UPDATE CPU COST INCLUDES UPDATING OF THE TWO LARGEST DISPLAYS, SYSTEM SUMMARY AND RM SENSORS.

SYSTEM SUMMARY CONTAINS:

34 ANALOGS

11 SCALARS

76 REMOTE TEXT

67 BILEVEL TEST

35 STATUS BYTE CHECK

96 X, Y COORDINATE SETS

RM SENSORS CONTAINS:

14 SCALARS

4 REMOTE TEXT

36 X, Y COORDINATE SETS

<u>POLLING (5HZ)</u> - PROCESSING TIMES BASED ON ESTIMATED INSTRUCTION COUNTS X 2.5μ/INSTRUCTION PLUS 15% HAL OVERHEAD.

APPENDIX B

FAST CYCLE EXEC. - ADL2

MODULE	EXEC. TIME(μSEC)	RATE	%CPU
EXECUTIVE SEQUENCER	96	25	0.240
FCS DATA PROCESSOR 1			
*RGA PROCESSING	331	25	0.828
*AA PROCESSING	220	25	0.550
*ELEVON FEEDBACK PROCESSING	421	25	1.052
ELEVATOR COMPUTATION	38	25	0.095
PROCEDURE LOGIC	40	25	0.100
ELEVATOR MANUAL DIRECT (MD) CONTROL ELEMENT**	356	25	0.770
AILERON MD CONTROL ELEMENT**	308	25	0.770
RUDDER MD CONTROL ELEMENT**	268	25	0.670
FCS COMMAND PROCESSOR			
ELEVON & RUDDER CMD. COMPENSATION	132	25	0.330
SPEEDBRAKE CMD. COMPENSATION	26	12.5	0.033
PROCEDURE LOGIC	40	25	0.100
FCS DATA PROCESSOR 2			
25HZ DISCRETES SELECTION FILTERING	315	25	0.788
TRIM PROCESSING	59	25	0.148
12.5HZ DISCRETES S.F.	195	12.5	0.244
PITCH & ROLL/YAW PBI PROCESSING	39	12.5	0.049
*RHC PROCESSING	860	12.5	1.075
BODY FLAP DISCRETES PROCESSING	56	6.25	0.035

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FAST CYCLE EXEC. (MANUAL DIRECT) - ADL2 (CONT.)

MODULE	EXEC. TIME (μSEC)	RATE	%CPU
*SBTC PROCESSING	200	6.25	0.125
SPEEDBRAKE TAKEOVER/STANDBY	125	6.25	0.078
*RPTA PROCESSING	467	6.25	0.292
*SPEEDBRAKE & B.F. FEEDBACK PROCESSING	210	6.25	0.131
AILERON POSITION COMPUTATION	9	1.04	0.001
*RUDDER FEEDBACK PROCESSING	105	1.04	0.011
PITCH CONTROL ELEMENT	816	12.5	1.020
ROLL/YAW C.E.	864	12.5	1.080
BODY FLAP C.E.	304	6.25	0.190
TOTAL			10.925

*1 LRU GOES THROUGH SELECTION FILTER

**IN MANUAL CAS (MC) MODE:

ELEVATOR MC CONTROL ELEMENT	1557	25	3.893
AILERON MC CONTROL ELEMENT	635	25	1.587
RUDDER MC CONTROL ELEMENT	935	25	2.338

IMU MINOR CYCLE PROCESSOR - ADL2

MODULE	EXEC. TIME	RATE	%CPU
IMU BITE PROCESSING	600	25	1.50
IMU ACCELEROMETER PROCESSING*	576	25	1.44
IMU RESOLVER PROCESSING*	1394	25	3.48
IMU GYRO TORQUE PROCESSING*	584	25	1.46
IMU MINOR CYCLE PROCESSING*	200	25	0.50
TOTAL			8.38%

*REPRESENTS 1 IMU

IMU MAJOR CYCLE PROCESSOR (3.25HZ)-ADL2

FUNCTION	MAX. % CPU	AVG (% CPU)	MIN (% CPU)
CLUSTER POSITIONING*	3.98	3.16	2.90
GROUND SEQUENCE*	3.91	1.36	1.36

*CLUSTER POSITIONING AND GROUND SEQUENCE ARE MUTUALLY EXCLUSIVE EVENTS.

PREFLIGHT EXECUTIVE - ADL2

MODULE	EXEC. TIME	RATE	%CPU
AIR DATA CONVERSION	612	12.5	0.765
AIR DATA CALCULATIONS	857	12.5	1.071
CALLS TO PROCESSING STUBS	21	12.5	.263
DISPLAY PROCESSING-IMU CONTROL MONITOR DISPLAY	145	12.5	.181
TOTAL			2.280

APPENDIX C

ADL GN&C I/O PROFILE

INPUT GROUP 1	RATE	MDM
	25HZ	FF1-4
ACCELEROMETER ASSEMBLY		
LEFT AND RIGHT RHC		
LEFT AND RIGHT SBTC		
LEFT AND RIGHT RPTA		
FF MDM DISCRETES		
INPUT GROUP 2	25HZ	FA1-4
RGA		
ASA FEEDBACKS		
FA MDM DISCRETES		
LEFT AND RIGHT AFT ATTACH PT VOLTAGES		
APU PRESSURES		
INPUT GROUP 3	12.5HZ	FF1-4
ADTA		
INPUT GROUP 4	25HZ	FF1-3
IMU		
(TIME TAG)		
INPUT GROUP 5	12.5HZ	FF1-3
TACAN		
RA		
INPUT GROUP 6	12.5HZ	FF1-3
MSBLS		

	RATE	MDM
OUTPUT GROUP 1	25HZ	FF1-4
ASA COMMANDS		
FA MDM DISCRETES SET		
FA MDM DISCRETES RESET		
OUTPUT GROUP 2	25HZ	FF1-4
FF MDM DISCRETES SET		
FF MDM DISCRETES RESET		
SPI		
TACAN CONTROL REG		
IMU TORQUE & SLEW COMMAND		
OUTPUT GROUP 3	12.5HZ	DDU1-2
DEDICATED DISPLAY UNIT #1		
DEDICATED DISPLAY UNIT #2		

IOP SOFTWARE ANALYSIS

FINAL REPORT

July 29, 1975

PURPOSE AND SCOPE

The purpose of this task was to evaluate the performance of the FCOS 5 I/O design, specifically that of the IOP Software, under the ALT I/O profile. The scope was restricted to the IOP software; the resulting change in the AP101 CPU cost of I/O Management was not addressed in the model.

OBJECTIVES

The objectives of the study were twofold: 1) use the detailed IOP model to evaluate the performance of the IOP with respect to request start jitter, DMA loading, and service response times; 2) use the results to provide parameters for I/O performance characteristics to calibrate the Flight Software (FSW) simulation model. Both of these objectives have been accomplished.

SUMMARY OF RESULTS & RECOMMENDATIONS

Overall performance of the IOP software is much improved over the design analyzed prior to the FSW PDR. The elapsed time for I/O requests has been greatly reduced, especially on the Flight Critical Busses. As a result, transport lag is no longer a problem. The variability in starting an I/O request is also much less; the interval between sampling the critical inputs on successive executions of the Fast Cycle Executive is well within requirements.

One system response requirement appears to be in some jeopardy. For certain inputs, the variation in sampling MDM's in a redundant request which are commanded by different computers must not exceed 300μsec. To meet this requirement, the jitter in starting a request should not exceed about 250μsec, which was true for all of the I/O requests modeled.

The theoretical maximum for this jitter, however, is the time interval between points where the IOP checks for new work to start; while more than 95% of these intervals were less than 200μsec, a few ranged up to 300μsec. Very detailed analysis would be required to determine whether these variations could occur in a different order in different IOP's; intuitively, the IOP's should embark on these long paths at about the same time, thereby staying within requirements.

METHOD

Three MSC routines perform the I/O functions: 1) FIOMPSDO executes when no I/O is outstanding. Its purpose is to monitor for new work to perform (as directed by the CPU), and to start the appropriate routine. 2) FIOMCNTL is executed to start the BCE programs for a new request submitted by the CPU. 3) FIOMNTR

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is executed to monitor for request completion and interrupt the CPU on a completed request.

These routines were modeled by simulating the MSC instructions required to perform the functions of each, together with a control structure to determine which logic paths were to be taken. Statistics were obtained on DMA activity and queueing, elapsed time for the routines (actually for segments of the MNTR routine), variability in starting a request, and intervals between checking for new work to start. Results given below are organized in this fashion.

FINDINGS

DMA Activity

There were about 49000 DMA requests per second in the modeled run - 29000/sec for the MSC and 20000/sec for the BCE's. This load requires 3.9% of all available memory cycles and causes an effective additional CPU utilization due to I/O interference of 2.8%. A threshhold of 8 pending DMA requests was used to cause the burst mode to be entered. The maximum number of outstanding requests observed in the model was 10, and only about .2% of requests were issued in the burst mode. Table 1 provides more detail on these results.

MSC Routines Elapsed Time

As stated previously, three MSC routines, FIOMPSDO, FIOMCNTL, and FIOMNTR, were modeled for this study. FIOMPSDO is active when no I/O is outstanding. It checks for new work every 120μsec, and branches to the appropriate routine as directed by the CPU. The MSC spends about 73% of its time in this routine.

FIOMCNTL is the routine used to start the BCE programs associated with an I/O request. Its average elapsed time is 172μsec, with a range of 150-220μsec. The MSC spends about 4% of its time here.

FIOMNTR is the routine that monitors for request completion and notifies the CPU when the request is complete. The routine consists of three segments: 1) the set-up time prior to issuance of the RAW instruction; 2) the RAW instruction itself, which actually recognizes the request completion; and 3) interrupting the CPU. The set-up portion of the routine requires an average of 78μsec, and ranges from 70 to 95μsec. The RAW instruction will wait for completion for up to 112μsec before timing out and eventually repeating itself; when it finds a completion, then, it takes an average of about 56μsec. The clean-up segment of the routine requires an average of 58μsec, and ranges from 50-65μsec. The Monitor routine is active about 23% of the time.

Table 1 - DMA Activity

	Requests/sec	Avg response (μsec) including queuing	Maximum response (μsec)	% Queued up	% of time Instruction was delayed
Total	48800	3.2μsec	19μsec	34%	-
MSC	29000	2.5μsec	18μsec	-	-
Read	28100	2.5μsec	18μsec	-	15%
Write	900	3.1μsec	16μsec	-	0%
BCE	19800	4.3μsec	19μsec	-	-
Read	17500	4.3μsec	19μsec	-	0.5%
Write	2300	4.4μsec	15μsec	-	0%

Table 2

Request Start Variability

Time (μsec)	% of samples in this range	Cumulative %
0-50	40%	40%
50-100	34	74
100-150	21	95
150-200	3	98
200-250	2	100

Table 3

Interval Between Checking for New Work

Time (μsec)	% of samples in this range	Cumulative %
100-120	78.7%	78.7%
120-140	1.0	79.7
140-160	0.1	79.8
160-180	1.0	80.8
180-200	14.1	94.9
200-220	2.9	97.8
220-240	0.2	98.0
240-260	0.2	98.2
260-280	1.1	99.3
280-300	0.7	100

Request Start Variability

The average time between the CPU requesting new work and the MSC starting on the work at FIOMCNTL is 73μsec. Table 2 gives a further breakdown of the distribution of this time. Assuming that IOP's could differ in starting a request by the maximum variability shown for a single IOP, this figure (250μsec) is the major impediment to meeting the 300μsec window for redundant sensor reads. If this requirement is firm, design changes may be required to reduce the start variability.

Intervals Between Checking for New Work

As stated earlier, this time is the limiting factor of request start jitter. The average time between checking for work is 135 sec. Table 3 gives a distribution of the times. The longest path without checking in the MSC routines is in FIOMNTR; it occurs when all BCE's for a request finish just before the MSC times out of the RAW instruction. This path can take up to 300μsec. It should be noted that other MSC routines are designed but were not modeled (Self-test, Compare word exchange). The execution time of these routines, if longer than 300μsec, can increase the maximum interval described here.

REFERENCE

IOP Software Analysis - Initial Report by R. W. Burns, Jr., 4/23/75.

UDF I/O LOADING STUDY

FINAL REPORT

8/1/75

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1.0 MANAGEMENT OVERVIEW

This report covers two major Utility/Data Flow areas: (1) Test Control Supervisor (TCS); (2) Frequency Response Tests (FRT). Analysis of the current UDF design shows these findings:

TCS

- 5 test sequences can do work simultaneously assuming no test sequence is CPU bound.
- all 5 test sequences will share the CPU equally if the test sequences contain I/O reads and testing with averaging.

FRT

- FRT I does not meet the requirement that all responses from avionics stimuli fall within 1 ms. The response variation was 7 ms.
- FRT II cannot complete its workload in the 10 ms allotted. The average elapsed time of the task was 12.7 ms. and the task missed 50.5% of its scheduled executions in a 2 second simulation

Based on the above findings, further analysis was done to address solutions for the FRT performance problems. This analysis produced the following recommendations that will permit FRT to meet response time requirements:

- Synchronize all cyclic process starts. (T_o)
- Skew the start of FRT I process 15 milliseconds from Downlist by scheduling FRT I 15 milliseconds prior to T_o.
- Make FRT the highest priority task in the system.
- Write a hard-coded BCE program which will write to the activators and read the sensors..
- The IOP Software design in FCOS 5.0 release is needed to meet FRT II requirements to cycle every 10 ms.

2.0 PURPOSE AND SCOPE

The purpose of this task was to evaluate the performance of the UDF software. This evaluation was done in two steps: (1) evaluate the efficiency of the Sequence Processor Module while running five test sequences simultaneously; and (2) evaluate the response time for Frequency Response Tests (FRT) Part I Write Commands to the Control Surfaces, and evaluate the I/O loading effects for FRT Part II.

3.0 OBJECTIVES

The objectives of this task were to help UDF software designers to:

(1) determine the most efficient method to run multiple test sequences simultaneously (5 maximum).

(2) determine a read/write method for FRT Part I to meet the requirement that elapsed times between the write command to the control surfaces reading the MDM and the response from the read command reaching the MDM will not vary more than 1 millisecond.

(3) determine if FRT Part II meets requirements to write to six Control Surfaces and read 28 Control Surface responses in 10 milliseconds.

These objectives were achieved in this task. Another objective, to show the impact of Housekeeping Data Acquisition processing, was not accomplished and is deferred for future UDF analysis tasks.

4.0 METHODS

To accomplish these objectives a model of UDF was developed. For step 1, the model includes:

(1) a functional Single Command Processor

(2) a functional Sequence Acquisition Processor

(3) a detailed Sequence Processor Module which sequences through any test sequence. CPU is charged by operator function so that it varies with each unique test sequence.

In addition to the modules above the model includes for steps 2 and 3:

(1) a functional FRT Part I Control Module.

(2) one functional Aerosurface Actuator (ASA) program.

(3) a functional Command module.

(4) a functional, Cyclic Waveform Generator module.

(5) a functional Control Surface Read module.

Both steps will run in an environment of:

(1) LDB polling at 25 Hz. with no data input.

(2) DEU polling at 5 Hz. with no data input.

(3) Downlist data at a rate of 3200 16-bit words/second.

See Figure 1 for the organization of the Flight Software model and its interactions with the UDF model.

Priorities to be used for this study are:

(UDF priorities are relative)

1.	Downlist	246
2.	DEU Polling	230
3.	LDB Polling	134
4.	Single Command Processor	129
5.	Sequence Acquisition Processor	110
6.	Sequence Processors	69-65
7.	Waveform Generator	60
8.	FRT Control	58
9.	FRT Control Surface Read	58
10.	ASA Program	56

11.	FRT Command	52
12.	Telemetry Format Load (TFL) Program	44
13.	Computer Status Lights Test	42

Figure 2 shows the assumptions made for the TCS study and Figure 3 lists the process times assigned to the TCS operators. Figure 5 shows the System Software environment used on the FRT study.

5.0 FINDINGS

5.1 TCS

TCS has no apparent problems with the current design. Five sequence processors can get work done simultaneously.

The test sequences used in this study were not typical, rather, an attempt was made to create a 'worst case' condition (See Figure 4). The highest priority Sequence Processor executed a test containing only repeated read with no averaging. This is a minimum of I/O activity by the highest priority task, yet, all four Sequence Processor, at a lower priority, were able to accomplish work (See Figures 8 and 9). Figure 10 shows the ratio of process time to time lost because the CPU was not available. (Task suppression time)

A more typical test sequence would have reads and tests with averaging and, possibly, some delays. These delay periods would allow all Sequence Processors to complete an equal amount of work.

If any Sequence Processor executes a test sequence without any I/O or delays, all Sequence Processors at a lower priority will be 'locked out' and unable to accomplish any work until the higher priority Processor completes.

5.2 FRT

The large variability of the current IOP design (FCOS 4.0) prevents FRT I and FRT II from meeting current response requirements.

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FRT I The two cases run for FRT I are summarized below (see Figure 6 for detailed case descriptions).

Case I - The current FRT I design and the current IOP design were used in this case.

Case II - The new IOP design (FCOS 5.0) was used in this case.

Case II indicates that the new IOP design will reduce the variability between the write request and the response data to 1 ms, which is the requirement (See Figure 11). Since the modeled response is bordered on exceeding the requirement, it is recommended that a BCE program be written which will issue both the write to the actuators and the read of the sensors.

This hard-coded BCE design modification could not be measured in the current IOP model, but, analysis of the FCOS capabilities indicates 67 microseconds is the maximum variability that will occur between a series of write-read requests.

FRT II The four cases run for FRT II are summarized below (see Figure 7 for detailed case descriptions):

Case I - The current FRT II design and the current IOP design were used in this case.

Case II - The use of the hard-coded BCE program was implemented in this case.

Case III- The new IOP design was used in this case.

Case IV - Both the new IOP design and the hard-coded BCE program were implemented in this case.

As the data in Figure 12 indicates, the hard-coded BCE program alone is not sufficient to meet FRT II requirements. The missed executions were reduced to 25.5% from 50.5% with the BCE program. Since the BCE program is required for FRT I and it does help FRT II response it should be used for both. A savings of 5% FCOS CPU utilization is also realized by using the BCE program. The new IOP design is needed to meet FRT II requirements as Cases III and IV indicate.

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6.0 RECOMMENDATIONS

Recommendations 1-3 are to make the FRT system more efficient. Recommendations 4-5 are needed to meet FRT requirements. There are no recommendations at this time for TCS.

1. Synchronize all cyclic process starts (T_o). This allows control of the system workload and helps predict variations in that workload.

2. Skew the start of FRT I process 15 ms from Downlist by scheduling FRT I 15 ms prior to T_o.

3. Make FRT the highest priority tasks in the system. FRT II has the fastest cyclic rate in the system and should have priority to get its work done. When using the FCOS 5.0 IOP design, FRT uses flight critical busses which will have the 2nd highest I/O priority next to ICC traffic.

4. Write a hard-coded BCE program which will write to the actuators and read the sensors. This ensures a minimum variation in the elapsed time between write and read commands for FRT I.

5. The FCOS 5.0 IOP design must be available to UDF for FRT II to meet requirements.

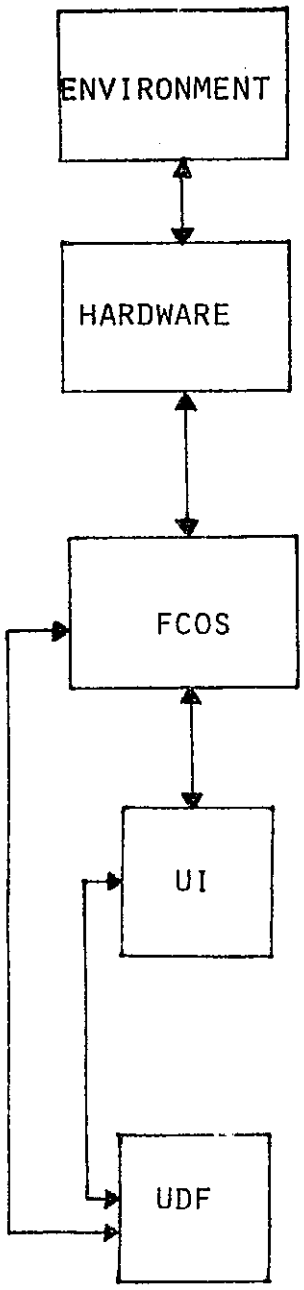
7.0 REFERENCES

1. "UDF I/O Loading Study - Initial Report" by R. L. Singhaus, 5/2/75.

APPENDIX A

FSW PERFORMANCE MODEL ORGANIZATION

FOR UDF STUDY



ROUTINES TO SIMULATE EXTERNAL DPS INTERFACES INCLUDING:

- ROUTINES TO TABULATE STATISTICS ON DEVICES TIED TO MDM'S AND DBIU

- FLIGHT COMPUTER
- IOP
- ALL DEVICES THAT INTERFACE WITH IOP

- PROCESS MGT.
- I/O MGT.
- CONFIGURATION MGT.
- INTERFACES TO OTHER FUNCTIONS

- DISPLAY SUPPORT
- DISPLAY FORMATTING
- LDB POLLING
- DISPLAY UPDATING
- DEU STATUS MAINTENANCE

- TEST CONTROL SUPERVISOR
- GENERAL TEST SUPPORT
- FREQUENCY RESPONSE TESTS
- TELEMETRY FORMAT LOAD

FIGURE 1

APPENDIX B

TCS ASSUMPTIONS

- ENVIRONMENT
  - ALL OPERATOR INPUTS PREVIOUSLY RECEIVED
  - MCDS POLLING WITH NO INPUTS
  - DISPLAY UPDATE WITH NO DISPLAYS
  - DOWNLIST 3200 16-BIT WORDS/SECOND
- NO I/O ERRORS
- TEST SEQUENCES ON MASS MEMORY
- 5 TEST SEQUENCES RUN CONTINUOUSLY
- FORCED HEAVY WORKLOAD ON HIGHEST PRIORITY PROCESSOR IN ORDER TO ASSESS IMPACT ON LOWER PRIORITY PROCESSORS

FIGURE 2

TCS PROCESS TIMES

OPERATOR	PROCESS TIMES IN μs
BEGIN	110
ISSUE	1400
READ (no averaging or 1st read)	1840
READ (averaging-each subsequent read)	600
TEST (no averaging or 1st read/test)	2920
TEST (averaging-each subsequent read/test)	1680
DELAY	300
BRANCH	1100
CALL	890
TEXT	620
STOP	1000
END (main sequence)	1150
END (subsequence)	830
TASK/EXECUTION	
Sequence Acquisition Processor	2130
Sequence Processor (plus Operator Charges)	900

Figure 3

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TCS TEST SEQUENCES

- Sequence Processor 1

Operators	Processing Time
1. Begin	1100μs
2. Read 1 word - FF3	1800μs
3. Repeat steps 1 and 2	1100μs

- Sequence Processors 2-5

Operators	Processing Time
1. Begin	1100μs
2. Text	620μs
3. Issue 1 word - FF1	1400μs
4. Read 1 word - FF1	1840μs
5. Test 1 word - PCMMU	2920μs
6. Issue 1 word - FF2	1400μs
7. Read 1 word - FF2	1840μs
Read 100 samples - wait 50 ms between samples	59400μs
8. Read/Test 1 word - PCMMU	2920μs
Test 50 samples - wait 100 ms between samples	82320μs
9. Delay 100 ms.	300μs
10. Repeat steps 1 through 9	1100μs

Figure 4

FRT SYSTEMS SOFTWARE ENVIRONMENT

- DOWNLIST
  - NEW ALT DESIGN
  - EXECUTE AT 25 HZ RATE
  - OUTPUT 3200 16-BIT WORDS/SECOND
  - PRIORITY = 246

- DISPLAY UPDATE
  - NEW ALT LOADING ESTIMATES
  - EXECUTE AT 10 HZ RATE
  - UPDATE 3 DISPLAYS
  - OUTPUT 32 16-BIT WORDS/SECOND FOR 3 DEU'S
  - PRIORITY = 142

- MCDS POLLING
  - EXECUTE AT 5 HZ RATE
  - POLL 3 DEU'S
  - NO KEYBOARD INPUTS
  - PRIORITY = 230

- LDB POLLING
  - EXECUTE AT APPROXIMATELY 25 HZ RATE. EXECUTION VARIES WITH SYSTEM LOADING.
  - NO LDB INPUTS
  - NO LDB OUTPUTS
  - PRIORITY = 134

FIGURE 5

FRT I ENVIRONMENT

- EXECUTE AT 25 HZ RATE
- 2860μSECONDS PROCESSING EVERY 40 MILLISECONDS
- 3520μSECONDS PROCESSING EVERY 80 MILLISECONDS
- WRITE 16 WORDS TO FLIGHT AFT MDM 1 USING A BCE CHAIN OF 5 ELEMENTS. THIS IS THE HARD-CODED BCE PROGRAM WRITTEN FOR GN&C.
- READ 56 WORDS FROM FLIGHT AFT MDM 1 USING GN&C PROM
- WAIT FOR I/O COMPLETE FOR BOTH THE WRITE AND READ REQUESTS
- RESPONSE TIMES MEASURED FROM THE WRITE COMMAND AT THE MDM TO THE READ COMMAND AT THE MDM.
- PRIORITY = 58
- WAVEFORM GENERATOR, PRIORITY = 60

- CASES
  - CASE I
    - WAIT FOR I/O COMPLETE ON READ AND WRITE REQUESTS
    - NO SKEW IN SCHEDULING FRT I
    - PRIORITY = 58
  - CASE II
    - CURRENT FRT I DESIGN
    - NEW IOP DESIGN
    - PRIORITY = 249
    - SKEW FRT I SCHEDULE 15 MS FROM DOWNLIST

FIGURE 6

FRT II ENVIRONMENT

- EXECUTE AT 100 HZ RATE
- 440μSECONDS PROCESSING EVERY 10 MILLISECONDS
- 590μSECONDS PROCESSING EVERY 40 MILLISECONDS
- 880μSECONDS PROCESSING EVERY SECOND
- WRITE AND READ DEFINITIONS ARE THE SAME AS FRT I
- PRIORITY = 57
- WAVEFORM GENERATOR, PRIORITY = 60
- CASES
  - CASE 1
    - WAIT FOR I/O COMPLETE ON READ AND WRITE REQUESTS.
    - NO SKEW IN SCHEDULING FRT II
    - PRIORITY = 57
  - CASE II
    - SKEW FRT II SCHEDULE 15 MS FROM DOWNLIST
    - PRIORITY = 248
    - HARD-CODED BCE PROGRAM
    - CURRENT IOP DESIGN
  - CASE III
    - SKEW FRT II SCHEDULE 15 MS FROM DOWNLIST
    - PRIORITY = 248
    - CURRENT FRT II DESIGN
    - NEW IOP DESIGN
  - CASE IV
    - SKEW FRT II SCHEDULE 15 MS FROM DOWNLIST
    - PRIORITY = 248
    - HARD-CODED BCE PROGRAM
    - NEW IOP DESIGN

FIGURE 7

APPENDIX C

TCS CPU UTILIZATION (%)

DOWNLIST	12.87
MCDS POLLING	1.04
LDB POLLING	.36
DISPLAY UPDATE	.06
SEQUENCE ACQUISITION	.03
SEQUENCE PROCESSORS	
TASK #1	32.5
TASK #2	1.3
TASK #3	1.3
TASK #4	1.2
TASK #5	1.1
FCOS	24.3
TOTAL	76.1

FIGURE 8

FLIGHT COMPUTER TASK SUMMARY FOR TCS STUDY

PROCESS	SUB SYSTEM	RATE	PRIORITY	CPU MSEC/SEC	IO REQ PER SEC
DOWNLIST	UI	25 hz	246	128.7	25
MCDS POLLING	UI	5 hz	230	10.4	15
DISPLAY UPDATE	UI	10 hz	142	.06	12
LDB POLLING	UI	28.5 hz	134	3.6	28.5
SEQUENCE PROCESSORS					
TASK #1	UDF		69	325	106.8
TASK #2	UDF		68	13	13.5
TASK #3	UDF		67	13	13.7
TASK #4	UDF		66	12	13.4
TASK #5	UDF		65	11	13.4

FIGURE 9

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TCS TASK PROCESSING AND WAIT TIME

	WAIT FOR CPU	USING CPU
TASK #1	19.5%	32.5%
TASK #2	9.5%	1.3%
TASK #3	10.7%	1.3%
TASK #4	11.6%	1.2%
TASK #5	16.4%	1.1%

TCS I/O RESPONSE TIME

DEVICE	# REQUESTS (20 SEC RUN)	AVERAGE I/O RESPONSE	RANGE
PCMMU1	616	8.76MS	3MS-13MS
MDMFF1	10	4.66MS	3MS-7MS
MDMFF2	418	4.61MS	2MS-10MS
MDMFF3	2010	4.29MS	2MS-8MS

FIGURE 10

FRT I RESULTS

CPU SUMMARY

TASK	CPU%
DOWNLIST	2.83
MCDS POLLING	1.04
DISPLAY UPDATE	1.52
LDB POLLING	.36
FRT I	7.97
APPLICATION TOTAL	13.72

CASE	I	II
APPLICATION TOTAL %	13.72	13.72
FCOS %	20.29	17.29
FRT TOTAL %	34.01	31.01
RESPONSE VARIATION	7 MS	1 MS

FIGURE 11

FRT II RESULTS

CPU SUMMARY

TASK	CPU%
DOWNLIST	2.83
MCDS POLLING	1.04
DISPLAY UPDATE	1.52
LDB POLLING	.36
SYSTEM SOFTWARE TOTAL	5.75

CASE	I	II	III	IV
SYSTEM SOFTWARE TOTAL %	5.75	5.75	5.75	5.75
FRT II %	2.48	3.59	4.81	4.81
FCOS %	29.10	29.82	38.20	33.05
FRT TOTAL %	37.33	39.16	48.76	43.61
MISSED EXECUTIONS %	50.5	25.5%	0	0
WRITE-READ I/O AVERAGE ELAPSED TIME	12.7 MS.	9.54 MS.	6.07 MS.	5.44 MS.

FIGURE 12

MULTI-FLIGHT COMPUTER MODELING ANALYSIS

FINAL REPORT

9/12/75

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MANAGEMENT OVERVIEW

In order to evaluate the MFC software design, modeling analysis was performed. The FSW ALT Approach and Landing (A/L) Baseline case, as defined in the methods section of this report, showed the following:

- Total CPU utilization was 114.9%
- FCOS utilization was 30.2%
- The number of sync points was 638.5/sec
- The IOP software design changes resulted in reduced I/O response time and a decrease in the variability of IOP starting work on requests.
- Transport lag averaged 11 ms and ranged between 10.8-11.8 ms.
- Flight critical input sampling jitter requirements were met.
- The 300μ maximum input skew requirement may not be met.
- Bus contention problems did occur but should be solvable by optimizing skew of process starts and by balancing the I/O load.

This report presents MFC Software performance results. Since alternate designs were not evaluated, no specific recommendations resulted from the analysis task.

PURPOSE AND SCOPE

The purpose of this analysis task was to predict the performance of the Flight Software ALT Multi-Flight Computer Software functional design as defined in the Space Shuttle Orbiter Avionics Software ALT Functional Design Specification (FDS) of 7/25/75. Performance results, based on model simulations, were presented at the Flight Software ALT Delta Preliminary Design Review. The scope of the task was limited to ALT Approach and Landing (A/L) mode with emphasis on the MFC software in a steady state, error free environment.

OBJECTIVES

The overall objective was to evaluate the effects of the MFC functions on system performance. Specific objectives accomplished were:

1) To predict CPU utilization for each of these functions.

2) Predict the number of sync points utilized in the current FSW design.

3) To determine if the skew between the process starts of SIP and Fast Cycle Executive enables each of them to complete successfully without interference from the other.

4) To predict the sampling jitter for the MTU

5) To predict I/O response times

6) To predict the occurrence of missed process executions

7) To determine the effects of increased ICC traffic on the successful execution of SIP

8) To determine the effect of the new IOP software design and of the MFC functions on the sampling jitter of critical GN&C inputs and on the GN&C transport lag.

9) To determine if maximum input skew requirements are met.

METHOD

To determine the effects of the MFC software, three redundant computers were simulated. No drift between the computers' GPC clocks was represented. Any drift between the computers due to their clock differences must be factored into the cost of synchronization.

The model used for this analysis task reflects the rates and execution times resulting from the May Scrub and the FSSR rewrite for UI, SM and GN&C. This set of rates and execution times is referred to as the 'Tornado Baseline'. While the 'Tornado Baseline' does not include all the latest scrub items, it was determined to be a good reference point for evaluation of the MFC software. Therefore, emphasis is placed on the additional CPU loading resulting from the MFC software rather than total system CPU utilization. Refer to Appendix A for a list of scrub items not included.

The FSW model was updated to reflect the system software design as defined in the FDS of July 25, 1975. To be specific, updates for the synchronization routines, sync points in FCOS routines, IOP software, Time Management routines, System Interface Processor (SIP), usage of Update Blocks/Exclusive Procedures, and ICC interface were added to the FSW model. However, the Downlist function does not reflect the FDS design. It is modeled to represent the Downlist design in the 'Tornado Baseline' which will be implemented for ALT.

Appendix B contains a summary of the rates and usage of FCOS services for the processes modeled. It also shows a timeline of the process starts. All processes except the Fast Cycle Executive (F/C Exec.) were scheduled to start at the same time as SIP. Thus, multiple processes were started by one timer interrupt resulting in a CPU savings of interrupt handling overhead. The start of F/C Exec was skewed from the start of SIP by 20 ms in order to minimize CPU and I/O contention between the two high priority processes. Assumptions for modeling the SIP process are also documented in Appendix B.

The operation of the IOP is represented as a series of delays in the model. The delay times were derived from the detailed IOP modeling study (reference 2) performed on the IOP software defined in the FDS of 7/25/75. Appendix C contains a breakdown of the IOP delays used for this study.

Performance results for the Baseline represent nominal conditions for only cyclic functions in an error-free environment. Non-cyclic functions such as specialist functions, crew inputs or requests for display changes, and error conditions are not included. However, a preliminary evaluation of the effects of transferring a full Inter-computer channel (ICC) buffer due to error conditions was made.

FINDINGS

CPU Utilization

The total CPU utilization for the A/L Baseline case was 114.9%. FCOS utilization was 30.2%. Table 1 compares the Delta PDR baseline CPU utilization with the CPU utilization for the 'Tornado Baseline' (104.1%). The CPU for applications increased 1.3% due to SIP processing. FCOS CPU increased due to the following:

- Additional FCOS required for SIP functions (4.5%)

- Baseline model results for the cost of MFC software (9.6%) replaced preliminary estimates of MFC functions in the 'Tornado Baseline'.

As a result of the detailed IOP analysis, references 2, the DMA utilization was shown to be 2.8%.

Table 2 shows a breakdown by process of application and FCOS CPU utilization for the baseline case. The cost of Downlist which is called by the SIP process is broken out separately. Table 3 shows a further breakdown of FCOS utilization.

Computer Synchronization

GPC synchronization is designed to keep GPC's together with respect to time, data gathering, and internal queue manipulation. Based on usage of FCOS services in the Baseline case, 638.5 synchronization points occurred each second. Table 4 shows a detailed breakdown of usage of synchronization routines. It also compares the 638.5 sync points per second to the 390.5 sync points per second estimated at PDR in March, 1975. The most significant difference is that sync was not performed at I/O initiation in the preliminary analysis for PDR.

In order to minimize the number of sync points, the following design features were included in the Baseline:

- No SVC synchronization was performed on change of I/O completion event states. Sync was accomplished by the I/O completion sync routine.
- No SVC synchronization was performed on initiation of the MTU request which was issued by the SIP synchronization routine.
- Only one sync was required to activate multiple processes which shared one timer expiration.

The cost of sync for the baseline case was 7.6%. This cost depends not only on the number of sync points but on the skew between computers arriving at the sync points. Each computer must execute a non-agree loop until all redundant computers agree with its sync code. Each time thru the no-agree loop extends the cost of sync by 40μs. Table 5 shows the modeled usage of the no-agree loop. Any additional skew between the computers such as GPC clock drift or variability in redundant IOPs must be factored in.

Contention Between F/C Exec and SIP

As a result of the 20 ms. skew between the process starts of F/C Exec and SIP, (See Appendix B) contention for the CPU between these two high priority processes was minimal. SIP's average elapsed time was 5.3 ms. Thus, it is completed 15 ms before the start of F/C Exec, whose average elapsed time was 20.3 ms. A 20 ms skew of the process starts may not be optimum for load balancing. Further analysis must be made to determine the skew that has the best effect on total system performance.

Contention for the FF buses between SIP and F/C Exec occurs when the MTU is read by SIP on the same cycle F/C Exec issues its 12.5 hz I/O requests. Figure 1, which contains a sample timeline of the I/O elapsed times, illustrates that the elapsed time for I/O requests for the FF buses extended past the start of SIP, where the MTU read is issued. Since F/C Exec I/O extends into the start of SIP on alternate F/C Exec cycles, bus contention can be avoided if the MTU is always read on the cycle that doesn't issue the F/C Exec 12.5 hz I/O requests.

MTU Sampling Jitter

MTU sampling jitter is the variation in the time measured from time tagging the MTU request by FCOS until the MTU data is read from the MDM. Due to the impact of bus contention on MTU sampling jitter, two cases were modeled. In the case where bus contention between F/C Exec was eliminated so that the FF bus was always free, the maximum variation to occur was 320μs. In the case where contention was not avoided, the variability ranged as high as 4.6 ms. These sampling jitter results were provided as inputs to an indepth analysis on timekeeping by the Mission Studies and Analysis Department. Reference 3 discusses the results from this analysis.

I/O Response Times

Figure 1 contains a sample timeline of I/O elapsed times, illustrating the I/O activity for a particular 80 ms period for the model simulation. It shows when each request was issued and the elapsed time for each request, which includes FCOS, IOP processing and data transfer time.

Missed Process Executions

Due to overloaded CPU utilization, (114.9%) lower priority processes were not always able to complete within their allotted time. Missed process executions occur when an interval timer interrupt occurs to start the next process' execution and the process is still working on the previous cycle execution. In a two-second model simulation the following process executions were missed:

1 of 4 Display Update Executions
11 of 25 Mated/Drop Executive Executions
1 of 2 PM Control Executions

If processes continue to miss executions after the CPU utilization is within requirements, better balancing of the CPU load must be obtained.

Increased ICC Traffic

The following two cases were run to determine the effects on SIP of increased ICC traffic:

1) The baseline case with an I/O error requiring Input Problem Reporting (IPR) via ICC.

2) The baseline case with an annunciation requiring transmission of a full ICC buffer.

In case 1, IPR for an I/O error on GN&C's critical read of the FA MDM tied up the ICC buses 2.5 ms. Since execution of SIP is offset from F/C Exec's input request, this IPR did not contend with SIP's cyclic request for the ICC buses. In case 2, transmission of a full ICC buffer (128 16-bit words) by SIP extended the average elapsed time for the ICC exchange from 2.5 ms to 6.6 ms. In turn, the average elapsed time of the SIP process increased from 5.3 ms to 9.4 ms. However, the increase in the ICC data transfer had no ill effects on system performance.

While no ICC contention problems existed in these two cases, possible contention problems could occur. The use of the ICC must continue to be monitored.

GN&C Input Sampling Jitter

Sample variations are defined as the variation from 40 ms of the differences in the times between succeeding samples of the time critical inputs 1 and 2 of the F/C Exec. The requirement is that the variation cannot exceed 2% of the iteration rate of 40 ms, i.e., .8 ms, for more than 4% of the variations and that the variation must never exceed 4 ms. Table 6 shows that input sampling jitter for the baseline case meets requirements. The maximum sample variation was 1 ms and 2% of the cases for input 1 exceeded .8 ms.

The new IOP software design reduced the variability in the IOP in starting work on a request (reference 2). Table 7 [illegible] input sampling variation due to the IOP is between 0-250μs. Other contributors to sample variation are:

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- Suppression of the start of the F/C Exec due to disabled FCOS processing for lower priority processes.

- I/O interrupts occurring at the start of the Fast Cycle Executive which delay the initiation of the critical input requests.

Transport Lag

The GN&C transport lag in this study is defined as the elapsed time from activation of the FF MDM to read the Accelerometer Assembly (AA) to activation of the FA MDM for the critical output to the Aerosurface Amplifier (ASA). The current requirement is that the transport lag must not exceed 15 ms.

In the Baseline case, transport lag requirements were met. Transport lag averaged 11 ms and ranged from 10.8 to 11.8 ms. Figure 2 illustrates a timeline for an average transport lag. The new IOP software design reduced the IOP response time for fight critical buses enabling transport lag requirements to be met.

Maximum Input Skew

The variation in sampling MDM's commanded by different computers in a redundant request must not exceed 300μs. Two contributors to this input skew are:

- The skew between computers in notifying the IOP of a new request. This is equal to the skew between computers in exiting the sync routine, or about 50μs.

- The interval between points where the IOP checks from new work, which is defined in Table 8. The maximum interval is 300μs.

While the 300μs input skew requirement will be met in the majority of cases, the jitter between IOPs starting a request could be as high as 350μs (reference 2).

FUTURE CONSIDERATIONS

Systems Analysis will continue to upgrade the FSW model in preparation for the FSW CDR. Model changes anticipated include:

- Recalibration of CPU sizing data for GN&C, SM, and Systems Services.

- Changes to FCOS as a result of the FCOS Audit.

- The GN&C redesign.

- Usage of the Hybrid Dispatcher

- Usage of the % SVC macro to replace most of GN&C's Update/ Blocks.
- A new consolidated GN&C I/O Profile.

REFERENCES

1. Multi-Flight Computer Analysis Task - Initial Report by K. L. Williams.
2. IOP Software Analysis - Final Report by B. Burns, Aug. 4, 1975.
3. Timekeeping Algorithm by Ira Saxe, Aug. 19, 1975.

TABLE 1

COMPARISON OF CPU (%) FOR

TORNADO BASELINE AND DELTA PDR BASELINE

	TORNADO BASELINE		Δ PDR BASELINE	
APPLICATION				
GN&C	52.9		52.9	
GN&C-MOVEMENT OF DATA IN UPDATE BLOCKS	7.5		7.4	
SM	6.2		6.2	
UI (POLLING, DOWNLIST, DISPLAY UPDATE)	14.2		14.1	
UI-SSIP	-		1.3	
TOTAL APPL		80.8		81.9
FCOS				
SINGLE STRING	17.8		16.1	
SSIP (MINUS CYCLING AND DOWNLIST WRITES)	-		4.5	
		17.8		20.6
MFC				
UPDATE BLOCKS	2.5		1.1	
SSIP-UPDATE BLOCKS	-		.3	
	2.5		1.4	
MTU RM	.5		.3	
SSIP-MTU RM	-		.1	
	.5		.4	
SYNC	2.5		6.3	
SSIP-SYNC	-		1.3	
	2.5		7.6	
FDI	-		-	
SSIP-FDI	-		.2	
	-		.2	
TOTAL FCOS-MFC		5.5		9.6
TOTAL FCOS		23.3		30.2
DMA		-		2.8
TOTAL SYSTEM		104.1		114.9

TABLE 2

CPU UTILIZATION FOR ALT A/L

	APPL	FCOS	TOTAL
UI			
DISPLAY UPDATE	10.6	.6	11.2
MCDS INPUT	.9	2.2	3.1
SSIP	1.3	8.3	9.6
• DOWNLIST	2.6	1.5	4.1
GPC SWITCH MONITOR	-	.1	.1
UI TOTAL	15.4	12.7	28.1
SM			
DATA ACQUISITION	1.9	.9	2.8
PM CONTROL	4.3	.2	4.5
SM TOTAL	6.2	1.1	7.3
GN&C			
FAST CYCLE EXEC	25.3	13.2	38.5
MATED/DROP EXEC	35.0	3.2	38.2
GN&C TOTAL	60.3	16.4	76.7
DMA INTERFERENCE			2.8
TOTAL SYSTEM	81.9	30.2	114.9

TABLE 3

FCOS CPU UTILIZATION (%)

FOR ALT A/L MODE

PROCESS CONTROL		
DISPATCHER	4.2	
SWITCH	.4	
SVC	2.4	
CLOSE	.4	
UPDATE BLOCK/EXCLUSIVE PROCEDURE	1.4	
	8.8	
TIME MANAGEMENT		
TIMER QUEUE/DEQUEUE	1.7	
TIMER QUEUE ELEMENT EXPIRATION	2.3	
MTU REDUNDANCY MANAGEMENT	.4	
	4.4	
EVENT MANAGEMENT		
EVENT STATES CHANGE	.8	
EVENT QUEUE/DEQUEUE	.6	
EVENT EVALUATOR	.6	
	2.0	
I/O MANAGEMENT	7.2	
GPC REDUNDANCY MANAGEMENT		
SYNCHRONIZATION	7.6	
FAULT DETECTION ISOLATION	.2	
	7.8	
TOTAL		30.2

BREAKDOWN OF UTILIZATION OF SYNCHRONIZATION ROUTINES
FOR ALT A/L MODE

PROCESS	# OF TIMER SYNC/ SEC	# OF SSIP SYNC/ SEC	# I/O COMPLETION SYNC/SEC	# SVC SYNC/SEC			
				I/O INIT	SET/RESET	WAIT	UPDATE BLOCK/ EXCLUSIVE PROC
SSIP (Downlist)	(25)	25 (0)	55 (0)	50 (0)		30 (0)	25 (0)
Fast Cycle Exec.	25 (25)		112.5 (112.5)	112.5 (0)	(14)	25 (25)	50 (50)
Data Acquisition	(10)		5 (0)	5 (0)	1 (2)	-	
MCDS Input (Polling)	(5)		15 (15)	15 (0)		-	15 (0)
Mated/Drop Exec	(12.5)					12.5 (12.5)	50 (50)
Display Update	(10)		4 (12)	4 (0)			
GPC Switch Mon.	-		-				
PM Control	(2)		(6)		1 (0)	1 (2)	
Total	25 (89.5)	25 (0)	191.5 (145.5)	186.5 (0)	2 (16)	68.5 (39.5)	140 (100)

TABLE 4

() Numbers enclosed in parenthesis represent number of syncs represented in preliminary analysis at PDR.

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TABLE 5

MODELED USAGE OF SYNC ROUTINES

NUMBER OF TIMER SYNC POINTS	25/SEC
NUMBER OF TIMES THRU NO-AGREE LOOP	0
NUMBER OF SSIP SYNC POINTS	25/SEC
NUMBER OF TIMES THRU NO-AGREE LOOP	0
NUMBER OF I/O INTERRUPT SYNC POINTS	191/SEC
NUMBER OF TIMES THRU NO-AGREE LOOP	141/SEC
NUMBER OF TIMES INTERRUPTED BY TIMER INTERRUPT	0
NUMBER OF SVC INTERRUPT SYNC POINTS	397/SEC
NUMBER OF TIMES THRU NO-AGREE LOOP	85/SEC
NUMBER OF TIMES INTERRUPTED BY I/O INTERRUPT	3/SEC
NUMBER OF TIMES INTERRUPTED BY TIMER INTERRUPT	0

TABLE 6

Flight Critical Input Sample Variation for ALT A/L

•20 ms Skew between SSIP and Fast Cycle Exec

Time (sec)	% of samples in this range		Cumulative %	
	Input 1-FF	Input 2-FA	Input 1-FF	Input 2-FA
0-200	78	84	78	84
200-400	16	10	94	94
400-600	2	2	96	96
600-800	4	2	100	98
800-1000		2		100

TABLE 7

I/O Request IOP Start Variability*

Time (μsec)	% of samples in this range	Cumulative %
0-50	40%	40%
50-100	34	74
100-150	21	95
150-200	3	98
200-250	3	100

*The variability in the elapsed time between the CPU requesting new work and the MSC starting work on the request is represented. Distribution resulted from FSW model simulations.

TABLE 8

MSC Interval Between Checking for New Work*

Time (μsec)	% of samples in this range	Cumulative %
100-120	78.7%	78.7%
120-140	1.0	79.7
140-160	0.1	79.8
160-180	1.0	80.8
180-200	14.1	94.9
200-220	2.9	97.8
220-240	0.2	98.0
240-260	0.2	98.2
260-280	1.1	99.3
280-300	0.7	100

*Elapsed time in MSC software between issuing SEC instructions, which causes MSC to look for a new request.

(20ms Skew Between Fast Cycle Exec and SSIP)

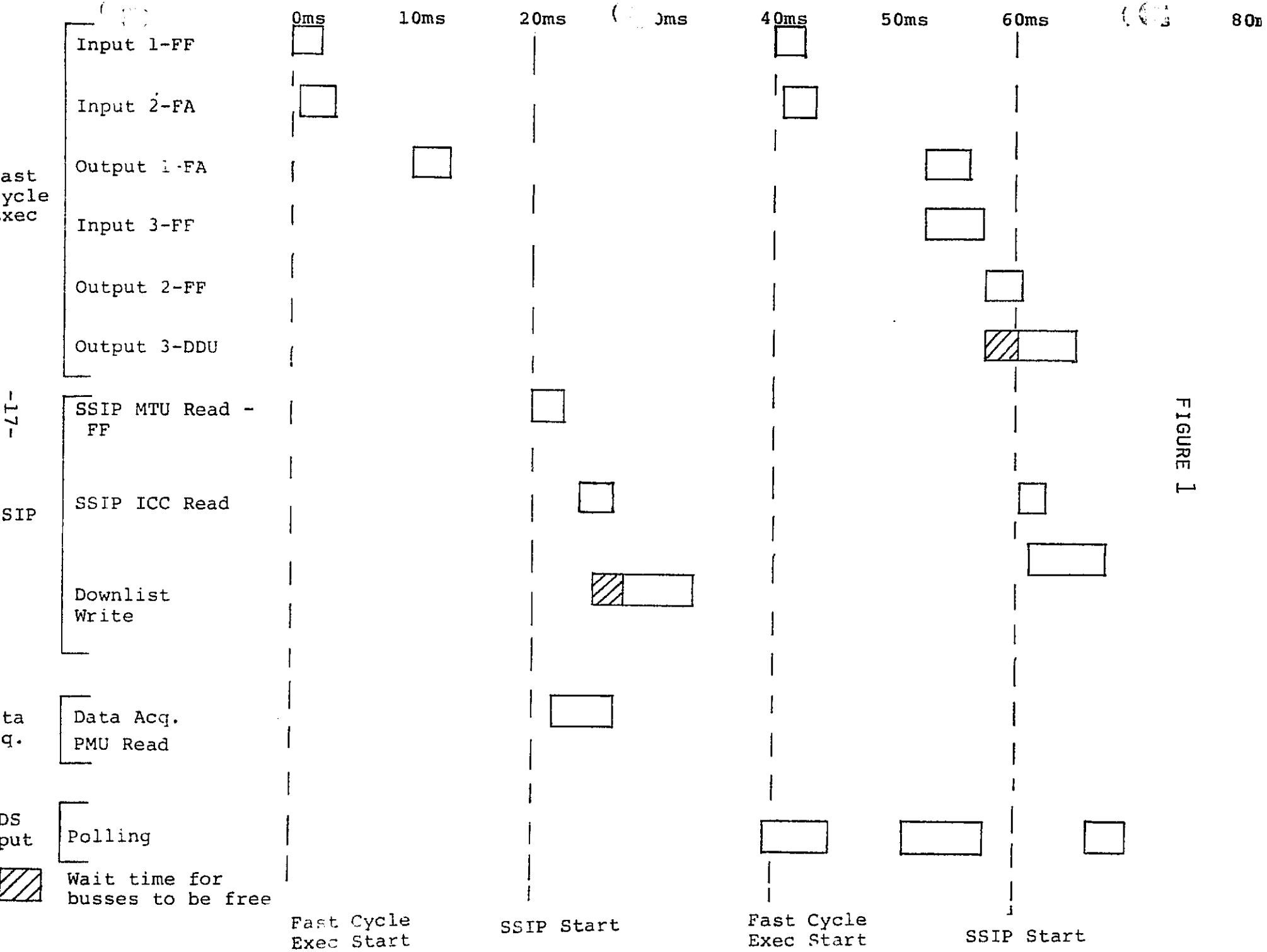
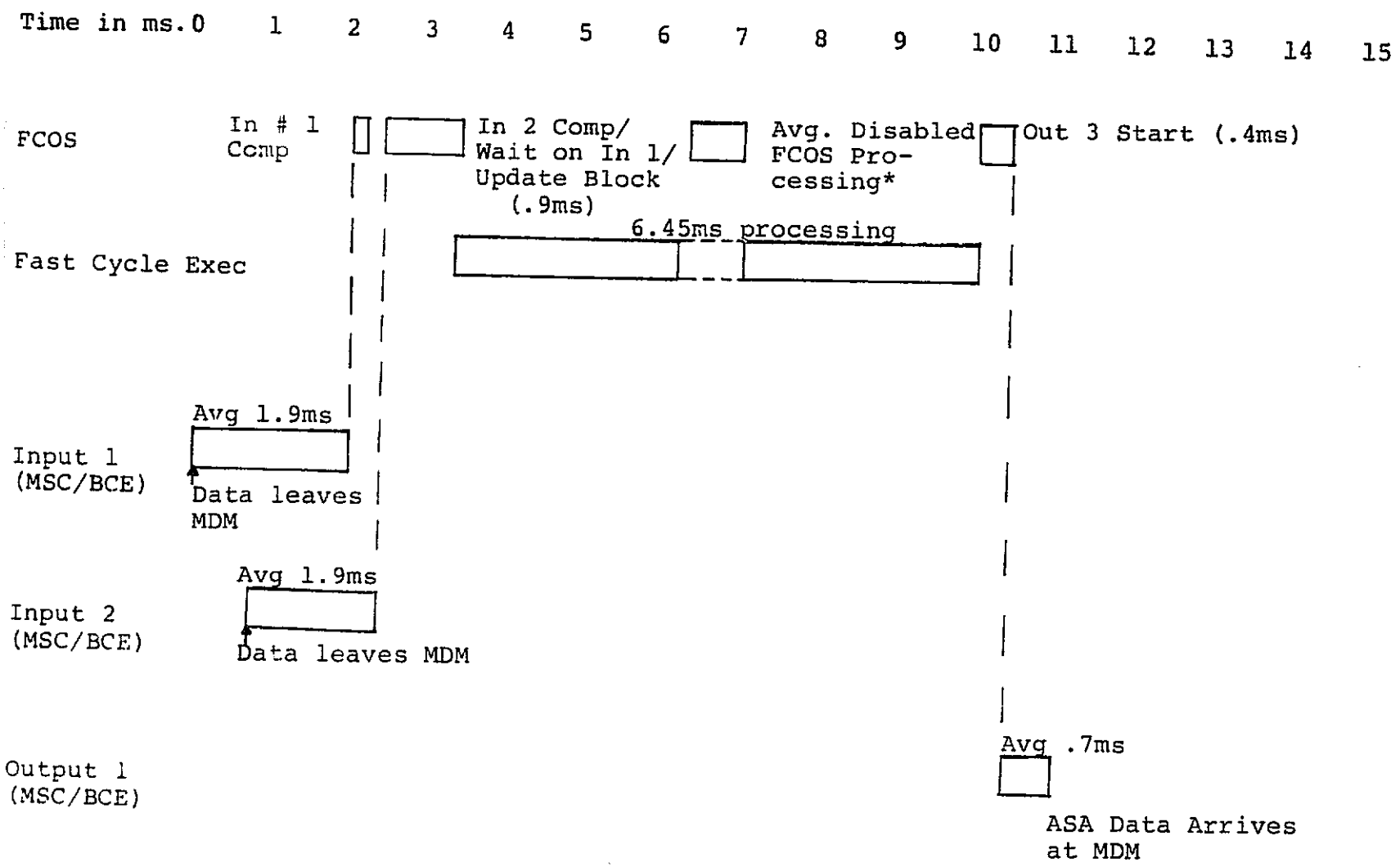


FIGURE 1

FACTORS CONTRIBUTING TO TRANSPORT LAG

Average Transport Lag of 11 ms (Range 10.8-11.8 ms)



*Disabled FCOS processing extending Transport lag includes

- Interval Timer interrupts to start lower priority processes
- I/O completion Interrupts for lower priority processes
- Suppression of Critical I/O Interrupts due to servicing lower priority processes.

FIGURE 2

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APPENDIX A

APPROVED SCRUB ITEMS NOT INCLUDED IN BASELINE

- NZ GUIDANCE
- ELIM. OF FADERS
- COMFAULT PROC
- RAW DATA SELECT
- F.O.H. FOR DD REDUCED
- EVENT LIGHT PROC.
- ADI ERROR NEEDLE PROC.
- CRT DIGITAL DATA @ VARIABLE RATE (APPLICATIONS)
- MICROCODE
- HAL OPTIMIZATION
- LIBRARY OPTIMIZATION
- HYBRID DISPATCHER
- DDU LOADSHARE

FLIGHT COMPUTER TASK SUMMARY
FOR ALT APPROACH AND LANDING MODE

PROCESS	SUBSYSTEM	RATE	PRIORITY	UPDATE BLOCKS/ EXCLUSIVE PROCEDURE	I/O REQ PER SEC	# WAITS/ SEC	# IMPLIED WAITS/SEC	# SET, RESET/SEC	MTU RM/SEC
SSIP	UI	25hz	251	25	55	30		30	5
Fast Cycle Exec.	GN&C	25hz	250	50	112.5	25	37.5	37.5	12.5
Data Acquisition	SM	5hz	234		5		5	1	
MCDS Input Polling	UI	5hz	230	15	15		15		
Mated/Drop Exec.	GN&C	12.5hz	150	50		12.5			
Display Update	UI	2hz	142		4				
GPC Switch Mon.	UI	1hz	134						
PM Control	SM	1hz	122			1		1	
Total				140	191.5	68.5	61.5	69.5	17.5

ALT DISPLAY SUMMARY FOR APPROACH/LANDING

- RM SENSORS

  UPDATE 1/SEC

- SYSTEM SUMMARY

  UPDATE 1/SEC

- FINAL APPROACH

  UPDATE 2/SEC

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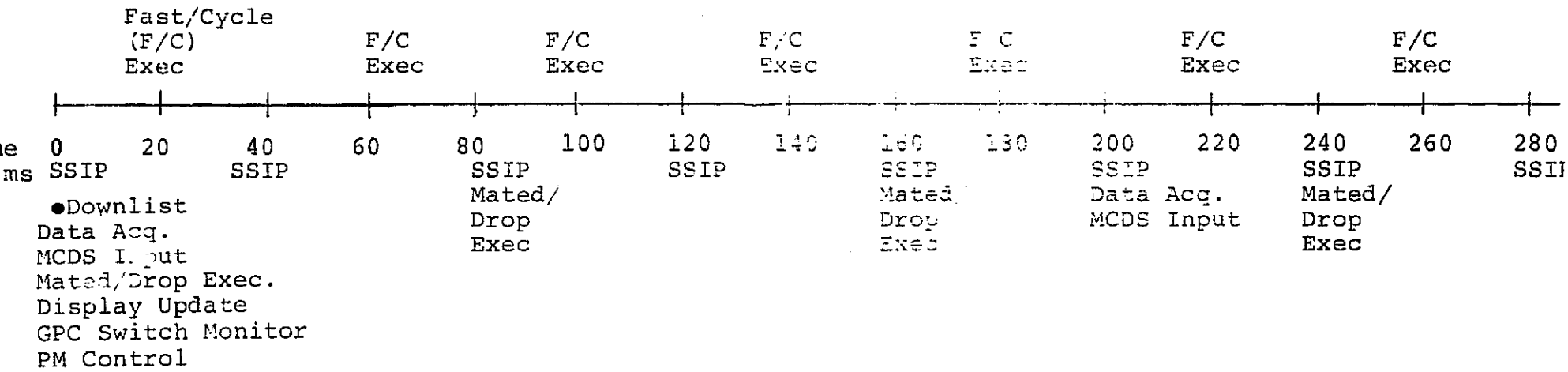
TIMELINE OF PROCESS STARTS FOR ALT A/I BASELINE



SIP PROCESS PROFILE* FOR CYCLIC FUNCTIONS

1) SSIP SYNCHRONIZATION IS INVOKED AT TIMER EXPIRATION.
MTU READ ISSUED 5/SEC BY SSIP SYNC. ROUTINE.

2) INVOKE ICC MSG COLLECTOR TO TURN ICC BUFFER OFF. (EXCLUSIVE PROCEDURE AND 50μ PROCESSING).

3) CALL FAULT MESSAGE SCAN
50μ PROCESSING AT 25/SEC TO CHECK FLAGS.
400μ PROCESSING AT 1/SEC TO SCAN FMPTS.

4) WAIT FOR COMPLETE OF MTU READ 5/SEC. MOVE INTO ICC BUFFER (50μ).

5) ISSUE ICC WRITE FOR:
RM COMPARE WORD - 4 16-BIT WORDS
GPC TIME - 4 16-BIT WORDS 5/SEC
GPC AND DPS STATUS WORDS - 56 16-BIT WORDS 1/SEC
FDI IS PERFORMED AT ICC I/O COMPLETION. (90μ)

6) CALL DOWNLIST FOR PMU WRITES.

7) WAIT FOR ICC READ COMPLETE.

8) CALL ICC ROUTER FOR:
NO MESSAGE (50μ) 20/SEC
MTU DATA MOVED (180μ) 5/SEC
GPC AND DPS STATUS WORDS MOVED (470μ) 1/SEC

9) LIGHT AND ALARM PROCESSING PERFORMED ON FUEL GAUGING 1/SEC.

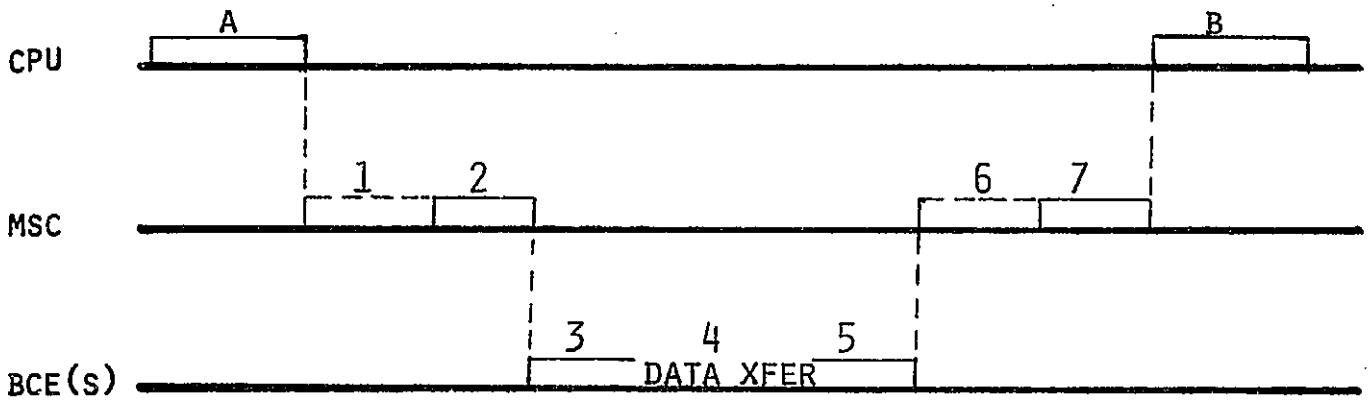
10) PROCESS MTU RM 5/SEC

11) CLOSE

*370μ OF MISCELLANEOUS PROCESSING IS REQUIRED FOR STEPS 2-10.

APPENDIX C

APPLICATION REQUEST FOR I/O
SEQUENCE OF EVENTS



A. FCOS STARTS REQUEST. 250μ-300μ

1. TIME FROM FCOS READYING THE REQUEST UNTIL MSC STARTS ON REQUEST 0-300μ AVG. 73μ

2. MSC SET UP TIME 150μ-220μ AVG. 172μ

3. BCE SET UP TIME WRITE-165μ/BCE PROGRAM IN CHAIN
READ - 200μ+200μ/BCE PROGRAM IN CHAIN

4. BUS SPEED 33μ/16-BIT WORD

5. BCE CLEAN-UP TIME 66μ

6. MSC RECOGNITION OF BCE COMPLETION DEU, PMU BUSSES 164-8100μ, AVG 762μ
FC, ICC BUSSES 20-400μ, AVG 95μ

7. MSC CLEAN-UP TIME 50-65μ AVG 58μ

8. FCOS SERVICES OF I/O INTERRUPT AND DISPATCHING OF TASK IF IT WAITED.

RANGE OF TIMES WITHIN IOP (1-7):

DEU, PMU REQUEST:
MIN .43 MS + BCE SET UP (3) + DATA TRANSFER (4)
MAX 8.75 MS + BCE SET UP (3) + DATA TRANSFER (4)
FC, ICC REQUEST:
MIN .29 MS + BCE SET UP (3) + DATA TRANSFER (4)
MAX 1.05 MS + BCE SET UP (3) + DATA TRANSFER (4)

SDL FC MODE ALT

FINAL MODELING ANALYSIS

FINAL REPORT

6/11/75

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Management Overview

Based on analysis of simulation modeling data, the current SDL design does not provide real time responses to FC commands in every minor cycle. Real time support (reported in Reference 2) has been impacted by the following increases:

- Pass 2 Math Model execution time
- Output calibration processing time
- EOML time in current FSW I/O profile.

The key results of this analysis are summarized below:

- Real Time was achieved in 7 out of 25 minor cycles
- Average SDL response time was 24.6 ms
- The SDL response complete time/elapsed minor cycle time difference for non-real time minor cycles ranged between 0.1-3.3 ms and averaged 2.0 ms.
- Average CPU utilization was 84.3%.

This analysis resulted in the following design recommendations that can improve the SDL response time by as much as 8.3 ms. The estimated savings is indicated in parenthesis for each recommendation.

- Overlapping some Pass 2 Model CPU with PDA1 I/O. (≈ 3.7 ms)
- Calibrate and Transfer output (Header + Data + Filler) of Pass 1 Model execution. (≈ 3.1 ms)
- Reduce discrete and analog data VBS buffer control word overhead. (≈ 1.0 ms)
- Reduce math model CPU through tighter code. (≈ .5 ms)

As a result of this study the following areas of concern have been identified for SDL consideration:

- SDL response time should be targeted less than 20 ms to allow for FSW design changes, safety and growth factors.
- Consider the need for real time runs and effect on CPU and response time during user aids and background activity.
- There is a time period of at least 3.6 ms in every minor cycle where the data in the Variable Buffer Storage (VBS) is not homogeneous. If the FC stops after EOML, this time can grow to 15 ms or more. The impact of this condition on simulation fidelity must be understood and resolved by SDL personnel as soon as possible to minimize program impact.

2. Objectives and Accomplishments

The objectives of this analysis effort were as follows:

- To further evaluate the SDL's ability to provide real time responses to FC ALT I/O
- To identify Host CPU utilization
- To analyze optimization of the PDA2 data collection buffer size.

The above objectives have been achieved using analyzed data from computer simulation runs based on the following:

- A model representing the current SDL Host & FEID Designs
- A full minor cycle ALT FC I/O Profile, for Approach and Landing phase, (Reference 1) as opposed to the Flight Critical I/O Profile used in the Interim Modeling Analysis. The I/O Profile includes minor cycle sample variation and DEU traffic but not MM traffic because MM is not accessed during Approach and Landing Phase.
- Measurements of ALT Math Model execution times and output calibration processing time (Attachment I).
- Host-to-FEID PDA1 Traffic Profile (Attachment II).
- Control Program Services supplied by MPSM, Systems Analysis' simulation model of EOS.

Results

3.1 Real time Response - Based on model simulations, the current SDL design does not support real time response to FC commands in every minor cycle. The total number of real time minor cycles was 7 out of 25. Previous results presented in the Interim Modeling Analysis Report (Reference 2) showed all 25 minor cycles achieved real time response to FC commands. The reduction of real time minor cycles can be attributed to the following reasons:

- A 3.3 ms increase in Pass 2 Math Model execution times by replacing estimated math model times with actual measured times.
- An 8μs/data item increase in output calibration processing time also by using actual measured times.
- A correction to Systems Analysis SDL Model design to include calibration of Pass 1 Math Model output after Pass 2 Math Model execution, instead of after Pass 1 Model execution.
- An increase in EOML (End of Minor Loop) time due to Flight Software design changes.

The SDL response times for the current design ranged from 23.0 to 25.7 ms and averaged 24.6 ms. Figure 1 illustrates a breakdown of SDL response times. Interim Modeling Analysis results showed the SDL response times averaged 20.7 ms. but the components of the SDL response have increased since that study. Table 1 presentes a comparison of previous and current SDL design results with EOS overhead included in the response times.

Since the current design does not support real time, two design changes as described below were analyzed:

- Design Change 1 (DC1) - Calibrate Pass 1 Math Model output after Pass 1 Math Model execution.

- Design Change 2 (DC2) - Calibrate Pass 1 Math Model output and transfer Data I/O (Header + Data + Filler) after Pass 1 Math Model Execution.

Results of design changes are compared to current design in Table 2. DC2 shows an average SDL response savings of 2.5 ms and an increase in the number of real time minor cycles. The average CPU utilization increased by 5.8%. This design change is recommended to be implemented to the SDL design to improve the SDL response and real time support.

3.2 CPU Utilization - The CPU utilization for the SDL in FC Mode is summarized below:

Components	Average CPU %
SDL	79.3
EOS	5.0
TOTAL	84.3

The total CPU utilization ranged from 72.3 to 94.1% The average CPU utilization for the SDL is approaching the design guideline of 85%. CPU utilization is expected to increase with the addition of user aids and background activity. Thus any tuning of the SDL system must be considered in light of the impact on CPU utilization.

The EOS CPU utilization is low because it represents only a one second steady state environment for the simulation job step, with no user aids active. This EOS CPU utilization can't be used as a general figure for EOS usage by the SDL.

3.3 PDA1 Buffer size - To analyze optimization of the PDA2 data collection buffer sizes, four cases of the SDL model were run varying the Priority and Non-Priority Data Collection buffer sizes. The results of these cases are summarized in Table 3. The results shows that more real time minor cycles and lower SDL response complete times can be achieved by varying the buffer sizes. Although case 4 shows profitable results over all, the buffer size of 2048 bytes increases the probability for a long hold off of a priority buffer. The non-priority buffer size of 1024 is suggested since this buffer size is the same for RTLOG and will balance I/O overhead with hold-off potential.

This PDA1 buffer size analysis indicates that the SDL can be tuned, but tuning is very I/O Profile dependent.

4. Conclusions and Recommendations

This analysis of the current design of SDL for the ALT FC Mode has lead to the following conclusions:

- SDL design does not currently support real time.
- The SDL can be "tuned" to meet real time support.

The SDL response time can be improved by as much as 8.3 ms by implementation of the following recommendations:

- Reduce critical path elapsed time by overlapping some Pass 2 model CPU with PDA1 I/O. (≈ 3.7 ms savings)
- Transfer Output (Header + Data + Filler) of Pass 1 Math Models after Pass 1 Math Model execution. (≈ 1.8 ms savings)
- Calibrate Pass 1 Math Model output after Pass 1 Math Model execution. (≈ 1.3 ms savings)
- Reduce PDA1 transfer time for real time runs by reducing discrete and analog data VBS buffer control word overhead (≈ 1.0 ms savings)
- Reduce critical path math model CPU by tighter code (≈ 0.5 ms savings).

The following concerns must be addressed to avoid problems in the future:

- The need for real time runs and the affect on CPU and response times during
  - user aid activity
  - background activity
  - host substituted DEU/MM I/O
- Further increases in the EOML time due to FSW design changes.
- SDL response time should be targeted < 20 ms to allow for growth and safety factors.
- Time period of at least 3.6 ms in every minor cycle where the data in the Variable Buffer Storage (VBS) is not homogeneous.

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FIGURE 1

CURRENT DESIGN SDL RESPONSE TIME BREAKDOWN
(TIMES IN MILLISECONDS)

TOTAL ELAPSED SDL RESPONSE TIME

RANGE	23.0 - 25.7			
AVERAGE	24.6			
	HOST STARTUP TIME[1]	PASS II MODEL EXECUTION	PASS I AND PASS II OUTPUT CALIBRATION	PDA1 TRANSFER
	2.3 - 2.6	10.5	3.1 - 3.4	7.1-7.5
	2.4	10.5	3.1	7.2

SDL RESPONSE COMPLETE TIME (FROM START OF MINOR CYCLE):

RANGE: 38.4 -43.8 AVERAGE: 41.2

NUMBER OF REAL TIME MINOR CYCLES - 7

SDL RESPONSE COMPLETE TIME/ELAPSED MINOR CYCLE DIFFERENCE FOR 18 NON-REAL TIME MINOR CYCLES

RANGE: 0.1 -3.3 AVERAGE 2.0

[1]STARTS WHEN DATA COLLECTION OF EOML DATA HAS COMPLETED; AVERAGE FET=16.6MS (RANGE= 14.3-18.7MS)
SOURCE: SDL MODEL BASE CASE RUN 6/6/75

Table 1

Comparison of SDL Response Time Averages
(Times in Milliseconds)

SDL Response Category	Previous Results* 3/5/75	Current Design** 6/6/75	Variance
Flight Elapsed Time for EOML Data in PDA2 Data Collection Buffer	10.5	16.6	+6.1[1]
SDL Startup Time (PDA2 Transfer + Input Calibration)	4.2	2.6	-1.6[1]
Pass II Model Execution Time (Includes SLINKER overhead)	7.6	10.9	+3.3[2]
Pass I & Pass II Output Calibration Time	1.3	3.1	+1.8[3]
PDA1 Startup/Transfer Time	7.6	8.0	+0.4[4]
SDL Response Complete Time (Includes task communication/linkage overhead)	31.2	41.2	10.0

1. Flight Software I/O Profile differences

2. Increase due to using measured math model execution time

3. Increase due to change in output calibration time of 18μs/data item to 23μs/data item and design change

4. Previous results based on hand calculation

*Source: Interim Modeling Analysis - Final Report (Reference 2).
**Source: SDL Model Run 6/6/75

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Table 2

SDL Design Changes Response Statistics
(Times in milliseconds)

SDL Response Category		Current Design[1]	Design Change 1[2]	Design Change 2[3]
SDL Response Time	R	23.0-25.7	22.5-24.0	21.0-23.5
	A	24.6	23.3	22.1
SDL Response Complete	R	38.4-43.8	37.3-42.3	35.9-41.3
	A	41.2	40.0	38.7
SDL Response Complete Time/Elapsed Minor Cycle Differences for Non-Real time Minor Cycles	R	0.1-3.3	0.6-2.2	0.5-0.8
	A	2.0	1.2	0.6
Number of Real time Minor Cycles		7	12	20
Number of Non-Real time Minor Cycles		18	13	5
Average Pass 2 Output Calibration Time		3.1	2.0	2.0
Average PDA1 Transfer Time		7.2	7.2	5.7
CPU Utilization		84.3%	84.5%	90.1%

R-range A-average

1 Source: SDL Model runs 5/20/75
2 Source: SDL Model runs 6/6/75
3 Source: SDL Model runs 6/11/75

TABLE 3

SDL ALT FC MODE RESPONSE COMPLETE STATISTICS
(TIMES IN MILLISECONDS)

	AVERAGE	RANGE	NUMBER OF REAL TIME MINOR CYCLES
BASE CASE (512/512)*	41.3	38.4 - 43.8	7
CASE 1 (256/512)	41.3	38.4 - 43.7	7
CASE 2 (128/512)	40.9	37.8 - 43.7	10
CASE 3 (128/1024)	40.7	37.8 - 43.2	11
CASE 4 (128/2048)	40.6	37.8 - 43.2	11

*(XXX/YYY) = PRIORITY/NON-PRIORITY DATA COLLECTION BUFFER SIZES IN BYTES

SOURCE: SDL MODEL SIMULATION RUNS 5/19 - 5/21/75

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5. References

1. Memo to K. J. Davidson from J. E. Knight, 4/7/75 "SDL FC Mode ALT Final Modeling Analysis - Initial Report".

2. Memo to K. J. Davidson from R. S. Carter, 3/5/75 "SDL FC Mode (ALT) Interim Modeling Analysis - Final Report".

ATTACHMENT I

ALT HOST MODEL EXECUTION SEQUENCE SIMULATED

MODULE	MODEL	CYCLE # (1-25)	MEASURED CPU/EXEC. (MS)	EXECUTION PHASE	MEASURED PROGRAM SIZE
SMDLGACS	ACS	ALL	2.200	II	6K
SMDLENV2	AER(2)	ALL	1.260	II	2K
	EOM(2)	ALL	.890	II	3.5K
SMDLGSEN	IMU(2)	ALL	4.800	II	7K
	RGA	ALL	.610	II	0.5K
	NLA	ALL	.720	II	1.0K
SMDLGLDS	LDS	ALL	.270	I	1.0K
SMDLENV1	EOM(1)	ALL	.550	I	1.0K
	ERV1	ALL	1.830	I	1.0K
	ATM	ALL	.620	I	1.0K
	WND	ALL	2.000	I	1.0K
	GRA	ALL	.660	I	1.0K
	LND	ALL	3.830	I	-
	AER(1)	ALL	8.800 1ST MC .520 2-25TH MC	I	2.0K
SMDLGNAV	TAC	ALL	2.160	I	2.5K
	MLS	3,8,13, 18,13,	.900	I	2.5K
	RAD	ALL	.600	I	1.5K
	IMU(1)	ALL	.950	I	1.5K
	ADS	ALL	.830	I	1.5K
SMDLSPMU	PMU	ALL	.500	I	-
SMDLRCLK	-	ALL		I	.1K

SOURCE: SDL DEVELOPMENT PERSONNEL, 4/14/75

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ATTACHMENT II

ALT HOST-TO-FEID PDA1 TRAFFIC PROFILE MODELED

LOAD MODULE/ PARAMETERS	NUMBER OF WORDS (16-BIT) CALIBRATED	TOTAL OUT[1]	CYCLES OUTPUT (ALL = 1 THRU 25)
PHASE II MODELS			
SMDLGACS/			
ACS FDBK. SIG.	28	152	ALL
ACS DISC. SIG.	0	22	ALL
SMDLENV2/-	NONE	NONE	N/A
SMDLGSEN/			
IMU(2)	42	60	ALL
RGA	9	60	ALL
NLA	6	48	ALL
RGA DISC.	0	30	ALL
PHASE I MODELS			
SMDLGLDS/LDS	NONE	NONE	N/A
SMDLENV1/-	NONE	NONE	N/A
SMDLGNAV/			
TAC	15	48	ALL
MLS	9	30	3,8,13,18,23
RAD	4	32	ALL
ADS	28	56	ALL
NAV DISC.	INCLUDED WITH CSB DISCRETES		N/A
CSB DISC.	0	54	DEMAND RESPONSE
MAN CONTROL	30	62	DEMAND RESPONSE
EDS	2	6	DEMAND RESPONSE
SMDLSPMU/PMU	0	42	ALL

SOURCE: SDL PERSONNEL 3/75

[1] INCLUDES FILL, HEADER, & FEID BUFFER CONTROL WORDS

FEID DEU CONTROLLER TRAFFIC ANALYSIS

FINAL REPORT

6/13/75

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PURPOSE AND SCOPE

This report covers the results of the DEU Controller study, completed 3/26/75, and the DEU Controller/FEID study, completed 5/19/75. The purpose of these studies was to evaluate the DEU Controller under worse case loading conditions.

The scope of this study was limited to a DEU Controller stand-alone case and DEU plus FEID with OFT worse case I/O Profile cases.

STUDY OBJECTIVES

The objectives of this study were to determine:

1) DEU Controller CPU Utilization
2) Response times of various DEU commands. (MODE STATUS, KEYBOARD REQ & MEM FILL)
3) The response time to the first word of a KEYBOARD request.

The results of these studies are discussed under study findings. Also additional statistics are presented for:

1) AGE/PDA2 controller CPU Utilization - This includes only PDA2 data collection activity.
2) Data Collection Response times from the start of Data Collection until the DEU Controller level 1 interrupt occurs.

3) PDA2 Data Collection response times measured from the time a full buffer is ready for transfer until the PDA2 transfer complete interrupt occurs.

METHOD

The first study was conducted using a discrete model of the DEU Controller software and its hardware interfaces (Case 1). The DEU Controller model is based on the design reflected by References 1-4. This model was combined with the current FEID model for the second study (Cases 2 and 3). FEID model is based on the design reflected in reference 5. Case 3 was run for comparison with case 2 to determine the impact of DEU traffic on PDA2 buffer response times.

The configuration used in these studies are summarized on Chart 1. The number of real and virtual DEU's shown were included in all Poll and Graphic update sequences.

	Case 1	Case 2	Case 3
DEU Traffic	Heavy	Heavy	Light
FEID Model Included	No	Yes	Yes
Num Real DEU's (Poll and Graphic Update)	3	3	1
Num Virtual DEU's (Poll and Graphic Update	1	1	0
Simulation Time	2 sec.	1 sec.	1 sec.
Poll Rate	100 ms	100 ms	100 ms
Total Positive Responses	5	5	0
Graphic Update Rate	100 ms	100 ms	1 sec
Graphic Update Word Count	509	509	300

STUDY CONFIGURATION CHART

CHART 1

STUDY FINDINGS

Table 1 summarizes the overall controller CPU utilization, traffic, command and Data Collection responses for all modeled cases. Tables 2, 3 and 4 show detailed command responses for each modeled case.

The DEU Controller CPU utilization is under 10% for all modeled cases. The CPU utilization for the PDA2 controller includes only Data Collection traffic with no AGE or discrete traffic. Case 1 shows a low PDA2 CPU utilization because lower process times were used for this earlier case.

The Channel Controller Queue (CCQ) was stopped twice (awaiting buffers) by virtual DEU 4 in case 1 only. The CCQ stopped for 1690 seconds on a KEYBOARD REQUEST and for 1184 seconds on the following KEYBOARD ECHO. These delays in getting buffers are caused by Controller processing for MEMORY FILLS for DEU's 1, 2 and 3 during the KEYBOARD REQUEST for DEU 4. These stops caused a maximum build up in the CCQ of 39 words. The CCQ stack can handle 128 words before it is necessary to stop the Flight Computer. This traffic case and timing are in the extreme and are not likely to be encountered in actual operation. Positive responses from all 4 DEU's on the same 100 milli-second polling cycle do not cause the CCQ to stop because the Flight Computer timing between KEYBOARD REQUESTS separates these activities enough to prevent buffer depletion.

In Table 1, average response times in micro seconds are shown for each command type. Line 1 for each command shows responses which are not perturbed by other controller activity. Lines 2 and 3 show perturbations within the controller for other DEU activity or hold off because of MEMORY FILL to the same DEU. Line 2 of the (509 and 300 word) MEMORY FILLS shows the response of the virtual DEU. Since there is no I/O to a DEU device to complete, the response of a virtual DEU is measured to the completion of Data Collection.

Comparison of PDA2 Data Collection responses for Case 2 and Case 3 show no significant (14μsec) difference in the average response time for Non-Priority Data collection buffers. Average Priority Data Collection buffer response times do show a difference of about 10% (52μsec) but this is not great enough to affect overall performance.

REFERENCES

1. DEU Controller Program Flow Charts from Bill Carter 10/10/74.

2. IOPI Flow Hardware Flow Charts from John King 10/30/74.

3. Telephone conversations with Bill Carter and John King Dec. 1974 and Jan.-March 1975.

REFERENCES (CONT.)

4. SDL Requirements Document Vol. 2 Part 2 Section 6 MCDS Rev 7/8/74.

5. FEID Design and Performance Specification Change Set 10 (Rev 3) 2/24/75 Contract NAS 9-13548, Drawing No. 7929440.

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STUDY SUMMARY

		3-26-75 Study DEU Only Heavy Traffic	5-19-75 Study DEU + FEID Heavy Traffic	5-19-75 Study DEU + FEID Light Traffic
		Case 1	Case 2	Case 3
Total Time Simulated		2 sec.	1 sec.	1 sec.
DEU Controller CPU Utilization		4.52%	5.02%	.76%
Level 0 Utilization		NA	1.11%	.14%
Level 1 Utilization		NA	1.17%	.16%
Level 2 Utilization		NA	2.57%	.29%
Level 3 Utilization		NA	.15%	.15%
PDA2 Controller CPU Utilization		1.39%	4.26%	1.00%
DEU Controller Queue Activity				
CCQ Maximum Content (Wds)		39	4	1
Total Traffic (Wds)		42989	21510	322
Level 0 Queue Max Content (MSGS)		1	1	1
Total Traffic (MSGS)		265	145	21
Level 1 Queue Max Content (MSGS)		1	1	1
Total Traffic (MSGS)		294	162	27
Level 2 Queue Max Content (MSGS)		5	4	1
Total Traffic (MSGS)		175	95	11
Level 3 Queue Max Content (MSGS)		1	1	1
Total Traffic (MSGS)		8	5	5
DEU SIO Queue Activity				
DEU 1 Maximum Content (MSGS)		2	2	1
Total Traffic (MSGS)		34	20	6
DEU 2 Maximum Content (MSGS)		1	2	1
Total Traffic (MSGS)		31	20	5
DEU 3 Maximum Content (MSGS)		1	1	1
Total Traffic (MSGS)		31	17	5
MODE STATUS Avg. Resp.	1	253	254	252
	2	1468	-	-
KEYBOARD REQUEST Avg. Resp.	1	3425	3259	-
	2	17284	-	-
KEYBOARD REQUEST 1st wd	1	1960	1964	-
	2	2483	-	-
Avg. Resp.	3	15994	-	-

(Table 1 Continued on Next Page)

STUDY SUMMARY (CONT.)

		3-26-75 Study DEU Only Heavy Traffic	5-19-75 Study DEU + FEID Heavy Traffic	5-19-75 Study DEU + FEID Light Traffic
		Case 1	Case 2	Case 3
ECHO CHECK Avg. Resp.	1	3237	3235	-
	2	1776	-	-
	3	-	20244	-
MEM FILL (509 wds)	1	35301	35143	-
Avg. Resp.	2	24069	24566	-
MEM FILL (300 wds)	1	20481	-	20403
Avg. Resp.	2	10916	-	-
PDA2 - Buffer Response Times				
HIGH PRIORITY DATA COLL. (5 WORD BUFFERS)		-	950	-
PRIORITY DATA COLL. (78/79 WORD WEIGHTED AVERAGE BUFFERS)		-	550	498
NON-PRIORITY DATA COLL. (256 WORD BUFFERS)		-	1330	1316

-Table 1-

DEU RESPONSES CASE 1

Case 1 (3-36-75) DEU Controller Only	DEU DEVICE (1-3 REAL) (4 VIRT)	NUM MSGS	Response Times in μsec. AVG	LOW	HIGH
MODE STATUS REQUEST	1	20	252	249	255
	2	20	1468	1462	1478
	3	20	253	248	255
	4	20	254	250	267
KEYBOARD REQUEST (Full MSG)	1	2	17284	17276	17291
	2	1	3240	-	-
	3	1	3264	-	-
	4	1	3772	-	-
KEYBOARD REQUEST (1st word)	1	2	15994	15993	15995
	2	1	1953	-	-
	3	1	1967	-	-
	4	1	2483	-	-
ECHO	1	2	3232	3231	3232
	2	1	3243	-	-
	3	1	3238	-	-
	4	1	1766	-	-
MEMORY FILL (509 wds)	1	21	35671	34230	35844
	2	20	34941	34903	34966
	3	20	35293	35257	35316
	4	20	24069	24010	24149
DATA COLLECTION FOR MEM FILL	1	21	2335	1876	2366
	2	20	2214	2192	2258
(510 wds)	3	20	2354	2322	2384
	4	20	2343	2327	2369
MEMORY FILL (300wds)	1	1	20506	-	-
	2	1	20517	-	-
	3	1	20420		
	4	1	10916	-	-
DATA COLLECTION FOR MEM FILL	1	1	1264	-	-
	2	1	1424	-	-
(300 wds)	3	1	1248	-	-
	4	1	1019	-	-

-Table 2-

DEU RESPONSES CASE 2

Case 2 DEU + FEID/HEAVY TRAFFIC	DEU DEVICE (1-3 REAL) (4 VIRT)	NUM MSGS	Response Times in μsec. AVG	LOW	HIGH
MODE STATUS REQUEST	1	10	257	248	300
	2	10	252	247	255
	3	10	252	248	254
	4	10	253	249	255
KEYBOARD REQUEST (Full MSG)	1	2	3239	3236	3246
	2	2	3283	3293	3273
	3	1	3254	-	-
	4	-	-	-	-
KEYBOARD REQUEST (1st word)	1	2	1949	1948	1949
	2	2	1985	1973	1997
	3	1	1957	-	-
	4	-	-	-	-
ECHO	1	2	3243	3249	3237
	2	2	*20244	20239	20249
	3	1	3227	-	-
	4	-	-	-	-
MEMORY FILL (509 wds) (No Occurrance of 300 wds for this case	1	10	34884	34822	35035
	2	10	35096	34623	35260
	3	10	35448	35210	35563
	4	10	24566	22901	25039
DATA COLLECTION FOR MEM FILL (510 wds)	1	10	2668	2509	3190
	2	10	2638	2618	2673
	3	10	2676	2630	2749
	4	10	2648	2605	2680
PDA2 Data Collect Responses					
HIGH PRI DATA COLL. (5 WORD BUFFERS)	50	10	950	236	1401
PRIORITY DATA COLL. (78 WORD WTD AVG BFRS)	1887	24	**550	**487	**785
NON-PRI DATA COLL (256 WORD BUFFERS)	24832	97	1330	1273	1697

*SIO to IOPI held off by MEM FILL between KBD REQ and ECHO
**Values Corrected for 78 Word Avg Buffer.

-Table 3-

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DEU RESPONSES CASE 3

Case 3 DEU + FEID/LIGHT TRAFFIC	DEU DEVICE (1-3 REAL) (4 VIRT)	NUM MSGS	Response Times in µsec AVG	LOW	HIGH
MODE STATUS REQUEST	1	10	252	249	255
	2	-	-	-	-
	3	-	-	-	-
	4	-	-	-	-
KEYBOARD REQUEST (Full MSG)	1	-	-	-	-
	2	-	-	-	-
	3	-	-	-	-
	4	-	-	-	-
KEYBOARD REQUEST (1st word)	1	-	-	-	-
	2	-	-	-	-
	3	-	-	-	-
	4	-	-	-	-
ECHO	1	-	-	-	-
	2	-	-	-	-
	3	-	-	-	-
	4	-	-	-	-
MEMORY FILL (300 wds) (No occurance of 509 words for this case)	1	1	20403	-	-
	2	-	-	-	-
	3	-	-	-	-
	4	-	-	-	-
DATA COLLECTION FOR MEM FILL (301 wds)	1	1	1326	-	-
	2	-	-	-	-
	3	-	-	-	-
	4	-	-	-	-
PDA2 Data Collect Responses					
HIGH PRI DATA COLL	-	-	-	-	-
PRIORITY DATA COLL (79 WD WTD AVG BFR)	1972	25	**498	**491	**507
NON-PRI DATA COLL (256 WORD BUFFERS)	3072	12	1316	1270	1700

**Values Corrected for 79 Word AVG Buffer

-Table 4-

SDL/FSW JOBSHOP TURNAROUND STUDY

FINAL REPORT

6/26/75

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1.0 Management Overview

The findings of this study are summarized below:

- Current job/hr rate is 5-8 jobs for SDL/FSW jobshop
- Step PLMSUP requires 400K-600K and is active approximately 65% of elapsed time in a sample segment of jobshop time
- OPDSK seek time avg 22.88 ms. to 24.33 ms.
- SYSAUX seek time avg 13.52 ms.
- SYSR21 seek time avg 32.6 ms.
- Region requests for FSIM and ICS are not excessive
- Jobshop set-up time varies from 10-30 minutes and IPL from 8-24 minutes.

Based on the above findings and associated analysis, recommendations are made for the following areas:

- Add job classes LMN to 2nd jobshop initiator
- Rearrange VTOC, CATALOG, and permanent data sets on certain disk volumes (See Section 7.0 for specific recommendations)
- Modify FSW/SDL Proc's to improve temporary data set efficiency
- Improve handling of scratch packs and permanently restored packs for jobshop
- Update the SDL simulation jobstep region estimating procedure frequently.

Also it is recommended that future studies should be conducted in the following areas:

- Analysis tools and procedures for more efficiently conducting throughput studies
- Regular analysis of FSW/SDL jobshop by Systems Analysis
- PLMSUP - to permit multijobbing or reduce elapsed time in system.

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- Frequent "Figure of Merit" studies on SVCLIB
- Modification of Job Stream Manager to permit automatic backlog aging.

2.0 Purpose and Scope

The purpose of this study was to investigate FSW and SDL jobshop turnaround and make recommendations to achieve improvements. Primary emphasis was placed on throughput (jobs/jobsteps per hour) improvements which could be easily identified and quickly realized. The impact of changes already made can't be completely evaluated without additional analysis. Areas which need additional effort or study to further improve jobshop turnaround are identified.

The scope of this study has been limited only by the amount of time allocated for completion of the study.

3.0 Objectives

The planned objectives of this study were:

a) Evaluate the Job Stream Manager (JSM) matrix and the default FSW/SDL initiator class assignments and recommend changes where necessary.

b) Measure and analyze jobshop disk volume seek times and recommend alternative data set allocations to reduce seek times.

c) Determine SDL simulation jobstep actual region requirements and reconcile an estimated FSIM region requirement of 450K with the actual requirement of 506K.

d) Obtain and analyze performance measurement data on five typical jobs.

e) Quantify the major components of jobshop turnaround, including:

- Deck submission until arrival in the RTCC.
- Time spent in the RTCC waiting to be run.
- Time spent waiting for print to complete after execution is complete.
- Time from print complete until output is returned to programmer's desk.

Of these objectives analysis of the five sample jobs (item d) and quantification of jobshop turnaround components (item e) were not pursued to completion. In depth tracking of jobs through the processes indicated would have required more time than could be made available in this study. However, a brief review of the procedures did not disclose any significant problems in this area.

4.0 Method

This analysis has been conducted using available analysis tools as follows:

Jobshop throughput/turnaround - System Management Facility (SMF), System Online (or Log Data set)
Job Performance - ASC, Load Module and Task option
DASD performance - ASC, I/O Trace option
Simulation Jobstep Region Requirements - Core Dump and Region size estimating procedure for SDL version 1 (reference 1)
Job Stream Manager - Statistical output from Job Stream Manager

5.0 Findings

The findings in this section address the following areas:

- Job Throughput
- Job Stream Manager
- Disk Volume Activity
- FSW/SDL Cataloged Procedures (Proc's)
- SDL Simulation Jobstep Region Requirements
- Operational Procedures/Scheduling

5.1 Job Throughput

The number of jobs/jobsteps per hour varies with each jobshop period. The job/jobstep rates are meaningful only if all background and environmental factors are taken into consideration. The analysis of SMF data has shown that the current job rate falls in the range of 5 to 8 jobs per hour (range of jobstep rate is 26 to 64 jobsteps per hour).

Using the first 1.5 hours of a 7.3 hour FSW jobshop period (8 P.M. on 4-30-75 to 5 A.M. on 5-1-75) an analysis was made to determine how the main core resource was being used. Figure 1 (Job Throughput) graphically depicts the elapsed time of the Program Library Management Supervisor (PLMSUP) jobstep in relation to the total time the job is in the system. In the sample period observed, the PLMSUP main core region varies from 400K to 600K and the average step elapsed time was about 6 minutes. Allocating main core for

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the size and duration of these steps has prevented multijobbing of similar steps for 65% of this segment of jobshop time. A study of ways to make PLMSUP multijobbable or reduce elapsed time in the system is recommended.

5.2 Job Stream Manager

A study of the Job Stream Manager job class assignment matrix was already underway in the ROS Dept. at the start of this study. Figure 2 shows the job class assignment matrix and initiator classes used prior to this study. The Job Stream Manager generates reports showing the reason(s) jobs are placed in a particular class. Class "L" was assigned in many cases because the estimated job time was between 5 and 15 minutes. A new matrix has been prepared by the ROS Dept. and implemented to better distribute the job classes. The new matrix will cause jobs of less than 2, 4 and 10 minutes to be assigned to classes I, J and K respectively. Also job classes LMN should be added to initiator J2 to give better turnaround on the larger and longer jobs. The Job Stream Manager matrix changes and suggested initiator class assignments are shown in Figure 2.

Job turnaround times in excess of 24 hours have been experienced on several occasions. Currently, when jobs are backlogged from one jobshop period to the next, Operations reads in the backlog jobs and allows them to start before reading in the new jobstream to give the backlog priority in the system. Since this procedure for inputting jobs doesn't insure a priority for the backlog, the newer jobs can crowd the older and longer jobs toward the end of jobshop and cause them to become backlogged again. To prevent order of reading jobs into the system from determining priority of jobs runs, the Job Stream Manager program may be modified to date and time stamp incoming jobs and then assign a higher dispatching priority and a more favorable job class to the older jobs. This would insure the backlog being run first regardless of the order in which the old and new jobstreams were loaded into the system.

5.3 Disk Volume Activity

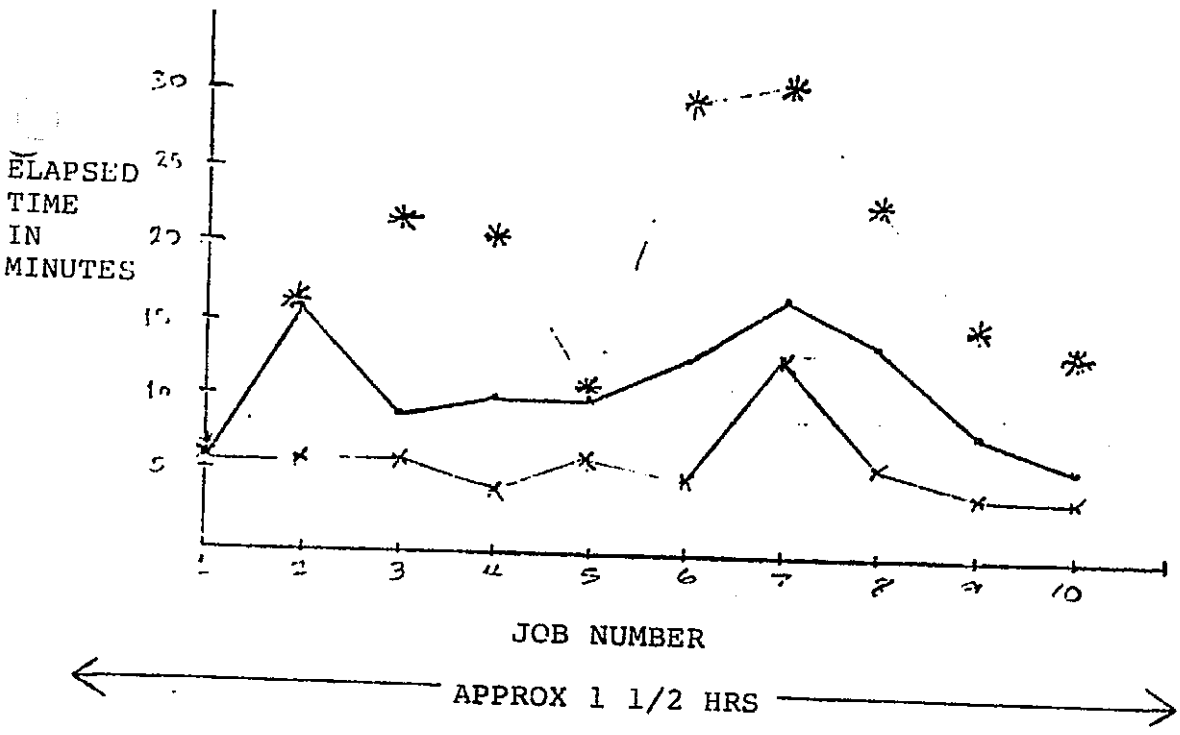
Temporary data set activity is heaviest on the OPDSK and SYSAUX volumes. For the measured cases, average disk arm seek time on OPDSK was 22.88 milli-seconds (ms) on FSW jobshop and 24.33 ms on SDL jobshop. SYSAUX, however, showed an average seek time of 13.52 ms on FSW jobshop and 14.73 ms on SDL jobshop. Analysis shows that the higher average seek time on OPDSK is caused by the relative position of the VTOC in the FSW jobshop case and the relative position of permanent data sets on that volume in the SDL jobshop

JOB THROUGHPUT PLOT

JOBSHOP RUN TIME IN HRS. (EXCLUDES SETUP)	NUMBER OF JOBS	NUMBER OF JOBSTEPS	JOBS/HR	JOBSTEPS/HR
2.0	10	54	5.0	27.0
*7.3	48	192	6.6	26.2
6.4	44	181	6.9	28.4
3.0	24	174	8.0	58.0
1.6	11	101	7.0	64.3

PLMSUP STEP ELAPSED (NO REGION WAIT TIME 59.9 MIN
WALL CLOCK TIME PERIOD 92.0 MIN

65% OF TIME PERIOD MAIN CORE WAS TIED UP WITH 400-600K REGIONS FOR PLMSUP.



—— TOTAL JOB ELAPSED TIME (INCLUDING REGION WAIT AND JOB OVERLAP)

—— TOTAL ELAPSED PLMSUP JOB STEP (INCLUDES REGION WAIT AND JOB OVERLAP)

x--x ESTIMATED ELAPSED TIME PLMSUP JOBSTEP (EXCLUDING REGION WAIT AND WITH NO JOB OVERLAP)

Figure 1

JOB STREAM MANAGER MATRIX

AND INITIATOR CLASS ASSIGNMENTS

JOB CLASS DEFINITIONS/CLASS	H	I	J	K	L	M	N	O
EXECMAIN	250	400	400	400	600	1000	1000	1000
EXECLCS	3000	3000	3000	3000	3000	3000	3000	3000
9-TRK	1	2	2	2	4	8	8	8
7-TRK	0	0	0	0	0	0	0	1
TAPES	1	2	2	2	4	8	8	8
SYSOUT	6000	6000	6000	6000	6000	6000	6000	32000
WORK	6000	6000	6000	6000	6000	6000	6000	32000
TIME	15	2	4	10	15	30	1440	1440
PRTY	15	15	15	15	15	15	15	15

INIT.J1,,,(DAHIJK)

INIT.J2,,,(DANMLKJIH)

INIT.J3,,,(LMNOE)

FIGURE 2

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case (see Figures 3 and 4). Moving the VTOC from cylinder 0 to the center of the data set activity would reduce disk arm movement in the FSW jobshop case. The SDL jobshop OPDSK volume does have the VTOC in the center of the volume, but permanent data sets are arranged between it and the temporary data sets. Arm movement over these unused data sets causes a higher average seek time. Scratching VTOC or clearing the pack before clipping it to OPDSK would alleviate this situation.

Figure 5 shows a SYSAUX volume with VTOC and data sets arranged for more efficient accessing, which results in an average seek time of 9-10 ms less than that observed on OPDSK.

Analysis of the access distribution and arm movement on the SYSR21 volume indicates that SVCLIB, the VTOC and JOBQUE are accessed most frequently (see figure 6). Based on the above finding, the ROS Department conducted a "Figure of Merit" study to determine which SVC modules should be made resident. A new Resident SVC list has been included in the latest ROS release and should result in at least 6% fewer accesses to SVCLIB than with the previous list. Since the jobshop environment is constantly changing "Figure of Merit" studies should be conducted at regular intervals.

Improvement in the average seek time on the SYSR21 volume is possible by arranging SVCLIB, the VTOC, CATALOG and JOBQUE together on the volume.

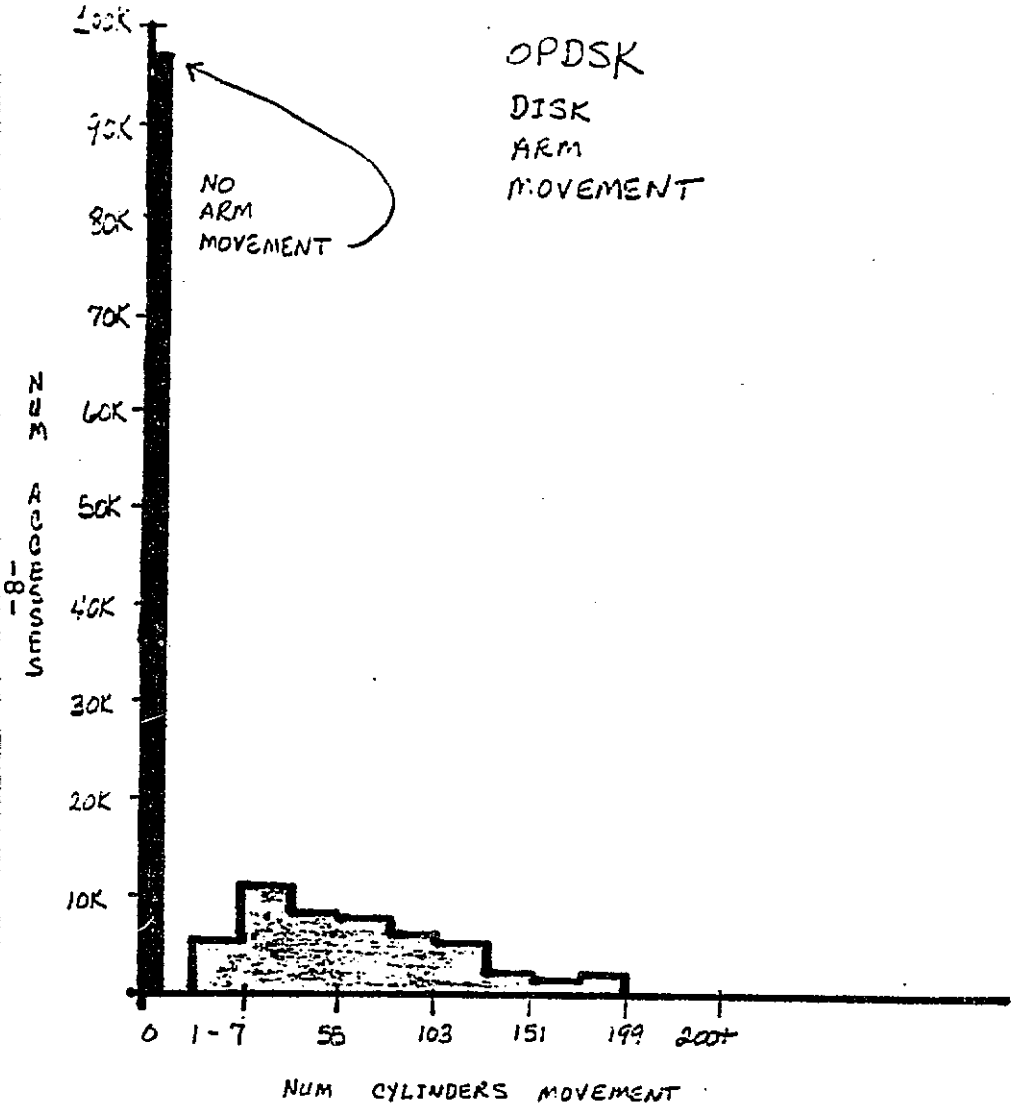
5.4 FSW/SDL Proc's

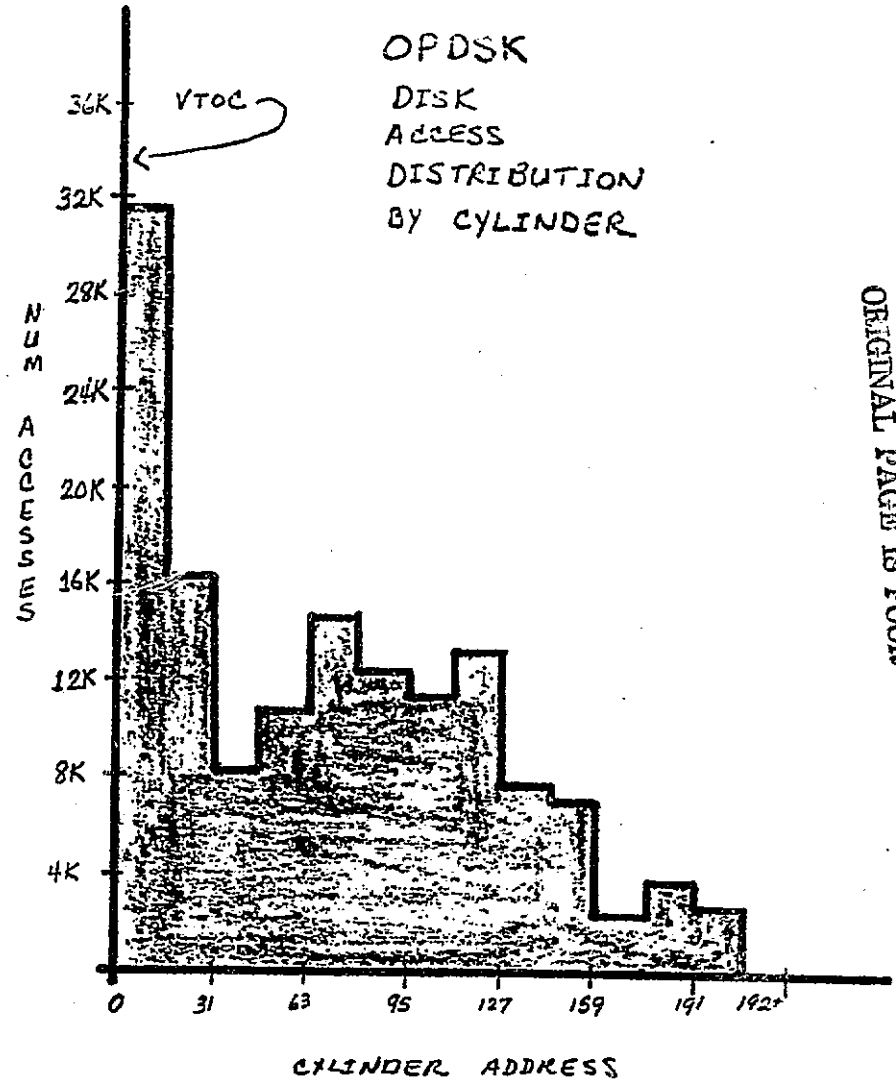
Analysis of SMF data has shown that the high speed main core resource is not always used most efficiently, especially when small I/O bound jobsteps and large CPU bound jobsteps compete for this resource. Many I/O bound jobsteps require smaller regions and use comparatively little CPU time, but occupy main core during I/O wait time. These jobsteps with smaller regions increase the possibility of core fragmentation which will prevent the larger CPU bound jobsteps from starting. Relocating these steps to LCS will not significantly impact their performance but will free up main core for the larger CPU bound steps.

At the time this study started, a list of program steps to be relocated to LCS was already being prepared (see figure 7). Evaluation of the impact of these changes cannot be determined unless additional jobshop throughput analysis is performed.

A sample FSIM job run was analyzed to determine the extent and kind of temporary data set activity. This job of four steps (compile, Pre-Sim, Simulation, and Post-Sim) caused the allocation of 60 temporary data sets. Figure 8 summarizes the use of these data sets and the average measured CPU cost of the allocate and scratch services. Although the actual allocation and scratch of

AVG SEEK TIME = 22.88 MS





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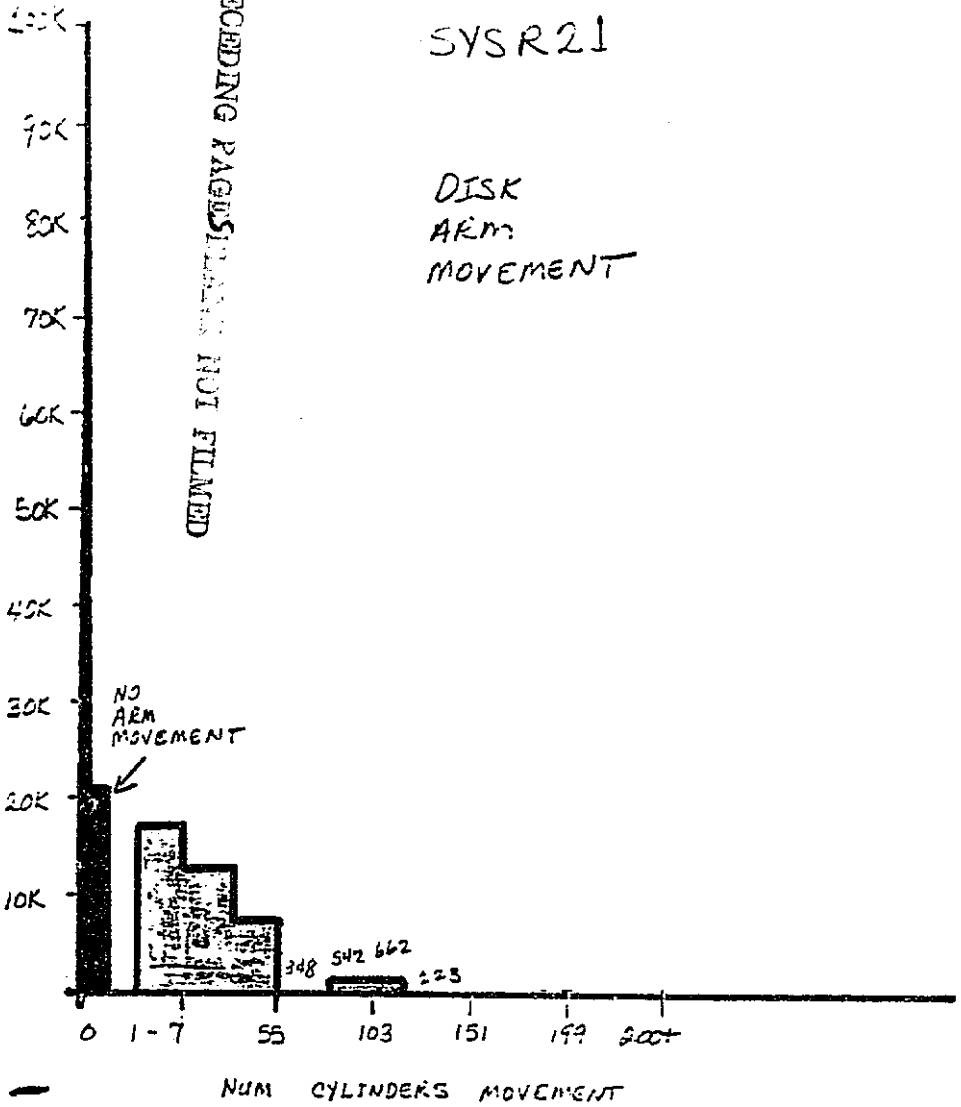
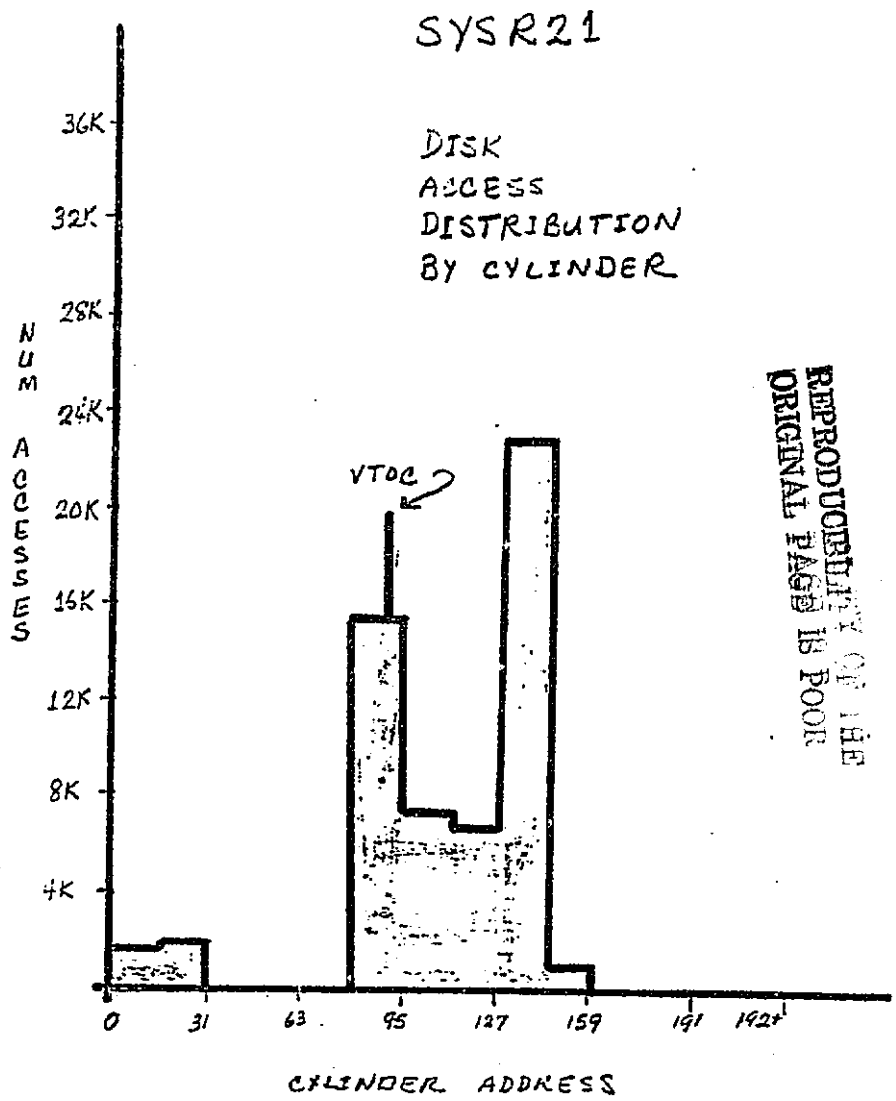
FSW JOBSHOP (10 HRS 25 MIN)

Figure 3

AVG SEEK TIME = 32.6 MS





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FSW JOBSHOP (10 HRS 25 MIN)

Figure 6

SDL PROC REGION CHANGES

PROC	PROC STEP	PROGRAM	OLD REGION	NEW REGION
*CYCTRIOI	CYCI1	SMTRIOED	150K,0)	(,150K)
	CYCI2	QMSMOVER	(20K,50K)	(,150K)
	CYCI3	QMSMOVER	(20K,50K)	(,150K)
	CYCI4	QMSMOVER	(20K,50K)	(,150K)
*CYCTRION	CYCI1	IEBGENER	(200K,0)	(,150K)
	CYCI3	IEFBR14	(2K,0)	(,80K)
	CYCI4	IEFBR14	(2K,0)	(,80K)
*CYCTRIOO	CYCO2	QMSMOVER	(20K,50K)	(,150K)
	CYCO3	QMSMOVER	(20K,50K)	(,150K)
	CYCO4	QMSMOVER	(20K,50K)	(,150K)
FSWJSTP1	JSTEP	SMDLRJSC	(0,150K)	(,220K)
*MOVER	MOVE	QMSMOVER	(20K,100K)	(,150K)
SDLCOLTP	PLMS	PLMSUP	(350K,350K)	NC
	COLPRT	QMBCOLPT	(MAIN DE-FAULT)	(,150K)
SDLDTAB	DTPLMS	PLMSUP	(350K,350K)	NC
	DTAB	REFDDTAB	(0,500K)	NC
*SDLJSTP1	JSTEP	SMDLRJSC	(150K,150K)	(,220K)
SDLDFLG	S2	SMBJMDJS	(50K,50K)	(,150K)
SDLPOST	S1	SMDLPOST	(150K,50K)	(,150K)
SDLPLOT	S2	SMDLPINT	(100K,50K)	(,150K)
SDLTEST	STST	REFCDARY	(300K,500K)	(350K,500K)

NC=No Change
*Changes for system growth only

Figure 7

these data sets takes place outside the limits of the jobsteps (i.e., within the schedular, reader, writer) the total CPU time used for these services is approximately 4.96 seconds. Compared to the 141 seconds of the job, this is an additional 3.5% of CPU time. The elapsed time for these services has not been determined. The impact for this activity is not only the CPU time overhead but the additional disk arm movement which can impact all jobs in the system.

The allocate and scratch activity can be reduced by:

- Elimination of any un-used DD cards from the Proc's. (This could occur if similar Proc's are used for different programming areas).

- The use of dedicated data sets in the initiator Proc for those temporary data sets which are most frequently used. (SYSIN and SYSOUT data sets cannot be used in this manner).

5.5 SDL Simulation Jobstep Region Requirements

Two main questions were to be answered by this study regarding main core region requirements. First, are the requested regions excessive and second, why did a reported difference of 56K exist between the estimated and the actual requirements for an FSIM run.

A mapping of main core usage was made from core dumps of the FSIM and ICS modes for the SDL simulation jobstep for Rel 4.1 version 4. The results of this effort are tabulated in Figure 9, which shows that the regions requested are not excessive.

The actual data case in which a 56K difference was observed between the estimated FSIM core requirements and the actual core requirement was not available for analysis. However, the core requirements observed in the above study were compared with the calculated estimate from the procedure outlined in the release memo for "Release 4.1 version 1 of the SDL" dated 3-28-75 (Reference 1) as follows:

SDL FSIM Mode	300K
Closed Loop GN&C Math Models	100K
Flight program size (from Dump)	33K
	433K

TEMPORARY DATA SETS ACTIVITY

FOR A FSIM JOB

TYPE DATA SET	NUM
SYSOUT	16
TEMPORARY/SYSIN	29
TEMPORARY PASSED	15
	60

	AVG EXEC TIME IN MS.	AVG TOTAL FOR SERVICE IN MS.	TOTAL TIME (IN MS.) FOR 60 SCR/ALLOC
SCRATCH	20.8	45.6	2736
ALLOCATE	6.3	37.1	2226
			4962

JOB ELAPSED TIME	12 MIN
JOB CPU TIME	141.78 SECONDS
60 SCR/ALLOCATE	4.96 SECONDS

Figure 8

SIMULATION STEP MAIN CORE USAGE

(REL 4.1 VER 4)

SUBPOOL ID	USE	MAIN CORE USED FSIM MODE	MAIN CORE USED ICS MODE
251	USER'S JOBLIB REENTRANT MODULES	100K	164K
252	LINK PACK AREA REENTRANT MODULES	8K	10K
200	REAL TIME TABLES	6K	6K
199	DYNAMIC SUBROUTINES, SYSTEM PARMS	34K	34K
191/192	RT QUES AND BUFFERS	4K	4K
0	MODE INDEPENDENT DATA BASE + BUFFER POOLS	46K	46K
43	COMMUNICATOR	18K	30K
50	ENVIRONMENT MODELS	50K	*
51	GN&C MODELS	28K	*
62	FSIM	22K	-
64	MODE DEPENDENT DATA BASE	98K	70K
67	USER AIDS (HAL SIM TABLES)	10K	-
MISC	SP65/68 USER AIDS	6K	4K
FREE	FREE REGION CORE (AT TIME OF DUMP)	70K	112K
MAIN REGION REQUESTED		500K	480K
MAIN REGION USED		462K	476K
MAIN REGION UN-USED		38K	4K

*NO MATH MODELS WERE USED IN THE ICS RUN.

FIGURE 9

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The actual core used by the Rel 4.1 version 4 run was 462K or 29K more than estimated under the procedure. Time did not permit a detailed comparison of Rel 4.1 V1 and Rel 4.1 V4 dumps, but these findings indicate that the estimating procedure needs to be reviewed and updated if necessary for each SDL release.

5.6 Operational Procedure/Scheduling

A complete study of operational procedures and scheduling was beyond the scope of this task. However, certain areas which may improve throughput if attention is given them are discussed below:

Initial set up time for a block of computer time can use from 10 to 30 minutes depending upon the number of disk volumes to be mounted, restored or cleared, the problems encountered (e.g., tape errors), and the number of other manual operator interventions required. A review of procedures for the use of permanently restored disk volumes is recommended, in conjunction with an inventory of such disk volumes.

The time between IPL and start of the first job varies. Using the onlines, times of 8 to 24 minutes were observed.

Assuming that this set up is necessary, users requiring the same set up and IPL options could be scheduled on consecutive blocks of computer time. In this way set up time could be reduced for users following the first user.

6.0 Results

Certain activities were found to be in process at the time this study started. Others were initiated as a result of this study. Those which are completed and in place now are listed below:

- Job Stream Manager parameters - a new matrix was already being prepared when this study began and is in place at this time (EOS 21.23).
- Relocation of Proc steps to LCS - an update to PROCLIB was already in process and is in place at this time.
- "Figure of Merit" study was conducted by ROS and a new Resident SVC list has been generated and is currently on the system.

Systems Analysis concurs with the changes being made in the above areas.

7.0 Recommendations/Action Items

The recommendations which follow are based on the data gathered for this study. Some areas may require some additional investigation or study before implementation.

- Add job classes LMN to initiator 2 as follows (DANMLKJIH)
- Rearrange SYSR21 to group SVCLIB, VTOC/CATALOG and JOBQUE together.
- Move VTOC and CATALOG (if applicable) to the center of activity on OPDSK, SDLA01, SDLB01, FSWA01 and SSWA01 volumes.
- Move most active permanent data sets close to VTOC and CATALOG on volumes SDLA01, SDLB01, FSWA01 and SSWA01.
- Use the SDLMM1 volume for temporary data sets because of its extremely low access frequency.
- Initiate a procedure to insure that scratch disks (OPDSK) are clear or have the VTOC scratched before being used for jobshop.
- Eliminate any un-used DD cards from Proc's.
- Select temporary data sets (other than SYSIN/SYSOUT) which can be allocated as dedicated data sets in the initiator Proc's.
- Update SDL Region Requirements estimating procedure for each version of the SDL if necessary.
- Review procedures for use of permanently restored packs and inventory the current packs.

To achieve and maintain maximum utilization of the RTCC jobshop resources, additional study efforts are necessary. The following can be done individually or together as a total effort:

- Investigate tools and procedures for performing jobshop throughput and turnaround analysis to permit more timely idnetification of problems.
- Establish an analysis task to regularly monitor FSW/SDL jobshop (should include disk activity study).

- Initiate an analysis of PLMSUP to accomplish either of the following

  - Reduce region requirements to permit multijobbing (consider LCS buffering of module and tables).

  - Reduce the step elapsed time to free up main core sooner (some of the changes which improve disk access efficiency will also help in this area).

- Initiate a task to perform "Figure of Merit" studies on jobshop at regular intervals (perhaps the need for this activity can be determined by a separate disk activity study).

- Investigate the possible modification of the Job Stream Manager to provide a date and time stamp capability for the automatic aging of backlogged jobs. Old jobs could be reassigned to a higher dispatching priority and more favorable job class.

8.0 References

1. "Release 4.1 Version 1 of the SDL" by J. R. Gililland 3-28-75.

2. "SDL/FSW Jobshop Turnaround Study - Initial Report" by J. R. McLean, 5/9/75.

PDA2 CONTENTION

SENSITIVITY ANALYSIS

FINAL REPORT

September 8, 1975

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MANAGEMENT OVERVIEW

Using Systems Analysis' simulation model of the SDL, a study of the SDL's sensitivity to the current PDA2 interface (I/F) management scheme for the 2FC and MFC modes of operation has been conducted. Analysis of simulation output reveals that:

- End-of-minor-loop (EOML) record holdoff due to PDA2 I/F contention can become sufficient (14.8 ms maximum) to keep the SDL out of real time in the 2FC and MFC modes.

- This holdoff can be reduced to 3.3 ms (maximum) by setting non-priority data collection record sizes to 256 bytes.

Final PDA2 I/F tuning recommendations, based on SDL MFC performance analysis currently in progress, will be made at the Release 6 DDR in November.

OBJECTIVES

The objectives of this study have been to:

(1) bound the expected effect of Master/Slave FEID contention for the PDA2 interface on the SDL's performance in the 2FC and MFC modes of operation, and

(2) determine how PDA2 priority record throughput might be improved.

Both of these objectives have been accomplished.

FINDINGS

Objective 1 - Bounding the Effect of PDA2 Contention

For this study PDA2 I/F contention is measured in terms of PDA2 holdoff time. Holdoff occurs in the 2FC and MFC modes when any PDA2 transfer from one FEID cannot occur immediately because the PDA2 is busy with a transfer from another FEID (see Figure 1, p. 2). Holdoff impacts SDL response performance when EOML transfers, which trigger Host processing, are delayed by non-priority transfers. Holdoff time is defined to be the elapsed time from the time the last FEID's priorioty EOML data collection record is ready for transfer over PDA2, until the time its transfer is actually started. Under the study's assumptions (Appendix A), the last EOML record in the 2FC mode is from the left slave FEID. In the MFC mode, the last EOML record is from the right slave FEID.

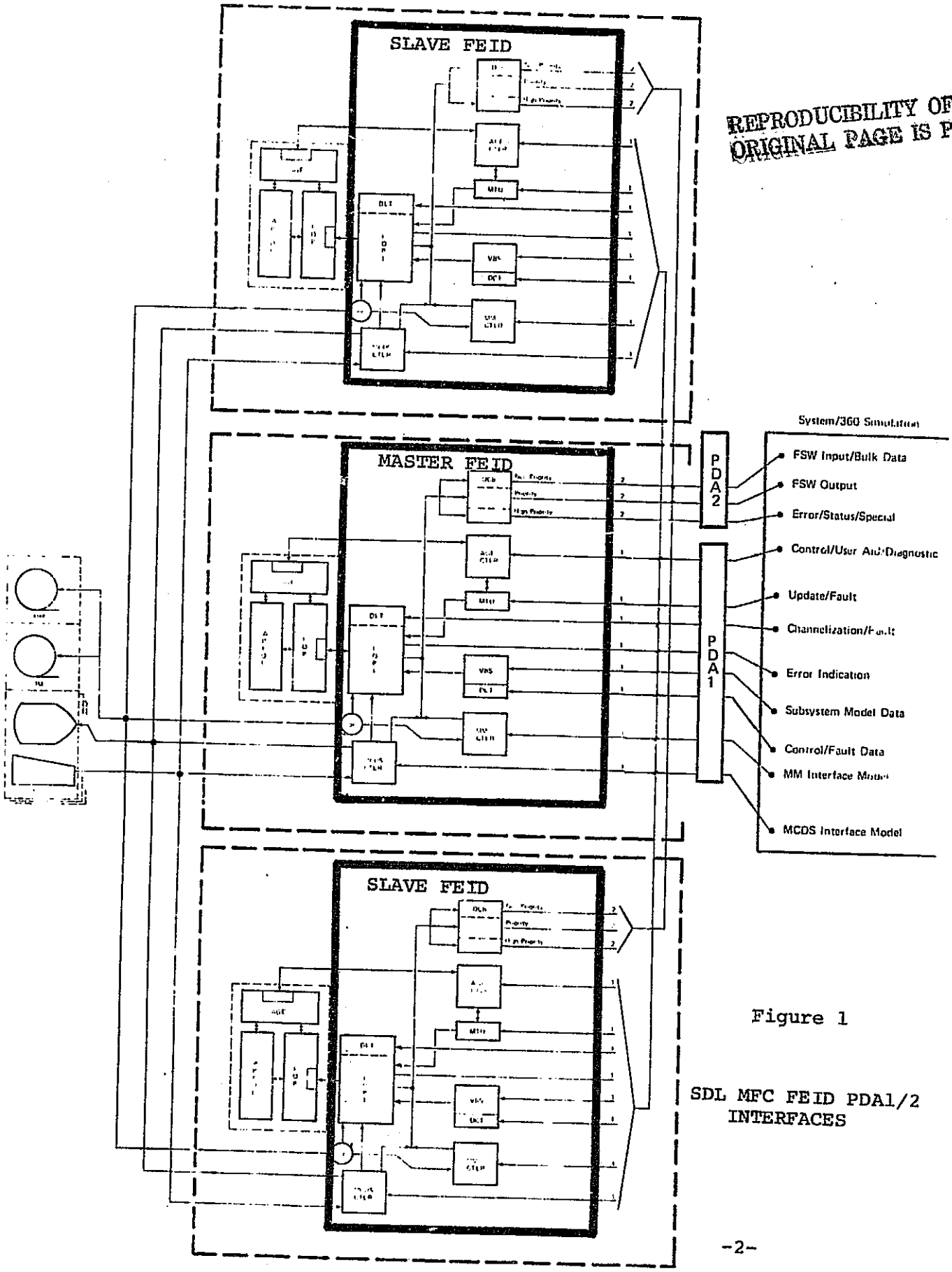

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Figure 1

SDL MFC FEID PDA1/2 INTERFACES

As shown in Table 1 (p. 4), PDA2 holdoff times range from 200 microseconds to 14.8 ms. in the environments represented by cases 1-5. The low holdoff times shown occur when Master and/or other slave FEID EOML record transfers delay the last slave FEID's EOML transfer. The high holdoff times shown occur when EOML and non-priority Master and/or other slave FEID transfers delay the last FEID's EOML transfer. Variability between cases is atributable to modeling:

- different missions (ALT vs. OFT)
- different modes (2FC vs. MFC)
- different flight computer I/O profiles (typical worst case vs. theoretical worst case)
- different data collection record sizes (minimum vs. maximum).

Based on the magnitude of the high holdoff times seen in cases 2-5 relative to the 20-25 ms. available for the Host to respond to FC I/O, SDL performance is definitely sensitive to the current PDA2 I/F management scheme. In fact EOML record holdoff can keep the SDL out of real time in the 2FC and MFC modes.

Objective 2 - Improving Priority Record Throughput

To improve PDA2 priority record throughput, three factors are analyzed with respect to their impact on interface performance:

- data collection record sizing
- equal opportunities for Master and slave FEID PDA2 transfers
- priority/FIFO PDA2 I/F management logic.

While these are not all of the variables available for interface tuning, they are logically straightforward, and are reasonable kinds of tuning to consider in this study.

Since the effect of non-priority data collection sizing was isolated in the different maximum holdoff times for cases 1 and 2, "tuned" versions of cases 1, 3, 4, and 5 were run (cases 6-9 in Table 2, p. 5) to further quantify this effect. That is, for cases 6-9 priority record sizes were set to 128 bytes and non-priority record sizes were set to 256 bytes and all other model run parameters were left unchanged. The effect of this data collection record size tuning on PDA2 contention is reflected in the dramatically reduced (.9-11.5 ms.) maximum holdoff times shown. Clearly, the impact of PDA2 contention on SDL performance can be reduced through data collection record size tuning.

Table 1

PDA2 HOLDOFF STATISTICS - INITIAL SIMULATION RUNS

Case #	Case Description[1]	PDA2 Holdoff Range Observed (ms)
1	Baseline ALT[2] 2FC (128/512)	.2-1.9
2	Baseline ALT[2] 2FC (128/1024) - Case 1 with larger non-priority record size.	.2-4.2
3	Theoretical ALT[3] 2FC (512/2048)	.5-8.9
4	Baseline OFT[4] MFC (128/1024)	.4-6.1
5	Theoretical OFT[5] MFC (512/2048)	1.6-14.8

Source: SDL MFC Simulation Model Runs 8/15-8/18/75

[1] Numbers in parentheses represent priority and non-priority data collection record sizes (in bytes), respectively.

[2] Reference 2

[3] Reference 2 with certain flight computer I/O (DEU and SM) timed to cause heavy transient loading of the PDA2 interface management logic.

[4] Reference 3

[5] Reference 3 with certain flight computer I/O (DEU and SM) timed to cause heavy transient loading of the PDA2 interface management logic.

Table 2

PDA2 HOLDOFF STATISTICS - "TUNED" SIMULATION RUNS

Case #	Case Description[1]	Holdoff Range (ms)	Improvement (ms)
6	Baseline ALT 2FC (128/256) - Tuned Case 1	.2-1.0	.9
7	Theoretical ALT 2FC (128/256) - Tuned Case 3	.2-1.5	7.4
8	Baseline OFT MFC (128/256) - Tuned Case 4	.4-1.8	4.3
9	Theoretical OFT MFC (128/256) - Tuned Case 5	.4-3.3	11.5
10	Baseline ALT 2FC (128/256) - Case 6 w/Priority/ FIFO I/F Management	.2-.5	.5[2] (1.4)
11	Baseline OFT MFC (128/256) - Case 8 w/Priority/ FIFO I/F Management	.4-.8	1.0[2] (5.3)

Source: SDL MFC Simulation Model Runs 8/19-8/21

[1] Numbers in parentheses represent priority and non-priority data collection record sizes (in bytes), respectively.

[2] These savings are in addition to the savings realized in cases 6 and 8. The numbers in parentheses represent total savings for cases 1 and 4.

In evaluating the second PDA2 I/F performance factor, equal opportunities for Master and slave FEID transfers, the following PDA2 I/F management polling schemes were simulated:

2FC -	Master FEID	Left Slave FEID	Master FEID	Left Slave FEID	. . .
MFC	Master FEID	Left Slave FEID	Master FEID	Right Slave FEID	. . .

Since the current scheme allows two Master FEID transfers per slave transfer, the intent of these new schemes was to give the slave FEID('s) the same number of chances as the Master FEID to transfer data over PDA2. However, no improvement in PDA2 throughput was gained. This is because the new schemes did not eliminate the factors contributing to PDA2 holdoff, but merely effected a re-ordering of those transfers which delay the last FEID's EOML record transfer.

To evaluate the third tuning consideration, a PDA2 I/F management scheme was simulated which transferred data collection records on a priority/FIFO basis. That is, the oldest and highest priority record ready for transfer at the time the interface became available was transferred, regardless of the originating FEID. Using this scheme, cases 6 and 8 were rerun and additional holdoff reductions of .5-1.0 ms. (Table 2) were realized. These are small savings, however, especially when compared with the impact to the FEID program (expressed by FEID developers) to incorporate the priority/FIFO scheme evaluated. Because of this poor benefit/cost relationship, adoption of this scheme is not recommended.

RESULTS and RECOMMENDATIONS

SDL performance in the 2FC and MFC modes has been shown to be very sensitive to the current PDA2 I/F management scheme. Fortunately this sensitivity can be reduced through tuning and without costly FEID design changes. For example, maximum PDA2 I/F holdoff times can be reduced from the 1.9-14.8 ms. range to the 1.-3.3 ms. range just by setting non-priority data collection record size to 256 bytes. Also, during this study, SDL PDA2 I/F tuning capabilities, other than those already discussed, were suggested by SDL personnel. Based on these suggestions, the following Systems Analysis action is recommended to determine the most effective way to tune PDA2 I/F performance:

(1) As part of the MFC performance evaluation task currently in progress evaluate the effect of:

- turning off non-priority data collection record transfers at various times during the minor cycle (e.g., first 20 ms.; 10-20 ms. into each minor cycle)

- doing priority data collection in the Master FEID only (i.e., no slave FEID priority data collection).

(2) Compare/include the tuning results from step (1) with the data collection record sizing results from this study to determine exactly how the SDL should drive the PDA2 I/F to achieve the best priority record throughput.

The results of this additional PDA2 I/F analysis should be presented with other MFC performance information at the Release 6 DDR in November.

REFERENCES

(1) "PDA2 Contention Sensitivity Analysis - Initial Report" by R. Stephen Carter, dated August 8, 1975.

(2) "SDL FC Mode ALT Final Modeling Analysis - Initial Report" by Johnny E. Knight, dated April 7, 1975.

(3) Attachment C to "FSW Processing and I/O Profiles" by G. D. Carlow dated 1/7/75.

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APPENDIX A

PDA2 CONTENTION SENSITIVITY ANALYSIS BASIS/ASSUMPTIONS

(1) Systems Analysis' understanding of FEID PDA2 interface management scheme:*

- <u>2FC Mode</u> - At a four megacycle rate the interface management hardware will poll for PDA2 transfers in the following sequence:

Master FEID	Master FEID	Left Slave FEID	Master FEID	Master FEID	Left Slave FEID	Master FEID	Master FEID

- <u>MFC Mode</u> - At a four megacycle rate the interface management hardware will poll for PDA2 transfer in the following sequence:

Master FEID	Left Slave FEID	Master FEID	Right Slave FEID	Master FEID	Left Slave FEID	Master FEID	Right Slave FEID

(2) When a PDA2 transfer completes, polling for the next record to be transferred will resume at the point in the polling sequence where the last positive polling response was encountered.

(3) PDA2 data collection record priority is not considered in either of the schemes described.

(4) The flight computer/FEID combinations in the 2FC and MFC configurations modeled are assumed to be in synch with each other.

*Source: Phone conversations with Jim Allen of IBM Huntsville, 8/8/75.

SDL

FLIGHT COMPUTER MODE (ALT)

FINAL MODELING

ANALYSIS:

REAL TIME PROBLEM

INTERIM REPORT

September 30, 1975

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MANAGEMENT OVERVIEW

The system design changes recommended in the SDL FC Real Time Problem Report (Reference 3) have been evaluated. The Systems Analysis simulation model of the SDL was used as the basis of the analysis. Individually, none of these designs allow the Host to achieve real time response to Flight Computer (FC) commands and keep CPU utilization under the 85 percent target. However, one combination of these design changes as described in Appendix B, SDD will allow the SDL FC Mode to meet real time and keep CPU utilization under 85 percent. Specific results of this combination include:

- SDL average response time is 19.5 ms
- Average Host CPU utilization is 83.8 percent
- Host computer meets real time in every minor cycle.

As a result of the analysis the following recommendation is made:

- The SDL should adopt system design SDD because it supports real time with CPU utilization under 85 percent and minimizes impact to SDL design.

Since CPU utilization is approaching 85 percent and there is a need for sufficient CPU availability for growth and non-cyclic activity it is also recommended that:

- Additional analysis be conducted to bound the CPU required for non-cyclic activity and to estimate CPU growth for OFT
- A detailed review of model inputs and operation of SDL functions in Systems Analysis' SDL model be conducted.

PURPOSE AND SCOPE

The purpose of this modeling analysis is to evaluate the SDL system design changes discussed in Reference 3.

The scope of this analysis is limited to those system design changes recommended and not rejected by SDL developers and also limited to the FC Mode in the ALT environment.

OBJECTIVES AND ACCOMPLISHMENTS

The objective of this analysis effort was to evaluate the impact of the referenced SDL system design recommendations in the following areas:

- Host's ability to provide real time response to Flight Computer (FC) commands
- Average Host system CPU utilization
- SDL Response Time range and average.

The above objective has been achieved by analyzing data from computer simulation runs which were based on:

- Computer simulation model representing current SDL Host & FEID designs
- Driven by ALT I/O profile generated by Systems Analysis' simulation model of the functional ALT Flight Software Design as of 2/1/75 (Appendix C)
- SDL ALT Math Model execution sequence & measured processing times (math models & output calibration) supplied by SDL developers 4/14/75 (Appendix D)
- SDL ALT math model estimated processing times (resulting from changes in model requirements) supplied by developers 7/10/75 (Appendix E)
- Host-Host (PDA1) traffic profile provided by SDL personnel (Appendix F)
- Control program services supplied by Systems Analysis' simulation model of EOS

METHOD OF ANALYSIS

The method of this analysis was to develop a revised baseline model of the current SDL design with updates provide by SDL developers since SDL DDR 6/4/75. This was accomplished by upgrading Systems Analysis' SDL Model with logic & timing modifications and new math model processing estimates. The results of the baseline model was used as a basis when evaluating each of the specific system designs outlined in Reference 3.

RESULTS

A simulation run of the new baseline model shows 15 out of 25 minor cycles providing real time response to FC commands. The number of real time minor cycles was based on FSW's 15 ms requirement for transport lag time actually modeled. The average SDL response time was 24.6 ms as shown in Figure 1.

A summary of system design (SD1-SD12) evaluation results obtained using this new baseline model appears in Table 1 along with an explanation of designs not modeled. Design change effects on the baseline model results ranged from :

- 0.1 ms to 2.3 ms SDL response time improvements
- -0.8 ms to +1.9 ms per minor cycle CPU processing impact
- 0 to 10 additional real time minor cycles.

The important point, however, is that none of the system designs recommended (SD1-SD12) individually achieved real time response to FC commands and CPU utilization under 85 percent. Appendix A presents individual design evaluation results in detail and describes causes for CPU utilization and SDL response impacts reported.

Since no individual design change improved Host performance with the CPU utilization and response guidelines desired, combinations of design changes (SDA-SDD) were simulated (results presented in Table 1). Of the combinations simulated, only one (SDD) met the performance targets established.

This system design showed 83.8 percent CPU utilization, SDL response time of 19.5 ms and achieved real time response to FC commands in every minor cycle. The detailed results for this case are presented in Appendix B.

FIGURE 1

BASELINE CASE OF

CURRENT SDL DESIGN RESPONSE TIME BREAKDOWN

(TIMES IN MILLISECONDS)

TOTAL ELAPSED SDL RESPONSE TIME

RANGE	22.3 - 26.9			
AVERAGE	24.6			
	HOST STARTUP TIME[1]	PASS II MODEL EXECUTION	PASS I AND PASS II OUTPUT CALIBRATION	PDA[1] TRANSFER
	3.7 - 4.3	9.0	3.1 - 3.3	7.4 - 7.8
	4.0	9.0	3.1	7.5

SDL RESPONSE COMPLETE TIME (FROM START OF MINOR CYCLE):

RANGE: 38.3 - 43.6 AVERAGE: 41.2

NUMBER OF REAL TIME MINOR CYCLES* - 15

*NUMBER OF MINOR CYCLES PROVIDING REAL TIME RESPONSE TO FC COMMANDS WITH TRANSPORT LAG ≤ 15 MS.

[1] STARTS WHEN DATA COLLECTION OF EOML DATA HAS COMPLETED; AVERAGE FET=16.6MS (RANGE= 14.3-18.7MS)

SOURCE: SDL MODEL BASE CASE RUN 8/1/75

TABLE 1

SYSTEM DESIGN EVALUATION SUMMARY

	ITEM	NO. REAL* TIME MINOR CYCLES	AVERAGE PROCESSING PER MINOR CYCLE(MS)	AVERAGE CPU TIME IMPACT PER MINOR CYCLE(MS)	SDL RESPONSE TIMES(MS)	SDL RESPONSE IMPACT(MS)	AVERAGE CPU % ADJUSTED FOR REAL TIME	COMMENTS
	BASE CASE	15	32.4		24.6		81.0	
SD1	OVERLAP PDA1 WITH PASS II MODEL EXECUTION	20	34.3	+1.9	23.7	-0.9	85.8	INCREASE DUE TO EXTRA CALIBRATION AND I/O HANDLING (A)+
SD2	CALIBRATE PASS I MATH MODEL OUTPUT AFTER PASS I MODEL EXECUTION	22	32.7	+0.3	23.5	-1.1	81.8	INCREASE DUE TO EXTRA CALIBRATION (A)
SD3	TRANSFER OUTPUT (HEADER + DATA + FILLER) OF PASS I MODELS AFTER PASS I MODEL EXECUTION	25	34.3	+1.9	22.3	-2.3	85.8	INCREASE DUE TO EXTRA CALIBRATION AND I/O HANDLING (A)
SD4	ACCUMULATE 1024 BYTES OF NON-PRIORITY DATA PRIOR TO ISSUING SVC TO RTLOG	CURRENTLY IMPLEMENTED INTO SDL DESIGN & INCLUDED IN BASECASE						
SD5	USE MDM PROM WORDS AS A DIRECT INDEX			NOT MODELED				PROM IMAGE MUST BE USED PER M. GAMBLE
SD6	INPUT/OUTPUT CALIBRATION & MODEL DATA BASE REVISION	15	32.3	-0.1	24.5	-0.1	80.8	DECREASE DUE TO 2μs/ LOGICAL DEVICE SAVINGS. NO SAVING FOR OUTPUT CALIBRATION PER B. TAYLOR (A)

*NUMBER OF REAL TIME MINOR CYCLES MEETING REAL TIME RESPONSE TO FC COMMANDS WITH TRANSPORT LAG ≤ 15 MS.
+LETTERS IN PARENTHESES INDICATE THE APPENDIX WHICH CONTAINS DETAIL RESULTS OF SPECIFIC DESIGN.

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SYSTEM DESIGN EVALUATION SUMMARY (CONT.)

	ITEM	NO. REAL* TIME MINOR CYCLES	AVERAGE PROCESSING PER MINOR CYCLE (MS)	AVERAGE CPU TIME IMPACT PER MINOR CYCLE (MS)	SDL RESPONSE TIMES (MS)	SDL RESPONSE IMPACT (MS)	AVERAGE CPU % ADJUSTED FOR REAL TIME	COMMENTS
SD7	REVISE FEID (DECREASE BCW REQUIRED)			NOT MODELED				INFEASIBLE AT PRESENT PER M. GAMBLE
SD8	GROUP PARAMETERS FOR CALIBRATION BASED ON FSW READ FREQUENCY	22	31.6	-0.8	22.5	-2.1	79.0	DECREASE DUE TO LESS OUTPUT CALIBRATION PROCESSING (A)
SD9	REMOVE ERROR CHECK FROM FEID ACCESS METHOD	15	32.3	-0.1	24.5	-0.1	80.8	DECREASE DUE TO FEID ERROR CHECK PROCESSING REMOVED (A)
SD10	REVIEW CURRENT CALIBRATED OUTPUT			NOT MODELED				NO SIGNIFICANT IMPACT TO SDL, NOT FEASIBLE PER M. GAMBLE
SD11	EXECUTE MODELS AT FSW READ FREQUENCY			NOT MODELED				NEED TO MEET REAL TIME WITHOUT THIS DESIGN PER D. HORNER
SD12	EVALUATE CALCULATIONS BASED ON DEMAND RESPONSE INPUTS			NOT MODELED				DEMAND RESPONSE ACTIVITY NOT MODELED
SDA	CHANGE IN DATA COLLECTION BUFFER SIZES	22	32.7	+0.3	23.6	-1.0	81.8	INCREASE DUE TO PDA2 I/O HANDLING (B)
SDB	COMBINATION OF SD1-3 (NOT ADDITIVE)	25	35.9	+3.5	20.1	-4.5	89.8	INCREASE DUE TO EXTRA CALIBRATION AND I/O HANDLING (B)

SYSTEM DESIGN EVALUATION SUMMARY (CONT.)

	ITEM	NO. REAL* TIME MINOR CYCLES	AVERAGE PROCESSING PER MINOR CYCLE(MS)	AVERAGE CPU TIME IMPACT PER MINOR CYCLE(MS)	SDL RESPONSE TIMES(MS)	SDL RESPONSE IMPACT(MS)	AVERAGE CPU% ADJUSTED FOR REAL TIME	COMMENTS
SDC	COMBINATION OF SD6, SD8, SD9, SDA, SDB	25	34.9	+2.5	17.3	-7.3	87.3	INCREASE DUE TO EXTRA CALIBRATION AND I/O HANDLING (B)
SDD	COMBINATION OF SD3, SD6, SD8, SD9, SDA	25	33.5	+1.0	19.5	-5.1	83.8	INCREASE DUE TO EXTRA OUTPUT CALIBRATION AND I/O HANDLING (B)

RECOMMENDATIONS AND CONCLUSIONS

Based on analysis of simulation results the following conclusions are made:

- Host response time can be improved to support real time by:
  - more overlap of CPU with PDA1 I/O
  - grouping parameters for calibration based on FSW read frequency
  - transferring of data and buffer control words at different times over PDA1.
- The magnitudes of the CPU utilization and SDL response time results presented are I/O Profile dependent but the direction of saving achievable is not I/O Profile dependent.

There is at least one Host processing sequence that can support real time with CPU utilization under 85 percent. Adoption of this system design (SDD) is recommended to the SDL because:

- Less impact to SDL design
  - No break-up of Pass II models
  - Output calibration and PDA1 transfers remain the same, operating one after the other.

Since CPU utilization is approaching 85 percent and there exists a need for sufficient CPU availability for growth and non-cyclic activity it is also recommended that:

- Additional analysis of FC mode be done to bound the CPU required for non-cyclic activity and the estimated OFT growth
- A detailed review be done of model inputs which include processing estimates and measured time and operation of SDL functions, e.g., output calibration routine, in Systems Analysis' SDL model.

SCHEDULE

The system designs accepted by SDL 10/2/75 and to be implemented into the SDL design are:

- SD1 - Implies the following change to SDL response time

  Host startup (Input calibration + PDA2 transfer)
  Pass II model execution (NLA, ACS, AER, EOM & RGA)
  Calibration of Pass II data
  PDA1 transfer of Pass II data and BCW's
  Pass III model execution (IMU)
  Calibration of Pass III data
  PDA1 transfer of Pass III data and Pass I & III BCW's

- SD2 - Calibrate Pass 1 data after Pass I model execution

- SD8 - Calibrate model data based on FSW read frequency.

- SDA - Data collection buffer size change; 128 bytes for Priority and 1024 bytes for Non Priority.

To complete this modeling analysis the following milestones have been identified:

Milestones	Completion Dates
Upgrade SDL model to new design	10/8/75
Analysis of FC commanding all busses	10/15/75
Analysis of FC ALT new design	10/17/75
Final Report	10/27/75
Parameter Table Update	10/27/75

REFERENCES

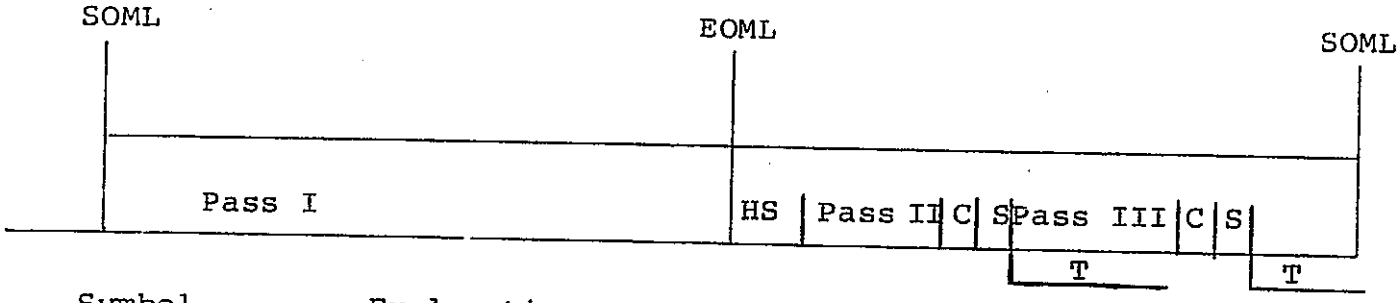
1. Memo to K. J. Davidson from J. E. Knight, April 7, 1975 "SDL FC Mode ALT Final Modeling Analysis - Initial Report."

2. Memo to K. J. Davidson from J. E. Knight, June 11, 1975, "SDL FC Mode ALT Final Modeling Analysis - Final Report."

3. Memo to J. R. Gililland from T. L. Anderson and W. C. Bridges, July 16, 1975, "SDL FC Mode Real Time Problem."

APPENDIX A

DETAIL RESULTS OF SYSTEM DESIGN 1



Symbol	Explanation	Average Response Time (in milliseconds)
Pass I	Pass I model execution	14.0
HS	Host startup time (Input calibration + PDA2 transfer)	4.0
Pass II	NLA, ACS, AER, EOM, RGA model execution	4.6
C	Calibrate Pass I & II model data	2.2
S, T	Start I/O and transfer calibrated data	3.4
Pass III	IMU model execution	4.4
C	Calibrate IMU model data	1.0
S, T	Start I/O and transfer calibrated data + all BCW's	4.4

Number of adjusted real time minor cycles (MC)	20 mc
Number of real time minor cycles observed	11 mc
CPU processing per minor cycle	34.3
CPU processing time impact	+1.9*
SDL Response time	23.7
SDL Response time impact	-0.9+
Average CPU % adjusted for real time	85.8%

*Increase due to extra output calibration and I/O handling
+Decrease due to overlapped I/O and CPU

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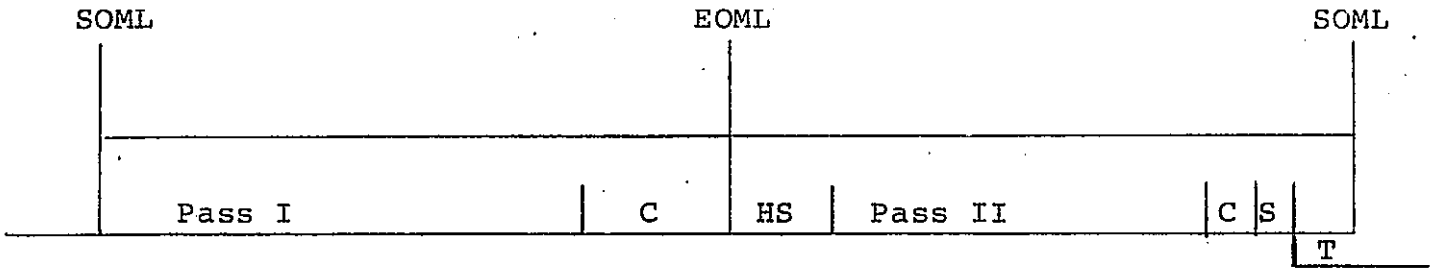
APPENDIX A

DETAIL RESULTS OF SYSTEM DESIGN 2



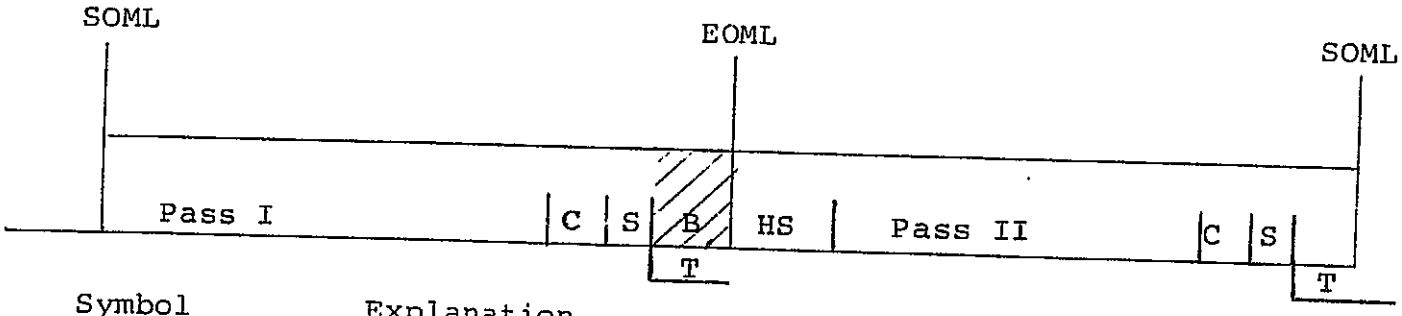
Symbol	Explanation	Average Response Time (in milliseconds)
Pass I	Pass I model execution	14.0
C	Calibrate Pass I model data	1.2
HS	Host startup time (Input calibration + PDA2 transfer)	4.0
Pass II	Pass II model execution	9.0
C	Calibrate Pass II model data	2.0
S, T	Start I/O and transfer calibrated data + all BCW's	7.5

Number of adjusted real time minor cycles (MC)	22 mc
Number of real time minor cycles observed	12 mc
CPU processing per minor cycle	32.7
CPU processing time impact	+0.3*
SDL Response time	23.5
SDL Response time impact	-1.1+
Average CPU % adjusted for real time	81.8%

*Increase due to extra AMOD processing during output calibration
+Decrease due to less items calibrated during SDL response time

APPENDIX A

DETAIL RESULTS OF SYSTEM DESIGN 3



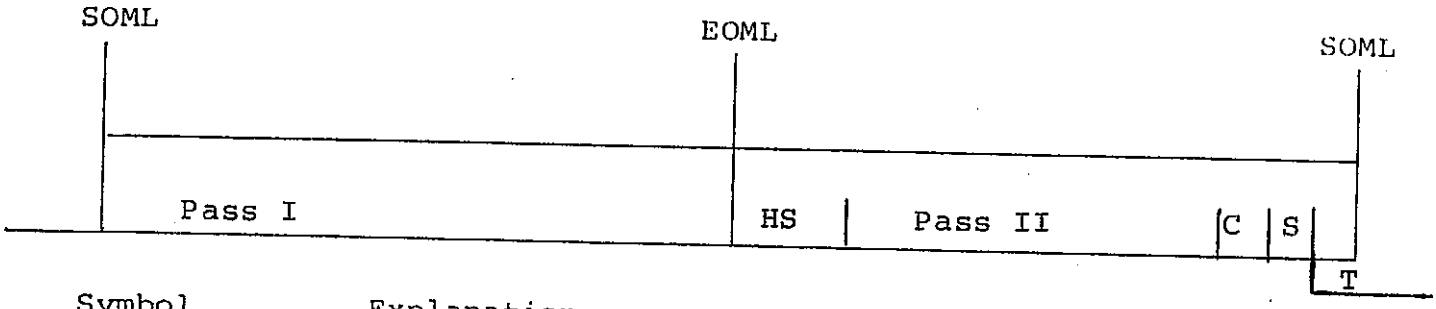
Symbol	Explanation	Average Response Time (in milliseconds)
Pass I	Pass I model execution	14.0
C	Calibrate Pass I model data	1.2
S, T	Start I/O and transfer calibrated data	2.0
B	Background processing	-
HS	Host startup time (Input calibration + PDA2 transfer)	4.0
Pass II	Pass II model execution	9.0
C	Calibrate Pass II model data	2.0
S, T	Start I/O and transfer calibrated data + all BCW's	6.0

Number of adjusted real time minor cycles (MC)	25 mc
Number of real time minor cycles observed	17 mc
CPU processing per minor cycle	34.3
CPU processing time impact	+1.9*
SDL Response time	22.3
SDL Response time impact	-2.3+
Average CPU % adjusted for real time	85.8%

*Increase due to extra output calibration and I/O handling.
+Decrease due to less items calibrated and transferred during SDL response time.

APPENDIX A

DETAIL RESULTS OF SYSTEM DESIGN 6



Symbol	Explanation	Average Response Time (in milliseconds)
Pass I	Pass I model execution	14.0
HS	Host startup time (Input calibration + PDA2 transfer)	3.9
Pass II	Pass II model execution	9.0
C	Calibrate Pass I & II model data	3.1
S, T	Start I/O and transfer calibrated data + BCW's	7.5

Number of adjusted real time minor cycles (MC)	15 mc
Number of real time minor cycles observed	7 mc
CPU processing per minor cycle	32.3
CPU processing time impact	-0.1*
SDL Response time	24.5
SDL Response time impact	-0.1+
Average CPU % adjusted for real time	80.8%

*Decrease due to the 2μs/logical device less processing required during input calibration processing time.
+Decrease results from less processing time during input calibration

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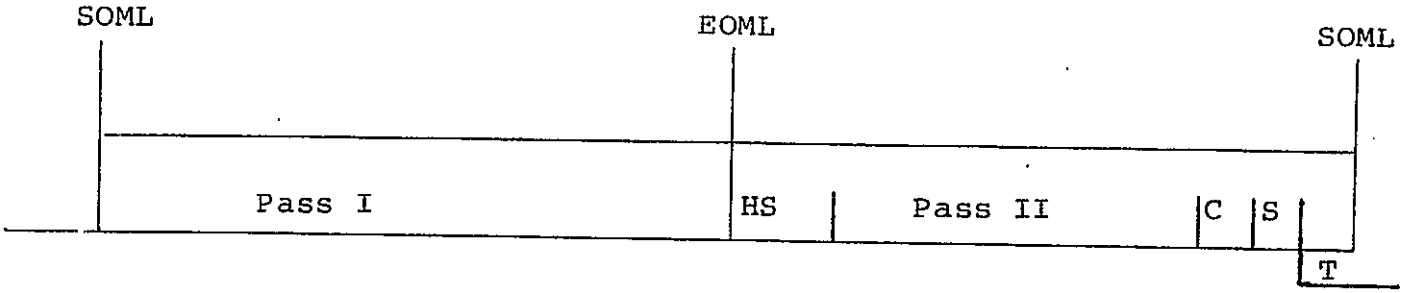
APPENDIX A

DETAIL RESULTS OF SYSTEM DESIGN 8



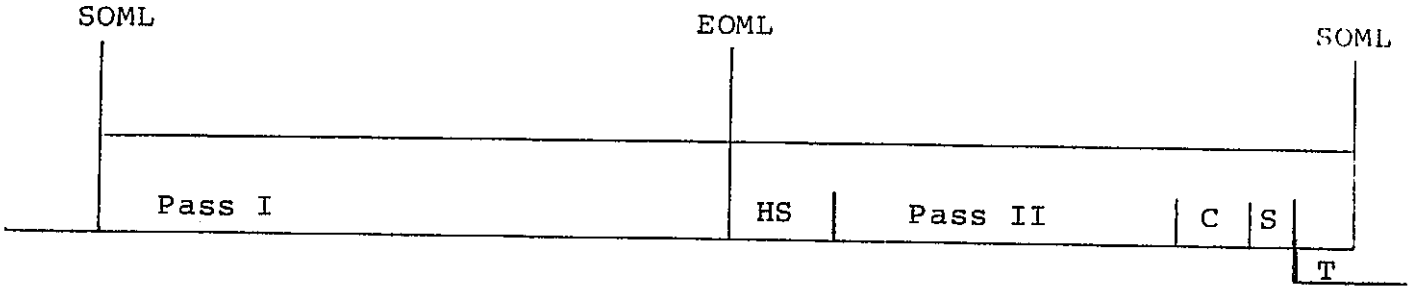
Symbol	Explanation	Average Response Time (in milliseconds)
Pass I	Pass I model execution	14.0
HS	Host startup time (Input calibration + PDA2 transfer	4.0
Pass II	Pass II model execution	9.0
C	Calibrate Pass I & II model data at 12.5 hz for ADS, IMU, TAC, RAD and MLS at 5 hz.	2.1
S, T	Start I/O and transfer calibrated data + BCW's	6.2

Number of adjusted real time minor cycles (MC)	22 mc
Number of real time minor cycles observed	18 mc
CPU processing per minor cycle	31.6
CPU processing time impact	-0.8*
SDL Response time	22.5
SDL Response time impact	-2.1+
Average CPU % adjusted for real time	79.0%

*Decrease due to the reduction of data items output calibrated which varies from 43 to 141 data items.
+Decrease results from less data items output calibrated

APPENDIX A

DETAIL RESULTS OF SYSTEM DESIGN 9



Symbol	Explanation	Average Response Time (in milliseconds)
Pass I	Pass I model execution	14.0
HS	Host startup time (Input calibration + PDA2 transfer	4.0
Pass II	Pass II model execution	9.0
C	Calibrate Pass I & II model data	3.1
S, T	Start I/O and transfer calibrated data + BCW	7.5

Number of adjusted real time minor cycles (MC)	15 mc
Number of real time minor cycles observed	7 mc
CPU processing per minor cycle	32.3
CPU processing time impact	-0.1*
SDL Response time	24.5
SDL Response time impact	-0.1+
Average CPU % adjusted for real time	80.8%

*Decrease due to not executing FEID Access Method error check.
+Decrease results from less processing during PDA1 transfers.

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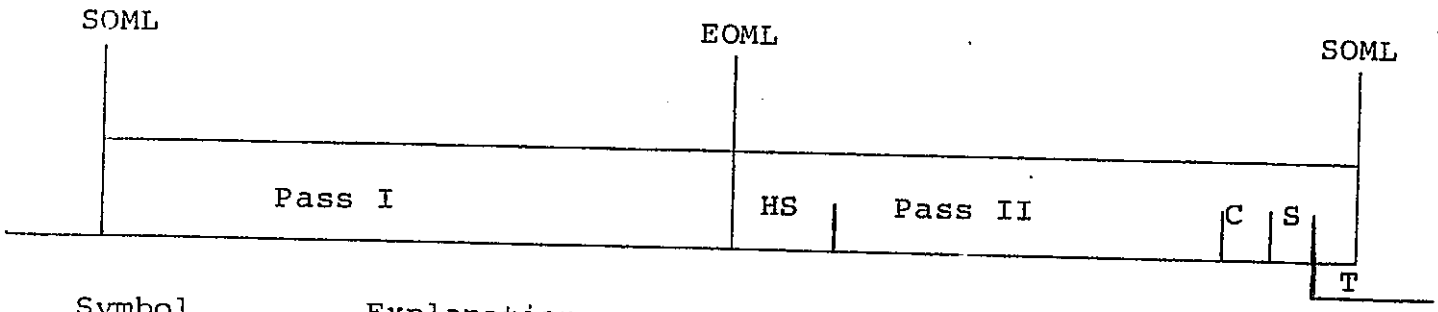
APPENDIX B

DETAIL RESULTS OF SYSTEM DESIGN A (buffer sizes)



Symbol	Explanation	Average Response Time (in milliseconds)
Pass I	Pass I model execution	14.0
HS	Host startup time (Input calibration + PDA2 transfer)	2.8
Pass II	Pass II model execution	9.0
C	Calibration Pass I & II model data	3.1
S	Start I/O and transfer calibration data + BCW	7.5

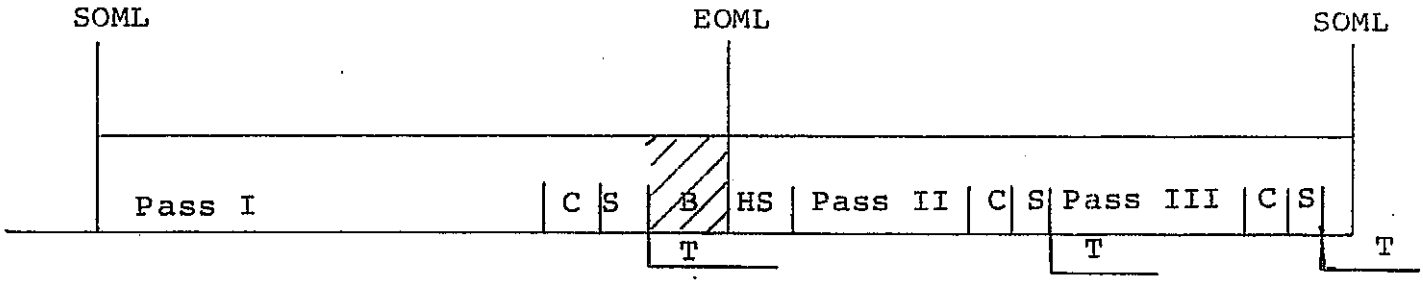
Number of adjusted real time minor cycles (MC)	22 mc
Number of real time minor cycles observed	10 mc
CPU processing per minor cycle	32.7
CPU processing time impact	+0.3*
SDL Response time	23.6
SDL Response time impact	-1.0+
Average CPU % adjusted for real time	81.8%

*Increase due to I/O handling during PDA2 data collection buffers. (Two 64 halfword buffers filled per minor cycle in this design instead of one 256 halfword buffer during base case). Overlapping savings resulting from less SVC's to RTLOG.

+Decrease results from overlapping PDA2 I/O with input calibration processing and less transfer time because first transfer is completed 50% of the time before EOML is data collected.

APPENDIX B

DETAIL RESULTS OF SYSTEM DESIGN B(SD1-3)



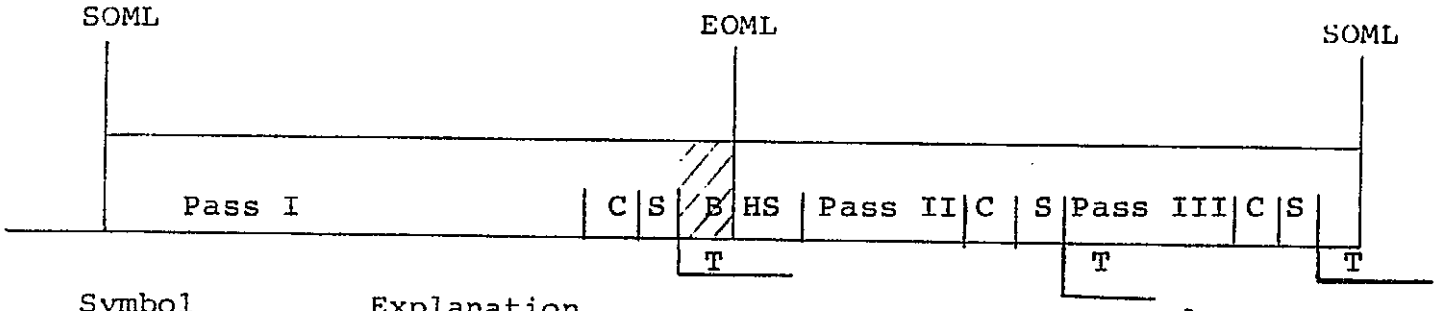
Symbol	Explanation	Average Response Time (in milliseconds)
Pass I	Pass I model execution	14.0
C	Calibrate Pass I model data	1.2
S, T	Start I/O and transfer calibrated data	2.0
B	Background processing	NA
HS	Host startup time (Input calibration + PDA2 transfer)	4.0
Pass II	NLA, ACS, AER, EOM, RGA model execution	4.6
C	Calibrate Pass II model data	1.0
S, T	Start I/O and transfer calibrated data + BCW's for Pass II models	4.4
Pass III	IMU model execution	4.4
C	Calibrate IMU model data	1.0
S, T	Start I/O and transfer calibrated data + rest of BCW's	2.0

Number of adjusted real time minor cycles (MC)	NA
Number of real time minor cycles observed	25 MC
CPU processing per minor cycle	35.9
CPU processing time impact	+3.5*
SDL Response time	20.1
SDL Response time impact	-4.5+
Average CPU % adjusted for real time	89.8%

*Increase due to two extra output calibration and I/O handling
+Decrease due to less data calibrated and transferred during SDL response time and overlapped I/O and CPU.

APPENDIX B

DETAIL RESULTS OF SYSTEM DESIGN C(SD6, 8, 9, A, B)



Symbol	Explanation	Average Response Time (in milliseconds)
Pass I	Pass I model execution	14.0
C	Calibrate Pass I model data	0.6
S, T	Start I/O and transfer calibrated data	1.1
B	Background processing	NA
HS	Host startup (Input calibration + PDA2 transfer)	2.8
Pass II	NLA, ACS, AER, EOM, RGA model execution	4.6
C	Calibrate Pass II model data	1.0
S, T	Start I/O and transfer calibrated data + Pass II BCW;s	4.4
Pass III	IMU model execution	4.4
C	Calibrate Pass III model data	0.5
S, T	Start I/O and transfer calibrated data + rest of BCW's	1.0

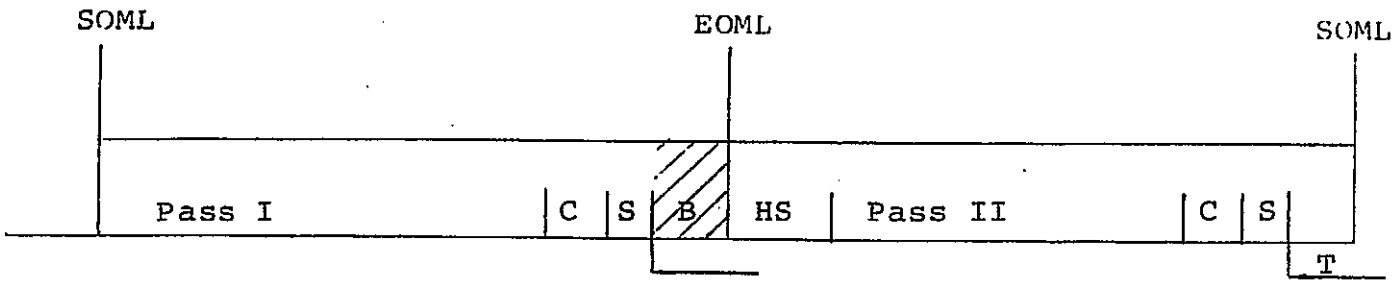
Number of adjusted real time minor cycles (MC)	NA
Number of real time minor cycles observed	25 mc
CPU processing per minor cycle	34.9
CPU processing time impact	+2.5*
SDL Response time	17.3
SDL Response time impact	-7.3+
Average CPU % adjusted for real time	87.3%

*Increase due to extra output calibration, I/O handling and SDA overlapping saving resulting from SD6, 8 and 9

+Decrease results from SD6, 8, 9, A & B.

APPENDIX B

DETAIL RESULTS OF SYSTEM DESIGN D(SD3, 6, 8, 9, A)



Symbol	Explanation	Average Response Time (in milliseconds)
Pass I	Pass I model execution	14.0
C	Calibrate Pass I model data at 12.5 hz for IMU, TAC, ADS and RAD and 5 hz for MLS	0.6
S, T	Start I/O and transfer calibrated data	1.1
B	Background processing	-
HS	Host startup time (Input calibration+PDA2 transfer)	2.8
Pass II	Pass II model execution	9.0
C	Calibrate Pass II model data 12.5 hz for IMU	1.5
S, T	Start I/O and transfer calibrated data + all BCW	5.2

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Number of adjusted real time minor cycles (MC)	25 mc
Number of real time minor cycles observed	23 mc
CPU processing per minor cycle	33.5
CPU processing time impact	+1.0*
SDL Response time	19.5
SDL Response time impact	-5.1+
Average CPU % adjusted for real time	83.8

*Increase due to extra calibration and I/O handling overlapping savings resulting from SD6, 9 and 8
+Decrease results from SD3, 6, 8, 9, A

I/O Definitions For GNC Mated Flight, Sep., TAEM, A/L Major Modes

	WORDS/ MDM	TOTAL WORDS	RATE	MDM's	BCE's
INPUT GROUP 1					
Accel Assembly	2	6	25	FF1-3	10-12
RH RHC	3	9	25	FF1-3	10-12
RH RPTA	1	3	25	FF1-3	10-12
RH SBTC	1	3	25	FF1-3	10-12
LH RHC	3	9	25	FF1-3	10-12
LH RPTA	1	3	25	FF1-3	10-12
LH SBTC	1	3	25	FF1-3	10-12
FF1 Discretes	7	7	25	FF1	10
FF2 Discretes	6	6	25	FF2	11
FF3 Discretes	7	7	25	FF3	12
FF4 Discretes	5	5	25	FF4	13
INPUT GROUP 2					
Rate Gyro Assembly	3	9	25	FA1-3	14-16
Actuator Feedback	7	28	25	FA1-4	14-17
FA1 Discretes	2	2	25	FA1	14
FA2 Discretes	2	2	25	FA2	15
FA3 Discretes	2	2	25	FA3	16
FA4 Discretes	1	1	25	FA4	17
Aft Attach Pt. Volt.	2	4	25	FA1,FA2	14,15
APU Pressures	1	3	25	FA1-3	14-16
INPUT GROUP 3					
Fwd. Attach Pt. Volt.	1	2	12.5	FF1,FF2	10,11
ADTA	7	28	12.5	FF1-4	10-13
IMU	14	42	12.5	FF1-3	10-12
MSBLS	3	9	12.5	FF1-3	10-12
TACAN	4	12	12.5	FF1-3	10-12
TACAN Control Reg.	2	6	12.5	FF1-3	10-12
Radar Altimeter (Time Tag)	1	2	12.5	FF1,FF2	10,11

Source: ALT FSW Preliminary Design Review 3/10/75

I/O Definition For GNC (Cont'd.)

	WORDS/ MDM	TOTAL WORD	RATE	MDM's	BCE's
OUTPUT GROUP 1					
ASA Commands	6	24	25	FA1-4	14-17
F A1 Discretes	4	4	25	FA1	14
FA2 Discretes	4	4	25	FA2	15
FA3 Discretes	4	4	25	FA3	16
FA4 Discretes	2	2	25	FA4	17
OUTPUT GROUP 2					
FF1 Discretes	8	8	12.5	FF1	10
FF2 Discretes	8	8	12.5	FF2	11
FF3 Discretes	8	8	12.5	FF3	12
FF4 Discretes	4	4	12.5	FF4	13
SPI	1	1	12.5	FF1	10
TACAN Control Reg.	2	6	12.5	FF1-3	10-12
IMU Torque & Slew	2	6	12.5	FF1-3	10-12
OUTPUT GROUP 3					
Dedicated Display #1	37	111	12.5	DDU 1	10,11,13
Dedicated Display #2	37	111	12.5	DDU 2	10-12

A/L I/O Definitions For SM And UI

	Read/ Write	Words/ Device	Total Words	Rate	Exec Cycles	Device BCE
DOWNLIST PROCESSOR						
Downlist Buffer	W	128	128	25	1-25	DACBU 24
DEU POLLING						
DEU1 Poll	R	1	1	5	1-5	DEU1 6
DEU2 Poll	R	1	1	5	1-5	DEU2 7
DEU3 Poll	R	1	1	5	1-5	DEU3 8
SM DATA ACQUISITION						
Obtain Data	R	37	37	7	1-10	DACBU1 24
Obtain Status Byte	R	1	1	1	5	DACBU1 24
DISPLAY UPDATE						
Final Approach Display	W	25	25	10	1-10	DEU1 6
System Summary Display	W	282	282	1	2	DEU 2 7
RM-CONT Display	W	347	347	1	3	DEU3 8

APPENDIX D

ALT HOST MATH MODEL CHARACTERISTICS

MODULE	MODEL	CYCLE # (1-25)	MEASURED CPU/EXEC. (MS)	EXECUTION PHASE	MEASURED PROGRAM SIZE
SMDLGACS	ACS	ALL	2.200	II	6K
SMDLENV2	AER(2)	ALL	1.260	II	2K
	EOM(2)	ALL	.890	II	3.5K
SMDLGSEN	IMU(2)	ALL	4.800	II	7K
	RGA	ALL	.610	II	0.5K
	NLA	ALL	.720	II	1.0K
SMDLXDDM	DDM	ALL	.250	I	1.0K
	DDS	EVEN	.600	I	1.0K
SMDLGLDS	LDS	ALL	.270	I	1.0K
SMDLENV1	EOM(1)	ALL	.550	I	1.0K
	ERV1	ALL	1.830	I	1.0K
	ATM	ALL	.620	I	1.0K
	WND	ALL	2.000	I	1.0K
	GRA	ALL	.660	I	1.0K
	LND	ALL	3.830	I	-
	AER(1)	ALL	8.800 1ST MC .520 2-25TH MC	I	2.0K
SMDLGNAV	TAC	ALL	2.160	I	2.5K
	MLS	3,8,13, 18,13,	.900	I	2.5K
	RAD	ALL	.600	I	1.5K
	IMU(1)	ALL	.950	I	1.5K
	ADS	ALL	.830	I	1.5K
SMDLSPMU	PMU	ALL	.500	I	-
SMDLRCLK	-	ALL		I	.1K

SOURCE: SDL DEVELOPMENT PERSONNEL, 4/14/75

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APPENDIX E

ALT HOST MATH MODEL CHARACTERISTICS

MODULE NAME	MODEL NAME	CYCLE NO. 1-25	ESTIMATED CPU/EXEC (MS)
SMDLGACS	ACS	ALL	1.881
SMDLENV2	AER(2)	ALL	1.260
	EOM(2)	ALL	.890
SMDLGSEN	IMU(2)	ALL	4.400
	RGA	ALL	.110
	NLA	ALL	.420
SMDLXDDM	DDM	ALL	.250
	DDS	EVEN	.600
SMDLGLDS	LDS	ALL	.270
SMDLENV1	EOM(1)	ALL	.550
	ERV1	ALL	1.430
	AFP	ALL	.700
	PER	1,4,7,10,13,16,19,22,25	1.300
	ATM	2,5,8,11,14,17,20,23	.620
	GRA	3,6,9,12,15,18,21,24	.660
	LND	ALL	3.830
	AER1	ALL	8.600, 320+
SMDLGNAV	TAC	ALL	1.360
	MLS	3,8,13,18,23	.900
	RAD	ALL	.600
	IMU(1)	ALL	.950
	ADS	ALL	.830
SMDLSPMU	PMU	ALL	.500
SMDLRCLK	-	ALL	-

+FIRST TIME REPRESENTS MODEL EXEC TIME FOR 1ST MINOR CYCLE
SECOND TIME REPRESENTS MODEL EXEC TIME FOR 2ND-25TH MINOR CYCLES

SOURCES: SDL PERSONNEL 7/10/75

APPENDIX F

ALT HOST-TO-FEID PDA1 TRAFFIC PROFILE MODELED

LOAD MODULE/ PARAMETERS	NUMBER OF WORDS (16-BIT) CALIBRATED	TOTAL OUT[1]	CYCLES OUTPUT (ALL = 1 THRU 25)
PHASE II MODELS			
SMDLGACS/			
ACS FDBK. SIG.	28	152	ALL
ACS DISC. SIG.	0	22	ALL
SMDLENV2/-	NONE	NONE	N/A
SMDLGSEN/			
IMU(2)	42	60	ALL
RGA	9	60	ALL
NLA	6	48	ALL
RGA DISC.	0	30	ALL
PHASE I MODELS			
SMDLGLDS/LDS	NONE	NONE	N/A
SMDLENV1/-	NONE	NONE	N/A
SMDLGNAV/			
TAC	15	48	ALL
MLS	9	30	3,8,13,18,23
RAD	4	32	ALL
ADS	28	56	ALL
NAV DISC.	INCLUDED WITH CSB DISCRETES		N/A
CSB DISC.	0	54	DEMAND RESPONSE
MAN CONTROL	30	62	DEMAND RESPONSE
EDS	2	6	DEMAND RESPONSE
SMDLSPMU/PMU	0	42	ALL

SOURCE: SDL PERSONNEL 3/75

[1] INCLUDES FILL, HEADER, & FEID BUFFER CONTROL WORDS