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Produced by the NASA Center for Aerospace Information (CASI)
FINAL REPORT

DIGITAL DATA PROCESSING SYSTEM

DYNAMIC LOADING ANALYSIS

30 APRIL 1976

J. J. Lagas
J. J. Peterka
A. E. Tucker

This document has not been cleared for open publication.
This Final Report provides the results of a 10-month study by System Development Corporation (SDC) that involved the simulation and analysis of the Space Shuttle Orbiter Digital Data Processing System (DDPS). This Dynamic Loading Analysis was performed for the NASA Johnson Space Center under contract NAS9-14630. The Mated Flight and Postseparation Flight phases of the Space Shuttle's Approach and Landing Test (ALT) configuration were modeled utilizing the Information Management System Interpretative Model (IMSIM) in a computerized simulation modeling of the ALT hardware, software, and workload.

System Requirements simulated for the ALT configuration were defined. Sensitivity analyses determined areas of potential data flow problems in DDPS operation. Based on the defined system requirements and the sensitivity analyses, a test design is described for adapting, parameterizing, and executing the IMSIM. Varying load and stress conditions for the model execution are given. The analyses of the computer simulation runs were documented as results, conclusions, and recommendations for DDPS improvements.
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1. SUMMARY

This report summarizes the results of a simulation analysis of the Space Shuttle Orbiter Digital Data Processing System. This study was performed for the Avionics Integration Branch of the Avionics Systems Engineering Directorate for NASA's Johnson Space Center. The study was conducted by members of the Systems Analysis Center of the Satellite Control Program of System Development Corporation under contract NAS9-14630, and was performed during the period of 24 June 1975 through 30 April 1976.

NASA Technical Monitor has been Mr. Carroll T. Dawson of the JSC Avionics Integration Branch. Under Mr. Dawson's direction, SDC has performed an extensive simulation modeling analysis utilizing IMSIM of the Approach and Landing Test (ALT) configuration, with total emphasis on the related impact on the orbiter's Digital Data Processing System (DDPS). SDC personnel involved in this study and primary responsibilities were:

Richard W. Bilek - Head, Systems Analysis Center: overall project supervision and quality assurance
Jacobus J. Lagas - Project Manager: requirements definition, test design, execution, and analysis.
James J. Peterka - model adaptation, execution, and analysis
Alfred E. Tucker - requirements definition, sensitivity analysis, and model parameterization.

1.1 OBJECTIVES

As the end product of this contract, this report constitutes a detailed analysis of the DDPS, and identifies constituents of the system which are potentially subject to overload under stress and which may significantly degrade performance of the system in critical situations. The analysis is based on a quantitative representation of the DDPS as a discrete simulation model and on the results derived from the operation of this model. This report also includes a qualitative study of the system organization and structure to determine the adaptability of the system to varying loads and requirements. This information was used to parameterize the model and was instrumental in completing the analyses.

1.2 DATA SOURCES

Sources for the study included current documentation of the DDPS/ALT functional requirements and detailed design specifications as listed in Appendix F. Upon NASA direction, the study was primarily confined to the hardware and software which may be employed during the airborne and flight phases of the ALT. These efforts were applied to investigation of characteristics and activities which are discernible to a time resolution of one millisecond; i.e., items
such as control signals, IOP memory access for commands, parity checking, and CPU instruction execution were considered only insofar as collective effects are concerned. The effort was focused on quantitative data processing aspects of the DDPS, i.e., data flow, throughput, response, etc., rather than upon planned information content or quality, reliability, human engineering, or other more qualitative aspects.

Level A Hardware specifications and the Functional Subsystem Software Requirements (FSSR) System Interface document were used to determine the DDPS ALT configuration and the nature of the components to be connected to the GPCs via data buses for communication and control. These sources also provided information on the processing rates of the CPUs, capacities for data retention by terminal elements such as displays, transmission rates for components and data buses, and sizing of message transmissions. Documents pertaining to the Central Processing Units (CPUs) and Input-Output Processors (IOPs) functional descriptions and principles of operation were consulted to gain an understanding of the functioning of these modules.

Level A Software specifications, requirements for ALT Guidance, Navigation, and Control (GN&C) and System Management (SM) plus functional design specifications for ALT GN&C, SM, and Systems Software were used to determine the structure of the DDPS software. Significant program modules to be executed in these simulations were also determined from these documents. For each of these program modules, characteristics were determined with regard to the conditions for executing the module, the impact of the current system status on the execution time of the module, the effect that execution of the module has on the system status, and the data transmissions performed by the module. This information was used to compile a set of system states for the DDPS which were principal factors in determining system loading.

1.3 MODEL DEVELOPMENT

The information which was derived from study of the source documents as described in section 1.2 was used to adapt and parameterize a discrete event simulation model of the DDPS. The basic model is a computer program simulator for information management simulation, denoted as "IMSIM" (Information Management System Interpretive Model). This program was originally developed by SDC under contract to NASA to provide methods and capabilities for performing dynamic loading studies of computer-based data processing systems, and has been well suited to the simulation of the Shuttle Orbiter DDPS. IMSIM is described in detail in the IMSIM User's Manual (Reference 2), and summarized in Section 5.1.3.

Hardware characteristics of each component of the DDPS were transcribed to IMSIM input specification forms, and configuration specification forms were used to specify the connection of terminal elements and memory units to data buses. The DDPS components so represented are the Display Electronic Units, Display Units, Multiplexer/Demultiplexers, Display Driver Units, Keyboard Units, PCM/MUs, and the memory units and CPUs of the GPCs. The data buses themselves are represented as IMSIM "datalinks" in the model (see Appendix B).
Depiction of the software for simulation is somewhat more complex than the hardware representation. It is necessary to exercise value judgement in deciding whether a program module is to be individually represented, combined with other modules for collective representation, or excluded from the model. Modules such as the Rate Gyro FDIR, require significant time for execution, but involve no change in system state which would affect loading. On the other hand, modules such as control segments, cause a significant change of state when executed but involve only inconsequential execution time. Some modules are called by several other modules, while others are called by only one.

Software is described for IMSIM in terms of schedulable "tasks", loadable "routines", mathematical expressions or tables which yield execution time as a function of the model state, and logic sequences which manipulate the system state. It was necessary to map the salient software characteristics of the DDPS into IMSIM counterparts so as to retain a meaningful correspondence between system and model constituents, while conforming to the rules and constraints imposed by IMSIM. (It should be noted that this problem is common to all modeling processes, regardless of the tools used, since a model is normally intended to be only a suitable approximation of an actual system.)

Scheduled processes such as SPECS, OPS, and cyclic executives were designated as IMSIM tasks, and logic sequences were developed to schedule them as a function of the simulated clock, externally introduced events, or the simulated system state (e.g., mode or pending keyboard request). Program modules which are executed for a specific task, or for a specific set of tasks, were collectively described as "routines". For each routine, a mathematical algorithm was prepared which indicates the amount of computation to be simulated when a task which employs the routine is activated, as a function of the system state at the time of activation. More than one routine may be employed in performance of a task. For each DDPS program module which significantly alters the system state when executing, a similar change was programmed into IMSIM as a logic sequence, and was synchronized for concurrent execution with the appropriate task.

Sizing of program modules was not a significant factor for the model, since dynamic memory allocation and loading are not characteristics of the ALT, and they therefore have no impact on system loading.

Data transmission within the DDPS is described to IMSIM in terms of "messages". A message can define a set of transmissions, whether parallel or sequential, and with varying origins and destinations. All transmissions simulated for the DDPS are between the memory of a GPC and some other unit (e.g. a MDM or PCMMU, or even another GPC memory in the case of intercomputer communication). Similar transmissions such as reading of data from the three IMUs, are described by a single message which represents concurrent transmissions from FFO1, FFO2, and FFO3 (see Appendix E for abbreviations) to the GPC memory. Messages are associated with tasks and are synchronized to task performance; e.g., if performance of a task is deferred or interrupted for higher priority processing, its associated transmissions may be delayed (but not interrupted).
The general rules used to specify transmission lengths and execution periods are (a) maximum transmission lengths, (b) biased random execution of alternate or optional program sequences, and (c) 130% of estimated average periods for sequences for which precise timing figures were not available.

1.4 APPLIED WORKLOADS

The workload specification for the DDPS model is actually an integral part of the software representation, but it must be activated and controlled by an event schedule which effectively specifies parametric values for the simulated software. Various event schedules were prepared to represent segments of the ALT airborne and flight phases. Each schedule was designed to provide a realistic sequence of events with the additional objective of causing maximum stress during a critical time period. The event schedules were developed and modified in the course of the iterative process of dynamic simulation and analysis of results.

1.5 DYNAMIC SIMULATION

SDC initially performed a series of computer runs with the DDPS model for validation and verification against predicted performance under unsophisticated loading. Subsequently, a series of "production" runs was conducted with sophisticated stress loading. The automatic monitoring and data reduction facilities of IMSIM were augmented with special software probes and reports to obtain the maximum of useful information from the runs, and to simplify extrapolation of results to predicted performance of the DDPS. IMSIM is a discrete event simulator and generally functions in a deterministic mode, although random behavior can be simulated by drawing pseudorandom numbers from built-in number generators. Randomness was incorporated in the delivery of calculated execution times for some routines and is discussed in paragraph 5.2.4.2.

One major simplification of DDPS simulation was introduced for most of the computer runs. Since the GPCs of the DDPS are all organized as a redundant set for the ALT, they must necessarily perform identical functions in close synchronization. In fact, the GPCs are precisely synchronized in the model unless a perturbation is explicitly introduced. Thus, no additional information is obtained from simulating the functions of four GPCs in a redundant configuration as opposed to a single GPC insofar as processor loading is concerned. Since simulation of parallel computations must be performed serially on a simplex computer, it is both cost-effective and efficient to eliminate the redundancy in the model. Note that intercomputer communication is still simulated among the four GPCs in order to achieve a realistic load on the ICC data buses and to properly represent ICC activity for the single GPC. Some runs were made with the four GPCs simulated as four active, separate virtual machines, to verify the above.
Data produced from each simulation run include a history of the important events and activities, a summary of the final state of the model, and statistics on resource utilization and software functions. Snapshots were often taken of the dynamic state of the model in order to investigate stress situations in more detail.

1.6 SIMULATION ANALYSIS

Results of simulation runs were analyzed to determine how the simulated DDPS performed under specified workloads and what workload variations should be considered for subsequent runs. The data from history outputs (see Appendix C) provide specific information on task contention for resources and the maximum interference in performing each type of task. The history output also provides valuable insight regarding patterns of behavior in DDPS operation and situations of peak strain. The summary results (see Appendix D) provide information on backlogging of tasks for CPU service, delays incurred in performing I/O, system component utilization, and statistics on contention for resources. System status information yielded clues as to potential system behavior under different conditions, which could then be imposed for subsequent simulation runs. In consequence, data were accumulated from the series of runs which describe the DDPS model behavior and performance under a variety of stress situations. Subject to the conditions and assumptions detailed in Section 5, SDC is confident that the model accurately reflects the operation of the DDPS and that the results described in Section 2 are indicative of the expected operational performance of the DDPS.
2. RESULTS

2.1 HARDWARE CONFIGURATION ANALYSIS

SDC conducted a study and analysis of the DDPS hardware system as a prerequisite to development of the model. The study was confined to investigation of components involved in data transmission and processing, and the interconnection of the components. The subsequent analysis determined the loading characteristics of components and the constraints under which they interact. Emphasis was placed on consideration of hardware functions that operate on a time scale of a millisecond or more.

The DDPS system with which the investigation was concerned is the ALT configuration as specified in Reference 7, the Level A Hardware Specification. Components, that are not employed during airborne or flight phases of ALT were nevertheless analyzed and are represented in the DDPS model for completeness, and possible use in later studies. The ALT configuration as it was viewed for the purpose of the analysis and model construction is depicted in Figure 2-1. The principal factors in the makeup of this configuration are: (1) four independent computers which can be forced to operate in synchronized or lockstep mode, (2) numerous and varied peripheral equipments which may perform local functions asynchronously with the computers but with which the computers must regularly communicate, and (3) a network of data buses which provide redundant paths between components for communication, and which permit broadcasting of data to several components.

Analysis of programmable components such as the PCMMUs and IOPs indicated that the potential for variations in their operation would not have significant impact on the overall system loading at the millisecond level of discrimination; i.e., they can be treated as essentially hardwired components with relatively fixed behavioral characteristics. Local data transfer functions such as those between DEUs and connected keyboards and display units were considered to have minimal impact on the overall system and could safely be integrated with the behavioral characteristics of the unit in direct communication with the computers (e.g., DEUs and MDMs).

In summary, the analysis indicated that the ALT configuration should be treated as a computer-oriented data processing system, with a bus network and bus terminals, to and from which data are transmitted to the computers.

2.2 SOFTWARE STRUCTURE ANALYSIS

Through the structural analysis of DDPS software, SDC determined the conditions and methods for invoking all of the program modules. The hierarchical organization of the DDPS software and the documentation techniques employed in the design specifications enabled a systematic approach to the development and parameterization of a software model. The control interface specifications and the structured control flow proved particularly useful in this effort.

Module invocation is either a direct or indirect call from another module, or activated as a scheduled process by the Flight Control Operating System (FCOS). The scheduled processes which are significant to system loading
Figure 2-1. IMSIM Simulated ALT Configuration for the Space Shuttle Orbiter
during the airborne and flight phases of ALT are listed in Table 2-1, together with conditions for executing each. Virtually all computation performed by the CPUs is for these processes; i.e., these are tasks to be performed by the CPUs using the program modules as tools. Certain of the processes are used only to effect mode or state transitions; these include the various control segments and the Navigation Transition Task. They occur infrequently and involve negligible processing. A class of "cyclic" processes deals with activities which must respond to events in a timely manner. Processes of this class are scheduled during appropriate phases of the mission, to be activated at frequent intervals. The bulk of computation and data processing is either performed as low priority, long-term tasks, or as a series of short segments which can be incorporated in higher priority cyclic tasks.

Since the DDPS is required to deal with fluctuating loads and possible component failures under severe real-time constraints, the software is designed for self-adaptation to environment and demands within specified limits, and "tuning" parameters have been incorporated to ensure that it meets stated requirements through effective utilization of the DDPS resources. Three features which have been incorporated in the software design facilitate fine tuning for optimum performance: (a) a priority/interrupt system for scheduled processes, (b) distribution of recurrent functions among cyclically scheduled processes with individually assigned frequencies for execution, and (c) use of a central dispatcher to call modules as subfunctions of a cyclic process, at multiples of the fundamental interval for the process.

During ALT airborne and flight phases, all I/O control is concentrated in four cyclic tasks and one event-triggered task; viz., the System Software Interface Processor, the Fast Cycle Executive, System Management Data Acquisition, the Cyclic Display Processor, and the User Interface Control Supervisor. In general, I/O is initiated by these processes through calls on FCOS, and the processes may yield control of the CPU and enter a "wait" state until the requested I/O is complete. Since I/O requests can be enqueued for execution by the IOPs, the CPU can be assigned to lower priority processes during such waiting periods.

Analysis of the software generally did not include consideration of the mission-oriented aspects of the DDPS; i.e., logical intent, mathematics, reliability and information content of data, etc., were not investigated except as required to determine their potential loading impact on the DDPS. This view from a data processing standpoint has determined that certain combinations of functions can be invoked concurrently, which are probably not logically consistent with each other or with the state of the system in the context of mission requirements. For example, it appears to be possible for an IMU calibration SPEC to be invoked during flight, although this is a time-consuming activity which is indicated as a preflight SPEC in Software Awareness Memo #10H for FSW Process Priorities (Reference 34).
### Table 2-1. Significant Scheduled Processes of ALT

<table>
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<tr>
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<th>Descriptive Name</th>
<th>NASA Priority*</th>
<th>Invocation</th>
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<tr>
<td>AIE</td>
<td>System Software Interface Proc.</td>
<td>250</td>
<td>40 ms intervals</td>
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<tr>
<td>GEF</td>
<td>Fast Cycle Executive</td>
<td>250</td>
<td>40 ms intervals unless mode 200</td>
</tr>
<tr>
<td>GMA</td>
<td>Minor Cycle Executive</td>
<td>242</td>
<td>40 ms intervals unless mode 200 and platform not released</td>
</tr>
<tr>
<td>GAD</td>
<td>Mated/Drop Test Idle Mode</td>
<td>238</td>
<td>40 ms intervals during mode 200</td>
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<td>SDA</td>
<td>SM Data Acquisition</td>
<td>234</td>
<td>50 ms intervals</td>
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<td>DMI</td>
<td>MCD Input Processor</td>
<td>230</td>
<td>200 ms intervals</td>
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<tr>
<td>GEM</td>
<td>Mated/Drop Executive</td>
<td>228</td>
<td>80 ms intervals</td>
</tr>
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<td>DMC</td>
<td>User Interface Control Supervisor</td>
<td>226</td>
<td>For MCDS or ICC msg, or application service request</td>
</tr>
<tr>
<td>GAA</td>
<td>Mated/Drop OPS Control Segment</td>
<td>218</td>
<td>For OPS2 message</td>
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<tr>
<td>SFD</td>
<td>SM Flight OPS Control Segment</td>
<td>210</td>
<td>For OPS2 message</td>
</tr>
<tr>
<td>GLC</td>
<td>IMU Operation SPEC Control Seg.</td>
<td>202</td>
<td>For SPEC message</td>
</tr>
<tr>
<td>GUN</td>
<td>RM-NAV SPEC Control Segment</td>
<td>198</td>
<td>For SPEC message</td>
</tr>
<tr>
<td>GUI</td>
<td>RM-CONT SPEC Control Segment</td>
<td>194</td>
<td>For SPEC message</td>
</tr>
<tr>
<td>GUK</td>
<td>NAV/TARGET Update SPEC Control Seg.</td>
<td>190</td>
<td>For SPEC message</td>
</tr>
<tr>
<td>GUA</td>
<td>Horizontal Situation SPEC Control Seg.</td>
<td>186</td>
<td>For SPEC message</td>
</tr>
<tr>
<td>GUB</td>
<td>Vertical Situation SPEC Control Seg.</td>
<td>182</td>
<td>For SPEC message</td>
</tr>
<tr>
<td>DCI</td>
<td>Cyclic Display Processor</td>
<td>142</td>
<td>100 ms intervals</td>
</tr>
<tr>
<td>ARA</td>
<td>GPC Switch Monitor</td>
<td>138</td>
<td>1000 ms intervals</td>
</tr>
<tr>
<td>DGI</td>
<td>LDB I/O Processor</td>
<td>134</td>
<td>40 ms intervals</td>
</tr>
<tr>
<td>GET</td>
<td>Navigation Transition Task</td>
<td>126</td>
<td>once for mode 204 for Navigation Transition Event</td>
</tr>
<tr>
<td>SDM</td>
<td>SM Performance Monitor Ctrl.</td>
<td>122</td>
<td>500 ms intervals</td>
</tr>
<tr>
<td>GEN</td>
<td>TAEN Navigation Cycle Executive</td>
<td>118</td>
<td>2000 ms intervals after platform release</td>
</tr>
<tr>
<td>GMG</td>
<td>IMU Major Cycle Executive</td>
<td>114</td>
<td>320 ms intervals for IMU function</td>
</tr>
<tr>
<td>GMV</td>
<td>IMU Velocity and Tilt</td>
<td>110</td>
<td>as SPEC option</td>
</tr>
<tr>
<td>GTX</td>
<td>FCS/DD Dedicated Display Checkout</td>
<td>106</td>
<td>as SPEC option</td>
</tr>
<tr>
<td>GMT/GMU/GMV</td>
<td>IMU Calibration</td>
<td>80/85/90</td>
<td>as SPEC option</td>
</tr>
<tr>
<td>GMX</td>
<td>IMU Gyrocompass Alignment</td>
<td>75</td>
<td>as SPEC option</td>
</tr>
<tr>
<td>GMS</td>
<td>IMU Attitude Determination</td>
<td>70</td>
<td>as SPEC option</td>
</tr>
</tbody>
</table>

*higher values indicate higher priorities
2.3 DYNAMIC SYSTEM BEHAVIOR

The dynamic behavior of the DDPS model was recorded on an event-by-event basis for each of the simulation runs, in the form of history printouts. As expected, all runs show a continuing conflict among the cyclic processes which were synchronized on 40 ms clock pulses (see the graph of the timeline in Figure 2-2). Since the Software Interface Processor (AIE) has highest priority, it always starts the cycle and initiates ICC transmissions, after which it enters a waiting state. This gives the Fast Cycle Executive (GEF) an estimated 1 to 2 ms to perform before AIE resumes and completes. Following AIE completion for a cycle, GEF runs to completion (it involves not waiting for transmission and hence does not provide an opportunity for lower priority processes to use the CPU until it completes). Upon its completion, the Minor Cycle Executive gains control of the CPU until its completion. This sequence of activity is estimated to require between 12 and 18 ms of the 40 ms cycle, depending mainly on the activity of GEF.

If the assumption is made that the AIE waiting interval is insufficient to permit all GEF I/O to be initiated, then the uninitiated remainder will be deferred for approximately 4 ms until AIE completes. This may be expected to cause some Read requests to be shifted back and forth between the interval and the completion period of GEF in successive cycles. Such a condition would strain or exceed the software systems performance requirements set forth in the Computer Program Development Specification, Volume 1, Book 2, Level A Software (Reference 7). Such variations in reading do occur in the simulations.

Start and completion times for the remainder of the scheduled processes vary as a function of the applied workload. Start and end variations for these tasks are tabulated for two computer runs in Tables 2-2 and 2-3. Each start (or end) variation is determined from the history printouts by subtracting the time of the triggering event (e.g., keyboard input) from the start (or end) time. Table 2-2 shows the result of a typical loading for a 1.1 second simulated flight segment of ALT. Table 2-3 shows results for a 1.24 second period which encompasses Separation.

The first 40 ms cycle is excluded from the derived statistical measures. In fact, the heavy activity of the first 40 ms cycle will recur every 16 seconds, as the cycles of the various processes are in phase at 16-second intervals. Process activity during such periods is depicted graphically in Figure 2-3.

System Management Data Acquisition (SDA) operates on a 50 ms cycle, and hence conflicts with the high priority cyclic processes every fourth cycle. Thus, its initiation (and completion) may be deferred as much as 14 ms, with an average observed variation of 3.5 ms and a standard deviation of 5.3 ms under normal loading. With a heavier loading as shown in Table 2-3, the average delay rises to 4 ms, with a maximum of 18 ms.

The Mated/Drop Executive (GEM) also experiences longer delays in starting under the heavier workload ranging from an average of 14.8 ms to 15.8 ms, although the maximum delay remains 17 ms. The delays are consistently in the range of 13 to 17 ms, and produce a relatively small standard deviation of 1.5 to 1.8 ms.

The MCDS Input Processor (DMI) was able to complete its function within 19 ms of activation in all instances of simulated input. This is within 10% of its cycle period. The User Interface Control Supervisor was generally able to respond to the keyboard inputs within 8 ms, with an average response time of
Figure 2-2. Timeline Graph of Cyclic Tasks
Table 2-2. Time Variations for Processes, Schedule JSAC06

<table>
<thead>
<tr>
<th></th>
<th>80 ms Cycle</th>
<th>50 ms Cycle</th>
<th>Irregular</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>GMR(80)</td>
<td>GMG(320)</td>
<td>SDA(50)</td>
</tr>
<tr>
<td>Start</td>
<td>End</td>
<td>Start</td>
<td>End</td>
</tr>
<tr>
<td>-------</td>
<td>-----</td>
<td>-------</td>
<td>-----</td>
</tr>
<tr>
<td>21*</td>
<td>32*</td>
<td>62</td>
<td>70</td>
</tr>
<tr>
<td>15</td>
<td>29</td>
<td>0</td>
<td>6</td>
</tr>
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<td>26</td>
<td>0</td>
<td>6</td>
</tr>
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<td>27</td>
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</tr>
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<td>14</td>
<td>25</td>
<td>27</td>
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</tr>
<tr>
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<td>28</td>
<td>3</td>
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<td>6</td>
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<td>6</td>
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<td>6</td>
</tr>
<tr>
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<td>16</td>
<td>11</td>
<td>16</td>
</tr>
<tr>
<td>2</td>
<td>7</td>
<td>2</td>
<td>7</td>
</tr>
<tr>
<td>Avg.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>S.D.</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Data from the first cycle, on a 16-second period, are not included in Average Delay and Standard Deviation.
Table 2-3. Time Variations for Processes, Schedule JSCAO7

<table>
<thead>
<tr>
<th></th>
<th>80 ms Cycle</th>
<th>50 ms Cycle</th>
<th>Irregular</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>GEM(80)</td>
<td>GNG(320)</td>
<td>SDA(50)</td>
</tr>
<tr>
<td>Start</td>
<td>End</td>
<td>Start</td>
<td>End</td>
</tr>
<tr>
<td>21*</td>
<td>32*</td>
<td>62</td>
<td>70</td>
</tr>
<tr>
<td>15</td>
<td>29</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>16</td>
<td>27</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>17</td>
<td>28</td>
<td>3</td>
<td>8</td>
</tr>
<tr>
<td>14</td>
<td>28</td>
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<tr>
<td>17</td>
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<td>26</td>
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</tr>
<tr>
<td>17</td>
<td>28</td>
<td>0</td>
<td>6</td>
</tr>
<tr>
<td>Avg.</td>
<td>15.8</td>
<td>27</td>
<td>4</td>
</tr>
<tr>
<td>S.D.</td>
<td>1.8</td>
<td>1.3</td>
<td>6.2</td>
</tr>
</tbody>
</table>

*Data from the first cycle, on a 16-second period, are not included in Average Delay and Standard Deviation.
Figure 2-3. Delay Time for Functions Due to Priority
1.5 ms, although one input during the high-priority activity for a 40 ms cycle delayed response for 22 ms. If the key-in had required significant processing (e.g., a DISPLAY request), the process would have been interrupted for the subsequent 40 ms high priority activity, and this would have resulted in a total delay of up to 40 ms.

The System Performance Monitor Control (SDM) has a relatively low priority with respect to other cyclic executives, and was delayed as much as 33 ms before obtaining CPU service. During peak loading cycles, the Major Cycle Executive (CMG), which also has a low priority, was delayed as much as 28 ms. Because of its significant processing, it may occasionally extend into the subsequent 40 ms cycle and be interrupted for high-priority activity of the cycle, thereby incurring a delay for its completion from the optimum by as much as 51 ms. The Cyclic Display Processor (DCI) also encountered delays of up to 50 ms during two 40 ms cycles, but it was still able to complete its functions well within its 100 ms cycle.

2.4 SYSTEM PERFORMANCE

Statistical data for system loading were gathered during each of the simulation runs. The data included average and maximum loads on individual DDPS components and the delays and interrupts incurred in performing tasks. Only the CPUs were observed to experience heavy loading, and variations in workload were introduced to stress these components in particular.

The run which produced the highest load on the simulated DDPS was controlled by the job schedule denoted as JSAC05. This run showed an overall CPU utilization of 75%; however, it included invocation of IMU calibration which, while apparently not precluded by GN&C software design, is nevertheless an unlikely load for the DDPS during the Mated/Drop Test. The calibration process was subject to interruptions by high priority processes for a total of 178 ms during an elapsed time of 240 ms. If the processor had not been occupied with calibration during this period, it would have been 74% busy; with the calibration, it was 100% occupied, and the period of calibration was increased by 287% (i.e., from a possible 62 ms to 240 ms).

A more realistic, high-load scenario was specified by the job schedule JSAC07, described in detail in paragraph 5.2.5.3. Processor utilization for this run was 70% (see Table 2-4). This includes 97.5% utilization during the initial 80 ms period, the conditions of which recur every 16 seconds. If the initial 80 ms period is excluded, the average CPU utilization is 68% with a standard deviation of 10%; otherwise, the average is 70%, with a standard deviation of 13%. The maximum CPU utilization for any regular 80 ms cycle (other than the first) is 88%. Thus, although the CPU duty cycle appears to have 30% reserve capacity for growth, as required of systems software (see Reference 7, Level A Software Specification), it exists only for processes which can tolerate delays of up to 200 ms. For growth of processes which require an 80 ms cycle, only 10-12% growth potential exists, without degradation in performance of currently defined processes.

Table 2-4 provides a synopsis of the CPU utilization by 80 ms time slices. It gives the idle periods in ms and processor utilization % for each of the 80 ms
Table 2-4. CPU Activity for JSCA07

<table>
<thead>
<tr>
<th>Cycle Number</th>
<th>Start Time (ms)</th>
<th>Idle Periods (ms)</th>
<th>% Busy</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>32001</td>
<td>2</td>
<td>97.5</td>
</tr>
<tr>
<td>2</td>
<td>32081</td>
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<td>32241</td>
<td>13</td>
<td>67.5</td>
</tr>
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<td>32321</td>
<td>1</td>
<td>67.5</td>
</tr>
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<td>6</td>
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<tr>
<td>8</td>
<td>32561</td>
<td>15</td>
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<td>9</td>
<td>32641</td>
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<td>66.3</td>
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<td>32961</td>
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</tr>
<tr>
<td>15</td>
<td>33121</td>
<td>5</td>
<td>50</td>
</tr>
</tbody>
</table>

Average with Initial Cycle 70.0
Standard Deviation with Initial Cycle 12.5
Average without Initial Cycle 67.7
Standard Deviation without Initial Cycle 10.3
time slices indicating their cycle start times. It also gives the average CPU utilization percent and standard deviation with and without the initial 80 ms heavy load period. These figures are graphically depicted in Figure 4-2, CPU utilization per 80 ms regular cycle.

The transport lag for the highest rate flight control functions was not specifically investigated. However, it is apparent that no significant time is spent in transmitting either way between the MDMs and GPC memory because of the high data transfer rates of the MDMs and buses, and because flight-critical buses are dedicated for these transmissions. If delays do occur, it would be the result of contention between the Fast Cycle Executive and the System Software Interface Processor for the CPU, or of excessive computational requirements for the Fast Cycle Executive. The latter computational requirement is estimated to be less than 15.8 ms in the worst case. Although it should be possible to organize computation for the Fast Cycle Executive so that critical output occurs earlier in the process, it should be noted that this time exceeds the limit of 15 ms specified in Reference 7, the Level A Software Specification. The System Software Interface Processor is estimated to require a maximum of 3.7 ms per cycle and may have serious impact on the transport lag if allowed to interrupt the Fast Cycle Executive. The Fast Cycle Executive may be further delayed if it performs concurrently with ICC data transmission. This transmission reduces memory accessibility to the CPUs by one third; if the transmission requires 2 ms, concurrent processing time is increased by 0.67 ms.

Loading of other components and traffic on buses can generally be characterized as light. The nature of the bus network, and the configuration of DDPS components essentially eliminates data traffic congestion. The most heavily loaded buses and bus terminals, as indicated by simulation summary statistics, are:

- PCMMU #1 and its bus (IPI) 18% utilization
- ICC buses 15% utilization
Figure 2-4. CPU Utilization per 80 ms Regular Cycle
3. CONCLUSIONS

3.1 SYSTEM CAPACITY

The CPU duty cycle of each computer appears to have a 30% reserve capacity for the major cycle (assumed to be 320 ms) as required. For processes having an 80 ms cycle, reserve capacity is estimated at 10%.

The databus network is only lightly loaded and is configured so that virtually no message congestion occurs. The ICC buses operate at capacity during memory transmission and impose the most significant I/O loads on memory during a period of every 40 ms cycle; however, this is estimated at 30% of memory processes for 5% of the time, or 1.5% of the capacity for memory access. Databuses are estimated to have reserve capacity for transmission in excess of 80%.

In summary, the capacities for processing and data transmission of the GPCs and the databus network appear adequate to support the Approach and Landing Test.

Memory capacities were not studied. See Section 3.3 for discussion on this subject.

3.2 RESPONSE CHARACTERISTICS

Since the System Software Interface Processor is assigned the highest priority of scheduled processes, it is executed on schedule and can respond to I/O completion with virtually no delay. Offset adjustments in the schedules for the second and third highest priority cyclic processes - the Fast Cycle Executive and the Minor Cycle Executive - should make it possible for both of these processes to execute on schedule, and for the Fast Cycle Executive to respond immediately to I/O completions.

Response of other processes generally deteriorates as priority decreases. Delays in completion of 25 - 35 ms are typical, although these can probably be reduced by 10 ms through offset scheduling for the cyclic processes. Delays of 40 - 70 ms were experienced in completing longer-running processes (i.e., Cyclic Display Processing, Performance Monitoring, and IMU Major Cycle Processing) because they overlap two successive 40 ms cycles and were subject to interruption by the high-priority processes of the second cycle.

Only the high-level timing requirements set forth in Reference 7, the Level A Software Specification, were considered in determining the suitability of the response characteristics indicated by simulation; the applications software function timing requirements, which were mentioned in this reference as being specified in Level B CPDS documents, were not available at the time of the requirements analysis. Performance of the functions of the Fast Cycle Executive can be made virtually independent of other processes by priority and scheduling offsets, and is therefore only determined by the programming of functions executed for the process and the dispatching algorithm used in calling the functions. Variation in initiation and input times can probably be confined within the specified limits, but it is not clear that lag time for flight control functions is less than the required 15 ms period.
A cursory study of the just-received Detailed Software Design Specifications for GN&C (Reference 29) indicates that significant effort has gone into design of the Fast Cycle Executive to minimize its response times. However, this document was not received by SDC prior to the completion of the analysis phase of this contract, and this information was not subjected to detailed analysis, nor was it used in modeling and simulation of the DDPS.

3.3 ADAPTABILITY

The DDPS design, as specified in the Level A Software Requirements (Reference 7), limits the scope of the software to meet mission requirements, but does not impair the capability for adaptation to new requirements and changing environmental conditions. On the contrary, such capabilities are explicitly incorporated in design specifications. The concepts of hierarchical software structure, modular coding, and centralized data base and dispatching control provide great flexibility for adapting the software to meet new demands. The traceability provided by design specifications enables the tracking of data elements from source to destinations and the tracing of program logic through the software structure. It appears to be relatively easy to locate and change any portion of the software and to determine impact on the remainder of the system. Additional logic can readily be "plugged in" to the system, insofar as programming and data manipulation are concerned.

Changes or additions to the software which affect the critical timing of DDPS software pose special problems. As discussed in the Software Analysis (Section 2.2), special features have been incorporated in the software design to facilitate tuning of the system to meet the real-time requirements of Shuttle Orbiter missions. The scheduling and dispatching facilities appear admirably suited to meet these needs, and to accommodate future requirements as they become known, without necessitating changes to the basic software structure or to logically disconnected functions.

The most severe constraint on adaptability of the DDPS appears to be the amount of main memory available for the GPCs. The Level A Software Requirement specifies a 15% reserve capacity to be retained in main memory for growth. SDC did not investigate memory requirements for software since dynamic loading of software is not performed in the ALT; in any case, data software sizing was not available for most of the applications modules. However, on the basis of SDC's previous experience with similar system development, it is reasonable to expect difficulty in maintaining the specified reserve.

The DDPS design specifications provide for system parameterization and control interfaces which essentially establish a logically open-ended system. The upper-level structure and components of the software are rigidly specified Operational Sequences, Modes, and Displays, but the provisions for Specialist Functions and Item inputs act as escape clauses to permit additional facilities to be incorporated. The options and electives for system control should be itemized as requirements in the Level A Software Specification and corresponding checks should be incorporated in the software to prevent undefined system status or inconsistent processes.
from being established. For example, as noted in Section 2.4, IMU calibration was simulated during flight phase although this is ostensibly a preflight process. This was done because analysis of the design specifications did not uncover software checks which would preclude activation through an option of the IMU Specialist Function.

With the above mentioned qualification, the software is readily adaptable to future requirements.
4. RECOMMENDATIONS

The following recommendations have evolved from extensive analyses of the results of these simulations, and also reflect detailed SDC studies of the proposed hardware and software structures that preceded these modeling efforts.

4.1 DDPS CONFIGURATION RECOMMENDATIONS

a. The estimated 10% expansion margin for 80 ms cycle processes may not be adequate. The possibility should be examined, and both effects and remedies for inadequacy should be detailed. Additional simulations should be performed as necessary to verify these remedies.

b. The memory space requirements of the software should be monitored closely during development. If the required 15% reserve is infringed upon, efforts to reduce space requirements should be concentrated on changes in program organization and algorithms; coding techniques and shortcuts which stretch or break the rules for DDPS software development (i.e., rules regarding structured programming and compool-defined data) will degrade its adaptability and interfere with subsequent maintenance.

c. Greater control over process scheduling and response characteristics can be achieved through the use of counters to record event occurrences, instead of simple flipflops. An example of the need for this capability is evidenced by the phase counts employed by the hybrid dispatcher to control module execution on multiples of the basic cycle of a process. This concept should be incorporated as a fundamental design specification and employed liberally for frequent synchronous and asynchronous events. Note that it is not necessary to reduce or reset such counters during the mission. They may be tested against threshold values which can be continually raised by 1, 2, 8, or any number to cause response at the desired multiple of the event occurrence. This not only serves the purpose of the hybrid dispatcher, but allows self-checking by a module to determine if it is missing cycles because of time and priority constraints.

d. As discussed in Section 3.3, more checks should be specified and incorporated in the software to ensure proper keyboard inputs for the system state. "Software Design Specification - Part II: Approach and Landing Test (ALT) Detailed Design Specification - Guidance, Navigation, and Control" (Reference 29) indicates the possibility of placing the system in an "unknown and unverified state". Furthermore, even theoretically legal requests may activate functions which are not consistent with the mode or phase of the mission. To deal with these problems, legality and reasonableness checks should be incorporated in the User Interface software. Such checks could improve reliability and aid flight personnel in interacting with the DDPS, and would expand design specifications to close loopholes in requirements which might be
inadvertently used as a convenient, but unsystematic, adaptation of the software system to meet unforeseen demands. SDC recommends that attention be directed to a study of this area.

e. System tuning is necessary to meet critical response requirements, and has been planned for in the design specifications. SDC recommends that as much tuning as possible for dynamic functions be performed through the use of computer simulation, prior to completion and exercise of actual software. Use of scheduling offsets, priority changes, dispatching, etc., can readily be tested in a variety of combinations prior to experimentation with the real system.

4.2 AUGMENTATION OF SIMULATION EFFORTS

a. The dynamic, discrete simulation model of the DDPS was developed by SDC to fulfill the objectives of the DDPS study. Its operation has been verified and validated against requirements and currently available performance data. SDC recommends its continued use as a device for experimenting with scheduling algorithms and applied workloads for the DDPS under a variety of conditions which would be difficult or impossible to create for the actual system. The monitoring and reporting facilities of the model could not be effectively incorporated in the real system; no other approach can enable system designers to obtain more insight into the dynamic behavior of the DDPS during its development. Use of the model also provides project management with an overview of the dynamic, as well as static, character of the DDPS.

b. Continued use of the model should include incorporation of up-to-date information on detailed design specifications, estimates of program module timing, and message lengths and frequencies, with emphasis on key functions such as GN&C. To accomplish an extended analysis of GN&C functions, most of the hardware specifications (IMSIM Forms 6 through 14) will remain unchanged, but virtually all of the software workload parameters (IMSIM Forms 2 through 5) must be redone completely. Efforts to be accomplished include aspects of the following activities:

1. Requirements analysis
2. Test design
3. Model adaptation and parameterization
4. Model execution
5. Test analysis and documentation

c. Further effort should be expended to determine the greatest stress situations which can develop during the ALT mission, and results should be employed in constructing workloads for the model. Additional conditions which should be investigated via simulation include system errors and component failures. These can be simulated according to precise schedules to achieve maximum impact.
d. The model has direct application to the study of DDPS performance for missions and test phases. In particular, Operational Flight Test requirements for the DDPS need to be analyzed from a dynamic functional standpoint to determine behavior with an additional simplex mode GPC and software execution for new major functions and modes. The impact of additional dynamic loading for activities such as uplink-downlink and payload monitoring should also be investigated.

e. While the DDPS model is well suited to the investigation of dynamic functions at a resolution of 1 ms, it should not be indiscriminately used to represent all such functions of the DDPS. Functions which are independent of each other, or at least series-related, should be individually modeled as required to observe their individual behavior.

SDC has designed the DDPS model to represent the functions of the GPCs, the bus network, and bus terminals as an integrated system in which feedback is an essential characteristic. Localized activity, such as occurs in DEUs, IOPs, and PCMMUs, may normally have negligible impact on the DDPS operation at the 1 ms level of discrimination, but may still require simulation to determine situations in which they become saturated or otherwise loaded so as to change their operating characteristics and affect general system performance. The precise steps by which the Process Management component of the Flight Control Operating System monitors events and schedules processes should be simulated in detail to determine performance and dynamic loading conditions, and used as an aid in making systematic, effective improvements in scheduling algorithms and methods of implementation. In this manner, a variety of aspects of synchronous and asynchronous approaches can be evaluated effectively.

f. SDC also recommends that consideration be given to the construction of models of system components to study their behavior through simulation on appropriate time scales (e.g., to a microsecond level). Such models may be built using IMSIM, as was the DDPS model, or they may be constructed using the underlying general-purpose simulation package MODLIT - upon which IMSIM is based. Both of these tools may be used to construct models which can be operated dynamically by discrete simulation to yield useful data on behavior under conditions which are difficult or impossible to duplicate in real systems. Furthermore, processes such as intercomputer communication may be represented at more than one level of time resolution in different models. For example, a fine-resolution model can be used to determine "macroscale" characteristics for inclusion in another model.
5. TECHNICAL DESCRIPTION

The following paragraphs describe in detail the objectives of the Dynamic Loading Analysis Study and the efforts performed under each of the tasks defined in Section 2.1 of the Statement of Work.

5.1 INTRODUCTION

High-speed digital computers have been increasingly applied to the analysis and design of complex systems. One of the most useful techniques for such applications is that of discrete simulation, in which the system is represented in the computer as a dynamic model which changes its state with the stepwise passage of simulated time.

The IMSIM model has been developed to aid in the investigation of systems which include computers. It is constructed upon the MODLIT Discrete System Simulator. In effect, IMSIM is a general model of a computerized transmission system, which can be tailored to represent a wide variety of configurations, components, and applied loadings. Furthermore, as a fully interactive model, it enables the user to monitor its behavior and to make dynamic modifications during simulation.

The objectives of the Dynamic Loading Analysis Study and the model goals are presented in paragraph 5.1.1. The guidelines and assumptions for the model development are delineated in paragraph 5.1.2. A brief conceptual overview of IMSIM is given in this introduction in paragraph 5.1.3, and the overall approach to the model development, applied workloads, and dynamic simulation is given in paragraph 5.1.4.

5.1.1 Objectives and Model Goals

The primary objective of the Space Shuttle Orbiter Digital Data Processing System Dynamic Loading Analysis effort was to investigate the dynamic behavior of the Orbiter's data processing subsystem during specific operational sequences, in order to identify and formulate resolution of potential problems for critical performance areas.

To meet this objective, the generalized IMSIM model was adapted and parameterized, so that the Space Shuttle's hardware and software functions were properly represented in this model.

The model goals were established as a result of the work performed under the Data Systems Requirements Definition task (Statement of Work task 2.1.1).

From a study of the overall dynamic hardware and software data flow requirements it was determined that the IMSIM model should be constructed within the following set of basic guidelines:

- The model should be configured so as to allow statistical data generation on the dynamic behavior of central processing units, which will be the focal point for analyzing system performance.
Suspected potential data flow problem areas (defined by a Sensitivity Analysis) should be modeled such that data could be generated to determine if and/or to what extent these areas are critical in respect to system performance.

- The model should be designed for a specific operational configuration and include only that hardware and software required to simulate the functional dynamics required for that operation, i.e., Shuttle Orbiter Data Processing Subsystem characteristics such as operational reconfiguration, fail and fault redundancy, and BITE should not be incorporated in the model.

5.1.2 Guidelines and Assumptions

5.1.2.1 Model Guidelines. The following NASA specified guidelines for the IMSIM model were defined in a project coordination meeting held in August 1975 and in subsequent coordination communications:

a. The simulation model will be adapted, parameterized, and executed for the Approach and Landing Test (ALT) configuration for the Mated Flight/Drop Test.

b. The specific configuration to be simulated is the ALT Memory Configuration #2 as specified on page 6-15 of Computer Program Development Specification Volume I, Book 2 (revised) #SS-P-002-120A-1-System Level A Requirements, Software, (Reference 7) and restated in revision B, dated 26 September 1975.

c. A four-GPC redundant configuration with data paths to the multiplexer/demultiplexer (MDM) hardware level is to be simulated.

d. ALT Memory configuration #2 is to include the Downlist format #1, as specified on page 4-1 of Computer Program Development Specification, Volume I, Book 4, #SS-P-0002-140, Downlist/Uplink Software Requirements (Reference 9).

e. The GN&C Mated Flight/Drop Test OPS and the SM Flight OPS will be the operational sequences for the model.

f. Hardware units that will be excluded from the ALT configuration are as follows:

Ascent TVC Driver
Forward Reaction Jet Driver
Reaction TOT OMS Driver
Star Tracker and Light Shield
Network Signal Processor
S-Band Network Equipment
Doppler Extension
Payload Signal Processor
Rendezvous Radar
Transition Hand Control Unit
MDMs for LL, LR, and OT
Engine Interface Unit
Master Events Controller.

There will be no uplink capability for the ALT configuration. Downlink will be accomplished via a direct interface from the PCMMU to the S-band system. The downlink data rate will be at 128 Kbps.

The Downlist Data Controls Processor (DDC_DWN_LST_CONTROLS) will not be active during Mated/Drop Test.

The GPC/PCMMU Data Cycle Synchronizer (DCS_SYNC) will not be invoked during Mated/Drop Test.

5.1.2.2 Assumptions. Based on the NASA supplied guidelines, the Approach and Landing Test (ALT) Functional Design Specifications (References 18 through 21), and the ALT Computer Program Development Specifications (References 10 and 11), the following assumptions have been defined for the IMSIM model:

a. IOP control activity and its memory access for commands have negligible impact on system functions at the millisecond level of perception, and therefore is not simulated. Data transmissions are associated directly with the processes which initiate or process them.

b. Only the processes within one GPC are simulated, based on the assumption that virtually identical loading of the CPU occurs in all members of a redundant set. Simulation of activity in all GPCs would simply increase operating times for simulation and would yield no additional information.

c. The User Interface Control Supervisor is only simulated for MCDS messages and Applications service. Completion of MM I/O service is excluded.

d. For Cyclic Display Processing (DCI_CYC_DISPLAY) and New Display Processing (DMC_NEW_DISPLAY) I/O is not suppressed for any DEU, displays are never frozen, and output is always a full page (509 words).

e. The GPC Downlist Formatter (DCD_DOWNLIST) is assumed to be enabled.

f. The Launch Data Bus I/O Processor is not employed during the Mated/Drop Test.

g. The DEU Loader (AIG_DEU_LOADER) is not scheduled during Mated/Drop Test.

h. No change of state results from switches monitored by the GPC Switch Monitor (ARA_GPC_SWITCH).
i. The following System Control processes are not simulated because they are irrelevant to the Mated/Drop Test: ASA, ASB, ASC, ASD, AIB, ARB, ARC, ARH.

j. The computation associated with GNC OPS 2 Control Segment (GAA_OPS2 MATED DROP TEST) is included in the User Interface process (DMC_SUPER); hence, this process is not simulated as a task.

k. The Preflight OPS Control Segment (GAV_OPS1_PRE_FLT) is not invoked during the Mated/Drop Test and is not simulated as a task. The Preflight Executive which is scheduled during mode 101 of OPS 1 is also not simulated but the Fast Cycle Executive and the IMU Minor Cycle Executive are started prior to simulation of the Mated/Drop Test.

l. IMU Calibration is assumed to be performed with only one type of calibration at a time (i.e., GMT, GMU, or GMV).

m. The Control Segments for GMC Specialist Functions are assumed to involve negligible computation and are not simulated as tasks; they include GUA, GUB, GUC, GUG, GUH, GUI AND GUK.

n. ALT memory configuration #2 can be accommodated in GPC memory with no capacity problems.

o. Task scheduling will be performed as follows:
   a) Processing is interruptible by the executive and critical tasks (IMSIM tasks of service class #1).
   b) Critical tasks have precedence and confiscation privileges over noncritical tasks in obtaining processors.
   c) Scheduling is determined by task priority.

p. All transmissions are to be over explicitly defined data links and no implicit links are allowed.

q. The CPU will not be interrupted in performing a task in order to initiate and service I/O (this function is performed by the IOP of the DDPS).

r. A time resolution of 1 ms is sufficient for the investigation of DDPS processes as specified by the S W.

s. Mass Memory Message Processing (DMP_MM_MSG_PROC) is not used in ALT.

t. Reconfiguration does not occur in ALT.

u. MCDS Major function change does not occur.

v. CMPTR/CRT and CMPTR/BUS keys are not used in ALT.

w. The ITEM DATA key sequence is not used.

x. New displays are always sent to DEUI.
y. Three DEUs are updated by Cyclic Display Processing (DCI_CYC_DISPLAY).

z. The ICC Router (DME_ICC_ROUT) is referenced by the System Software Interface Processor (AIE_SIP).

aa. Each display update requires four scalar conversions and 10 item formatings.

5.1.3 Conceptual Overview of IMSIM

5.1.3.1 Hardware Representation. The equipment simulation categories used in IMSIM cover five basic types of equipment: memory units, storage units, computer processors, data transmission links, and a group called "devices" that includes all hardware not covered by the other four categories. Although there is no theoretical constraint upon the organization of processors and memory units, attempts by the computing industry to design control programs (operating systems) for various configurations of computers have resulted in the definition of a substructure for large computer systems. To realistically represent such systems for simulation, IMSIM includes the concept of the "virtual machine": a computer in which at least one processor can access all memory units. In its simulation runs, SDC has simulated the Space Shuttle's digital data processing system both ways, viz., as one Virtual Machine with four GPCs, and as four separate Virtual Machines.

Storage units and devices are generally considered as global (system-wide) system components, but can be viewed as local (to a virtual machine) when connected exclusively to a machine via data transmission links. Processors and memory units are always considered as local components. Data links are defined for use in connecting any components except processors, and have either local or global status, depending upon the configuration.

Inputs to IMSIM include the means for specifying characteristics for individual members of each of the component types mentioned, together with a description of the way in which they are to be configured. One other type of component is defined in IMSIM and is classified as hardware: the "data set". A data set may be viewed as a subdivision of a storage unit, and is intended to correspond to a file of data to be stored in the unit.

5.1.3.2 Software and Workload Representation. In order to study the dynamic behavior of a system representation by IMSIM, it is necessary to apply a load to the system. A workload structure has been incorporated in IMSIM which resembles that of the actual computer system. It includes general building blocks for rudimentary representation of computer programs and data and for describing data transmissions, and the means for organizing these elements into a hierarchical structure which is consistent with the hardware representation. The building blocks are denoted as routines, data blocks, and messages. These are combined into "tasks" which are units of work to be
performed by a single virtual machine. Tasks, in turn, are organized as a time-distributed network of steps which are collectively denoted as a "job"; a job is a unit of work to be performed by the overall system. This organization is depicted in Figure 5-1.

Routines and data blocks are always considered to be local elements of virtual machines, while messages may have either global or local significance, depending upon their individual characteristics and the hardware configuration. Inputs to IMSIM provide the means for specifying characteristics of individual elements, including constraints on assignment to virtual machines and sharability among concurrent tasks.

Figure 5-1 - Workload Structure in a Simulated System
5.1.3.3 Functional Description. The functional logic which is incorporated in IMSIM includes representation of hardware behavior, applications programs, and executive software. Distinguished system components - whether hardware or software - are represented by suitable MODLIT entities such as facilities and storages. Both the logic and the system components are generalized IMSIM capabilities which must be tailored to suit the system to be simulated. For this reason, IMSIM is designed to operate in two phases: initialization and simulation. In the initialization phase, IMSIM receives and processes "forms" which complete a system definition and describe a workload to be applied to the defined system during simulation. Certain system specifications can also be processed during simulation, thereby permitting the dynamic modification of the system.

The logic of IMSIM is expressed in terms of MODLIT logic blocks, and can be subdivided into eight sections:

a. Processing of input specifications
b. Processing of job requests
c. Task preparation
d. Task execution
e. Element space allocation
f. Message preparation
g. Message transmission
h. Task removal

The first of these constitutes the initialization phase. A portion of this phase together with the other seven sections, comprise the simulation phase.

5.1.3.4 Preparation of Model Specifications. This section describes the various specification forms which were used to complete the definition of IMSIM for representation of the Space Shuttle's DDPS and to define software and workload characteristics.

Each form is represented by one or more lines of input. Only the first 71 characters of each line are interpreted. Positions 1 through 70 contain the information to be read; position 71, if occupied by any character other than a zero, indicates that the next line in the input sequence is a continuation of the current line. Positions 72 through 80 are used for sequence numbers.

A double prime ("" ) in positions 1 and 2 or a quotation mark ("" ) in position 1 indicates that the line is a comment which is used solely to annotate printed outputs. All input lines are interpreted on a free-field basis, i.e., one or more spaces separate successive fields.
The first field of each form contains an integer which identifies the form type. The layout line which follows the column headings line of each form description indicates roughly the magnitude of values for each field (e.g., nnnnnnn) and signifies the optional use of a fractional value: nnn. means a fractional value is possible, while nnn means that only integer values should appear. If a fractional value is specified, it must be presented as decimal with at least one integer on each side of the decimal point, i.e., 5.01, 66.0, and 0.2 are legal but 5., 66., and .2 are not.
### FORM 1 - JOB DEFINITION

<table>
<thead>
<tr>
<th>Form</th>
<th>Job</th>
<th>Task Type</th>
<th>Priority</th>
<th>Nature</th>
<th>Go/NoGo</th>
<th>Immediate Predecessors</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>nn</td>
<td>nn</td>
<td>n</td>
<td>n</td>
<td>nnn</td>
<td>nn nn ... (to a maximum of 24)</td>
</tr>
<tr>
<td>E.G.</td>
<td>1</td>
<td>2</td>
<td>6</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>15</td>
<td>3</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>8</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>6 15</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>6</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>377</td>
</tr>
</tbody>
</table>

**Job**: The number of the job prototype being defined (Job 1 is reserved for the simulated executive).

**Task Type**: Each line specifies a job step - this field contains the number of the type of task for the step (see Form 2).

**Priority**: A number between 1 and 9, indicating the priority of the step; 9 is the highest priority.

**Nature**: A 3 in this field for any job step indicates that the job is cyclic (i.e., it repeats continuously); if the job is not cyclic, a 2 indicates that the step is cyclic; otherwise, a 1 should appear.

**Go/NoGo**: The number of a MODLIT variable whose value determines whether or not the step is to be performed; nonzero = Go, zero = NoGo.

**Immediate Predecessors**: The numbers of other tasks in the job which must directly precede the given step during performance, and which must be completed before the given step can start; there may be no predecessors.

---

**ORIGINAL PAGE IS OF POOR QUALITY**
b. **FORM 2 - TASK DEFINITION**

<table>
<thead>
<tr>
<th>Form</th>
<th>Task Type</th>
<th>Service Class</th>
<th>Permissible Delay</th>
<th>Required Elements</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>nn</td>
<td>n</td>
<td>nnnnnnnnnnnnnnnn</td>
<td>nnnn nnnn ... (to a maximum of 100)</td>
</tr>
<tr>
<td>E.G.</td>
<td>6</td>
<td>5</td>
<td>0</td>
<td>30007 30021 40035 40030 50020 50008</td>
</tr>
<tr>
<td></td>
<td>15</td>
<td>1</td>
<td>100</td>
<td>30008 40030 50010 50011</td>
</tr>
</tbody>
</table>

**Task Type**
- The number of the task prototype being defined (Tasks 1 through 5 are reserved for the simulated executive).

**Service Class**
- 1 - critical; perform immediately (Permissible Delay is ignored).
- 2 - timely; becomes critical following lapse of Permissible Delay.
- 3 - timely; becomes noncritical following lapse of Permissible Delay.
- 4 - timely; discard if Permissible Delay elapses.
- 5 - noncritical (Permissible Delay is ignored).

**Permissible Delay**
- A period in milliseconds commencing with job start (see Service Classes 2 - 4)

**Required Elements**
- Identifiers of routines (see Form 3), data blocks (see Form 4), and messages (see Form 5) which comprise the task; identifiers are
  - 300nn for a routine type nn
  - 400nn for a data block type nn
  - 500nn for a message type nn
### FORM 3 - ROUTINE DEFINITION

<table>
<thead>
<tr>
<th>Form</th>
<th>Routine</th>
<th>Share Class</th>
<th>Library Data Set</th>
<th>Size</th>
<th>Execution Time</th>
<th>Processor Class</th>
<th>Memory Residence</th>
<th>Computation Time</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>nnn</td>
<td>n</td>
<td>nnnnnnn</td>
<td>nnnnnnnnn</td>
<td>nnnnnnnnnn</td>
<td>nn</td>
<td>nnnnn</td>
<td>v</td>
</tr>
</tbody>
</table>

**Routine**
The number of the routine type being defined (Routine 1 is reserved for the simulated executive).

**Share Class**
1 if the routine can be shared among tasks; 0 if not.

**Library Data Set**
The identifier of the data set which is supposed to contain a loadable form of the routine (See Form 11), or the number of a MODLIT variable which is to be evaluated when loading occurs, to determine the identifier.

**Size**
The number of characters of memory space required for the routine.

**Execution Time**
The maximum amount of time (in milliseconds) that the routine will operate for a task; zero if no limit.

**Processor Class**
The level of processor capability required to execute the routine (See Form 9).

**Memory Residence**
The memory into which copies of the routine can be loaded, or zero if no restriction;
- 0 - load into any memory, as required for tasks
- nnn - evaluate variable nnn to determine memory identifier
- 70001 - the memory to which the routine is to be loaded

**Computation Time**
The number of a MODLIT variable to be evaluated whenever a transmission completes for a task, to determine the amount of computing (in milliseconds) to be spent in executing the routine; also, the values assigned to X44 and X45 for possible use as parameters in the given variable (they may be ignored).
d. **FORM 5 - MESSAGE DEFINITION**

<table>
<thead>
<tr>
<th>Form</th>
<th>Message</th>
<th>Nature</th>
<th>Source</th>
<th>Sink</th>
<th>Length</th>
<th>Interval</th>
<th>Start Time</th>
<th>Total</th>
<th>Storage Effect</th>
<th>Trigger Domain</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V X44 X45</td>
<td>V X44 X45</td>
<td>nnnnn</td>
<td>n</td>
</tr>
<tr>
<td>5</td>
<td>nnn</td>
<td>n</td>
<td>nnnnn</td>
<td>nnnnn</td>
<td>nnnnn</td>
<td>nnnnn</td>
<td>nnnnn</td>
<td>nnnnn</td>
<td>nnnnn</td>
<td>n</td>
</tr>
</tbody>
</table>

**Examples:**

```
5  8  0  60003  40030  16  20  0  16  0  0  0  1  0  0
5 20  1  57050 110002 1000 200 15 16 70 0 0 0 0 1 0
5  31  0  397  398  399  0 0 16 20 0 100 0 0 1
```

**Message**
The number of the message type being defined (Messages 1 through 5 are reserved for the simulated executive).

**Nature**
- 0 - Frequency of transmission (see the Interval field) is dependent upon task execution; a separate transmission sequence is established for each task.
- 1 - Message transmission is shared among tasks and occurs independently of task execution, but transmissions may accumulate.
- 2 - Message transmission is shared among tasks and occurs independently of task execution, but if a transmission is not started prior to the next transmission due for the message, the transmission is lost.

**Source**
The identifier of a defined unit which is suitable for use as a source or sink, or the number of a MODLIT variable to be evaluated whenever the message is to be transmitted, to determine the identifier:
- nnn - variable number
- 60nnn - device (See Form 6)
- 40nnn - data block (See Form 4)
- 70nnn - memory (See Form 7)
- 50nnn - message (used only as a source)
- 110nnn - data set (See Form 11)

**Sink**
The number of a MODLIT variable to be evaluated whenever a transmission of the message is to be transmitted, to determine the length (in characters) of the transmission; also, the values assigned to X44 and X45 for possible use as parameters in the given variable (they may be ignored).

**Length**
The number of a MODLIT variable to be evaluated whenever a transmission of the message (or triggering message if appropriate) completes, to determine a time interval (in milliseconds). If Source is a message, this is the time between completion of the triggering message and the start of the response; if the Source is not a message, this is the time between successive transmissions of this message. X44 and X45 are used as in the Length field; the Interval field is ignored if Total is 1 for a nontriggered message.

**Interval**
The period (in milliseconds) which must elapse before the message can be transmitted; measured from the start of a task if Nature is 0, or else from the start of the job.

**Start Time**
The number of transmissions of the message; 0 if no limit.

**Trigger Domain**
Applies only to messages triggered by other messages; 0 if any transmission of the trigger message is to trigger this message; 1 if only transmissions related to the task are relevant to this message.
6. FORM 6 - DEVICE DESCRIPTION

<table>
<thead>
<tr>
<th>Form</th>
<th>Device</th>
<th>A/D</th>
<th>Share Class</th>
<th>Record Size</th>
<th>Transmission Rate</th>
<th>Reset Period</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Input</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Output</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>nnn</td>
<td>n</td>
<td>n</td>
<td>nnnnn</td>
<td>nnnn.</td>
<td>nnnn.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E.G.</td>
<td>6</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>10</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>12</td>
<td>1</td>
<td>1</td>
<td>800</td>
<td>5</td>
<td>6</td>
</tr>
</tbody>
</table>

Device
The number of the device being described.

A/D
1 - digital
2 - analog
3 - digital to analog
4 - analog to digital

Share Class
0 - can only be assigned to one task at a time
1 - can be shared among tasks

Record Size
Limits the length of a transmission by truncating it, if necessary, to the number of characters indicated; zero if no limit on record size.

Transmission Rate
The rate (in characters/millisecond) at which data can be received (Input) or sent (Output) by the device.

Reset Period
The time (in milliseconds) required by the device to recover from a transmission before it can start another.
**f. FORM 7 - MEMORY UNIT DESCRIPTION**

<table>
<thead>
<tr>
<th>Form</th>
<th>Memory Unit</th>
<th>Speed Factor</th>
<th>Number of Pages</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>nnn</td>
<td>nnnn</td>
<td>nnnnn</td>
</tr>
<tr>
<td>E.G.</td>
<td>7 1</td>
<td>1</td>
<td>256</td>
</tr>
<tr>
<td></td>
<td>7 2</td>
<td>0.25</td>
<td>1000</td>
</tr>
</tbody>
</table>

- **Memory Unit**: The number of the memory unit being described.
- **Speed Factor**: The ratio of the memory access rate to a nominal rate of 1 character per microsecond; e.g., "2.5" indicates an access rate of 2.5 characters/microsecond.
- **Number of Pages**: The number of virtual machine pages (see Form 14) which constitute the capacity of the memory unit.
### Form 8 - Storage Unit Description

<table>
<thead>
<tr>
<th>Form</th>
<th>Storage Unit</th>
<th>A/D Share Class</th>
<th>Cycle</th>
<th>Transmission Rate</th>
<th>Capacity</th>
<th>Access Period</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>nn</td>
<td>n n</td>
<td>mm</td>
<td>mmmm</td>
<td>nnnnnnnn</td>
<td>nn nn nn nn</td>
</tr>
<tr>
<td>E.G.</td>
<td>8</td>
<td>1 1</td>
<td>0</td>
<td>8.2</td>
<td>1000000</td>
<td>16 5</td>
</tr>
<tr>
<td></td>
<td>8</td>
<td>2 1</td>
<td>25</td>
<td>12.1</td>
<td>500000</td>
<td>388 20 5</td>
</tr>
</tbody>
</table>

**Storage Unit**
The number of the storage unit being described.

**A/D**
1 - digital
2 - analog

**Share Class**
0 - can only be assigned to one task at a time.
1 - can be shared among tasks.

**Cycle**
A zero indicates that the storage unit is noncyclic; i.e., it is in motion only during transmission operations (e.g., a tape). A nonzero value indicates that the storage unit is cyclic (e.g., a disk or drum) with a period in milliseconds as specified by the value.

**Transmission Rate**
The rate (in characters/millisecond) at which the storage unit can send or receive data.

**Capacity**
The number of characters which the storage unit can accommodate.

**Access Period**
The number of a MODLIT variable to be evaluated whenever the storage unit is to be accessed, to determine the time (in milliseconds) that is to be spent in locating the data (or place for the data) to be transmitted; also, the values assigned to X44, X45, X56, and X57 for possible use as parameters in the given variable (they may be ignored). Note that X44 must be in milliseconds if Cycle is 0.
h. FORM 9 - PROCESSOR DESCRIPTION

<table>
<thead>
<tr>
<th>Form</th>
<th>Processor Unit</th>
<th>Speed Factor</th>
<th>Class</th>
<th>Interrupts</th>
<th>Task Switch Period</th>
<th>Virtual Machine</th>
<th>Connected Memory Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>nn</td>
<td>nnn.</td>
<td>nn</td>
<td>n</td>
<td>nnn</td>
<td>n</td>
<td>nn nn ... (to a maximum of 20)</td>
</tr>
<tr>
<td>E.G.</td>
<td>9 1</td>
<td>1.5</td>
<td>10</td>
<td>5</td>
<td>2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>9</td>
<td>2</td>
<td>0.9</td>
<td>11</td>
<td>0</td>
<td>4</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**Processor Unit**  
The number of the processor being described.

**Speed Factor**  
The ratio of the processor operating speed to a nominal rate of 1 instruction per microsecond; e.g., "1.5" indicates a processing rate of 1,500,000 instructions per second.

**Class**  
A number used to match routines (see Form 3) with appropriate processors; classes 1 through 9 have related capabilities such that 1 is a subset of 2, 2 is a subset of 3, etc. There are no implied capability relations concerning classes 10, 11, etc.

**Interrupts**  
A number which indicates the types of interrupts to which the processor can respond:
- 0 - none
- 1 - I/O
- 4 - job and task initiation requests
- 5 - all

**Task Switch Period**  
The time (in milliseconds) required for the processor to drop one task and commence another, as a consequence of an interruption.

**Virtual Machine**  
The number of the virtual machine (see Form 14) to which the processor belongs.

**Connected Memory Units**  
The numbers of memory units (see Form 7) which are addressable by the processor; all of the memory units must belong to the same virtual machine as the processor.
### 1. FORM 10 - DATA LINK DESCRIPTION

<table>
<thead>
<tr>
<th>Form</th>
<th>Data Link</th>
<th>Mode</th>
<th>Transmission Rate</th>
<th>Time Lag</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>nnn</td>
<td>n</td>
<td>nnnnn.</td>
<td>nnn.</td>
</tr>
<tr>
<td>E.G.</td>
<td>10</td>
<td>5</td>
<td>10</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>306</td>
<td>2</td>
<td>0</td>
</tr>
</tbody>
</table>

**Data Link**
- If less than 100, this field contains the number of a half-duplex communication channel. If greater than 100, it signifies a multiplexed set of half-duplex subchannels; the set number is given by the 100's digit, and the number of subchannels in the set is given by the last two digits (e.g., "230" would define a multiplexed channel number 2, consisting of 30 subchannels).

**Mode**
- Applies only to multiplexed data links:
  - 0 - the subchannels are completely independent of each other.
  - 1 - the channel will operate in "burst mode" if any of its subchannels is subjected to a load in excess of the specified transmission rate. This will cause interruption of any other transmissions in progress on the data link, and may result in data loss.

**Transmission Rate**
- The maximum rate (in characters/millisecond) at which the link operates; in the case of a multiplexed channel, it is the rate for each subchannel.

**Time Lag**
- The period (in milliseconds) between sending and receiving one unit of data.
j. **FORM 11 - DATA SET DEFINITION**

<table>
<thead>
<tr>
<th>Form</th>
<th>Data Set</th>
<th>Storage</th>
<th>Organization</th>
<th>Initial Size</th>
<th>Maximum Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>nn</td>
<td>nn</td>
<td>n</td>
<td>nnnnnnnnn</td>
<td>nnnnnnnnn</td>
</tr>
<tr>
<td>E.G.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>1000000</td>
</tr>
<tr>
<td>11</td>
<td>66</td>
<td>12</td>
<td>1</td>
<td>10000</td>
<td>5000000</td>
</tr>
</tbody>
</table>

**Data Set**  
The number of the data set being defined.

**Storage**  
The number of the storage unit (see Form 8) on which the data set resides.

**Organization**  
0 - the data set is serially addressed.  
1 - the data set is randomly addressed.

**Initial Size**  
The number of characters in the data set when simulation commences.

**Maximum Size**  
The maximum space (in characters) reserved for the data set on the specified storage unit.
k. **FORM 12 - CONFIGURATION SPECIFICATIONS**

<table>
<thead>
<tr>
<th>Form</th>
<th>Unit</th>
<th>Data Link Connections</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>nnnn</td>
<td>nnn nnn nnn ... (to a maximum of 96)</td>
</tr>
<tr>
<td>E.G.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>60002</td>
<td>1 23 73 202 203</td>
</tr>
<tr>
<td>12</td>
<td>70011</td>
<td>200 300</td>
</tr>
<tr>
<td>12</td>
<td>80006</td>
<td>5 6 7 8 9</td>
</tr>
</tbody>
</table>

**Unit**
A 5-digit identifier of a memory unit (see Form 7), a storage unit (see Form 8), or a device (see Form 6) which is to be connected to specified data links (e.g., 60002 specifies device 2).

**Data Link Connection**
The numbers of data links (see Form 11) to which the given unit can be connected for message transmission. Independent channels are represented by their respective numbers. A particular subchannel of a multiplexed channel is represented by specifying the set number of the channel as the 100's digit, and the ordinal number of the subchannel in the set as the last two digits (e.g., 209 for the ninth subchannel of set 2); all subchannels of a multiplexed channel are represented by the set number as the 100's digit and 00 for the last two digits.

Any units which do not share some data link can be assumed to share an implicit link for the purpose of message transmission (see Form 13, Algorithm 48).
1. **FORM 13 - ALGORITHM SELECTION**

<table>
<thead>
<tr>
<th>Form</th>
<th>Algorithm 1</th>
<th>Algorithm 2</th>
<th>Algorithm 3</th>
<th>Algorithm 4</th>
<th>Algorithm 5</th>
<th>Algorithm 6</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Transmission Path Selection:</td>
<td>Memory Allocation:</td>
<td>Task Scheduling:</td>
<td>Unit Selection:</td>
<td>Element Loading:</td>
<td>I/O Service:</td>
</tr>
<tr>
<td></td>
<td>A = 0 If all suitable links are in use, choose the first one and wait.</td>
<td>A = 0 Element (i.e., routine and data block) confiscation is not permitted.</td>
<td>A = 0 Processing is not interruptible.</td>
<td>A = 0 No special treatment for critical tasks.</td>
<td>A = 0 Do not use a processor to perform loading service.</td>
<td>A = 0 Do not use a processor for I/O initiation or I/O interrupt response.</td>
</tr>
<tr>
<td></td>
<td>A = 1 If all suitable links are in use, wait until one becomes available.</td>
<td>A = 1 If critical tasks are being considered (See Algorithm 3B), they may confiscate elements or space.</td>
<td>A = 1 Processing is interruptible by the executive and critical tasks.</td>
<td>A = 1 If critical tasks are being considered (See Algorithm 3B), they may confiscate nonsharable devices and storage units.</td>
<td>A = 0 Do not use a processor to perform loading service.</td>
<td>A = 1 Use a processor to initiate I/O and to respond to I/O interrupts.</td>
</tr>
<tr>
<td></td>
<td>B = 0 Choose the first suitable link which is not in use; if all are in use, see Algorithm 1A.</td>
<td>B = 0 Consolidate space whenever an element is no longer needed.</td>
<td>B = 0 Task criticality is not considered; i.e., all tasks are treated as noncritical.</td>
<td>B = 0 Choose a virtual machine for a task without regard to explicit data link connections; i.e., implicit links are to be assumed.</td>
<td>B = 0 Place elements in memory without transmitting loading messages.</td>
<td>B = 1 Load elements by transmitting from library data sets to memory.</td>
</tr>
<tr>
<td></td>
<td>B = 1 Choose the first suitable link whether or not it is in use.</td>
<td>B = 1 Consolidate space only when required for loading additional elements.</td>
<td>B = 1 Critical tasks have precedence and confiscation privileges over noncritical tasks in obtaining processors if interruptions are permitted (See Algorithm 3A).</td>
<td>B = 1 Select a virtual machine for each task which permits all messages associated with the task to be transmitted over explicit data links; i.e., implicit links are not allowed.</td>
<td>B = 1 Load elements by transmitting from library data sets to memory.</td>
<td>B = 1 Load elements by transmitting from library data sets to memory.</td>
</tr>
<tr>
<td></td>
<td>C = 0 Elements may coreside in pages.</td>
<td>C = 0 Elements may coreside in pages.</td>
<td>C = 0 Scheduling is on a cyclic basis; i.e., tasks are placed in time-ordered queues for execution.</td>
<td>C = 1 Scheduling is by task priority.</td>
<td>C = 0 Elements may coreside in pages.</td>
<td>C = 0 Elements may coreside in pages.</td>
</tr>
<tr>
<td></td>
<td>C = 1 Each element must start on a new page.</td>
<td>C = 1 Each element must start on a new page.</td>
<td>C = 1 Scheduling is by task priority.</td>
<td>C = 1 Scheduling is by task priority.</td>
<td>C = 0 Elements may coreside in pages.</td>
<td>C = 0 Elements may coreside in pages.</td>
</tr>
<tr>
<td></td>
<td>D = 0 Inhibit space consolidation.</td>
<td>D = 0 Inhibit space consolidation.</td>
<td>D = 0 Inhibit space consolidation.</td>
<td>D = 0 Inhibit space consolidation.</td>
<td>D = 0 Inhibit space consolidation.</td>
<td>D = 0 Inhibit space consolidation.</td>
</tr>
<tr>
<td></td>
<td>D = 1 Permit space consolidation.</td>
<td>D = 1 Permit space consolidation.</td>
<td>D = 1 Permit space consolidation.</td>
<td>D = 1 Permit space consolidation.</td>
<td>D = 1 Permit space consolidation.</td>
<td>D = 1 Permit space consolidation.</td>
</tr>
<tr>
<td></td>
<td>E = 0 Consolidate space only to meet a requirement.</td>
<td>E = 0 Consolidate space only to meet a requirement.</td>
<td>E = 0 Consolidate space only to meet a requirement.</td>
<td>E = 0 Consolidate space only to meet a requirement.</td>
<td>E = 0 Consolidate space only to meet a requirement.</td>
<td>E = 0 Consolidate space only to meet a requirement.</td>
</tr>
<tr>
<td></td>
<td>E = 1 Consolidate space in total for a virtual machine whenever a requirement cannot be met for element loading.</td>
<td>E = 1 Consolidate space in total for a virtual machine whenever a requirement cannot be met for element loading.</td>
<td>E = 1 Consolidate space in total for a virtual machine whenever a requirement cannot be met for element loading.</td>
<td>E = 1 Consolidate space in total for a virtual machine whenever a requirement cannot be met for element loading.</td>
<td>E = 1 Consolidate space in total for a virtual machine whenever a requirement cannot be met for element loading.</td>
<td>E = 1 Consolidate space in total for a virtual machine whenever a requirement cannot be met for element loading.</td>
</tr>
</tbody>
</table>
### FORM 14 - VIRTUAL MACHINE DEFINITION

<table>
<thead>
<tr>
<th>Form</th>
<th>Virtual Machine</th>
<th>Executive Memory Unit</th>
<th>Virtual Memory</th>
<th>Size</th>
<th>Page Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>14</td>
<td>n</td>
<td>nn</td>
<td>nnnnnnnn</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E.G.</td>
<td>14</td>
<td>1</td>
<td>100000</td>
<td>1000</td>
<td></td>
</tr>
<tr>
<td></td>
<td>14</td>
<td>2</td>
<td>120000</td>
<td>500</td>
<td></td>
</tr>
</tbody>
</table>

**Virtual Machine**

A number between 1 and 6, indicating the virtual machine being defined.

**Executive Memory Unit**

The number of the memory unit (see Form 7) in which the simulated executive for the virtual machine (i.e., routine 30001 and data block 40001) will reside. It must be a memory which is connected to a class 1 processor (see Form 9) for the machine, since that is required for execution of the executive.

**Virtual Memory**

Size is the total number of addressable characters in the composite of memory units for the virtual machine. Page Size is the number of characters per addressable page of memory.
5.1.3.5 Preparation of a Job Schedule. The Job Schedule provides the means to initiate jobs, add job and task definitions, modify or add system specifications, and specify events through setting of Savex Cells.

The formats for scheduling must conform to the same rules that apply to specification forms. Each initiation is represented by a line of input, of which only the first 70 positions are relevant.

A double prime ("'") in positions 1 and 2 or a quotation mark (""") in position 1 indicating that the line is a comment, as specified in paragraph 5.1.3.4 - Preparation of Model Specifications, can also be used for the job schedule. All input lines are interpreted on a free-field basis, i.e., one or more spaces separate successive fields.

The Job Schedule is read during simulation and forms should be ordered on the time field (i.e., the first field). No job or event should be scheduled to start before simulated time 20 since a line which begins with a number less than 20 is treated as a specification form. The executive is automatically started and should not have a job initiation in the schedule.
## JOB INITIATION

<table>
<thead>
<tr>
<th>Time</th>
<th>Job</th>
<th>Trigger Message</th>
<th>Repeat Flag</th>
</tr>
</thead>
<tbody>
<tr>
<td>nnm</td>
<td>nn</td>
<td>nn</td>
<td>n</td>
</tr>
<tr>
<td>E.G.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>150</td>
<td>2</td>
<td>28</td>
<td>0</td>
</tr>
<tr>
<td>160</td>
<td>3</td>
<td>12</td>
<td>1</td>
</tr>
<tr>
<td>210</td>
<td>5</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Time**: The time (in milliseconds) at which the job is to introduced to the system.
- **Job**: The number of the job (see Form 1) to be initiated.
- **Trigger Message**: If this field is specified, it must contain the number of a message (see Form 5) which must complete transmission after the given time, in order to start the job. If unspecified, the job will be started immediately.
- **Repeat Flag**: Applicable only if a trigger message is specified:
  - 0 - the job is initiated once, following the next completion of the transmission of the specified message.
  - 1 - the job is to be initiated following every occurrence of the specified message transmission.

**Example**: 150 2 28 0
### EVENT OCCURRENCE

<table>
<thead>
<tr>
<th>Time</th>
<th>0</th>
<th>Events</th>
<th></th>
<th>Event K</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Savex</td>
<td>Increment</td>
<td>Savex</td>
<td>Increment</td>
</tr>
<tr>
<td>nnnnn</td>
<td>0</td>
<td>nnnn</td>
<td>nnn</td>
<td>nnnn</td>
<td>nnn</td>
</tr>
<tr>
<td>E.G.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1800</td>
<td>0</td>
<td>688</td>
<td>+2</td>
<td>681</td>
<td>10</td>
</tr>
<tr>
<td>1950</td>
<td>0</td>
<td>680</td>
<td>1</td>
<td>681</td>
<td>1</td>
</tr>
<tr>
<td>1960</td>
<td>0</td>
<td>688</td>
<td>-1</td>
<td>681</td>
<td>1</td>
</tr>
</tbody>
</table>

- **Time**: The time (in milliseconds) at which the indicated events occur. It must be greater than 19.
- **Savex**: The number of the Savex cell associated with the event.
- **Increment**: The amount by which the Savex cell is to be changed.
5.1.4 Overall Approach

In coordination with NASA a simulation model version was developed for the Space Shuttle, reflecting the hardware characteristics and the functions to be performed during the Approach and Landing Test (ALT) of the Space Shuttle Orbiter.

Hardware parameters were extracted from NASA Computer Program Development Specifications, from IBM Functional and Technical Descriptions, and from Rockwell International Functional Subsystem Requirements documentation. These parameters are discussed in detail in paragraph 5.2.3.

Characteristics relating to the expected performance of software programs, modules, and cyclic executives have been based largely on the ALT Functional Design Specifications by IBM that describe the functions performed during the various major modes of the ALT configuration, the cyclic executive processors and the Specialist functions. Refined timing of the execution phase of each routine was derived by determining the execution time for each set of instructions that operate under certain specified conditions, based on the instruction execution times given in References 26 through 28 and execution times given in Appendix D of Volume 2, Part I (Table D-2), of Reference 19 and Appendix D (Table D-2) of Volume 2, Part 3, of Reference 19.

5.1.4.1 Approach to Hardware Definition. The model consists of the entities listed below.

Certain entities are simulated separately as their characteristics and functions are distinct and logically different even though they are physically constructed as a unit, e.g., the GPCs are logically depicted as consisting of a CPU, a Core Memory, and an IOP.

The number in parentheses indicates the IMSIM specification number as explained in paragraph 5.1.3 and corresponds to the number on the diagram in Figure 2-1.

a. Four Space Shuttle Advanced System/4Pi Model AP-101 Central Processing Units (90001, 90002, 90003, 90004).
b. Four GPC/IOP combined Main Memories, containing 65.5K words each (262K bytes each) (70001, 70002, 70003, 70004).
c. Four Input/Output Processors (IOP) with 24 channels each.
d. Mass Memory consisting of a tape controller and two Mass Memory tapes, each tape with a capacity of 134 X 10^6 bits (17,000,000 characters) (80001, 80002).
e. Four Display Electronic Units (DEU) (60001, 60002, 60003, 60004).
f. Four Display Units (DU) (60005, 60006, 60007, 60008).
g. Three Keyboard Entry Units (KB) (60027, 60028, 60029).
h. Eight Multiplexer/Demultiplexer units (MDM) for flight critical functions (60009, 60010, 60011, 60012, 60013, 60014, 60015, 60016).
i. Three Display Driver Units (DDU) (60017, 60018, 60019).
j. Two Pulse Code Modulator Master Units (PCMMU) (60095, 60096).
k. Seven Multiplexer/Demultiplexers (MDM) for forward and aft operational instrumentation (60020, 60021, 60022, 60023, 60024, 60025, 20026).
l. Twenty-seven data link buses grouped by function 100001 through 100027).
m. Eleven half-duplex data links for interdevice communications (100028 through 100038).

Each of the above items is described in detail in paragraph 5.2.3.2.

A diagram of the simulated configuration for ALT is given in Figure 2-1 contained in Section 2.1 of the Summary, and depicts the hook-up of these elements.

5.1.4.2 Approach to Workload Definition. The software requirements for the Space Shuttle Orbiter onboard digital data processing system specify a hierarchical system to be constructed according to established techniques of structured programming. The activity within an individual computer of the DDPS essentially consists of a set of tasks which may be performed concurrently (i.e., multitasking) and which compete with each other for use of the central processor. The tasks are assigned unique priorities to be used in resolving conflicts over the CPU, and they are scheduled either by time pulses or by the occurrence of specific events. All input/output control is confined to certain "executive" tasks and is handled by input/output processors (IOP), thereby relieving the CPU of these specialized functions.

Definition of an IMSIM workload to represent this activity necessitated:

a. establishment of specific objectives for simulation,
b. an understanding of the organization and intercommunication of the software,
c. information and assumptions concerning the amount of computing and data transmission performed as a function of the state of the system,
d. value judgments as to relative significance of functions, events, states, etc., to the simulation objectives, and
e. methods to be used for representation of each of the significant aspects of the system.

These five areas of concern were interdependent and had to be treated in parallel; for example, it is impractical to gather detailed information and make assumptions about a software module which is essentially irrelevant to simulation goals. Simulation objectives were tentatively established and are presented in Sections 5.1.1 and 5.1.2. The methods for software representation
are described in Section 5.2.3.3. Since virtually all of the activity within the DDPS is organized into schedulable "processes", these processes are identified, together with the conditions for activating them, and the program modules which are executed for them. The processes are associated with four areas: User Interface, System Control, Guidance Navigation and Control, and Systems Management.

5.1.4.2.1 User Interface Processes. Six User Interfaces processes were considered for representation. They are identified by the principal modules as follows:

a. DCI_CYC_DISPLAY - Cyclic Display Processing
   Scheduled for execution at 100 ms intervals.
   Other modules called include:
   DCI#FMT - Data Formatting
   DCI#CON - Data Conversion

b. DCS_SYNC - GPC/PCMMU Data Lile Synchronizer
   Scheduled by DDC when a GPC initialized or on user request
   for synchronization of data cycles. It enables DCD for call
   by AIE.

c. DDC_DWN_LST_CONTROLS - Downlist Data Controls Processor
   Scheduled to execute on an undetermined time interval.

d. DGI_LDB_IO - Launch Data Bus I/O Processor
   Scheduled to execute on an undetermined time interval.
   Other modules called include:
   DLM_LDB_ROUT - LDB Message Router
   DMM_MCDS_PROCESS - MCDS Message Processor

e. DMC_SUPER - User Interface Control Supervisor
   Performed whenever events indicate MDCS or ICC messages, or an
   applications service request, or completion of MM I/O service.
   Other modules called include:
   DMC FUNCTIONS - Keyboard Functions
   DMC_SEQ_REQ_PROC - Sequence Request Processing
   DMC_APP_INT - Application Control Interface
   DMC_MCDS_CNT - MCDS Display Control
   DMC_NEW_DISPLAY - New Display Processing
   DMC_APP_KEY_PROCESS - Application Keys Processing
   DIM_ICC_COLLECTOR - ICC Message Collector

f. DMI_MCDS_IN - MCDS Input Processor
   Scheduled to execute at 200 ms intervals.
   Other modules called include:
   DMM_MCDS_PROCESS - MCDS Message Processor
5.1.4.2 System Control Processes. Eleven System Control processes were considered for representation. They are identified by their principal modules as follows:

a. **AIE SIP** - System Software Interface Processor
   Scheduled to execute at 40 ms intervals on all GPCs for synchronization and ICC.
   Other modules called include:
   - **DCD DOWNLIST** - CPC Downlist Formatter
   - **DIN ICC COLLECTOR** - ICC Message Collector
   - **DME ICC ROUT** - ICC Message Router
   - **DLA LIGHT ALARM PROC** - Lights and Alarm Processing

b. **AIG DEU LOADER** - DEU Loader
   Scheduled for execution only during IPL or SMB to load a DEU.

c. **ARA GPC SWITCH** - GPC Switch Monitor
   Scheduled to execute at 1000 ms intervals to monitor switches and adjust system state.
   Other modules called include:
   - **DMS MSG LSF** - Message Line Support Function
   - **DIM ICC COLLECTOR** - ICC Message Collector

d. **ASA IDLE_SPEC** - Idle Specialist Function (SPEC 0-00)

e. **ASB RD/WRT** - Read/Write Specialist Function

f. **ASC TIME MGMT** - Time Management Specialist Function

g. **ASD DATA CONTROL** - Data Control Specialist Function
   Not invoked during Mated/Drop Test

h. **AIB GPC LOCATOR** - GPC Locator

i. **ARB IDLE OPS** - Idle Operational Sequence

j. **ARC GPC RECONFIG** - GPC Reconfiguration

k. **ARH SEC GPC RECONFIG** - Secondary GPC Reconfiguration
   Not scheduled during Mated/Drop Test

5.1.4.2.3 Guidance, Navigation, and Control Processes. Twenty-two GN&C processes were considered for representation. They are identified by their principal modules as follows:

a. **GAA OPS2 MATED DROP TEST** - Mated/Drop OPS Control Segment
   Scheduled via UI to process requests related to GNC OPS 2.
   Other modules called include:
   - **ARF DPS CONFIG_ITEM** - DPS Configuration Item Processor
   - **GKR RM CONT KYBD_PROC** - RM-Control Keyboard Processor
b. GAD_MATE_IDLE - Mated/Drop Test Idle Mode
Scheduled to execute at 40 ms intervals while Mode 200 prevails.

Other modules called include:
- GBM_IMU_BYTE - IMU Byte Processing
- GMC_ACP_ACUM - IMU Accelerometer Accumulation
- GMD_RES_PROC - IMU Resolver Processor
- GMC_FLT_ATT - IMU Flight Attitude Processor
- GMD_CYO_TORQ - IMU Gyro Torquing
- GRC_NAVAID_SF - FDI NAVAID Selection Filter

c. GAV_OPS1_PREFLT - Preflight OPS Control Segment
Scheduled via UI to process requests related to GNC OPS 1.
Not invoked during Mated/Drop Test.

d. GEF_FC_EXEC - Fast Cycle Executive
Scheduled to execute at 40 ms intervals for Preflight and Mated/Drop Test Flight Control except during idle modes.

Other modules called include:
- GCA_PITCH_CE - FCS Pitch Control
- GCB_ROLL_CE - FCS Roll/Yaw Control
- GCC_BODY_CE - FCS Body Flap Control
- GCD_ELVT_CE - FCS Elevator Auto Control
- GCF_ELVT_MD_CE - FCS Elevator Man/Dir Control
- GGF_ELVT_CAS_CE - FCS Elevator CAS Control
- GCH_ALRN_AUTO_CE - FCS Aileron Auto Control
- GCH_ALRN_MD_CE - FCS Aileron Man/Dir Control
- GCI_ALRN_CAS_CE - FCS Aileron CAS Control
- GCJ_RDR_AUTO_CE - FCS Rudder Auto Control
- GCJ_RDR_MD_CE - FCS Rudder Man/Dir Control
- GCL_RDR_CAS_CE - FCS Rudder CAS Control
- GMC_NW_CE - FCS Nosewheel Control
- GCO_SYS_CHKOUT - FCS Checkout (from GCR)
- GCS_SCHED_GAINS - FCS Schedule Gains - Control Laws
- GPN_DP_1 - FCS Data Processing 1
- GPO_DP_2 - FCS Data Processing 2
- GPP_CMDS_PROC - FCS Commands Processor

e. GEN_MATE_DROP_EXEC - Mated/Drop Executive
Scheduled to execute at 80 ms intervals during active modes of OPS 2.

Other modules called include:
- GDA_DED_DISP_PROC - Dedicated Display Processor
- GDB_AVI_AMI_PROC - Dedicated Display AVVI, AMI Processor
- GDE_ADI_PROC - Dedicated Display ADI Processor
- GDF_HSI_PROC - Dedicated Display HSI Processor
f. GEN_TAEM NAV_CYC - TAEM Navigation Cyclic Executive
Scheduled to execute at 2000 ms intervals following platform release request.
Other modules called include the Navigation Executive (GNE) and the navigation modules called for GEM, plus:

GN2_INFLT_HARDSTAND - Navigation Inflight/Hardstand Update
GN4_COV_RECONFIG - Navigation State and Covariance Reconfiguration
GN5_AVG_G_DP - Navigation Double Precision Average G
GN6_COV_PROP - Navigation Covariance Matrix Propagation

**g. GEP_PRE_FLT_EXEC - Preflight Executive**
Scheduled to execute at 80 ms intervals during the preparation mode (101) of OPS 1.

Other modules called include:
GDA_DED_DISP_PROC - Dedicated Display Processor
GDZ_DISP_PROC - CRT Display Processor
GMH_IMU_MODING - IMU Moding
GPA_ADTA_DATA_PROC - ADTA Data Processor
GPM_MBSLS_DATA_PROC - MSBLS Data Processor
GPR_RA_DATA_PROC - Radar Altimeter Data Processor
GPT_TACAN_DATA_PROC - TACAN Data Processor
GRE_FIDR - FDI Sequencer
plus FDI sequencer modules as for GEM

**h. GET_NAV_TRANS - Navigation Rate/Mode Transition Task**
Scheduled for execution when the Navigation Transition event occurs.

**i. GMA_MIN_EXEC - Minor Cycle Executive**
Scheduled to execute at 40 ms intervals during the preparation mode of OPS 1 and during the Mated/Drop Test unless the idle mode is entered while the platform is not released.

Other modules called include:
GM8_IMU_BITE - IMU Bite Processing
GMC_ACP_ACUM - IMU Accelerometer Accumulator
GMD_RES_PROC - IMU Resolver Processor
GMF_GYO_TORQ - IMU Gyro Torquing

**j. GMG_MAJ_EXEC - IMU Major Cycle Executive**
Scheduled to execute at 320 ms intervals when specified IMU functions are to be performed.

Other modules called include:
GMH_ACP_COMP - IMU Accelerometer Compensation
GMT_T_UPDATE - IMU Transform Update
GMJ_TOR_TRSF - IMU Torquing Transform
GMK_GYO_COMP - IMU Gyro Compensation
GML_ACP_TRSF - IMU Accelerometer Pulse Transform
GMM_LATFUNC - IMU Large Angle Torquing
GMQ_LSF_FILR - IMU Least Squares Filter
k. GMS IMU ATT - IMU Attitude Determination  
   Scheduled by SPEC GUC to control tilt estimation via GMG. It  
   waits for the function to complete.  

   Other modules called include:  
   GMP_TNB_CL - IMU Nav Base-to-Cluster Transform  

l. GMT PFLT CALA - IMU Preflight Calibration A  
   GMU HANG CALA - IMU Hangar Calibration A  
   GMV HANG CALB - IMU Hangar Calibration B  
   Any of which is scheduled by SPEC GUC to control cluster positioning via GMG. It waits for the function to complete.  

m. GMX GC ALIGN - IMU Gyrocompass Alignment  
   Scheduled by SPEC GUC to control gyrocompass alignment via GMG. It waits for the function to complete.  

n. GMY VEL TILT - IMU Velocity and Tilt  
   Scheduled by SPEC GUC for execution upon completion of GMX.  

o. GTX DD CKOUT - DD Dedicated Display Checkout  
   Scheduled to execute at 1000 ms intervals by SPEC GUC.  

p. GUA HORIZ SIT - Horizontal Situation Control Segment  
   Scheduled by UI upon request for horizontal situation display.  

q. GUB VERT SIT - Vertical Situation Control Segment  
   Scheduled by UI upon request for vertical situation display.  

r. GUC IMU OPRTNS - IMU Operations Control Segment  
   Scheduled by UI upon request for IMU functions.  

s. GUG FCS DD CKOUT - FCS/Dedicated Display Checkout Control Segment  
   Scheduled by UI upon request for FCS/Dedicated display checkout.  

t. GUH RM NAV - RM-NAV Control Segment  
   Scheduled by UI upon request for RM-NAV functions.  

u. GUI RM CONT - RM-CONT Control Segment  
   Scheduled by UI upon request for RM-CONT functions.  

   Other modules called include:  
   GKR RM CONT_KYBD_PRO - RM-Control Keyboard Processor  

v. GUK NAV TRGT UPDT - NAV/TARGET Update Control Segment  
   Scheduled by UI upon request for NAV/TARGET update.
5.1.4.2.4 Systems Management Processes. Eleven SM processes were considered for representation. They are as follows:

a. SDA DATA ACQUISITION - Data Acquisition
   Scheduled to execute at 50 ms intervals.

b. SDM PERFORM MON CONTROL - Performance Monitoring Control
   Scheduled to execute at 500 ms intervals.
   Other modules called include:
   SFD_FAULT DETECT ANNUN - Fault Detection & Annunciation
   SPP_PRECON_PROCESS - Precondition Processing
   SSC_SPECIAL COMP - Special Computations
   SAS_ANALOG_SCALE - Analog Scaling

c...g. Five Specialist functions which are not invoked during Mated/Drop Test.

h. Pretakeoff SCM Specialist Function

i. Predrop SCM Specialist Function
   Scheduled by UI upon request for subsystem configuration monitoring.
   Includes the module:
   SPM_SUBSYS_CONFIG_MON - Subsystem Configuration Monitoring

j. SPO PREFLIGHT OPS - SM Preflight Operational Sequence
   Scheduled via UI to process requests related to SM OPS1, not invoked during Mated/Drop Test.

k. SPO FLIGHT OPS - SM Flight Operational Sequence
   Scheduled via UI to process requests related to SM OPS 2.
   Other modules called include:
   SSC_SPECIAL COMP - Special Computations
   SPP_PRECON_PROCESS - Precondition Processing
   SAS_ANALOG_SCALE - Analog Scaling
   SFD_FAULT_DETEC ANNUN - Fault Detection & Annunciation
   SPM_SUBSYS_CONFIG_MON - Subsystem Configuration Monitoring

5.1.4.2.5 Representation of Processes for Simulation. The DDPS processes listed in the preceding sections have the following common operational characteristics: Each is activated by external stimuli (specific events and/or clock pulses) by assigning a CPU to the process on a priority basis; each is subject to interruption for transfer of its assigned processor to a process of higher priority; each process involves the execution of one or more modules of code which are resident in main memory; and, computation associated with performing a process is a function of the state of the system at the time the process is invoked. These characteristics can all be satisfactorily incorporated in the DDPS model if the processes are represented as IMSIM "tasks".
Each task is assigned to a "service class" and given a working "priority" within the class to create a precedence series which correlates with that of the actual DDPS process priorities. Processes which recur at regular time intervals are designated as "cyclic" tasks. The modules which are executed in performing a process are defined as "routines" and may be included or shared among several tasks by declaring them to be elements of specific tasks. DDPS data transmissions are defined as IMSIM "messages"; these are also declared to be elements of appropriate tasks.

IMSIM has been augmented with logic for the representation of significant DDPS events and the maintenance of a system state vector. These are employed in the definition of "GO-NoGo" functions and "Computation Time" functions. The former are used to control the activation of tasks and the latter are evaluated when a task is activated to determine the amount of computing to be simulated for the represented process. The Computation Time functions are actually associated with routines rather than tasks, and therefore, when a task is activated, the functions for all routines which are elements of the task are evaluated and the results summed.

A detailed description of the represented events and state vector is presented in Section 5.2.4.

5.1.4.3 Approach to Simulated Time-Line Segments (JOBSCHEDULES). The first set of time-line segments, hereafter called "JOBSCHEDULES", was developed for the purpose of exercising the model and taking the model through all phases of flight to exercise all software functions. The set started at simulated time 0 with preflight conditions and continued through Mated Flight, Separation, TAEM, Approach & Landing, and Rollout. The purpose was to determine if any significant problems developed during any of the phases.

A second set of JOBSCHEDULES was developed based on the fact that the heaviest workload occurs at 16-second intervals, when all cyclic processors, executives, and programs are competing for the CPU. This will occur when the tasks that are cyclic at 40 ms, 50 ms, 80 ms, 100 ms, 200 ms, 320 ms, 500 ms, 1000 ms, and 2000 ms all culminate at 16-second intervals. The purpose was to determine if any significant problems developed during a concentration of functions at a given time.

A third set of JOBSCHEDULES was developed based on different flight segments during ALT, such as Mated Flight and Separation, Postseparation and TAEM, TAEM and Approach & Landing, and Rollout. The purpose here was to determine if any significant problems developed during flight segments.

A fourth set of JOBSCHEDULES with four jobs was developed based on the simulation of four different Virtual Machines. The purpose was to determine that operation with four active GPCs did not result in problems not discovered in the previous set of runs.

Events based on manual actions (Specialist Functions) were incorporated in each of these JOBSCHEDULES and are detailed in paragraph 5.2.5.

All these JOBSCHEDULES with the simulated Specialist Functions are discussed in detail in Section 5.2.5.
5.2 TASKS PERFORMED

This section discusses the activities performed under each of the six tasks specified in the Statement of Work.

5.2.1 Data System Requirements Definition (S.O.W. 2.1.1)

All documentation received from NASA was analyzed, and a thorough understanding of the functional requirements for the Space Shuttle Orbiter's hardware and software was gained.

In close coordination with NASA a baseline for the simulation model was established, viz., the Approach and Landing Test (ALT) configuration, with Memory Configuration #2 and Downlist format #1 as established in the Computer Program Development Specification, Volume I. The two Major Functions in this configuration were determined to be Guidance, Navigation & Control (GN&C), and System Management (SM). The Operational Sequences for the model were determined to be GN&C Mated/Drop Test Ops and SM Flight Ops.

The requirements that were defined for the functions to be performed in the model constituted a realistic approach for the IMSIM simulation model.

These requirements were subsequently transformed into a form suitable for IMSIM and resulted in the simulation model version described in paragraphs 5.2.3 and 5.2.4 that accurately reflected the defined requirements for the Orbiter in the ALT configuration.

Details of the Hardware and Software configurations is given in paragraph 5.2.3.

5.2.2 Sensitivity Analysis (S.O.W. 2.1.2)

Following the Data System Requirements Definition Task, and prior to establishing a specific simulation configuration and its operational modes, a sensitivity analysis of the proposed Space Shuttle Orbiter Data Processing Subsystem was conducted. The primary sources of information and data used to conduct the sensitivity analysis were References 6, 7, 12, and 14. From a detailed review of the referenced documents five potential data processing bottleneck problem areas were defined. The potential problem areas were identified as:

a. CPU Utilization
b. IOP lockout of the CPU
c. The GPC/PCMMU interface
d. CPU synchronization
e. Multifunction Display processing
The process by which the five potential problem areas were identified was based on a detailed review of the technical tasks to be performed by the DDPS, the characteristics of the hardware and software to be used in performing these technical tasks, and the operational environment (flight phases, operational modes, etc.) within which the tasks would be required.

The final configuration and operational mode of the IMSIM modeled Orbiter Digital Data Processing Subsystem provided data for only one of the five potential problem areas identified (CPU utilization). However, each potential problem area is discussed in this section to indicate why it was initially identified.

5.2.2.1 CPU Utilization. From a detailed review of the Orbiter DDPS tasks to be performed for various operational modes and the requirement that the CPU be capable of handling cyclic tasks plus randomly generated special tasks, the question of the CPU’s capability to perform all required tasks within an allocated time period was identified as a potential problem area. Following the selection of the ALT configuration with the two major functions of “Guidance, Navigation, and Control” plus “Systems Management” for the IMSIM model, this problem area was selected as the principal problem area to be investigated.

Based upon this decision the IMSIM model described in this report was adapted to investigate the potential CPU utilization problem.

5.2.2.2 IOP Lockout of the CPU. Functional and operating requirements for the IOP define two basic operational modes for IOP-initiated requests for access to main memory. The first is when seven or less requests are stacked in the direct memory access (DMA) queue. For this condition, the IOP accesses main memory during CPU instruction execution by cycle-stealing action. The average time for IOP access to main memory for a single request, for this condition, is 2.5 microseconds.

When there are more than seven IOP requests stacked in the DMA queue, IOP DMA enters a "BURST MODE" of operation. During Burst Mode operation, CPU program execution is stopped and the IOP has exclusive access to main memory. The average main memory access time for each IOP request is 1.4 microseconds for Burst Mode operation. A maximum of 64 consecutive main memory accesses by the IOP are allowed in the Burst Mode. The sixty-fifth consecutive IOP main memory request generates an IOP error condition and an interrupt is sent to the CPU and the Burst Mode is disabled.

There are three types of IOP requests for main memory, these are (1) a request for the next MSC or BCE macroinstruction for program execution, (2) a request for data to be transmitted to Shuttle subsystems, and (3) a request to place data received from Shuttle subsystems into main memory.
The question raised by the above description of the IOP "Burst Mode" is the possibility of limiting CPU access to main memory to a time insufficient to accomplish required processing. This condition could possibly exist if there were repeated sequences of IOP Burst Mode operations.

The IMSIM model established to investigate ALT CPU Utilization was incapable of addressing the potential problem of IOP lockout of the CPU for two reasons. First the ALT configuration does not include major portions of the shuttle orbiter's subsystems. It is the IOP requests to and from main memory for these subsystems that could possibly create the problem. Second, the discrete time unit element of the IMSIM simulation model was one milliscond.

To adequately study the potential IOP lockout problem the simulation would require a time unit resolution of one microsecond.

5.2.2.3 The GPC/PCMMU Interface. The pulse code modulation master unit (PCMMU) is an intermediate data transfer unit between the GPCs and seven operational instrument data subsystems and between the GPCs and the payload data subsystem. Within the total Shuttle Orbiter DDPS, the CPU and the PCMMU are the only devices that can enable multiplexer interface adapter units for the transmission or reception of serial bus data.

Functionally the PCMMU performs the following:

a. Through internal control, it requests input data from the operational instrumentation and payload data subsystems. These data are stored in appropriate PCMMU random access memories.

b. The PCMMU stores data commanded to it from each GPC into toggle buffers and allows any GPC to access all operational instrumentation and payload data.

c. The PCMMU outputs formatted (downlisted) data to a network signal processor which is used to control downlink data.

Operational functions conducted between GPCs and a PCMMU are performed asynchronously within a data cycle which is synchronized between the two units. Because there will be different operational functional requirements between the GPCs and the PCMMU for different operational modes, a potential data processing problem could exist for excessive GPC/PCMMU asynchronous operation and/or for malfunctions of the GPC/PCMMU Data cycle synchronization.

Because the ALT Mated/Drop test does not incorporate the GPC/PCMMU Data Cycle Synchronizer Software, this potential problem area was not investigated.
5.2.2.4 CPU Synchronization. The five GPCs in the Space Shuttle Orbiter are interconnected by serial data buses and can be operated as independent or redundant units. A basic operational design philosophy of the Shuttle Orbiter DDPS is to provide a capability whereby the computations of any one CPU may be verified by other CPUs whenever these CPUs constitute a redundant set. The objective of this capability is to ensure fail-operational and fail-safe system performance during critical flight phases.

To achieve this operational capability, CPU synchronization of all GPCs which constitute a redundant set has been assumed. A potential data processing problem area could be created if CPU synchronization for redundant operations is not maintained.

From the functional design specifications of the DDPS it would appear that adequate hardware and software design considerations have been given to the CPU synchronization requirement. Each GPC contains three real-time clock timers and systems management synchronizing software programs have been functionally defined.

While the possibility of nonsynchronization of CPUs for redundant set operation may have been minimized by the system design, the consequences of its occurrence warrant its consideration as a potential problem area to be studied by simulation. For this reason it was so identified in the sensitivity analysis.

Because the IMSIM Model configured to study CPU Utilization was constructed on the ground rule that only one active GPC need be simulated (because all other GPCs would have identical loading), the problem of CPU synchronization was not addressed. A specific model should be developed to assess this potential problem area. The present model is not appropriate, as it employs a 1 millisecond time unit.

5.2.2.5 Multifunction Display Processing. The multifunction CRT display system has been designed to provide the principal flight crew interface for data entry, subsystem monitoring, program selection, and the presenting of alphanumeric and graphic data displays. A variety of fixed-display formats and types of displays are defined by the software system to be used. It would appear that under normal operating conditions for the various flight tests and operational phases this interacting crew/system design is capable of meeting all requirements and does not constitute a data processing problem. However, for abnormal operating conditions a potential data processing problem could be generated if extensive crew/system interaction is required. Operationally, most displays are stored in mass memory and are updated by the GPCs. For a condition where the number and rate of crew requests for displays is very high, the possibility exists that the combination of GPC operational task processing and GPC display processing could create an Orbital Data Processing System problem.
For the ALT, the extent of crew/system interface is not extensive, and for the durations of the tests, the crew would not be generating a large number of display requests. For this reason, the potential problem of multifunction display processing was not addressed.

It was noted in some simulation runs, however, that manual actions, generated within a 25-millisecond time frame, will cause a disrupt in the calling of the servicing function.

5.2.3 Test Design (S.O.W. 2.1.3)

Based on the results of task 1 - Data System Requirements Definition and task 2 - Sensitivity Analyses, a test design was developed incorporating the findings of the previous studies. The Test Design resulted in:

a. The model generation, described in detail in paragraph 5.2.3.1.

b. The model's adaptation and parameterization, described in detail in paragraph 5.2.4.

c. The job schedule inputs, described in detail in paragraph 5.2.5.

5.2.3.1 Model Generation. This section describes the inputs and required formats for building and parameterizing the IMSIM model. Nine "input specification form" categories (Forms 6 through 14), as described in paragraph 5.1.3, are used for defining the hardware configuration. These inputs are described and listed in Section 5.2.3.2 below.

Five input specification form categories (Forms 1 through 5) are employed in specifying software workload characteristics. These inputs are described and listed in Section 5.2.3.3.

The inputs on these 14 specification forms were assembled for execution in the NASA.SPECS10.DAT and the NASA.SPECS20.DAT files.

A printout of these files is contained in Appendix B.

5.2.3.2 Hardware Simulation. The simulated hardware is described in detail by:

a. Processors

b. Memories

c. Mass Memory Storages

d. Devices

e. Datalinks
The parameters for the hardware simulation were derived from values extracted from the following references:


d. Functional Subsystem Software Requirements System Interface, Volume 6, Parts 1 and 2, Sections 1 through 11, and Appendices A through K, Orbiter 101 (References 12 and 13).

e. Space Shuttle Advanced System/4 Pi - Model AP-101, Central Processor Unit, Technical Description (Reference 15).

5.2.3.2.1 Processors. Four processors were simulated, one for each of the four GPC complexes.

Each of the GPC processors for the IBM 4pi/AP101 computer has a command execution time of 1.4 microseconds (processing speed of 714300 instructions per second) and is designated as belonging to Virtual Machine #1. The 4pi/AP101 central processor can respond to the following interrupts:

- I/O
- Bounds Fault
- Service request

There is no task switch time involved.

Two approaches were used. One approach was to simulate the four GPCs as all belonging to one Virtual Machine. One processor was represented as actively servicing all tasks while the other three processors were operating passively in the redundant mode, assuming to process identical tasks with ICC messages interchanging between GPC memories for synchronization. These specifications are contained in a data set NASA.SPECSIO.DATA. Format description is given in paragraph 5.1.3 and in the IMSIM User's Manual (Reference 2).
The scripted inputs for this approach for the processors on IMSIM specification form 9 were as follows:

```
'CENTRAL PROCESSING UNIT (CPU) NO. 1
  SPEED CLASS INTERRUPT SWITCH VIRT MACH CONNECTED MEMORIES
9  1 0.48 10  5  0  1  1  2  3  4

'CENTRAL PROCESSING UNIT (CPU) NO. 2
  SPEED CLASS INTERRUPT SWITCH VIRT MACH CONNECTED MEMORIES
9  2 0.48 10  5  0  1  2  1  3  4

'CENTRAL PROCESSING UNIT (CPU) NO. 3
  SPEED CLASS INTERRUPT SWITCH VIRT MACH CONNECTED MEMORIES
9  3 0.48 10  5  0  1  3  1  2  4

'CENTRAL PROCESSING UNIT (CPU) NO. 4
  SPEED CLASS INTERRUPT SWITCH VIRT MACH CONNECTED MEMORIES
9  4 0.48 10  5  0  1  4  1  2  3
```

The second approach used was to simulate each of the four processors as belonging to a different Virtual Machine (V.M.). This resulted effectively in each GPC representing a Virtual Machine. All computations were done fourfold and each VM acted independently, except for ICC. The actual output messages for three of the four VMs were suppressed except for the ICC messages, which were transmitted by all four VMs.

These specifications are contained in a data set NASA.SPECS20.DATA. The scripted inputs for this approach for the four processors on IMSIM specification Form 9 were as follows:

```
'CENTRAL PROCESSING UNIT (CPU) NO. 1
  SPEED CLASS INTERRUPT SWITCH VIRT MACH CONNECTED MEMORIES
9  1 0.48 10  5  0  1  1

'CENTRAL PROCESSING UNIT (CPU) NO. 2
  SPEED CLASS INTERRUPT SWITCH VIRT MACH CONNECTED MEMORIES
9  2 0.48 10  5  0  2  2

'CENTRAL PROCESSING UNIT (CPU) NO. 3
  SPEED CLASS INTERRUPT SWITCH VIRT MACH CONNECTED MEMORIES
9  3 0.48 10  5  0  3  3

'CENTRAL PROCESSING UNIT (CPU) NO. 4
  SPEED CLASS INTERRUPT SWITCH VIRT MACH CONNECTED MEMORIES
9  4 0.48 10  5  0  4  4
```
5.2.3.2.2 Memories. Four memories were simulated, one for each GPC. The main memory for each IBM/4pi AP-101 computer has a total capacity of 256K bytes. The main memory access rate was simulated at 750 ns (speedfactor of 1.4 bytes/microsec.). The page size in these memories was simulated at 2048 bytes with a total of 125 pages for each memory.

During the ALT Simulation, Memory Configuration #2 was in core permanently and no other Memory Configurations were required.

ALT Memory Configuration #2 was simulated with GN&C Ops #2 and SM Ops #2 as the Ops Overlays. This ALT Memory Configuration #2 was assumed loaded in all four GPCs.

As memory configurations will all be predetermined prior to flight, no problems were expected as to memory capacity and therefore, no division was simulated for the Major Function GN&C overlay and the Major Function System Management overlay, or the Ops overlays. The size of the routines are therefore also immaterial and a nominal value of 1 was used on the specification forms.

The scripted inputs for the core memories on Form 7 were as follows:

```
MEMORY GPC 1
  SPEED FACTOR      PAGES
  7     1     1.4  .25

MEMORY GPC 2
  SPEED FACTOR      PAGES
  7     2     1.4  125

MEMORY GPC 3
  SPEED FACTOR      PAGES
  7     3     1.4  125

MEMORY GPC 4
  SPEED FACTOR      PAGES
  7     4     1.4  125
```

5.2.3.2.3 Mass Memory Storage. Two Mass Memory Storages were simulated. Both are identical in their characteristics and are simulated as two tape units, each tape with a 17,000,000 byte capacity (134 X10^6 bits). Access time to the unit was simulated as Variable 400 & Variable 399 with a minimum of 0.5 seconds and a maximum of 8 seconds for each tape unit. (See paragraph 5.2.4 for details on these random variables.) Transmission rate for each unit was set for 125 bytes/ms.
The scripted inputs for the mass memory storages on Form 8 were as follows:

<table>
<thead>
<tr>
<th>Mass Memory Storage (MM) No. 1</th>
<th>A/D Share</th>
<th>Cycle</th>
<th>TX Rate</th>
<th>Capacity</th>
<th>Access Period</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>125</td>
<td>17000000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>399 500 0 0 0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Mass Memory Storage (MM) No. 2</th>
<th>A/D Share</th>
<th>Cycle</th>
<th>TX Rate</th>
<th>Capacity</th>
<th>Access Period</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>125</td>
<td>17000000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>399 500 0 0 0</td>
</tr>
</tbody>
</table>

5.2.3.2.4 Devices. The following devices were simulated:

a. Fifteen Multiplexer/Demultiplexers (MDMs) - 60009 through 60016 and 60020 through 60026 - which can be shared among tasks. Maximum record size each can hold was simulated at 1024 bytes.

Input and output rates were simulated at 120 bytes/ms. No reset time required.

The scripted inputs for these units on IMSIM specification Form 6 were as follows:

<table>
<thead>
<tr>
<th>Multiplexer/Demultiplexer (MDM) FF1</th>
<th>A/D Share</th>
<th>Record</th>
<th>Transmission Rate</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF1</td>
<td>9</td>
<td>1</td>
<td>1024</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>120</td>
<td>120</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Multiplexer/Demultiplexer (MDM) FF2</th>
<th>A/D Share</th>
<th>Record</th>
<th>Transmission Rate</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF2</td>
<td>10</td>
<td>1</td>
<td>1024</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>120</td>
<td>120</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Multiplexer/Demultiplexer (MDM) FF3</th>
<th>A/D Share</th>
<th>Record</th>
<th>Transmission Rate</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF3</td>
<td>11</td>
<td>1</td>
<td>1024</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>120</td>
<td>120</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Multiplexer/Demultiplexer (MDM) FF4</th>
<th>A/D Share</th>
<th>Record</th>
<th>Transmission Rate</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF4</td>
<td>12</td>
<td>1</td>
<td>1024</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>120</td>
<td>120</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Multiplexer/Demultiplexer (MDM) FA1</th>
<th>A/D Share</th>
<th>Record</th>
<th>Transmission Rate</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>FA1</td>
<td>13</td>
<td>1</td>
<td>1024</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>120</td>
<td>120</td>
</tr>
<tr>
<td>Multiplexer/Demultiplexer (MDM)</td>
<td>FA2</td>
<td>A/D Share</td>
<td>Record</td>
<td>Transmission Rate</td>
</tr>
<tr>
<td>-------------------------------</td>
<td>------</td>
<td>-----------</td>
<td>--------</td>
<td>-------------------</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CLASS</td>
<td>SIZE</td>
<td>INPUT</td>
</tr>
<tr>
<td>6</td>
<td>14</td>
<td>1</td>
<td>1</td>
<td>1024</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Multiplexer/Demultiplexer (MDM)</th>
<th>FA3</th>
<th>A/D Share</th>
<th>Record</th>
<th>Transmission Rate</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>CLASS</td>
<td>SIZE</td>
<td>INPUT</td>
<td>OUTPUT</td>
</tr>
<tr>
<td>6</td>
<td>15</td>
<td>1</td>
<td>1</td>
<td>1024</td>
<td>120</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Multiplexer/Demultiplexer (MDM)</th>
<th>FA4</th>
<th>A/D Share</th>
<th>Record</th>
<th>Transmission Rate</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>CLASS</td>
<td>SIZE</td>
<td>INPUT</td>
<td>OUTPUT</td>
</tr>
<tr>
<td>6</td>
<td>16</td>
<td>1</td>
<td>1</td>
<td>1024</td>
<td>120</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Multiplexer/Demultiplexer (MDM)</th>
<th>OF1</th>
<th>A/D Share</th>
<th>Record</th>
<th>Transmission Rate</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>CLASS</td>
<td>SIZE</td>
<td>INPUT</td>
<td>OUTPUT</td>
</tr>
<tr>
<td>6</td>
<td>20</td>
<td>1</td>
<td>1</td>
<td>1024</td>
<td>120</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Multiplexer/Demultiplexer (MDM)</th>
<th>OF2</th>
<th>A/D Share</th>
<th>Record</th>
<th>Transmission Rate</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>CLASS</td>
<td>SIZE</td>
<td>INPUT</td>
<td>OUTPUT</td>
</tr>
<tr>
<td>6</td>
<td>21</td>
<td>1</td>
<td>1</td>
<td>1024</td>
<td>120</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Multiplexer/Demultiplexer (MDM)</th>
<th>OF3</th>
<th>A/D Share</th>
<th>Record</th>
<th>Transmission Rate</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>CLASS</td>
<td>SIZE</td>
<td>INPUT</td>
<td>OUTPUT</td>
</tr>
<tr>
<td>6</td>
<td>22</td>
<td>1</td>
<td>1</td>
<td>1024</td>
<td>120</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Multiplexer/Demultiplexer (MDM)</th>
<th>OF4</th>
<th>A/D Share</th>
<th>Record</th>
<th>Transmission Rate</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>CLASS</td>
<td>SIZE</td>
<td>INPUT</td>
<td>OUTPUT</td>
</tr>
<tr>
<td>6</td>
<td>23</td>
<td>1</td>
<td>1</td>
<td>1024</td>
<td>120</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Multiplexer/Demultiplexer (MDM)</th>
<th>OA1</th>
<th>A/D Share</th>
<th>Record</th>
<th>Transmission Rate</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>CLASS</td>
<td>SIZE</td>
<td>INPUT</td>
<td>OUTPUT</td>
</tr>
<tr>
<td>6</td>
<td>24</td>
<td>1</td>
<td>1</td>
<td>1024</td>
<td>120</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Multiplexer/Demultiplexer (MDM)</th>
<th>OA2</th>
<th>A/D Share</th>
<th>Record</th>
<th>Transmission Rate</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>CLASS</td>
<td>SIZE</td>
<td>INPUT</td>
<td>OUTPUT</td>
</tr>
<tr>
<td>6</td>
<td>25</td>
<td>1</td>
<td>1</td>
<td>1024</td>
<td>120</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Multiplexer/Demultiplexer (MDM)</th>
<th>OA3</th>
<th>A/D Share</th>
<th>Record</th>
<th>Transmission Rate</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>CLASS</td>
<td>SIZE</td>
<td>INPUT</td>
<td>OUTPUT</td>
</tr>
<tr>
<td>6</td>
<td>26</td>
<td>1</td>
<td>1</td>
<td>1024</td>
<td>120</td>
</tr>
</tbody>
</table>
b. Four Display Electronic Units (DEUs) - 60001 through 60004 - which can be shared among tasks. Maximum record size each can hold was simulated at 8192 bytes.

Input rate was simulated at 120 bytes/ms and output rate at 62 bytes/ms. No reset time required.

The scripted inputs for these units on IMSIM specification Form 6 were as follows:

<table>
<thead>
<tr>
<th>DISPLAY ELECTRONIC UNIT NO. 1</th>
<th>A/D</th>
<th>SHARE</th>
<th>RECORD</th>
<th>TRANSMISSION RATE</th>
<th>RESET</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>6</td>
<td>1</td>
<td>1</td>
<td>8192</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>62</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DISPLAY ELECTRONIC UNIT NO. 2</th>
<th>A/D</th>
<th>SHARE</th>
<th>RECORD</th>
<th>TRANSMISSION RATE</th>
<th>RESET</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>6</td>
<td>2</td>
<td>1</td>
<td>8192</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>62</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DISPLAY ELECTRONIC UNIT NO. 3</th>
<th>A/D</th>
<th>SHARE</th>
<th>RECORD</th>
<th>TRANSMISSION RATE</th>
<th>RESET</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>6</td>
<td>3</td>
<td>1</td>
<td>8192</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>62</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DISPLAY ELECTRONIC UNIT NO. 4</th>
<th>A/D</th>
<th>SHARE</th>
<th>RECORD</th>
<th>TRANSMISSION RATE</th>
<th>RESET</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>6</td>
<td>4</td>
<td>1</td>
<td>8192</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>62</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

c. Four Display Units (DUs) - 60005 through 60008 - which can be shared among tasks. Maximum record size each can hold was simulated at 8192 bytes. Input rate was simulated at 38 bytes/ms. No reset time required.

The scripted inputs for these units on IMSIM specification Form 6 were as follows:

<table>
<thead>
<tr>
<th>DISPLAY UNIT NO. 1</th>
<th>A/D</th>
<th>SHARE</th>
<th>RECORD</th>
<th>TRANSMISSION RATE</th>
<th>RESET</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>6</td>
<td>5</td>
<td>1</td>
<td>8192</td>
<td>38</td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>DISPLAY UNIT NO. 2</th>
<th>A/D</th>
<th>SHARE</th>
<th>RECORD</th>
<th>TRANSMISSION RATE</th>
<th>RESET</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>6</td>
<td>6</td>
<td>1</td>
<td>8192</td>
<td>38</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>
d. Three Display Driver Units (DDUs) - 60017 through 60019 - which can be shared among tasks. Maximum record size each can hold was simulated as unlimited and the Input and Output rates were simulated at 120 bytes/ms. No reset time required.

The scripted inputs for these units on IMSIM specification Form 6 were as follows:

```
"DISPLAY DRIVER UNIT (DDU) NO. 1"
  A/D SHARE RECORD                TRANSMISSION RATE   RESET
  CLASS SIZE                      INPUT  OUTPUT  PERIOD
6  17  1  1  0                   120    120    0

"DISPLAY DRIVER UNIT (DDU) NO. 2"
  A/D SHARE RECORD                TRANSMISSION RATE   RESET
  CLASS SIZE                      INPUT  OUTPUT  PERIOD
6  18  1  1  0                   120    120    0

"DISPLAY DRIVER UNIT (DDU) NO. 3"
  A/D SHARE RECORD                TRANSMISSION RATE   RESET
  CLASS SIZE                      INPUT  OUTPUT  PERIOD
6  19  1  1  0                   120    120    0
```
e. Three keyboard units (KBUs) - 60027 through 60029 - which can be shared among tasks. No specific record size was simulated. The output rate was simulated at 1 byte/ms with a 1 ms delay.

The scripted inputs for these units on IMSIM specification Form 6 were as follows:

```
"KEYBOARD UNIT (KBU) NO. 1
" A/D SHARE  RECORD  TRANSMISSION RATE  RESET
" CLASS  SIZE  INPUT  OUTPUT  PERIOD
6  27  1  1  0  0  1  1

"KEYBOARD UNIT (KBU) NO. 2
" A/D SHARE  RECORD  TRANSMISSION RATE  RESET
" CLASS  SIZE  INPUT  OUTPUT  PERIOD
6  28  1  1  0  0  1  1

"KEYBOARD UNIT (KBU) NO. 3
" A/D SHARE  RECORD  TRANSMISSION RATE  RESET
" CLASS  SIZE  INPUT  OUTPUT  PERIOD
6  29  1  1  0  0  1  1
```

f. Two Pulse Code Modulation Master Units (PCMMUs) - 60095 and 60096 - which can be used by all tasks. The maximum record size for each unit was simulated at 2048 bytes and the Input and Output rates were simulated at 120 bytes/ms. No delay required.

The scripted inputs for these units on IMSIM Specification Form 6 were as follows:

```
"PULSE CODE MODULATION MASTER UNIT (PCMMU) NO. 1
" A/D SHARE  RECORD  TRANSMISSION RATE  RESET
" CLASS  SIZE  INPUT  OUTPUT  PERIOD
6  95  1  1  2048  120 120 0

"PULSE CODE MODULATION MASTER UNIT (PCMMU) NO. 2
" A/D SHARE  RECORD  TRANSMISSION RATE  RESET
" CLASS  SIZE  INPUT  OUTPUT  PERIOD
6  96  1  1  2048  120 120 0
```
5.2.3.2.5 Datalinks. The following datalinks were simulated in the ALT Configuration depicted in Figure 2-1:

a. Five databuses for intercomputer communication - IC1 through IC5 - (100001 through 100005) with a maximum transmission rate of 1 MHz.

The scripted inputs for these datalinks on IMSIM Specification Form 10 were as follows:

```
''INTERCOMPUTER COMMUNICATIONS DATALINK - IC1
''   MODE TRANSMISSION RATE   TIME LAG
10 1 0 120 0
''
''INTERCOMPUTER COMMUNICATIONS DATALINK - IC2
''   MODE TRANSMISSION RATE   TIME LAG
10 2 0 120 0
''
''INTERCOMPUTER COMMUNICATIONS DATALINK - IC3
''   MODE TRANSMISSION RATE   TIME LAG
10 3 0 120 0
''
''INTERCOMPUTER COMMUNICATIONS DATALINK - IC4
''   MODE TRANSMISSION RATE   TIME LAG
10 4 0 120 0
''
''INTERCOMPUTER COMMUNICATIONS DATALINK - IC5
''   MODE TRANSMISSION RATE   TIME LAG
10 5 0 120 0
''
```

b. Four databuses for Display System communication - DK1 through DK4 - (100006 through 100009) with a maximum transmission rate of 1 MHz.

The scripted inputs for these datalinks on IMSIM Specification Form 10 were as follows:

```
''DISPLAY SYSTEM DATALINK - DK1
''   MODE TRANSMISSION RATE   TIME LAG
10 6 0 120 0
''
''DISPLAY SYSTEM DATALINK - DK2
''   MODE TRANSMISSION RATE   TIME LAG
10 7 0 120 0
''
```
c. Eight databuses for Flight-Critical communication - FC1 through FC8 - (100010 through 100017) with a maximum transmission rate of 1 MHz.

The scripted inputs for these datalinks on IMSIM Specification Form 10 were as follows:

```
'"DISPLAY SYSTEM DATALINK - DK3"
'" MODE TRANSMISSION RATE TIME LAG
10 8 0 120 0
'"DISPLAY SYSTEM DATALINK - DK4"
'" MODE TRANSMISSION RATE TIME LAG
10 9 0 120 0
```

'"FLIGHT CRITICAL BUS DATALINK - FC1"
'" MODE TRANSMISSION RATE TIME LAG
10 10 0 120 0
'"FLIGHT CRITICAL BUS DATALINK - FC2"
'" MODE TRANSMISSION RATE TIME LAG
10 11 0 120 0
'"FLIGHT CRITICAL BUS DATALINK - FC3"
'" MODE TRANSMISSION RATE TIME LAG
10 12 0 120 0
'"FLIGHT CRITICAL BUS DATALINK - FC4"
'" MODE TRANSMISSION RATE TIME LAG
10 13 0 120 0
'"FLIGHT CRITICAL BUS DATALINK - FC5"
'" MODE TRANSMISSION RATE TIME LAG
10 14 0 120 0
'"FLIGHT CRITICAL BUS DATALINK - FC6"
'" MODE TRANSMISSION RATE TIME LAG
10 15 0 120 0
```
d. Two databuses for Mission Critical communication - PL1 through PL2 - (100020 through 100021) with a maximum transmission rate of 1 MHz.

The scripted inputs for these datalinks on IMSIM Specification Form 10 were as follows:

```
''MISSION CRITICAL DATALINK - PL1
''  MODE  TRANSMISSION RATE  TIME LAG
10  20   0       120     0
''MISSION CRITICAL DATALINK - PL2
''  MODE  TRANSMISSION RATE  TIME LAG
10  21   0       120     0
```

e. Two databuses for Mass Memory communication - MM1 through MM2 - (100018 through 100019) with a maximum transmission rate of 1 MHz.

The scripted inputs for these datalinks on IMSIM Specification Form 10 were as follows:

```
''MASS MEMORY DATALINK - MM1
''  MODE  TRANSMISSION RATE  TIME LAG
10  18   0       120     500
''MASS MEMORY DATALINK - MM2
''  MODE  TRANSMISSION RATE  TIME LAG
10  19   0       120     500
```
f. Two databuses for Ground Interface communication - LBl through LB2 - (100022 through 100023) with a maximum transmission rate of 1 MHz.

The scripted inputs for these datalinks on IMSIM Specification Form 10 were as follows:

```
GROUND INTERFACE DATALINK - LBl
10 22 0 120 0
```

```
GROUND INTERFACE DATALINK - LB2
10 23 0 120 0
```

g. Four databuses for PCMMU communication - IP1 through IP4 - (100024 through 100027) with a maximum transmission rate of 1 MHz.

The scripted inputs for these datalinks on IMSIM Specification Form 10 were as follows:

```
PCMMU DATALINK - IP1
10 24 0 120 0
```

```
PCMMU DATALINK - IP2
10 25 0 120 0
```

```
PCMMU DATALINK - IP3
10 26 0 120 0
```

```
PCMMU DATALINK - IP4
10 27 0 120 0
```
h. Four datalinks for communication between Display Electronic Units and Display Units (100028 through 100031) with a maximum transmission rate of 800 bps. (bits/sec).

The scripted inputs for these datalinks on IMSIM Specification Form 10 were as follows:

```
'0DU1/DEU1 DATALINK
'0 MODE TRANSMISSION RATE TIME LAG
10 28 0 1 0
'
'0DU2/DEU2 DATALINK
'0 MODE TRANSMISSION RATE TIME LAG
10 29 0 1 0
'
'0DU3/DEU3 DATALINK
'0 MODE TRANSMISSION RATE TIME LAG
10 30 0 1 0
'
'0DU4/DEU4 DATALINK
'0 MODE TRANSMISSION RATE TIME LAG
10 31 0 1 0
```

i. Five datalinks for communication between Display Electronic Units and Keyboard Units (100032 through 100036) with a maximum transmission rate of 800 bps.

The scripted inputs for these datalinks on IMSIM Specification Form 10 were as follows:

```
'0KB1/DEU1 DATALINK
'0 MODE TRANSMISSION RATE TIME LAG
10 32 0 1 0
'
'0KB1/DEU3 DATALINK
'0 MODE TRANSMISSION RATE TIME LAG
10 33 0 1 0
'
'0KB2/DEU2 DATALINK
'0 MODE TRANSMISSION RATE TIME LAG
10 34 0 1 0
'
'0KB2/DEU3 DATALINK
'0 MODE TRANSMISSION RATE TIME LAG
10 35 0 1 0
'
'0KB3/DEU4 DATALINK
'0 MODE TRANSMISSION RATE TIME LAG
10 36 0 1 0
```
j. Two datalinks for communication between PCMMU and Instrumentation (100037 through 100038) with a maximum transmission rate of 800 KBps.

The scripted inputs for these datalinks on IMSIM Specification Form 10 were as follows:

```
''PCM1/INSTRUMENTATION DATALINK
''   MODE TRANSMISSION RATE TIME LAG
10 37 0 100 0
''
''PCM2/INSTRUMENTATION DATALINK
''   MODE TRANSMISSION RATE TIME LAG
10 38 0 100 0
''
```
5.2.3.3 Workload Specifications. The activity which is to transpire in the DDPS model should reflect every significant activity of the DDPS itself. The IMSIM workload specification forms enable the model designer to maintain a close correlation between elements of the model workload and the actual DDPS workload. The DDPS processor, modules, and data transmissions are defined as tasks, routines, and messages for the model. Static characteristics for each of these system constituents are generally coded directly in the specification forms; however, the dynamic characteristics (those which change as a function of time or system state) are coded as "variables" as described in Sections 5.2.4.2 and 5.2.4.3, and only cross-references to the appropriate variables are included in the specification forms.

All coding for the specification forms is numeric, although comments are associated with each form to describe it for the reader. The following general conventions should be noted:

a. The form number appears as the first field of the form (1 - job step, 2 - task, 3 - routine, 5 - message, 11 - data set)
b. An * at the end of a form line indicates that the form is continued on the next line
c. The second field of a form identifies the member of the class defined by the form.

5.2.3.3.1 Job Definition. For the purpose of IMSIM representation of the DDPS workload, the entire activity within a GPC may be treated as a single job, consisting of a set of independently scheduled tasks. Since IMSIM permits the same type of task to be invoked for more than one job, task characteristics are divided into two classes: those which pertain to the type of task, and those which relate to the occasion in which the task appears as a step of a job. The latter are included in IMSIM Form 1 which is discussed in this section.

The DDPS job consists of 20 independent job steps, corresponding to the 20 types of tasks defined in Section 5.2.3.3.2. Each step is assigned a priority, which is subordinate to the task "service class". All of the steps are defined to be cyclic, even though some do not represent inherently cyclic processes; this is done to permit rescheduling of such steps according to events by IMSIM.

A Go/Nogo condition is specified for each step, to indicate the conditions under which it is to commence an execution cycle. The condition is coded as the number of a "variable" which is defined in Section 5.2.4; in general, each condition is a test of an indicator which is manipulated via logic described in Section 5.2.4.1. The step is held inactive while the condition variable is zero, and becomes active when the variable assumes a positive, nonzero value.
In the approach with four Virtual Machines a different job with identical job steps was assigned to each of the four GPCs. Output messages to MDMS were suppressed for jobs 3, 4, and 5, as only the active computer actually transmits these messages.

a. The scripted inputs for the jobs in Approach #1 with one VM (NASA.SPECS10. DATA) on IMSIM Specification Form 1 were as follows:

<table>
<thead>
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<th>JOBS</th>
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### Approach 1 (Four active Virtual Machines) on IMSIM Specification Form 1

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30 April 1976
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5.2.3.3.2 Tasks. Each of the 20 scheduled processes of the DDPS which are relevant to the Mated/Drop Test was defined as an IMSIM task through use of the Form 2. The tasks were referenced in the definition of the DDPS job as described in the preceding section. Each task was assigned to one of two "service classes"; class 1 tasks obtain absolute priorities in the range 20-29, while class 5 tasks obtain absolute priorities of 0-9. The "delay" field indicated for Form 2 is not relevant to class 1 or 5 tasks, but must be filled in as a place-keeper (0 was used).

The process modules which are executed in a GPC are defined as "routines" as described in Section 5.2.3.3.3. Each module is called for execution in one or more processes, and the analog in the DDPS model is listing of routines as "Required Elements" of a task. The 5-digit numbers listed for each task (see the Form 2 table below) indicate the type of element and the individual of that type to be included for execution of the task. If the first digit is 3, the remaining digits identify a routine; if it is 5, the remaining digits identify a message (see Section 5.2.3.3.4).

Note that the amount of computation involved in performing a process was not directly associated with the task which represents the process, but rather with the routines which were employed for the task.

The tasks numbered 100 and higher were used for the simulation with four Virtual Machines.

The scripted inputs for the tasks on IMSIM Specification Form 2 were as follows:

```
"GEF_FC_EXEC  FAST CYCLE EXECUTIVE
"SCHEDULED AT 40MS INTERVALS BY GAV (20017) AND GAA (20016)
" CLASS  DELAY  REQUIRED ELEMENTS
   2   6   1   0  30087 30301 50006 50007 50008 50009 *
   50010 50011 50012 50013 50014 50015 *
   50016 50017 50018 50019 50020 50021 *
   50022 50023 50024 50025 50026 50027 *
   50050 50051 50052 50053 50054 1
   2 106  1   0  30087 30301 1
"

"AZE_SIP  SYSTEM SOFTWARE INTERFACE PROCESSOR
"SCHEDULED AT 40MS INTERVALS BY SYSTEM INITIALIZATION
" CLASS  DELAY  REQUIRED ELEMENTS
   2   7   1   0  30116 30130 30138 30147 50028 *
   50058 30151 30140 1
   2 107  1   0  30116 30130 30138 30147 30151 30140 *
   50028 1
"

"GAD_MATE_IDLE  MATED/DROP TEST IDLE MODE - 200
"SCHEDULED AT 40MS INTERVALS BY GAA (20016) UNTIL MODE TRANSITION
" CLASS  DELAY  REQUIRED ELEMENTS
   2   8   1   0  30302 30303 30045 30089 1
"
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"GMA_MIN_EXEC   MINOR CYCLE EXECUTIVE
"SCHEDULED AT 40MS INTERVALS BY GAV (20017). IF MODE 200 IS
"ENTERED WHILE PLATFORM IS NOT RELEASED, GMA IS CANCELLED AND THEN
"RESCHEDULED AT MODE TRANSITION.
" CLASS   DELAY   REQUIRED ELEMENTS
2    9      1      0 30042 30043 30045

"GEM MATE DROP_EXEC   MATED/DROP EXECUTIVE
"SCHEDULED AT 80MS INTERVALS BY GAA (20016) FOR MODE 201. IF MODE
"200 IS ENTERED, GEM IS CANCELLED.
" CLASS   DELAY   REQUIRED ELEMENTS
2   10      1      0 30304 30305 30306 30089 30087
3   05      1      0 30307 30312 30313 30315

"SDA_DATA_ACQUISITION   SM DATA ACQUISITION
"SCHEDULED AT 50MS INTERVALS BY SM OPS 1
" CLASS   DELAY   REQUIRED ELEMENTS
2   11      1      0 30155 50032 50033
2   111     1      0 30155

"SDM_PERFORM_MON_CONTROL   SM PERFORMANCE MONITORING CONTROL
"SCHEDULED AT 500MS INTERVALS BY SM OPS 1
" CLASS   DELAY   REQUIRED ELEMENTS
2   12      5      0 30316 30317

"SFO_FLIGHT_OPS   SM FLIGHT OPERATIONAL SEQUENCE (OPS 2)
"SCHEDULED BY UI SOFTWARE (20034)
" CLASS   DELAY   REQUIRED ELEMENTS
2   13      1      0 30157 30316

"SPM_SUBSYS_CONFIG_MON   SM SUBSYSTEM CONFIGURATION MONITORING
"PRETAKEOFF & PREDROP SM SPECS SCHEDULED BY UI SOFTWARE (20034)
" CLASS   DELAY   REQUIRED ELEMENTS
2   14      1      0 30157

"GEN_TAEM_NAV_CYC   TAEM NAVIGATION CYCLIC EXECUTIVE
"SCHEDULED AT 2000MS INTERVALS BY SPEC GUC (20027) UPON PLATFORM
"RELEASE REQUEST
" CLASS   DELAY   REQUIRED ELEMENTS
2   15      5      0 30306 30308

"GMS MAJ_EXEC   IMU MAJOR CYCLE EXECUTIVE
"SCHEDULED AT 320MS INTERVALS BY GMU/GMT/GMV (20021), GMS (20022),
"GMY (20023), AND GMS (20020), ALL OF WHICH ARE SCHEDULED BY
"SPEC GUC (20027).
" CLASS   DELAY   REQUIRED ELEMENTS
2   19      5      0 30309 30305
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**TM-(L)-5658/000/00**

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*Note: The above table lists the elements and their respective scheduling details. The classes, delays, and required elements are specified for each entry.*
5.2.3.3.3 Routines. The program modules which are called for DDPS processes are represented as IMSIM "routines". An IMSIM Form 3 is used to define each routine. As a practical consideration, a one-one correspondence between routines and modules was not maintained; instead, modules which are collectively employed for a process are grouped together and treated as a single routine. The conditions under which individual modules are exercised and to what extent they perform computation is represented by segments of the "Computation Time" function associated with each routine. These functions are defined and discussed in Section 5.2.4.2.

For each Form 3 listed below, comments are included to indicate which modules were represented by the routine. If the routine is to be used for more than one task, the "Share" code must be 1; otherwise its value is irrelevant.

A number of fields of Form 3 are not significant to simulation of the DDPS but must be filled with acceptable values for proper operation of IMSIM. Thus, a "Library Data Set" is specified for reading of routines from some external source in case they are not resident in memory (which they are); "Size" for each routine is given although analysis of memory loading is not being conducted and the values are therefore only set to a nominal value of 1; the "Time" field indicates an optional cutoff of computation and 0 indicates that no cutoff is desired; since there is only one class of processor being simulated (the CPU) it is nominally defined as a class 10; finally since there is only a single memory unit for each GPC, and one GPC was being simulated as the active transmitting computer for each Virtual Machine while the other three were simulated as redundant, the memory is designed as a variable function of the job being executed.

The scripted inputs for these routines on IMSIM Specification Form 3 were as follows:

```
"TAEM GUIDANCE  (TASK 10)
GGA_TAEM_GUID
SHARE LIB.DS SIZE TIME PROCOR MEMORY COMP.TIME
3 31 1 110001 1 0 10 442 359 0
"IMU MINOR CYCLE EXECUTIVE  (TASK 9)
GMA_MIN_EXEC
SHARE LIB.DS SIZE TIME PROCOR MEMORY COMP.TIME
3 42 1 110001 1 0 10 442 355 0
"IMU RESOLVER PROCESSOR  (TASKS 8, 9)
GMD_RES_PROC
SHARE LIB.DS SIZE TIME PROCOR MEMORY COMP.TIME
3 45 1 110001 1 0 10 442 356 0
"IMU GYRO-COMPASS ALIGNMENT (TASK 22)
GMX_GC_ALIGN
SHARE LIB.DS SIZE TIME PROCOR MEMORY COMP.TIME
3 62 1 110001 1 0 10 442 16 0.4
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(TASKS 8, 9, 10)

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<td>HANGAR CALIBRATION B</td>
<td>3</td>
<td>327</td>
<td>1</td>
<td>15601</td>
<td>0</td>
</tr>
<tr>
<td>GMT_PREFLIT_CALA</td>
<td>PREFLIGHT CALIBRATION A</td>
<td>3</td>
<td>328</td>
<td>1</td>
<td>15601</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td><strong>REDUNDANCY MANAGEMENT</strong></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>GRE_FDIR</td>
<td>FDI SEQUENCER</td>
<td>3</td>
<td>329</td>
<td>1</td>
<td>15601</td>
<td>0</td>
</tr>
<tr>
<td>GRF_TRANS_FDIR</td>
<td>TRANSDUCER SEQUENCER</td>
<td>3</td>
<td>330</td>
<td>1</td>
<td>15601</td>
<td>0</td>
</tr>
<tr>
<td>GRG_FDBK_FDIR</td>
<td>ACTUATOR FEEDBACK SEQUENCER</td>
<td>3</td>
<td>331</td>
<td>1</td>
<td>15601</td>
<td>0</td>
</tr>
<tr>
<td>GRH_SWITCH_FDIR</td>
<td>SWITCH SEQUENCER</td>
<td>3</td>
<td>332</td>
<td>1</td>
<td>15601</td>
<td>0</td>
</tr>
<tr>
<td>GRL_RGA_FDIR</td>
<td>RATE-GYRO SEQUENCER</td>
<td>3</td>
<td>333</td>
<td>1</td>
<td>15601</td>
<td>0</td>
</tr>
</tbody>
</table>
```
GRJ_AA_FDIR    ACCELEROMETER ASSEMBLY
GRK_RA_FDIR    RADAR ALTIMETER
GRL_TMU_FDIR   IMU SEQUENCER
GRM ADTA_FDIR  ADTA SEQUENCER
GRN TACAN_FDIR MSBLs SEQUENCER
GRO_MSBLs_FDIR MSBLs SEQUENCER
GRP BF_FDIR    BODY FLAP SEQUENCER
SHARE LIB.DS   SIZE TIME PROCSR MEMORY COMP.TIME
3  312    1  110001    1   0   10   442   428   0

"USER INTERFACE SUPERVISOR (TASK 34)
"DMC_SUPER USER INTERFACE CONTROL SUPERVISOR
"DMC_FUNCTIONS KEYBOARD FUNCTIONS
"DMC_APP_INT APPLICATION CONTROL INTERFACE
"DMC_MCDS_CNT MCDS DISPLAY CONTROL
"DMC_APP_KEY_PROCESS APPLICATION KEYS PROCESSING
"DMC_DISPLAY DISPLAY COORDINATION
"DMC_SEQ_REQ_PROC SEQUENCE REQUEST PROCESSING
"DIM ICC_COLLECTOR ICC MSG COLLECTOR
SHARE LIB.DS   SIZE TIME PROCSR MEMORY COMP.TIME
3  313    0  110001   10380   0   10   442   431

"CYCLIC DISPLAY PROCESSING (TASK 35)
"DCI#CYC CYCLIC DISPLAY PROCESSING
"DCI#CON DATA CONVERSION
"DCI#FMT DATA FORMATTING
SHARE LIB.DS   SIZE TIME PROCSR MEMORY COMP.TIME
3  314    0  110001   5252    0   10   442   435   2.06   8.3

"MATED DROP, WARMUP, AND RAW DATA PROCESSING (TASKS 10, 18)
"GGJ_AVG_G_SP SINGLE PRECISION AVERAGE G
"GGK_USER_PARAM USER PARAMETERS
"GPA ADTA DATA_PROC ADTA DATA PROCESSOR
"GPM MSBL DATA_PROC MSBLs DATA PROCESSOR
"GPR RA DATA_PROC RADAR ALTIMETER PROCESSOR
"GPT TACAN DATA_PROC TACAN DATA PROCESSOR
"GTM TACAN WARMUP TACAN WARM-UP
"GTP MSBLs WARMUP MSBLs WARM-UP
"GTR RA WARMUP RADAR ALTIMETER WARM-UP
SHARE LIB.DA   SIZE TIME PROCSR MEMORY COMP.TIME
3  315    0  110001    1   0   10   442   396   0
```
"SYSTEMS MANAGEMENT PERFORMANCE MONITORING (TASKS 12, 13)
" SFD_FAULT_DETECT_ANNUN  FAULT DETECTION & ANNUNCIATION
" SPP_PRECON_PROCESS  PRECONDITION PROCESSING
" SSC_SPECIAL_COMP  SPECIAL COMPUTATIONS
" SAS_ANALOG_SCALE  ANALOG SCALING
SHARE  LIB.DS  SIZE  TIME  PROCOR  MEMORY  COMP.TIME
3  316  1  110001  1  0  10  442  425  0
"
"PERFORMANCE MONITORING CONTROL (TASK 12)
" SPM_PERFORM_MON_CONTROL  PM CONTROL
SHARE  LIB.DS  SIZE  TIME  PROCOR  MEMORY  COMP.TIME
3  317  1  110001  1  0  10  442  387
"
5.2.3.3.4 Messages. All data transmissions performed by the IOP of the GPC being simulated were defined as messages using IMSIM Form 5. Other transmissions were not simulated as they had no impact on loading of the GPC under study; i.e., they did not occupy resources of the GPC and, due to the configuration of the DDPS, could not interface with transmissions controlled by the GPC.

Each Read transmission is preceded by a Write transmission to query the appropriate device. Although a message defined via Form 5 represents a type of transmission, it may represent one or more occurrences of the transmission, each with different source, destination, length, etc. These capabilities are employed in characterizing DDPS transmissions for the model, and are best illustrated by example. Consider the pair of message definitions 6 and 7 as shown in the list of forms below (the first two lines which begin with the number 5). As indicated by the "Total" field, each of these messages represents three transmissions. Message 6 represents a sequence of Write transmissions (from memory 1, denoted by 70001) to a destination denoted by Variable 380. This variable is described in Section 5.2.4; in essence, it states that the destination for the first (of three) transmissions is the Multiplexer/Demultiplexer for the Flight Critical Forward Instruments #3 (6001), that the second is Multiplexer/Demultiplexer for the Flight Critical Forward Instruments #2 (6000), and that the third is Multiplexer/Demultiplexer for Flight Critical Forward Instruments #1 (6000).

The "Length" and "Interval" fields are each comprised of three subfields; the value 16 in the first subfield denotes a constant length (12 characters) or interval (1 ms), as indicated by the second subfield (the third subfield is not used for the DDPS model). "Length" is expressed in terms of 8-bit characters of data transmitted, and transmission rates for hardware (as described in Section 5.2.3.2) are adjusted to compensate for the added control bits of each transmission. The "Nature" of message 6 is given as 0 - indicating that it can only be initiated when the task has been activated - and the "Start" of 1 causes the first transmission to be initiated 1 ms after the task commences.

Message 7 represents the response to message 6 and its transmission is correlated on a one-one basis with transmission of message 6 by specifying Nature 2 and giving the "Source" of the message as message 6 (50006). Note that in this situation, transmission of message 7 is triggered by completion of a message 6 transmission, and the source of message 7 is taken to be the sink of message 6. Message transmissions were simulated whenever a task was activated which includes the message among its required elements (see Section 5.2.3.3.2). Interference in accessing system components for transmission is automatically handled by IMSIM according to hardware and configuration specifications included in Forms 6 through 12.

The scripted inputs for these messages on IMSIM Specification Form 5 were as follows:
```
System Development Corporation

30 April 1976

"READ FROM FF01, FF02, FF03 -
  ACCELEROMETER ASSEMBLY (ACCLRM)
  ROTATIONAL HAND CONTROLLER 1 & 2 (LH RHC, RH RHC)
  SPEEDBRAKE THRUST CONTROLLER 1 & 2 (SBTC)
  RUDDER PEDAL TRANSDUCER ASSEMBLY 1 & 2 (RPTA)
  FF MDM DISCRETES
  NATURE  SOURCE  SINK  LENGTH  INTERVAL  START  TOTAL  SE  T
  5  6   0  70001  380  16  12  0  16  1  0  1  3
  5  7   2  50006  70001 16  56  0  16  0  0  0  3

"READ FF04 MDM DISCRETES
  NATURE  SOURCE  SINK  LENGTH  INTERVAL  START  TOTAL  SE  T
  5  8   0  70001  60012 16  2  0  16  0  0  1  1
  5  9   2  50008  70001 16  24  0  16  0  0  0  1

"READ IMU FROM FF01, FF02, FF03
  NATURE  SOURCE  SINK  LENGTH  INTERVAL  START  TOTAL  SE  T
  5 10  0   70001  380  16  2  0  16  1  0  1  3
  5 11  2  50010  70001 16  28  0  16  0  0  0  3

"READ FROM FF01 -
  FWD ATTACH POINT VOLTAGE (LCA)
  AIR DATA TRANSDUCER ASSEMBLY (ADTA)
  MSBLS
  TACAN AND TACAN REGISTER
  RADAR ALTIMETER (RAD ALT)
  NATURE  SOURCE  SINK  LENGTH  INTERVAL  START  TOTAL  SE  T
  5 12  0  70001  60009 16 12  0  16  0  0  1  1
  5 13  2  50012  70001 16 32  0  16  0  0  0  1

"READ FROM FF02 -
  ADTA
  MSBLS
  TACAN AND TACAN CONTROL REGISTER
  RAD ALT
  NATURE  SOURCE  SINK  LENGTH  INTERVAL  START  TOTAL  SE  T
  5 14  0  70001  60010 16 10  0  16  0  0  1  1
  5 15  2  50014  70001 16 34  0  16  0  0  0  1

"READ FROM FF03 -
  LCA
  ADTA
  MSBLS
  TACAN AND TACAN CONTROL REGISTER
  NATURE  SOURCE  SINK  LENGTH  INTERVAL  START  TOTAL  SE  T
  5 16  0  70001  60011 16 10  0  16  0  0  1  1
  5 17  2  50016  70001 16 30  0  16  0  0  0  1
```
```
!READ DATA FROM FF04
<table>
<thead>
<tr>
<th>NATURE</th>
<th>SOURCE</th>
<th>SINK</th>
<th>LENGTH</th>
<th>INTERVAL</th>
<th>START</th>
<th>TOTAL</th>
<th>SE</th>
<th>T</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 18</td>
<td>70001</td>
<td>60012</td>
<td>16 20</td>
<td>16 00</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 19</td>
<td>50018</td>
<td>70001</td>
<td>16 14</td>
<td>16 00</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

!READ CLOCK (MTU) FROM FF01, FF02, FF03
<table>
<thead>
<tr>
<th>NATURE</th>
<th>SOURCE</th>
<th>SINK</th>
<th>LENGTH</th>
<th>INTERVAL</th>
<th>START</th>
<th>TOTAL</th>
<th>SE</th>
<th>T</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 20</td>
<td>70001</td>
<td>380</td>
<td>16 20</td>
<td>16 10</td>
<td>1</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 21</td>
<td>50020</td>
<td>70001</td>
<td>16 14</td>
<td>16 00</td>
<td>0</td>
<td>3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

!READ FROM FA01, FA02, FA03
 RATE GYRO ASSEMBLY
| MDM DISCRETES
<table>
<thead>
<tr>
<th>NATURE</th>
<th>SOURCE</th>
<th>SINK</th>
<th>LENGTH</th>
<th>INTERVAL</th>
<th>START</th>
<th>TOTAL</th>
<th>SE</th>
<th>T</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 22</td>
<td>70001</td>
<td>381</td>
<td>16 60</td>
<td>16 10</td>
<td>1</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 23</td>
<td>50022</td>
<td>70001</td>
<td>16 18</td>
<td>16 00</td>
<td>0</td>
<td>3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

!READ FROM FA04
 ACTUATOR POSITION FEEDBACKS (ASA)
| MDM DISCRETES
<table>
<thead>
<tr>
<th>NATURE</th>
<th>SOURCE</th>
<th>SINK</th>
<th>LENGTH</th>
<th>INTERVAL</th>
<th>START</th>
<th>TOTAL</th>
<th>SE</th>
<th>T</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 24</td>
<td>70001</td>
<td>60016</td>
<td>16 60</td>
<td>16 00</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 25</td>
<td>50024</td>
<td>70001</td>
<td>16 26</td>
<td>16 00</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

!READ FROM FA01, FA02
 ATTACH POINT VOLTAGE (LCA)
| MDM DISCRETES
<table>
<thead>
<tr>
<th>NATURE</th>
<th>SOURCE</th>
<th>SINK</th>
<th>LENGTH</th>
<th>INTERVAL</th>
<th>START</th>
<th>TOTAL</th>
<th>SE</th>
<th>T</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 26</td>
<td>70001</td>
<td>381</td>
<td>16 20</td>
<td>16 10</td>
<td>1</td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 27</td>
<td>50026</td>
<td>70001</td>
<td>16 12</td>
<td>16 00</td>
<td>0</td>
<td>2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

!ICC FOR REDUNDANT SET
<table>
<thead>
<tr>
<th>NATURE</th>
<th>SOURCE</th>
<th>SINK</th>
<th>LENGTH</th>
<th>INTERVAL</th>
<th>START</th>
<th>TOTAL</th>
<th>SE</th>
<th>T</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 28</td>
<td>383</td>
<td>384</td>
<td>16 256</td>
<td>16 00</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

!READ DISPLAY FORMAT FROM MASS MEMORY
 NOT USED IN ALT
<table>
<thead>
<tr>
<th>NATURE</th>
<th>SOURCE</th>
<th>SINK</th>
<th>LENGTH</th>
<th>INTERVAL</th>
<th>START</th>
<th>TOTAL</th>
<th>SE</th>
<th>T</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>70001</td>
<td>110002</td>
<td>16 20</td>
<td>16 00</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>50030</td>
<td>70001</td>
<td>16 1024</td>
<td>16 00</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

!READ PERFORMANCE DATA FROM PCMU
<table>
<thead>
<tr>
<th>NATURE</th>
<th>SOURCE</th>
<th>SINK</th>
<th>LENGTH</th>
<th>INTERVAL</th>
<th>START</th>
<th>TOTAL</th>
<th>SE</th>
<th>T</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 32</td>
<td>70001</td>
<td>60095</td>
<td>16 256</td>
<td>16 10</td>
<td>1</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5 33</td>
<td>50032</td>
<td>70001</td>
<td>16 256</td>
<td>16 00</td>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
<table>
<thead>
<tr>
<th>Action</th>
<th>Register</th>
<th>Nature</th>
<th>Source</th>
<th>Sink</th>
<th>Length</th>
<th>Interval</th>
<th>Start</th>
<th>Total</th>
<th>SE</th>
</tr>
</thead>
<tbody>
<tr>
<td>WRITE TO FF01, FF02, FF03</td>
<td>CONTROL REGISTER</td>
<td>MDM DISCRETES</td>
<td>NATURE</td>
<td>SOURCE</td>
<td>SINK</td>
<td>LENGTH</td>
<td>INTERVAL</td>
<td>START</td>
<td>TOTAL</td>
</tr>
<tr>
<td>WRITE FF MDMDISCRETESTO FF04</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WRITE IMU TO FF01, FF02, FF03</td>
<td>SOURCE SINK LENGTH INTERVAL START TOTAL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WRITE TO DDU1, DDU2</td>
<td>AERO SURFACE SERVO AMPLIFIER (ASA)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WRITE TO DDU1, 2, AND 3 (TASK 34)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>WRITE PRIMEFRAME TO PCMMU</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>READ KEVRD 1 AND WRITE NEW DISPLAY TO DEUL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
5.2.3.3.5 Data Sets. Data sets represent files of data allocated to auxiliary storage. For representation of the DDPS, two data sets were defined, as shown in Form 11 listing below. Data set 1 represents the library file from which major function overlays are selected for main memory. Since simulation of the Mated/Drop Test does not include the overlay function, it is performed as part of the initializing process of the model; nevertheless, a library data set must be specified for each routine to be addressed, and the data set must be defined. Data set 2 represents one of the mass storage files for display images. Only one is represented as only one is to be used for a given system configuration.

Both data sets are assigned to storage 1 (mass storage facility) and are defined to be serially addressed ("Org" = 0). The "Initial Size" and "Maximum Size" for a data set are separately specifiable to permit dynamic change in the data content of a data set; however, this feature is not required for DDPS Simulation, and therefore, both fields are specified as the same: 10^7 characters for the library, and 1.024x10^7 characters for the displays.

The scripted inputs for these data sets on IMSIM Specification Form 11 were as follows:
```
20 STORAGE ORG INIT.SIZE MAX.SIZE
11 1 1 0 10000 10000
11 2 1 0 10240 10240
```

5.2.3.3.6 Executive Algorithms. IMSIM Form 13 is used to select from among various options the methods to be used by IMSIM in performing some of the functions normally relegated to executive or operating systems of computers. While some are not relevant to DDPS Simulation, they are all specified and listed below with clarification as needed.

```
ALGORITHM SELECTION
13 1 0 1 1 0 0 0 1 1 1 1 1 0 0 0
```

1A If alternative paths between a source and sink are available, but all are in use when a transmission is to be performed, defer the transmission until any path becomes available.

1B If more than one path for a transmission is open, choose the first one in the list.
2A These options pertain to memory allocation and are not meaningful for the DDPS simulation.
2B
2C
2D
2E

3A Processing is interruptible for executive functions and for tasks of service class 1.
3B

3C Scheduling precedence is determined by task priority.

4A This option pertains to use of nonsharable systems components (other than a CPU) by tasks, and is not relevant to DDPS Simulation.
4B All transmissions are to be over explicitly defined data links, i.e., no implicit links are allowed.

5A These options pertain to simulation of program loading, and are not relevant to the DDPS Simulation.
5B

6A The CPU is not to be interrupted in performing a task in order to initiate and service I/O (this function is performed by the IOP of the DDPS).
5.2.4 Model Adaptation and Parameterization (S.O.W. 2.1.4)

The following paragraphs under this section describe in detail the work performed under this task. In summary it entailed:

a. Logic changes made to IMSIM to accommodate NASA-unique simulation, which include:
   1. Cyclic activation of functions
   2. Dynamic setting of conditions through the jobschedule
   3. Delivery of computational units by the routines through the setting of gates and savex cells
   4. Suppression of zero-length transmission
   5. Deletion of segments of IMSIM not pertaining to the NASA simulation to reduce computer simulation run time
   6. Incorporation of a checkpoint capability

b. Incorporation of a new report #2 in IMSIM to better reflect the status of task activations and cyclic operations.
   The reports for message traffic were revised for easier reading.

c. Defining a total of 100 new variables for:
   1. Stipulating functional conditions for delivering computation time by routines
   2. Defining sources and sinks and message length for data messages
   3. Determining conditions for operations of functions
   4. Calculating time slices
   5. Clearing keyboard inputs
   6. Determining branch locations dependent upon operational conditions
   7. Time slice setting and counters

d. Parameterizing the model with the parameters reflecting the simulated hardware and software as described in detail in paragraph 5.2.3.

5.2.4.1 NASA-Unique IMSIM Revisions. IMSIM was adapted for NASA-unique conditions with the following changes:

a. Facilitate cyclic activation of functions
b. Dynamic setting of conditions through the jobschedule
c. Delivery of computational units by routines
d. Suppression of zero-length transmission
e. Deletion of segments of IMSIM not pertinent to the NASA simulation
5.2.4.1.1 Cyclic Activation of Functions. In order to facilitate the operation of cyclic functions at various intervals, transactions were generated at each of the intervals, parameter 3 (P3) was set with the unique gate number for that function, and parameter 4 (P4) was set with the unique task number for that function. The gate was used for intercommunication with the prototype task and was closed again after task was activated. The transactions were only admitted if the conditions for operation of that function were met.

Cyclic activation took place at the following intervals for the specified functions as given in Table 5-1 below.

Table 5-1. Cyclic Activation of Functions

<table>
<thead>
<tr>
<th>INTERVAL</th>
<th>FUNCTION NAME</th>
<th>FUNCTION DESIGNATOR</th>
<th>TASK NUMBER</th>
<th>GATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>40 ms</td>
<td>System Software Interface Proc</td>
<td>AIE</td>
<td>7</td>
<td>1502</td>
</tr>
<tr>
<td></td>
<td>Minor Cycle Executive</td>
<td>GMA</td>
<td>9</td>
<td>1504</td>
</tr>
<tr>
<td></td>
<td>Fast Cycle Executive</td>
<td>GEF</td>
<td>6</td>
<td>1501</td>
</tr>
<tr>
<td></td>
<td>Mated/Drop Idle Mode</td>
<td>GAD</td>
<td>8</td>
<td>1503</td>
</tr>
<tr>
<td>50 ms</td>
<td>S.M. Data Acquisition</td>
<td>SDA</td>
<td>1</td>
<td>1520</td>
</tr>
<tr>
<td></td>
<td>Mated/Drop Executive</td>
<td>GEM</td>
<td>10</td>
<td>1505</td>
</tr>
<tr>
<td></td>
<td>Cyclic Display Processing</td>
<td>DCI</td>
<td>35</td>
<td>1517</td>
</tr>
<tr>
<td></td>
<td>MCDS Input Processor</td>
<td>DMI</td>
<td>32</td>
<td>1514</td>
</tr>
<tr>
<td></td>
<td>IMU Major Cycle Executive</td>
<td>GMG</td>
<td>19</td>
<td>1508</td>
</tr>
<tr>
<td></td>
<td>S.M. Performance Monit. Cntrl.</td>
<td>SDM</td>
<td>12</td>
<td>1521</td>
</tr>
<tr>
<td></td>
<td>GPC Switch Monitor</td>
<td>ARA</td>
<td>37</td>
<td>1518</td>
</tr>
<tr>
<td></td>
<td>TAEM Navigation Cyclic Exec.</td>
<td>GEN</td>
<td>15</td>
<td>1506</td>
</tr>
<tr>
<td>1000 ms</td>
<td>S.M. Flight Ops 2</td>
<td>SFO</td>
<td>13</td>
<td>1522</td>
</tr>
<tr>
<td></td>
<td>User Interface</td>
<td>DMC</td>
<td>34</td>
<td>1516</td>
</tr>
<tr>
<td></td>
<td>S.M. Subsystem Conf. Monitor</td>
<td>SPM</td>
<td>14</td>
<td>1523</td>
</tr>
<tr>
<td></td>
<td>FCS Dedicated Display Checkout</td>
<td>GTX</td>
<td>24</td>
<td>1513</td>
</tr>
<tr>
<td></td>
<td>IMU Attitude Determination</td>
<td>GMS</td>
<td>20</td>
<td>1509</td>
</tr>
<tr>
<td></td>
<td>IMU Calibration</td>
<td>GAT,GMU,GMV</td>
<td>21</td>
<td>1510</td>
</tr>
<tr>
<td></td>
<td>IMU gyro Alignment</td>
<td>GMX</td>
<td>22</td>
<td>1511</td>
</tr>
<tr>
<td></td>
<td>IMU Velocity &amp; Tilt</td>
<td>GMY</td>
<td>23</td>
<td>1512</td>
</tr>
</tbody>
</table>
The logic for this change is depicted in Figure 5-2 giving the flow diagrams for this logic. Reference 1, the MODLIT Reference Manual, details the symbols and code used in these flow diagrams.

Figure 5-2. Flow Diagrams for Cyclic Activation of Functions
Figure 5-2 (cont)
Figure 5-2 (cont)
Figure 5-2 (cont)
Figure 5-2 (cont)
5.2.4.1.2 Dynamic Setting of Conditions Through the Job Schedule. In order to enable dynamic setting of events during a simulated time period (e.g., manual actions taken by the Commander or Pilot, or request of Specialist Functions) IMSIM was modified to recognize this at the time specified in the job schedule. This was accomplished by adding a new form with a zero in the 2nd field, indicating this was an event occurrence. In this case, the next four fields on the line were interpreted respectively as a Savex Cell, incremental value, 2nd Savex Cell, and 2nd incremental value. The IMSIM Program Logic Manual (Reference 3) details the program blocks where the revision is inserted.

The code accomplishing this is as follows:

```
REVISE 238000 238000    'SET SAVEX FROM JOBSCHEDULE
1010 DETOUR 1012
   ADMIT IF P2 = 0
   X(P3) + P4
   DETOUR 30012
   ADMIT IF PL1 GR 0
   SAVE P5
30010 X(P6) + P7
   POP
   POP
   DETOUR 30010
   ADMIT IF PL1 = 0
30012 REMOVE
1012 P2 = V153
```

5.2.4.1.3 Delivery of Computational Units by Routines. IMSIM was modified to calculate the computation time for a given function by summing the computational units assigned to each routine that is called by this function at a particular cycle. Thus, the routine will be the determining factor as to the amount of computation time it provides, dependent upon the conditions under which it is called to operate.

Calculation of the computation time for each routine is discussed in more detail in paragraph 5.2.4.2.

The code accomplishing this change is as follows:

```
REVISE 1134000 1134000
   'PREVENT COMP TIME FROM MESSAGES
   ADMIT IF X(P2) = 1
```

5.2.4.1.4 Suppression of Zero-Length Transmissions. This change was incorporated in IMSIM as a technical one to control the message transmission by its length, i.e., a zero-length transmission would prevent transmission or receipt.
The code for this change is as follows:

```
REVISE 881000 881000 "SUPPRESS ZERO LENGTH TRANSMISSION"
   DETOUR 1606
   ADMIT IF P3 = 0
   POP P2
   TRY 1865
   1606 P2 = P6
```

5.2.4.1.5 Deletion of Segments of IMSIM. Certain segments of IMSIM, being a general purpose model, did not pertain to the simulation to be performed for NASA. These deletions were for Virtual Machine and Memory Recording, and to eliminate prototypes after they are initialized. These deletions avoided unnecessary scanning and calculations, that became a burdensome factor in the actual wall clock time for simulation runs.

The code for this change is as follows:

```
REVISE 390000 390000 "SPEED-UP BY ELIMINATING PROTOTYPES"
REVISE 649000 661000 "SPEED-UP BY ELIMINATING V.M. & MEM.RECO"
   TRY 1352
REVISE 663000 680000 "SPEED-UP BY ELIMIN. V.M. & MEMORY RECORDING"
   X(V67) = 1
```

5.2.4.1.6 Checkpoint Capability. This feature was incorporated in MODLIT/IMSIM to facilitate NASA simulation runs of longer duration, with a restart capability from previously established checkpoints.

5.2.4.1.7 New Reports. The following two new reports were incorporated in IMSIM to ease the reading of statistical outputs for cyclic functions performed during a simulation run.

```
REPORT 2 1 1
   DURING V232 SECONDS OF SIMULATED SHUTTLE OPERATIONS
   A TOTAL OF BW1160 DIFFERENT FUNCTIONS WERE INTRODUCED.
   THESE FUNCTIONS WERE ACTIVATED BW1166 TIMES, STATUS IS:
   BW1196 WERE COMPLETED
   B1167 ARE WAITING FOR NEXT ACTIVATION
   B3032 ARE IN READY STATE, I.E. WAITING FOR CPU
   B1182 ARE WAITING FOR MESSAGES TO COMPLETE
   V306 PRESENTLY EXECUTING, I.E. IN ACTIVE STATE
   FUNCTIONS WERE INTERRUPTED BW2000 TIMES.
   X643 FUNCTION ACTIVATIONS WERE ABORTED AS FUNCTION STILL ACTIVE. ENDR
REPORT 30 1 1 X577
   AT TIME C1 ACTIVATION FOR FUNCTION X577 ABORTED, AS
   FUNCTION X577 IS STILL ACTIVE. ENDR
```
The two reports for "Message Start" and Message End" were modified for easier reading and scanning in the simulation results. The new format is reflected in the history printout of simulation runs in Appendix C.

5.2.4.2 Compute Times for Routines. Computational units in microseconds for routines pertaining to the Operating System or System Control were obtained from the ALT Functional Design Specification, Volume 2, Part 1 and Volume 2, Part 3. (Reference 19)

Computational units in microseconds for all other routines were determined by plotting all functions performed by each routine down to instruction level and applying the instruction execution times as given in IBM's Software System Notes #156-005 and IBM's CPU Instruction Execution Times Notes #C69-75-254 and #C69-75-256 (References 26, 27, and 28).

The conditions for operation of the routines (including flight conditions and states of the system) were then included for proper allocation of computing units, and were incorporated in "Variables" used by IMSIM to generate the computation time.

As IMSIM is based on millisecond time units, the computation times were given in fractions to 3 decimals for the proper microsecond presentation multiplied by a factor of 0.48 to compensate for the CPU processing speed factor so that the end result again would give the absolute calculated computation time for each routine.

Following is a discussion of the Variables developed for the routines to determine delivery of computation time. For clarity, the multiplication factor of 0.48 for all absolute computation times, included to compensate for the CPU's speed factor, has been omitted from the discussion in this paragraph (see Section 5.1.3.4). The matrix values and makeup of all Variables are specified in detail in Appendix A).

a. If in the columns designated for computation time on form 3 a Variable 16 appears in column 1, then the succeeding value (X44) is the unconditional computation time whenever the routine is called for execution.

Any value other than 16 indicates functional conditions which are expressed in that numbered variable.

b. Routine 31 (TAEM GUIDANCE) - Variable 359

\[ V359 = \text{DFN} \times X700 \] (matrix values)

The computation time of V359 is a discrete function of the 80 ms Time Slice Counter X700. This counter maintains the count of 80 ms cycles for 12 periods (960 ms). V359 is 0 for counter values between 0 and 5 and for a value of 7. V359 equals 0.03 ms for a counter value of 6 and 8 through 12. Computation time therefore varies between 0 and 30 μs.

c. Routine 42 (IMU Minor Cycle Executive) - Variable 355

\[ V355 = 1.55 + (\text{RFI}) \times 0.3 \]

The computation time of the variable consists of a constant 1.55 ms and a random-generated time ranging between 0 and 0.3 ms. Computation for this variable is therefore between 1.55 and 1.85 ms.
d. Routine 45 (IMU Resolver Processing) - Variable 356
   \[ V_{356} = 0.72 + (RF1) \times 0.11 \]
   Variable 356 has a computation time consisting of a constant 0.72 ms and
   a random-generated time ranging from 0 to 0.11 ms. Comp time for this
   routine therefore varies between 720 µs and 830 µs.

e. Routine 63 (IMU Velocity Tilt) - Variable 397
   \[ V_{397} = V_{398} + X_{44} \]
   \[ V_{398} = DFN (X_{685}) \text{(matrix values)} \]
   The computation time of this variable is a discrete function of the
   Specialist function state. For a TERMINATE state \( V_{398} = 0.005 \text{ ms} \) and
   for any other Specialist function state \( V_{398} = 0.135 \text{ ms} \). The fixed
   value of the routine 63 Savex cell \( X_{44} \) is 0.26 ms. The comp time of
   this variable therefore is between 265 and 395 µs.

f. Routine 134 (GPC/PCMU Data Cycle Synchronizer) - Variable 364
   \[ V_{364} = 0.5 + (RF1) \times 30 + X_{44} \]
   The computation time for this variable consists of a constant 0.5 ms
   plus a random-generated time of from 0 to 30 ms plus a computation time
   which is stored in Savex cell \( X_{44} \). The initial value of \( X_{44} \) is 0.215 ms.
   Comp time therefore varies between 715 µs and 30.715 ms.

g. Routine 135 (GPC Downlist Data Control Processor) - Variable 365
   \[ V_{365} = V_{362} + V_{356} + 0.66 \]
   \[ V_{362} = 0.56 + (RF1) \times 0.03 = \text{Time for Routine 303} \]
   \[ V_{356} = 0.72 + (RF1) \times 0.11 = \text{Time for Routine 45} \]
   The computation time for variable 365 consists of the computation time
   for routine 303, routine 45, and a constant of 0.66 ms. Comp time will
   therefore range between 1.94 and 2.08 ms.

h. Routine 155 (Systems Management Data Acquisition) - Variable 386
   \[ V_{386} = DFN (G_{1551})(\begin{array}{c}
   0.0024 \\
   0.096 
\end{array}) \]
   The computation time for this routine is a function of the setting of gate
   1551, which is the processing gate for data acquisition. This gate is
   set every 50 ms by Variable 427, which is a function of the value pro-
   duced by a random-number generator. If the gate is set, processing
   time will be 200 microseconds, if the gate is not set, comp time
   drops to 5 microseconds.

i. Routine 301 (Flight Control) - Variable 350
   \[ V_{350} = 0.98 + V_{351} + V_{352} \]
   \[ V_{351} = DFN (X_{683}, X_{684})(\text{matrix values}) \]
   \[ V_{352} = FDN (X_{681}, X_{682})(\text{matrix values}) \]
   \( X_{683} = \text{Navigational Status Savex} \)
   \( X_{684} = \text{Flight Condition Savex} \)
   \( X_{681} = \text{Time Slice Savex} \)
   \( X_{682} = \text{Major Mode Savex} \)
This variable consists of a fixed time of 0.98 ms plus two additional times which are discrete functions of system conditions. The time for Variable V351 is a function of Navigational state and flight conditions and can range from 0 to 0.615 ms. The time for Variable V352 is a function of the processing time-slice period and the major mode and has a range from 0.31 to 5.875 ms.

The computation time for this routine therefore is 1.29 ms minimum to 7.47 ms maximum.

j. Routine 302 (Mated/Drop Control) - Variable 361

\[
V_{361} = V_{360} \\
V_{360} = DFN (V_{366}, V_{367}) \text{ (matrix values)} \\
V_{366} = X_{681} \cdot 2 \text{ 80 ms Time slice} \\
V_{367} = X_{684} \cdot 2 \text{ Platform Release}
\]

The computation time for V361 is a variable whose identification number is defined by V360. For the conditions where the time slice is not 80 ms and the IMU platform has not been released or where the time slice is 80 ms and the IMU platform has been released, V360 = V365. For the condition where the time slice is not 80 ms but the IMU platform has been released, V360 = V363 = 0.

\[
V_{365} = V_{362} + V_{356} + 0.66 \\
V_{362} = 0.58 + (RF1) \cdot 0.03 \\
V_{356} = 0.72 + (RF1) \cdot 0.11
\]

For the condition where V360 = V363, the computation time of V361 will be zero.

For the condition where V360 = V365, the computation time for V361 will be determined by two randomly generated values plus a constant. For this condition, the computation time will vary between 1.96 ms and 2.10 ms.

k. Routine 303 (IMU Processing, Accelerometer Accumulator and Gyro Torquing) - Variable 362.

\[
V_{362} = 0.56 + (RF1) \cdot 0.03
\]

The computation time of this variable is randomly generated and will range from 0.56 ms to 0.59 ms.

l. Routine 304 (Displays and IMU Moding) - Variable 390

\[
V_{390} = 0.09 + V_{391} \\
V_{391} = 0.01 + X_{687} \cdot V_{392} \\
V_{392} = DFN (X_{685}, X_{682}) \text{ (matrix values)}
\]

The value of V392 is a discrete function of the Major mode and the status of the Specialist Function. However, the value of V392 can only be used if DISPLAY status is in the "New Display" condition. Depending on the conditions of the Major mode, the Specialist function and Display conditions, V390 will have a range of 100 µs to 485 µs.
m. Routine 306 (Navigation) - Variable 368

\[ V_{368} = X_{44} + 369 \]
\[ V_{369} = DFN(X_{682})(\text{matrix values}) \]

Computation time for \( V_{368} \) consists of a fixed value of 150 \( \mu \)s (stored in Savex cell \( X_{44} \)) and a value which is a discrete function of the Major operational mode. The times for \( V_{369} \) are as follows:

- 0.3 ms for Null and Preflight Prep Modes
- 0.34 ms for Mated Idle, Mated Flight, Separation, Postseparation and TAEM Modes
- 0.16 ms for the Approach & Landing Mode
- 0.34 ms for the Rollout mode.

Computation time will therefore range between 490 ms and 310 ms.

n. Routine 307 (Guidance) - Variable 370

\[ V_{370} = V(379) \]
\[ V_{379} = DFN(X_{682})(\text{matrix values}) \]

The computation times for this variable are defined by a variable which is selected by the conditions of \( V_{379} \). When the major mode is Null, Preflight Prep, Mated Idle, Mated Flight, Presep or Postsep, \( V_{379} = V_{363} \). When the major mode is TAEM, Approach & Landing or Rollout, \( V_{379} = V_{393} \).

\[ V_{363} = 0 \]
\[ V_{393} = DFN(X_{688})(\text{matrix values}) \]

SaveX Cell \( X_{688} \) contains Flight Path Conditions. For trajectory capture and steep glide slope conditions, \( V_{393} = 0.09 \) ms. For a shallow glide slope condition, \( V_{393} = 0.12 \) ms, and for the final flare condition, \( V_{393} = 0.08 \) ms.

The computation time for \( V_{370} \) is thus a function of major mode and flight path conditional states, and ranges between 0. and 120 \( \mu \)s.

o. Routine 308 (TAEM Navigation) - Variable 357

\[ V_{357} = 1.9 + V_{358} \]
\[ V_{358} = DFN(X_{682})(\text{matrix values}) \]

The computation time of this variable is a constant of 1.9 ms plus a variable time which is a discrete function of the state of the Major Mode. For the Null, Preflight Prep, and Mated Idle states the variable time is 1.05 ms. For all other major mode states the variable time is 0.75 ms. Computation time for this routine is therefore between 2.65 ms and 3.95 ms.

p. Routine 309 (IMU Major Functions) - Variable 353

\[ V_{353} = DFN(X_{682})(\text{matrix values}) \]

The computation time for Variable \( V_{353} \), is a discrete function of the state of the Major Mode. For NULL and Preflight Prep the computation time is 6.0 ms. For all other major modes the computation time is 5.3 ms.
q. Routine 310 (IMU Attitude and Nav-Base to Cluster Transformation) - Variable 354
   \[ V_{354} = DFN(V_{366}, X_{682})(\text{matrix values}) \]
   \[ V_{366} = X_{681}'2 = 80\,\text{ms time slice} \]

   The computation time of variable 354 is a discrete function of the 80 ms processing time slice and the Major Mode condition. Minimum time is 0.85 ms and occurs when the major mode is any mode other than NULL or Preflight Prep and the computation is within an 80 ms time cycle. The maximum time is 2.5 ms and occurs when the Major Mode is either NULL or Preflight Prep and the computation is not within an 80 ms time cycle.

r. Routine 312 (Redundancy Management) - Variable 428
   \[ V_{428} = V_{394} \times 0.48 \]
   \[ V_{394} = DFN(X_{700})(\text{matrix values}) \]

   Savex Cell \( X_{700} \) is the 80 ms time slice counter which maintains a sequential count of the number of 80 ms time slices for each 960 ms time span. \( V_{394} \) will have a specific computation time depending on the time slice counter. These values are:

<table>
<thead>
<tr>
<th>Value of Time Slice Counter</th>
<th>Value of ( V_{394} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.25 ms</td>
</tr>
<tr>
<td>2</td>
<td>0.075 ms</td>
</tr>
<tr>
<td>3</td>
<td>0.116 ms</td>
</tr>
<tr>
<td>4</td>
<td>0.316 ms</td>
</tr>
<tr>
<td>5</td>
<td>0.105 ms</td>
</tr>
<tr>
<td>6</td>
<td>0.098 ms</td>
</tr>
<tr>
<td>7</td>
<td>0.238 ms</td>
</tr>
<tr>
<td>8</td>
<td>0.129 ms</td>
</tr>
<tr>
<td>9</td>
<td>0.128 ms</td>
</tr>
<tr>
<td>10</td>
<td>0.220 ms</td>
</tr>
<tr>
<td>11</td>
<td>0.093 ms</td>
</tr>
<tr>
<td>12</td>
<td>0.154 ms</td>
</tr>
</tbody>
</table>

   Therefore, this variable will have a computation time ranging from 75 \( \mu \)s to 316 \( \mu \)s.

s. Routine 315 (Mated Drop, Warm Up, and Raw Data Processing) - Variable 396
   \[ V_{396} = 5.986 + V_{367}(V_{362} + V_{395} + 0.125) + V_{390} \]
   \[ V_{362} = \text{Computation Time for Routine 303} \]
   \[ V_{367} = \text{Platform Release} \]
   \[ V_{390} = \text{Computation Time for Routine 304} \]
   \[ V_{395} = DFN(X_{682})(\text{matrix values}) \]

   The value of variable 395 is a discrete function of the Major Mode. For all modes except Approach & Landing, and Roll Out, \( V_{395} = 0.15 \) ms. For the latter two modes, \( V_{395} = 85 \mu \)s. The value of \( V_{362} \) will range from 0.56 to 0.59 ms (see sub "k"). The use of the times defined by \( V_{362} \) and \( V_{395} \) for \( V_{396} \) is dependent on the platform release condition. These variables are a part of the computation time if the platform is in a
released condition. The value of V390 will range from 0.1 ms to 0.485 ms (see sub "l"). From the above values, V396 will have a range between 6.036 ms and 7.336 ms.

t. Routine 316 (Systems Management Performance Monitoring) - Variable 425
V425 = DFN (X685) (matrix values)
The computation time for this routine is a function of the Keyboard & Applications Control Savex setting. Normal computation time is 130 microseconds, but when Specialist Key Special Computations is requested, the computation time increases to 320 μsec.

5.2.4.3 Variables. The Variables for the computation time of routines were discussed in the previous paragraphs.

The other variables used in this model for the ALT Space Shuttle simulation are for the following areas:

a. System Conditions
b. Sinks or Sources for Messages
c. Time Setting and Generation
d. Task Branching
e. Go/No-Go Setting
f. Access Time for Mass Memory
g. Memory determination for each of four Virtual Machines

They are discussed below in the same order.

5.2.4.3.1 System Conditions.

V367 = X684'2
This variable tests the value of Savex Cell X684 to determine, through remainder division by 2, if the last bit of the value is a "1" or a "0". When the last bit is a "1", it indicates that the IMU platform is released.

b. Condition for Routine GMA Operation - Variable 378
V378 = DFN (X682, V367) (matrix values)
X682 is the Major Mode Savex Cell
V367 is the Platform Release variable.
This variable sets the condition that the routine GMA will operate only when the Major Mode is MATED-IDLE and the IMU platform has not been released.
5.2.4.3.2 Message Sources and Sinks.

a. Sinks for FF messages.
The FF MDMs are Device numbers: 6009, 60010, 60011, and 60012. Message transmissions are sent to these devices by Variable 380.

\[ V_{380} = P_8 + 60008 \]

- \( P_8 \) = Number of transmissions remaining for a message.
- \( 60008 \) = Device number used as an index for determining the device identification to which transmissions are to be sent.

b. Sinks for FA Messages
FA MDM Device numbers are: 60013, 60014, 60015, and 60016. Message transmissions are sent to these devices by Variable 381.

\[ V_{381} = P_8 + 60012 \]

c. Sinks for DDU Messages.
The device numbers of the DDU units are: 60017, 60018, and 60019. Message transmissions are sent to these units via Variable 382.

\[ V_{382} = P_8 + 60016 \]

d. Sinks for ICC Messages
ICC message Sinks will be GPC memory units which are identified in the model by the numbers 70001, 70002, 70003, and 70004. Messages to these units are sent via Variable 384.

\[ V_{384} = P_8 + 70001 \]

e. Sources for ICC Messages
The memory units 70001, 70002, 70003, and 70004 are both the source and sink for ICC messages. To control the source of these message transmission, the Variable 383 is used.

\[ V_{383} = P_7 + 70001 \]

- \( P_7 \) is the number of transmissions remaining for a message to be used for determining transmission sources.

5.2.4.3.3 Time Settings and Time Generation.


\[ V_{371} = V_{375} + V_{376} \]

- \( V_{375} = \text{DFN} (V_{372}, V_{373}) \) (matrix values)
- \( V_{376} = \text{DFN} (V_{374}) \) (matrix values)
- \( V_{372} = C1'80 \)
- \( V_{373} = C1'320 \)
- \( V_{374} = C1'2000 \)

Savex 681 indicates the processing time slice. Values for time slices of 40, 80, 160, 320, 1000, and 2000 are generated by performing remainder division of clock time \( (V_{372}, V_{373}, \text{and } V_{374}) \) and by defining logical bit settings \( (V_{375} \text{ and } V_{376}) \) for the results, followed by combination of these results.
b. 80 MS Time Slice
For some model routines a simple indicator of the presence or absence of the 80 ms time is required. This is accomplished via Variable 367.
\[ V367 = X681'2 \]

Upon performing remainder division by 2, a result of 1 indicates an 80 ms time slice.

5.2.4.3.4 Task Branching.

a. Branching conditions for the User Interface Function - DMC.
Branching to internal IMSIM locations is a function of the setting of Savex 685 (Keyboard and Application Control) and is defined by Variable 388 as follows:
\[ V388 = DFN (X685)(20090 1, 20100 2, 20150 3, 20162 4, 20181 5, 20015 6) \]

b. Branching conditions for GUG tasks (Display Checkout Control) are required for numerical keyboard inputs. These branches to internal IMSIM locations are defined by Variable 389 as follows:
\[ V389 = DFN (X699)(2014 0, 2017 10, 20104 11, 20130 12, 2014 13, 20104 16) \]

5.2.4.3.5 Go/NoGo Settings. Model variables V401 through V418 and V420 through V423 are used to establish Go or NoGo conditions for tasks. In all cases, this condition is accomplished via a corresponding IMSIM GATE.

Listed below are the Go/NoGo variables used in the model:

\[
\begin{align*}
V401 &= G1501 & V409 &= G1509 & V417 &= G1517 \\
V402 &= G1502 & V410 &= G1510 & V418 &= G1518 \\
V403 &= G1503 & V411 &= G1511 & V420 &= G1520 \\
V404 &= G1504 & V412 &= G1512 & V421 &= G1521 \\
V405 &= G1505 & V413 &= G1513 & V422 &= G1522 \\
V406 &= G1506 & V414 &= G1514 & V423 &= G1523 \\
V407 &= G1507 & V415 &= G1515 \\
V408 &= G1508 & V416 &= G1516
\end{align*}
\]
5.2.4.3.6 Mass Memory Access Time. Mass Memory access time is specified as having a range of 500 ms to 8000 ms. This condition is simulated by Variable 399.

\[ V_{399} = X_{44} + V_{400} \]
\[ V_{400} = CFN \times (RFI) \times (\text{Matrix Values}) \]
\[ X_{44} \] is a Savex constant of 500 ms.
\[ V_{400} \] is a randomly generated value having a range of 0 to 7500 ms.

5.2.4.3.7 Memory Determination for each of the four Virtual Machines.

a. Variable 422 is used for the memory definition of each of the tasks. It is a function of the job, and the appropriate tasks are initiated in each of the four GPCs.
\[ V_{442} = X(V_{29}) + 69999. \]

b. Memory Determination for ICC messages. Variable 384 is used for the memory determination of the ICC messages generated by each of the four GPCs. It is a function of the job number in each GPC.
\[ V_{384} = DFN \times (X(V_{29}))(70002 2 \ 70003 3 \ 70004 4 \ 70001 5) \]
5.2.4.4 Savex Cells and Gates

5.2.4.4.1 Savex Cell Utilization. A group of Savex Cells has been designated and used for NASA-Unique conditional requirements, systems conditions, counters, and miscellaneous functions.

The utilization of these Savex Cells and the values associated with their use follows:

- **X638** - START TIME FOR UTILIZATION REPORTS
- **X639** - LIGHT
  - 00 = NO LIGHT ALARM
  - 01 = LIGHT ALARM EVENT
- **X640** - TIME MGT
  - 00 = NOT ENABLED
  - 01 = TIME MANAGEMENT ENABLED
- **X641** - DOWNLIST
  - 00 = NOT ENABLED
  - 01 = DOWNLIST ENABLED
- **X642** - 40 MS TIME SLICE COUNTER
- **X643** - FUNCTION ABORT COUNTER
- **X656** - START TIME GROUP 1 FUNCTIONS (40 & 80 MS)
- **X657** - START TIME GROUP 2 FUNCTIONS (50, 100, 200, & 500 MS)
- **X658** - START TIME GROUP 3 FUNCTIONS (320 MS)
- **X659** - START TIME GROUP 4 FUNCTIONS (1000 & 2000 MS)
- **X660** - START TIME GROUP 5 FUNCTIONS (2 MS)
- **X681** - TIME SLICE
  - 00000 = 40 MS
  - 00001 = 80 MS
  - 00010 = 160 MS
  - 00100 = 320 MS
  - 01000 = 1000 MS
  - 10000 = 2000 MS
- **X682** - MAJOR
  - 00 = NULL
  - 01 = PREFLIGHT PREP
  - 10 = MATED IDLE
  - 11 = MATED FLIGHT
  - 12 = SEPARATION PRESEP
  - 13 = SEPARATION POSTSEP
  - 14 = TAEM
  - 15 = APPROACH & LANDING
  - 16 = ROLLOUT
30 April 1976

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
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<tr>
<td></td>
<td>02 = AUTO-RY</td>
</tr>
<tr>
<td></td>
<td>03 = AUTO-BF</td>
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<tr>
<td></td>
<td>11 = CAS-P</td>
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<td>12 = CAS-RY</td>
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<td>13 = CAS-BF</td>
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<td>21 = MD-P</td>
</tr>
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<td></td>
<td>22 = MD-RY</td>
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<tr>
<td></td>
<td>23 = MD-BF</td>
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<tr>
<td>X684</td>
<td>FLIGHT CONDITIONS:</td>
</tr>
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<td>00000 =</td>
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<tr>
<td></td>
<td>00001 = IMU PLATFORM RELEASED</td>
</tr>
<tr>
<td></td>
<td>00010 = NWSE</td>
</tr>
<tr>
<td></td>
<td>00100 = WONG</td>
</tr>
<tr>
<td></td>
<td>01000 = WOWLON</td>
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<tr>
<td></td>
<td>10000 = FLAT TURN</td>
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<tr>
<td>X685</td>
<td>KEYBRD &amp; APPLICAT. CONTROL:</td>
</tr>
<tr>
<td></td>
<td>01 = TERMINATE SPEC KEY</td>
</tr>
<tr>
<td></td>
<td>02 = IMU OPERATIONS SPEC KEY</td>
</tr>
<tr>
<td></td>
<td>03 = FGS/DED.DISPL C.O SPEC KEY</td>
</tr>
<tr>
<td></td>
<td>04 = SPECIAL COMPUT SPEC KEY</td>
</tr>
<tr>
<td></td>
<td>05 = MODE CHANGE OPS KEY</td>
</tr>
<tr>
<td></td>
<td>06 = CLEAR NO SIM</td>
</tr>
<tr>
<td></td>
<td>07 = FAULT NO SIM</td>
</tr>
<tr>
<td></td>
<td>08 = RESUME SIM</td>
</tr>
<tr>
<td></td>
<td>09 = EXECUTE SIM</td>
</tr>
<tr>
<td></td>
<td>10 = PRO SIM</td>
</tr>
<tr>
<td></td>
<td>11 = ITEM SIM</td>
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<td></td>
<td>12 = ACK NO SIM</td>
</tr>
<tr>
<td></td>
<td>13 = MSG RESET NO SIM</td>
</tr>
<tr>
<td></td>
<td>14 = RETURN NO SUPPORT</td>
</tr>
<tr>
<td></td>
<td>15 = CMPTR/CRT NO SIM</td>
</tr>
<tr>
<td></td>
<td>16 = CMPTR/BUS NO SIM</td>
</tr>
<tr>
<td></td>
<td>19 = DISPLAY SIM</td>
</tr>
<tr>
<td></td>
<td>20 = ENTER NO SIM</td>
</tr>
<tr>
<td></td>
<td>21 = TRANSFER NO SUPPORT</td>
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<td>X687</td>
<td>DISPLAY</td>
</tr>
<tr>
<td></td>
<td>00 = DISPLAY UPDATE</td>
</tr>
<tr>
<td></td>
<td>01 = NEW DISPLAY</td>
</tr>
<tr>
<td>X688</td>
<td>A &amp; L STATES:</td>
</tr>
<tr>
<td></td>
<td>01 = TRAJECTORY CAPTURE</td>
</tr>
<tr>
<td></td>
<td>02 = STEEP GLIDE SLOPE</td>
</tr>
<tr>
<td></td>
<td>03 = SHALLOW GLIDE SLOPE</td>
</tr>
<tr>
<td></td>
<td>04 = FINAL FLARE</td>
</tr>
</tbody>
</table>
X689 - MAJOR
  MODES
  SM:
  00 = IDLE
  01 = SYSTEM MONITOR
  02 = PRE TAKE OFF
  03 = SYSTEM MONITOR
  04 = PRE DROP
  05 = SYSTEM MONITOR

X695 - CURRENT MAJOR MODE SM

X696 - CURRENT MAJOR MODE GN&C

X697 - 50 MS TIME SLICE COUNTER: 1 - 10

X698 - TERMINATE
  00 = NO TERMINATE ACTION
  01 = TERMINATE ACTION TAKEN

X699 - NUMERICAL KEYBOARD INPUTS: 1 - 99

X700 - 80 MS TIME SLICE COUNTER: 1 - 12
5.2.4.4.2 Gate Utilization. Gates 1501 through 1523 have been used as communication gates between the generated transactions and the prototype tasks to activate the proper tasks at the proper intervals. A gate setting of "1" will activate, whereas a setting of "0" specifies a "No-Go" condition. Gate 1551 has been used as the processing gate for S.M. data acquisition processing. A "1" setting provides processing. Gate 1552 has been used for a "Terminate" action for the various functions. Setting of this gate to "1" presents a "Terminate" condition for designated task.

5.2.4.5 Parameterization. The model has been parameterized with the parameters listed in Appendix B under NASA.SPECS10.DATA (for one Virtual Machine with four GPCs) and under NASA.SPECS20.DATA (for simulation with four Virtual Machines).

5.2.5 Model Execution (S.O.W. 2.1.5)

This section describes the work performed under task 2.1.5 as defined in the Statement of Work (Exhibit "A") of the contract.

a. A battery of simulation runs was executed. The first set of runs was geared towards overall loading of the model and the cyclic execution of all its tasks. The runs went through the major phases of flight. Details of these simulation run executions are found in paragraph 5.2.5.1.

b. The second set of runs was concentrated on peak loads developing during flight. Based on the cyclic nature of the software functions and the intervals between function executions, peak loading will occur every 16 seconds when all cyclic functions culminate and compete for the CPU, and every four seconds, when all but the 320 ms functions are activated. Details of these simulation run executions are found in paragraph 5.2.5.2.

c. A third set of runs was based on certain flight segments to determine if any bottlenecks would develop in any segment. Details of these simulation run executions are found in paragraph 5.2.5.3.

d. A fourth set of runs was based on four separate Virtual Machines, with each GPC depicting one Virtual Machine. Details of these simulation run executions are found in paragraph 5.2.5.4. Software variations were made in the second, third, and fourth set of simulation runs, when the new operational System Logic as specified in the ALT Detailed Design Specification for FCOS, User Interface, and System Control was incorporated in the model specifications. Hardware variations were based on the concepts of one Virtual Machine with the four GPCs operating in the redundant mode, versus four Virtual Machines each with one GPC. These variations were exercised within the second set and the fourth set of executed simulation runs.

In order to facilitate simulated situations that create peak loads, the start times of the cyclic functions were controlled in some sets of runs by the setting of Savex Cells 656 through 660 as indicated in Table 5-2. The functions were grouped together by cyclic intervals as follows:
Table 5-2. Function Grouping for Start Times

<table>
<thead>
<tr>
<th>Group</th>
<th>Savex</th>
<th>Tasks</th>
<th>No.</th>
<th>Time Interval</th>
</tr>
</thead>
<tbody>
<tr>
<td>A = 1</td>
<td>656</td>
<td>GEF</td>
<td>6</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td></td>
<td>AIE</td>
<td>7</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GAD</td>
<td>8</td>
<td>40</td>
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<tr>
<td></td>
<td></td>
<td>GMA</td>
<td>9</td>
<td>40</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GEM</td>
<td>10</td>
<td>80</td>
</tr>
<tr>
<td>B = 2</td>
<td>657</td>
<td>SDM DA</td>
<td>11</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCI</td>
<td>35</td>
<td>100</td>
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<tr>
<td></td>
<td></td>
<td>DMI</td>
<td>32</td>
<td>200</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SDM PM</td>
<td>12</td>
<td>500</td>
</tr>
<tr>
<td>C = 3</td>
<td>658</td>
<td>GMG</td>
<td>19</td>
<td>320</td>
</tr>
<tr>
<td>D = 4</td>
<td>659</td>
<td>ARA</td>
<td>37</td>
<td>1000</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GEN</td>
<td>15</td>
<td>2000</td>
</tr>
<tr>
<td>E = 5</td>
<td>660</td>
<td>GTX</td>
<td>24</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>GMX</td>
<td>22</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GMY</td>
<td>23</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GMT/U/V</td>
<td>21</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GMS</td>
<td>20</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DMC</td>
<td>34</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SM OPS2</td>
<td>13</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SPM</td>
<td>14</td>
<td>2</td>
</tr>
</tbody>
</table>

The results of the model execution through the four sets of simulation runs are discussed in Section 2 - Results, Section 3 - Conclusions, and Section 5.2.6 - Test Analysis.
5.2.5.1 Initial Set of Simulation Runs. The first part of this set of runs was to validate the model. After the validation runs that exercised all modeled software and hardware, a time line, hereafter called a 'jobschedule' was developed that encompassed all major modes of flight, and started the second part of this set. The start time for the job was specified at 20 ms, at which time the IMSIM executive has completed its initiation cycle.

Specialist functions were fed in through the jobschedule at various subsequent times.

This jobschedule is given in Table 5.3. The first column in the table indicates the time (in milliseconds) at which the job or event is introduced to the system.

The second column specifies the job to be initiated. A zero in this column indicates that the next four fields are events to be set in Savex Cells (column 3 = Savex Cell number, column 4 = value to be set in this Savex, column 5 = 2nd Savex Cell number (if any), column 6 = value to be set in this 2nd Savex, if applicable).

Table 5.3. Jobschedule JSCA02

<table>
<thead>
<tr>
<th>Time (ms)</th>
<th>Savex Cell</th>
<th>Event 1</th>
<th>Event 2</th>
<th>Event 3</th>
<th>Event 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>682</td>
<td>Preflight</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>150</td>
<td>682</td>
<td>Display Checkout</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>150</td>
<td>689</td>
<td>-do.-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1000</td>
<td>682</td>
<td>Mated Idle</td>
<td></td>
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</tr>
<tr>
<td>1200</td>
<td>684</td>
<td>IMU Released</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1500</td>
<td>682</td>
<td>Mated Flight</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>1800</td>
<td>682</td>
<td>Presep</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1900</td>
<td>683</td>
<td>AUTO-RY</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2100</td>
<td>682</td>
<td>Postsep</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2200</td>
<td>685</td>
<td>IMU Ops</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2201</td>
<td>699</td>
<td>IMU Alignment</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2300</td>
<td>685</td>
<td>IMU Ops</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2301</td>
<td>699</td>
<td>IMU Attitude</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2400</td>
<td>683</td>
<td>CAS-RY</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3000</td>
<td>682</td>
<td>TAEM</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3200</td>
<td>683</td>
<td>MD-BF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3250</td>
<td>682</td>
<td>Approach &amp; Landing</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3300</td>
<td>684 10000</td>
<td>Flat turn</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3350</td>
<td>688</td>
<td>Trajectory capture</td>
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</tr>
<tr>
<td>3400</td>
<td>688</td>
<td>Steep glide slope</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3450</td>
<td>688</td>
<td>Shallow glide slope</td>
<td></td>
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<tr>
<td>3500</td>
<td>688</td>
<td>Final flare</td>
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</tr>
</tbody>
</table>
Table 5-3 presents a time-sequenced list of this workload schedule. The job for the ALT Configuration of the Space Shuttle will start at time 20 (ms). At the same time, the Major Mode is set to "Preflight" by means of setting Savex Cell X682 to 1. At 150 ms the Display Checkout Specialist Function is selected by means of setting Savex Cell X685 to 3 and Savex Cell X699 to 2.

At 1 sec (1000 ms), the Major Mode is changed to "Mated Idle" by increasing X682 by 9. 200 ms later, the IMU Release is simulated (controlled by X584). At time 1500, the Major Mode changes to "Mated Flight" and at time 1800, to "Preseparation". The Navigational State is set to AUTO-RY at time 1900 by means of X683 and at time 2100, the "Postseparation" mode is entered. At time 2200 the IMU ops "IMU Alignment" is activated (X685 = 2 and X699 = 10), while 100 ms later the IMU ops "IMU Attitude" (X685 = 2, X699 = 12) is simulated. At time 2400, the Navigation State is changed to CAS-RY (X683 = 12). A change to Major Mode "TAEM" is activated at time 3000. During the last 500 ms, the Major Mode is changed to "Approach Landing". The Navigational State is changed, and the Trajectory Capture and Glide Slope is simulated.

In running with this jobschedule, it became apparent that between time 150 ms and 1000 ms, only the routine cyclic functions executed repeatedly without change in state. For analysis purposes, this was of little value. A more compacted timeline sequence of workload was constructed, thereby avoiding long segments of routine cyclic operations. This jobschedule then became the standard schedule used for the other runs in the previously defined first set of executed simulation runs (Table 5-4).

<table>
<thead>
<tr>
<th>JOBSCHEDULE</th>
<th>JSCA03</th>
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<tbody>
<tr>
<td>20</td>
<td>2</td>
</tr>
<tr>
<td>25</td>
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</tr>
<tr>
<td>100</td>
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<td>1200</td>
<td>0</td>
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<tr>
<td>1250</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 5-4. Compacted Jobschedule JS5CA03
5.2.5.2 Concentrated Segment Runs. Simulation runs executed in this set were based on the theory that due to the cyclic nature of part of the Shuttle's functions, and the intervals between the cyclic execution of these functions, peak loads were developed at certain times.

Based on intervals of 40 ms, 50 ms, 80 ms, 100 ms, 200 ms, 320 ms, 500 ms, 1000 ms, and 2000 ms, this would occur at 4-second and 16-second intervals, when all cyclic functions would compete for usage of the CPU.

A timeline was developed that would simulate this situation. The jobschedule for this set of runs is given in Table 5-5. Flight state and conditions were preset at the start of these runs.

Table 5-5. Concentrated Jobschedule JSCA05

<table>
<thead>
<tr>
<th>JOBSCHEDULE --</th>
<th>JSCA05</th>
</tr>
</thead>
<tbody>
<tr>
<td>JOB START</td>
<td></td>
</tr>
<tr>
<td>FCS DISPLAYS</td>
<td></td>
</tr>
<tr>
<td>AUTO-RY</td>
<td></td>
</tr>
<tr>
<td>IMU OPS - ALIGNMENT</td>
<td></td>
</tr>
<tr>
<td>PREDROP MODE SM</td>
<td></td>
</tr>
<tr>
<td>CAS-RY</td>
<td></td>
</tr>
<tr>
<td>IMU OPS - CALIBRATION</td>
<td></td>
</tr>
<tr>
<td>TAEM MODE GN&amp;C</td>
<td></td>
</tr>
<tr>
<td>SYSTEM MONITOR MODE SM</td>
<td></td>
</tr>
<tr>
<td>CAS-P</td>
<td></td>
</tr>
<tr>
<td>MD-BF</td>
<td></td>
</tr>
<tr>
<td>INIT. AUTO-LAND DISPLAY</td>
<td></td>
</tr>
<tr>
<td>APPROACH &amp; LANDING MODE GN&amp;C</td>
<td></td>
</tr>
<tr>
<td>ND-P</td>
<td></td>
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<tr>
<td>ND-P</td>
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</tr>
<tr>
<td>FLAT TURN</td>
<td></td>
</tr>
<tr>
<td>END AUTO-LAND DISPLAY</td>
<td></td>
</tr>
<tr>
<td>END FLAT TURN</td>
<td></td>
</tr>
<tr>
<td>TRAJECTORY CAPTURE</td>
<td></td>
</tr>
<tr>
<td>STEEP GLIDE SLOPE</td>
<td></td>
</tr>
<tr>
<td>FIRST FLARE DISPLAY</td>
<td></td>
</tr>
<tr>
<td>SHALLOW GLIDE SLOPE</td>
<td></td>
</tr>
<tr>
<td>END FIRST FLARE DISPLAY</td>
<td></td>
</tr>
<tr>
<td>PULL UP &amp; FLARE DISPLAY</td>
<td></td>
</tr>
<tr>
<td>FINAL FLARE</td>
<td></td>
</tr>
<tr>
<td>WOWLON</td>
<td></td>
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<tr>
<td>WONG</td>
<td></td>
</tr>
<tr>
<td>AUTO-BF</td>
<td></td>
</tr>
<tr>
<td>IDLE MODE GN&amp;C</td>
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</tr>
<tr>
<td>IDLE MODE SM</td>
<td></td>
</tr>
</tbody>
</table>
The preset conditions for this jobschedule were:

- \( S_X638 = 72000 \) "START TIME FOR UTILIZATION REPORT"
- \( S_X640 = 1 \) "TIME MGT ENABLED"
- \( S_X641 = 1 \) "DOWNLIST ENABLED"
- \( S_X656 = 72000 \) "START TIME GROUP 1 TASKS"
- \( S_X657 = 72000 \) "START TIME GROUP 2 TASKS"
- \( S_X658 = /2000 \) "START TIME GROUP 3 TASKS"
- \( S_X659 = 72000 \) "START TIME GROUP 4 TASKS"
- \( S_X660 = 72000 \) "START TIME GROUP 5 TASKS"
- \( S_X682 = 12 \) "PRESEP GN&C MODE"
- \( S_X683 = 1 \) "AUTO-P"
- \( S_X684 = 1 \) "IMU RELEASED"
- \( S_X689 = 3 \) "SYSTEM MONITOR SM MODE"
- \( S_X695 = 3 \) "PRESENT SM MODE"
- \( S_X696 = 12 \) "PRESENT GN&C MODE"

One Specialist Function that was simulated at time \( 72200 \), viz. IMU calibration, in all probability would not be done in flight. Therefore, this jobschedule was changed to JSCA06 replacing this Specialist Function.

The new jobschedule JSCA06 is shown in Table 5-6.
Table 5-6. Concentrated Jobschedule JSCA06

```
'JOBSCHEDULE -- JSCA06

'job start
71095 2 699 2 'FCS displays
72010 0 685 5 683 1 'auto-ry
72075 0 685 2 699 10 'imu ops - alignment
72125 0 685 5 689 1 'predrop mode sm
72160 0 685 10 683 10 'cas-ry
72200 0 685 2 699 12 'imu ops - attitude
72240 0 685 5 682 2 'taem mode gn&c
72265 0 685 5 689 1 'system monitor mode sm
72290 0 685 5 683 -1 'cas-p
72340 0 685 5 683 12 'md-bf
72350 0 685 19 687 1 'init. auto-land display
72375 0 685 5 682 1 'approach & landing mode gn&c
72390 0 685 10 683 -2 'md-p
72410 0 684 10000 'flat turn
72450 0 687 -1 'end auto-land display
72500 0 687 -10000 'end flat turn
72510 0 688 1 'trajectory capture
72550 0 688 1 'steep glide slope
72575 0 687 1 'first flare display
72650 0 688 1 'shallow glide slope
72675 0 687 -1 'end first flare display
72680 0 687 1 'pull up & flare display
72700 0 688 1 'final flare
72750 0 684 10000 'wowlon
72800 0 684 100 'wong
72805 0 685 5 683 -18 'auto-bf
72875 0 685 5 682 -5 'idle mode gn&c
72900 0 685 5 689 -5 'idle mode sm
```

This jobschedule became the standard schedule for execution control in this set of tests.
Preset conditions for these runs were:

- $S \ X638 = 72000$  
  "START TIME FOR UTILIZATION REPORT"
- $S \ X640 = 1$  
  "TIME MGT ENABLED"
- $S \ X641 = 1$  
  "DOWNLIST ENABLED"
- $S \ X656 = 72000$  
  "START TIME GROUP 1 TASKS"
- $S \ X657 = 72000$  
  "START TIME GROUP 2 TASKS"
- $S \ X658 = 72000$  
  "START TIME GROUP 3 TASKS"
- $S \ X659 = 72245$  
  "START TIME GROUP 4 TASKS"
- $S \ X660 = 72000$  
  "START TIME GROUP 5 TASKS"
- $S \ X682 = 12$  
  "PRESEP GN&C MODE"
- $S \ X683 = 1$  
  "AUTO-P"
- $S \ X684 = 1$  
  "IMU RELEASED"
- $S \ X689 = 3$  
  "SYSTEM MONITOR SM MODE"
- $S \ X695 = 3$  
  "PRESENT SM MODE"
- $S \ X696 = 12$  
  "PRESENT GN&C MODE"

The jobschedule in Table 5-6 was also the basis for the variations in hardware from one Virtual Machine to four Virtual Machines.

5.2.5.3 ALT Flight Segment Runs. In addition to the runs described in paragraphs 5.2.5.1 and 5.2.5.2, jobschedules were developed for running particular flight segments. A timeline for this purpose is given in Table 5-7.
Table 5-7. Jobschedule JSCA07 for Flight Segments

<table>
<thead>
<tr>
<th>JOBSCHEDULE</th>
<th>JSCA07</th>
</tr>
</thead>
<tbody>
<tr>
<td>31095 2</td>
<td>JOB START</td>
</tr>
<tr>
<td>32010 0 685 3 699 2</td>
<td>FCS DISPLAYS</td>
</tr>
<tr>
<td>32050 0 685 5 683 1</td>
<td>AUTO-RY</td>
</tr>
<tr>
<td>32075 0 685 2 699 10</td>
<td>IMU OPS - ALIGNMENT</td>
</tr>
<tr>
<td>32125 0 685 5 689 1</td>
<td>PREDROP MODE SM</td>
</tr>
<tr>
<td>32160 0 685 10 683 10</td>
<td>CAS-RI</td>
</tr>
<tr>
<td>32200 0 685 2 699 12</td>
<td>IMU OPS - ATTITUDE</td>
</tr>
<tr>
<td>32240 0 685 5 682 1</td>
<td>SEP. MODE</td>
</tr>
<tr>
<td>32350 0 685 5 68 1</td>
<td>POST SEP.</td>
</tr>
<tr>
<td>32375 0 685 5 683 -1</td>
<td>CAS-P</td>
</tr>
<tr>
<td>32400 0 685 5 689 1</td>
<td>SYSTEM MONITOR MODE SM</td>
</tr>
<tr>
<td>32450 0 685 5 683 12</td>
<td>MD-BF</td>
</tr>
<tr>
<td>32600 0 685 5 689 1</td>
<td>TAEM</td>
</tr>
</tbody>
</table>

Preset conditions for these runs were:

S X640 = 1 "TIME MGT ENABLED"
S X641 = 1 "DOWNLIST ENABLED"
S X656 = 32000 "START TIME GROUP 1 TASKS"
S X657 = 32000 "START TIME GROUP 2 TASKS"
S X658 = 32000 "START TIME GROUP 3 TASKS"
S X659 = 32245 "START TIME GROUP 4 TASKS"
S X660 = 32000 "START TIME GROUP 5 TASKS"
S X682 = 11 "MATED FLIGHT"
S X683 = 1 "AUTO-P"
S X684 = 1 "IMU RELEASED"
S X689 = 3 "SYSTEM MONITOR SM MODE"
S X695 = 3 "PRESENT SM MODE"
S X696 = 11 "PRESENT GN&C MODE"
5.2.5.4 Multiple Virtual Machine Runs. A set of simulation runs was executed in which each GPC was simulated as a separate virtual machine. All GPCs are active, but only one performs the actual message transmission to MDMs. All four virtual machines transmit and receive ICC messages. Specification File NASA.SPECS20.DATA was used for these runs.

The jobschedule developed for these runs is given in Table 5-8, with each Virtual Machine assigned its own job.

Table 5-8. Jobschedule JSCA08 for Four Virtual Machines.

```
  71995   2       JOBSCHEDULE -- JSCA08
  71995   3
  71995   4
  71995   5
 72010   0  685   3  699   2  FCS DISPLAYS
 72050   0  685   5  683   1  AUTO-RY
 72075   0  685   2  699  10  IMU OPS - ALIGNMENT
 72125   0  685   5  689   1  FREDROP MODE SM
 72160   0  685  10  683  10  CAS-RY
 72200   0  685   2  699  12  IMU OPS - ATTITUDE
 72240   0  685   5  682   2  TAEM MODE GN&C
 72265   0  685   5  689   1  SYSTEM MONITOR MODE SM
 72290   0  685   5  683  -1  CAS-P
 72340   0  685   5  683  12  MD-BF
 72350   0  685  19  687   1  INIT. AUTO-LAND DISPLAY
 72375   0  685   5  682   1  APPROACH & LANDING MODE GN&C
 72390   0  685  10  683  -2  MD-P
 72410   0  684  10000  FLAT TURN
 72450   0  687   -1  END AUTO-LAND DISPLAY
 72500   0  684  -10000  END FLAT TURN
 72510   0  688   1  TRAJECTORY CAPTURE
 72550   0  688   1  STEEP GLIDE SLOPE
 72575   0  687   1  FIRST FLARE DISPLAY
 72650   0  688   1  SHALLOW GLIDE SLOPE
 72675   0  687   -1  END FIRST FLARE DISPLAY
 72680   0  687   1  PULL UP & FLARE DISPLAY
 72700   0  688   1  FINAL FLARE
 72750   0  684  10000  WOWLON
 72800   0  684    100  WONG
 72805   0  685   5  683  -18  AUTO-BF
 72875   0  685   5  682  -5  IDLE MODE GN&C
 72900   0  685   5  689  -5  IDLE MODE SM
```

Preset conditions for these runs were:

\[
\begin{align*}
S &\ x638 = 72000 & \text{''START TIME FOR UTILIZATION REPORT} \\
S &\ x640 = 1 & \text{''TIME MGT ENABLED} \\
S &\ x641 = 1 & \text{''DOWNLIST ENABLED} \\
S &\ x656 = 72000 & \text{''START TIME GROUP 1 TASKS} \\
S &\ x657 = 72000 & \text{''START TIME GROUP 2 TASKS} \\
S &\ x658 = 72000 & \text{''START TIME GROUP 3 TASKS} \\
S &\ x659 = 72245 & \text{''START TIME GROUP 4 TASKS} \\
S &\ x660 = 72000 & \text{''START TIME GROUP 5 TASKS} \\
S &\ x682 = 12 & \text{''PRESEP GN&C MODE} \\
S &\ x683 = 1 & \text{''AUTO-P} \\
S &\ x684 = 1 & \text{''IMU RELEASED} \\
S &\ x689 = 3 & \text{''SYSTEM MONITOR SM MODE} \\
S &\ x695 = 3 & \text{''PRESENT SM MODE} \\
S &\ x696 = 12 & \text{''PRESENT GN&C MODE}
\end{align*}
\]
5.2.6 Test Analysis and Documentation (S.O.W. 2.1.6).

The following paragraphs describe in detail the work performed under this task. It included preparation of a draft Test Plan (Reference 5) which was submitted to NASA in January 1976, and which culminated in this Final Report.

5.2.6.1 Simulation Results. The simulation runs executed as described in paragraph 5.2.4 produced an abundance of results by means of history printouts and statistical reports.

A short description of these types of reports follows.

a. Statistical Reports.
   For a quick analysis, 10 statistical reports were printed out at the end of each simulation run.
   1. Job and Task Reports.
      Reports numbered 2 and 4 gave statistical data on the total number of jobs, tasks, and messages that are initiated, completed, interrupted, delayed, in progress, number of activations, etc.
   2. Utilization Reports.
      Reports 13 through 18 provided statistical data for processors, memories storages, devices, data links, and data sets. These reports gave utilization of processors, devices, etc.; total usage, maximum and average times and rates.
      
      Each prototype report was repeated for as many units as are specified on the input forms, e.g., one copy of report 16 for each central processor.
   3. Backlog Reports.
      Reports 20 and 21 provided the transaction backlog with maximum, average and current figures plus the average delay time in ms for the key blocks in the model.

b. Data Flow Reports.
   These reports presented the activities that took place in the model during a simulation run. They are also considered to be history printouts.
   1. Message Reports.
      Reports 5 and 6 gave all the particulars for each of the data flow messages, such as message length, origin (source), and destination (sink) of the data message, time of occurrence, transmission rate, data bus number, etc.
   2. Job Reports. Reports 8 and 9 indicated at what time a job started and finished and total time consumed for job execution.
   3. Task Reports.
      Reports 25 through 28 and report 31 gave all details of task transactions during a run such as start and finish of a task, execution time, message wait, task interruption, computation time, etc.
c. Control Reports.
These reports were provided to detect situations in which capacities are exceeded or unusual activities take place. Report 12 gave a printout of errors occurring during a simulation run. Report 42 was used as a control tool to evaluate the various system capacities during a simulation run.

The report numbering is not sequential as numbered reports were changed, added, or deleted during previous versions of IMSIM.

Representative printouts of these reports followed concentrated simulation runs as defined in Section 5.2.5.2, and are given in Appendix D for the Statistical Reports and Control Reports, and in Appendix C for the Data Flow Reports that occurred during these simulation runs.

The results of the analysis of these runs and reports is given in Section 2 - Results, and in Section 3 - Conclusions, of this Final Report.

Some runs were plotted for easier analysis of delays and functional interruptions. Part of such a plot of a concentrated simulation run is given in Figure 2-2.

It is clear that every 40 ms the System Software Interface Processor and the Fast Cycle Executive interfere with each other as the Fast Cycle Executive gets interrupted every 40 ms time slice because of its lower priority. An offset timewise of 10 ms in every 40 ms cycle could solve this problem.

Lower priority tasks experience delays in their execution from 1 ms up to 58 ms (see Figure 2-3).

5.2.6.2 Backlogs and Delays. Many of the problems of congestion and contention for resources which are present in most data processing systems are automatically measured and reported during simulation runs using IMSIM. The DDPS design eliminates the possibility of a number of these problems. Furthermore, some of the measurements gathered by IMSIM relate directly to input specifications and parameters, and therefore provide no insight into the dynamic system behavior. Data which are meaningful in the context of DDPS simulation are extracted from the general simulation results and presented in Section 2.

The following discussion pertains to the general results, as printed in reports 20 and 21, and may prove useful in indicating problems which the DDPS design has avoided or minimized.

Scheduled processes are essentially independent of each other (i.e., they are not organized in predecessor-successor relationships), so that backlogs of dependent tasks - measured in IMSIM block 1138 - do not develop.

Memory is allocated and programs and data loaded as required for major functions of the ALT, prior to the Mated/Drop Test. Thus, the nominal allocation activity - measured in IMSIM block 1151 - is not relevant to the DDPS model. For the same reason, the following measurements are not meaningful:

a. the backlog of program elements which cannot be allocated due to lack of space in virtual memory - block 1488
b. program elements currently in loading - block 1495
c. executive (FCOS) service for loading of program elements - block 1935
d. time spent in consolidating virtual memory space - block 1936

e. the backlog of elements waiting for space in specific memory units - block 6002

f. the backlog of elements waiting for space in any memory units - block 10052.

The time used by FCOS in activating processes is integrated with the scheduled processes, and job/task initiation service - measured by block 1204 - is bypassed.

The number of scheduled processes in the DDPS does not vary with time. Thus, block 1201, which measures the number of schedulable tasks, simply records the number of scheduled processes introduced to the model.

Statistics relating to processes in actual execution (i.e., having a CPU assigned) are recorded in two IMSIM blocks - block 1184 measures task execution with given computational values, while block 1192 measures execution with generated computation as needed to simulate production of output messages. Times recorded in these blocks are fragmented by task interruptions and thus indicate only the time periods continuously devoted to individual tasks. Data for these blocks, from various simulation runs, are shown in Appendix D.

Tasks which enter a "wait" state for completion of I/O are recorded in IMSIM block 1182. These data are presented for various simulation runs in Appendix D.

The DDPS is not configured as a multiprocessor (i.e., two or more CPUs cannot address the same main memory unit). IMSIM block 1185 records interference between processors in addressing the same memory; it has no useful information for the DDPS simulation.

The queue of processes that are ready for dispatching, either as the result of scheduling or as a consequence of interruption by higher priority processes, is represented by the backlog of tasks recorded in IMSIM block 3032. Data pertaining to this backlog for various simulation runs is shown in Appendix D.

So-called cyclic scheduling of IMSIM is not the same as the scheduling of cyclic processes within the DDPS. Rather, it refers to a "round robin" scheduling algorithm; since the latter is not simulated, the data pertaining to task queues for this type of scheduling - recorded in blocks 3004 and 3005 - are absent in summary printouts of DDPS simulation runs.

Task switchover time (i.e., the time it takes FCOS to store the status of an interrupted process and establish status for the interrupting task) is assumed to be well below the 1 ms threshold of time resolution, and statistics on switchover time - recorded in IMSIM block 3089 - are not significant.

As defined for IMSIM, "sink-driven" messages represent transmissions which are initiated in conjunction with task execution. If they are to be deferred until some time after the start of a task, a "start" specification is included in the message definition (IMSIM Form 5). IMSIM block 1605 records statistics
on message delays due to the start conditions. If a sequence of transmissions is defined as a sink-driven message, IMSIM block 1846 records statistics on the times between successive transmissions of the message. Sink-driven message transmissions are kept in synchronization with tasks as required and statistics on sync delays are recorded in block 1847; no such sync delays were recorded for DDPS transmissions.

All DDPS processes are described as repeatable or "cyclic" tasks to IMSIM. Since block 1601 records data for noncyclic tasks, it has no function in the DDPS model.

Only response messages were characterized as "source-driven" for the DDPS model; this was done to achieve responses independently of process performance. Thus, statistics on source-driven message delays for transmission starts - recorded in blocks 1608 and 1851 - is irrelevant to the DDPS model. Response time is specified as an input parameter via IMSIM Form 5; statistics on response transmission response periods is recorded in block 1675.

Since the DDPS software is designed as a single, integrated unit, there is no need to employ the concept of "nonsharable" resources (i.e., resources such as bus terminals which must be reserved for use by a single task). Thus, backlog statistics on tasks which must acquire nonsharable resources - recorded in IMSIM blocks 1682 and 1686 - are not relevant.

Mass memory is not employed in the Mated/Drop Test simulation and since no other components of the DDPS are represented as auxiliary storage devices for data transmission, statistics relating to the use of such components - recorded in blocks 1706, 1707, and 1748 - are not relevant.

No statistics are recorded on I/O initiation and completion interrupt service, since these functions are incorporated in the software representation and are assumed to require negligible processor time (considering the 1 ms time resolution of the DDPS model); thus data on periods during which these functions are performed - recorded in blocks 1693 and 1808 - are absent.

Statistics were recorded in the backlogs which develop when message transmissions are deferred due to current use of a data bus or bus terminal required for the transmission. These data are recorded in blocks 1708, 1712, 1738, and 8005. No backlogs of this nature were observed in the DDPS simulation runs.

Since multiplexed transmission links are not employed in the DDPS model, statistics on acquisition of such links - recorded by block 1734 - are absent.

Statistics were gathered on transmission backlogs which develop as the result of I/O saturation of memory (i.e., a condition in which a sufficient portion of the memory access cycles are being utilized during a period to preclude additional, fixed-rate transmission). These data are recorded in blocks 1751 and 1753. No backlogs of this nature were observed in the DDPS simulation runs.

The IMSIM block 1754 records data concerning the transmission periods of all messages which are sent during a simulation run.
Reset periods for bus terminals were defined as zero, to represent negligible time periods. Thus, data gathered on device reset periods in IMSIM block 9052 are not meaningful.

5.2.6.3 Unresolved Problems. The results of this dynamic loading analysis study will be affected by the change in the logic for the Guidance, Navigation and Control functions. This change occurred with the release of new detailed GN&C data that were received in February 1976, after tasks 1 through 4 reached scheduled completion. Further effort is required to define the new requirements for those functions and to assess the impact on the Shuttle Orbiter DDPS by modeling these newly developed requirements (see Section 4.2, item b).

Completion of these activities will result in an effective augmentation of the recently completed ALT simulation analyses, and will supply a deeper insight into the feasibility of performing ALT functions under stress conditions.

5.2.6.4 Documentation. The documentation part of this task resulted in the following publications:


b. Ten monthly Progress Reports, TM-(L)-5561/001/00 through TM-(L)-5561/010/00, issued at end of each month during the contract period (DRL Item No. 1).

c. A Final Report on DDPS Dynamic Loading Analysis, TM-(L)-5658/000/00 dated 30 April 1976 (DRL Item No. 2).

No related written or oral presentations at professional meetings or in professional journals were made in the course of this contract. Thus, no publications were made by SDC in conjunction with DRL Item No. 3, "Revision of Technical Information Releases".
APPENDIX A

NASA.REVAR15.DATA

This Appendix provides the matrix values of the Variables, discussed in paragraphs 5.2.4.2 and 5.2.4.3, and the revisions, discussed in paragraph 5.2.4.1, which were used in the IMSIM 03B model.

"" NASA.REVAR15.DATA - 03/22/76
""VARIABLES:

""COMP TIME FOR ROUTINE 301
V350 = (0.98 + V351 + V352) * 0.48

V351 = DFN (X683, X684)(
0.225 1 0
0.23 1 1
0.26 1 2
0.18 1 4
0.23 1 8
0.485 2 0
0.475 2 2
0.43 2 4
0.485 2 8
0.295 2 16
0 3 0
0.035 3 2
0 3 4
0.211 11 0
0.615 12 0
0.615 12 8
0 13 0
0.035 13 2
0 13 4
0.16 21 0
0.24 22 0
0 23 0)

V352 = DFN (X681, X682)(
0.31 0 0
2.2 1 0
2.15 1 12
2.5 1 13
2.565 1 14
2.67 1 16
4.685 2 0
4.635 2 12
4.985 2 13
5.05 2 14
5.155 2 16
4.685 4 0
4.635 4 12
4.985  4  13
5.05   4  14
5.155  4  16
1.0    8  0
1.03   8  16
2.890  9  0
2.840  9  12
3.19   9  13
3.255  9  14
3.39   9  16
5.375  11  0
5.325  11  12
5.675  11  13
5.74   11  14
5.875  11  16
5.375  15  0
5.325  15  12
5.675  15  13
5.74   15  14
5.875  15  16
2.89   16  0
2.84   16  12
3.19   16  13
3.255  16  14
3.39   16  16
5.375  19  0
5.325  19  12
5.675  19  13
5.74   19  14
5.875  19  16

'COMP TIME FOR ROUTINE 309
V353 = DFN (X682) (2.88 0
     2.544 10)

'COMP TIME FOR ROUTINE 310
V354 = DFN (V366, X682) (1.2 0 0
     0.84 0 10
     0.48 1 0
     0.408 1 10)

'COMP TIME FOR ROUTINE 42
V355 = 0.744 + (RF1) * 0.144

'COMP TIME FOR ROUTINE 45
V356 = 0.3456 + (RF1) * 0.0528

'COMP TIME FOR ROUTINE 308
V357 = (1.9 + V358) * 0.48
V358 = DFN (X682) (1.05 0
     0.75 11)
'COMP TIME FOR ROUTINE 31
V359 = DFN (X700)(
    0   0
    0.0144 6
    0   7
    0.0144 12)

'COMP TIME FOR ROUTINE 302
V360 = DFN (V366, V367)(
    365 0 0
    363 0 1
    365 1 1)

V361 = V(V360)

'COMP TIME FOR ROUTINE 303
V362 = (0.56 + (RF1) * 0.03) * 0.48
V363 = X73 - X73

'COMP TIME FOR ROUTINES 134 & 135
V364 = (0.5 + (RF1) * 30 + X44) * 0.48
V365 = V362 + V356 + 0.3168

'80 MS TIMESLICE
V366 = X681'2

'PLATFORM RELEASE
V367 = X684'2

'COMP TIME FOR ROUTINE 306
V368 = (X44 + V369) * 0.48
V369 = DFN (X682)(
    0.3 0
    0.34 10
    0.16 15
    0.34 16)

'COMP TIME FOR ROUTINE 307
V370 = V(V379)

'SET TIME FOR SAVEX 681
V371 = V375 + V376
V372 = C1'80
V373 = C1'320
V374 = C1'2000

V375 = DFN (V372, V373)(
    111  0  0
    001  0  40
    011  0  160
    001  0  200
    000  40  0)

V376 = DFN (V374)(
    11000  0
    0  40
    1000  1000
    0  1040)

"SET TIME SLICE COUNTER X700
V377 = X700'12 + 1"

"CONDITION FOR CMA OPERATION
V378 = DFN (X682, V367)(
    1  0  0
    0  10  0
    1  10  1)

"COMP TIME FOR ROUTINE 307
V379 = DFN (X682)(
    363  0
    393  15)

"SINKS FOR FF MESSAGES
V380 = P8 + 60008

"SINKS FOR FA MESSAGES
V381 = P8 + 60012

"SINKS FOR DDU MESSAGES
V382 = P8 + 60016

"SOURCES FOR ICC MESSAGES
V383 = P7 + 70001

"SINKS FOR ICC MESSAGES
V384 = P8 + 70001

"NEW DISPLAY DETERMINATION
V385 = DFN (X685)(
    0  0
    1  1
    0  6
    1  19
COMP TIME FOR ROUTINE 155
V386 = DFN (G1551)(
  0.0024 0
  0.096 1)

COMP TIME FOR ROUTINE 317
V387 = DFN (G1551)(
  0.0456 0
  0.12 1)

V388 = DFN (X685)(
  20090 1
  20100 2
  20150 3
  20162 4
  20181 5
  20015 6)

BRANCHES FOR GUC TASKS
V389 = DFN (X699)(
  20104 0
  20110 10
  20104 11
  20130 12
  20140 13
  20104 16)

COMP TIME FOR ROUTINE 304
V390 = (0.09 + V391) * 0.48
V391 = 0.01 + X687 * V392

V392 = DFN (X685, X682)(
  0.38 0 0
  0.345 0 14
  0.375 0 15
  0.385 0 16
  0 3 0
  0.38 4 0
  0.345 4 14
  0.375 4 15
  0.385 4 16
  0.345 5 14
  0.375 5 15
  0.385 5 16
  0 6 0)

COMP TIME FOR ROUTINE 307
```
V393 = \text{DFN} (X688) (\hspace{1em})
\begin{align*}
0.0432 & 1 \\
0.0576 & 3 \\
0.0354 & 4 \\
\end{align*}
''COMP TIME FOR ROUTINE 312
V394 = \text{DFN} (X700) (\hspace{1em})
\begin{align*}
0.25 & 1 \\
0.075 & 2 \\
0.116 & 3 \\
0.316 & 4 \\
0.105 & 5 \\
0.098 & 6 \\
0.238 & 7 \\
0.129 & 8 \\
0.128 & 9 \\
0.22 & 10 \\
0.093 & 11 \\
0.154 & 12 \\
\end{align*}
''COMP TIME FOR ROUTINE 315
V395 = \text{DFN} (X682) (\hspace{1em})
\begin{align*}
0.15 & 0 \\
0.085 & 15 \\
\end{align*}
''COMP TIME FOR ROUTINE 315
V396 = (5.986 + V367 \times (V395 + 0.125)) \times 0.48 + V367 \times V362 + V390
''COMP TIME FOR ROUTINE 63
V397 = (V398 + X44) \times 0.48
V398 = \text{DFN} (X685) (\hspace{1em})
\begin{align*}
0.005 & 1 \\
0.125 & 2 \\
\end{align*}
''MASS MEMORY ACCESS TIME
V399 = X44 + V400
V400 = \text{CFN} (RF1) (\hspace{1em})
\begin{align*}
0 & 0 \\
100 & 0.1 \\
500 & 0.2 \\
1000 & 0.3 \\
1600 & 0.4 \\
2300 & 0.5 \\
3100 & 0.6 \\
4000 & 0.7 \\
5000 & 0.8 \\
6200 & 0.9 \\
\end{align*}
```
7500  0.99)

'GO/NO GO SETTING TASKS
V401 = G1501
V402 = G1502
V403 = G1503
V404 = G1504
V405 = G1505
V406 = G1506
V407 = G1507
V408 = G1508
V409 = G1509
V410 = G1510
V411 = G1511
V412 = G1512
V413 = G1513
V414 = G1514
V415 = G1515
V416 = G1516
V417 = G1517
V418 = G1518
V419 = DFN (X698, X682)(
    1  0  0
    0  0  2)
V420 = G1520
V421 = G1521
V422 = G1522
V423 = G1523

'TIME SLICE COUNTER FOR DATA ACQ
V424 = X697'10 + 1

'COMP TIME FOR ROUTINE 316
V425 = DFN (X685)(
    0.0624  0
    0.1536  4
    0.0624  5)

'FOR GATE SETTING PROC BUFFER
V427 = DFN (RF1)(
    1  0.0
    0  0.75)

'COMP TIME FOR ROUTINE 312
V428 = V394 * 0.48

'COMP AS FN(40MS CTR) ROUTINES 140 & 151
V429 = (1 - X642'X45/(X642'X45)) * X44
"COMP TIME FOR ROUTINE 140
V430 = V429 * X639

"COMP TIME FOR ROUTINE 313
V431 = DFN (X685)(
  1.56    1    "SPEC
  1.204   5    "OPS
  2.51    8    "RESUME
  0.396   9    "EXEC & PRO
  0.662   11   "ITEM
  2.51   19)  "DISPLAY

"COMP TIME FOR ROUTINE 149
V432 = DFN (X685)(
  0.384    0
  1.104    1
)

"MSG LENGTH FOR DEU DISPLAY IMAGE
V433 = DFN (X685)(
  0    0
  1024    1
  0    8
  1024    19
  0    20
)

"MSG LENGTH FOR KEYBD INP
V434 = DFN (X685)(
  0    0
  10    1
)

"COMP TIME FOR ROUTINE 314
V435 = X44*3 + X45*X687

"ADDITION FOR COUNTER X643
V436 = X577$X577

" CONDITIONS FOR OPERATION OF GEF AND GAD
V437 = DFN (X682)(
  1503    0
  1501    11
)
V438 = DFN (X682)(
  8    0
  6    11
)

"CONDITION FOR CLEARING X699 KEYBD INPUT
V439 = X699 * X698

"CHECK FOR SPEC TERMINATE ACTION
V440 = DFN (X699)(

''CONDITION FOR GEN OPERATION
V441 = DFN (X682, V367)
    0  0  0
    1 14  1
 0  15  0

''IMSIM REVISIONS
V9 = FT(IC2)/((C1 - X638)*100$1
V10 = DFN (X(V47) X(V42))(1 0 0 0 0 0 1 0 0)
V232 = (C1 - X638)*X90/1000
V306 = B1192 + B1184
V442 = X(V29) + 69999

20000 GEN  40  0  X656  0  42
  X642 + 1
  X681 = V371
  ADMIT IF X577 = 0
  P3 = 1502
  P4 = 7
COPY TO 20013
  P3 = 1504
  P4 = 9
COPY TO 20013 V378
  P3 = V437
  P4 = V438
TRY 20013

20010 GEN  80  0  X656  0  40
  X700 = V377
  P3 = 1507
  P4 = 18
COPY TO 20013

20011 DETOUR 20015
  ADMIT IF X682 GE 11
  ADMIT IF X577 = 0
  P3 = 1505
  P4 = 10

20013 G(P3) = 1
  X577 = P4
  PR1 + 0
G(P3) = 0
PRINT R 30 30
X643 + V436
X577 = 0
20015 REMOVE
20020 GEN 100 0 X657 0 40
ADMIT IF X577 = 0
P3 = 1517
P4 = 35 "CYCLIC DISPLAY PROC - DCI
TRY 20013
20030 GEN 320 0 X658 0 40
ADMIT IF X577 = 0
P3 = 1508
P4 = 19 "MAJOR CYCLE EXEC - GMG
COPY TO V440
TRY 20013
20040 GEN 200 0 X657 0 40
ADMIT IF X577 = 0
P3 = 1514
P4 = 32 "MCDS INPUT PROC - DMI
TRY 20013
20050 GEN 1000 0 X659 0 40
ADMIT IF X577 = 0
P3 = 1518
P4 = 37 "GPC SWITCH MONITOR - ARA
TRY 20013
20060 GEN 2000 0 X659 0 40
ADMIT IF X577 = 0
P3 = 1506
P4 = 15 "TAEM NAV CYCLIC EXEC - GEN
COPY TO 20013 V441
TRY 20105
20070 GEN 2 0 X660 0 41
ADMIT IF X685 GQ 1
ADMIT IF X577 = 0
X577 = 34 "USER INTERFACE - DMC
G1516 = 1
PR1 + 0
G1516 = 0
20071 PRINT R 30 30
X643 + V436
X577 = 0
20072 DELAY 1
COPY TO V388
X685 = 0
X687 = V385
REMOVE
"20080 GEN 100 0 X657 0 40
" ADMIT IF V419 = 1
"20081 ADMIT IF X577 = 0
P3 = 1515
P4 = 33

LDB I/O PROC - DGI

TRY 20013

20090 X698 = 1
TRY 20105

20100 TRY V389

20104 C(P3) = 1
X577 = P4
PR1 + 0
G(P3) = 0

20106 PRINT R 30 30
X643 + V436
X577 = 0
X699 - V439
X698 = 0

20105 REMOVE

20110 G1511 = 1
X577 = 22
PR1 + 0
G1511 = 0

ADMIT IF X577 = 0

20112 P3 = 1512
P4 = 23
TRY 20104

20130 P3 = 1509
P4 = 20
TRY 20104

20140 P3 = 1510
P4 = 21
TRY 20104

20150 DETOUR 20015
ADMIT IF X699 = 2

20151 P3 = 1513
P4 = 24
''FCS/DD DEDICATED DISPLAY CH.OUT - GTX
TRY 20104

20160 GEN 50 0 X657 0 40
X697 = V424
G1551 = V427
''SET TIME SLICE
''SET GATE PROC BUFFER

20161 ADMIT IF X577 = 0
P3 = 1520
P4 = 11
''SM DATA ACQ
TRY 20013

20162 G1551 = 1
TRY 20161

20170 GEN 500 0 X657 0 40
ADMIT IF X697 = 1
''ONCE EVERY 10 CYCLES
ADMIT IF X577 = 0
P3 = 1521
P4 = 12
''SM PERFORM MONITOR
TRY 20013
DURING V232 SECONDS OF SIMULATED SHUTTLE OPERATIONS
A TOTAL OF BW1160 DIFFERENT FUNCTIONS WERE INTRODUCED.
THESE FUNCTIONS WERE ACTIVATED BW1166 TIMES, STATUS IS:
BW1196 WERE COMPLETED
B1167 ARE WAITING FOR NEXT ACTIVATION
B3032 ARE IN READY STATE, I.E. WAITING FOR CPU
B1182 ARE WAITING FOR MESSAGES TO COMPLETE
V306 PRESENTLY EXECUTING, I.E. IN ACTIVE STATE
FUNCTIONS WERE INTERRUPTED BW2000 TIMES.
X643 FUNCTION ACTIVATIONS WERE ABORTED AS FUNCTION STILL ACTIVE. ENDR
REPORT 3 1 1 0
NOT APPLICABLE FOR NASA. ENDR
REPORT 30 1 1 X577
AT TIME C1 ACTIVATION FOR FUNCTION X577 ABORTED, AS
FUNCTION X577 IS STILL ACTIVE. ENDR
REVISE 39000 39000
"SPEED-UP BY ELIMINATING PROTOTYPES"
REVISE 238000 238000
"SET SAVEX FROM JOBSCHEDULE"
REVISE 649000 661000
TRY 1352

REVISE 663000 680000
X(V67) = 1

''SPEED-UP BY ELIMINATING V.M. & MEM.RECO

REVISE 663000 680000
X(V67) = 1

''SPEED-UP BY ELIMIN. V.M. & MEMORY RECORDING

''SUPPRESS ZERO LENGTH TRANSMISSION

REVISE 881000 881000
''SUPPRESS ZERO LENGTH TRANSMISSION

DETOUR 1606
ADMIT IF P3 = 0
POP P2
TRY 1865
1606 P2 = P6

REVISE 1134000 1134000
''PREVENT COMP TIME FROM MESSAGES

ADMIT IF X(P2) = 1
SOURCE PRIMARY
END OF DATA
APPENDIX B

NASA.SPECS20.DATA

"NASA.SPECS20.DATA - 03/27/76"
"SIMULATION SPECIFICATIONS FOR SPACE SHUTTLE ORBITER"
"ONBOARD DATA PROCESSING SYSTEM"
"PRODUCED BY THE SYSTEM DEVELOPMENT CORPORATION"
"D...A ARE PREPARED ON IMSIM SPECIFICATION FORMS, AS DESCRIBED IN"
"SDC PUBLICATION TM-5328/102, "IMSIM INFORMATION MANAGEMENT SYSTEM"
"SIMULATOR USER'S MANUAL".

"**** JOBS "*

FIVE JOBS ARE INCLUDED IN THE MODEL. JOB 1 IS RESERVED FOR THE
SIMULATION EXECUTIVE. JOBS 2 THROUGH 5 ENCOMPASS ALL
FUNCTIONS OF THE ONBOARD DATA PROCESSING SYSTEM.
JOB 2 REPRESENTS THE WORKLOAD FOR GPC 1,
JOB 3 REPRESENTS THE WORKLOAD FOR GPC 2, ETC.

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*** TASKS 1 THROUGH 6 ARE RESERVED FOR THE SIMULATION EXECUTIVE.***

*** TASKS NUMBERED ABOVE 100 ARE FOR THE REDUNDANT CPC'S ***

**GEF_FC_EXEC**  FAST CYCLE EXECUTIVE

**SCHEDULED AT 40MS INTERVALS BY GAV (20017) AND GAA (20016)***

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' ' ' 'AIE_SIP  SYSTEM SOFTWARE INTERFACE PROCESSOR 00002010
'SCHEDULED AT 40MS INTERVALS BY SYSTEM INITIALIZATION 00002020
'' CLASS DELAY REQUIRED ELEMENTS 00002030
  2 7 1 0  30116 30130 30138 30147 50028 * 00002040
  50058 30151 30140 1 00002050
  2 107 1 0  30116 30130 30138 30147 30151 30140 * 00002060
    50028 1 00002070
''
' ' ' 'GAD_MATE_IDLE  MATED/DROP TEST IDLE MODE - 200 00002080
'SCHEDULED AT 40MS INTERVALS BY GAA (20016) UNTIL MODE TRANSITION 00002090
'' CLASS DELAY REQUIRED ELEMENTS 00002100
  2 8 1 0  30302 30303 30045 30089 1 00002110
''
' ' ' 'GMA_MIN_EXEC  MINOR CYCLE EXECUTIVE 00002120
'SCHEDULED AT 40MS INTERVALS BY GAV (20017). IF MODE 200 IS ENTERED WHILE PLATFORM IS NOT RELEASED, GMA IS CANCELLED AND THEN RESCHEDULED AT MODE TRANSITION. 00002130
'' CLASS DELAY REQUIRED ELEMENTS 00002140
  2 9 1 0  30042 30303 30045 1 00002150
''
' ' ' 'GEM_MATE_DROP_EXEC  MATED/DROP EXECUTIVE 00002160
'SCHEDULED AT 80MS INTERVALS BY GAA (20016) FOR MODE 201. IF MODE 200 IS ENTERED, GEM IS CANCELLED. 00002170
'' CLASS DELAY REQUIRED ELEMENTS 00002180
  2 10 1 0  30304 30303 30305 30306 30089 30087 * 00002190
    30307 30312 30031 30315 1 00002200
''
' ' ' 'SDA_DATA_ACQUISITION  SM DATA ACQUISITION 00002210
'SCHEDULED AT 50MS INTERVALS BY SM OPS 1 00002220
'' CLASS DELAY REQUIRED ELEMENTS 00002230
  2 11 1 0  30155 50032 50033 1 00002240
  2 111 1 0  30155 1 00002250
''
' ' ' 'SDM_PERFORM_MON_CONTROL  SM PERFORMANCE MONITORING CONTROL 00002260
'SCHEDULED AT 500MS INTERVALS BY SM OPS 1 00002270
'' CLASS DELAY REQUIRED ELEMENTS 00002280
  2 12 1 0  30316 30317 1 00002290
''
' ' ' 'SFO_FLIGHT_OPS  SM FLIGHT OPERATIONAL SEQUENCE (OPS 2) 00002300
'SCHEDULED BY UI SOFTWARE (20034) 00002310
'' CLASS DELAY REQUIRED ELEMENTS 00002320
  2 13 1 0  30157 30316 1 00002330
''
' ' ' 'SPM_SUBSYS_CONFIG_MON  SM SUBSYSTEM CONFIGURATION MONITORING 00002340
'PRETAKEOFF & PEDROP SM SPECS SCHEDULED BY UI SOFTWARE (20034) 00002350
'' CLASS DELAY REQUIRED ELEMENTS 00002360
  2 14 1 0  30157 1 00002370
''
' ' ' 'GEN_TAEM_NAV_CYC  TAEM NAVIGATION CYCLIC EXECUTIVE 00002380
'SCHEDULED AT 2000MS INTERVALS BY SPEC GUC (20027) UPON PLATFORM 00002390
''RELEASE REQUEST
'' CLASS  DELAY  REQUIRED ELEMENTS  00002510
  2  15  5  0  30306  30308  1  00002520
''
''GAA OPS2 MATED_DROP_TEST  MATED/DROP OPS CONTROL SEGMENT  00002530
''SCHEDULED BY UI SOFTWARE (20034)  00002540
''SERVICE LOAD ASSUMED NEGLIGIBLE. LOGIC SIMULATED.  00002550
'' CLASS  DELAY  REQUIRED ELEMENTS  00002560
  16  1  0  00002570
''
''GAV_OPS1_PRE_FLT  PREFLIGHT OPS CONTROL SEGMENT  00002580
''SCHEDULED BY UI SOFTWARE (20034)  00002590
''SERVICE LOAD ASSUMED NEGLIGIBLE. LOGIC SIMULATED.  00002600
'' CLASS  DELAY  REQUIRED ELEMENTS  00002610
  17  1  0  30004  00002620
''
''GEP_PREFLT_EXEC  PREFLIGHT EXECUTIVE  00002630
''SCHEDULED AT 80MS INTERVALS BY GAV (20017) WHILE IN MODE 101  00002640
''NOT ACTIVE DURING MATED/DROP TEST  00002650
'' CLASS  DELAY  REQUIRED ELEMENTS  00002660
  18  1  0  30304  30029  30312  30315  1  00002670
''
''GMG_MAJ_EXEC  IMU MAJOR CYCLE EXECUTIVE  00002680
''SCHEDULED AT 320MS INTERVALS BY GMU/GMT/GMV (20021), GMX (20022),  00002690
''GMY (20023), AND GMS (20020), ALL OF WHICH ARE SCHEDULED BY  00002700
''SPEC GUC (20027).  00002710
'' CLASS  DELAY  REQUIRED ELEMENTS  00002720
  2  19  5  0  30309  30305  1  00002730
''
''GMS_IMU_ATT  IMU ATTITUDE DETERMINATION  00002740
''SCHEDULED BY GUC (20027)  00002750
'' CLASS  DELAY  REQUIRED ELEMENTS  00002760
  2  20  5  0  30310  1  00002770
''
''GMT_PFLT_CALA  IMU PREFLIGHT CALIBRATION A  00002780
''GMU_HANG_CALA  IMU HANGAR CALIBRATION A  00002790
''GMV_HANG_CALB  IMU HANGAR CALIBRATION B  00002800
''SCHEDULED BY GUC (20027)  00002810
'' CLASS  DELAY  REQUIRED ELEMENTS  00002820
  2  21  5  0  30311  1  00002830
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''GMX_GC_ALIGN  IMU GYROCOMPASS ALIGNMENT  00002840
''SCHEDULED BY GUC (20027)  00002850
'' CLASS  DELAY  REQUIRED ELEMENTS  00002860
  2  22  5  0  30062  1  00002870
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''GMY_VEL_TILT  IMU VELOCITY AND TILT  00002880
''SCHEDULED BY GUC (20027) TO FOLLOW GMX (20022)  00002890
'' CLASS  DELAY  REQUIRED ELEMENTS  00002900
  2  23  5  0  30063  1  00002910
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''GMS_VEL_ATT  IMU VELOCITY DETERMINATION  00002920
''SCHEDULED BY GUC (20027)  00002930
'' CLASS  DELAY  REQUIRED ELEMENTS  00002940
  2  24  5  0  30064  1  00002950
''
''GMY_VEL_TILT  IMU VELOCITY AND TILT  00002960
''SCHEDULED BY GUC (20027) TO FOLLOW GMX (20022)  00002970
'' CLASS  DELAY  REQUIRED ELEMENTS  00002980
  2  25  5  0  30065  1  00002990
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''GMY_VEL_TILT  IMU VELOCITY AND TILT  00003000
''SCHEDULED BY GUC (20027) TO FOLLOW GMX (20022)  00003010
'' CLASS  DELAY  REQUIRED ELEMENTS  00003020
  2  26  5  0  30066  1  00003030
''
''GMY_VEL_TILT  IMU VELOCITY AND TILT  00003040
''SCHEDULED BY GUC (20027) TO FOLLOW GMX (20022)  00003050
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''GMY_VEL_TILT  IMU VELOCITY AND TILT  00003120
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''SCHEDULED BY GUC (20027) TO FOLLOW GMX (20022)  00003170
'' CLASS  DELAY  REQUIRED ELEMENTS  00003180
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''GMY_VEL_TILT  IMU VELOCITY AND TILT  00003240
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''GMY_VEL_TILT  IMU VELOCITY AND TILT  00003360
''SCHEDULED BY GUC (20027) TO FOLLOW GMX (20022)  00003370
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CLASS DELAY REQUIRED ELEMENTS

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DGI_LDB_IO LDB I/O PROCESSOR
SCHEDULED AT REGULAR INTERVALS BY SYSTEM CONTROL/INITIALIZATION
NOT USED DURING MATED/DROP TEST
CLASS DELAY REQUIRED ELEMENTS
33 5 0 30136 30141 30149 1

DMC_SUPER USER INTERFACE
SCHEDULED BY SYSTEM INITIALIZATION
CLASS DELAY REQUIRED ELEMENTS
34 1 0 30313 50059 50060 1

DCY_CYCLE_DISPLAY CYCLIC DISPLAY PROCESSING
SCHEDULED AT 100MS INTERVALS BY SYSTEM INITIALIZATION
CLASS DELAY REQUIRED ELEMENTS
35 1 0 30314 50055 50056 50057 1

DDC_DOWNLST_CONTROLS DOWNLIST DATA CONTROLS PROCESSOR
SCHEDULED BY SPEC ASS, WHICH IS NOT INVOKED DURING MATED/DROP TEST
CLASS DELAY REQUIRED ELEMENTS
36 1 0 30135

ARA_GPC_SWITCH GPC SWITCH MONITOR
SCHEDULED AT 100MS INTERVALS BY SYSTEM INITIALIZATION
CLASS DELAY REQUIRED ELEMENTS
37 5 0 30118 1

DGS_SYNC GPC/PCMU DATA CYCLE SYNCHRONIZER
SCHEDULED BY DDC (20036)
NOT REQUESTED DURING OPS2. DCD IS ASSUMED TO BE ENABLED.
CLASS DELAY REQUIRED ELEMENTS
38 1 0 30134

SPO_PREFLIGHT_OPS SM PREFLIGHT OPERATIONAL SEQUENCE (OPS 1)
SCHEDULED BY UI SOFTWARE (20034)
NOT USED DURING MATED/DROP TEST
CLASS DELAY REQUIRED ELEMENTS
39 1 0

*** ROUTINES ***********************************************
EACH FUNCTION OR SET OF FUNCTIONS CALLED IN PERFORMANCE OF A
SCHEDULED TASK IS DEFINED AS A ROUTINE. ROUTINE 1 IS RESERVED
FOR THE SIMULATION EXECUTIVE. ROUTINES WITH NUMBERS GREATER
THAN 300 REPRESENT SETS OF FUNCTIONS.

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"PREFLIGHT OPS CONTROL SEGMENT (TASK 17)
  GAV_OPSI_PRE_FLT
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  4 0 110001 1 0 10 442 16 0.4

"PREFLIGHT EXECUTIVE (TASK 18)
  GEP_FRE_FLT_EXEC
  SHARE LIB.DS SIZE TIME PROCSTR MEMORY COMP.TIME
  29 0 110001 1 0 10 442 16 0.4

"NAVIGATION TRANSITION TASK
  GET_NAV_TRANS
  SHARE LIB.DS SIZE TIME PROCSTR MEMORY COMP.TIME
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"TAEM GUIDANCE (TASK 10)
  GGA_TAEM_GUID
  SHARE LIB.DS SIZE TIME PROCSTR MEMORY COMP.TIME
  3 31 1 110001 1 0 10 442 359 0

"IMU MINOR CYCLE EXECUTIVE (TASK 9)
  GMA_MIN_EXEC
  SHARE LIB.DS SIZE TIME PROCSTR MEMORY COMP.TIME
  3 42 1 110001 1 0 10 442 355 0

"IMU RESOLVER PROCESSOR (TASKS 8, 9)
  GMD_RES_PROC
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  3 45 1 110001 1 0 10 442 356 0

"IMU GYRO-COMPASS ALIGNMENT (TASK 22)
  GMY_GC_ALIGN
  SHARE LIB.DS SIZE TIME PROCSTR MEMORY COMP.TIME
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"IMU VELOCITY TILT (TASK 23)
  GMY_VEL_TILT
  SHARE LIB.DS SIZE TIME PROCSTR MEMORY COMP.TIME
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"FDI FCS SELECTION FILTER (TASKS 6, 10)
  GRA_FCS_SF
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"FDI NAVNAVID SELECTION FILTER (TASKS 8, 10)
  GRC_NAVNAVID_SF
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"SPEC HORIZONTAL SITUATION CONTROL SEGMENT (TASK 25),
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" "SPEC VERTICAL SITUATION CONTROL SEGMENT (TASK 26),
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" "SPEC IMU OPERATIONS CONTROL (TASK 27),
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" "SPEC FCS/DEDICATED DISPLAY CHECKOUT CONTROL SEGMENT (TASK 28),
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" "SPEC RM-NAVIGATION CONTROL SEGMENT (TASK 29),
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" "SPEC RM-CONT CONTROL SEGMENT (TASK 30),
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" "SPEC NAV/TARGET UPDATE CONTROL SEGMENT (TASK 31),
" SHARE LIB.DS SIZE TIME PROCsr MEMORY COMP.TIME
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" "RM-CONTROL KEYBOARD PROCESSOR (TASKS 16, 30),
" SHARE LIB.DS SIZE TIME PROCsr MEMORY COMP.TIME
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" "DD DEDICATED DISPLAY CHECKOUT (TASK 24),
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" "GPC LOCATOR,
" SHARE LIB.DS SIZE TIME PROCsr MEMORY COMP.TIME
" 114 0 110001 1080 0 10 442 16 0.24
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'GPC STARTUP
' AIC_GPC_STARTUP
' SHARE LIB.DS SIZE TIME PROCSR MEMORY COMP.TIME
115 0 110001 660 0 10 442 16 0.24

'SYSTEM INTERFACE PROCESSOR (TASK 7)
' AIC_SLP
' SHARE LIB.DS SIZE TIME PROCSR MEMORY COMP.TIME
3 116 0 110001 800 0 10 442 16 0.656

'GPC SWITCH MONITOR (TASK 37)
' ARA_GPC_SWITCH
' SHARE LIB.DS SIZE TIME PROCSR MEMORY COMP.TIME
3 118 0 110001 1300 0 10 442 16 0.214

'IDLE OPERATIONAL SEQUENCE
' ARB_IDLE_OPS
' SHARE LIB.DS SIZE TIME PROCSR MEMORY COMP.TIME
119 0 110001 600 0 10 442 16 0.038

'GPC RECONFIGURATION
' ARC_GPC_RECONFIG
' SHARE LIB.DS SIZE TIME PROCSR MEMORY COMP.TIME
120 0 110001 2280 0 10 442 16 0.384

'BUS CONFIGURATION CHANGE
' ARB_BUS_CHG
' SHARE LIB.DS SIZE TIME PROCSR MEMORY COMP.TIME
121 0 110001 5200 0 10 442 16 0.192

'GPC RECONFIGURATION TABLE CHANGE
' ARE_GPC_TABLE_CHG
' SHARE LIB.DS SIZE TIME PROCSR MEMORY COMP.TIME
122 0 110001 480 0 10 442 16 0.13

'DPS CONFIGURATION ITEM PROCESSOR
' ARF_DPS_CONFIG_ITEM
' SHARE LIB.DS SIZE TIME PROCSR MEMORY COMP.TIME
123 0 110001 1000 0 10 442 16 0.072

'GPC RECONFIGURATION MESSAGE HANDLER
' ARG_RECONFIG_MSG
' SHARE LIB.DS SIZE TIME PROCSR MEMORY COMP.TIME
124 1 110001 500 0 10 442 16 0.048

'SECONDARY GPC RECONFIGURATION
' ARH_SEC_GPC_RECONFIG
' SHARE LIB.DS SIZE TIME PROCSR MEMORY COMP.TIME
125 1 110001 1000 0 10 442 16 0.307
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''LIGHTS AND ALARM PROCESSING  (TASK 7)  
'' DLA_LIGHT_ALARM_PROC
'' SHARE LIB.DS SIZE TIME PROCSTR MEMORY COMP.TIME 00006010
3 140 1 110001 1600 0 10 442 430 0.24 10 00006040
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''LDB MESSAGE ROUTER  (TASK 33)
'' DLM_LDB_ROUT
'' SHARE LIB.DS SIZE TIME PROCSTR MEMORY COMP.TIME 00006080
141 1 110001 840 0 10 442 16 0.144 00006090
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''ICC MESSAGE ROUTER  (TASK 7)
'' DME_ICC_ROUT
'' SHARE LIB.DS SIZE TIME PROCSTR MEMORY COMP.TIME 00006130
147 1 110001 1260 0 10 442 16 0.087 00006140
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''MCDS INPUT PROCESSOR  (TASK 32)
'' DMI_MCDS_IN
'' SHARE LIB.DS SIZE TIME PROCSTR MEMORY COMP.TIME 00006180
148 0 110001 400 0 10 442 16 0.18 00006190
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''MCDS MESSAGE PROCESSOR  (TASKS 32, 33)
'' DMM_MCDS_PROCESS
'' SHARE LIB.DS SIZE TIME PROCSTR MEMORY COMP.TIME 00006230
149 1 110001 2200 0 10 442 432 00006240
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''FAULT MESSAGE SCAN  (TASK 7)
'' DMS_FMS
'' SHARE LIB.DS SIZE TIME PROCSTR MEMORY COMP.TIME 00006280
151 1 110001 480 0 10 442 429 0.216 10 00006290
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''MESSAGE LINE SUPPORT FUNCTION
'' ASSUME IMPLICIT IN APPLICATION CONTROL SEGMENTS
'' DMS_MSG_LSP
'' SHARE LIB.DS SIZE TIME PROCSTR MEMORY COMP.TIME 00006340
152 1 110001 3800 0 10 442 16 0.096 00006350
''
''APPLICATION MODIFYING AND SEQUENCING
'' DNX_BMS
'' ASSUME IMPLICIT IN APPLICATION CONTROL SEGMENTS
'' SHARE LIB.DS SIZE TIME PROCSTR MEMORY COMP.TIME 00006400
153 1 110001 1000 0 10 442 16 0.096 00006410
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''TIME HOMOGENEOUS DATA REQUEST PROCESSOR
'' DTH_TIME_HOMO
'' SHARE LIB.DS SIZE TIME PROCSTR MEMORY COMP.TIME 00006450
154 1 110001 300 0 10 442 16 0.144 00006460
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''SYSTEMS MANAGEMENT DATA ACQUISITION  (TASK 11)
'' SDA_DATA_ACQUISITION
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**Navigation (Tasks 10, 15)**
- **GNA MLS MEAS**: MLS MEASUREMENT PROCESSING
- **GNB_TACAN MEAS**: TACAN MEASUREMENT PROCESSING
- **GNF_BARO_ALT**: BARO-ALTIMETER MEASUREMENT PROCESSING
- **GND_RADAR_ALT**: RADAR-ALTIMETER MEASUREMENT PROCESSING
- **GNE_NAV EXEC**: NAVIGATION EXECUTIVE
- **GN1_DATA SNAP**: DATA SAVING
- **GN3_meas SCHEDLR**: MEASUREMENT SCHEDULER
- **GN7_NAV FILTER**: FILTER

**Guidance (Task 10)**
- **GBH_AL GUID**: APPROACH/LANDING GUIDANCE
- **GCC_P_TRAJ**: PITCH TRAJECTORY
- **GGD_TRAJ_CAP**: TRAJECTORY CAPTURE
- **GGE SGS**: STEEP GLIDESLOPE
- **GGF_P SGS**: FLARE & SHALLOW GLIDESLOPE
- **GGC_FF**: FINAL FLARE
- **GGH_P_SYNC**: PITCH SYNCHRONIZATION
- **GGG_R_CMD**: ROLL COMMAND

**Taem Navigation (Task 15)**
- **GEN_TAEM NAV EXEC**: CYCLIC EXECUTIVE
- **GNN2_INFALT HARDSTAND**: INFLIGHT/HARDSTAND UPDATE
- **GNN4_COV RECONF**: STATE & COVARIANCE RECONFIGURATION
- **GNN5_AVG_G DP**: DOUBLE PRECISION AVERAGE G
- **GNN6_COV PROP**: COVARIANCE MATRIX PROPAGATION

**IMU Major Functions (Task 19)**

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GDE ADI_PROC: DEDICATED DISPLAY ADI PROCESSOR
CDF_HSI_PROC: DEDICATED DISPLAY HSI PROCESSOR
GDI Disp_PROC: CRT DISPLAY PROCESSOR
GNN IMU MODING: IMU MODING
GFC AD CALC: AIR-DATA CALCULATIONS

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30 April 1976
System Development Corporation
B-15
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System Development Corporation

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TM-(L)-5658/000/00

GMG_MAJ_EXEC MAJOR CYCLE EXECUTIVE 00007510
GMU_T_UPDATE TRANSFORM UPDATE 00007520
GMJ_TOR_TRSF TORQUING TRANSFORM 00007530
GMN_LAT_FUNC LARGE ANGLE TORQUING 00007540
GMQ_LSF_FILF LEAST SQUARES FILTER 00007550
SHARE LIB.DS SIZE TIME PROCUSR MEMORY COMP.TIME 00007560
3 309 1 110001 1 0 10 442 353 0 00007570

IMU ATTITUDE AND NAV-BASE TO CLUSTER TRANSFORMATION (TASK 20) 00007590

SHARE LIB.DS SIZE TIME PROCUSR MEMORY COMP.TIME 00007620
3 310 1 110001 1 0 10 442 354 0 00007630

IMU CALIBRATION (TASK 21) 00007660

SHARE LIB.DS SIZE TIME PROCUSR MEMORY COMP.TIME 00007690
3 311 1 110001 1 0 10 442 16 30.0 00007700

REDUNDANCY MANAGEMENT (TASKS 10, 18) 00007720

SHARE LIB.DS SIZE TIME PROCUSR MEMORY COMP.TIME 00007860
3 312 1 110001 1 0 10 442 428 0 00007870

USER INTERFACE SUPERVISOR (TASK 34) 00007890

SHARE LIB.DS SIZE TIME PROCUSR MEMORY COMP.TIME 00007990
3 313 0 110001 10380 0 10 442 431 00008000
"CYCLIC DISPLAY PROCESSING (TASK 35)
00008010
DCI#CYC CYCLIC DISPLAY PROCESSING 00008020
DCI#CON DATA CONVERSION 00008030
DCI#FMT DATA FORMATTING 00008040
SHARE LIB.DS SIZE TIME PROCSR MEMORY COMP.TIME 00008050
3 314 0 110001 5252 0 10 442 435 2.06 8.3 00008060
""MATED DROP, WARMUP, AND RAW DATA PROCESSING (TASKS 10, 18)
00008070
GEM_MATE_DROPC EXEC MATED/DROP EXECUTIVE 00008080
GGJ_AVG_G_SP SINGLE PRECISION AVERAGE G 00008090
GGK_USER_PARAM USER PARAMETERS 00008100
GPA_ADTA_DATA_PROC ADTA DATA PROCESSOR 00008110
GPM_MSLB_DATA_PROC MSLBS DATA PROCESSOR 00008120
GPR_RA_DATA_PROC RADAR ALTIMETER PROCESSOR 00008130
GPT_TACAN_DATA_PROC TACAN DATA PROCESSOR 00008140
GTM_TACAN_WARMUP TACAN WARM—UP 00008150
GTP_MSBLS_WARMUP MSLBS WARM—UP 00008160
GTR RA_WARMUP RADAR ALTIMETER WARM—UP 00008170
SHARE LIB.DA SIZE TIME PROCSR MEMORY COMP.TIME 00008180
3 315 0 110001 1 0 10 442 396 0 00008190
""SYSTEMS MANAGEMENT PERFORMANCE MONITORING (TASKS 12, 13)
00008200
SFD_FAULT_DETECT Annunci FAULT DETECTION & ANNUNCIATION 00008210
SPF_PRECON_PROCESS PRECONDITION PROCESSING 00008220
SSC_SPECIAL_COMP SPECIAL COMPUTATIONS 00008230
SAS_ANALOG_SCALE ANALOG SCALING 00008240
SHARE LIB.DS SIZE TIME PROCSR MEMORY COMP.TIME 00008250
3 316 1 110001 1 0 10 442 425 0 00008260
""PERFORMANCE MONITORING CONTROL (TASK 12)
00008270
SPM_PERFORM_MON CONTROL PM CONTROL 00008280
SHARE LIB.DS SIZE TIME PROCSR MEMORY COMP.TIME 00008290
3 317 1 110001 1 0 10 442 387 0 00008300
""MESSAGES
00008310
ALL DATA TRANSMISSIONS OF THE DPS ARE REPRESENTED AS MESSAGES.
MESSAGES 1 THROUGH 5 ARE RESERVED FOR THE SIMULATION EXECUTIVE.
READ FROM FF01, FF02, FF03 -
ACCELEROMETER ASSEMBLY (ACCLRM)
ROTATIONAL HAND CONTROLLER 1 & 2 (RH RHC)
SPEED/XF GTH CONTROLLER 1 & 2 (SBTC)
Rudder Pedal Transducer Assembly 1 & 2 (RPTA)
FF MDM DISCRETE
MATURE SOURCE SINK LENGTH INTERVAL START TOTAL SE T 00008320
5 6 0 70001 380 16 12 0 16 1 0 1 3 00008330
5 7 2 50006 70001 16 56 0 16 0 0 0 3 00008340
""
''READ FF04 MDM DISCRETES
  NATURE SOURCE SINK LENGTH INTERVAL START TOTAL SE T
  5 8 0 70001 60012 16 2 0 16 0 0 1 1 00008530
  5 9 2 50008 70001 16 24 0 16 0 0 0 1 00008550
''

''READ IMU FROM FF01, FF02, FF03
  NATURE SOURCE SINK LENGTH INTERVAL START TOTAL SE T
  5 10 0 70001 380 16 2 0 16 1 0 1 3 00008590
  5 11 2 50010 70001 16 28 0 16 0 0 0 3 00008600
''

''READ FROM FF01 -
  FWD ATTACH POINT VOLTAGE (LCA)
  AIR DATA TRANSUDER ASSEMBLY (ADTA)
  MSBL
  TACAN AND TACAN REGISTER
  RADAR ALTIMETER (RAD ALT)
  NATURE SOURCE SINK LENGTH INTERVAL START TOTAL SE T
  5 12 0 70001 60009 16 12 0 16 0 0 1 1 00008680
  5 13 2 50012 70001 16 32 0 16 0 0 0 1 00008700
''

''READ FROM FF02 -
  ADTA
  MSBL
  TACAN AND TACAN CONTROL REGISTER
  RAD ALT
  NATURE SOURCE SINK LENGTH INTERVAL START TOTAL SE T
  5 14 0 70001 60010 16 10 0 16 0 0 1 1 00008780
  5 15 2 50014 70001 16 34 0 16 0 0 0 1 00008790
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''READ FROM FF03 -
  LCA
  ADTA
  MSBL
  TACAN AND TACAN CONTROL REGISTER
  NATURE SOURCE SINK LENGTH INTERVAL START TOTAL SE T
  5 16 0 70001 60011 16 10 0 16 0 0 1 1 00008870
  5 17 2 50016 70001 16 30 0 16 0 0 0 1 00008880
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''READ ADTA FROM FF04
  NATURE SOURCE SINK LENGTH INTERVAL START TOTAL SE T
  5 18 0 70001 60012 16 2 0 16 0 0 1 1 00008920
  5 19 2 50018 70001 16 14 0 16 0 0 0 1 00008930
''

''READ CLOCK (MTU) FROM FF01, FF02, FF03
  NATURE SOURCE SINK LENGTH INTERVAL START TOTAL SE T
  5 20 0 70001 380 16 2 0 16 1 0 1 3 00008970
  5 21 2 50020 70001 16 14 0 16 0 0 0 3 00008980
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''READ FROM FA01, FA02, FA03 -
## RATE GYRO ASSEMBLY

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## READ FROM FA04

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## READ FROM FA04, FA02 -

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## WRITE TO FF01, FF02, FF03 -

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WRITE TO DDU1, DDU2 - AVI

WRITE TO DEU1, 2, AND 3 (TASK 34)

WRITE PRIME FRAME TO PCMMU

READ KEYBD 1 AND WRITE NEW DISPLAY TO DEU1

**** DEVICES

DISPLAY ELECTRONIC UNIT NO. 1

A/D SHARED RECORD
CLASS SIZE
1 1 8192

DISPLAY ELECTRONIC UNIT NO. 2

A/D SHARED RECORD
CLASS SIZE
1 1 8192

DISPLAY ELECTRONIC UNIT NO. 3

A/D SHARED RECORD
CLASS SIZE
1 1 8192

DISPLAY ELECTRONIC UNIT NO. 4

00009520
00009530
00009540
00009550
00009560
00009570
00009580
00009590
00009600
00009610
00009620
00009630
00009640
00009650
00009660
00009670
00009680
00009690
00009700
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00009960
00009970
00009980
00009990
00010000
30 April 1976

System Development Corporation
TM-(L)-5558/000/00

A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010020
4	 1 8192 120 62 0 00010030

DISPLAY UNIT NO. 1
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010040
5	 1 8192 38 0 0 00010050

DISPLAY UNIT NO. 2
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010060
6	 1 8192 38 0 0 00010070

DISPLAY UNIT NO. 3
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010080
7	 1 8192 38 0 0 00010090

DISPLAY UNIT NO. 4
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010100
8	 1 8192 38 0 0 00010110

MULTIPLEXER/DEMULTIPLEXER (MDM) FF1
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010120
9	 1 1024 120 120 0 00010130

MULTIPLEXER/DEMULTIPLEXER (MDM) FF2
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010140
10	 1 1024 120 120 0 00010150

MULTIPLEXER/DEMULTIPLEXER (MDM) FF3
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010160
11	 1 1024 120 120 0 00010170

MULTIPLEXER/DEMULTIPLEXER (MDM) FF4
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010180
12	 1 1024 120 120 0 00010190

MULTIPLEXER/DEMULTIPLEXER (MDM) FA1
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010200
13	 1 1024 120 120 0 00010210

MULTIPLEXER/DEMULTIPLEXER (MDM) FA2
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010220
14	 1 1024 120 120 0 00010230

MULTIPLEXER/DEMULTIPLEXER (MDM) FA3
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010240
15	 1 1024 120 120 0 00010250

MULTIPLEXER/DEMULTIPLEXER (MDM) FA4
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010260
16	 1 1024 120 120 0 00010270

MULTIPLEXER/DEMULTIPLEXER (MDM) FA5
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010280
17	 1 1024 120 120 0 00010290

MULTIPLEXER/DEMULTIPLEXER (MDM) FA6
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010300
18	 1 1024 120 120 0 00010310

MULTIPLEXER/DEMULTIPLEXER (MDM) FA7
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010320
19	 1 1024 120 120 0 00010330

MULTIPLEXER/DEMULTIPLEXER (MDM) FA8
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010340
20	 1 1024 120 120 0 00010350

MULTIPLEXER/DEMULTIPLEXER (MDM) FA9
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010360
21	 1 1024 120 120 0 00010370

MULTIPLEXER/DEMULTIPLEXER (MDM) FA10
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010380
22	 1 1024 120 120 0 00010390

MULTIPLEXER/DEMULTIPLEXER (MDM) FA11
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010400
23	 1 1024 120 120 0 00010410

MULTIPLEXER/DEMULTIPLEXER (MDM) FA12
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010420
24	 1 1024 120 120 0 00010430

MULTIPLEXER/DEMULTIPLEXER (MDM) FA13
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010440
25	 1 1024 120 120 0 00010450

MULTIPLEXER/DEMULTIPLEXER (MDM) FA14
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010460
26	 1 1024 120 120 0 00010470

MULTIPLEXER/DEMULTIPLEXER (MDM) FA15
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010480
27	 1 1024 120 120 0 00010490

MULTIPLEXER/DEMULTIPLEXER (MDM) FA16
A/D SHARE RECORD TRANSMISSION RATE RESET
CLASS SIZE INPUT OUTPUT PERIOD 00010500
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" A/D SHARE RECORD TRANSMISSION RATE RESET 00011060
" CLASS SIZE INPUT OUTPUT PERIOD 00011070
6 25 1 1 1024 120 120 0 00011080
"MULTIPLEXER/DEMULTIPLEXER (MDM) OA3
" A/D SHARE RECORD TRANSMISSION RATE RESET 00011110
" CLASS SIZE INPUT OUTPUT PERIOD 00011120
6 26 1 1 1024 120 120 0 00011130
"KEYBOARD UNIT (KBU) NO. 1
" A/D SHARE RECORD TRANSMISSION RATE RESET 00011160
" CLASS SIZE INPUT OUTPUT PERIOD 00011170
6 27 1 1 0 0 1 1 00011180
"KEYBOARD UNIT (KBU) NO. 2
" A/D SHARE RECORD TRANSMISSION RATE RESET 00011210
" CLASS SIZE INPUT OUTPUT PERIOD 00011220
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"KEYBOARD UNIT (KBU) NO. 3
" A/D SHARE RECORD TRANSMISSION RATE RESET 00011260
" CLASS SIZE INPUT OUTPUT PERIOD 00011270
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" A/D SHARE RECORD TRANSMISSION RATE RESET 00011310
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" A/D SHARE RECORD TRANSMISSION RATE RESET 00011360
" CLASS SIZE INPUT OUTPUT PERIOD 00011370
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"**** MEMORY UNITS
THE GPC CORE MEMORIES ARE REPRESENTED AS MEMORY UNITS.
"MEMORY CPC 1
" SPEED FACTOR PAGES 00011410
7 1 1.4 125 00011420
"MEMORY CPC 2
" SPEED FACTOR PAGES 00011450
7 2 1.4 125 00011460
**System Development Corporation**

30 April 1976

**B-24**

**TM-(L)-5658/000/00**

```
MEMORY GPC 3
SPEED FACTOR  PAGES
7   3    1.4    125

MEMORY GPC 4
SPEED FACTOR  PAGES
7   4    1.4    125

**** STORAGE UNITS ********************************************

MASS MEMORIES ARE REPRESENTED AS STORAGE UNITS.

MASS MEMORY STORAGE (MM) NO. 1
A/D SHARE CYCLE TRX RATE CAPACITY ACCESS PERIOD
8   1   1   0  125    17000000    399    500    0    0    0

MASS MEMORY STORAGE (MM) NO. 2
A/D SHARE CYCLE TRX RATE CAPACITY ACCESS PERIOD
8   2   1   0  125    17000000    399    500    0    0    0

**** PROCESSORS ***********************************************

THE CPU OF EACH GPC IS REPRESENTED AS A PROCESSOR. HOWEVER,
ONE IS ACTUALLY EMPLOYED IN SIMULATING DPS FUNCTION EXECUTION.

CENTRAL PROCESSING UNIT (CPU) NO. 1
SPEED CLASS INTERRUPT SWITCH VIRT MACH CONNECTED MEMORIES
9   1  0.48  10    5   0   1   1

CENTRAL PROCESSING UNIT (CPU) NO. 2
SPEED CLASS INTERRUPT SWITCH VIRT MACH CONNECTED MEMORIES
9   2  0.48  10    5   0   2   2

CENTRAL PROCESSING UNIT (CPU) NO. 3
SPEED CLASS INTERRUPT SWITCH VIRT MACH CONNECTED MEMORIES
9   3  0.48  10    5   0   3   3

CENTRAL PROCESSING UNIT (CPU) NO. 4
SPEED CLASS INTERRUPT SWITCH VIRT MACH CONNECTED MEMORIES
9   4  0.48  10    5   0   4   4

**** DATA LINKS ***********************************************

EACH OF THE TRANSMISSION PATHS FOR DATA IN THE DPS IS
REPRESENTED AS A DATA LINK.
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  '" MODE TRANSMISSION RATE TIME LAG
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  '" MODE TRANSMISSION RATE TIME LAG
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A DATA SET IS DEFINED TO REPRESENT THE DISPLAY IMAGES STORED IN EACH OF THE TWO MASS MEMORIES.

```
11 1 1 0 10000 10000
11 2 1 0 10240 10240
```

THE FOLLOWING FORMS DEFINE THE INTERCONNECTIONS OF DPS COMPONENTS THROUGH DATA LINKS.

```
UNIT DATALINK CONNECTIONS
12 60001  6 28 32 33
12 60002  7 29 34 35
12 60003  8 30 33 35
12 60004  9 31 36
12 60005  28
12 60006  29
12 60007  30
12 60008  31
12 60009  10 14
12 60010  11 15
12 60011  12 16
12 60012  13 17
12 60013  14 10
12 60014  15 11
12 60015  16 12
12 60016  17 13
12 60017  10 11 12 13
12 60018  10 11 12 13
12 60019  10 11 12 13
12 60020  37 38
12 60021  37 38
12 60022  37 38
12 60023  37 38
12 60024  37 38
12 60025  37 38
12 60026  37 38
12 60027  32 33
12 60028  34 35
12 60029  36
12 60095  24 25 26 27 37
```
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END OF DATA
The values listed on the preceding pages in this appendix for NASA.SPECS20.DATA can also be used for the simulation with one Virtual Machine and the IMSIM specification forms NASA.SPECS10.DATA, with the following exceptions:

'AIE SIP   SYSTEM SOFTWARE INTERFACE PROCESSOR
'SCHEDULED AT 40MS INTERVALS BY SYSTEM INITIALIZATION
'CLASS   DELAY REQUIRED ELEMENTS
2 7 1 0 30116 30130 30138 30147 50028 50029 *
      50058 30 51 30140 1

'ICC FOR REDUNDANT SET (GPC 2, 3, AND 4 COMMUNICATION WITH GPC 1)
'NATURE SOURCE SINK LENGTH INTERVAL START TOTAL SET
5 28 0 383 70001 16 256 0 16 0 0 0 3
5 29 0 70001 384 16 256 0 16 0 0 0 3

'CENTRAL PROCESSING UNIT (CPU) NO. 1
'\SPEED CLASS INTERRUPT SWITCH VIRT MACH CONNECTED MEMORIES
9 1 0.48 10 5 0 1 1 2 3 4

'CENTRAL PROCESSING UNIT (CPU) NO. 2
'SPEED CLASS INTERRUPT SWITCH VIRT MACH CONNECTED MEMORIES
2 0.48 10 5 0 1 2 1 3 4

'CENTRAL PROCESSING UNIT (CPU) NO. 3
'SPEED CLASS INTERRUPT SWITCH VIRT MACH CONNECTED MEMORIES
3 0.48 10 5 0 1 3 1 2 4

'CENTRAL PROCESSING UNIT (CPU) NO. 4
'SPEED CLASS INTERRUPT SWITCH VIRT MACH CONNECTED MEMORIES
4 0.48 10 5 0 1 4 1 2 3
APPENDIX C

HISTORY PRINTOUT

This appendix provides the History Printout of a simulation run with jobschedule JSCA07.

The abbreviations used in this appendix, in order of appearance, are as follows:

TUS    - Time Units
TS     - Task Starts
TI     - Task Index (internal IMSIM index)
T X    - Task in Execution
MS     - Message Starts
M E    - Message Ends
T W    - Task in Wait state
T E    - Task Ends

This printout gives the full history of the run by providing pertinent information at every time that an activity in the model takes place. This history specifies, at the time indicated, one or more of the following types of summaries:

a. The start and finish of jobs.

b. The start, execution, wait, and completion times of tasks, and the appropriate job number for which this task is called.

c. For messages, the task and job number as well as the message length, transmission rate, transmission path consisting of the origin (source), bus or datalink used for transmission, and the destination (sink).

At time 1, the Executive Functions are initialized, while at time 31095, the 20 functions (tasks) for job 2 are initiated. All functions are activated at time 32000, after which the printout provides the history of all events.
1 TUS START AT 0 SEC. JOB 1
1 TUS TS START TASK 1 JOB 1 TI=701
1 TUS TS START TASK 2 JOB 1 TI=702
1 TUS TS START TASK 3 JOB 1 TI=703
1 TUS TS START TASK 4 JOB 1 TI=704
1 TUS TS START TASK 5 JOB 1 TI=705
31095 TUS START AT 31.09SEC. JOB 2
31095 TUS TS START TASK 6 JOB 2 TI=706
31095 TUS TS START TASK 7 JOB 2 TI=707
31095 TUS TS START TASK 8 JOB 2 TI=708
31095 TUS TS START TASK 9 JOB 2 TI=709
31095 TUS TS START TASK 10 JOB 2 TI=710
31095 TUS TS START TASK 11 JOB 2 TI=711
31095 TUS TS START TASK 12 JOB 2 TI=712
31095 TUS TS START TASK 13 JOB 2 TI=713
31095 TUS TS START TASK 14 JOB 2 TI=714
31095 TUS TS START TASK 15 JOB 2 TI=715
31095 TUS TS START TASK 19 JOB 2 TI=716
31095 TUS TS START TASK 20 JOB 2 TI=717
31095 TUS TS START TASK 21 JOB 2 TI=718
31095 TUS TS START TASK 22 JOB 2 TI=719
31095 TUS TS START TASK 23 JOB 2 TI=720
31095 TUS TS START TASK 24 JOB 2 TI=721
31095 TUS TS START TASK 32 JOB 2 TI=722
31095 TUS TS START TASK 34 JOB 2 TI=723
31095 TUS TS START TASK 35 JOB 2 TI=724
31095 TUS TS START TASK 37 JOB 2 TI=725
32001 TUS TX EXECUTING TASK 7 JOB 2 TI=707
32001 TUS NS START 28 TASK 7 JOB 2 TI=707 LENGTH RATE
PATH 70004 1 70001 256 120
32001 TUS NS START 29 TASK 7 JOB 2 TI=707 LENGTH RATE
PATH 70001 1 70004 256 120
32001 TUS NS START 58 TASK 7 JOB 2 TI=707 LENGTH RATE
PATH 70001 2 60095 512 120
32003 TUS ME END 28 TASK 7 JOB 2 TI=707
32003 TUS ME END 29 TASK 7 JOB 2 TI=707
32003 TUS TX MSG WAIT TASK 7 JOB 2 TI=707
32003 TUS NS START 50 TASK 6 JOB 2 TI=706 LENGTH RATE
PATH 70001 12 60011 52 120
32003 TUS ME END 50 TASK 6 JOB 2 TI=706
32003 TUS NS START 51 TASK 6 JOB 2 TI=706 LENGTH RATE
PATH 70001 13 60012 48 120
32003 TUS ME END 51 TASK 6 JOB 2 TI=706
32003 TUS NS START 52 TASK 6 JOB 2 TI=706 LENGTH RATE
PATH 70001 12 60011 4 120
32003 TUS ME END 52 TASK 6 JOB 2 TI=706
32003 TUS NS START 53 TASK 6 JOB 2 TI=706 LENGTH RATE
PATH 70001 13 60016 36 120
32003 TUS ME END 53 TASK 6 JOB 2 TI=706
32003 TUS NS START 54 TASK 6 JOB 2 TI=706 LENGTH RATE
PATH 70001 10 60018 72 120
32003 TUS ME END 54 TASK 6 JOB 2 TI=706
32003 TUS NS START 5 TASK 6 JOB 2 TI=706 LENGTH RATE
PATH 70001 12 60011 12 120
32003 TUS ME END 6 TASK 6 JOB 2 TI=706
32003 TUS NS START 8 TASK 6 JOB 2 TI=706 LENGTH RATE
PATH 70001 13 60012 2 120
32003 TUS ME END 8 TASK 6 JOB 2 TI=706
32005 TUS T I INTERRUPT TASK 6 JOB 2 TI=706
32005 TUS T X EXECUTING TASK 7 JOB 2 TI=707
32005 TUS MS START 28 TASK PATH 70003 1 70001 256 120
32005 TUS MS START 29 TASK PATH 70003 2 70003 256 120
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7  
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INTERCEPT TASK  
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MSG WAIT TASK  
7 JOB  
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END 54 TASK  
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30 April 1976

System Development Corporation

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PATH 70004 1 70001 256 120
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32161 TUS TX EXECUTING TASK 7 JOB 2 TI=707
32161 TUS MS START 58 TASK 7 JOB 2 TI=707 LENGTH RATE
PATH 70001 24 60095 512 120
32161 TUS MS START 28 TASK 7 JOB 2 TI=707 LENGTH RATE
PATH 70004 1 70001 256 120
32161 TUS MS START 29 TASK 7 JOB 2 TI=707 LENGTH RATE
PATH 70004 2 70004 256 120
32163 TUS ME END 28 TASK 7 JOB 2 TI=707
32163 TUS NE END 29 TASK 7 JOB 2 TI=707
32163 TUS TW MSG WAIT TASK 7 JOB 2 TI=707
32163 TUS TX EXECUTING TASK 6 JOB 2 TI=706
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PATH 70001 13 60012 48 120
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32163 TUS MS START 54 TASK 6 JOB 2 TI=706 LENGTH RATE
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32163 TUS MS START 53 TASK 6 JOB 2 TI=706 LENGTH RATE
PATH 70001 13 60016 36 120
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PATH 60012 13 70001 24 120
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32163 TUS MS START 13 TASK 6 JOB 2 TI=706 LENGTH RATE
PATH 60009 10 70001 32 120
32163 TUS M E END 13 TASK 6 JOB 2 TI=706
32163 TUS MS START 15 TASK 6 JOB 2 TI=706 LENGTH RATE
PATH 60014 13 70001 26 120
32163 TUS MS END 15 TASK 6 JOB 2 TI=706
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PATH 60011 12 70001 14 120
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32163 TUS M E END 23 TASK 6 JOB 2 TI=706
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32163 TUS MS INTERRUPT TASK 6 JOB 2 TI=706
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PATH 70001 2 70003 256 120
32165 TUS M E END 28 TASK 7 JOB 2 TI=707
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32169 TUS T X EXECUTING TASK 6 JOB 2 TI=706
32169 TUS MS END 59 TASK 34 JOB 2 TI=723
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**System Development Corporation**

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32175 TUS T X
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32186 TUS T E
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PATH 60011 12 70001 14 120
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PATH 60015 12 70001 18 120
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PATH 70003 1 70001 256 120
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PATH 70001 2 70003 256 120
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32304 TUS MS
START 57 TASK
PATH 70001
35 JOB 2 TI=724 LENGTH RATE

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32306 TUS T I
INTERCEPT TASK
35 JOB 2 TI=724

32306 TUS T X
EXECUTING TASK
11 JOB 2 TI=711

32316 TUS T X
EXECUTING TASK
35 JOB 2 TI=724

32312 TUS M E
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35 JOB 2 TI=724

32312 TUS M E
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32312 TUS M E
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32312 TUS M E
END. 55 TASK
35 JOB 2 TI=724

32312 TUS M E
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32312 TUS M E
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32321 TUS M S
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START 29 TASK
PATH 70001
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PATH 70001
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APPENDIX D

SUMMARY OUTPUT REPORTS

This appendix provides the statistical and control reports as specified in paragraph 5.2.6.1.

Statistical summaries for four different runs are given, viz.,

1. for a 500 ms concentrated simulation run with specification NASA.SPECS10.DATA and jobschedule JSCA06. These printouts appear on pages D-2 through D-5.

2. for a 1.24-second flight-segmented simulation run with specification NASA.SPECS10.DATA and jobschedule JSCA07. These printouts appear on pages D-6 through D-9.

3. for a 1.10-second concentrated simulation run with specification NASA.SPECS10.DATA and jobschedule JSCA06. These printouts appear on pages D-10 through D-13.

4. for a 50 ms concentrated simulation run with specification NASA.SPECS20.DATA with four Virtual Machines and jobschedule JSCA08. These printouts appear on pages D-14 through D-17.
DURING 0.50 SECONDS OF SIMULATED SHUTTLE OPERATIONS
A TOTAL OF 20 DIFFERENT FUNCTIONS WERE INTRODUCED.
THESE FUNCTIONS WERE ACTIVATED 99 TIMES, STATUS IS:
95 WERE COMPLETED
16 ARE WAITING FOR NEXT ACTIVATION
3 ARE IN READY STATE, I.E. WAITING FOR CPU
0 ARE WAITING FOR MESSAGES TO COMPLETE
1 PRESENTLY EXECUTING, I.E. IN ACTIVE STATE
FUNCTIONS WERE INTERRUPTED 33 TIMES.
0 FUNCTION ACTIVATIONS WERE ABORTED AS FUNCTION STILL ACTIVE.

A TOTAL OF 822 MESSAGES WERE SUCCESSFULLY TRANSMITTED.
0 WERE IN BURST MODE OVER MULTIPLEXED DATA LINKS
0 TRANSMISSIONS WERE FOR LOADING OF MEMORIES
0 TRANSMISSIONS WERE INTERRUPTED BECAUSE OF BURST MODE
OPERATIONS OR KILLING OF TASKS
0 SOURCE-DRIVEN MESSAGES WERE LOST DUE TO BACKLOGGING.

DEVICE 1, CLASS 1, WAS INVOLVED IN 5 TRANSMISSIONS,
AVERAGING 8 MS. UTILIZATION WAS 7 PERCENT.

DEVICE 2, CLASS 1, WAS INVOLVED IN 5 TRANSMISSIONS,
AVERAGING 8 MS. UTILIZATION WAS 7 PERCENT.

DEVICE 3, CLASS 1, WAS INVOLVED IN 5 TRANSMISSIONS,
AVERAGING 8 MS. UTILIZATION WAS 7 PERCENT.

DEVICE 9, CLASS 1, WAS INVOLVED IN 5 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.

DEVICE 10, CLASS 1, WAS INVOLVED IN 5 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.

DEVICE 11, CLASS 1, WAS INVOLVED IN 5 TRANSMISSIONS,
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DEVICE 26, CLASS 1, WAS INVOLVED IN 5 TRANSMISSIONS,
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DEVICE 27, CLASS 1, WAS INVOLVED IN 5 TRANSMISSIONS,
AVERAGING 11 MS. UTILIZATION WAS 15 PERCENT.

DEVICE 28, CLASS 1, WAS INVOLVED IN 5 TRANSMISSIONS,
AVERAGING 2.79 MS. UTILIZATION WAS 18 PERCENT.

MEMORY 1, SIZE 125 PAGES, HELD AN AVERAGE OF 3 PAGES,
WITH A MAXIMUM OF 3 PAGES. THE POTENTIAL TRANSMISSION RATE
IS 1399 CH/MS. THE MAXIMUM ACHIEVED RATE WAS 720
CH/MS, AND THE AVERAGE RATE WAS 1.36 CH/MS.

MEMORY 2, SIZE 125 PAGES, HELD AN AVERAGE OF 0 PAGES,
WITH A MAXIMUM OF 0 PAGES. THE POTENTIAL TRANSMISSION RATE
IS 1399 CH/MS. THE MAXIMUM ACHIEVED RATE WAS 240
CH/MS, AND THE AVERAGE RATE WAS 0.15 CH/MS.

MEMORY 3, SIZE 125 PAGES, HELD AN AVERAGE OF 0 PAGES,
WITH A MAXIMUM OF 0 PAGES. THE POTENTIAL TRANSMISSION RATE
IS 1399 CH/MS. THE MAXIMUM ACHIEVED RATE WAS 240
CH/MS, AND THE AVERAGE RATE WAS 0.19CH/MS.
MEMORY 4, SIZE 125 PAGES, HELD AN AVERAGE OF 0 PAGES.
WITH A MAXIMUM OF 0 PAGES. THE POTENTIAL TRANSMISSION RATE
IS 1399 CH/MS. THE MAXIMUM ACHIEVED RATE WAS 240
CH/MS, AND THE AVERAGE RATE WAS 0.19CH/MS.

PROCESSOR 1, V.M. 1, WAS USED 175 TIMES FOR
A TOTAL OF 388 MS. UTILIZATION WAS 77 PERCENT.

DATA LINK 1 WAS INVOLVED IN 39 TRANSMISSIONS, AVERAGING
2 MS. UTILIZATION WAS 15 PERCENT.
POTENTIAL TRANSMISSION RATE IS 120 CH/MS.
DATA LINK 2 WAS INVOLVED IN 39 TRANSMISSIONS, AVERAGING
2 MS. UTILIZATION WAS 15 PERCENT.
POTENTIAL TRANSMISSION RATE IS 120 CH/MS.
DATA LINK 6 WAS INVOLVED IN 5 TRANSMISSIONS, AVERAGING
8 MS. UTILIZATION WAS 7 PERCENT.
POTENTIAL TRANSMISSION RATE IS 120 CH/MS.
DATA LINK 7 WAS INVOLVED IN 5 TRANSMISSIONS, AVERAGING
8 MS. UTILIZATION WAS 7 PERCENT.
POTENTIAL TRANSMISSION RATE IS 120 CH/MS.
DATA LINK 8 WAS INVOLVED IN 5 TRANSMISSIONS, AVERAGING
8 MS. UTILIZATION WAS 7 PERCENT.
POTENTIAL TRANSMISSION RATE IS 120 CH/MS.
DATA LINK 10 WAS INVOLVED IN 221 TRANSMISSIONS, AVERAGING
0 MS. UTILIZATION WAS 0 PERCENT.
POTENTIAL TRANSMISSION RATE IS 120 CH/MS.
DATA LINK 11 WAS INVOLVED IN 195 TRANSMISSIONS, AVERAGING
0 MS. UTILIZATION WAS 0 PERCENT.
POTENTIAL TRANSMISSION RATE IS 120 CH/MS.
DATA LINK 12 WAS INVOLVED IN 169 TRANSMISSIONS, AVERAGING
0 MS. UTILIZATION WAS 0 PERCENT.
POTENTIAL TRANSMISSION RATE IS 120 CH/MS.
DATA LINK 13 WAS INVOLVED IN 104 TRANSMISSIONS, AVERAGING
0 MS. UTILIZATION WAS 0 PERCENT.
POTENTIAL TRANSMISSION RATE IS 120 CH/MS.
DATA LINK 24 WAS INVOLVED IN 33 TRANSMISSIONS, AVERAGING
2.79MS. UTILIZATION WAS 18 PERCENT.
POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA SET 1, ON STORAGE UNIT 1, AVERAGED 10000 CH, AND REACHED
A MAXIMUM OF 10000 CH.
DATA SET 2, ON STORAGE UNIT 1, AVERAGED 10240 CH, AND REACHED
A MAXIMUM OF 10240 CH.

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SUMMARY FOR TIME 32501, RELATIVE TIME 32501

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**Current Transaction Count**: 146
**Maximum Number of Transactions**: 223
**Number of Try Operations**: 132809
**Number of Transaction Moves**: 394561
**Number of Variable Evaluations**: 612316
**Maximum Variable Recursion**: 5
**Number of Admit Attempts**: 907770
**Number of Function Points**: 1144
**Most Recent Block ID**: 3032
**Number of Block Spaces Used**: 1917
**Number of Report Lines**: 91
**Number of Variable Elements**: 1126
**Current Utilization of Stacks**: 846
DURING 1.24 SECONDS OF SIMULATED SHUTTLE OPERATIONS
A TOTAL OF 20 DIFFERENT FUNCTIONS WERE INTRODUCED.
THESE FUNCTIONS WERE ACTIVATED 196 TIMES, STATUS IS:
193 WERE COMPLETED
17 ARE WAITING FOR NEXT ACTIVATION
1 ARE IN READY STATE, I.E. WAITING FOR CPU
1 ARE WAITING FOR MESSAGES TO COMPLETE
1 PRESENTLY EXECUTING, I.E. IN ACTIVE STATE
FUNCTIONS WERE INTERRUPTED 63 TIMES.
0 FUNCTION ACTIVATIONS WERE ABORTED AS FUNCTION STILL ACTIVE.

A TOTAL OF 2001 MESSAGES WERE SUCCESSFULLY TRANSMITTED.
0 WERE IN BURST MODE OVER MULTIPLEXED DATA LINKS
0 TRANSMISSIONS WERE FOR LOADING OF MEMORIES
0 TRANSMISSIONS WERE INTERRUPTED BECAUSE OF BURST MODE
OPERATIONS OR KILLING OF TASKS
0 SOURCE-DRIVEN MESSAGES WERE LOST DUE TO BACKLOGGING.

DEVICE 1, CLASS 1, WAS INVOLVED IN 13 TRANSMISSIONS,
AVERAGING 8 MS. UTILIZATION WAS 8 PERCENT.
DEVICE 2, CLASS 1, WAS INVOLVED IN 13 TRANSMISSIONS,
AVERAGING 8 MS. UTILIZATION WAS 8 PERCENT.
DEVICE 3, CLASS 1, WAS INVOLVED IN 13 TRANSMISSIONS,
AVERAGING 8 MS. UTILIZATION WAS 8 PERCENT.
DEVICE 9, CLASS 1, WAS INVOLVED IN 314 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.
DEVICE 10, CLASS 1, WAS INVOLVED IN 319 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.
DEVICE 11, CLASS 1, WAS INVOLVED IN 320 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.
DEVICE 12, CLASS 1, WAS INVOLVED IN 160 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.
DEVICE 13, CLASS 1, WAS INVOLVED IN 157 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.
DEVICE 14, CLASS 1, WAS INVOLVED IN 159 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.
DEVICE 15, CLASS 1, WAS INVOLVED IN 96 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.
DEVICE 16, CLASS 1, WAS INVOLVED IN 96 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.
DEVICE 17, CLASS 1, WAS INVOLVED IN 32 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.
DEVICE 18, CLASS 1, WAS INVOLVED IN 32 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.
DEVICE 19, CLASS 1, WAS INVOLVED IN 8 TRANSMISSIONS,
AVERAGING 7 MS. UTILIZATION WAS 7 PERCENT.
DEVICE 27, CLASS 1, WAS INVOLVED IN 8 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.
DEVICE 25, CLASS 1, WAS INVOLVED IN 82 TRANSMISSIONS,
AVERAGING 2.74:15. UTILIZATION WAS 18 PERCENT.

MEMORY 1, SIZE 125 PAGES, HELD AN AVERAGE OF 3 PAGES,
WITH A MAXIMUM OF 3 PAGES. THE POTENTIAL TRANSMISSION RATE
IS 1400 CH/MS. THE MAXIMUM ACHIEVED RATE WAS 720
CH/MS, AND THE AVERAGE RATE WAS 3.31CH/MS.
MEMORY 2, SIZE 125 PAGES, HELD AN AVERAGE OF 0 PAGES,
WITH A MAXIMUM OF 0 PAGES. THE POTENTIAL TRANSMISSION RATE
IS 1400 CH/MS. THE MAXIMUM ACHIEVED RATE WAS 240
CH/MS, AND THE AVERAGE RATE WAS 0.45CH/MS.
MEMORY 3, SIZE 125 PAGES, HELD AN AVERAGE OF 0 PAGES, WITH A MAXIMUM OF 0 PAGES. THE POTENTIAL TRANSMISSION RATE IS 1400 CH/MS. THE MAXIMUM ACHIEVED RATE WAS 240 CH/MS, AND THE AVERAGE RATE WAS 0.45 CH/MS.

MEMORY 4, SIZE 125 PAGES, HELD AN AVERAGE OF 0 PAGES, WITH A MAXIMUM OF 0 PAGES. THE POTENTIAL TRANSMISSION RATE IS 1400 CH/MS. THE MAXIMUM ACHIEVED RATE WAS 240 CH/MS, AND THE AVERAGE RATE WAS 0.46 CH/MS.

PROCESSOR 1, V.M. 1, WAS USED 337 TIMES FOR A TOTAL OF 879 MS. UTILIZATION WAS 70 PERCENT.

DATA LINK 1 WAS INVOLVED IN 94 TRANSMISSIONS, AVERAGING 2 MS. UTILIZATION WAS 15 PERCENT. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 2 WAS INVOLVED IN 94 TRANSMISSIONS, AVERAGING 2 MS. UTILIZATION WAS 15 PERCENT. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 6 WAS INVOLVED IN 13 TRANSMISSIONS, AVERAGING 8 MS. UTILIZATION WAS 8 PERCENT. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 7 WAS INVOLVED IN 13 TRANSMISSIONS, AVERAGING 8 MS. UTILIZATION WAS 8 PERCENT. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 8 WAS INVOLVED IN 13 TRANSMISSIONS, AVERAGING 8 MS. UTILIZATION WAS 8 PERCENT. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 10 WAS INVOLVED IN 535 TRANSMISSIONS, AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 11 WAS INVOLVED IN 478 TRANSMISSIONS, AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 12 WAS INVOLVED IN 416 TRANSMISSIONS, AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 13 WAS INVOLVED IN 256 TRANSMISSIONS, AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 24 WAS INVOLVED IN 62 TRANSMISSIONS, AVERAGING 2.77 MS. UTILIZATION WAS 18 PERCENT. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA SET 1, ON STORAGE UNIT A, AVERAGED 10000 CH, AND REACHED A MAXIMUM OF 10000 CH.

DATA SET 2, ON STORAGE UNIT A, AVERAGED 10240 CH, AND REACHED A MAXIMUM OF 10240 CH.
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### CURRENT TRANSACTION COUNT

- **148**

### MAXIMUM NUMBER OF TRANSACTIONS

- **223**

### NUMBER OF TRY OPERATIONS

- **255171**

### NUMBER OF TRANSACTION MOVES

- **797804**

### NUMBER OF VARIABLE EVALUATIONS

- **1163262**

### MAXIMUM VARIABLE RECURSION

- **5**

### NUMBER OF ADMIT ATTEMPTS

- **1668396**

### NUMBER OF FUNCTION POINTS

- **1144**

### MOST RECENT BLOCK ID

- **8021**

### NUMBER OF BLOCK SPACES USED

- **1917**

### NUMBER OF REPORT LINES

- **92**

### NUMBER OF VARIABLE ELEMENTS

- **1126**

### CURRENT UTILIZATION OF STACKS

- **1290**
DURING 1.10 SECONDS OF SIMULATED SHUTTLE OPERATIONS
A TOTAL OF 20 DIFFERENT FUNCTIONS WERE INTRODUCED.
THOSE FUNCTIONS WERE ACTIVATED 184 TIMES, STATUS IS:
182 WERE COMPLETED
18 ARE WAITING FOR NEXT ACTIVATION
1 ARE IN READY STATE, I.E. WAITING FOR CPU
0 ARE WAITING FOR MESSAGES TO COMPLETE
1 PRESENTLY EXECUTING, I.E. IN ACTIVE STATE
FUNCTIONS WERE INTERRUPTED 60 TIMES.
1 FUNCTION ACTIVATIONS WERE ABORTED AS FUNCTION STILL ACTIVE.

A TOTAL OF 1448 MESSAGES WERE SUCCESSFULLY TRANSMITTED.
0 WERE IN BURST MODE OVER MULTIPLEXED DATA LINKS
0 TRANSMISSIONS WERE FOR LOADING OF MEMORIES
0 TRANSMISSIONS WERE INTERRUPTED BECAUSE OF BURST MODE
OPERATIONS OR KILLING OF TASKS
0 SOURCE-DRIVEN MESSAGES WERE LOST DUE TO BACKLOGGING.

DEVICE 1, CLASS 1, WAS INVOLVED IN 11 TRANSMISSIONS,
AVERAGING 8 MS. UTILIZATION WAS 7 PERCENT.
DEVICE 2, CLASS 1, WAS INVOLVED IN 11 TRANSMISSIONS,
AVERAGING 8 MS. UTILIZATION WAS 7 PERCENT.
DEVICE 3, CLASS 1, WAS INVOLVED IN 11 TRANSMISSIONS,
AVERAGING 8 MS. UTILIZATION WAS 7 PERCENT.
DEVICE 9, CLASS 1, WAS INVOLVED IN 220 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.
DEVICE 10, CLASS 1, WAS INVOLVED IN 220 TRANSMISSIONS,
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DEVICE 11, CLASS 1, WAS INVOLVED IN 220 TRANSMISSIONS,
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DEVICE 12, CLASS 1, WAS INVOLVED IN 110 TRANSMISSIONS,
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DEVICE 15, CLASS 1, WAS INVOLVED IN 66 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.
DEVICE 16, CLASS 1, WAS INVOLVED IN 66 TRANSMISSIONS,
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DEVICE 17, CLASS 1, WAS INVOLVED IN 22 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.
DEVICE 18, CLASS 1, WAS INVOLVED IN 22 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.
DEVICE 27, CLASS 1, WAS INVOLVED IN 9 TRANSMISSIONS,
AVERAGING 11 MS. UTILIZATION WAS 8 PERCENT.
DEVICE 95, CLASS 1, WAS INVOLVED IN 72 TRANSMISSIONS,
AVERAGING 2.78 MS. UTILIZATION WAS 18 PERCENT.

MEMORY 1, SIZE 125 PAGES, HELD AN AVERAGE OF 3 PAGES,
WITH A MAXIMUM OF 3 PAGES. THE POTENTIAL TRANSMISSION RATE IS 1400 CH/MS. THE MAXIMUM ACHIEVED RATE WAS 720 CH/MS, AND THE AVERAGE RATE WAS 1.31CH/MS.
MEMORY 2, SIZE 125 PAGES, HELD AN AVERAGE OF 0 PAGES,
WITH A MAXIMUM OF 0 PAGES. THE POTENTIAL TRANSMISSION RATE IS 1400 CH/MS. THE MAXIMUM ACHIEVED RATE WAS 240 CH/MS, AND THE AVERAGE RATE WAS 0.18CH/MS.
MEMORY 3, SIZE 125 PAGES, HELD AN AVERAGE OF 0 PAGES, WITH A MAXIMUM OF 0 PAGES. THE POTENTIAL TRANSMISSION RATE IS 1400 CH/MS. THE MAXIMUM ACHIEVED RATE WAS 240 CH/MS, AND THE AVERAGE RATE WAS 0.18 CH/MS.

MEMORY 4, SIZE 125 PAGES, HELD AN AVERAGE OF 0 PAGES, WITH A MAXIMUM OF 0 PAGES. THE POTENTIAL TRANSMISSION RATE IS 1400 CH/MS. THE MAXIMUM ACHIEVED RATE WAS 240 CH/MS, AND THE AVERAGE RATE WAS 0.18 CH/MS.

PROCESSOR 1, V.M. 1, WAS USED 318 TIMES FOR A TOTAL OF 741 MS. UTILIZATION WAS 67 PERCENT.

DATA LINK 1 WAS INVOLVED IN 84 TRANSMISSIONS, AVERAGING 2 MS. UTILIZATION WAS 15 PERCENT.

DATA LINK 2 WAS INVOLVED IN 84 TRANSMISSIONS, AVERAGING 2 MS. UTILIZATION WAS 15 PERCENT.

DATA LINK 6 WAS INVOLVED IN 11 TRANSMISSIONS, AVERAGING 8 MS. UTILIZATION WAS 7 PERCENT.

DATA LINK 7 WAS INVOLVED IN 11 TRANSMISSIONS, AVERAGING 8 MS. UTILIZATION WAS 7 PERCENT.

DATA LINK 8 WAS INVOLVED IN 11 TRANSMISSIONS, AVERAGING 8 MS. UTILIZATION WAS 7 PERCENT.

DATA LINK 10 WAS INVOLVED IN 374 TRANSMISSIONS, AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.

DATA LINK 11 WAS INVOLVED IN 330 TRANSMISSIONS, AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.

DATA LINK 12 WAS INVOLVED IN 286 TRANSMISSIONS, AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.

DATA LINK 13 WAS INVOLVED IN 176 TRANSMISSIONS, AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.

DATA LINK 24 WAS INVOLVED IN 72 TRANSMISSIONS, AVERAGING 2.7 MS. UTILIZATION WAS 18 PERCENT.

DATA SET 1, ON STORAGE UNIT 1, AVERAGED 10000 CH, AND REACHED A MAXIMUM OF 10000 CH.

DATA SET 2, ON STORAGE UNIT 1, AVERAGED 10240 CH, AND REACHED A MAXIMUM OF 10240 CH.
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**CURRENT TRANSACTION COUNT** 146  
**MAXIMUM NUMBER OF TRANSACTIONS** 223  
**NUMBER OF TRY OPERATIONS** 197939  
**NUMBER OF TRANSACTION MOVES** 615598  
**NUMBER OF VARIABLE EVALUATIONS** 893254  
**MAXIMUM VARIABLE RECURSION** 5  
**NUMBER OF ADMIT ATTEMPTS** 1273129  
**NUMBER OF FUNCTION POINTS** 1144  
**MOST RECENT BLOCK ID** 3032  
**NUMBER OF BLOCK SPACES USED** 1917  
**NUMBER OF REPORT LINES** 92  
**NUMBER OF VARIABLE ELEMENTS** 1126  
**CURRENT UTILIZATION OF STACKS** 1242
DURING 0.05 SECONDS OF SIMULATED SHUTTLE OPERATIONS
A TOTAL OF 80 DIFFERENT FUNCTIONS WERE INTRODUCED.
THese functions were activated 68 TIMES, STATUS IS:
52 WERE COMPLETED
12 ARE IN READY STATE, I.E. WAITING FOR CPU
6 ARE WAITING FOR MESSAGES TO COMPLETE
4 PRESENTLY EXECUTING, I.E. IN ACTIVE STATE
FUNCTIONS WERE INTERRUPTED 11 TIMES.
13 FUNCTION ACTIVATIONS WERE ABORTED AS FUNCTION STILL ACTIVE.

A TOTAL OF 121 MESSAGES WERE SUCCESSFULLY TRANSMITTED.
9 WERE IN BURST MODE OVER MULTIPLEXED DATA LINKS
0 TRANSMISSIONS WERE FOR LOADING OF MEMORIES
0 TRANSMISSIONS WERE INTERRUPTED BECAUSE OF BURST MODE
OPERATIONS OR KILLING OF TASKS
0 SOURCE-DRIVEN MESSAGES WERE LOST DUE TO BACKLOGGING.

DEVICE 1, CLASS 1, WAS INVOLVED IN 1 TRANSMISSIONS,
AVERAGING 8 MS. UTILIZATION WAS 15 PERCENT.
DEVICE 2, CLASS 1, WAS INVOLVED IN 1 TRANSMISSIONS,
AVERAGING 8 MS. UTILIZATION WAS 15 PERCENT.
DEVICE 3, CLASS 1, WAS INVOLVED IN 1 TRANSMISSIONS,
AVERAGING 8 MS. UTILIZATION WAS 15 PERCENT.
DEVICE 9, CLASS 1, WAS INVOLVED IN 20 TRANSMISSIONS,
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DEVICE 12, CLASS 1, WAS INVOLVED IN 10 TRANSMISSIONS,
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DEVICE 13, CLASS 1, WAS INVOLVED IN 10 TRANSMISSIONS,
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DEVICE 14, CLASS 1, WAS INVOLVED IN 10 TRANSMISSIONS,
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DEVICE 15, CLASS 1, WAS INVOLVED IN 6 TRANSMISSIONS,
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DEVICE 16, CLASS 1, WAS INVOLVED IN 6 TRANSMISSIONS,
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DEVICE 17, CLASS 1, WAS INVOLVED IN 2 TRANSMISSIONS,
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DEVICE 18, CLASS 1, WAS INVOLVED IN 2 TRANSMISSIONS,
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DEVICE 27, CLASS 1, WAS INVOLVED IN 1 TRANSMISSIONS,
AVERAGING 0 MS. UTILIZATION WAS 0 PERCENT.
DEVICE 95, CLASS 1, WAS INVOLVED IN 4 TRANSMISSIONS,
AVERAGING 3 MS. UTILIZATION WAS 23 PERCENT.

MEMORY 1, SIZE 125 PAGES, HELD AN AVERAGE OF 3 PAGES,
with a maximum of 3 PAGES. the potential transmission rate
is 1399 CH/MS. the maximum achieved rate was 360
CH/MS, and the average rate was 0.07CH/MS.
MEMORY 2, SIZE 125 PAGES, HELD AN AVERAGE OF 3 PAGES,
with a maximum of 3 PAGES. the potential transmission rate
is 1329 CH/MS. the maximum achieved rate was 240
CH/MS, and the average rate was 0.01CH/MS.
MEMORY 3, SIZE 125 PAGES, HELD AN AVERAGE OF 3 PAGES, WITH A MAXIMUM OF 3 PAGES. THE POTENTIAL TRANSMISSION RATE IS 1399 CH/MS. THE MAXIMUM ACHIEVED RATE WAS 240 CH/MS, AND THE AVERAGE RATE WAS 0.01 CH/MS.

MEMORY 4, SIZE 125 PAGES, HELD AN AVERAGE OF 3 PAGES, WITH A MAXIMUM OF 3 PAGES. THE POTENTIAL TRANSMISSION RATE IS 1399 CH/MS. THE MAXIMUM ACHIEVED RATE WAS 240 CH/MS, AND THE AVERAGE RATE WAS 0.01 CH/MS.

PROCESSOR 1, V.M. 1, WAS USED 22 TIMES FOR A TOTAL OF 49 MS. UTILIZATION WAS 97 PERCENT.

PROCESSOR 2, V.M. 2, WAS USED 16 TIMES FOR A TOTAL OF 49 MS. UTILIZATION WAS 97 PERCENT.

PROCESSOR 3, V.M. 3, WAS USED 16 TIMES FOR A TOTAL OF 49 MS. UTILIZATION WAS 97 PERCENT.

PROCESSOR 4, V.M. 4, WAS USED 16 TIMES FOR A TOTAL OF 49 MS. UTILIZATION WAS 97 PERCENT.

DATA LINK 1 WAS INVOLVED IN 2 TRANSMISSIONS, AVERAGING 120 CH/MS. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 2 WAS INVOLVED IN 2 TRANSMISSIONS, AVERAGING 120 CH/MS. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 3 WAS INVOLVED IN 2 TRANSMISSIONS, AVERAGING 120 CH/MS. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 4 WAS INVOLVED IN 2 TRANSMISSIONS, AVERAGING 120 CH/MS. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 5 WAS INVOLVED IN 1 TRANSMISSIONS, AVERAGING 120 CH/MS. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 6 WAS INVOLVED IN 1 TRANSMISSIONS, AVERAGING 120 CH/MS. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 7 WAS INVOLVED IN 1 TRANSMISSIONS, AVERAGING 120 CH/MS. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 8 WAS INVOLVED IN 1 TRANSMISSIONS, AVERAGING 120 CH/MS. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 9 WAS INVOLVED IN 1 TRANSMISSIONS, AVERAGING 120 CH/MS. POTENTIAL TRANSMISSION RATE IS 120 CH/MS.

DATA LINK 10 WAS INVOLVED IN 34 TRANSMISSIONS, AVERAGING 0 PERCENT. POTENTIAL TRANSMISSION RATE IS 0 CH/MS.

DATA LINK 11 WAS INVOLVED IN 30 TRANSMISSIONS, AVERAGING 0 PERCENT. POTENTIAL TRANSMISSION RATE IS 0 CH/MS.

DATA LINK 12 WAS INVOLVED IN 26 TRANSMISSIONS, AVERAGING 0 PERCENT. POTENTIAL TRANSMISSION RATE IS 0 CH/MS.

DATA LINK 13 WAS INVOLVED IN 16 TRANSMISSIONS, AVERAGING 0 PERCENT. POTENTIAL TRANSMISSION RATE IS 0 CH/MS.

DATA LINK 14 WAS INVOLVED IN 4 TRANSMISSIONS, AVERAGING 0 PERCENT. POTENTIAL TRANSMISSION RATE IS 0 CH/MS.

DATA LINK 15 WAS INVOLVED IN 3 TRANSMISSIONS, AVERAGING 0 PERCENT. POTENTIAL TRANSMISSION RATE IS 0 CH/MS.

DATA SET 1, ON STORAGE UNIT 1, AVERAGED 10000 CH, AND REACHED A MAXIMUM OF 10000 CH.

DATA SET 2, ON STORAGE UNIT 1, AVERAGED 10240 CH, AND REACHED A MAXIMUM OF 10240 CH.
### System Development Corporation

**30 April 1976**

**D-16**

**TM-(L)-5658/000/00**

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**MAXIMUM NUMBER OF TRANSACTIONS**: 768

**NUMBER OF TRY OPERATIONS**: 69662

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**NUMBER OF VARIABLE EVALUATIONS**: 500040

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**NUMBER OF FUNCTION POINTS**: 1152

**MOST RECENT BLOCK ID**: 1754

**NUMBER OF BLOCK SPACES USED**: 1918

**NUMBER OF REPORT LINES**: 96

**NUMBER OF VARIABLE ELEMENTS**: 1129

**CURRENT UTILIZATION OF STACKS**: 2607
APPENDIX E
TERMS AND ABBREVIATIONS

A. A/D - Analog/Digital
   ADI - Attitude Director Indicator
   ADTA - Air Data Transducer Assembly
   ALT - Approach and Landing Test
   AMI - Alpha/Mach Indicator
   Auto - Automatic
   Avg - Average
   AVVI - Altitude Vertical Velocity Indicator

B. BCE - Bus Control Element
   BF - Brake Flap
   bps - bits per second

C. CAS - Command Augmentation System
   CH/MS - Characters per Millisecond (Appendix D)
   CPDS - Computer Program Development Specification
   CRT - Cathode Ray Tube
   DD - Dedicated Display
   DDPS - Digital Data Processing System
   DDU - Digital Display Unit
   DEU - Display Electronic Unit
   DFN - Discrete Function
   DMA - Direct Memory Access
   DU - Display Unit

F. FAOI - Flight Aft Operational Instrumentation
   FCOS - Flight Computer Operating System
   FCS/DD - Flight Control System/Digital Data
   FDI - Fault Detection and Identification
   FDIR - Fault Detection Identification and Recovery
   FFOI - Flight Forward Operational Instrumentation
   FSW - Flight Software
   FSSR - Functional Subsystem Software Requirements

G. GPC - General-Purpose Computer

I. ICC - Inter-Computer Communication
   IMSIM - Information Management System Interpretive Model
   IMU - Inertial Measurement Unit
   IOP - Input/Output Processor
   I/O - Input/Output

K. KB - Keyboard
   KBPS - Kilobits per second
   KBU - Keyboard Unit

L. LDB - Launch Data Bus
M. MCDS - Multifunction CRT Display System
MDM - Multiplexer/Demultiplexer
M/D - Manual/Direct
M E - Message Ends (Appendix C)
MM - Mass Memory
MODLIT - SDC Discrete System Simulator
ms - millisecond
MS - Message Start (Appendix C)
MSC - Master Sequence Controller
MSC - Moding, Sequencing and Control
msg - message
MSBLS - Microwave Scan Beam Landing System

N. NASA - National Aeronautics and Space Administration

O. OMS - Orbiter Maneuvering Subsystem
OPS - Operations or Operational Sequence
OT - Operational Instrumentation

P. PCMMU - Pulse Code Modulator Master Unit
PL - Payload

R. RM-Nav - Redundancy Management - Navigation
RM-Cont - Redundancy Management - Control

S. S.D. - Std. Deviation
SDC - System Development Corporation
S.M. - System Management
S.O.W. - Statement of Work
Spec - Specialist

T. TACAN - Tactical Air Navigation
TAEM - Terminal Area Energy Management
T E - Task Ends (Appendix C)
TI - Task Interrupt (Appendix C)
TOT - Total
TS - Task Start (Appendix C)
TUS - Time Units (Appendix C)
TVC - Thrust Vector Control
TW - Task in Wait State (Appendix C)
TX - Task in Execution (Appendix C)

U. UI - User Interface

V. V - Variable
VIRT MACH - Virtual Machine (Appendix D)
VM - Virtual Machine

W. WONG - Weight on Nose Gear

X. X - Savex Cell
APPENDIX F

REFERENCES


17. IBM Electronic Systems Center, 74-A31-001, Space Shuttle Advanced System/4 Pi - Input/Output Processor (IOP), Functional Description, 6 May 1974


28. IBM Memorandum C69-75-256, Instruction Execution Times, 18 September 1975.


34. IBM FSW Design & Development Integration, Software Awareness Memorandum 10H, FSW Process Priorities, 20 November 1975.