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CAMERA (CCD-BURIED CHANNEL), REVISION 1
Final Report (Fairchild Imaging Systems)
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FINAL REPORT
SOLID STATE TELEVISION CAMERA
(CCD-Buried Channel)

3 December 1976



FAIRCHILD IMAGING SYSTEMS
A Division of Fairchild Camera and Instrument Corporation
300 Robbins Lane, Syosset, New York 11791

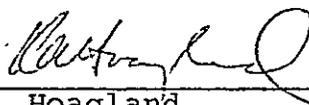
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FINAL REPORT

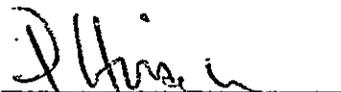
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ABSTRACT

The development of an all solid-state television camera, which uses a buried channel charge-coupled device (CCD) as the image sensor, was undertaken. A 380 x 488 element CCD array is utilized to ensure compatibility with 525-line transmission and display monitor equipment. Specific camera design approaches selected for study and analysis included (a) optional clocking modes for either fast (1/60 second) or normal (1/30 second) frame readout, (b) techniques for the elimination or suppression of CCD blemish effects, and (c) automatic light control and video gain control (i.e., ALC and AGC) techniques to eliminate or minimize sensor overload due to bright objects in the scene. Preferred approaches were determined and integrated into a deliverable solid state TV Camera which addressed the program requirements for a prototype qualifiable to space environment conditions.



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1.0 PURPOSE

1.1 OBJECTIVE

The objective of this Final Report is to describe the effort required to perform the engineering, design, development, test, and delivery of a solid-state television camera.

1.2 END PRODUCT

The end product of this contractual effort is a solid-state television camera which uses a buried-channel CCD (charge-coupled device) as the image sensor. It employs a scanning technique which allows the CCD to be used with conventional transmission characteristics and monitor displays meeting Electronic Industries Association (EIA) commercial standards.

Based on design investigations, several important features have been recommended and included in the end product design to make it compatible with the ultimate spaceborne application.

2.0 SCOPE

Fairchild has provided the necessary resources to perform development and test of a solid-state television camera using a buried-channel CCD for the image sensor. The engineering and design phases of the camera effort were accomplished in phase "A" of the subject contract. The results, reported in Fairchild Final Report ED-AX-75 dated July 1976, are incorporated in synopsis in Section 3 (para. 3.1).

CCD image sensors of the buried-channel interline-transfer type have features which make these devices particularly useful for solid-state TV cameras where small size, low power/low voltage operation, high sensitivity and extreme ruggedness are either desirable or mandatory characteristics. The solid-state camera design, which has evolved as a result of this NASA/JSC program, satisfies the requirements for a deliverable end product which can demonstrate feasibility for application in future space missions. The camera design utilizes a 380 x 488 element CCD to insure full compatibility with 525 line television transmission and display monitors without requiring the use of pseudo-resolution or special formatting techniques. Several additional features recommended for inclusion in the deliverable camera address specific aspects of the NASA/JSC requirement:

- . Dual-mode clocking has been included to demonstrate feasibility for operation with

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full-frame readout intervals of either 1/60 second or 1/30 second.

- . A thermoelectric cooling feature for the CCD minimizes thermally-generated dark current defects, and reduces the average dark-signal level, thereby effecting an increase in useful sensitivity and dynamic range.
- . Wide-range automatic light control, supplemented by a video AGC technique, has been included to minimize or eliminate CCD overload effects caused by intense point sources in the field-of-view.

The specific design requirements and the design implementations are discussed in detail in para. 3.2 of Section 3. The end product prototype camera development is described in para 3.3. and the acceptance test procedures and results are presented in Section 4. The camera development and test efforts were accomplished in Phase "B" segment of the contract. Recommendations are offered in Section 5 for future CCD camera concepts for the NASA/JSC spaceborne application.

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3.0 TECHNICAL REQUIREMENTS

This section presents a technical synopsis of program results for each of the tasks defined by Section 3.0 requirements of the contract Exhibit "A" Statement of Work. Major subsection headings conform with the subsection nomenclature of Exhibit "A". This section also presents the study, design, and development requirements for each of the tasks defined by Section 3.0 requirements of the contract Exhibits "A" and "B" Statements of Work. Major subheadings conform to the subsection nomenclature.

3.1 STUDY REQUIREMENTS

Study tasks were selected to develop alternate approaches and concepts applicable to SOW objectives. These were then examined in detail, including breadboard tests where necessary, to determine preferred approaches and concepts to be implemented in the deliverable solid state camera. Study task results are described in the Clocking Options, Blemish Suppression and Light Control subsections which follow.

A. Clocking Options

The 380 x 488 CCD sensor was specifically designed for 2/1 interlaced readout with separate photosensor rows for addressing each active line of the displayed TV frame. The integration time for the normal high-resolution readout mode is 1/30 second. There is an alternate readout clocking scheme which can be used when it is desirable to shorten the integration time to 1/60 second. In this mode charge packets from vertically adjacent sites along the even

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and odd field rows are added together in the vertical shift register before the normal charge transport clocking begins. Although the alternate mode has less vertical resolution than the normal mode the difference can be minimized by performing the addition differently on alternate fields. For example during the first field sensor rows 1 and 2, 3 and 4, 5 and 6, etc., are added together. During the next field sensor rows 2 and 3, 4 and 5, 6 and 7, etc. are added, with the row-addition sequence for subsequent fields alternating at field rate.

Because of the digital nature of the charge transport functions, relatively simple circuit modifications can be used to change the clocking system from normal to alternate mode operation. Feasibility for alternate mode operation was established by breadboard tests. Vertical resolution was observed to be about 2/3 of the normal Nyquist limit value. It was also determined that it is feasible to design the deliverable camera with a selector switch to enable operation in either mode.

Although the alternate mode has less static vertical resolution than the normal mode, there are compensating advantages: (1) shorter integration times can improve resolution when viewing moving images and (2) since all photosensing sites are read out during the same field interval, the alternate mode is preferred for sequential color TV applications.

B. Blemish Suppression

Early 380 x 488 arrays were relatively free of cosmetic defects except for isolated single element blemishes which appeared as

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white spots in the video display. To suppress these blemishes a Field Programmable Logic Array (FPLA) was considered for inclusion in the video processor circuit. The FPLA is a digital memory which can be used to store the locations of defective CCD elements. As shown in Figure 3-1 the FPLA accepts inputs from synchronous line and element counters. When a count corresponding to the location of the defective element is decoded, the FPLA provides a pulse output which can be used to inhibit the defective readout. During the breadboard test phase of the FPLA investigation, significantly improved blemish quality was achieved with 380 x 488 arrays from runs being fabricated for NAVELEX program requirements. A number of arrays were free of blemishes larger than one element when tested at room temperature and several devices exhibited near-zero defect counts when cooled to reduce the average dark current level. Nearly all defects were adequately suppressed at -10°C .

Since Fairchild is confident that further improvements in array quality can be expected, the FPLA blemish suppression technique, which adds circuit complexity, is not considered a desirable feature for inclusion in the deliverable camera. A means for array temperature control, such as a thermoelectric cooler, is desirable since it has been established that both dark signal and blemishes can be significantly reduced by cooling.

C. Light Control

Wide-range light control is necessary to prevent overload of the CCD sensor when viewing solar illuminated scenes in a space environment. Table 3-1 illustrates a calculation for the minimum control

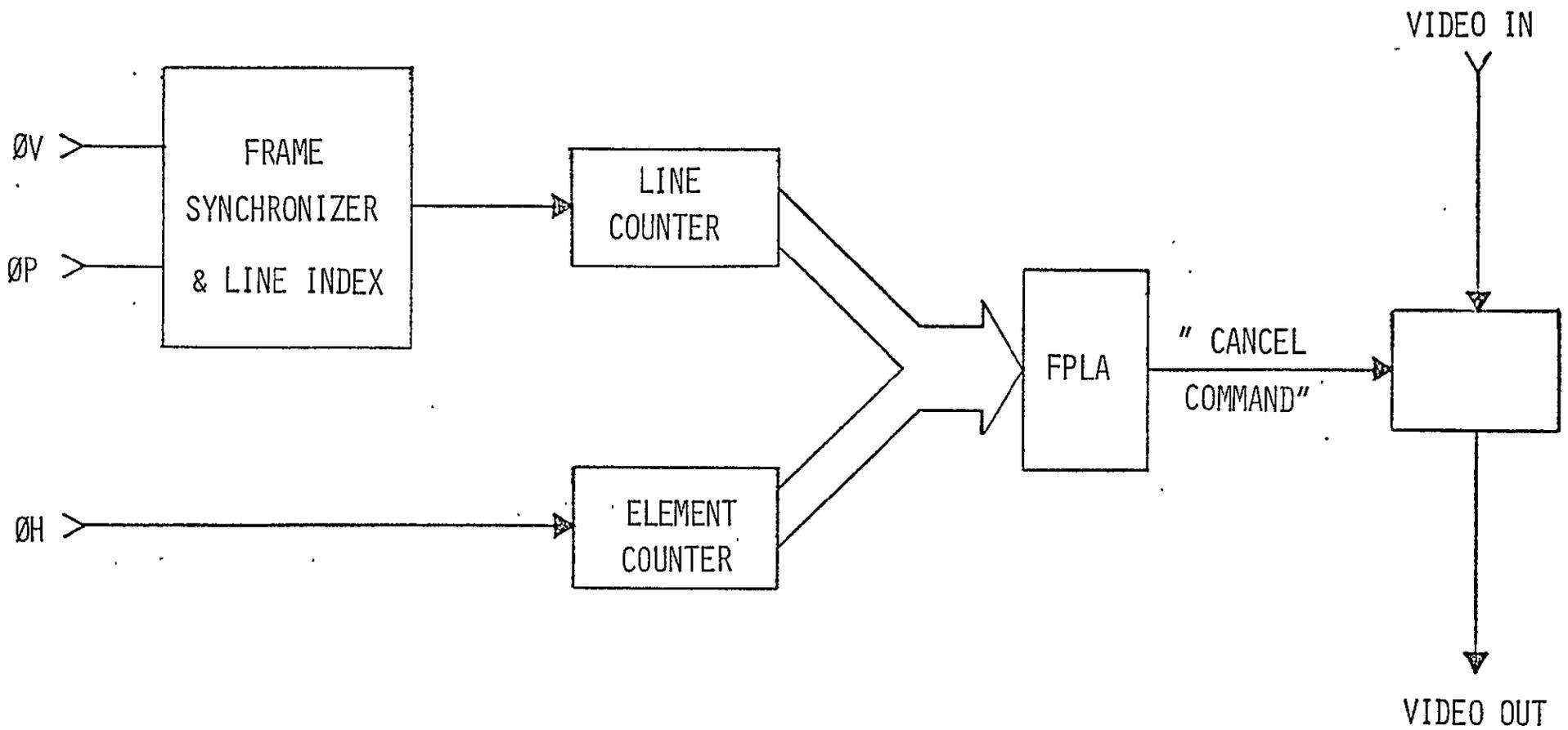


FIGURE 3-1
FPLA BLEMISH CANCELLATION

TABLE 3-1

LIGHT CONTROL RANGE

SENSOR SATURATION: $I_{\max} \approx 0.3 \text{ lumens/sq. ft., } 6000^\circ\text{K}$

SCENE LUMINANCE: Max. highlight, $B_{\text{scene}} = 1.3 \times 10^4$
lumens/sq. ft.

OPTICAL EFFICIENCY, α : $\alpha = \frac{t}{4f^2} = 0.2/f^2$

$$\alpha_{\min} = I_{\text{sensor}}/B_{\text{scene}} = 0.3/1.3 \times 10^4 \approx 2.3 \times 10^{-5}$$

LIGHT CONTROL RANGE: $f_{\max} = (0.2/2.3 \times 10^{-5})^{1/2} \approx 93$

$$f_{\max}/f_{\min} = 93/1.4 = 66.4$$

$$\therefore \text{Minimum Control Range} = (f_{\max}/f_{\min})^2 \approx 4.4 \times 10^3/1$$

CONDITIONS: 25 mA/W, 2854K CCD response; 30F/S

Solar Illuminance, 100% Diffuse
Reflectance Surfaces

Transmission, $t = 0.8$

$f_{\min} = 1.4$

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range assuming 100% diffuse reflectance scene surfaces exposed to solar illumination outside the earth's atmosphere. If the camera is equipped with an f1.4 lens, the effective lens f-value must be increased to at least f93 to prevent overload, indicating a minimum light control range of $4.4 \times 10^3/1$.

In order to assess the problem if specularly reflecting test objects are considered, an outdoor simulation test was conducted using a Fairchild Type MV201 CCD-TV camera. The results of this test are given in Table 3-2. In this case an attenuation in the optical path equivalent to f1100, was necessary to avoid overload with the standard Fairchild minus-red filter in front of the lens. With smaller f-values than those indicated, specularly reflected spot images caused CCD sensor blooming along the column direction.

Specular solar images can be expected if the camera is required to view space objects with a polished metallic finish, or other reflective-type surface. To minimize blooming for this condition, the light control range should be two or three orders of magnitude greater than the value indicated in Table 3-1 for diffuse reflectance surfaces.

Techniques for light control over the required range include a number of approaches such as filter wheels, movable film-strip filters, and lens iris-spot filters, which can be broadly classified as approaches requiring electro-mechanical control. The electro-optical approaches investigated, such as PLZT and liquid-crystal light valves were limited in control range (i.e. 10^2 to 10^3) with relatively poor open state transmission characteristics ($t \approx 0.2$).

TABLE 3-2

MV 201 OUTDOOR TEST RESULTS

"DR" Test Object Luminance, $B = 8800 \text{ ft. L.}$

Solar Illumination, $I = 8800/0.9 \approx 10^4 \text{ fc}$

<u>Array Sat, "DR" Test Object</u>	<u>f equiv.</u>
With MR Filter: f2.8 + ND 2	f28
Without Filter: f8.0 + ND 2	f80

<u>Array Sat "SR" Test Object</u>	
With MR Filter: f11 + ND 4	f1100
Without Filter: f22 + ND 4	f2200

(MR Filter Factor Equiv. To Schott KG-3, 5.5 mm)

NOTES:

1. "DR" test object is a Kodak Test Card, diffuse reflectivity ≈ 0.9 .
2. "SR" test object is a metallic-coated plastic film (with surface wrinkled).
3. MR filter is a Fairchild CCD-TV minus-red filter.
4. ND indicates neutral-density filter value.
5. f equiv. indicates the equivalent f-value of the objective optics required to suppress blooming in the column direction.

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The approach selected for the deliverable camera is based on the iris-spot filter principle, as implemented in commercially available Cosmincar type ES auto-iris lenses. Characteristics for three lenses, with 12.5, 25, and 50mm focal lengths, are given in Table 3-3.

The light control range of the lens (7×10^4) will be extended by utilizing the dynamic range inherent in the CCD sensor.

This is implemented with separate control loops for the automatic light control (ALC) and automatic gain control (AGC) functions of the camera electronics, as indicated in Figure 3-2.

3.1.1 Design Requirements

The concepts and theories emanating from the study effort have been integrated into a design for the deliverable solid-state camera. The camera circuitry is shown in block diagram form in Figure 3-3. The finalized circuit diagrams for the deliverable camera are present in para. 3.3 of this Section. The logic, driver and video processor circuits are similar to existing circuitry developed on contract No. N00010-75-C-0289 for a Missile Guidance Camera utilizing a 380 x 488 CCD array. These circuits are contained on three printed circuit cards.

The first card contains all TV sync, drive, and blanking signals in accordance with EIA-RS-170. A National MM4320 LSI-TV sync chip, combined with a crystal oscillator and output buffer stages, is used to generate these TV timing signals. Additional counters, gates, flip-flops and buffers are used to generate the timing logic signals for the CCD array.

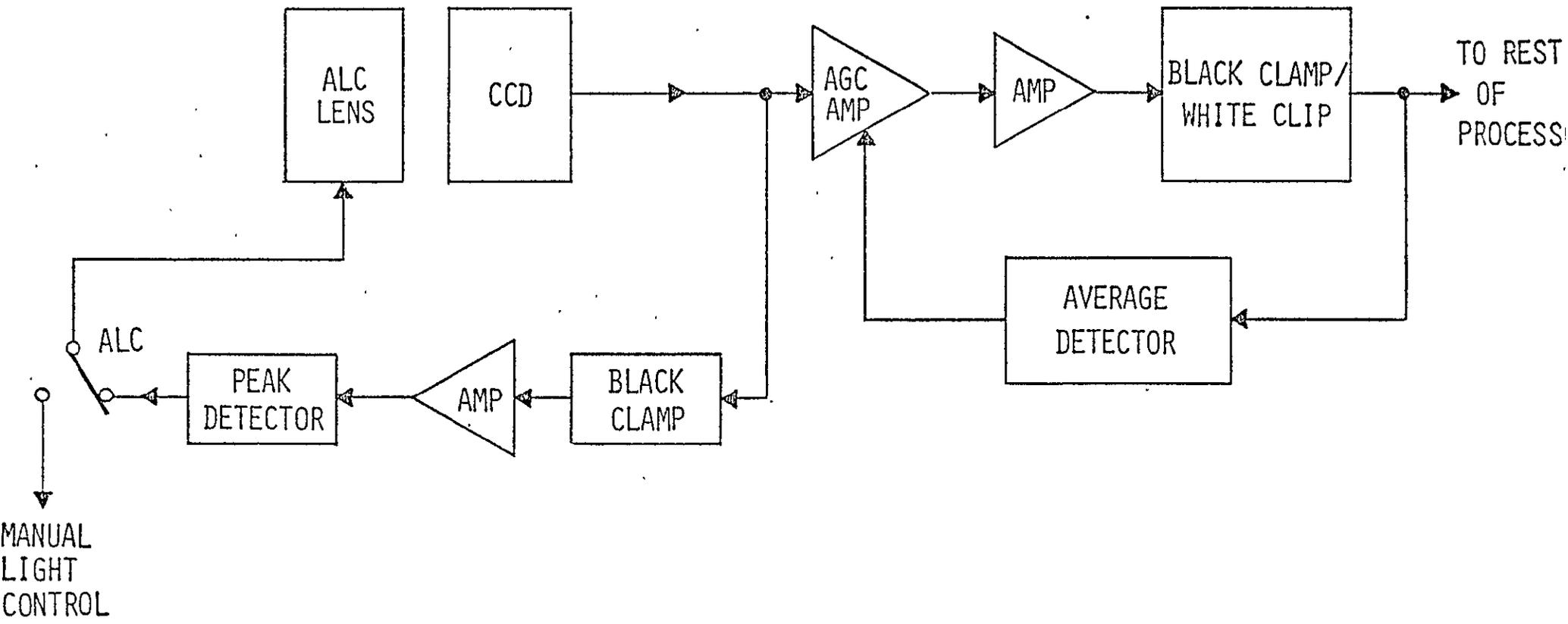


FIGURE 3-2

VIDEO PROCESSOR - AUTOMATIC LIGHT CONTROL/AUTOMATIC GAIN CONTROL BLOCK DIAGRAM

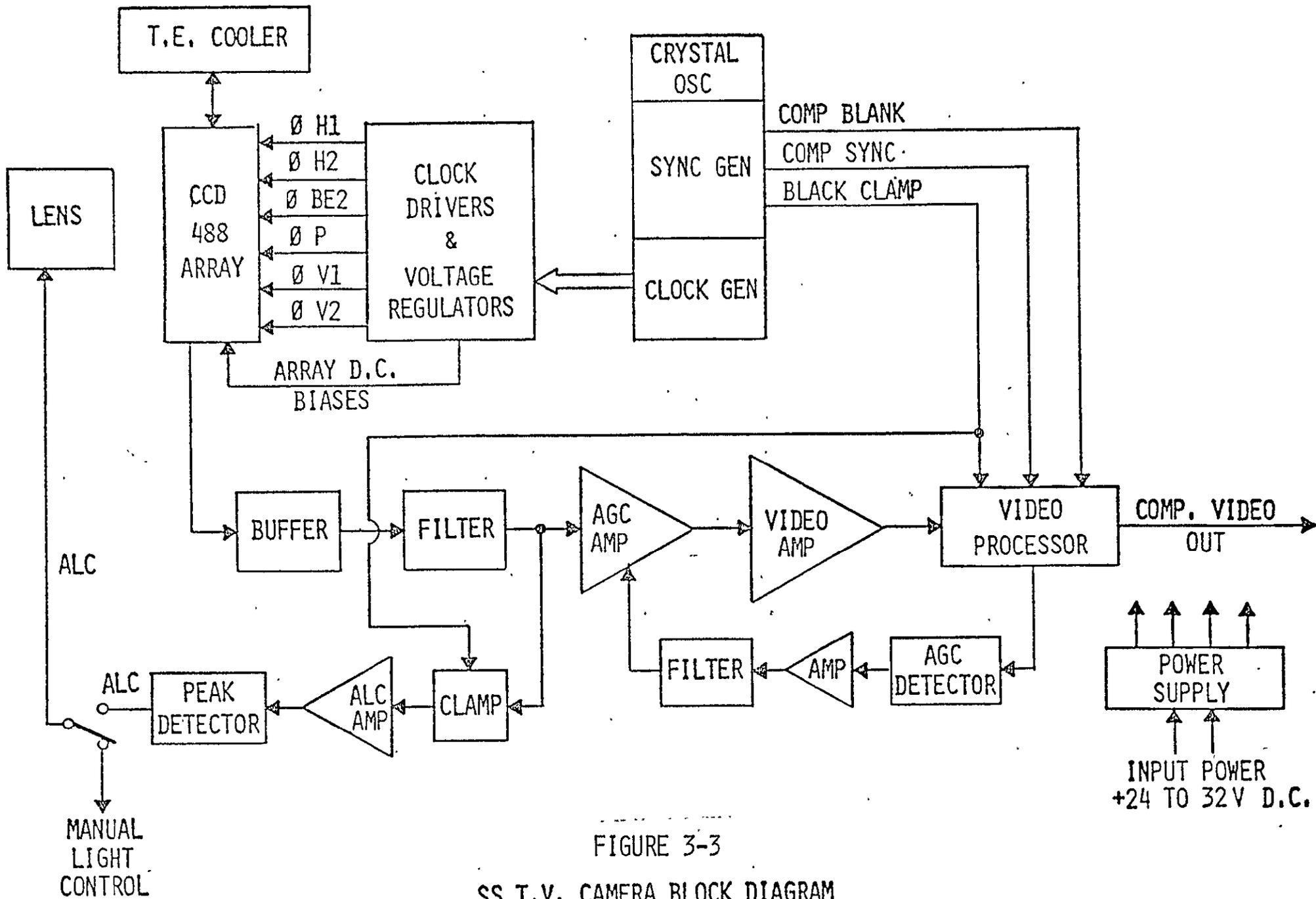


FIGURE 3-3

SS T.V. CAMERA BLOCK DIAGRAM

TABLE 3-3

COSMICAR AUTO-IRIS "ES" SERIES LENSES

Specification	<u>Model No.</u>		
	B1214AES	B2514CES	B5018AES
Focal Length	12.5mm	25mm	50mm
Maximum Aperture	1 : 1.4	1 : 1.4	1 : 1.8
Iris Range	1.4 - 360	1.4 - 360	1.8 - 360
Illumination Ratio	66,000X	66,000X	40,000X
Image Size	2/3" & 1"	2/3" & 1"	2/3" & 1"
Shortest Focus Distance	0.3m	0.6m	1.0m
Flange Back		17.526mm	
Focal Adjustment	Straight Helicoid: Rotating Angle 210° Torque 450±200g.cm.		
Mount		C Mount	
Filter Size		Ø = 49.0mm	
Overall Dimensions		66 x 51mm	
Weight	380g	350g	370g

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The second board contains the array logic driver stages, voltage regulators and setup pots for the array. FSDS hybrid drivers are used to drive the capacitive load of the array.

The third circuit board contains all of the video circuits, which consists of: an input buffer; a Nyquist filter; a variable gain AGC stage; a fixed gain video amplifier and video processor stages, which perform black-level clamping, pedestal adjustment, blanking insertion and sync insertion. In addition, there is an AGC detector, filter and amplifier stage and the ALC circuits to control the auto-iris lens. There is provision for operating with either manual light control or with ALC.

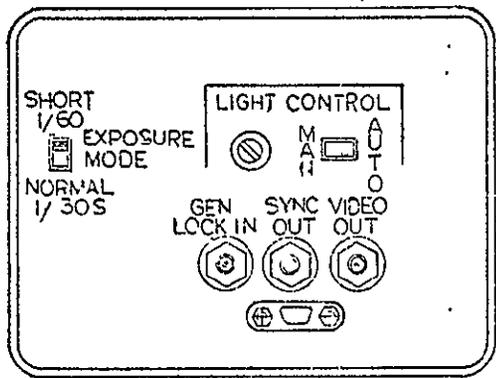
Figure 3-4 illustrates the packaging design for the deliverable camera. The CCD and a thermoelectric cooler are contained in a separate short housing affixed to the front face of a main rectangular housing containing the three circuit boards. All controls and connectors are mounted on the rear of the CCD housing.

An additional circuit board (misc/control board) is added to the above boards to complete the electric packages in the deliverable NASA/JSC camera.

A summary of specifications for the deliverable camera is given in Table 3-4.

3.2 DESIGN SPECIFICATIONS

Table 3-5 summarizes the detailed performance specifications applicable to the deliverable solid state camera. These specifications are in conformance with both Exhibit "A" and Exhibit "B"



VIEW A-A

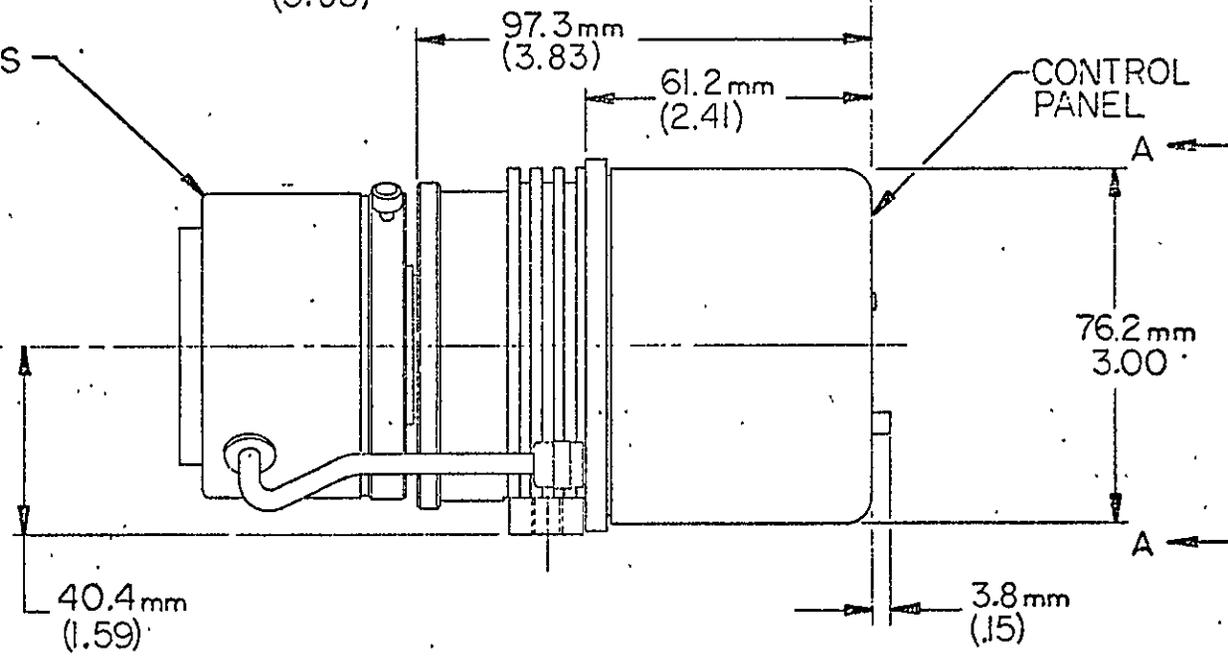
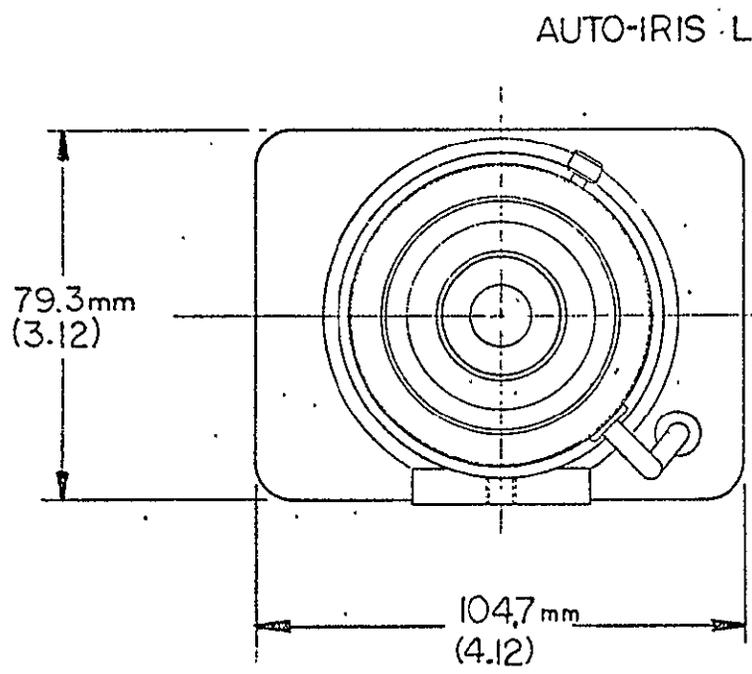
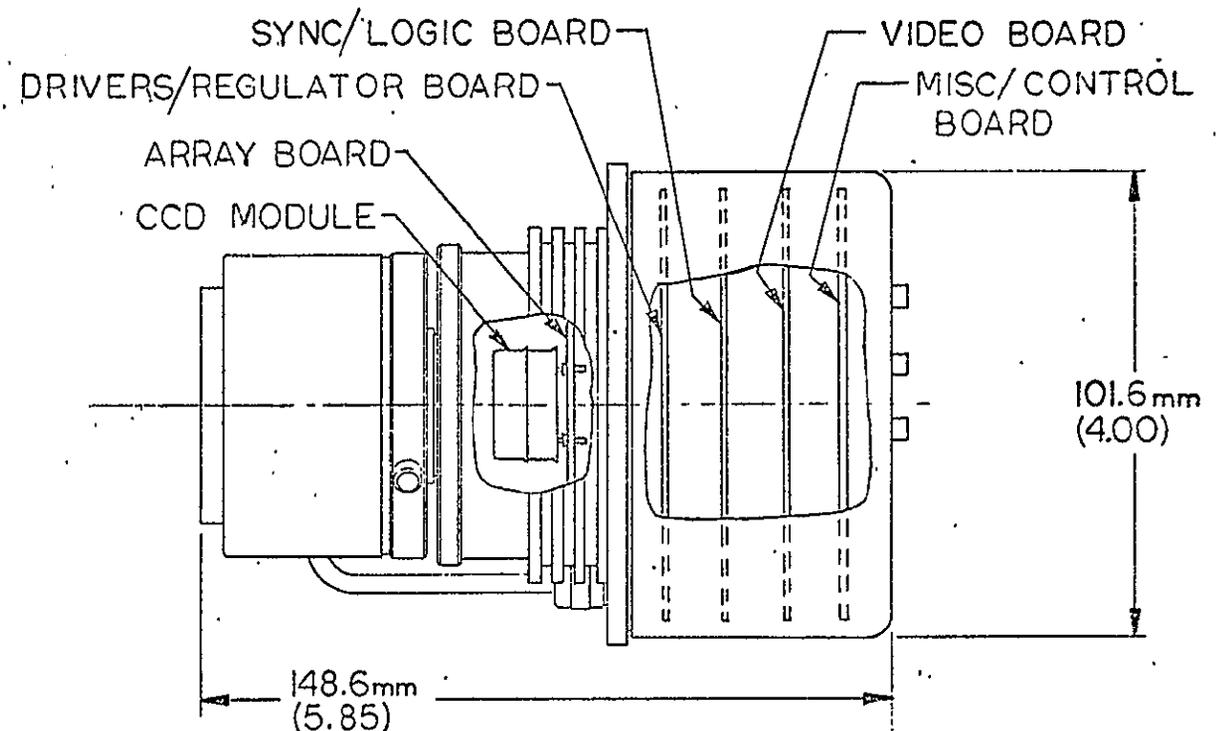


FIGURE 3-4 FAIRCHILD CCAID-488 SSTV CAMERA
CAMERA OUTLINE DWG
(NASA/JSC PROTOTYPE)

TABLE 3-4

SPECIFICATIONS

CCAID-488 SSTV CAMERA - (NASA/SSC PROTOTYPE)

Sensor	Fairchild CCD 488 x 380 array
Spectral Response	0.45 to 1.1 Micrometer
Optics	Auto-Iris fl.4-f360, "C" Mount
Sensitivity (Note 1)	Sensor Illuminance 2×10^{-4} fc
Electronic AGC	100:1 Range
Geometric Linearity	No Camera Distortion. System Performance limited by lens and display.
Frame Rate	30 Frames/sec.
Line Rate	15,750 Lines/sec. (nominal)
Format	488 lines: 380 picture elements/line
Sync	2:1 standard interlace
Video Output	1V p-p, composite video (RS 170)
Video Line Output	500 ft., 75 ohm
Power (uncooled)	6 watts (Note 2)
Camera Size (excluding lens)	<420 cc (see drawing)
Weight (excluding lens)	<0.9 kg
Ambient Temperature	0° to 50° C

NOTES:

1. Highlight illumination with 2854°K source (tungsten) for a S/N ratio of 1 (peak signal to temporal RMS noise ratio).
2. The camera will operate with ± 12 VDC and +5 VDC. A dc to dc converter will be supplied for operation from an unregulated +28 VDC supply.

TABLE 3-5

DETAILED CAMERA PERFORMANCE SPECIFICATIONS

		<u>Ref. Exhibit "A"</u> <u>SOW Paragraph No.</u>
RESOLUTION, TVL/PH		
Overlap interlace mode	285x325 (HXV)	3.2.1, 3.2.9
High resolution mode	285x485 (HXV)	
FIELD/FRAME INTERLACE RATIO	2 to 1	3.2.2
FORMAT ASPECT RATIO, HXV	4 x 3	3.2.3
VERTICAL SCAN		3.2.4
Frame rate	60/sec	
Field rate	30/sec	
Line periods/frame	525	
GRAY SCALE STEPS ($\sqrt{2}$)	10	3.2.5.1
DYNAMIC LIGHT RANGE (with ALC)	500/1 min.	3.2.5.2
OPERATING VOLTAGE	+28V \pm 4VDC	3.2.6
POWER (uncooled)	6W, max	3.2.7
OUTPUT VIDEO FORMAT		3.2.8
Load Impedance	75 Ω \pm 5%	3.2.8.1
Composite video polarity	Black negative	3.2.8.2.1
Signal levels, IRE units		3.2.8.2.2
reference white	+100	
blanking level	0	
sync	-40	
peak-to-peak	140	
Composite output video voltage	1V p-p (nom.)	3.2.10
Blanked picture signal, with setup	0.714 \pm 0.1V	3.2.10.1
Sync signal (from OVDC, ref.)	0.286 \pm 0.05V	3.2.10.2
Setup, blanking level to reference black level, (IRE units)	7.5 \pm 5	3.2.11

TABLE 3-5 (Cont.)

		Ref. Exhibit "A" <u>SOW Paragraph No.</u>
SIGNAL-TO-NOISE RATIO	35db (min)	3.2.11
GEOMETRIC DISTORTION (exc. lens)	<2%	3.2.12
SPOTS AND BLEMISHES	(See below)	3.2.13
BLOOMING	ALC/AGC inhibited	3.2.14
CAMERA OPTICS	Cosmicar Model B2514CES 25mm, f1.4-f360	3.2.15
CAMERA CONTROLS	Power ON/OFF Light Control AUTO/MANUAL Vertical Scan OVERLAP/NORMAL	3.2.16
CAMERA INTERFACES		
Connectors	Output Video Camera Power Lens Control	3.2.17
SPOTS AND BLEMISHES		3.2.13

A spot or blemish shall be defined as a video signal transition equal to or greater than 7% of the CCD sensor saturation signal observed with the sensor uniformly illuminated at a level corresponding to 50% saturation. The size of a spot or blemish shall be determined by counting the number of scan lines on which the transition occurs; i.e., the number of lines per frame on which the transition is greater than 7% of saturation signal. The total number of white and dark spots shall be less than or equal to:

10 spots over 1 but less than or equal to 4 TV lines/frame

2 spots over 4 but less than or equal to 8 TV lines/frame

0 spots over 8 TV lines/frame

No horizontal or vertical black lines resulting from a failed CCD element shall be allowed. Shading signal variations along any line averaged over sections of 10% of picture width shall not exceed 10% of V_{sat} at 50% uniform sensor illumination.

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requirements of the contract Statement of Work for all paragraphs 3.2.1 through 3.2.17, inclusive. The requirements and the implementations are discussed in detail in the following paragraphs 3.2.1 through 3.2.17.

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3.2 DESIGN

3.2.1 Resolution

Requirement: The buried-channel CCD matrix shall be no smaller than 488 (V) x 380 (H) elements. The number of vertical scan lines shall be compatible with the EIA positive interlace format.

Implementation: The camera design uses the Fairchild CCD221. This is a buried-channel area imaging sensor with 488 x 380 picture elements. The interline-transfer organization of this device provides interlaced video. The device is operated with a TV sync generator to assure compatibility with EIA standard television format.

3.2.2 Interlace Ratio

Requirement: Positive 2 to 1.

Implementation: The CCD 221 was specifically designed for a positive 2 to 1 interlaced readout. The normal operating mode is to alternate between transferring video information from odd and even numbered lines to the shift registers thus providing alternating odd and even fields.

3.2.3 Aspect Ratio

Requirement: The aspect ratio shall be 4 horizontally by 3 vertically.

Implementation: The X-Y format of the CCD221 has been designed to provide a 4 x 3 image aspect ratio. The image sensing sites are located on 18 uM vertical centers and 30 uM horizontal centers. The dimensions of the image sensing area are 8.8mm vertical and 11.4mm horizontal.

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3.2.4 Vertical Scan

Requirement: Nominal 60 fields/second, 30 frames/second and 525 lines/frame.

Implementation: The CCD221 with its 488 active lines has been designed to be fully compatible with 525 lines/frame EIA standard video. The camera design uses an integrated circuit television sync generator together with a crystal oscillator to accurately generate the timing for 60 field-30 frame operation.

3.2.5 Operating Light Ranges

3.2.5.1 Gray Scale Response

Requirement: Under normal conditions with a 10 step logarithmic gray scale target (contrast ratio 32:1) projected onto sensor faceplate with highlight illumination of 5×10^{-2} foot-candles, the camera shall resolve the 10 steps with its output displayed on a television monitor and exhibit a noise ratio of 35db minimum (refer to 3.2.11).

Implementation: The highlight illumination and contrast ratio specified are within the linear output range of the CCD221 array. The video amplifier has an adequate linear range to reproduce the signal. The typical saturation exposure of the array is $0.2 \text{ uJ/cm}^2 = 0.02 \text{ fcs}$. In normal operation, the integration time is 1/30 second thus the saturation exposure corresponds to an illumination of 12×10^{-2} foot-candle. The specified illumination level is then 41.67% of typical saturation illumination. Considering the 32:1 contrast ratio the last step is then 1/77 of saturation illumination. The array has a typical dynamic range of 300:1 thus the design readily accommodates the 10 gray scale requirement.

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3.2.5.2 Dynamic Light Range

Requirement: The camera shall meet performance specifications over a minimum 500:1 scene highlight illumination range. Minimum highlight illumination is 5×10^{-2} foot-candles on the sensor faceplate.

Implementation: The camera uses a combination of automatic light control (ALC) and automatic gain control (AGC) to maximize the dynamic range. The ALC controls the illumination reaching the sensor. It is implemented with commercially available Auto Iris lens. This lens uses non-AGC'd video as the feedback to an iris control servo. The iris' range is from a relative aperture of f1.4 to f360 and can thus accommodate an illumination ratio of 66000:1.

3.2.6 Operating Voltage

Requirement: Nominal 28 Volts. Camera shall operate normally from 24 to 32 volts. Camera circuits shall be isolated so that power line and other circuit noise does not feed through to the video output.

Implementation: A power supply unit is used with the camera. This unit operates from 28 ± 4 volts and provides the DC voltages required by the camera. Two DC-DC converters are provided. The first produces + 12 volts and - 12 volts for the analog circuits and 5 volts for the logic. The second converter generates the 5 volts for the thermo-electric cooler. Decoupling is provided at critical circuits, such as the array, to prevent noise from coupling through to the output video.

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3.2.7 Power Consumption

Requirement: The design of this camera shall be such that power consumption shall be minimized.

Implementation: The uncooled camera power consumption is 6 watts. This is measured at the camera inputs (on the ± 12 volt and 5 volt lines). Assuming a DC-DC converter efficiency of 50% results in an overall power drain of 12 watts or 0.43 amperes at 28 volts.

3.2.8 Output Video Format

3.2.8.1 Standard Load Impedance

Requirement: Output impedance 75 ohms. Load impedance 75 ohms.

Implementation: The 75 ohm output impedance is obtained with a 68 ohm resistor in series with an emitter follower output. With this source impedance, the camera will drive a 75 ohm load.

3.2.8.2 Composite Picture Signal

3.2.8.2.1 Polarity

Requirement: The standard polarity of the output of the camera shall be black-negative.

Implementation: The camera has been designed and will be tested for black negative polarity video.

3.2.8.2.2 Signal Levels

Requirements: The composite picture signal shall be measured using both IRE units and volts. Measurement of signal levels shall be made in accordance with appropriate portions of 58 IRE 23.51 IRE Standards on Television measurement of Luminance Signal Levels.

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Implementation: These measurement requirements have been reflected in the Acceptance Test Procedure.

3.2.8.3 Sync Signal Waveforms

Requirement: The sync signal waveform shall meet EIA Standard RS-170.

Implementation: The camera design uses an MM4320 integrated circuit TV sync generator. The composite blanking and the composite sync signals from this IC are combined with the video at the appropriate voltage levels to produce the composite picture signal. When the sync generator is controlled by a crystal oscillator it provides sync timing to RS-170.

3.2.9 Output Resolution Response

Requirement: Resolution response shall be measured in accordance with IEEE 208, 60 IRE 23.52, Standards on Video

Techniques: Measurement of Resolution of Camera Systems. The horizontal resolution response shall not be degraded by the video processing. The limiting resolution shall be no less than 70% of the number of TV elements.

Implementation: The Acceptance Test Procedure reflects the above referenced specification. Two separate tests are involved. In the first limiting resolution is determined. The vertical resolution shall exceed $0.7 \times 488 = 342$ TV lines/picture height. The horizontal resolution shall exceed $0.7 \times 0.75 (380) = 200$ TV lines/picture height. The limiting resolution is determined using a standard test chart with graduated wedges. The resolution response is measured using a spatial frequency test chart with test bars at $1/8$, $1/4$, $1/2$ and Nyquist-limit horizontal resolution.

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The camera has been designed for limiting resolution of:

Horizontal: 285 TV lines/picture height

Vertical: 485 TV lines/picture height.

These resolutions are for the normal operating mode with 1/30 second integration time. An alternate operating mode providing 1/60 second integration time is also incorporated into the camera. This alternate readout clocking technique is discussed in paragraph 3.1.A. It reduces the vertical resolution to about 2/3 of the normal Nyquist limit value and has no effect on the horizontal resolution. Thus in the alternate readout mode the camera's vertical resolution is specified as 325 TV lines/picture height.

3.2.10 Output Video Voltage

Requirement: The composite picture signal amplitude from sync tip to reference white, when the camera drives a 75 ohm load, shall nominally be 1 volt peak-to-peak.

3.2.10.1 The blanked picture signal with setup, as measured from blanking level to reference white level, shall be 0.714 ± 0.1 volts (100 IRE units).

3.2.10.2 The synchronizing signal, as measured from 0 volts DC shall be $+ 0.286 \pm 0.05$ volts (40 IRE units).

3.2.10.3 The standard setup shall be 7.5 ± 5 IRE units measured from blanking level to reference black level.

Implementation: The camera has been designed to provide the video voltage levels cited above. Factory adjustments are incorporated into the camera design so that the various voltages can be set during initial testing.

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3.2.11 Signal-To-Noise Ratio

Requirement: The S/N for nominal camera operation shall be 35db minimum, peak-to-peak noncomposite picture signal voltage to rms random noise voltage. The S/N for impulse or interference noise sources shall be 30db minimum.

Implementation: The camera has been designed with noise minimization as an important guideline. This has been reflected in particular attention to decoupling and isolation of ground paths. For the purposes of the S/N measurement in the Acceptance Test Procedure, the rms noise will be considered as 1/6 of the measured peak-to-peak noise.

3.2.12 Geometric Distortion

Requirement: The TV camera geometric distortion exclusive of the lens shall not exceed a displacement of any picture element from its true position in the object being viewed by more than $\pm 2\%$ of the picture height within Zones 1 and 2 and $\pm 5\%$ of the picture height within Zone 3. For any increment of 5% of the picture height, the rate of change of displacement of any picture element shall not be greater than 0.5% of the picture height.

Zone 1 shall be defined as the area within an inscribed circle centered within the scanned area the diameter of which is one-half the picture height. Zone 2 shall be the area included within an inscribed circle centered within the scanned area with diameter equal to the picture height, but excluding the area of Zone 1. Zone 3 shall be the remaining area of the scanned picture outside of or excluding Zones 1 and 2.

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Implementation: Since the CCD array is a semiconductor device manufactured with high precision mask making techniques, the geometric spec cited above is easily met.

3.2.13 Spots and Blemishes

Requirement: The total number of white and dark spots equal to or greater than 7% of saturation shall be less than or equal to:

10 spots over 1 but less than or equal to 4 TV lines/frame

2 spots over 4 but less than or equal to 8 TV lines/frame

0 spots over 8 TV lines/frame

No horizontal or vertical black lines resulting from a failed CCD element shall be allowed. Shading signal variations along any line averaged over sections of 10% of picture width shall not exceed 10% of V_{sat} at 50% uniform sensor illumination.

Implementation: The spot and blemish requirement is met by inspecting the images obtained from available arrays with this requirement in mind. An array with the appropriate characteristics, is then selected. Array temperature control using the thermo-electric cooler also helps reduce spots and blemishes since it has been established that both dark signal and blemishes can be significantly reduced by cooling.

3.2.14 Blooming

Requirement: The solid-state image sensor is particularly susceptible to "blooming" - the spreading of an optical overload-generated charge into adjacent regions. The Contractor shall propose various solutions to minimizing the blooming problem, incorporate the most acceptable solution into the camera, and include

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in the final report a detailed discussion of the solutions proposed and further work that may be done in this area.

Implementation: For the purposes of the present program, the most practical solution was deemed to be the combination of automatic light control and automatic gain control. In the future, on chip exposure control and antiblooming features would be the best solution. Investigations into the implementation of these features are currently in progress.

3.2.15 Camera Optics

Requirement: The camera shall be equipped with a lens with a fixed focal length between 25mm and 50mm with manual aperture and focus controls. The aperture control range shall be between f/2.2 to f/16 or better. The lens shall be mounted to the camera such that it will be interchangeable with other lenses. The lens shall be considered a part of the camera for all specifications herein. No development is intended in the optics area.

Implementation: The camera has been designed to accept standard C-mount television lenses. It is supplied with a Cosmincar Model B2514CES.

3.2.16 Camera Controls

Requirement: The camera shall be equipped with external controls that are accessible to the operator. The controls shall be so located, positioned, and labeled with sufficient size and contrast to allow ease of reading and operation.

Implementation: See outline drawing (Figure 3-4)

3.2.17 Camera Interfaces

Requirement: The camera shall include two connections so as to facilitate the provision of camera power from one source and camera video to a standard commercial-type TV monitor. The contractor shall select the appropriate connectors to meet all the requirements of this specification. They shall be small with a minimum number of pins and have a positive locking mechanism. Pin assignments are to be determined by the contractor.

Implementation: The camera interface requirement is a power source of 24 to 32 volts D.C. to the camera power supply unit and a standard commercial-type TV monitor. The input power connects to a pair of pendant wires from the camera power supply unit. Video is fed to the display by coax cable which has a standard BNC connector.

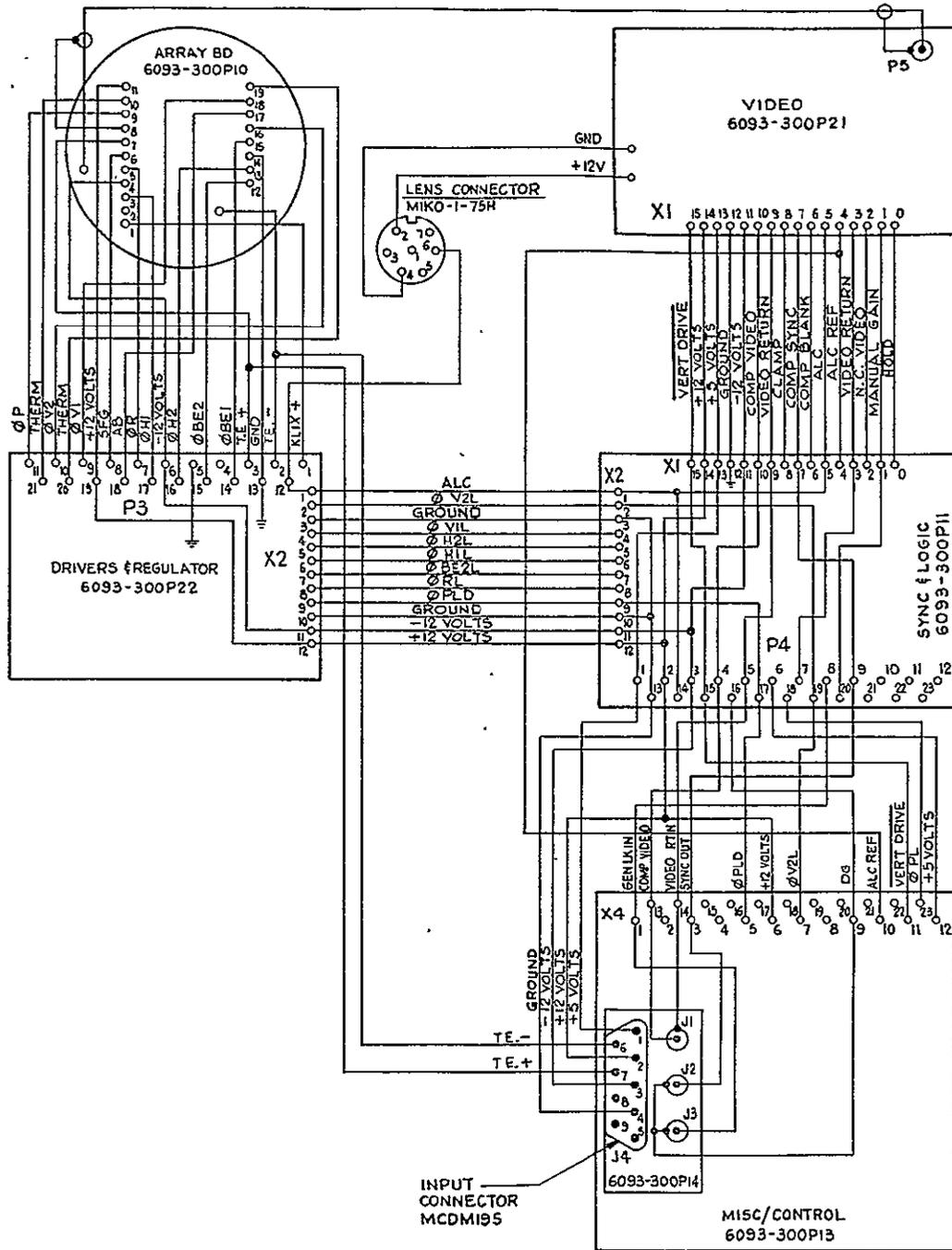


FIGURE 3-5 INTERCONNECT DIAGRAM

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3.3 PROTOTYPE CAMERA DEVELOPMENT

The prototype camera consists of six major electrical sub-assemblies as shown in Figure 3-4 and partially shown in the photograph of Figure 3-6.

- . CCD Module
- . Array Board
- . Drivers/Regulator Board
- . Sync/Logic Board
- . Video Board
- . Misc/Control Board

A lens assembly and power supply unit, as shown in the frontis-piece photograph, completes one system.

3.3.1 Cooled CCD Module

The uncovered CCD module consists of a 488 x 390 element CCD array, a thermoelectric cooler and a heat sink as shown in the CCD Module photograph of Figure 3-7.

3.3.1.1 Thermoelectric Cooler/Packaging

The CCD sensor is cooled thermoelectrically by a single stage, high efficiency cooler. To optimize cooling efficiency with minimum power and heat sink size requirement, the CCD sensor and cold side of the cooler are totally enclosed in the hermetically sealed enclosure as shown in Figure 3-8. Internal connections to the sensor are made with .002" diam. wire to minimize thermal conductive feedback to the sensor.

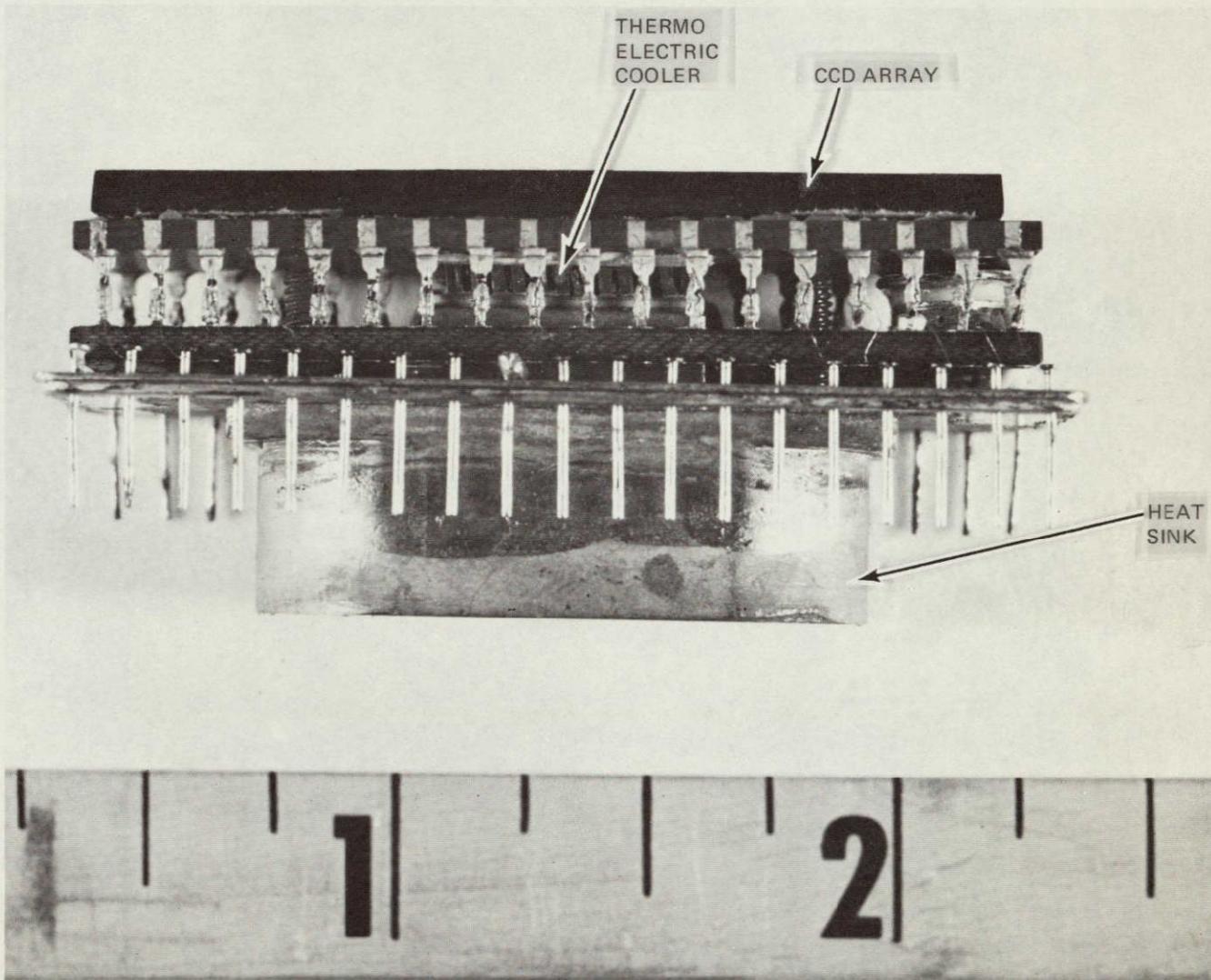


FIGURE 3-7. UNCOVERED CCD MODULE ASSEMBLY

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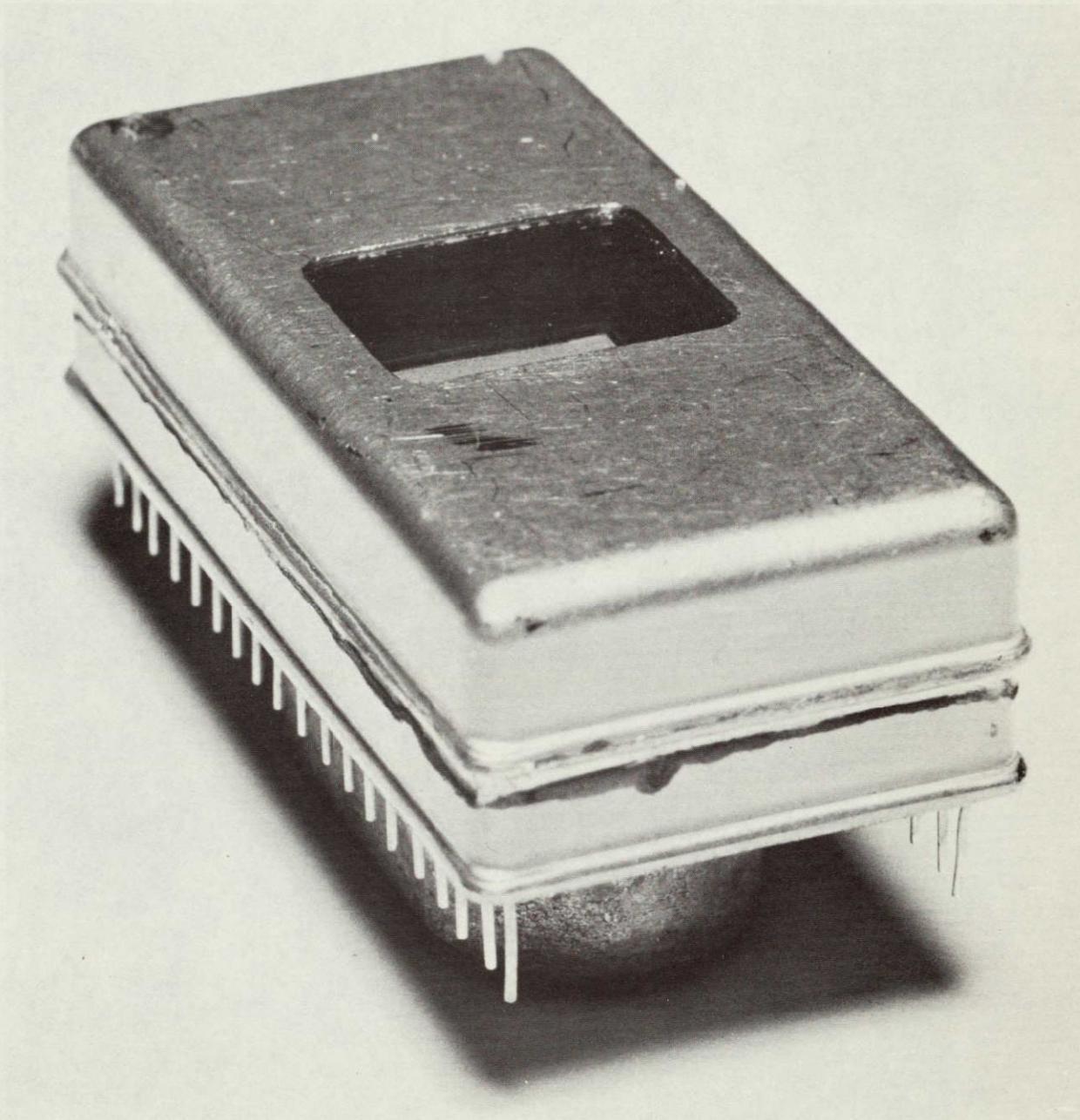


FIGURE 3-8. CCD MODULE ENCLOSURE PACKAGE

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A tiny thermistor, installed near the silicon chip provides temperature data while a miniature "Klixon" thermostat monitors the cooler's operation automatically at a desired temperature. To accomplish the sealed package arrangement, a copper heat sink block is hermetically soldered to a 40 pin header with the block protruding through a center opening of the header. The hot side of a single stage thermoelectric cooler (Borg Warner part #120-65) is soldered on the protruding surface of the copper block. The cold side of the cooler is in good thermal contact with the base of the CCD with a judicious application of thermal grease. Pressure is applied to this interface with two screws pulling the sensor against the cooler through an intermediate pad previously soldered to the sensor's pins.

A standard type cover, provided with a sealed optical window, hermetically encloses the sensor when soldered to its mating header in vacuum.

Condensation on the windows of sensor is avoided by totally isolating and sealing the cold sensor from the outside environment.

This arrangement provides an integral sensor and cooler package which plugs into a circuit board and at the same time mounts onto a heat sink structure which fits the camera configuration.

3.3.2 Array Board (Figure 3-9)

The array board is a circular printed circuit board which is located in the cylindrical portion of the camera between the lens and the main circuit board compartment. This board accepts the plug-in hermetically

sealed array assembly. The circuit board contains the decoupling networks for the CCD array supply voltages and also has an emitter follower stage to drive the video coax line. The circuit board has jumper provisions to allow the CCD to operate with either the GCI or the SFGA on-chip video amplifier.

3.3.3 Video Board (Figure 3-12)

The video board is one of the four circuit boards located in the main circuit board compartment and contains the circuits to amplify and process the video signal into a composite video signal which conforms to EIA-RS170 format. The board contains a FET gate to gate-out the large signal excursions during the inactive video time. This is followed by a low pass filter which attenuates the clock component of the video signal. An AGC stage is then followed by a fixed gain stage which provides a signal level of approximately 2.5 volts P-P to the processor stages. The processor contains a driven black clamp stage, a blanking adder, a gamma corrector, a sync adder, and an output stage. The average level of the video signal from the LP filter is amplified, clamped, peak detected, amplified, and provides the Automatic Light Control drive to the black spot iris of the lens.

The video amplifier has a provision to operate either the AGC mode or the manual gain control mode. The manual gain control is accomplished by connecting terminal X1-4 on the video board to ground and applying a variable d.c. voltage of +10V. to +7V to terminal X1-1.

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3.3.4 Sync and Logic Board (Figure 3-11)

The sync and logic board provides all the TV timing signals and all the logic signals for the CCD array. A crystal oscillator at 14.31818 MHz is divided by 2 to produce the 7.159 MHz clock signal. The oscillator frequency is divided by 7 to produce the 2.04545 MHz signal to the sync generator. A LSI sync chip develops all of the TV waveforms in accordance to EIA-RS 170. Counters gates, flip-flops and buffers develop all the required logic signals for the CCD array.

3.3.5 Driver and Regulator Board (Figure 3-10)

The driver and regulator board contains the logic driver stages which provide adequate drive power to drive the capacitance of the CCD array electrodes. The regulator circuits on this board provide regulated and variable voltages to the driver stages so that amplitude and D.C. level of the logic signals may be adjusted to the proper level for the CCD array.

3.3.6 Misc/Control Board (Figure 3-13)

The control board contains the camera operating controls, the input and output connectors and some miscellaneous circuits. An ALC switch selects either automatic or manual mode of light control. A potentiometer provides the means of manually controlling the light level. An Exposure Mode switch selects either 1/30 or 1/60 second exposure time. An input power connector accepts the camera voltages from the power supply unit. Coax connectors are provided for video output, sync output and genlock input. The board also contains logic circuitry which permits the array to be clocked in the normal interlace mode per EIA-RS170 wherein the integration time is 1/30 second or to be clocked in a quasi-interlace mode where the integration time is 1/60 second.

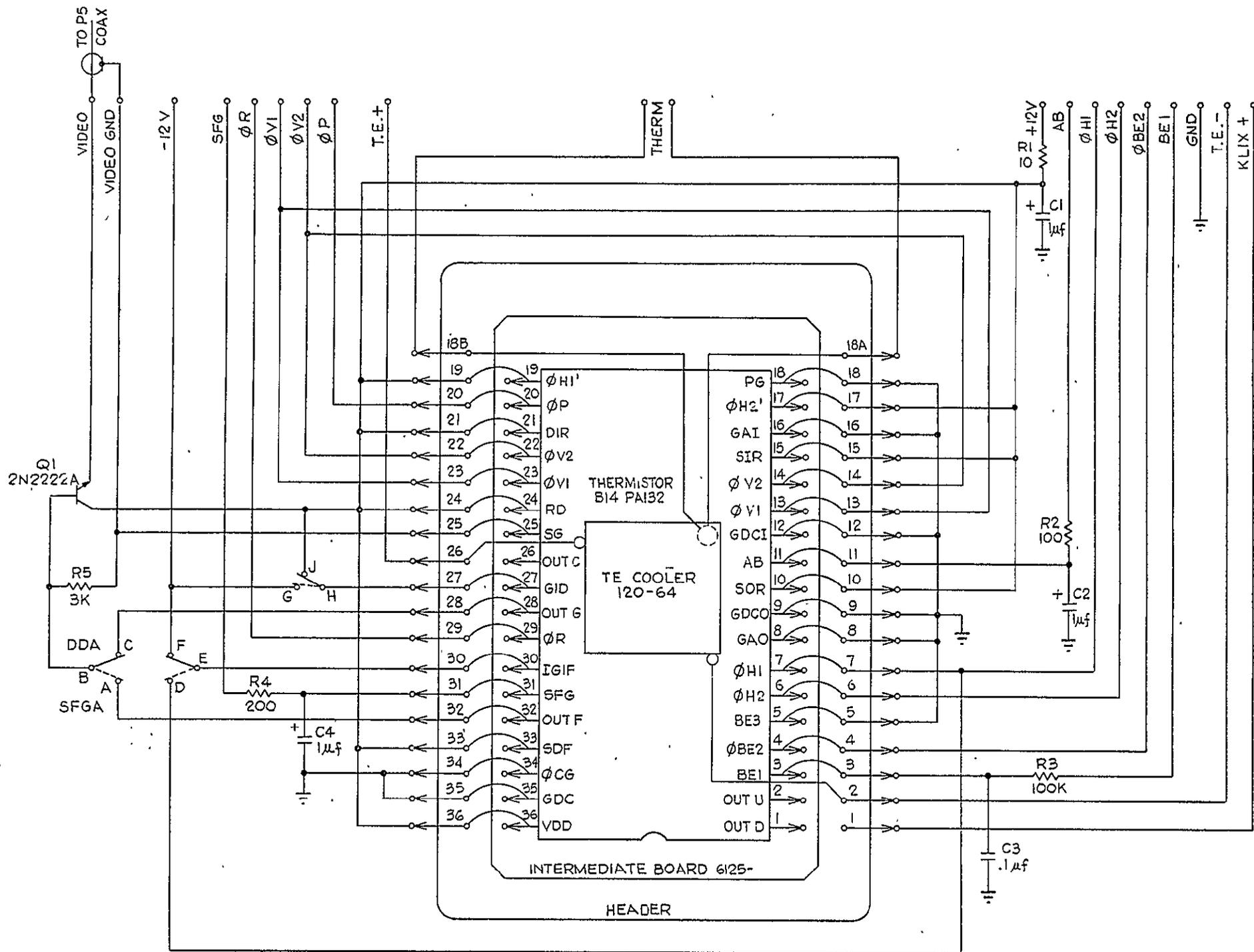


FIGURE 3-9 ARRAY BOARD

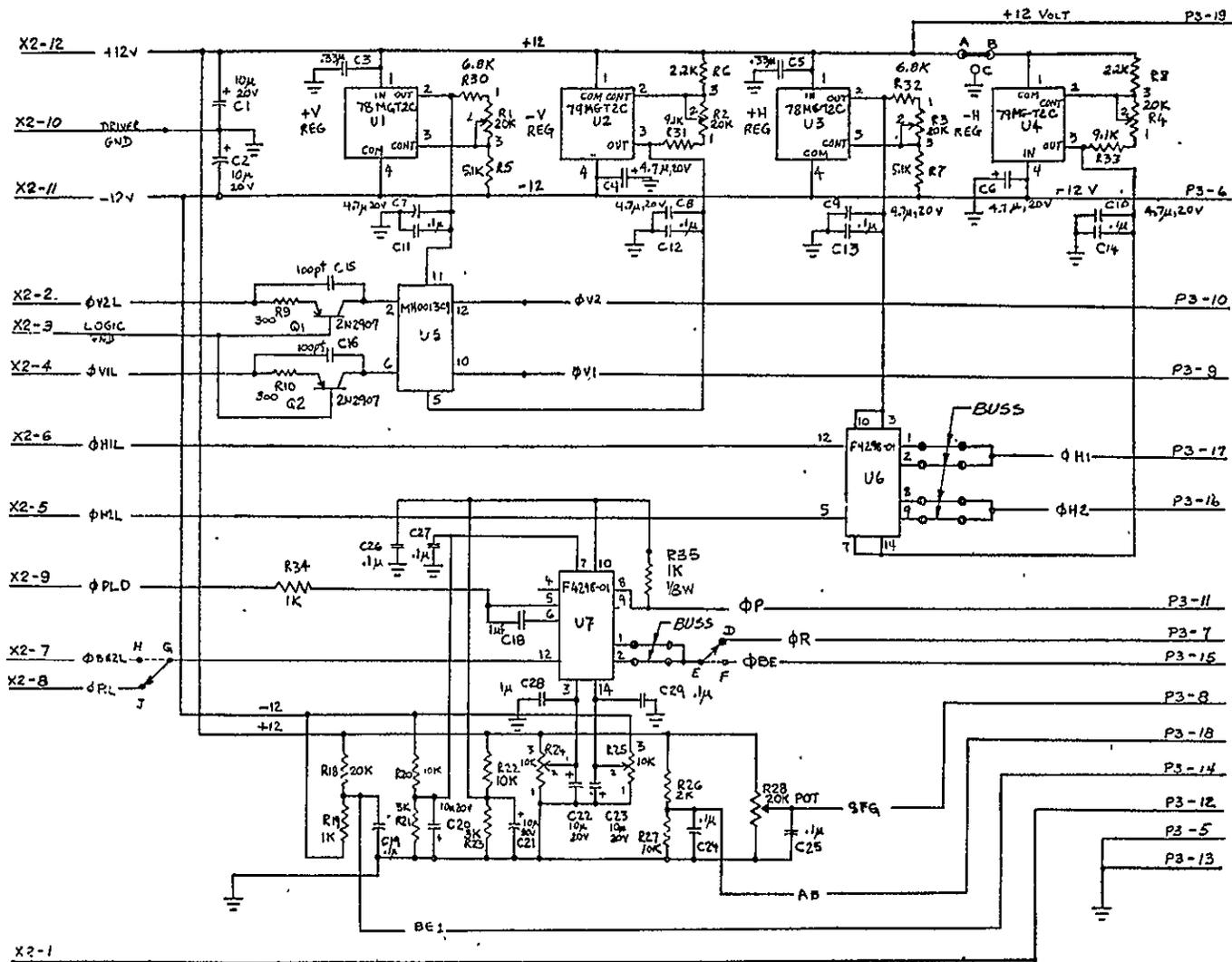


FIGURE 3-10. DRIVERS/REGULATOR BOARD

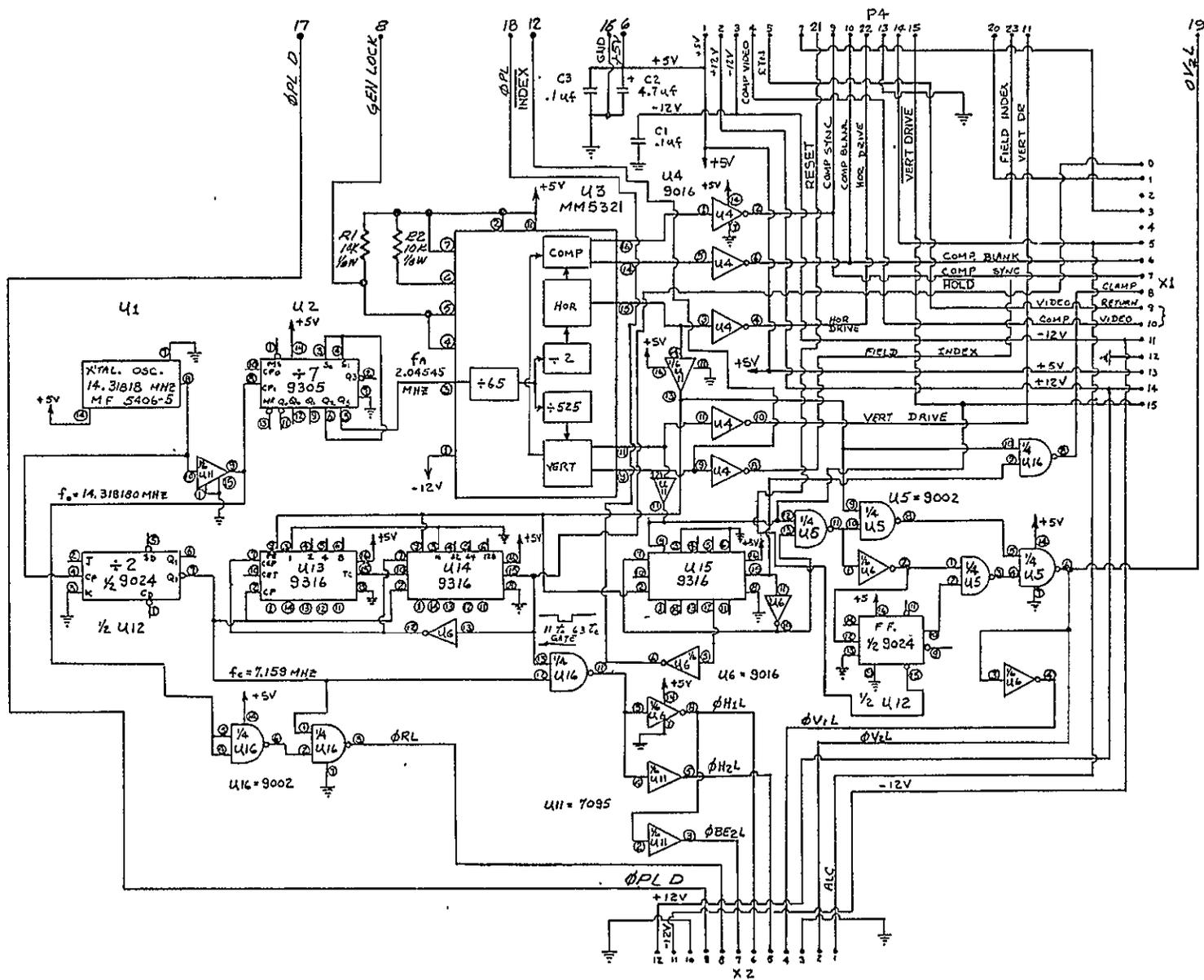


FIGURE 3-11 SYNC/LOGIC BOARD

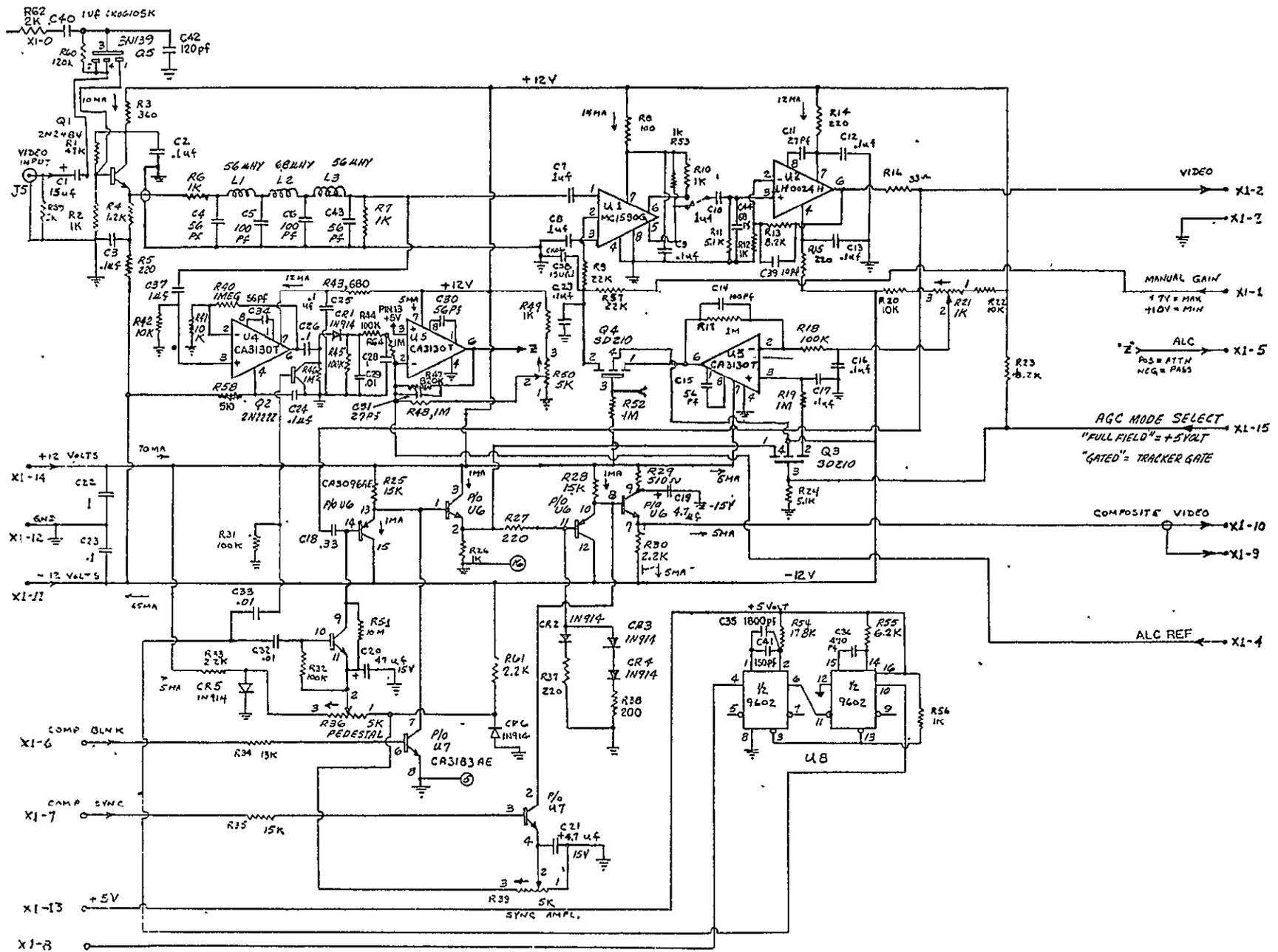


FIGURE 3-12 VIDEO BOARD

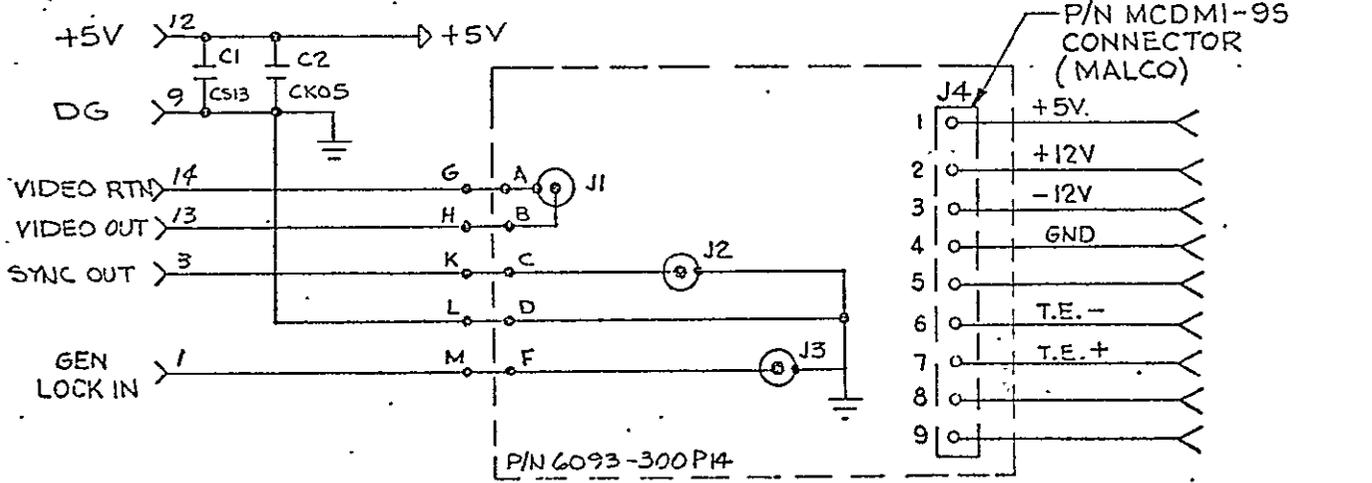
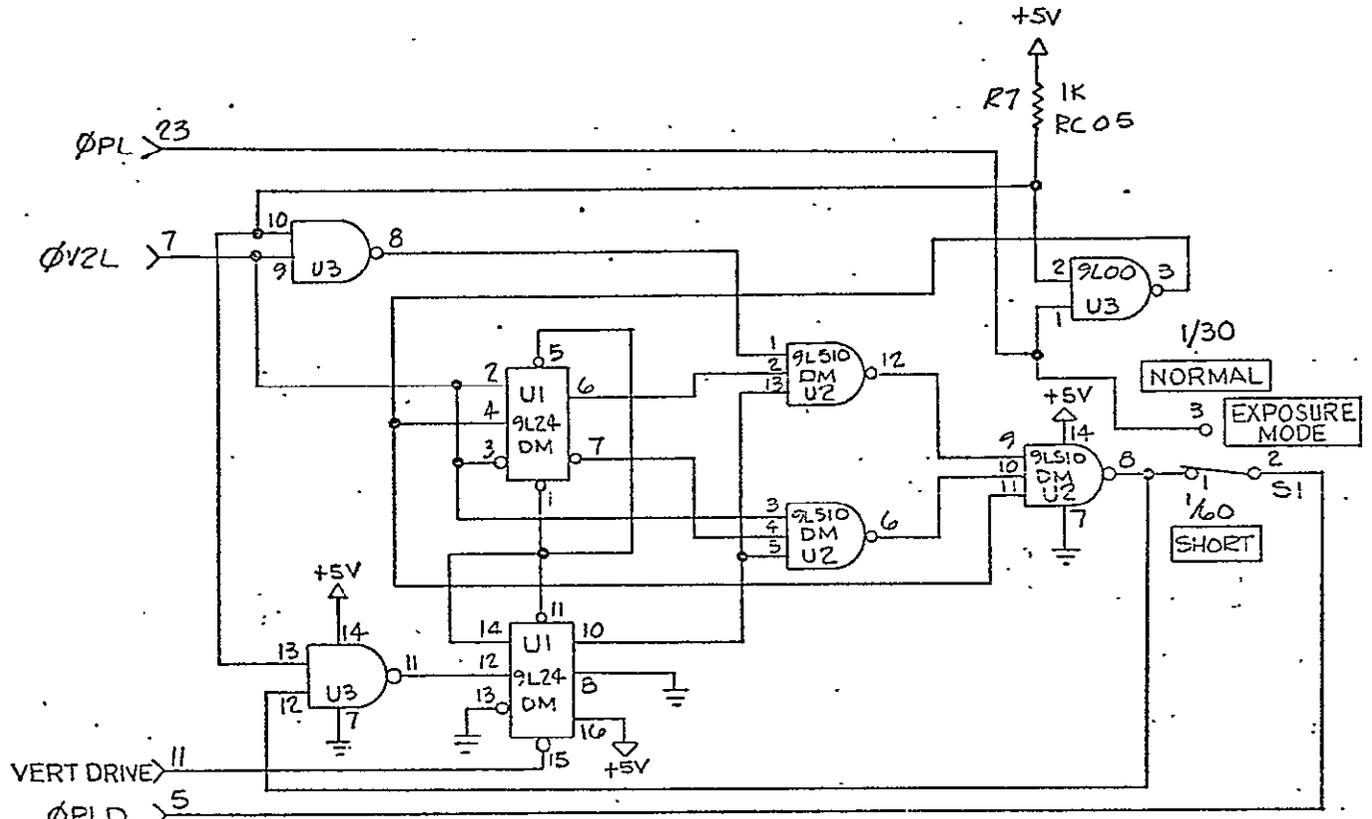
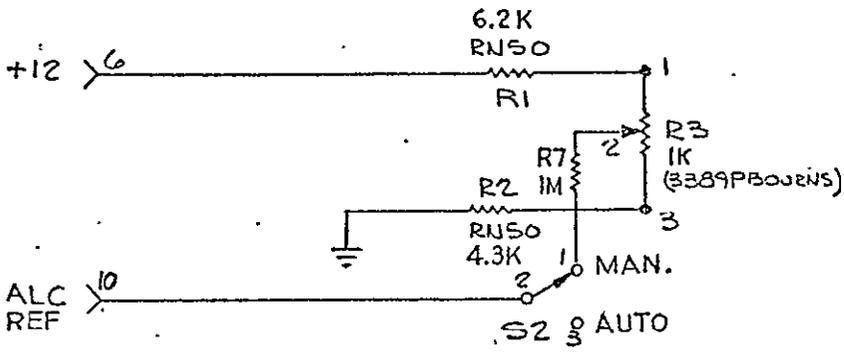


FIGURE 3-13 MISC/CONTROL BOARD

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4.0 ACCEPTANCE TEST PROCEDURE

The purpose of this Acceptance Test Procedure (ATP) is to demonstrate that equipment supplied by the Fairchild Imaging Systems Division (ISD) is suitable for use as a Solid State Television Camera System as defined by the requirements of Contract No. NAS 9-14844.

The test equipment to be used to verify the performance of the television camera system components is shown in Table 4-1.

The equipments comprising the complete solid state television camera assembly are:

- . One (1) Camera Head Unit
- . One (1) Lens, 25mm F.L., "C" Mount type,
Cosmicar Model B2514
- . One (1) Power Supply Unit

Prior to the Acceptance Test procedure, the serial numbers of the equipments are recorded on the data sheets. The data sheets, which are keyed to the numbering system of the procedure, are shown in paragraph 4.9. of this section.

TABLE 4-1

REQUIRED TEST EQUIPMENT

- a. Simpson Meter Model 260
- b. CCD Resolution Test Target, 4 x 3 aspect ratio, TP #1
- c. Logarithmic Gray Scale Test Target, TP #2
- d. Spatial frequency Test Target, TP #3
- e. Spectra Brightness Meter, Mod 15025-UB
- f. Power Supply, D.C., Power Designs Model 5015S, or equivalent
- g. Oscilloscope, Fairchild Model 766H, or equivalent
- h. Neutral Density Filters, N D 1.0, ND 2.0 and ND 3.0
- i. Tele-Measurement Light Box, Mod TELE-PAT III
- j. Test lens, C-mount type, 25mm f1.4-f22
- k. Display Monitor, Conrac Model DZA 14, or equivalent

The following tests shall be performed while the television system is in a normal operating mode except where otherwise noted.

4.1 SYSTEM INTERCONNECTION

See System Block Diagram, Figure 4-1.

4.2 LIGHT LEVEL CALIBRATION

- a. Replace the Auto-Iris camera lens with the 25mm test lens.
- b. Adjust the voltage input to the light box to obtain approximately 500 f1 highlights with the test patterns in position. Record reading on the data sheets.
- c. Place the ND2 filter in front of the test lens. Set the iris at f/4. Adjust camera alignment and lens focus until the test pattern image (TP#1) just fills the full width of the unblanked display raster. Adjust the lens iris to approximately one f stop below CCD saturation. Record f stop setting on the data sheets.
- d. Compute sensor highlight illumination I_H from the formula:

$$I_H = \frac{B \times 0.8}{4f^2} \quad (fc)$$

where B is the TP highlight value, f is the f-stop value. Record the computed I_H value for one-stop below saturation on the data sheet.

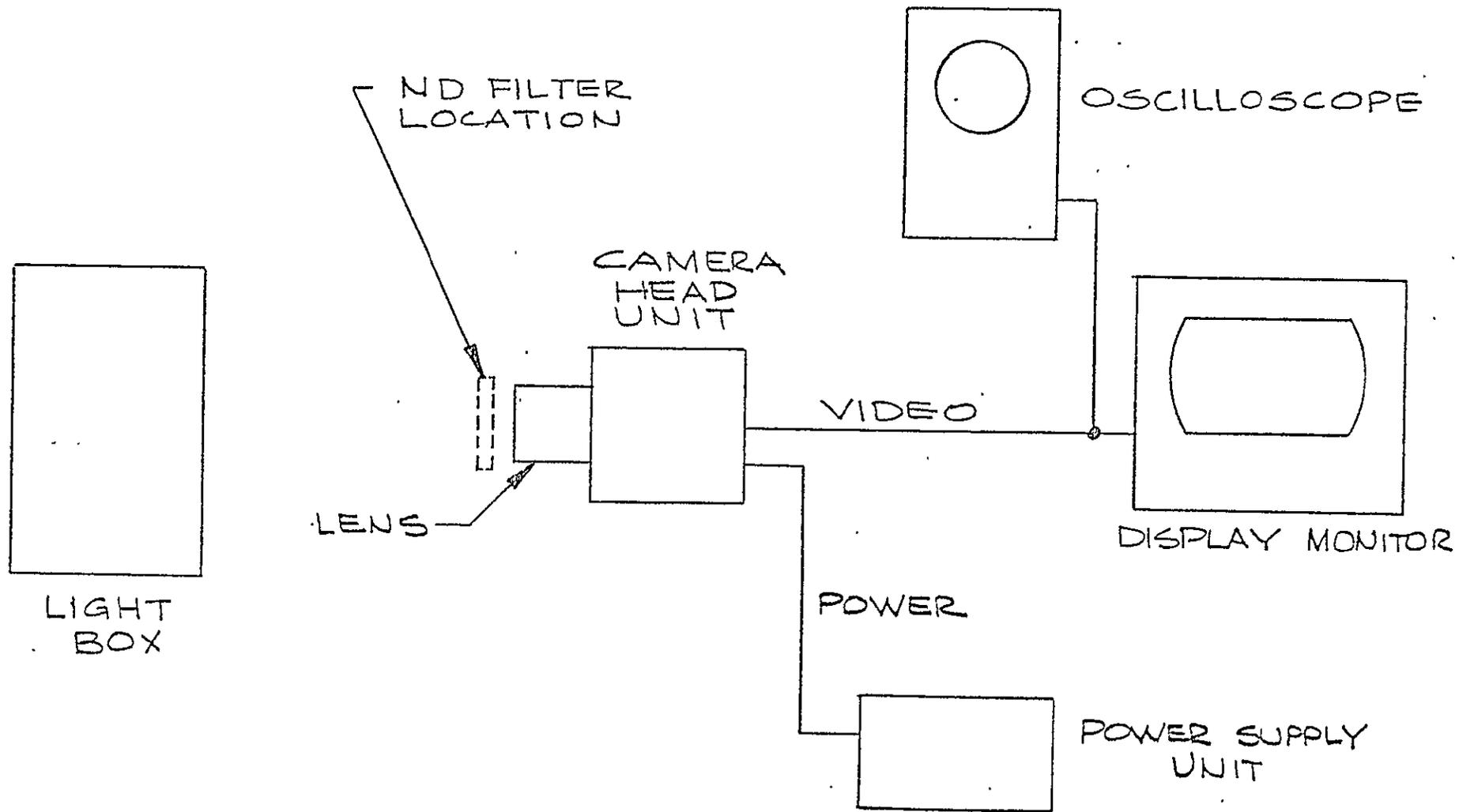


FIGURE 4-1 . SYSTEM BLOCK DIAGRAM

- e. Compute the f-stop value required to achieve $I_H = 5 \times 10^{-2} f_c$ at the sensor faceplate with the ND2 filter in front of the lens. Adjust "B" value of light box if necessary. Record the computed f-stop value and the corresponding "B" value on the data sheet.

With the light calibration condition defined by 4.2 (e) above, and with the camera viewing TP #1, adjust camera alignment and lens focus until the right and left edge marks just touch the corresponding edges of the unblanked display raster. (Figure 4-2)

With conditions as described in 4.3 above, the top and bottom edge marks shall coincide with the top and bottom edges of the unblanked scanning pattern within less than 24 scanning lines. Check on data sheet.

With conditions as described in 4.3.1, the horizontal resolution shall exceed $0.7 \times 285 = 200$ TV lines/picture height. The vertical resolution shall exceed $0.7 \times 488 = 342$ TV lines/picture height. Record observed values on data sheet.

Remove TP #1 and insert the spatial frequency test pattern, (Fig.4-3),

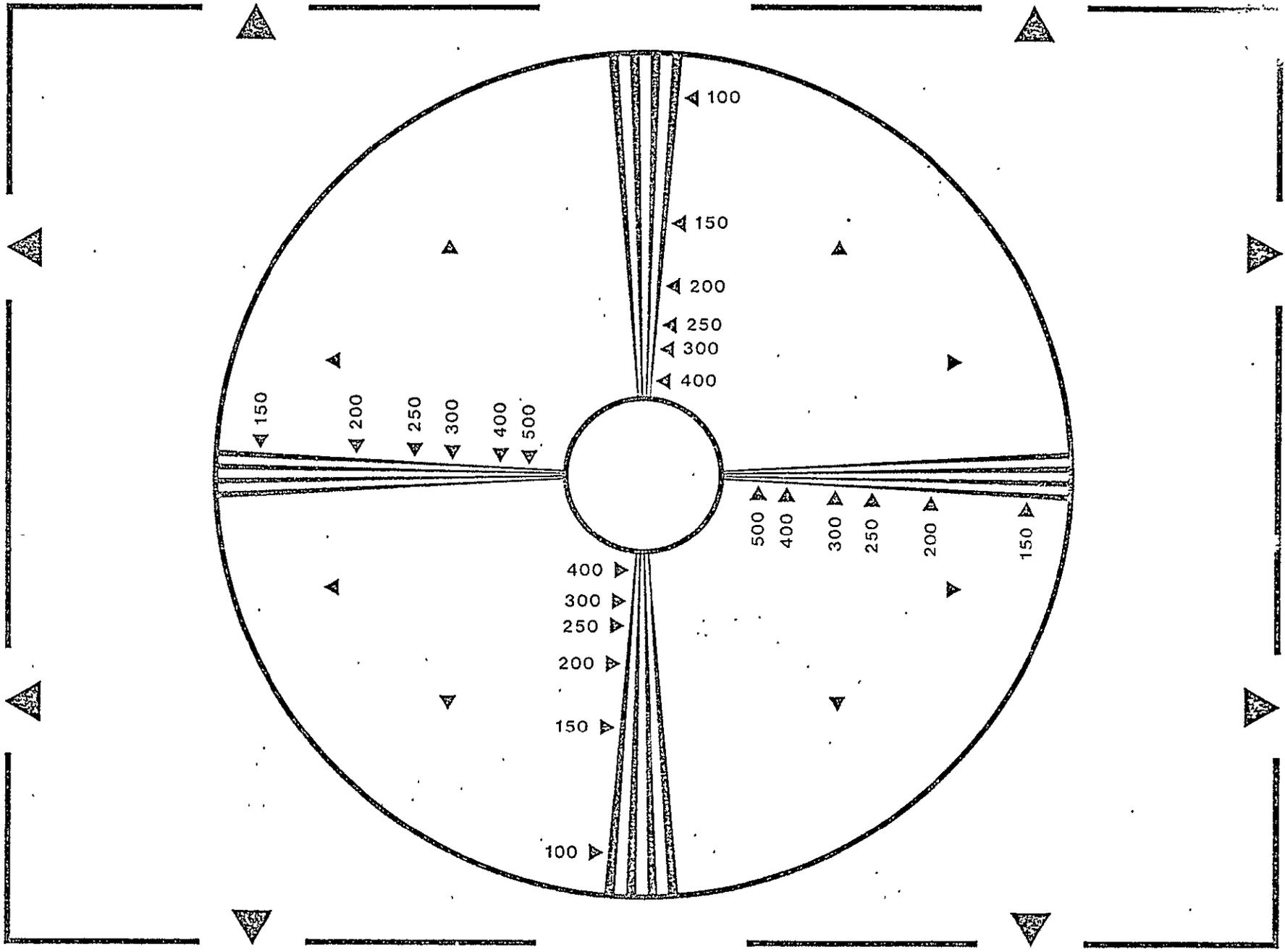


FIGURE 4-2 CCD RESOLUTION TEST TARGET TP #1

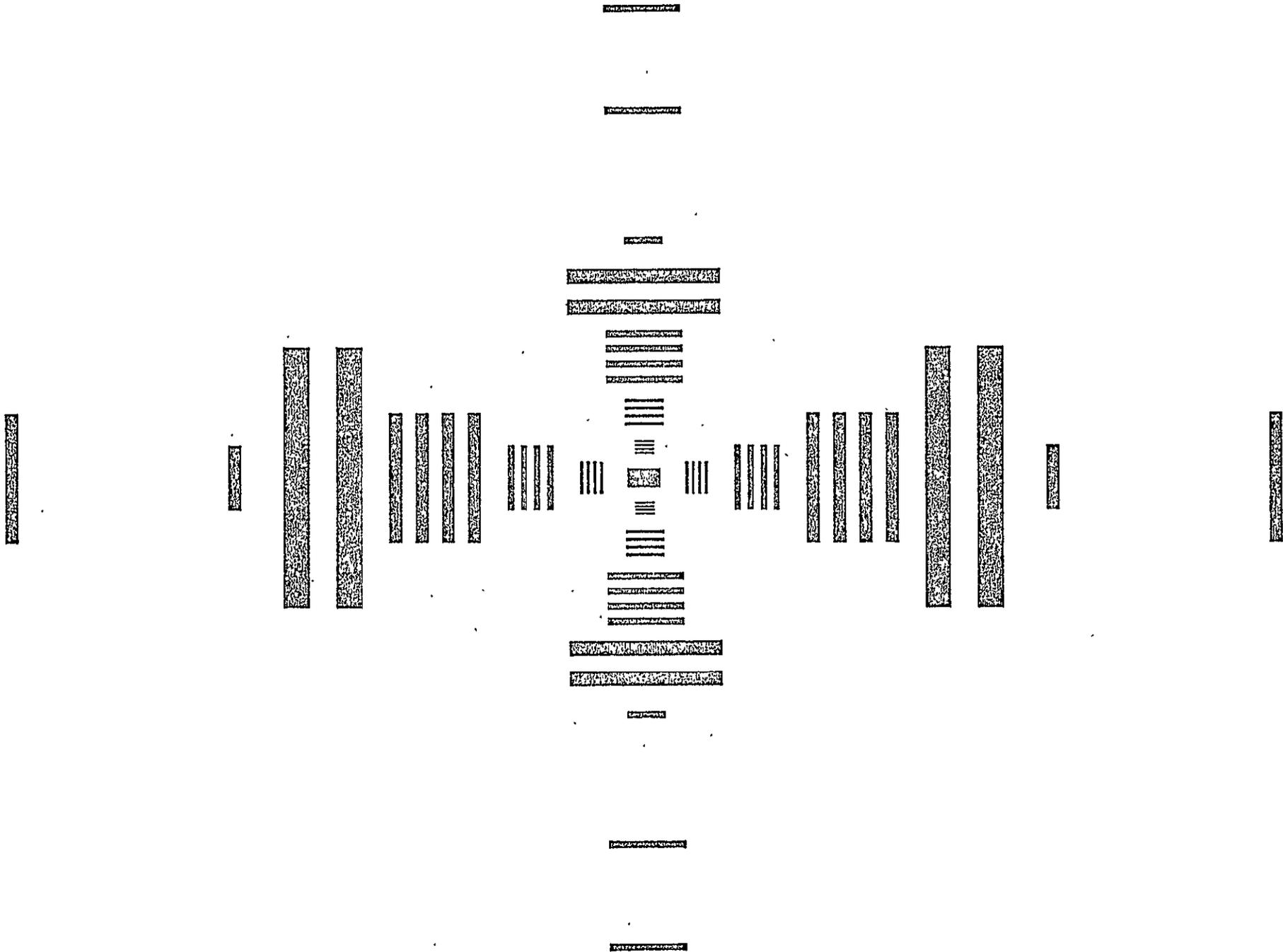


FIGURE 4-3 SPATIAL FREQUENCY TEST TARGET TP #3

TP #3, in the light box. Adjust camera alignment and focus to achieve optimum alignment and phasing conditions for the smallest (Nyquist-limit) test bar groups. Use the oscilloscope to view a single line of output video containing test bars at 1/8, 1/4, 1/2 and Nyquist-limit horizontal resolution. Photograph the scope display and attach copies to the data sheets.

With the sensor face uniformly illuminated at the level defined by light calibration condition 4.2 (c), locate spots and blemishes by observing the monitor display. Measure amplitudes using the oscilloscope in the line select mode.

A spot or blemish is defined as a video signal transition equal to or greater than 7% of the CCD sensor saturation signal, observed with the sensor uniformly illuminated at a level corresponding to 50% saturation. The size of a spot or blemish shall be determined by counting the number of scan lines on which the transition occurs; i.e., the number of lines per frame on which the transition is greater than 7% of saturation signal.

The total number of white and dark spots shall be less than or equal to:

- 10 spots over 1 but less than or equal to 4 TV lines/frame.
- 2 spots over 4 but less than or equal to 8 TV lines/frame.
- 0 spots over 8 TV lines/frame.

No horizontal or vertical black lines resulting from a failed CCD element shall be allowed.

Record the total number of spots and blemishes in each of the above categories on the data sheets.

4.4.1

SHADING

With conditions as defined in 4.4, verify that shading signal variations along any line, averaged over sections of 10% picture width, do not exceed 10% of the CCD saturation signal. Check on data sheets.

4.5

GRAY SCALE AND SIGNAL-TO-NOISE RATIO

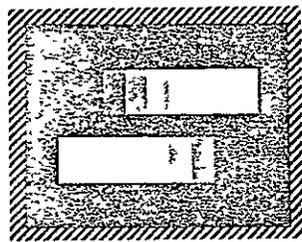
Insert the gray scale pattern, TP #2, in the light box. (Figure 4-4) With the sensor illumination conditions as defined by 4.2 (e), verify that ten gray scale steps can be resolved on the monitor display. Check on data sheets.

4.5.1

SIGNAL-TO-NOISE RATIO

While the camera system is operating as defined in 4.5 above, use the oscilloscope in the line select mode to determine the peak-to-peak signal, V_{p-p} , corresponding to maximum white to minimum dark signal. Record value on data sheets. Without changing camera operating conditions, increase scope gain to observe peak-to-peak temporal noise variations, N_{p-p} at the dark level signal. Verify that the signal-to-RMS noise ratio, as defined by:

TELE-MEASUREMENTS TM-315 PRECISION GRAY SCALE



8" X 10"

FIGURE 4-4. LOGARITHMIC GRAY SCALE TEST TARGET

4.5.1 SIGNAL-TO-NOISE RATIO (Cont'd.)

$$\text{SNR} = 20 \log \left(\frac{6V_{p-p}}{N_{p-p}} \right),$$

is less than 35db. Record observed values on data sheets.

4.6 DYNAMIC LIGHT RANGE

Remove the test lens and install the Auto-Iris lens assembly. Focus and align the camera to view TP #2, with the light box adjusted to provide approximately 500 fl highlights. Verify that useful imaging quality is observed, with the output video signal maintained constant within $\pm 3\text{db}$, over an illumination range of 1000:1 as determined by placing ND 1, and ND 2 and ND 3 filters in front of the lens aperture. Check on data sheets. Photograph display monitor image quality with and without the ND 3 filter in front of the lens. Attach photographs to data sheets.

With no ND filters in front of the lens, adjust the intensity of the light box by varying input voltage. Gradually reduce light box intensity until five gray scale steps are just discernible on the monitor display. Measure the highlight level of the test pattern corresponding to five gray step camera performance and record value on data sheets.

4.7 OUTPUT VIDEO FORMAT

With the camera operating as in 4.6, mount the ND 2 filter in front of the lens. Using the oscilloscope examine the output composite video waveform. Verify the following:

Composite Video polarity Black Negative

Blanked picture signal, with setup 0.714 \pm 0.1V
(nominally 100 IRE units)

Sync signal (from OVDC, Ref.) 0.286 ± 0.05V

Setup, blanking level to reference 7.5 ± 5
black level, (IRE units)

Record observations on data sheets.

Examine the sync signal and verify that the H and V blanking periods and waveforms conform with EIA RS-170 specifications. Check on data sheets.

Using a Simpson meter Mod No 260, measure the camera power supply input voltage. The reading shall be +28 VDC ± 4 VDC. Verify camera system operation with supply variations from 24V to 32V. Check on data sheets.

The acceptance test was performed on the deliverable prototype camera system (camera, lens, and power supply) S/N 001. The results were recorded on the data sheets shown following this page.

NASA/JSC SOLID STATE CAMERA SYSTEM
PREDELIVERY ACCEPTANCE TEST DATA SHEETS

3.0 CAMERA SERIAL NUMBER 001LENS SERIAL NUMBER 001POWER SUPPLY SERIAL NUMBER 001

4.2 LIGHT LEVEL CALIBRATION

(b) Test Pattern Highlight Brightness: 500 fL(c) "f" number for one stop below saturation: f 5.6(d) $I_h = \frac{B \times 0.8}{4f^2 \times 100} = \underline{.032}$ FT.C. (1 stop below saturation)

(e) $f = \sqrt{\frac{B \times 0.8}{4 \times 5 \times 10^{-2} \times 10^2}}$

for B = 400

$f = \sqrt{16} = 4$

4.3 ASPECT RATIO & RESOLUTION

4.3.1 UNBLANKED VERTICAL SCAN ALIGNMENT

less than 24 scan lines 15.64 pass

more than 24 scan lines _____ fail

4.3.2 RESOLUTION

Horizontal Resolution 750 TVL/PH ≥ 200 Pass < 200 FailVertical Resolution 450 TVL/PH ≥ 342 Pass < 342 Fail

4.3.3 RESOLUTION RESPONSE

Test Conducted By H. Balopole
 Test Witnessed By J. Siquiri

Date 12-8-76

4.4 SPOTS AND BLEMISHES

Total number of white and dark spots greater in size than one scan line and with video signal amplitude equal to or greater than 7% CCD saturation signal:

1 over 2 but less than or equal to 4 TVL ; ≤ 10 pass
 > 10 fail

1 over 4 but less than or equal to 8 TVL ; ≤ 2 pass
 > 2 fail

0 over 8 TVL ; 0 pass
 > 0 fail

NOTE: Horizontal or vertical black lines are counted as blemishes in the size category equivalent in defect area to circular spots of the sizes indicated above.

4.4.1 SHADING

Shading signal less than 10% of CCD saturation pass

Shading signal greater than 10% of CCD saturation fail

4.5 GRAY SCALE

Ten gray steps discernible pass

Less than 10 steps discernible fail

4.5.1 SIGNAL-TO-NOISE RATIO

Peak-to-peak highlight video signal $V_{p-p} = \underline{76}$

Peak-to-peak temporal noise variations $N_{p-p} = \underline{.015}$

$$\begin{aligned} \text{SNR} &= 20 \log (6 V_{p-p} / N_{p-p}) \\ &= \underline{49.7} \text{ db} \end{aligned} \quad \begin{aligned} &\geq 35 \text{ db } \input checked{} \text{ pass} \\ &< 35 \text{ db } \input type{} \text{ fail} \end{aligned}$$

4.6 DYNAMIC LIGHT RANGE

Highlight video signal, NO ND, $V_0 = \underline{0.62V}$

Highlight video signal, ND1, $V_1 = \underline{0.60V}$

Highlight video signal, ND2, $V_2 = \underline{0.60V}$

Highlight video signal, ND3, $V_3 = \underline{0.59V}$

$V_1, V_2,$ and V_3 within $\pm 3\text{db}$ of V_0 ; ✓ pass

$V_1, V_2,$ or V_3 not within $\pm 3\text{db}$ of V_0 ; _____ fail

Five gray scale steps discernible with light box highlight at 12 fl.

4.7 OUTPUT VIDEO FORMAT

Composite video polarity, black negative ✓ pass

black positive _____ fail

Blanked picture signal with setup, $V_{pp} = \underline{.74}$ V; 0.614 to 0.814V ✓ pass

< 0.614 or > 0.814V _____ fail

($V_{pp} = 100$ IRE units)

Sync signal (from OVDC, R of) $V_s = \underline{.28}$ V; 0.236 to 0.336V ✓ pass

< 0.236V or > 0.336V _____ fail

Setup, blanking level to ref black level 7.5 IRE units; *

* Passes spec with 25% APL (average picture level)

7.0 to 8.0 IRE units ✓ pass*

7.0 or 8.0 IRE units _____ fail

Sync signal waveform per EIA RS-170; ✓ pass

_____ fail

4.8 POWER SUPPLY

Power supply input voltage 28 VDC

Camera system operates at 24VDC and 32 VDC ✓ pass

Camera system does not operate at 24 dc and 32VDC fail

4.9 BLOOMING

Detail of lamp and reflector observed with

lamp voltage at 120VAC

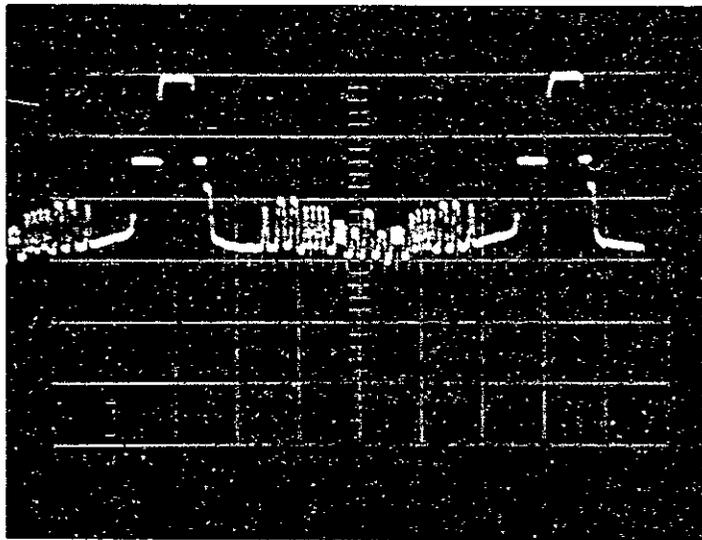
✓ pass

Details of lamp and reflector not

observed

 fail

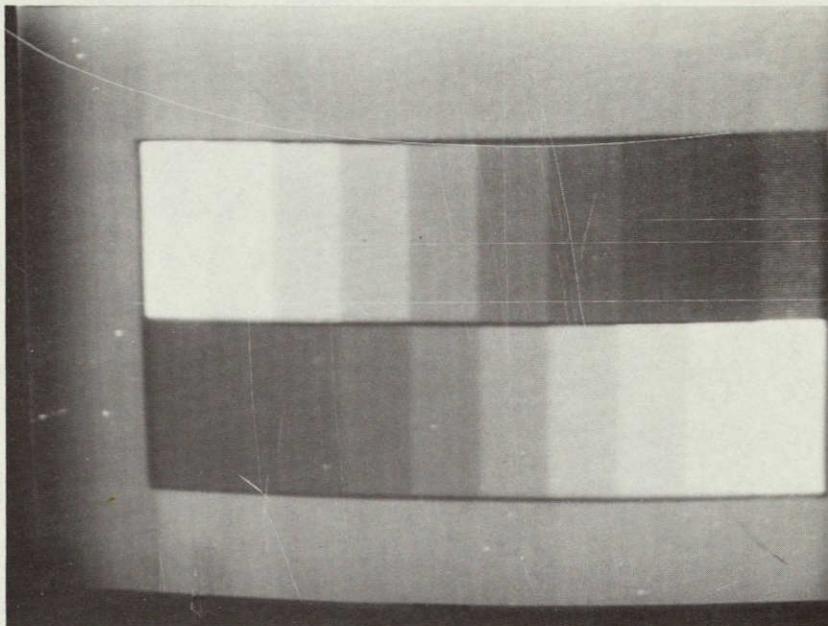
Peak lamp brightness 60K ftL



PARAGRAPH 4.3.3 RESOLUTION RESPONSE

FIGURE 4-5.

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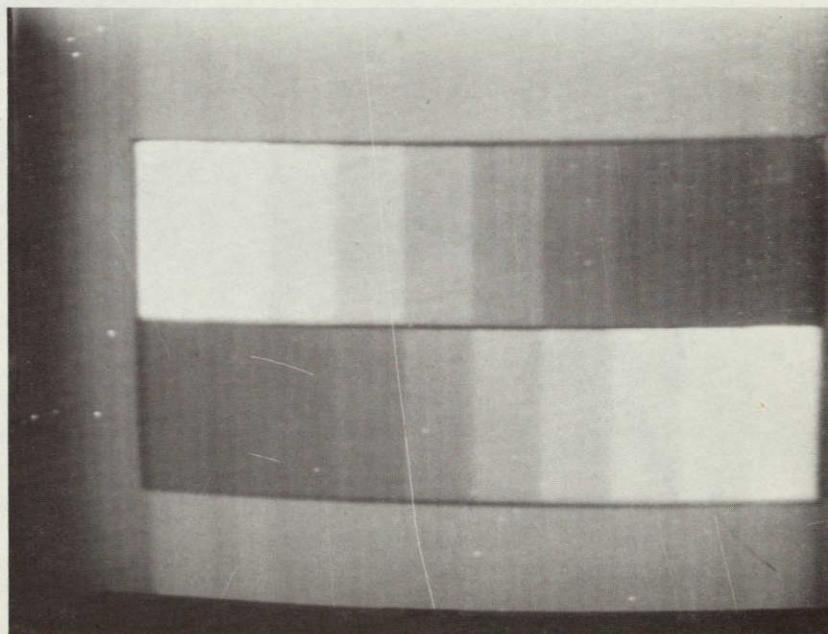
PARAGRAPH 4.6 DYNAMIC LIGHT RANGE

HIGHLIGHT = 500 FT. LAMB

LENS = f4

FILTER = N.D. 0.0

FIGURE 4-6.



PARAGRAPH 4.6 DYNAMIC LIGHT RANGE

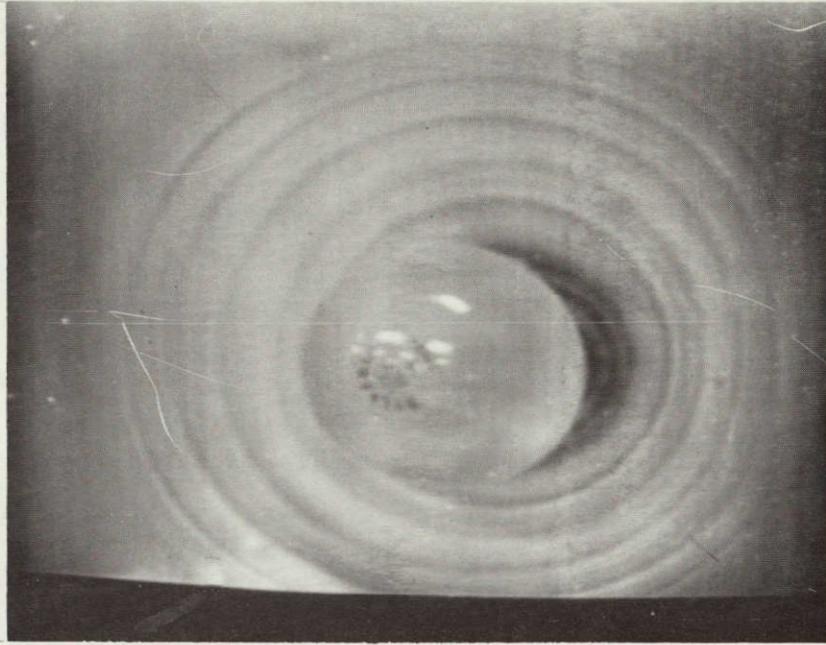
HIGHLIGHT = 500 FT. LAMB

LENS = f4

FILTER = N.D. 3.0

FIGURE 4-7.

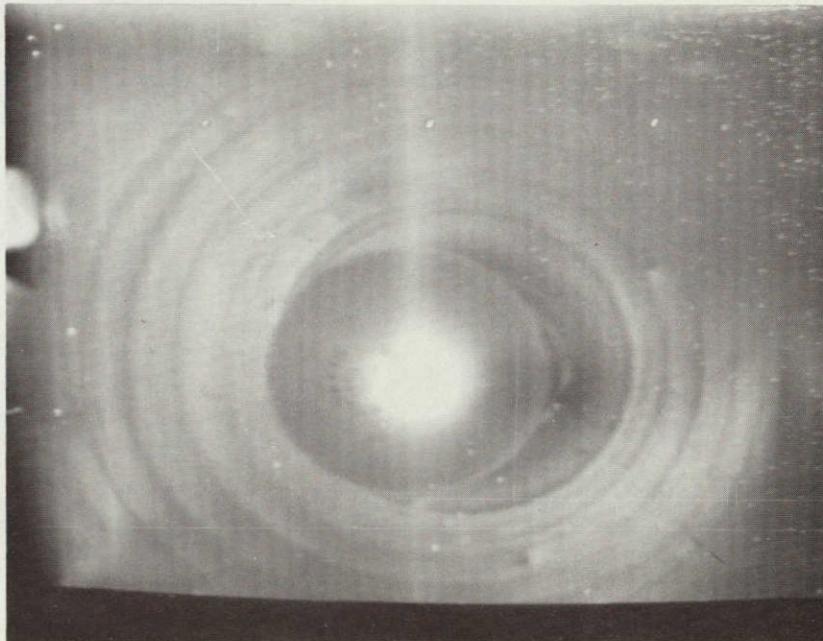
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PARAGRAPH 4.9 BRIGHTNESS OVERLOAD (BLOOMING)

NO LAMP VOLTAGE

FIGURE 4-8.



PARAGRAPH 4.9 BRIGHTNESS OVERLOAD (BLOOMING)

LAMP VOLTAGE = 120 VOLTS

FIGURE 4-9.

77P54

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5.0 RECOMMENDATIONS FOR FUTURE SSTV CAMERA DESIGNS

The work effort required to achieve program objectives resulted in the generation of several novel features which are expected to be useful in future SSTV camera designs. These features include:

1. The implementation of sensor temperature control by means of a modular subassembly which contains the CCD and thermoelectric cooler in a small hermetically-sealed enclosure. This implementation eliminates any requirement for pressurizing the camera housing when operating in humid environments.

2. The implementation of dual-mode clocking of the CCD array (ref. section 3.1A) which enables all sensor elements to be readout in either 1/60 or 1/30 second, while maintaining full compatibility with EIA RS-170 television system specifications.

3. Demonstration of feasibility for accomodating scene illumination range variations in excess of $10^6/1$ by means of combined ALC/AGC techniques.

During the course of program effort, particularly during the design, build and final test phase, it became apparent that there were several additional areas where design modifications could result in improved performance and/or smaller package size and reduced power consumption. Although schedule and funding constraints did not permit these modifications to be incorporated into the prototype, these items are worthy of consideration for inclusion in future SSTV cameras.

5.1 ALC-AGC-VIDEO CIRCUITS

The video amplifier design evolved in stages where additional requirements such as AGC and ALC were imposed as add-on modifications. As a result, some design compromises were

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necessary which could have been circumvented in a completely new design.

At present, the video signal is developed at the source terminal of the floating gate amplifier which is on the CCD chip. This signal goes to an emitter follower on the video amplifier board and then to a low-pass Nyquist filter into two paths (see figure 3-12). One path is through an AGC amplifier stage (U1) and then through an amplifier (U2) to the video processor stages (U6). The second path for the video is through U4 and U5 to provide the ALC signal. Although the AGC and ALC must function independently of each other, the video circuit could be simplified if a common fixed gain stage was first used to amplify the off-chip signal followed by a split into separate AGC and ALC paths.

Black level clamping is required in the video amplifier in order to establish a reference black level in the composite video signal. The present clocking logic for the CCD array provides an interval of 12 clock periods preceding each scan line which corresponds to a zero signal or "absolute black" reference level. Since this reference does not contain CCD dark current, there is an offset between reference black and scene black which varies in amplitude with array temperature variations. An additional offset of the black reference can occur when the CCD clocking signals are adjusted. A design modification for the CCD array is being evaluated to circumvent these problems. This modification provides six opaque photosites at the beginning of each line. Since the opaqued photosites contain samples of the array dark current, the present shifting of the black reference with temperature and clock adjustments should be eliminated.

Some applications of a TV camera encounter scenes with very low contrast and a complete absence of black or dark gray. In this case, the video signal appears as a small variation on a large pedestal corresponding to the background level. To improve contrast on the display monitor, it is desirable in this case to utilize the darkest part of scene video as the black reference. Such a feature can be included in the SSTV camera if viewing low contrast scenes is an important requirement.

5.2 SIZE, POWER AND CIRCUIT REDUCTION

Although the size of the present camera is relatively small and the power requirement is also low, further reductions are possible in both areas. The sync and logic circuits are an example where reductions are possible. The present circuit employs 12 DIPs and consumes approximately 1.8 watts. A newer design which is now being developed will consist of 4 DIPs and require only 0.4 watts. This modification, in combination with other circuit and packaging redesign efforts, can result in future SSTV camera electronic designs contained within a total package size of less than 250cc (16 cu. in.).

5.3 HIGH RESOLUTION AND COLOR SSTV CAMERAS

Multiplexed operation of two (or more) interline-transfer CCD image sensors is a potentially useful technique which has application in either monochrome or color TV cameras. An experimental camera system constructed as part of the CCD Sensor Development Program (NESC Contract #00039-73-C-0015) demonstrated horizontal resolution at twice the Nyquist-limit sampling frequency of a single sensor camera. This work supports feasibility for a multiplexed 380 x 488 element

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CCD TV camera design with 760 TVL/picture width resolution performance.

Although the aforementioned experimental camera was not specifically designed for color application, the multiplexing principles employed are clearly adaptable to future camera designs using multiple CCD arrays with red, green and blue channel filters in the optical path to derive scene image information suitable for forming into a NTSC-compatible color video signal. A problem area to be addressed during camera development is the attainment of adequate blue channel response, as may be achieved with modified sensor design, or by the use of image intensification principles prior to CCD readout.

APPENDIX

BURIED CHANNEL CHARGE COUPLED DEVICE (CCD) CONCEPT

The Fairchild design approach to the NASA/JSC requirement is based on the utilization of basic CCD sensor and camera design principles which fully address the requirement for compatibility with 525-line television standards. This section presents general background information concerning these principles.

CCD SENSOR

Charge-coupled image sensors integrate photon-generated minority carriers in depletion wells formed by the application of a bias voltage to elements of a control electrode (gate) structure overlaying photosensitive regions of the substrate. Following an integration period, the carriers are transported as individual signal packets by potential well motions induced by clocking the gate electrodes. After a sequence of transport steps determined by device organization, signal packets corresponding to element rows are serially shifted to an on-chip detector for conversion to an output video signal.

The cell organization of a CCD and the number of charge transport gates (phase lines) per cell, are of concern to the camera designer since precisely timed gate drive waveforms must be supplied to the device for self-scan operation. The interline-transfer (ILT) organization is used exclusively for the Fairchild family of area array CCD's, which includes designs with 100 x 100, 190 x 244 and 380 x 488 elements. These designs employ two-phase (2ϕ) charge transport principles which, in combination with the ILT organization, minimizes the number and complexity of gate drive waveforms necessary for device operation. In addition, these designs all utilize buried-channel charge transport principles. In a buried-channel CCD, the signal carriers are kept away from the silicon surface by an electrical field associated with an implanted layer of ions. Thus the trapping of carriers by surface states is inhibited resulting in high charge-transfer efficiencies which are essentially independent of the signal charge magnitude. For the 190 x 244 and 380 x 488 designs, buried-channel operation has been combined with on-chip low-noise floating-gate amplifiers. The combination of features extends the CCD performance range to threshold signal levels of a few tens of electrons per depletion well.

Figure 1 illustrates the ILT organization and the forcing-function inputs required for self-scan operation as a TV image sensor. The unit cells contain one photosensor site and an adjacent light-shielded site

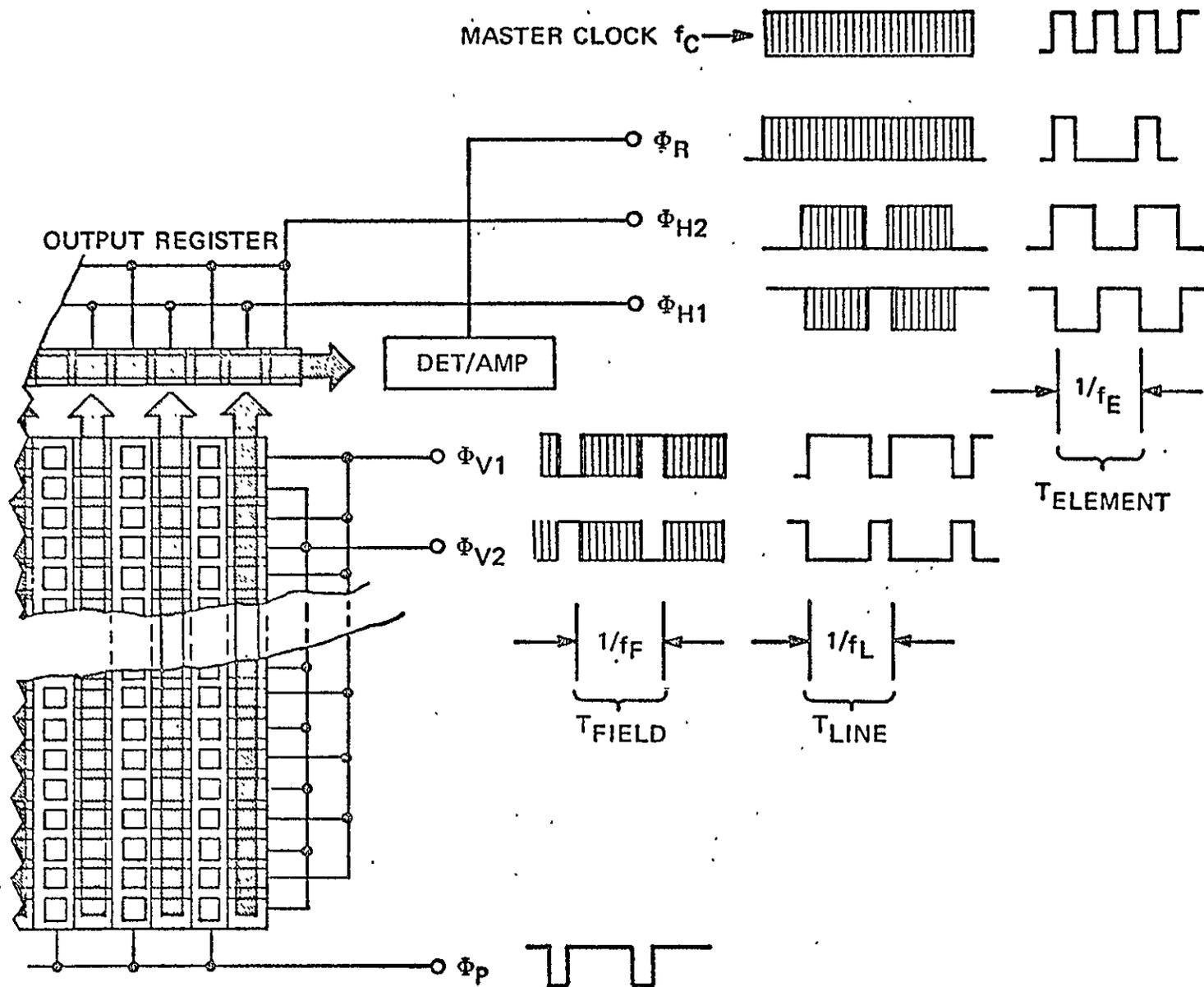


FIGURE 1

INTERLINE TRANSFER CCD ORGANIZATION AND DRIVE INPUT WAVEFORMS

which is one-half stage of a 2ϕ vertical-transport register. Cell dimensions are defined by comb channel stop boundaries on three sides of the photosite. Alternate cell rows are uniquely assigned to each of the two fields comprising a TV frame resulting in higher vertical MTF than for beam-scanned or frame-transfer type image sensors. An implanted potential barrier at the photosite/transfer site interface inhibits transfers to the vertical column register, except when the photogate (ϕ_p) is LOW and the adjacent transfer gate (ϕ_{V1} or ϕ_{V2}) is HIGH. Thus, 2/1 interlace readout is achieved by pulsing ϕ_p LOW during each vertical blanking interval and applying complementary ϕ_{V1} , ϕ_{V2} waveforms with HIGH states during alternate V-blanking periods.

At the start of the ODD field readout, elements corresponding to odd number rows are first shifted in unison into adjacent ϕ_{V1} sites for row transport along the column registers to the output register. The EVEN field sequence is similar except the initial shift is into ϕ_{V2} sites. Row transfers at the output register interface (for both ODD and EVEN rows) are effected by holding ϕ_{V1} LOW and ϕ_{H1} HIGH during the horizontal blanking interval. Complementary square-wave pulses at element rate are applied to the ϕ_{H1} , ϕ_{H2} transport gates to serially shift packets to the output detector.

CAMERA DESIGN FOR 525-LINE TELEVISION

Circuit functions for a TV camera using interline-transfer image sensors are illustrated in the block diagram, Figure 2. With the exception of the CCD and its associated gate drive waveforms, similar functions (plus horizontal and vertical scanning) are necessary for conventional camera designs using beam-scanned image sensors. A typical ILT-CCD camera logic design employs a crystal clock at frequency $f_C = 2f_E$, where f_E is the element readout rate, to provide decoding edges for pulses shorter in duration than an element period. All CCD gate waveforms, and the display sync and blanking signals, are derived from f_C by divide-down counters and combinational logic circuits.

A beam-scanned camera design requires relatively complex logic circuits to conform with 525-line TV system specifications such as EIA RS-170. In this case, the function of the logic is to synthesize synchronization and blanking waveforms with timing edges defined from the output of a master clock operating at a high multiple of the line scan frequency f_L . A typical single-chip MOS-LSI TV signal generator, such as the Fairchild type 3262, is controlled by a crystal clock operating at $910f_L$, facilitating the generation of a synchronous NTSC color subcarrier output at the nominal US Standard 3.58 MHz rate. Decoding edges for either monochrome or color system outputs are derived from an on-chip square wave clock at $130f_L$.

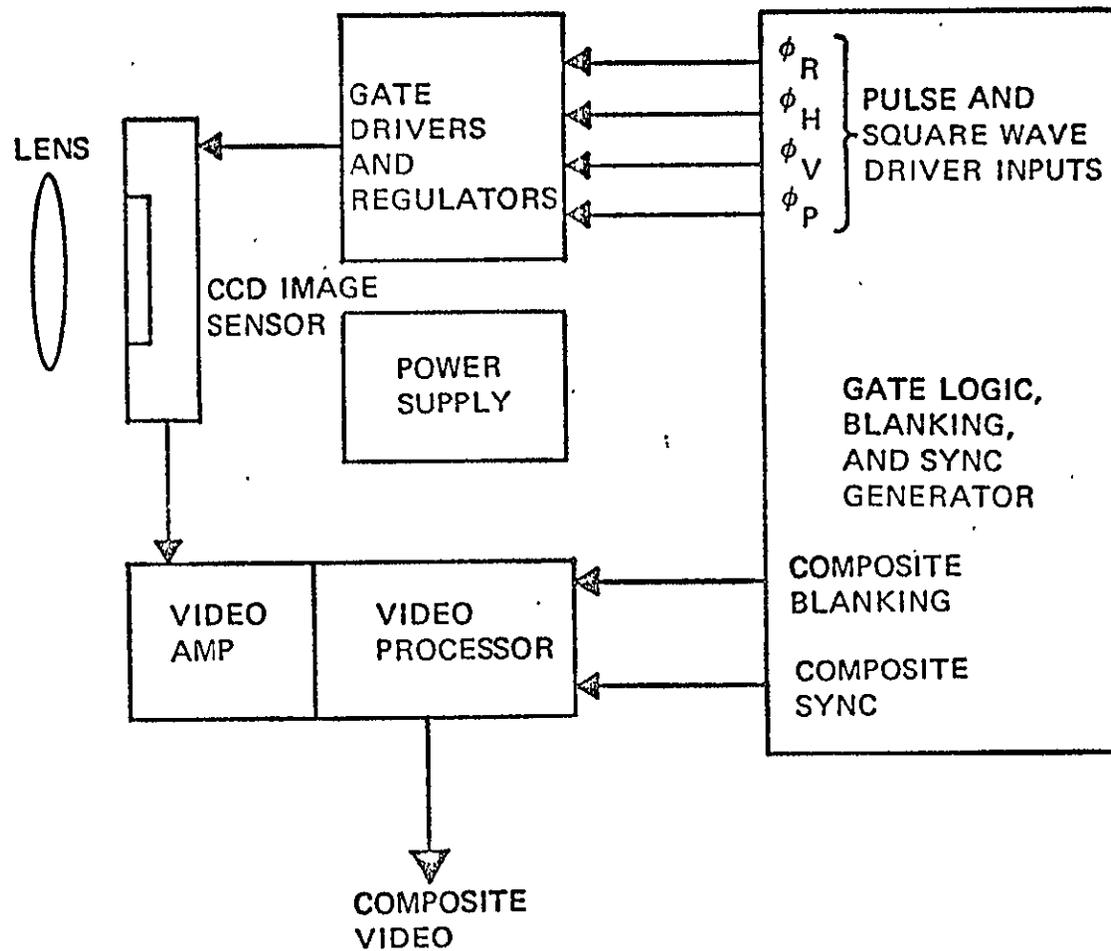


FIGURE 2

**FUNCTIONAL REQUIREMENTS FOR A CCD-TV CAMERA
UTILIZING AN ILT AREA IMAGE SENSOR**

Although existing waveform generators such as the 3262 do not provide CCD gate signal outputs, a modified CCD/RS-170 compatible design is feasible if the CCD design conforms to system specifications. For CCD imaging sensors, conformance implies a precisely defined number of readout lines per field. Also, if the CCD sensor element counts per line are properly defined, a simplified camera logic design using a single master clock input is possible.

In accordance with 525-line monochrome system specifications, the nominal values required for readout scan parameters are: line rate $f_L = 15,750$ Hz; field rate $f_F = 60$ Hz; and frame rate $f_R = 30$ Hz (with 2/1 field/frame interlace). The RS-170/3262 vertical blanking interval is $(20 + 22/130)$ line periods/field, defining a minimum of $(525-40) = 485$ active scan lines, hence sensor element rows per frame.

Horizontal blanking is defined as $(22/130)$ horizontal line periods, which is equivalent to: $(22/130)(n_A + n_B) = (22/130)n_T$ where n_A , n_B and n_T define the active, blanked, and total number of element periods/line period, respectively. If n_T is selected to be $910/2 = 455$, a single master clock can be used to satisfy the requirements for both RS-170 and CCD gate-drive waveform synthesis. For this condition, $n_B = (22/130) \times 455 = 77$, and $n_A = (n_T - n_B) = 378$. The CCAID-488 sensor has 380 elements/row, and 488 rows, hence a few terminal rows and columns can be blanked off when blanking signal edges are properly centered with respect to the active format region.